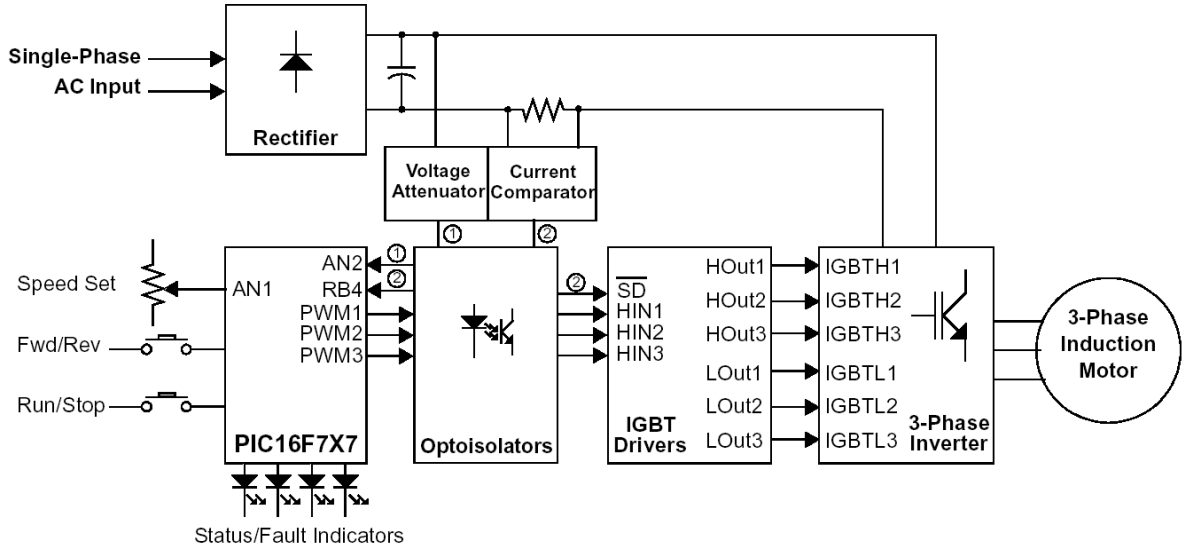
13 Switch-mode dc to ac inverters II

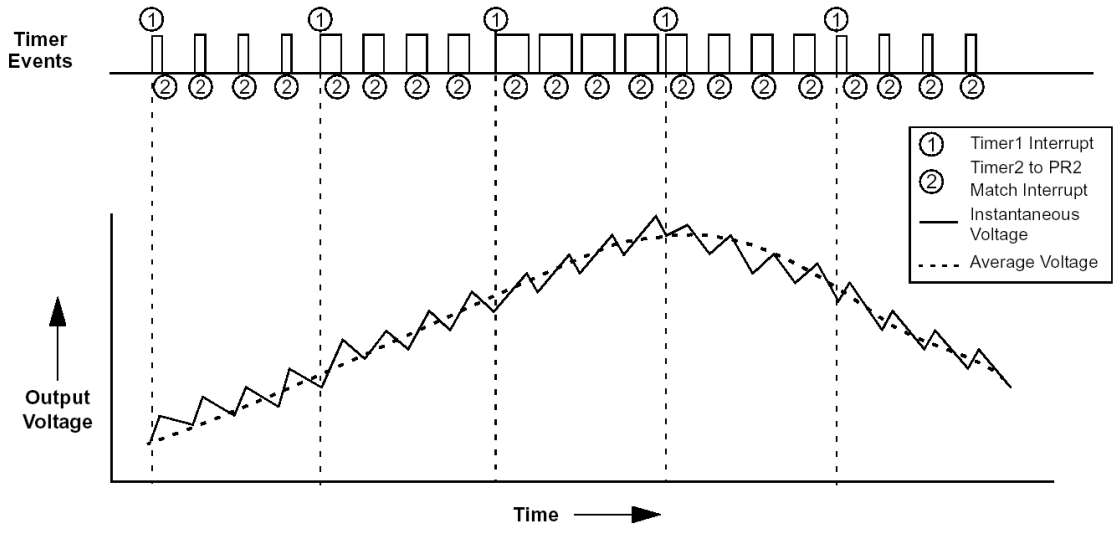
13.1 Variable Voltage Variable Frequency (VVVF) PWM

Very often, the frequency of the ac output should be varied as well as the voltage. This would be the case in an induction motor drive.



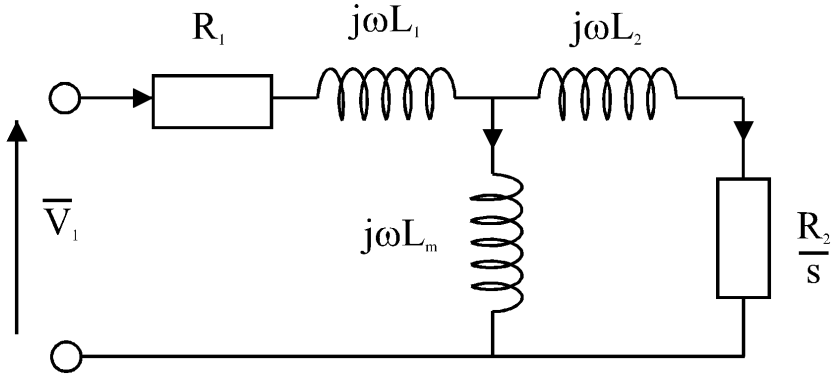
Induction motor drive demo using a PIC (Microchip AN889)

A variety of modulation strategies are possible. A simple strategy is 'naturally sampled'. This is produced in the same manner as in Lecture 12, but the integer ratio between the triangular (or sawtooth) wave and the controlling voltage is not maintained. Other schemes work hard to maintain the nice integer ratio, and have to adjust the frequency of the triangular waveform (the switching frequency). Some simplify it a little, e.g. Microchip AN889:



13.1.1 Practical considerations

If the load is a typical inductive load, the high frequency harmonics in the voltage waveform do not lead to large high frequency currents. Thus filtering at the load is not necessary. However, a problem arises in some cases. Consider the induction motor equivalent circuit:



Incomplete cycles of the carrier frequency within a complete cycle of the modulating frequency leave small portions of voltage varying slowly (the remainder of taking the integer ratio). These form "sub-harmonics" below the fundamental frequency. The motor impedance to these very low frequency sub-harmonics will be very low: (approximately R1 only). Thus high currents will flow and the drive and inverter damaged.

A high switching rate with naturally sampled pwm to reduces the amount of sub-harmonics in the inverter output waveform because the 'left over' voltage components are extremely small. The cost is higher switching losses.

13.1.2 Harmonic elimination

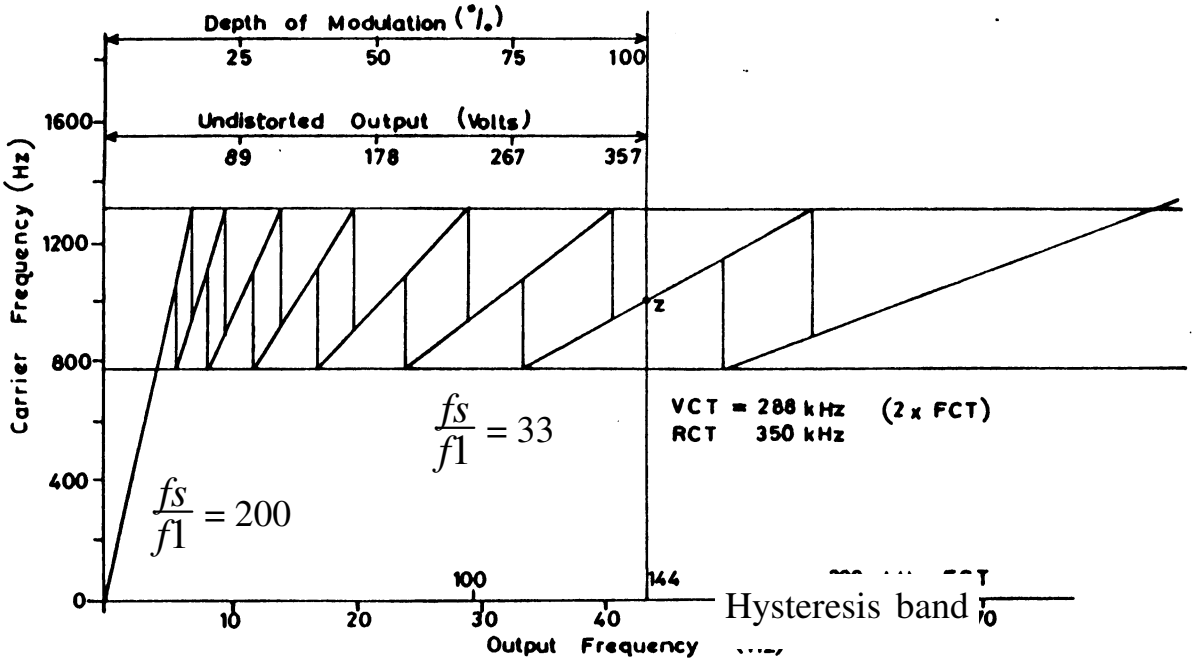
Precalculated switching waveforms with integer m_f , the harmonic elimianation method is intended specifically to ensure that there are no sub-harmonics and to keep a low switching frequency in the inverter. Only some harmonics above the fundamental will be removed.

The first version of this is the classic 'quasi-square' line voltage which eliminates the thirds. Further harmonics can be eliminated by adding more switching to the waveforms. It is usual to eliminate 5^{ths} and 7^{ths}, as well, leaving only 11, 13 etc. This is excellent for a large induction motor drive, which has a high impedance to the higher harmonics

13.1.3 Gear changing in pwm waveforms

To maintain an odd integer multiple of three number of switching cycles while the modulating waveforms are continuously variable requires a continuously variable switching (carrier) frequency. Using a single fixed ratio presents problems with the filtering as the harmonics will move as well as the fundamental. To overcome this and keep the switching frequency within a reasonable range, a form of gear changing is used.

The Philips HEF4752 three phase pwm generator chip illustrates gear changing.

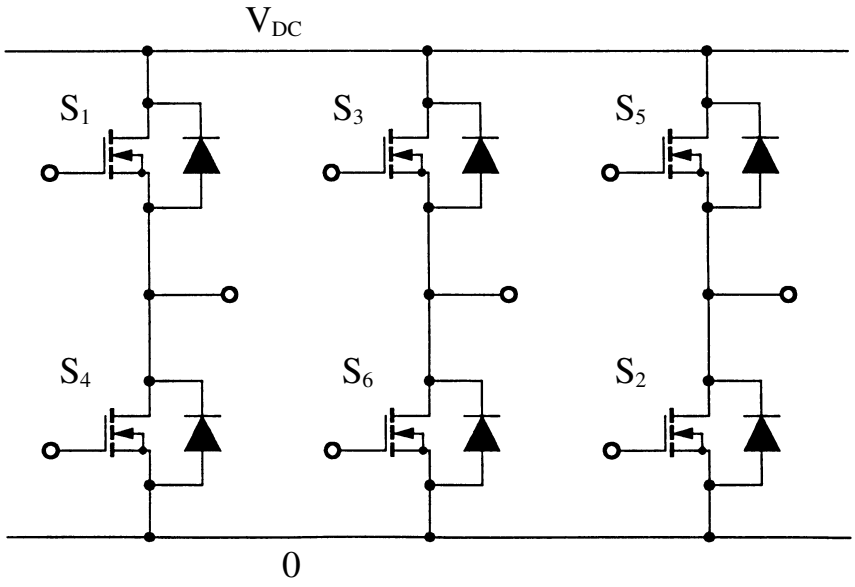


This effect can often be heard! Here, the output voltage is proportional to frequency up to 43Hz. Above this over modulation is adopted. This is common in induction motor drives.

13.2 Space Vector Modulation

SVM is a method of generating a sequence of switching combinations of the inverter, where each combination is called a state. The states can be represented in the complex plane by Space Vectors. By careful choice of the switch patterns being used, the total number of switching instances per cycle can be reduced, for a given quality of waveform

13.2.1 Voltage Vector Modulation



The eight states are

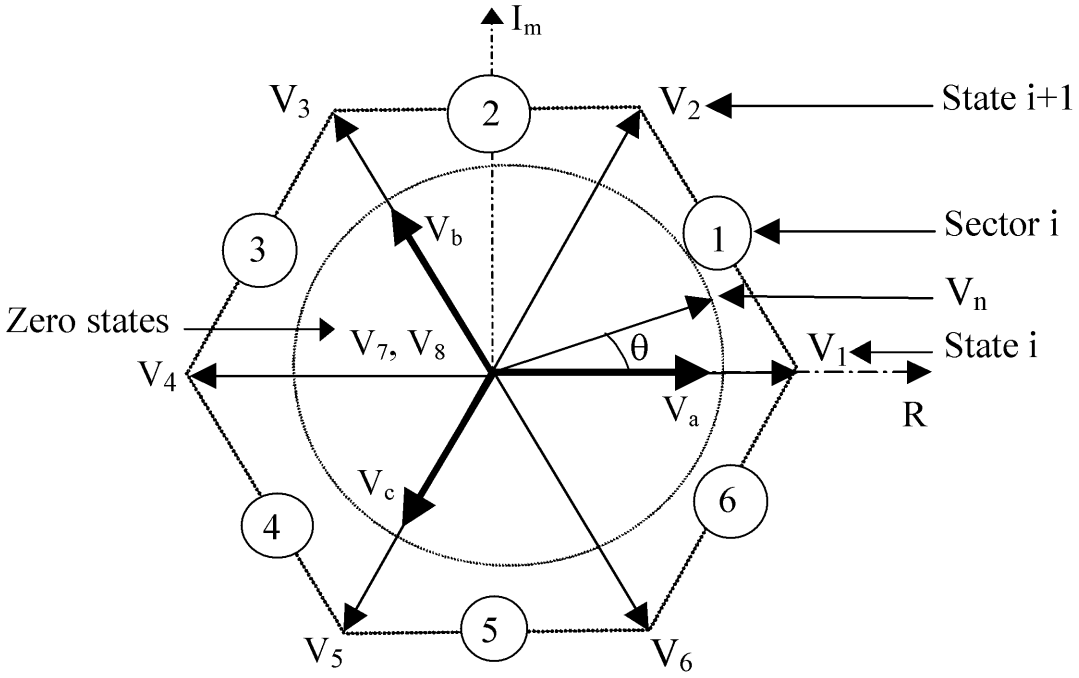
State	'ON' switches	$\frac{V_a}{V_{dc}}$	$\frac{V_b}{V_{dc}}$	$\frac{V_c}{V_{dc}}$
V_1	S_1 , S_6 , S_2	1	0	0
V_2	S_1 , S_3 , S_2	1	1	0
V_3	S_4 , S_3 , S_2	0	1	0
V_4	S_4 , S_3 , S_5	0	1	1
V_5	S_4 , S_6 , S_5	0	0	1
V_6	S_1 , S_6 , S_5	1	0	1
V_7	S_1 , S_3 , S_5	1	1	1
V_8	S_4 , S_6 , S_2	0	0	0

With two Zero States in grey.

The method is based on switching the three phase bridge as a whole to control the notional space vector of output voltage. Each state produces three phase voltages, and the line voltages are derived from these.

The six non zero inverter states can be considered as giving each of the three line voltages (and their opposites), in the same way that the three-phase thyristor bridge has six 'states'.

The phase and line voltages are represented on the complex plane as follows.



The objective of SVM technique is to obtain V_n with the eight SVs so that it will have an amplitude proportional to the modulation index m and rotating in the complex plane with an angular velocity ω_1 proportional to the frequency of the fundamental output f_1.

Obviously one should obtain V_n using the nearest two non-zero SVs, (State i and i+1), and either of the zero states. By switching between these three (or four) states, duty ratio modulation then controls the magnitude of the two nearest non-zero SVs.

Any magnitude & angle of Vn can be made within the hexagon and it can then be stepped around to rotate Vn at the desired output frequency, f_1. The output of each leg appears to be our usual pwm output. The method is often referred to as SVPWM to make it clear that it really is a form of pwm. By considering the bridge in terms of its logic, we can take advantage of unipolar switching.

There are two main switching sequences:

'Direct-Direct' uses V7, or 'state 7' (111), as the zero state in sectors 1, 3 and 5, and V8, state 8 (000), as the zero state in sectors 2, 4 and 6. The switching sequence remains the same during the same sector; for example in Sector 1, the switching sequence

V1, V2, V7, V1, V2, V7, V1, ...

The effective switching frequency for this strategy is $2f_s/3$.

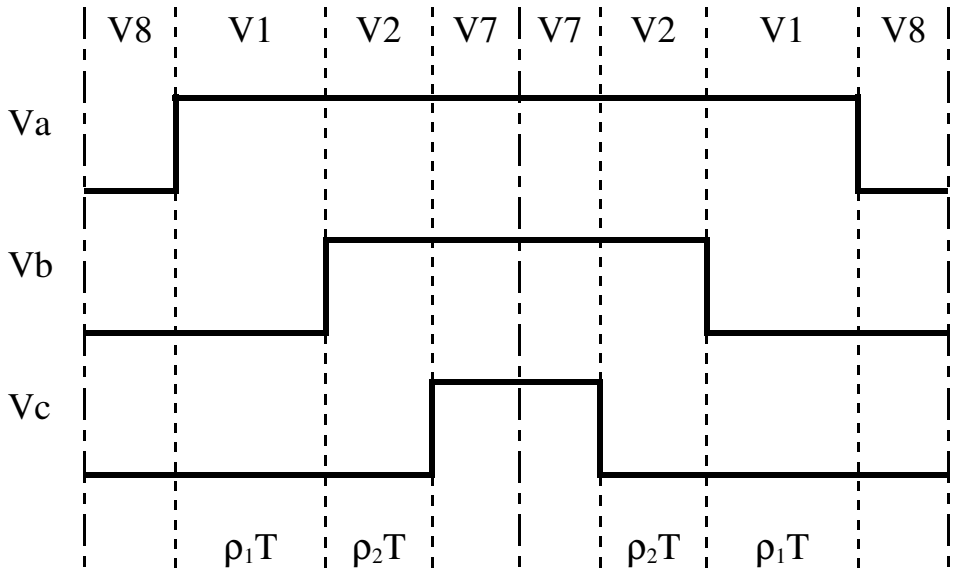
'Direct-Inverse' sequence, uses the two zero states in every sector to reduce the overall number of switching instances per cycle. The switching sequence is reversed after passing through each zero state; for example in the first sector the sequence is

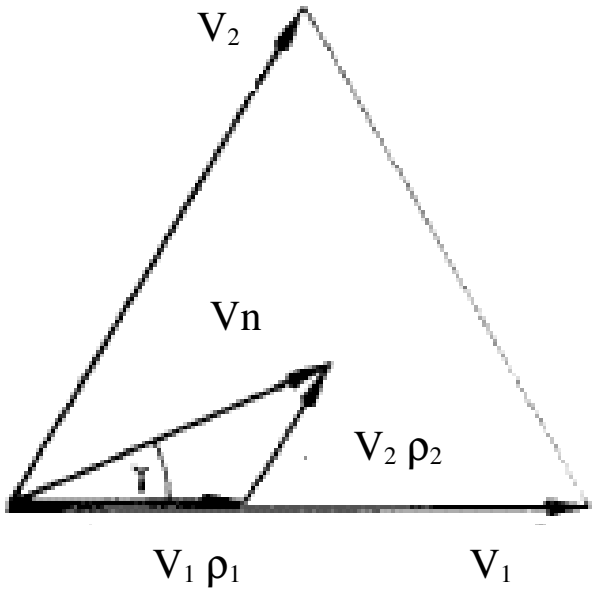
V1, V2, V7, V2, V1, V8, V1, ...

The advantage of this strategy is that it gives three commutations per cycle and gives symmetrical pulses. The effective switching frequency for this strategy is $f_s/2$.

13.2.2 Creation of the Direct-Inverse switching signals

For *two* cycles at the switching frequency:

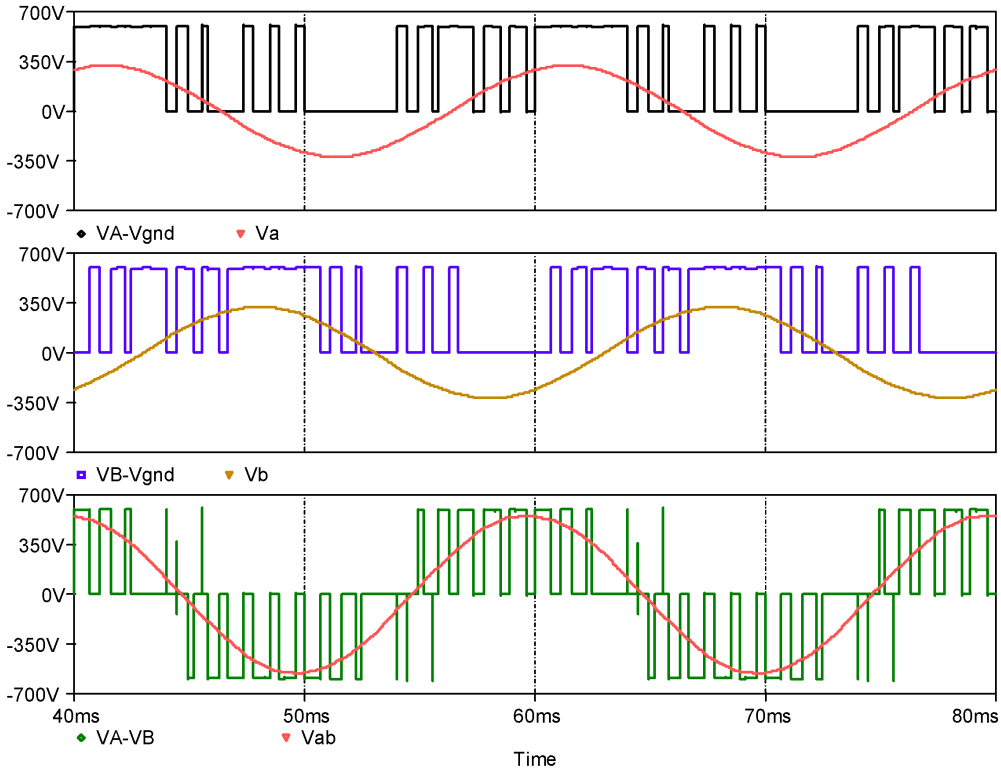




Each switching sequence has its own advantages and disadvantages in terms of switching losses and current ripple at the output, but this one is often quoted as the one with lowest switching losses.

13.2.3 Example waveforms

The lower switching rate and good performance can be seen below.



Note the symmetry in the waveforms and identify the six sectors.

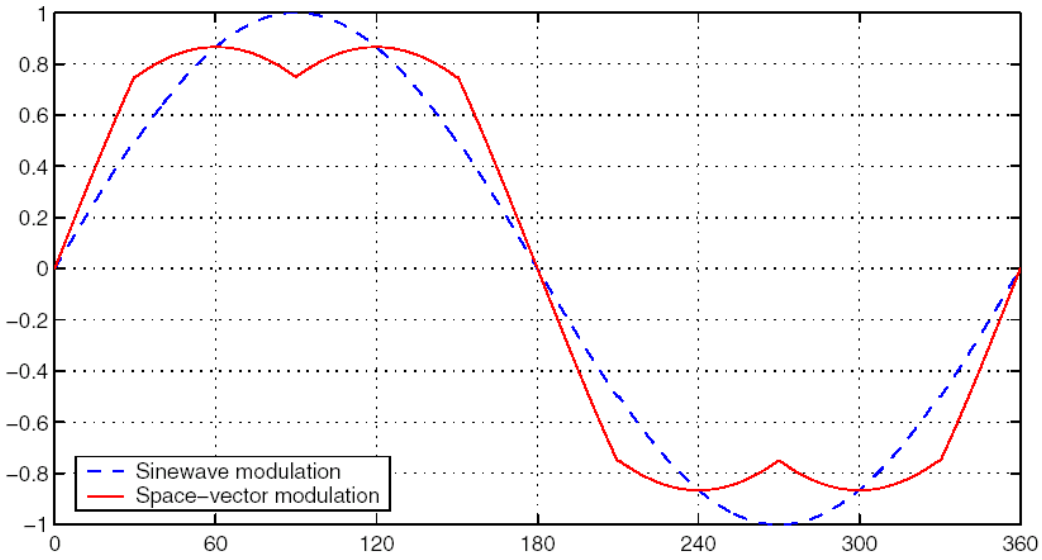
13.3 Comparison between SVM and PWM

SVM schemes are easy to implement in a microprocessor or FPGA. PWM with integer frequency modulation ratio are not so easy to produce, as the simplicity of naturally sampled pwm is lost.

In contrast to sinusoidal pwm, a modulation index m of 1.15 can be reached using SVM without the loss of quality usually associated with over modulation. However the standard sinusoidal pwm method can be improved by adding a third harmonic term to the reference waveforms, which will cancel in the bridge.

13.3.1 Comparison of the Bridge leg voltage output

Switching frequency components filtered out:



Since the filtered bridge leg output is the same as the reference waveform in pwm, it is clear that SVM can be considered as a special case of pwm and it is often described as SVPWM. However, such an understanding misses the state machine implementation advantage.

Both methods involve some trig calculations, although these maybe performed by using a look-up table. Clearly calculating which sector the vector is in is crucial to selecting the correct space vectors to modulate.

14 Resonant Inverters I

Probably the most common use of resonant circuits is in converting dc to ac with a fixed frequency set by the resonant load. It is an attractive way of producing clean sinewaves with simple switching circuits. The resonant circuit really acts as a filter. Such circuits are found in radio transmitters, fluorescent lamps, induction heating and even dielectric heating.

14.1 Resonance and Quality factor

14.1.1 Basic equations for series resonance

Staring with loss less resonance (infinite Q):

$$\omega_O =$$

$$Z_O =$$

1st half cycle equations from zero applying a dc voltage:

$$V_C = V_{DC}\,(1-\cos(\omega_O t))$$

$$I_C = V_{DC}/Z_O \sin(\omega_O t)$$

14.1.2Definition of Q

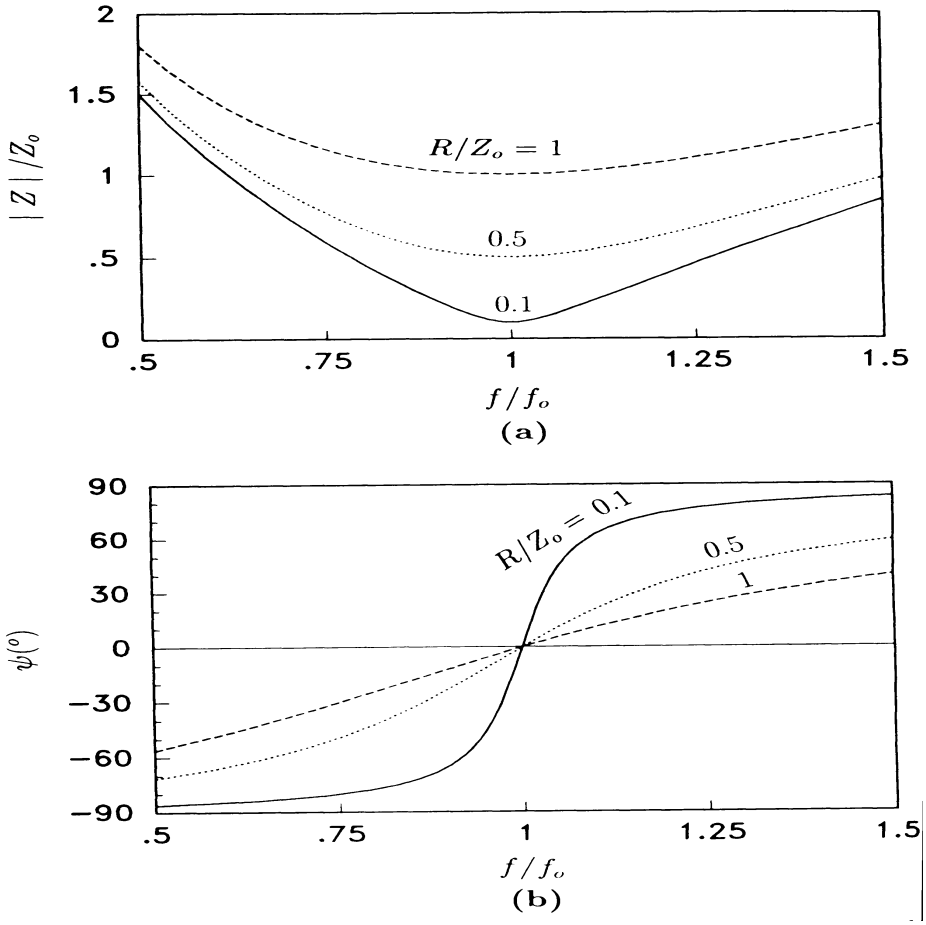
From data book:

Clearly finite Q is what interests us as we want to be transferring power from the supply to the load. This tends to imply we want a low Q. High Q circuits are good for the special use in resonant link dc-dc converters (last lecture)

Low Q circuits can give us various desirable features without the need for large and expensive capacitors and inductors.

14.1.3 Impedance of a series resonant LCR circuit

The impedance of the series resonant circuit can be plotted versus frequency. At high frequencies, the inductance dominates, and the phase is 90^O lag. At low frequencies, the capacitance dominates, and the phase is 90^O lead. At resonance, the impedance of the capacitor and inductor cancels leaving the impedance of the series resistance.



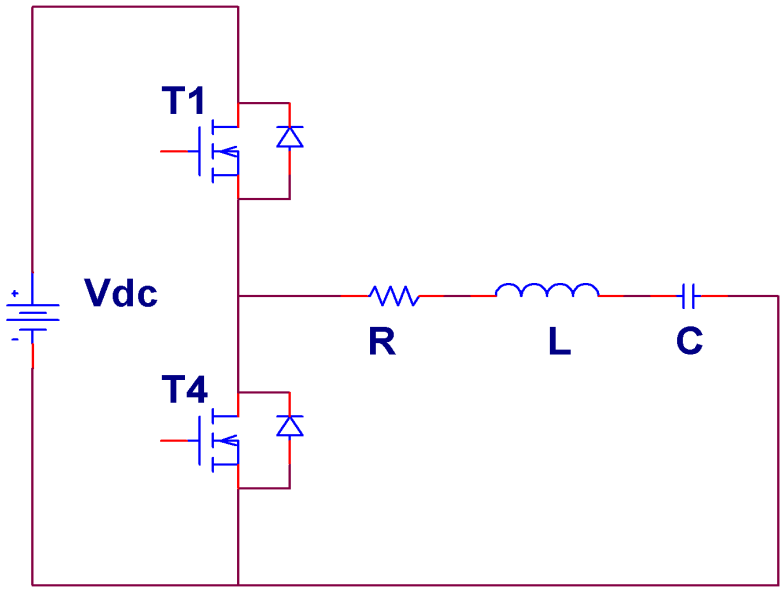
The impedance serves to reject the high and low harmonics of the voltage waveform present at the terminals. So the current is mostly a sinewave at or near the resonant frequency.

14.2 Class D Series Resonant Inverter

Class D inverters are classified into current source and voltage source according to the supply type (respectively inductor smoothed or capacitor smoothed immediately before the inverter stage). Voltage source resonant inverters use series resonant circuits and current source resonant inverters use parallel resonant circuits.

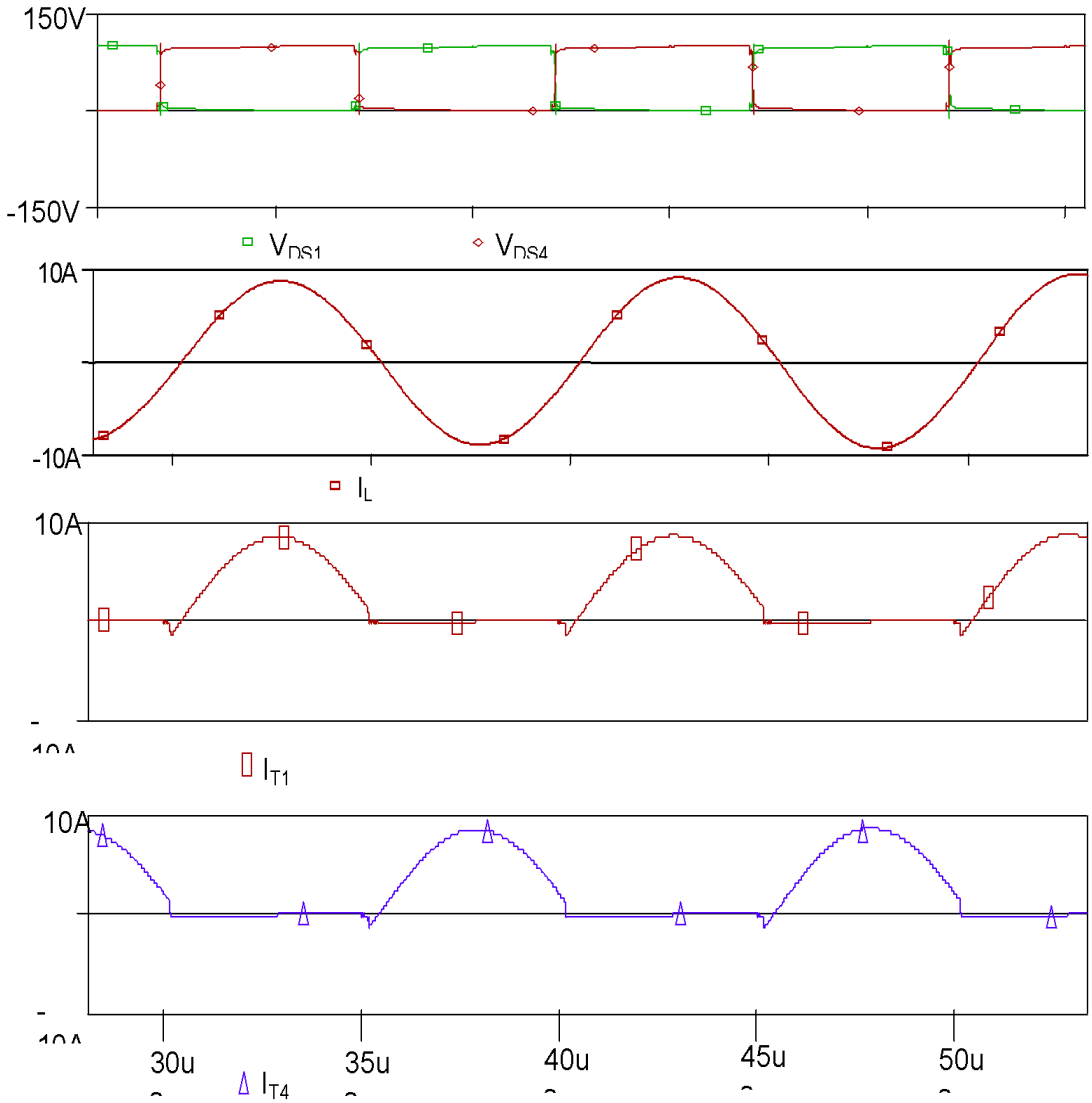
14.2.1 Class D Voltage source half bridge series resonant inverter

Two switches and a series resonant circuit:



The obvious way to use this circuit is on resonance. However, the off resonant behaviour is important, as in this mode the output power may be controlled.

14.2.2 Basic waveforms



Alternate half cycles flow through the two MOSFETs, as expected and in principle the diodes never conduct. This is very efficient as there are no switching losses.

Since the current is resonant, the inductor and capacitor voltages are also sinusoidal at the resonant frequency.

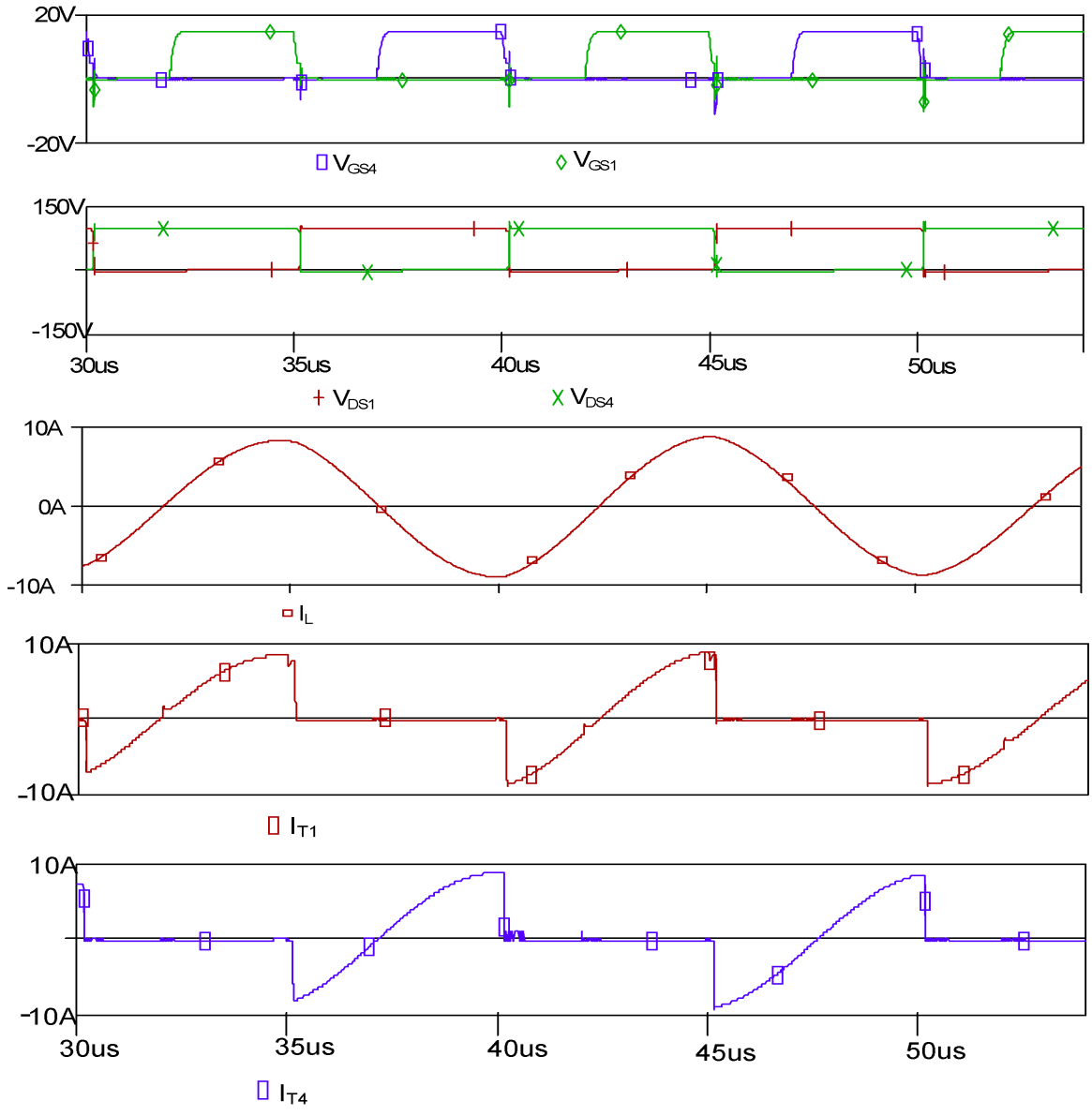
> Some deadband must be retained. It is also hard to tune it exactly, so it is unlikely to be perfectly on resonance, although the difference is very small.

.

14.2.3 Operation above resonance, $f > f_o$

The impedance of the inductor rises and the capacitor decreases, so the load appears inductive. This is a familiar mode of operation for the voltage source converter leg, except the current reverses each cycle. The current lags the voltage by the phase angle.

Waveforms:



In each case the switch current is negative immediately after turn on (the respective internal diode is conducting) and the current goes positive during the on-time. The conduction sequence is therefore

T1, D4, T4, D1, T1, D4.....

Consequently, the transistors turn on at nearly zero voltage, with conventional inductive turn off.

The filter effect of the resonant circuit is still very significant if f is not too much higher than f_O , and the current is very sinusoidal. Because the MOSFET current starts negative and ends positive in each case, the diode recovery is very gentle, as the reverse recovery current is part of the resonant load current.

Notice that a significant deadtime is now allowable, as the gate can be low when the diode of the particular switch is conducting. This is possible as the load on the switch leg is tightly defined in a resonant circuit. This makes operation above resonance a safe mode, although it is accompanied by severe turn off losses.

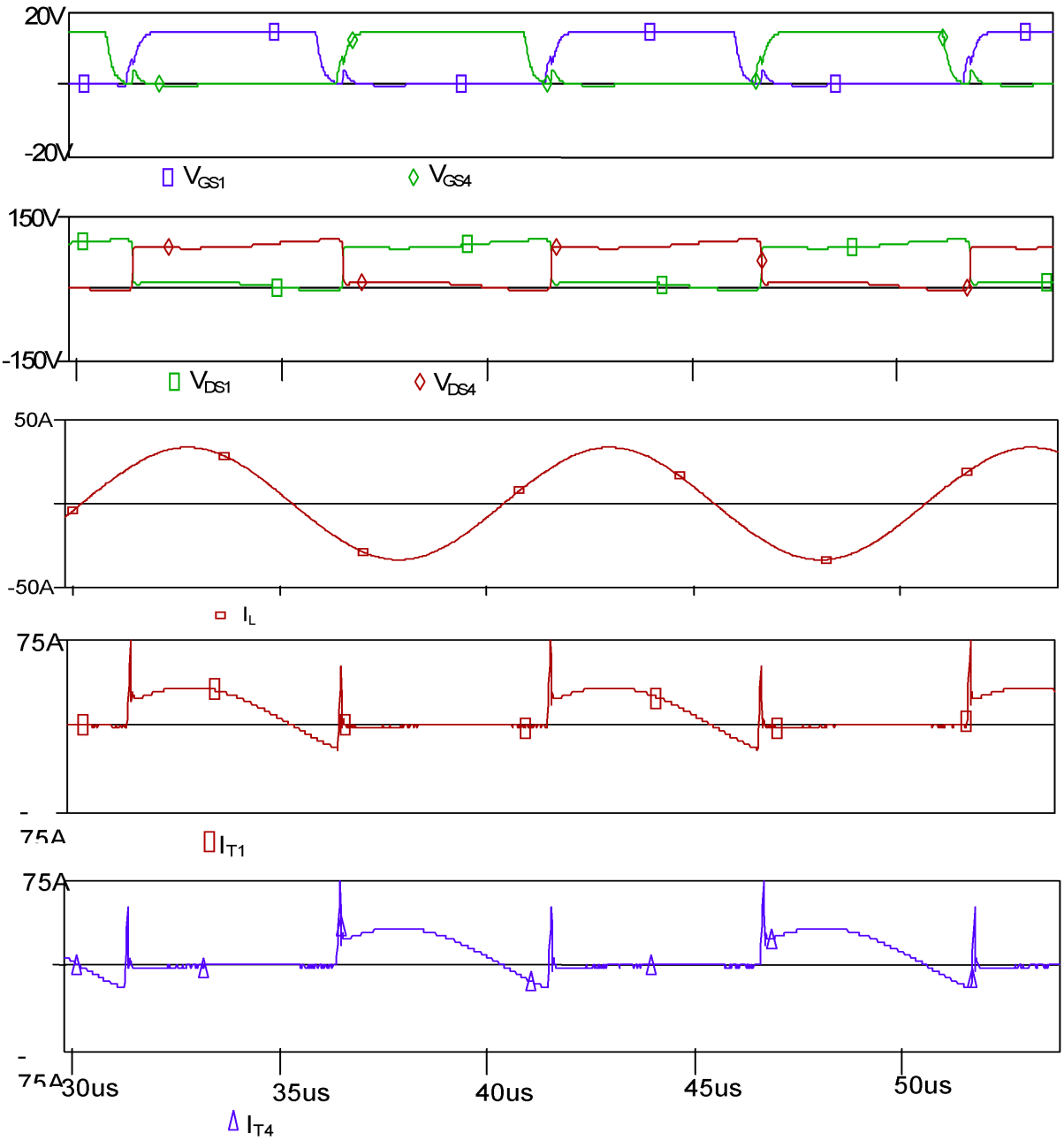
The switches can be seen to be forcing the frequency.

This is often the preferred mode for operation, as there is control of the current via the frequency and the switching is not stressful.

14.2.4 Operation below resonance, $f < f_O$

At below resonance, the resonant circuit appears capacitive: The current leads the voltage.

Waveforms:



The filter effect of the resonant circuit is still very significant if f is not too much lower than f_O , so the current is still very sinusoidal. The MOSFET current reverses while it is on (transferring to the diode from the MOS channel).

As the current goes negative during the on-time so the MOSFETSs turn off with zero current (lossless). The conduction sequence is therefore

T1, D1, T4, D4, T1.....

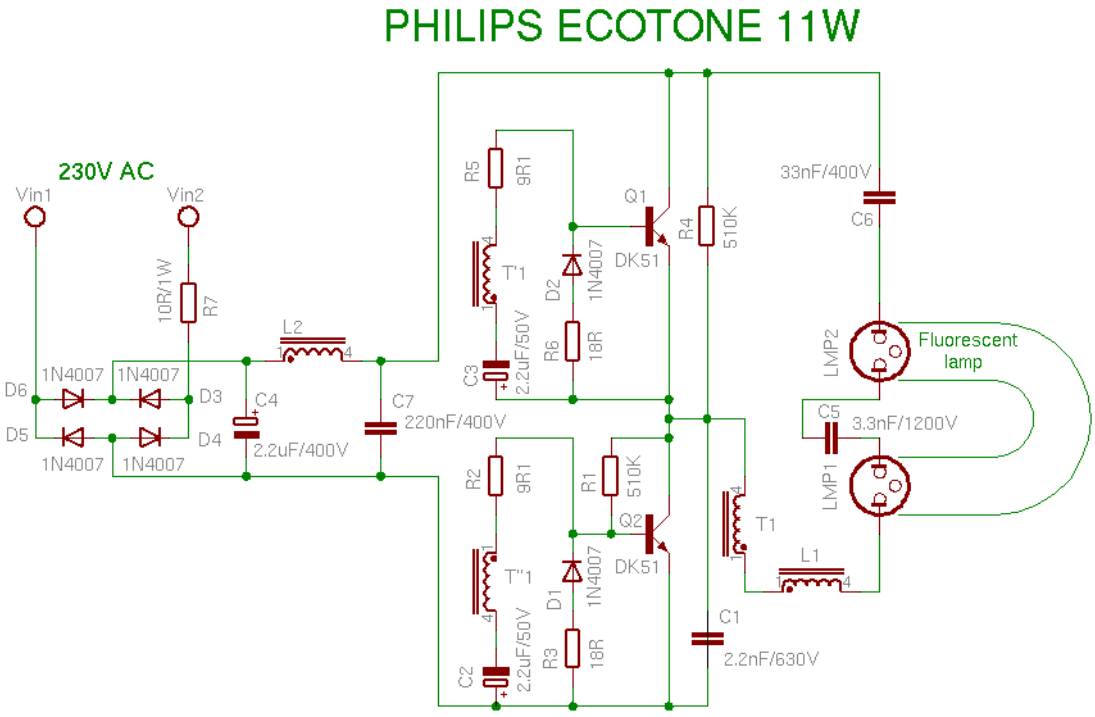
The transistors turn on into current as if it were an inductive load. This leads to significant turn-on switching losses, but zero turn off losses.

Again, a significant deadtime is now allowable, as the gate can be low when the diode of the particular switch is conducting. This is easy to arrange and very safe.

The switches can be seen to be holding back the resonant circuit frequency.

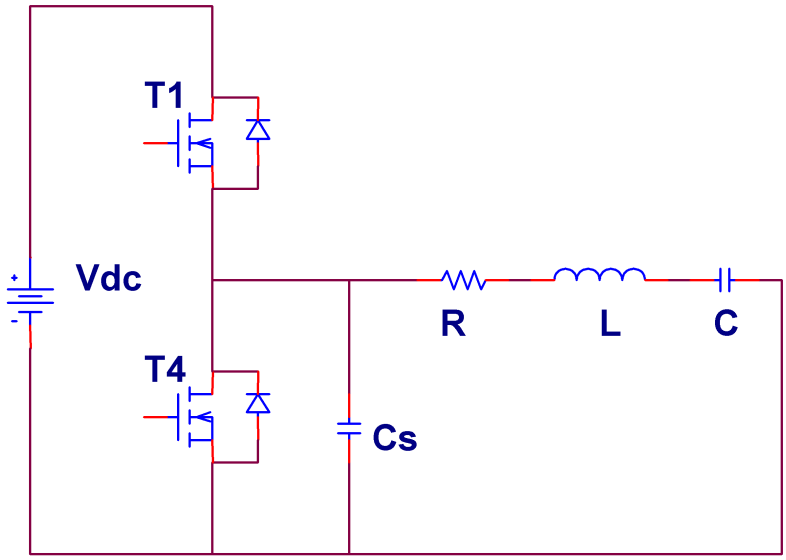
The reverse recovery current in the diode and MOSFET can lead to excessive losses, if operating at a high frequency. At more moderate frequencies, with IGBTs or MOSFETs as switches, the behaviour is rather better. Recall that the internal diode of the MOSFET is optimised for moderate switching frequencies,

14.2.5 Example circuit: Compact Fluorescent Lamp



The lamp appears resistive, related to the filament electrode.

14.2.6 Zero Voltage Switching Class D series resonant inverter



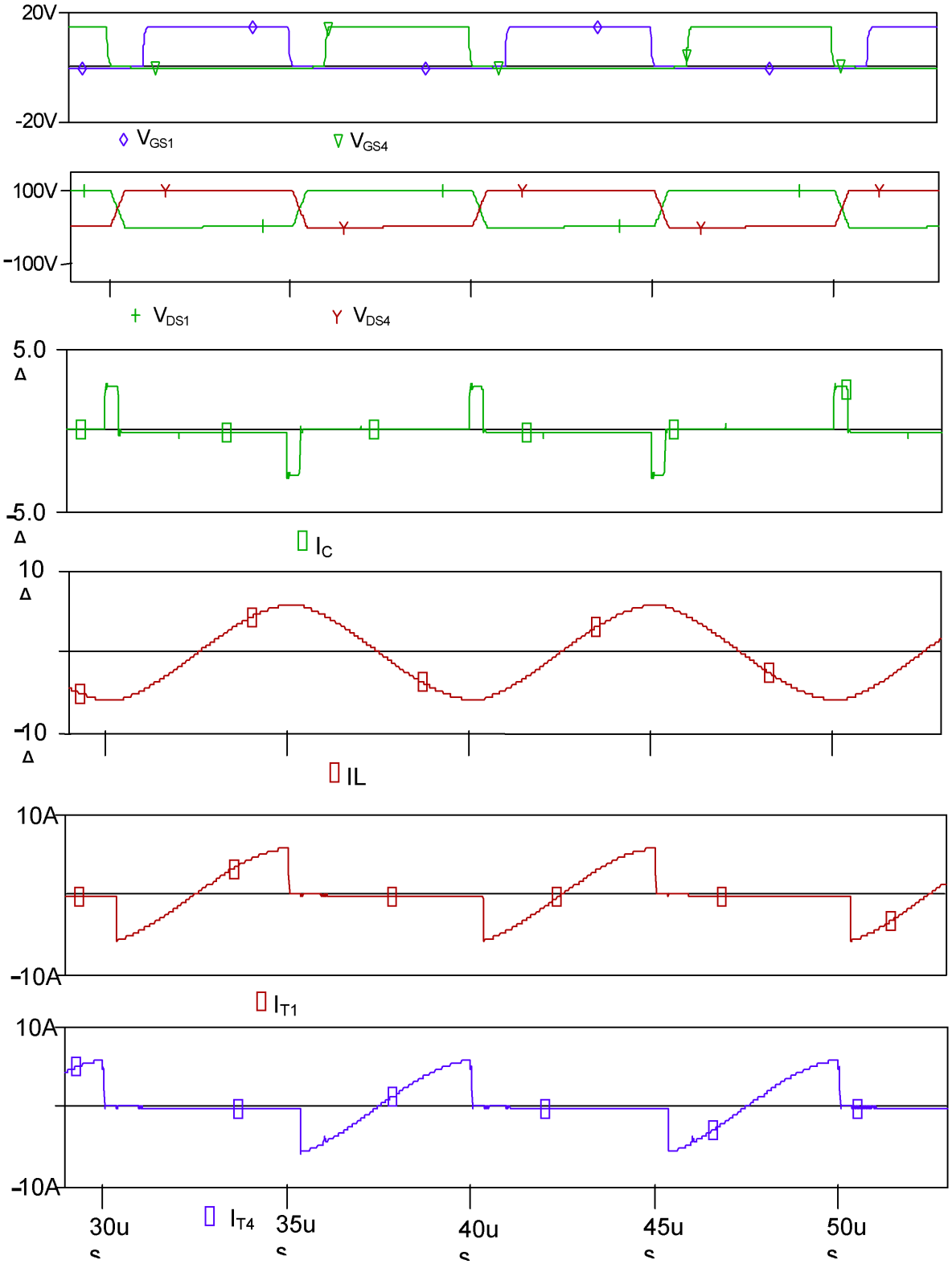
The circuit is identical to that seen in Section 14.2, with the addition of an extra capacitor at the leg output, to assist the switching for a short period within the resonant cycle.

Clearly there is the danger of blowing up the MOSFETs if the voltage across them is greater than zero when they turn on! This imposes the strict condition on the circuit that it is only used above resonance ($f > f_O$) so using zero-voltage turn on.

The intention of the additional capacitor is to assist the turn off, which was a hard switched turn off under these conditions without the capacitor. The capacitor C_S acts as a 'snubber'. Consider the case when T4 is on and conducting the load current. When it is turned off, the load current redirects to the capacitor C_S . The MOSFET current drops to zero immediately, with a low voltage across V_{DS} , thus ensuring no switching loss at turn off.

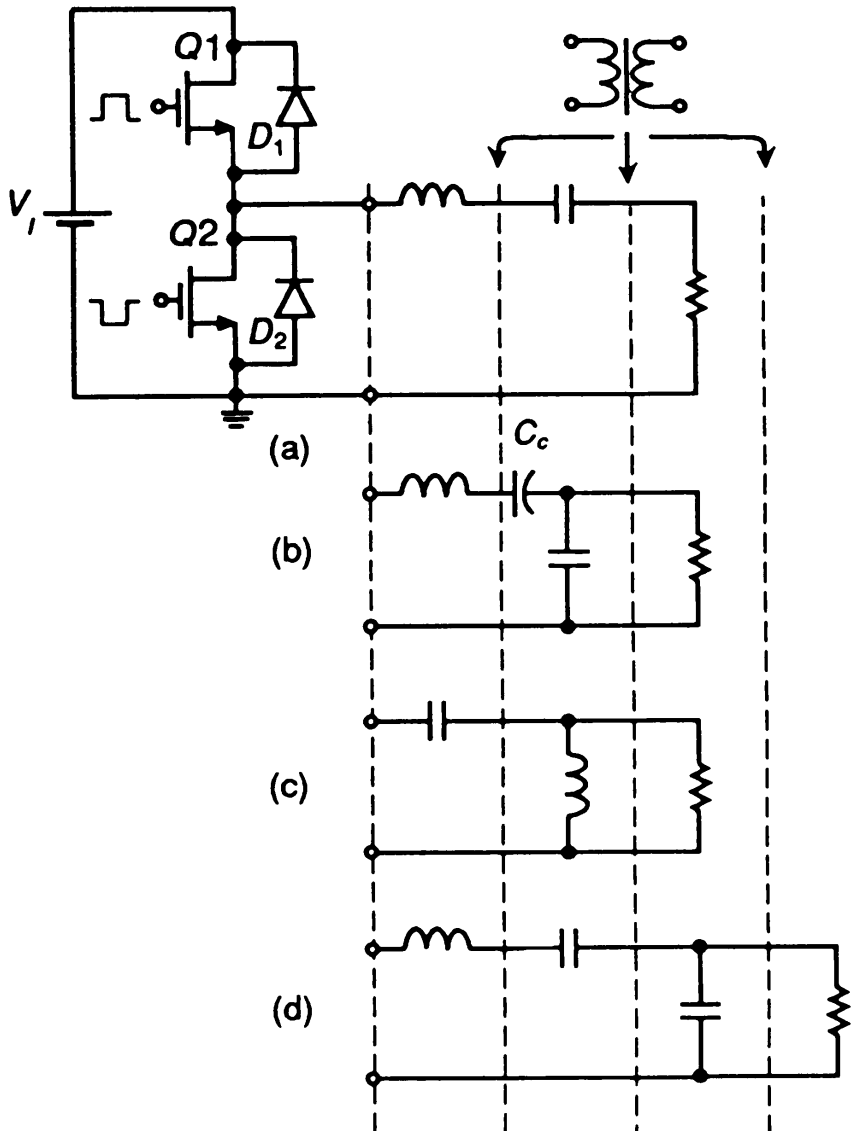
The capacitor should be small to charge up quickly, compared to the resonant frequency, so the load waveforms are barely affected.

Waveforms:



Compare to the results in section 14.2.3.

14.2.7 Alternate topologies

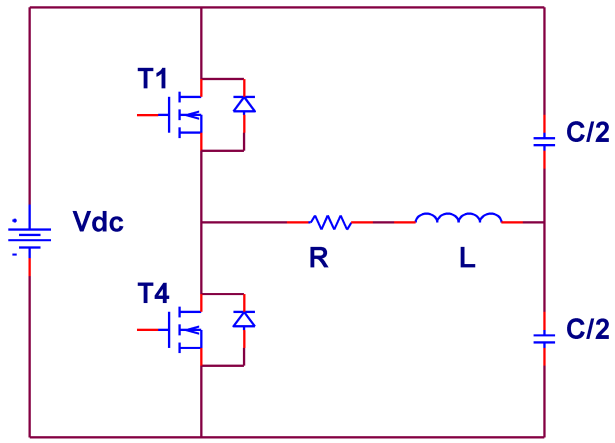


Since the only requirement here to producing a clean ac waveform is a reasonably high Q series resonant circuit operated near to resonance, any ac circuit with these terminal characteristics may be used. In particular, transformers may be introduced with benefit in some cases. A capacitor connected across the load can be attractive in cases where the load is variable.

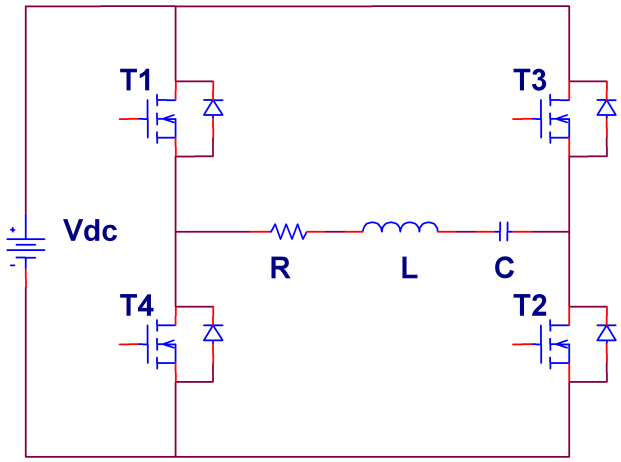
14.2.8 Symmetrical circuits

In the original circuit, the resonance is boosted in one half cycle per full cycle of the resonance. In symmetrical circuits, the resonance is boosted each half cycle by energy from the supply.

In the original circuit above, the resonant capacitor may be split between the supply rails (note it is not the same from the dc supply point of view).



While the full bridge circuit offers fully symmetrical operation, it has twice the MOSFETs and losses of the asymmetrical circuits.



This may be useful where the Q is very low.

Series resonant inverters clearly are very attractive for some applications. Only series resonant circuits can be used with voltage source inverters, as the high dv/dts at the leg output are filtered out. However, reduced switching losses and well characterised behaviour comes at the cost of higher switch currents than for simple inverters - so greater on-state losses.

15 Resonant Inverters II

15.1 Parallel resonant circuits

15.1.1 Basic equations for parallel resonance

For R, L and C in parallel, we can define the infinite Q resonant frequency and impedance.

$$\omega_O =$$

The parallel resonant circuit will have a sinusoidal current in its own mesh. This gives a sinusoidal voltage in the capacitor and inductor, as expected, BUT the terminal current is not related in magnitude to the 'ringing' current. Consequently the characteristic impedance is for the ringing L-C pair - not the impedance at the terminals.

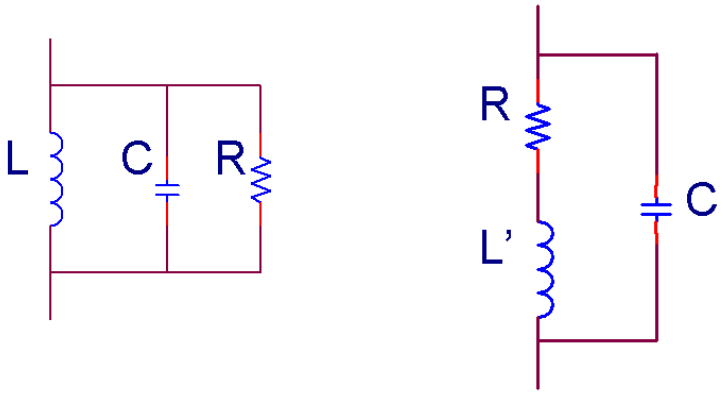
$$Z_O =$$

The quality factor Q_P is specified differently to take into account the operation

$$Q_P =$$

This is the inverse of the series case. A larger resistor give more output voltage so Q_P is often called the 'voltage magnification factor'.

Obtaining a pure L is impractical. Indeed, in many applications, the L is the inductive load, which has a capacitor placed across it to make it parallel resonant. An inductive load is modelled by a series L-R branch. Consider



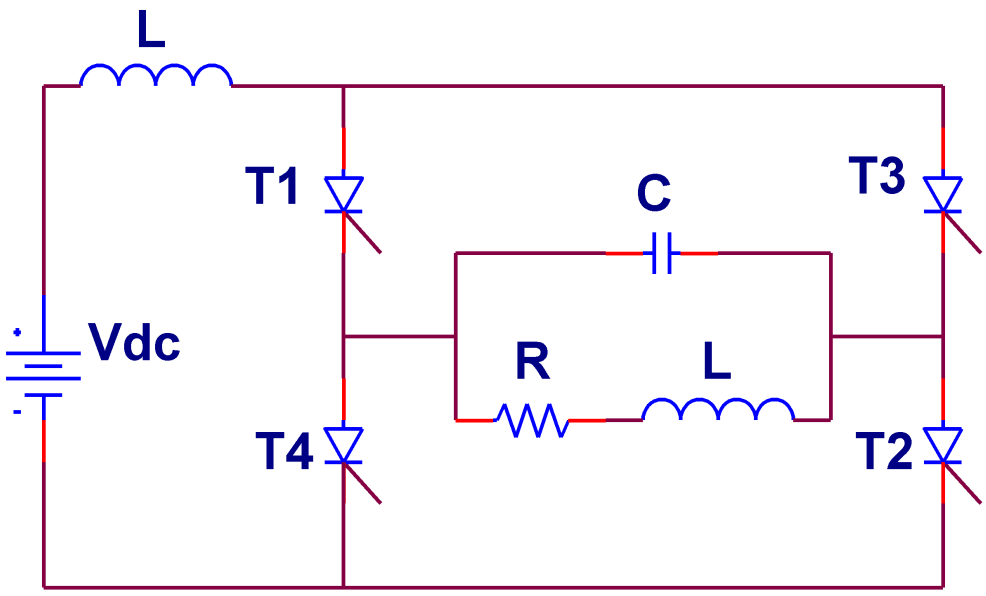
These circuits are equivalent, except at low frequencies.

15.2 Current Source parallel resonant inverters

The current source resonant inverter CSI based on a parallel resonant load has been used for a considerable period. The frequency was up to about 25 kHz, using thyristors, although many were based around about 50/60 Hz.

15.2.1 Class D parallel resonant inverter

The resonant load again acts as a filter. In this case the input to the parallel resonant load is a square wave current, which is turned into a sinewave voltage of adjustable magnitude depending on the frequency of operation.

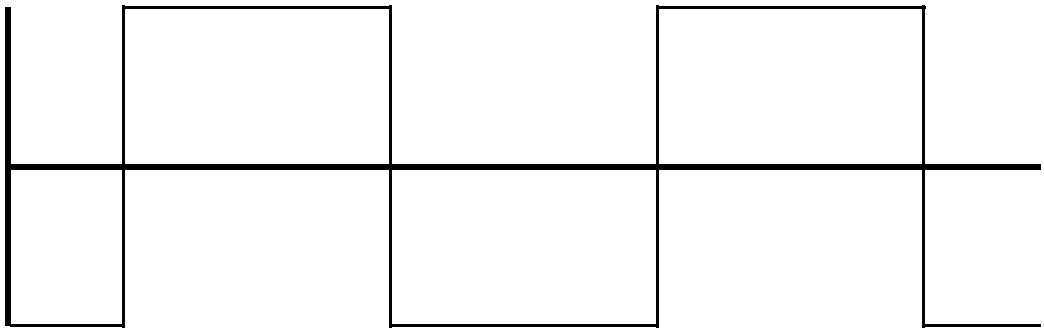


The circuit is operated with $f > f_O$ to ensure that the load to the bridge appears capacitive, with a leading power factor. This allows the thyristors to be commutated by the voltage on the capacitor:

For T1 and T2 on, the voltage V_O is positive at the point when T3 and T4 are fired. With the load voltage in this direction the thyristors turning on take over the current, thus commutating the previous set of thyristors. Clearly the thyristors must be switched in pairs:

T1T2, T3T4, T1T2.....

Waveforms



The phase angle between the current and voltage must allow enough time for the thyristor commutation. Overlap does appear due to stray inductance (in the capacitor and wiring) and the thyristors have their own commutation time. This must be carefully considered if operating at high frequencies such as 25 kHz and 'fast' thyristors must be used[1]. Most applications have a low Q.

In many cases the load resistance and inductance changes, such as when induction heating a billet of steel. Since the capacitor value is fixed,

The thyristor based parallel resonant inverter is an attractive version of the resonant inverter for high powers, as it employs the efficient thyristor and the control is simple. Loads may be transformer coupled and 'matched' in a variety of ways, in a similar fashion to the series resonant case. These circuits are widely used in induction heating of stell and the kiln drying of large quantities of wood: See footnote and the following links.
http://www.heatwave.com/technology/overview.htm,
http://www.woodweb.com/knowledge_base/Radio_frequency.html

[1] http://www.powerpulse.net/story.php?storyID=18019

15.3 Notes on circuit analysis

15.3.1 Resonant inverters

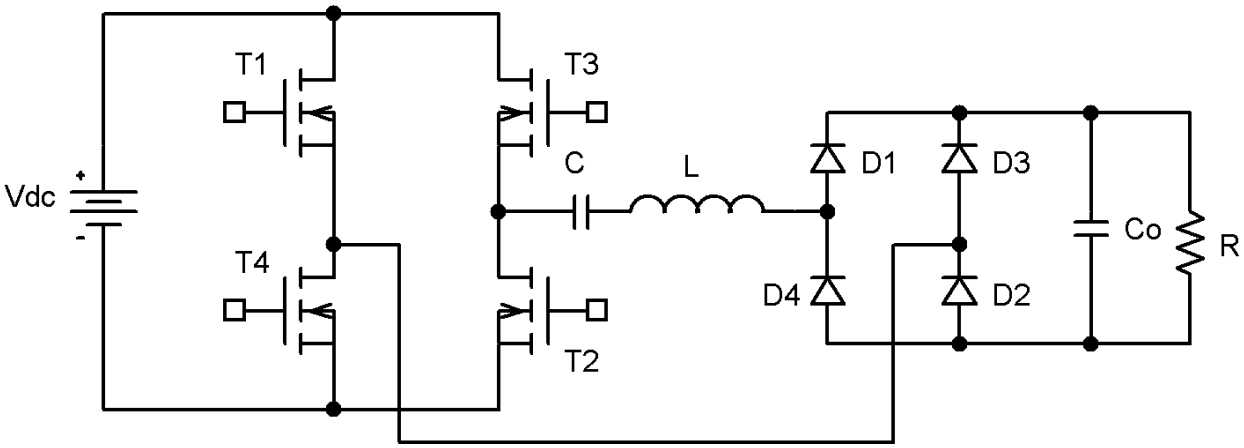
In all these DC to AC inverters, the resonant circuit including the load is a filter. For any reasonable Q, the current in the cycle is sinusoidal. Here, startup is not considered, so only the steady state needs consideration. The input of interest for Class D (square-wave) operation around the resonant frequency is the fundamental of the square wave:

$$\frac{4}{\pi} V_{DC} \sin \omega_1 t$$

In addition, the conversion process implies the current is doing work in the AC side. Consequently it is necessary to include the resistance of the load. Normal AC analysis methods, including power factor, may then be used.

15.3.2 Resonant converters

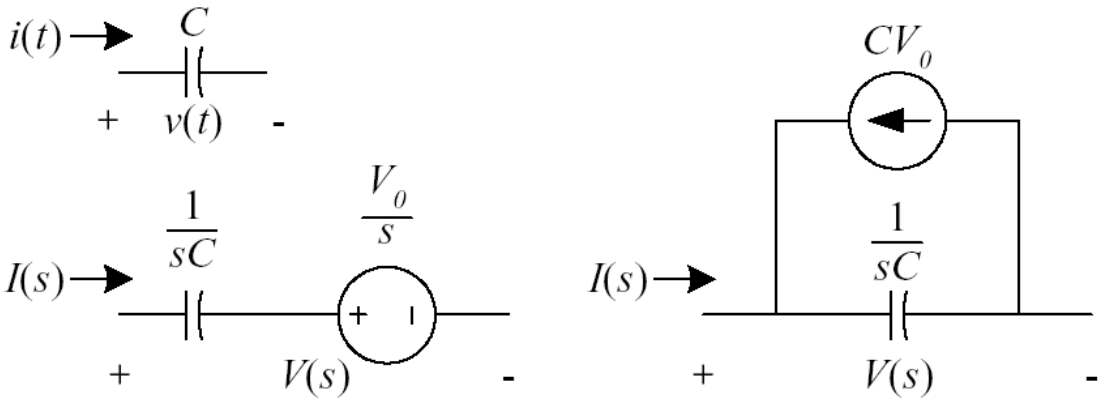
Resonant dc-dc converters may be made by adding a rectifier circuit on the ac side, converting the high frequency ac to dc. E.g. The class D series loaded resonant dc-dc converter:



Clearly the loads are after the rectifier. Therefore, all the resonant converter work here always assumes a lossless resonance - so use Z_O in the simple analysis to find the peak current. But this must be done on a period to period basis, depending on the state of the switches and diodes. Final conditions of one period become the initial conditions of the next.

15.3.3 Laplace approach to initial conditions

Consider a capacitor in Laplace transform terms:



$$V = \frac{1}{C}\int i\,dt + V_O \qquad\qquad i = C\frac{dv}{dt}$$

$$V(s) = \frac{1}{Cs}\,I(s) + \frac{V_o}{s} \qquad\qquad I(s) = Cs\,V(s) - CV_O\,,$$

where Vo is the initial voltage on the capacitor at the beginning of that time interval.

A similar analysis can be done for inductance.

$$I = \frac{1}{L}\int v\,dt + I_O$$

Remember that the dc voltage source transforms as

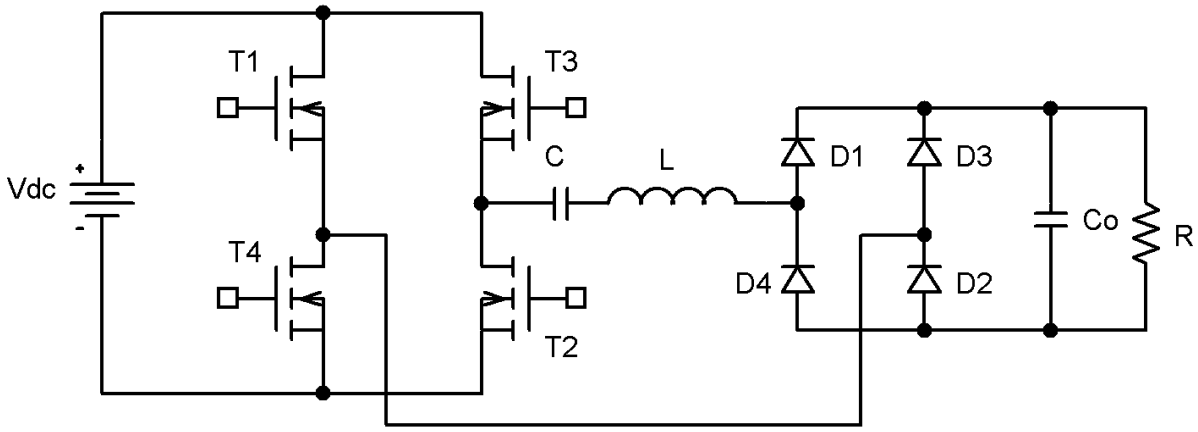
$$\text{Vdc} \Rightarrow \frac{V_{dc}}{s}$$

Compare this to the above Laplace transform for the voltage of a charged capacitor: The initial conditions appear to be a series voltage source (or a parallel current source).

> The capacitor's initial condition voltage can simply be added or subtracted from the dc supply voltage in an appropriate sense for the operation of the circuit. Then we do not even need to use the transforms!

15.4 The Class D series loaded resonant dc-dc converter

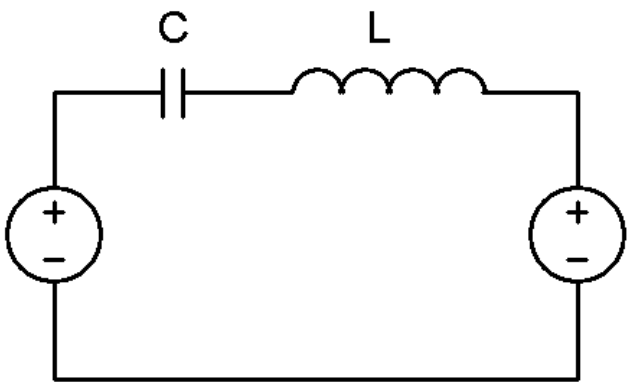
A diode bridge with capacitive smoothing is supplied by a series resonant link. The link is forced into resonance by the inverter bridge.



The main reason for going through sinusoidal ac rather than a simple switched mode is to reduce or eliminate switching losses. Then is can operate at a high switching frequency and use small L's and C's.

Ignoring the transient start-up conditions, we can assume that there is a positive output voltage as desired and that CoR >> T, so Vo is constant.

Once again, the circuit must be divided up into the relevant parts. This time, however, it is clear that there are various possible combinations of the resonant circuit as there is an inverter bridge and a rectifier bridge. Even with the Class D squarewave (Bipolar switching) in the inverter bridge there are 4 combinations.:



We can write down the four combinations in order with respect to the voltage across the resonant circuit current.

$i_L > 0$

$i_L < 0$

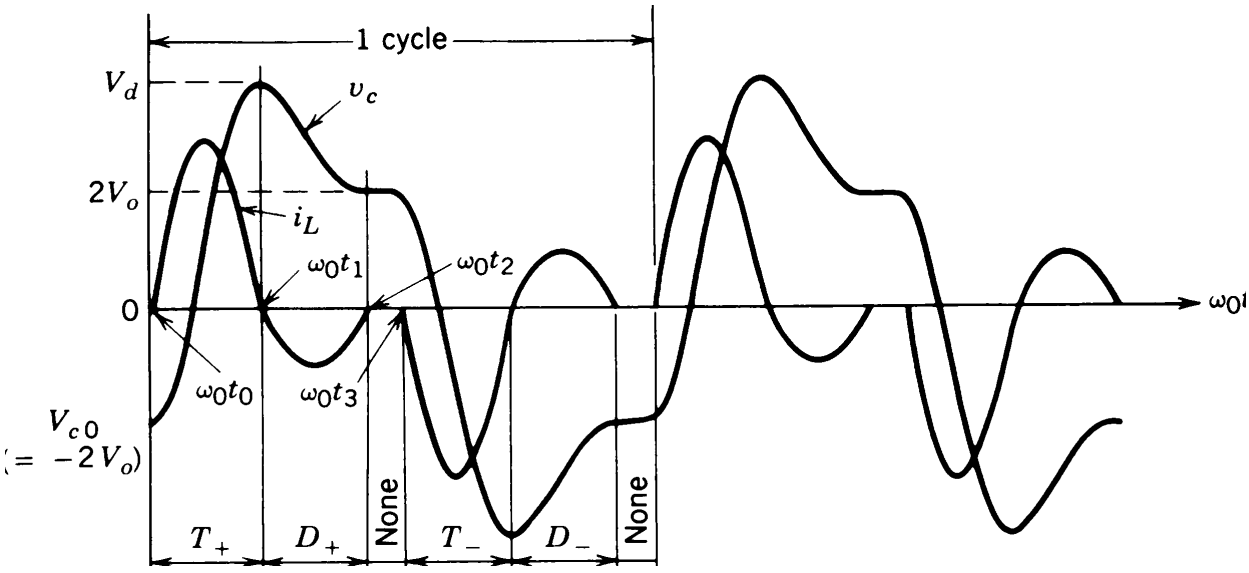
The rectifier bridge voltage resists the current in both senses!

The analysis is now straight forward if we assume ideal components in the resonant circuit. In particular the whole circuit is symmetrical so we only need analyse 2 periods and the period when the bridges are off.

Clearly the circuit can operate with $f > f_O$ or $f < f_O$.

15.4.1 Analysis for discontinuous conduction ($f < f_O/2$).

Waveforms:



This is an attractive mode, as each half cycle of the inverter bridge is a complete cycle of the resonant link and then the circuit 'rests' for a while, before the next half cycle of the inverter bridge. The output smoothing capacitior can supply the output current for the short period when there is no supply from the inverter.

By putting closed loop control into the system, the power transfered can be modulated by the duty ratio, rather like the flyback converter. (This is not strictly class D or Class E according to my understanding!*)

Period 1

Turning on T3, T4 gives a forward voltage step to the resonant link, with the current passing through the rectifier to the smoothing capacitor, Co. The voltage appled to the resonant link is

$$Vdc - Vo .$$

Since the initial condition of v_C is $-2V_O$ Anayse an uncharged L-C with

$$(Vdc - Vo) - (-2Vo) = Vdc + Vo$$

The current resonates and reverses, whereupon the voltage seen by the resonant capacitor C has changed by

$$2(Vdc + Vo)$$

Subtracting the initial condition $-2V_O$ gives the voltage on the capacitor of $2V_{DC}$ at the end of period 1. The peak current is given by

$$(Vdc+Vo)/2$$

Period 2

Remember that the current in the resonant circuit has reversed, but not the inverter bridge state, so the sense of the output voltage reverses due to the diode rectifier bridge action. So the voltage applied to the resonant link is

$$Vdc+Vo$$

The capacitor has a voltage at the start of this period of $2V_{dc}$, so the voltage across the resonant circuit is

$$(Vdc+Vo) -2Vdc = -Vdc+Vo$$

Thus the resonating current peak is reduced to $(V_{dc} - V_O)/Z_O$.

The ring ceases if T3, T4 are switched off by the time the current attmepts to reverse (deadtime is easy to arrange). So C remains charged.

$$2V_{dc}- 2(V_{dc} - V_O) = 2\ V_O$$

The reverse of our original initial conditions so the analysis works!

The load is then supplied by C_O.

Note carefully: The *average current* of the inverter waveform over one half cycle multiplied by the *DC input voltage* is the power transferred.

The switches turn off at zero current and zero voltage (so thyristors could be used here). The switches turn on at zero current but not zero voltage. Both are lossless switching conditions, so the switching losses are very low even for high frequency operation. The main drawback of this and many other resosnant dc-dc converters is the high resonant current, whcih causes on-state losses in the switches and diodes. Switching with ($f_O/2 < f < f_O$) and $f > f_O$ are possible, but do not benefit directly from lossless switching.

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November 2009