

# MIPS Overview

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The MIPS CPU architecture is used in computer architectures like SGI O2 and Octane systems, Nintendo N64 as well as the Sony Playstation, Playstation 2 and Playstation Portable.

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## General Registers

Name	Number	Function	Callee must preserve?
<b>\$zero</b>	\$0	constant 0	n/a
<b>\$at</b>	\$1	assembler temporary	no
<b>\$v0– \$v1</b>	\$2–\$3	values for function returns and expression evaluation	no
<b>\$a0– \$a3</b>	\$4–\$7	function arguments	no
<b>\$t0– \$t7</b>	\$8–\$15	temporaries	no
<b>\$s0– \$s7</b>	\$16–\$23	saved temporaries	yes
<b>\$t8– \$t9</b>	\$24–\$25	temporaries	no
<b>\$k0–</b>	\$26–\$27	reserved for OS kernel	no

<b>\$k1</b>			
<b>\$gp</b>	\$28	global pointer	yes
<b>\$sp</b>	\$29	stack pointer	yes
<b>\$fp/\$s8</b>	\$30	frame pointer	yes
<b>\$ra</b>	\$31	return address	n/a

**Note:** All except registers on the MIPS except \$zero, HI and LO are general registers; the listed usage is per convention and not enforced by the processor or the assembler. The register name \$s8 is a synonym for \$fp used in some assemblers, in systems where the frame pointer is not regularly used.

## Arithmetic Registers

Register	Multiplication	Division
HI	Multiplicand Upper word	Quotient
LOW	Multiplicand Lower word	Remainder

## Coprocessor 0 Registers

Name	Number	Function	Callee must preserve?
c0_index	cop0 \$0	TLB entry index register	n/a
c0_random	cop0 \$1	TLB randomized access register	n/a
c0_entrylo	cop0 \$2	Low-order word of "current" TLB entry	n/a
c0_context	cop0 \$4	Page-table lookup address	n/a
c0_vaddr	cop0 \$8	Virtual address associated with certain exceptions	n/a
c0_entryhi	cop0 \$10	High-order word of "current" TLB entry	n/a
c0_status	cop0 \$12	Processor status register	n/a
c0_cause	cop0 \$13	Exception cause register	n/a
c0_epc	cop0 \$14	PC at which exception occurred	n/a

## Instruction fields

Field	Size	Position	Op Types	Description
<b>op</b>	6	26-31	R, I, J	opcode for the instruction or group of instructions.
<b>rs</b>	5	21-25	R, I	Source register for store operations, destination for

				all other operations.
<b>rt</b>	5	16-20	R, I	First operand register.
<b>rd</b>	5	11-15	R	Second operand register.
<b>shift</b>	5	6-10	R	Immediate operand for shift and rotate instructions.
<b>func</b>	6	0-5	R	Extended opcode.
<b>imm</b>	16	0-15	I	Half-word immediate operand.
<b>address</b>		0-25	J	26-bit address field for unconditional jump operations.

## Addressing modes

Type	Assembly Format	Opcode format	Comments
Register	inst rs, rd, rt	op rs, rd, rt, shift, func	The opcode represents a group of operations rather than a specific instruction; the func field contains the actual operation. The shift field is only used in shift and rotate operations.
Immediate (I-type)	inst rs, rt, imm	opcode rs, rt, imm	Immediate operation use a 16-bit immediate value from the instruction word itself.
Load (I-type)	inst rs, imm(rt)	op rs, rt, imm	Load/Store operations are a special case of immediate, where the offset is the immediate operand.
Store (I-type)	inst rs, offset(rt)	op rs, rt, imm	Unlike in most other operations, the rs register is the data source.
Cond. Branch(I-type)	inst rs, rt, label	op rs, rt, imm	Conditional branches have a 16-bit relative range.
Jump {J-type}	inst label	op address	the J and JAL operations have a 26-bit relative range.

**Note:** The assembly formats given are those from the official MIPS Technologies documentation. Other assemblers (e.g., gas) may use different formats.

## See Also

### Articles

- System Initialization (SGI Mips)

### References

- Wikibooks: MIPS Assembly - Instruction Formats ([http://en.wikibooks.org/wiki/MIPS\\_Assembly/Instruction\\_Formats](http://en.wikibooks.org/wiki/MIPS_Assembly/Instruction_Formats))
- MIPS Instruction Coding (<http://www.d.umn.edu/~gshute/spimsal/talref.html>)

- MIPS Encoding Reference (<http://www.student.cs.uwaterloo.ca/~isg/res/mips/opcodes>)

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