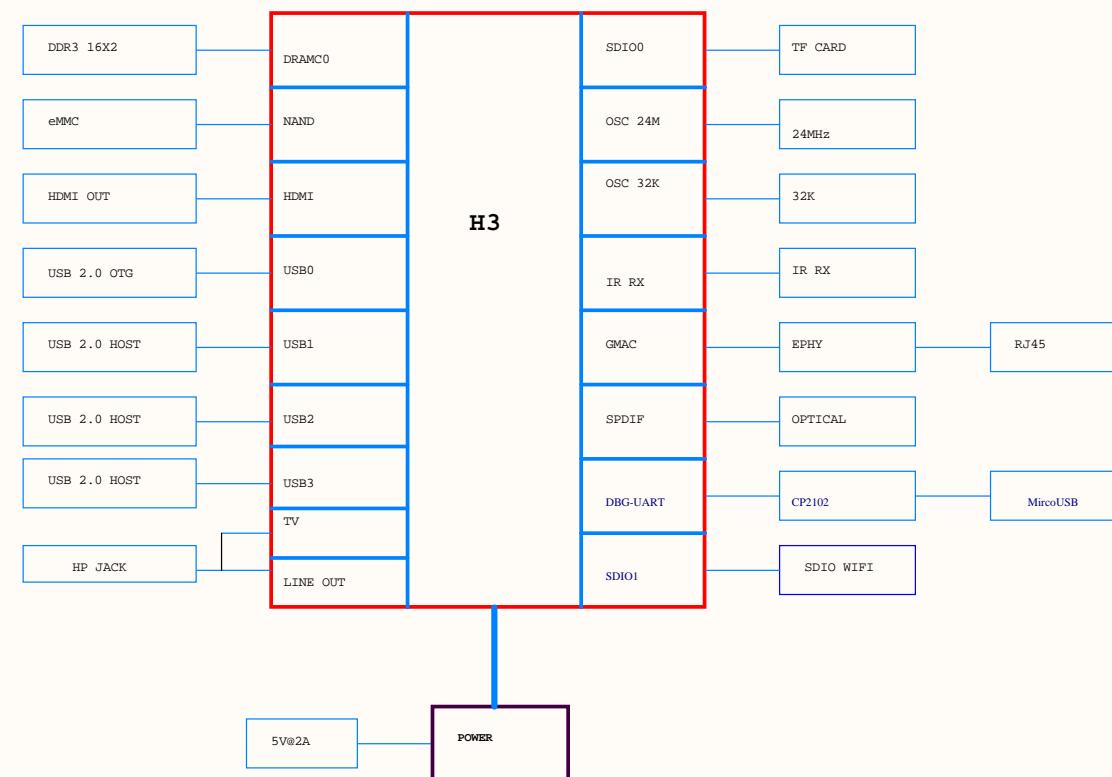


## REVISION HISTORY

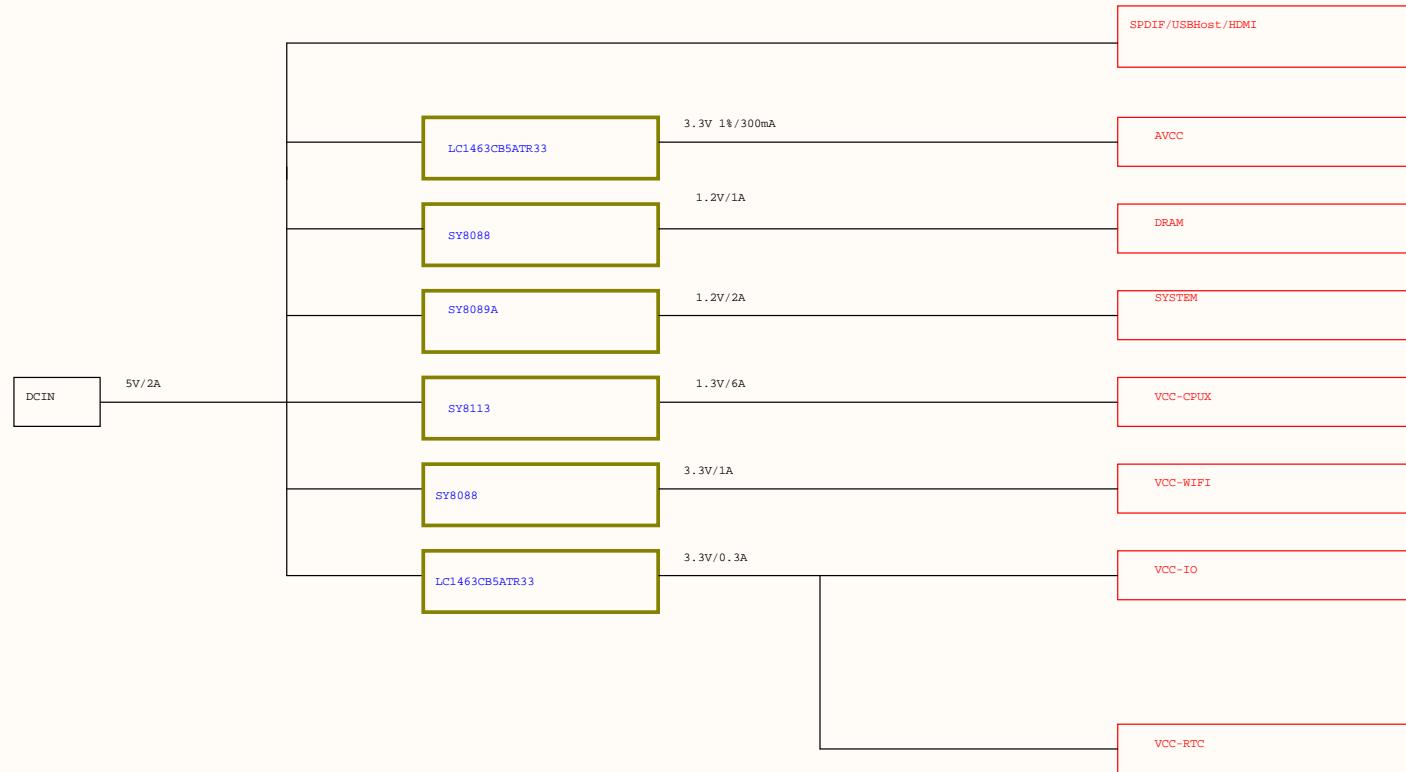
### Schematics Index:

01 REVISION HISTORY  
02 BLOCK  
03 POWER TREE  
04 GPIO ASSIGNMENT  
05 DDR3 16X2  
06 CPU  
07 POWER  
08 NAND-eMMC  
09 CARD-USB-WIFI  
10 AV-SPDIF  
11 HDMI-MISC  
12 FE-DIG  
13 HDMI  
14 POWER OPTION

Revision	Description	Date	Drawn	Checked
Ver 1.0		2015-01-05		
Ver 1.1		2015-01-23		

**BLOCK**

## POWER TREE



## GPIO ASSIGNMENT

PIN	Define	CFG	Function
PA0	SerialDevReset	3/1	
PA1	TX-DriverReset	3/1	
PA2	I2C-SCL	3/1	
PA3	SDI	3	
PA4	SART-TX	3	
PA5	SART-RX	3	
PA6	SIM-PWREN	7	
PA7	SIM-CLK	7	
PA8	SIM-DAT	7	
PA9	SIM-RST	7	
PA10	SIM-DT	7	
PA11	NC	7	
PA12	NC	7	
PA13	NC	7	
PA14	USBID	7	
PA15	STATUS-LED	1	LED
PA16	MUTE	1	AV
PA17	SPDIF-OUT	2	SPDIF
PA18	NC	7	
PA19	NC	7	
PA20	NC	7	
PA21	NC	7	

PIN	Define	CFG	Function
PC0	NWE	2/3	
PC1	NALE	2/3	
PC2	NCLE	2/3	
PC3	NCE1	2/3	
PC4	NCE0	2	
PC5	NRE	2/3	
PC6	NRB0	2/3	
PC7	NRB1	2	
PC8	NDQ0	2/3	
PC9	NDQ1	2/3	
PC10	NDQ2	2/3	
PC11	NDQ3	2/3	
PC12	NDQ4	2/3	
PC13	NDQ5	2/3	
PC14	NDQ6	2/3	
PC15	NDQ7	2/3	
PC16	NDQS	2/3	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	NC	7	
PD2	NC	7	
PD3	NC	7	
PD4	NC	7	
PD5	NC	7	
PD6	NC	7	
PD7	NC	7	
PD8	NC	7	
PD9	NC	7	
PD10	NC	7	
PD11	NC	7	
PD12	NC	7	
PD13	NC	7	
PD14	NC	7	
PD15	NC	7	
PD16	NC	7	
PD17	NC	7	

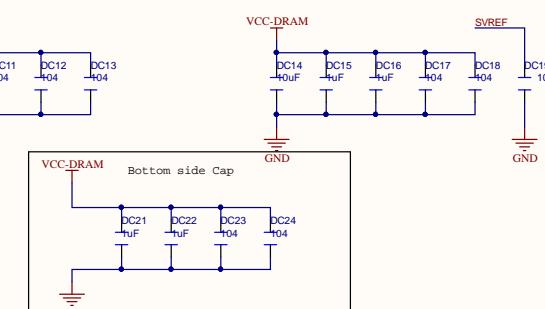
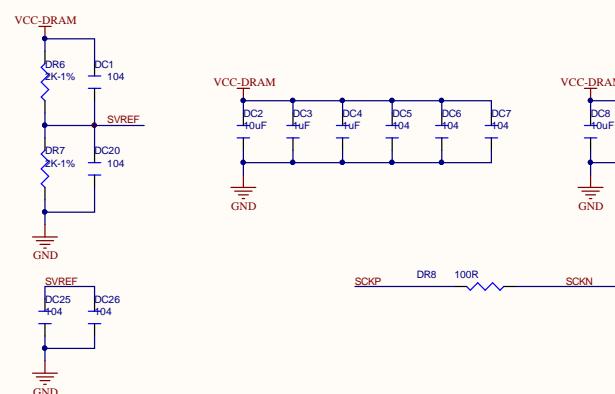
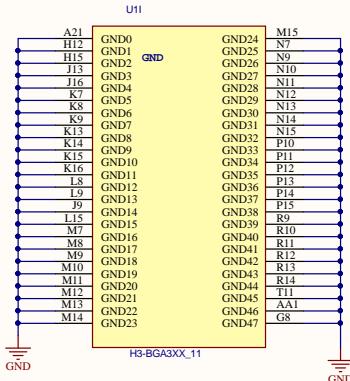
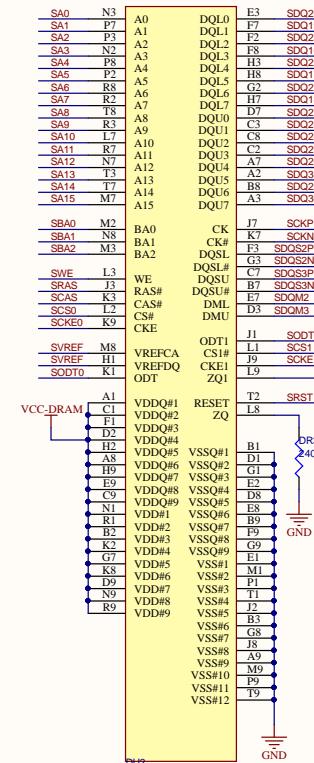
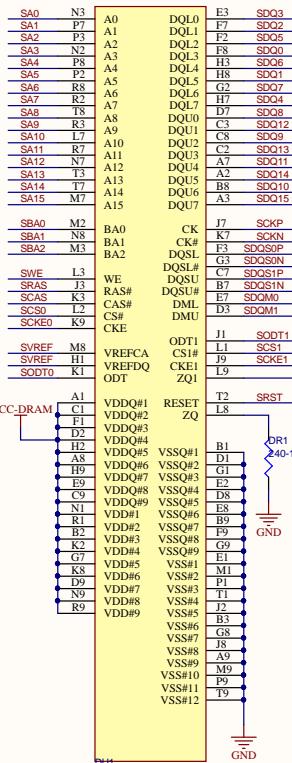
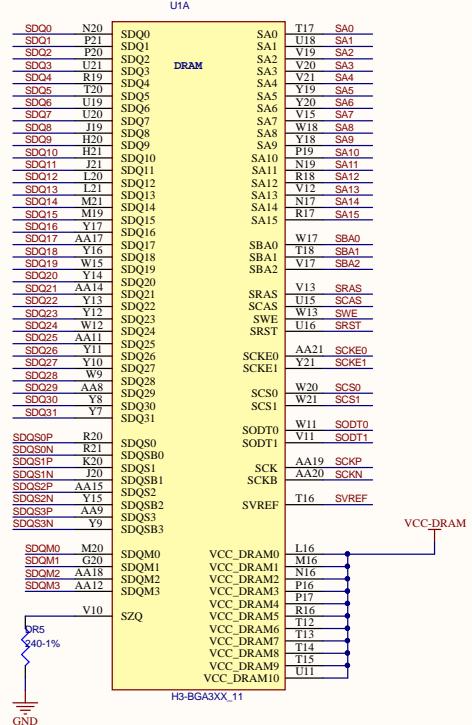
PIN	Define	CFG	Function
PE0	TS-CLK	7	
PE1	TS-ERR	7	
PE2	TS-SYNC	7	
PE3	TS-DVLD	7	
PE4	TS-D0	7	
PE5	TS-D1	7	
PE6	TS-D2	7	
PE7	TS-D3	7	
PE8	TS-D4	7	
PE9	TS-D5	7	
PE10	TS-D6	7	
PE11	TS-D7	7	
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	

PIN	Define	CFG	Function
PF0	D1	2	
PF1	D0	2	
PF2	CLK	2	
PF3	CMD	2	
PF4	D3	2	
PF5	D2	2	
PF6	DET	0	

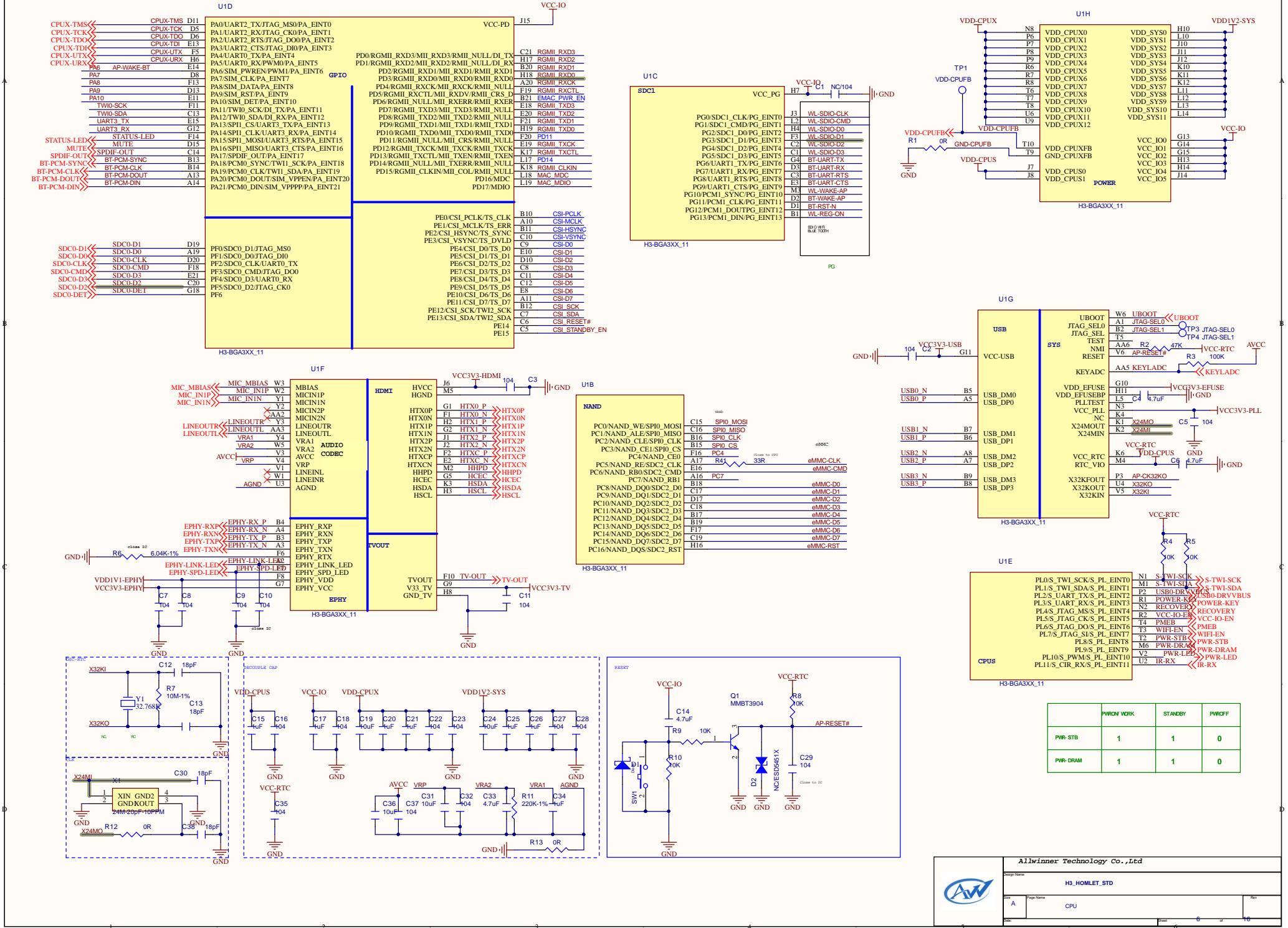
PIN	Define	CFG	Function
PG0	WL-SDIO-SCL	7	
PG1	WL-SDIO-CMD	7	
PG2	WL-SDIO-D0	7	
PG3	WL-SDIO-D1	7	
PG4	WL-SDIO-D2	7	
PG5	WL-SDIO-D3	7	
PG6	BT-UART-TX	7	
PG7	BT-UART-RX	7	
PG8	BT-UART-RXS	7	
PG9	BT-UART-CRS	7	
PG10	BT-WAKE-AP	7	
PG11	BT-WAKE-AP	7	
PG12	BT-BT-B	7	
PG13	NC	7	

PIN	Define	CFG	Function
PL0	WL	2	TWI
PL1	TWI	2	TWI
PL2	ESD0-DRVVBUS	1	USB
PL3	ESD1-DRVVBUS	1	USB
PL4	RECOVERY	0	KEY
PL5	IOC-IO-EN	1	IO-EN
PL6	IOMUX-VSET	7	IOMUX-VSET
PL7	WIFI-EN	7	WIFI-EN
PL8	PWR-STB	1	
PL9	PWR-DRAM	1	
PL10	PWR-LDO	1	
PL11	IR-RX	2	

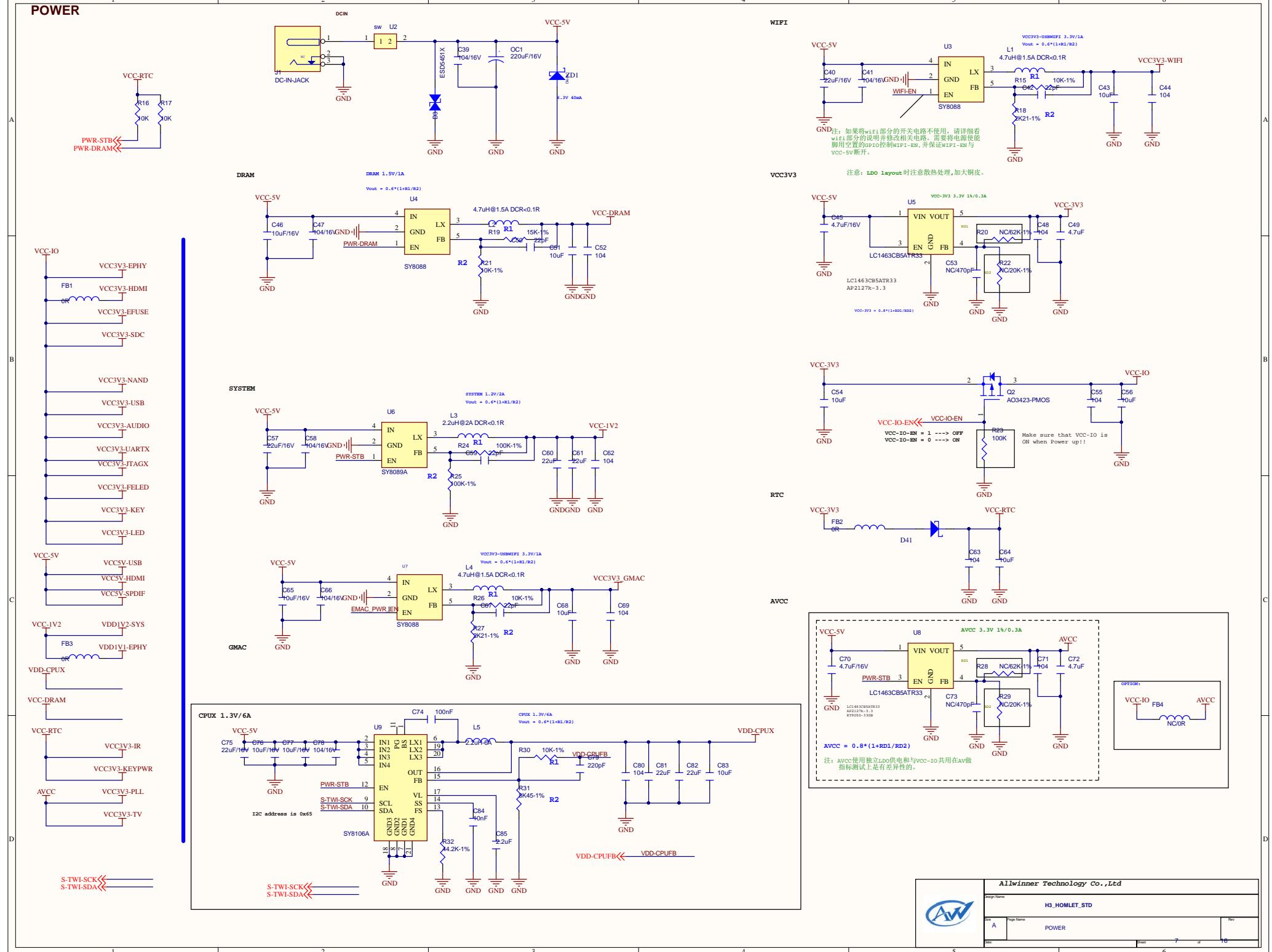
**DDR3 16x2**

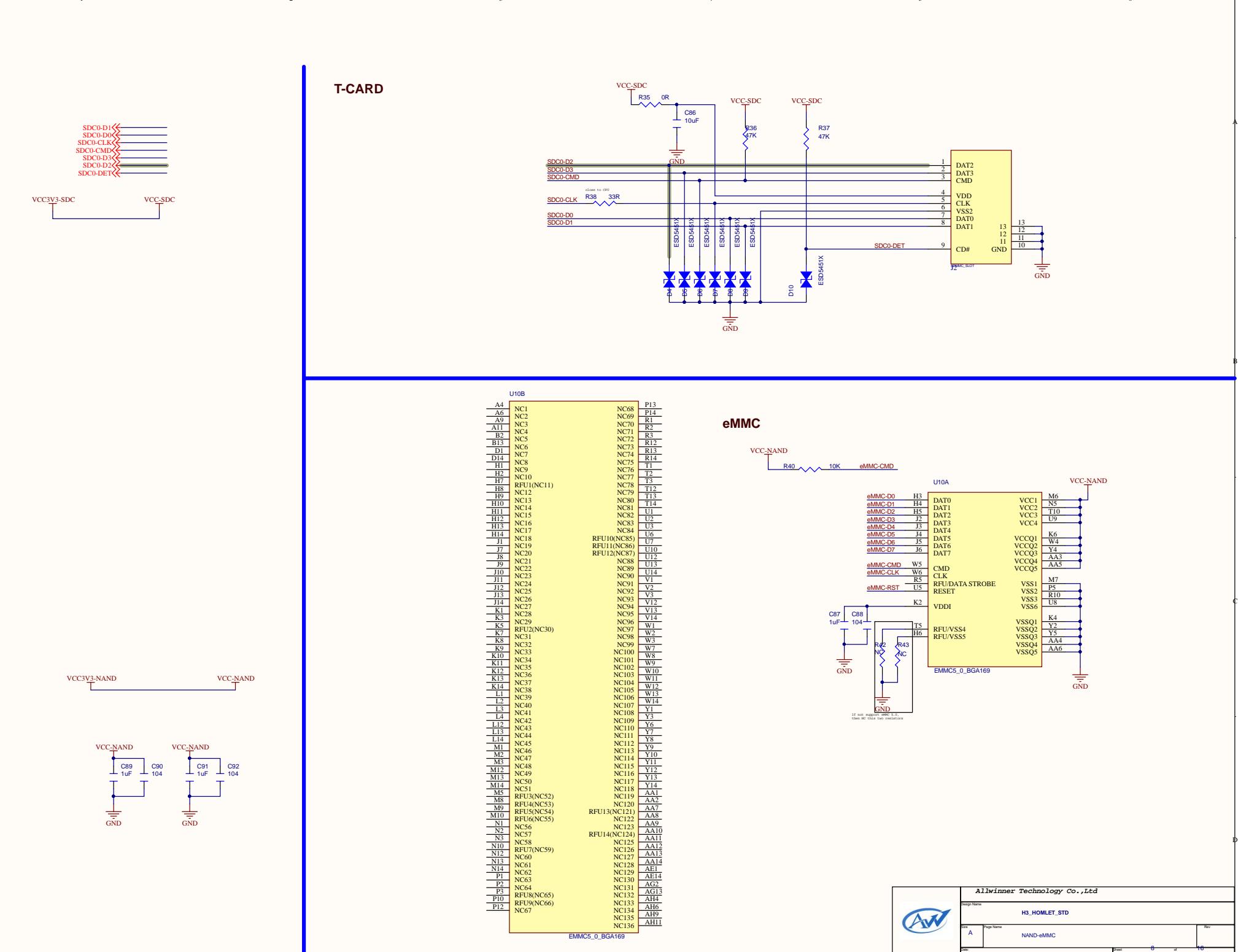


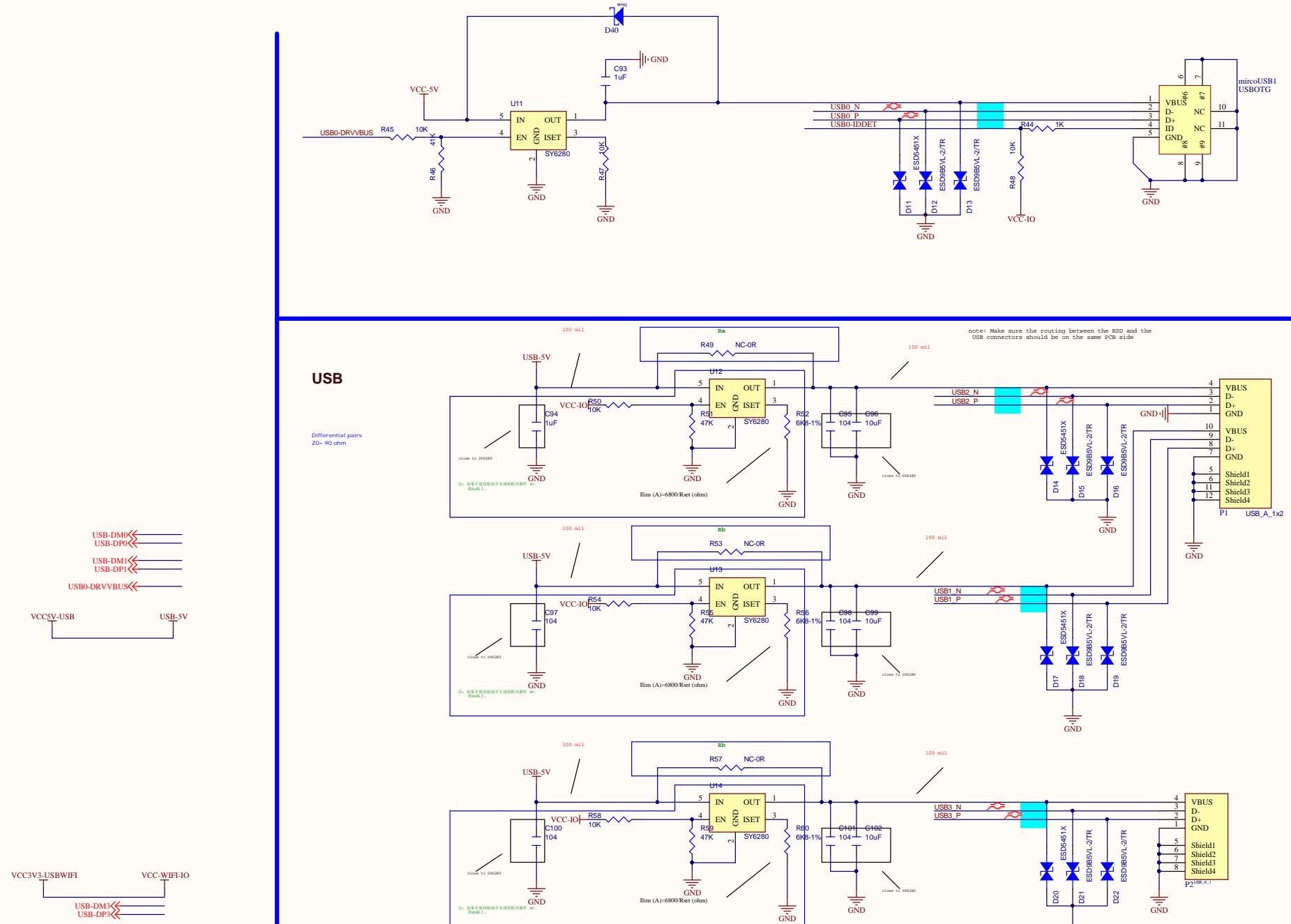
CPU



POWER

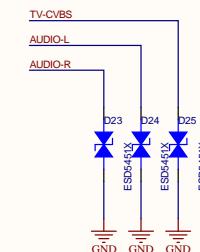
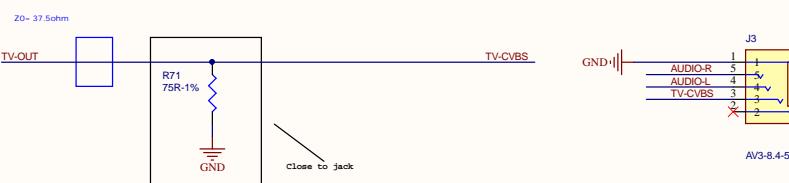




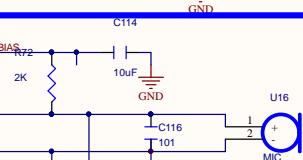
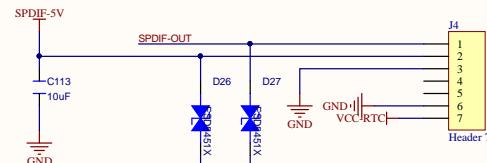


**AV**

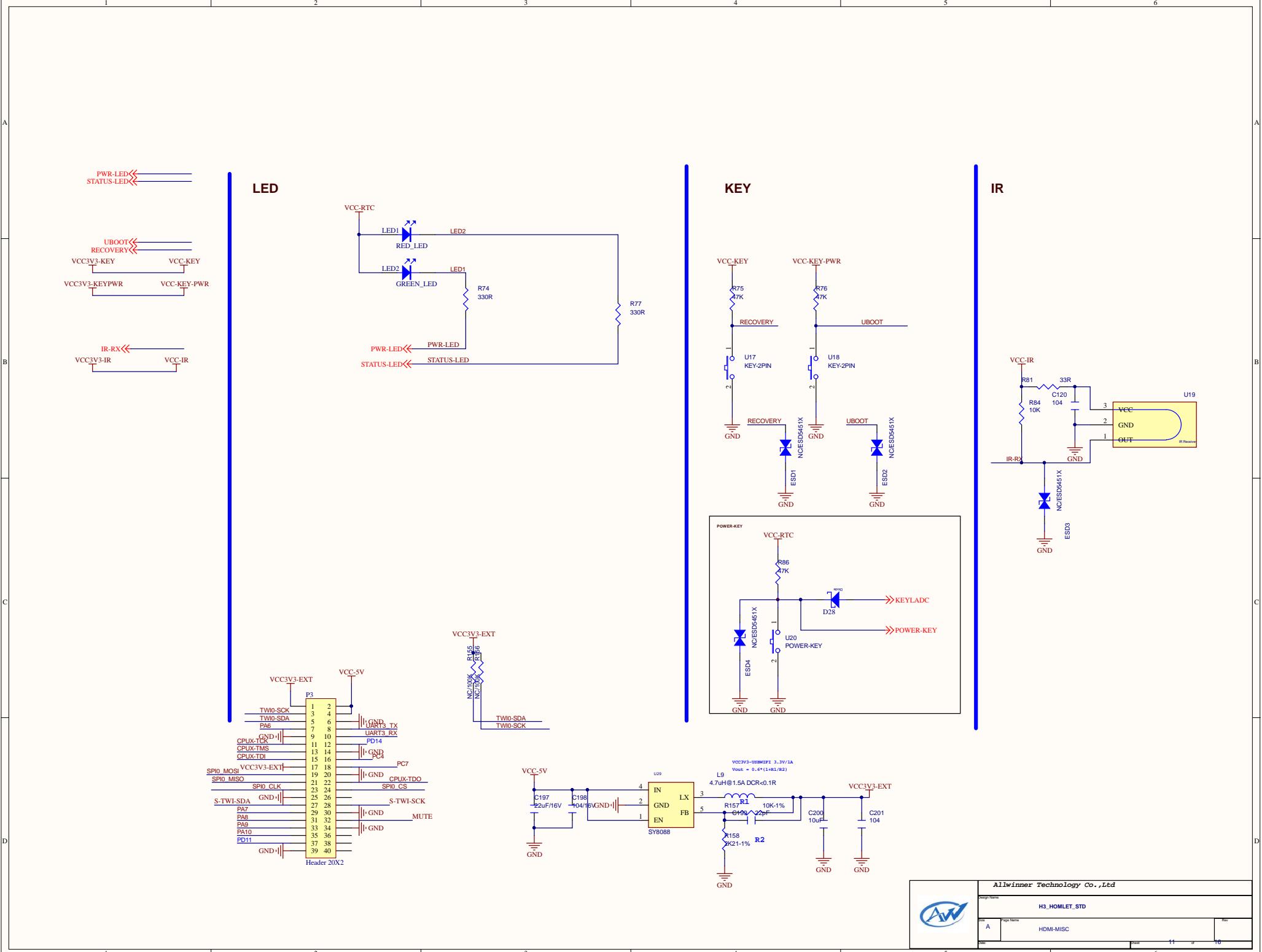
输出2Vrms

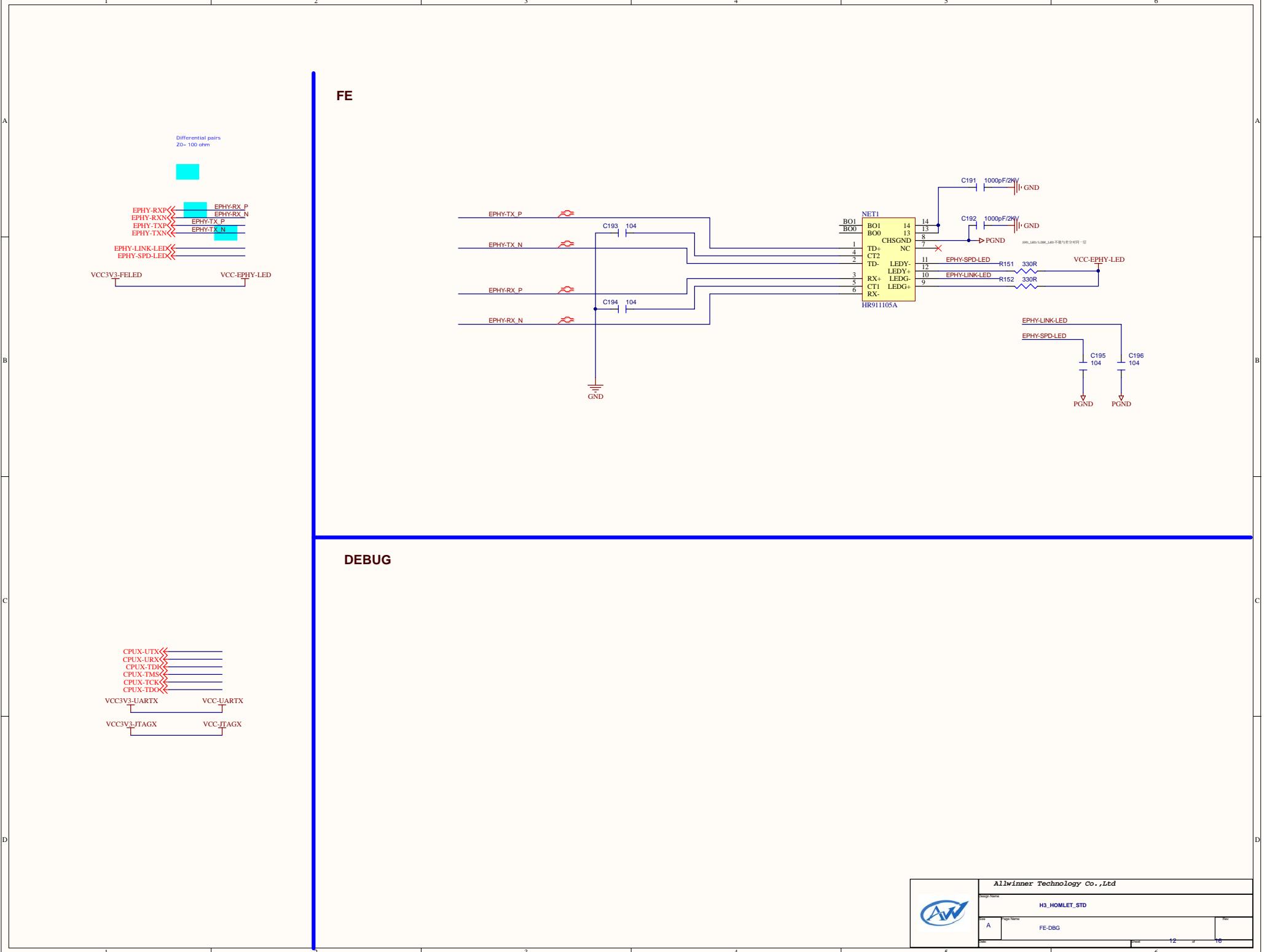


SPDIF-OUT  
VCC5V-SPDIF

**SPDIF****MIC**

MIC\_MBIAS  
MIC\_IN1P  
MIC\_IN1N

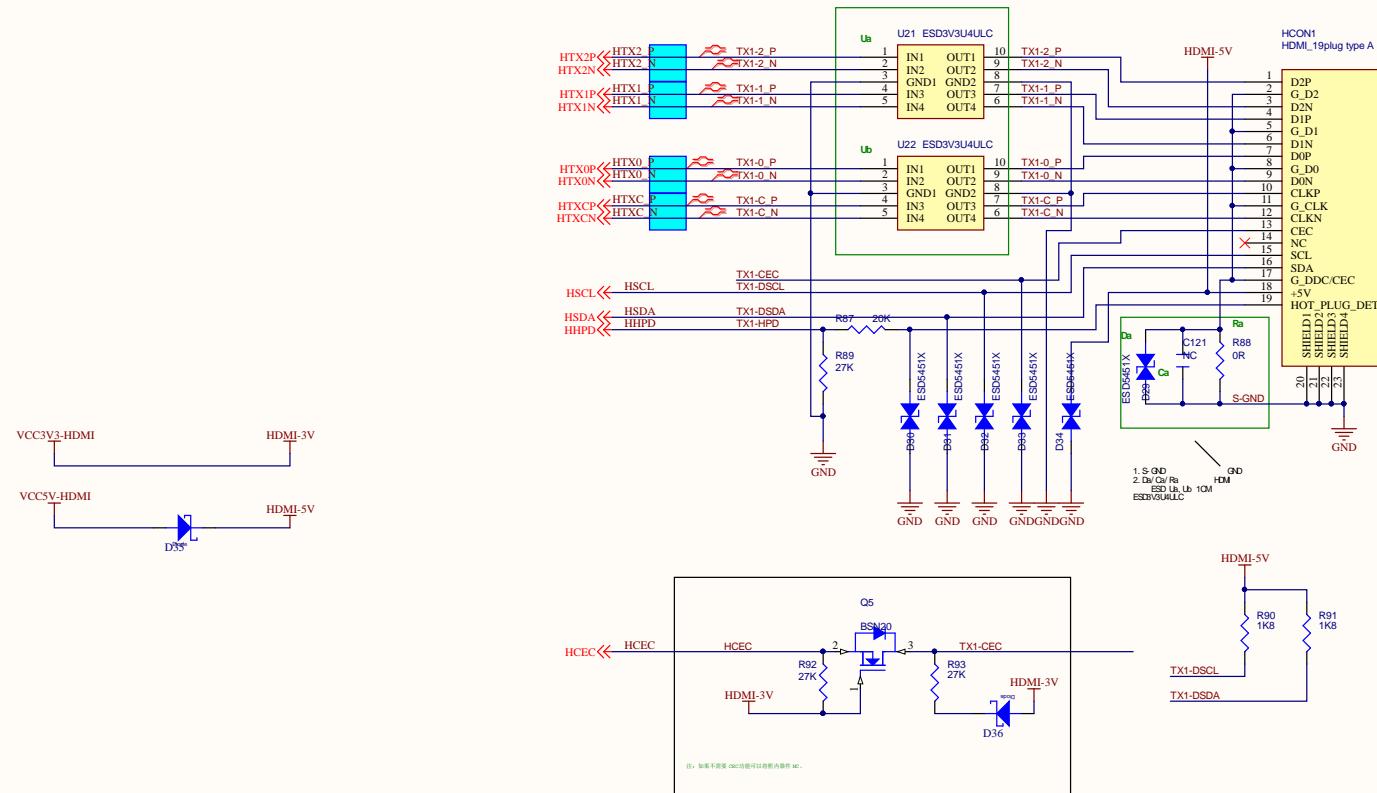




A

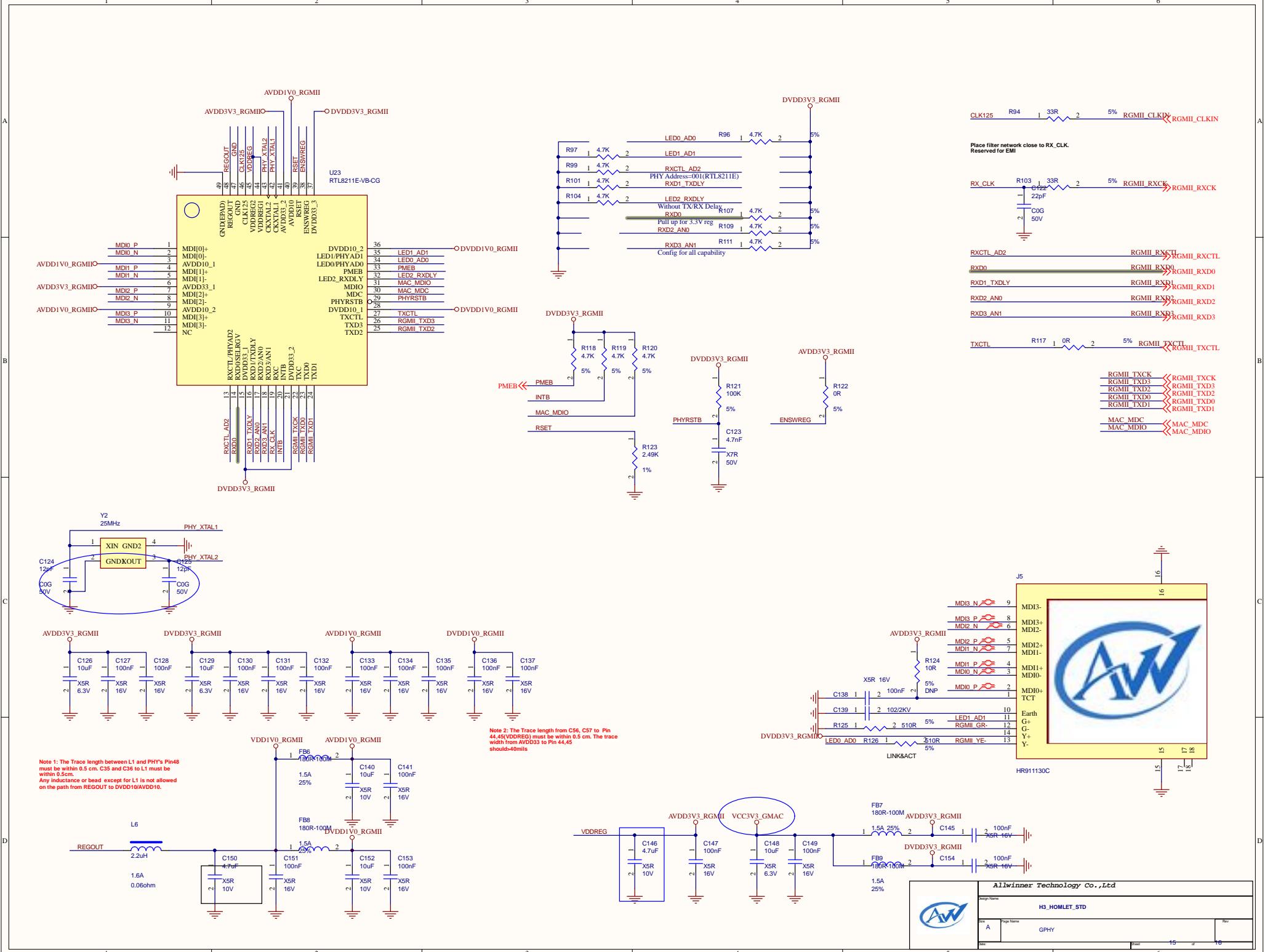
HDMI

B

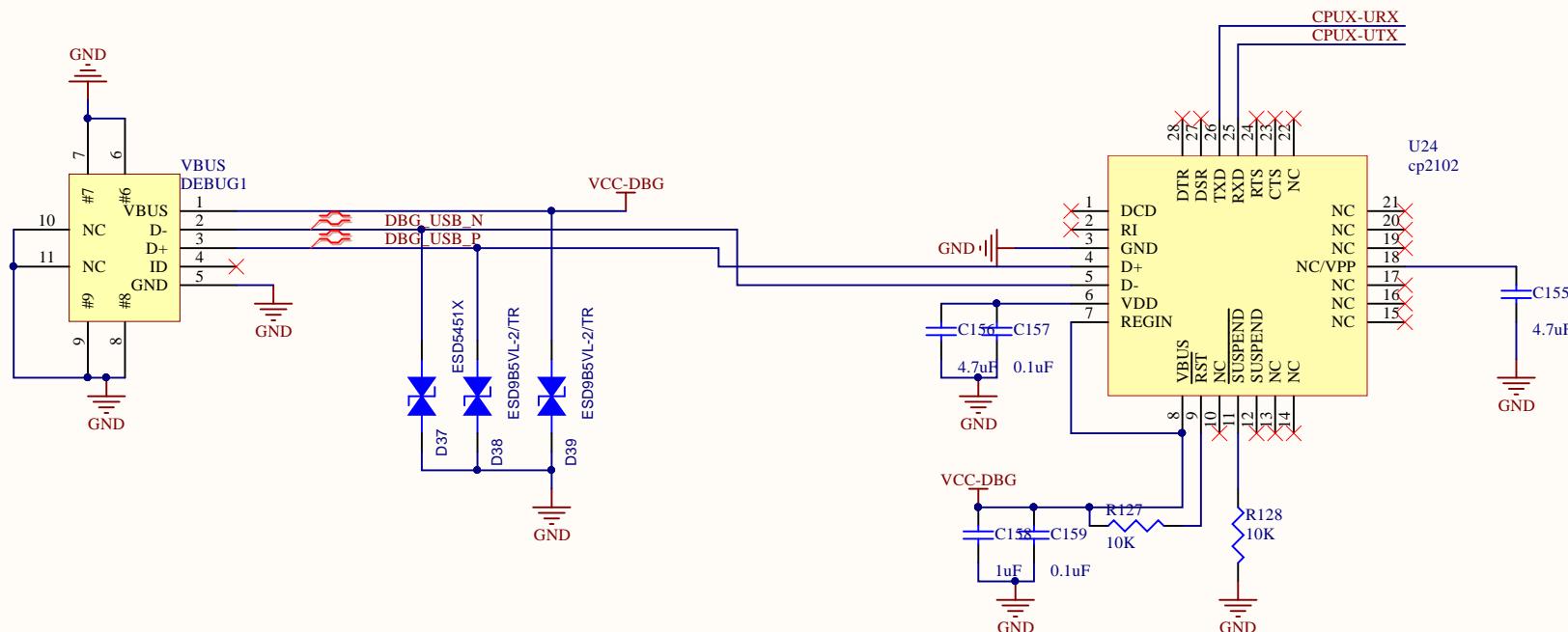


1

1



## DEBUG



Title

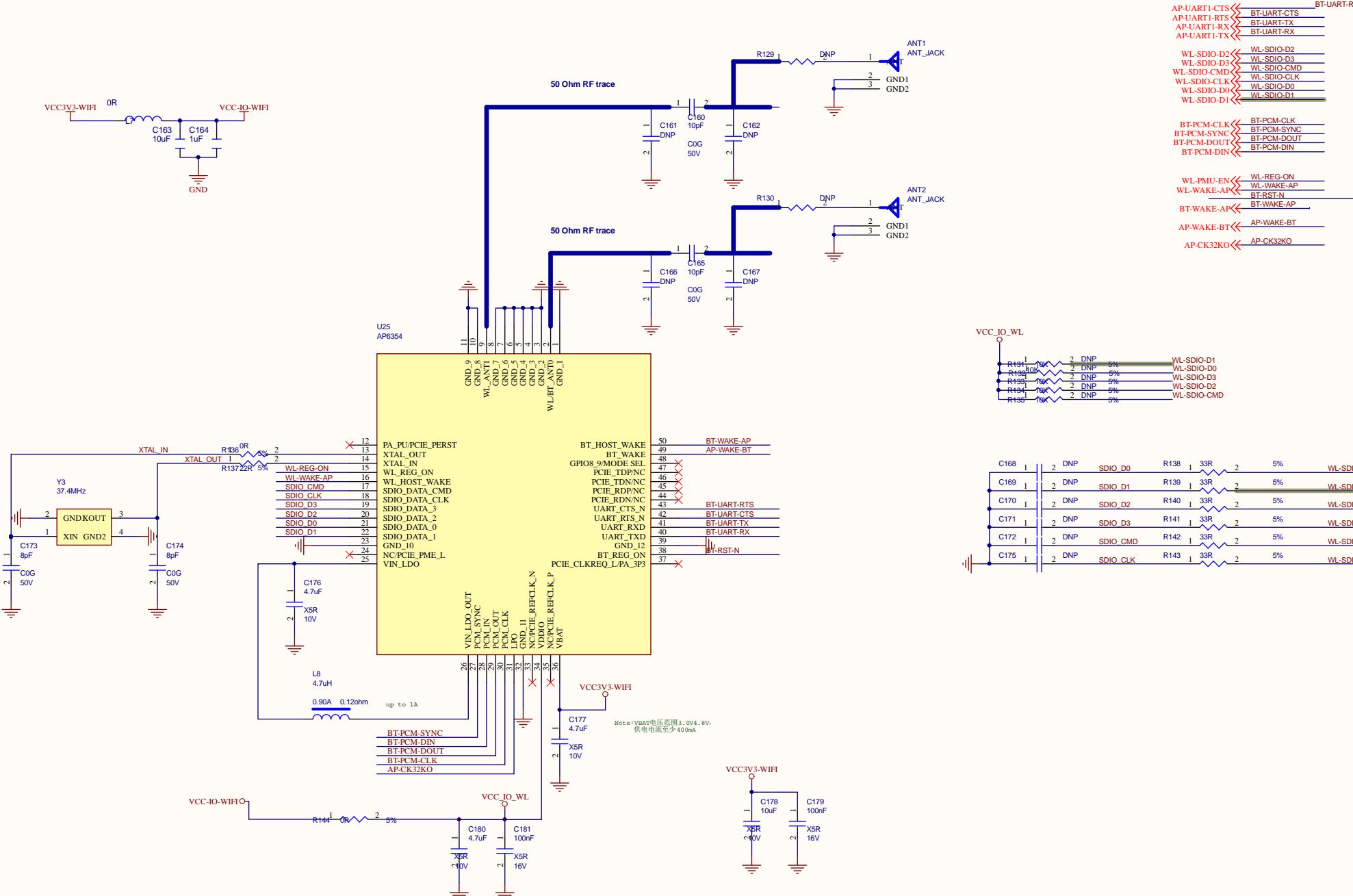
Size  
A4

Number

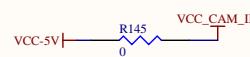
Revision

Date: 2019-08-16  
File: D:\work\...\17 usb2uart.SchDocSheet of  
Drawn By:

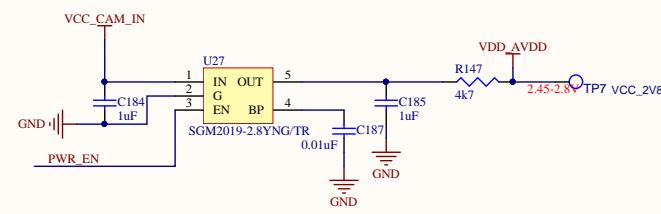
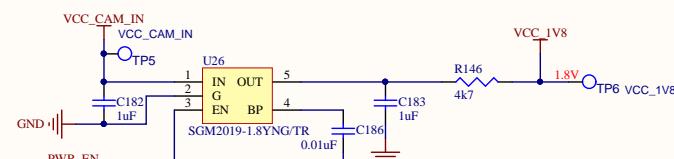
## WIFI/WIFI ac/BT MODULE



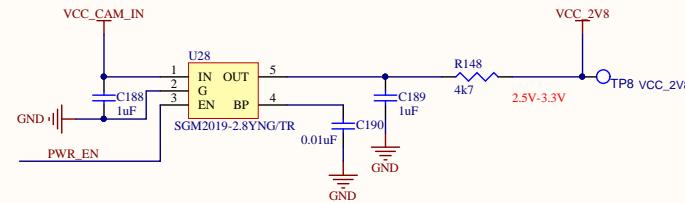
A



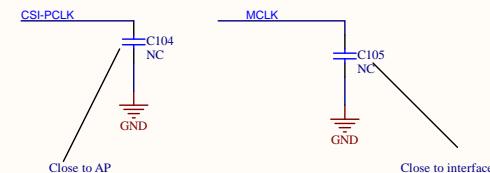
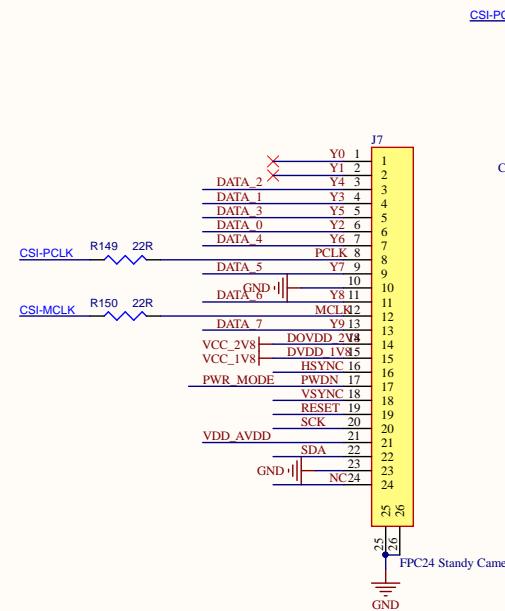
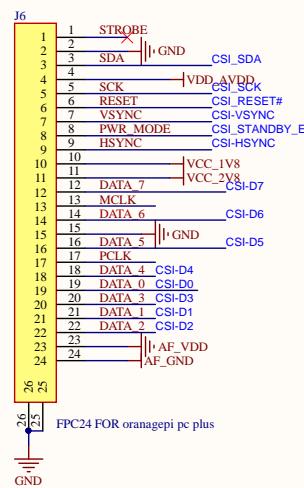
CSI-PCLK  
CSI-MCLK  
CSI-HSYNC  
CSI-VSYNC  
CSI-D0  
CSI-D1  
CSI-D2  
CSI-D3  
CSI-D4  
CSI-D5  
CSI-D6  
CSI-D7  
CSI-SCK  
CSI-SDA  
CSI\_RESET#  
CSI\_STANDBY\_EN



B



C



Allwinner Technology Co.,Ltd			
Design Name	Size	Number	Revision
A3	Page Name	HOMLEY_STD	
Date: 2019-08-16	File: D:\work\19 CAMERA.SchDoc	Sheet 11 of 11	Rev A

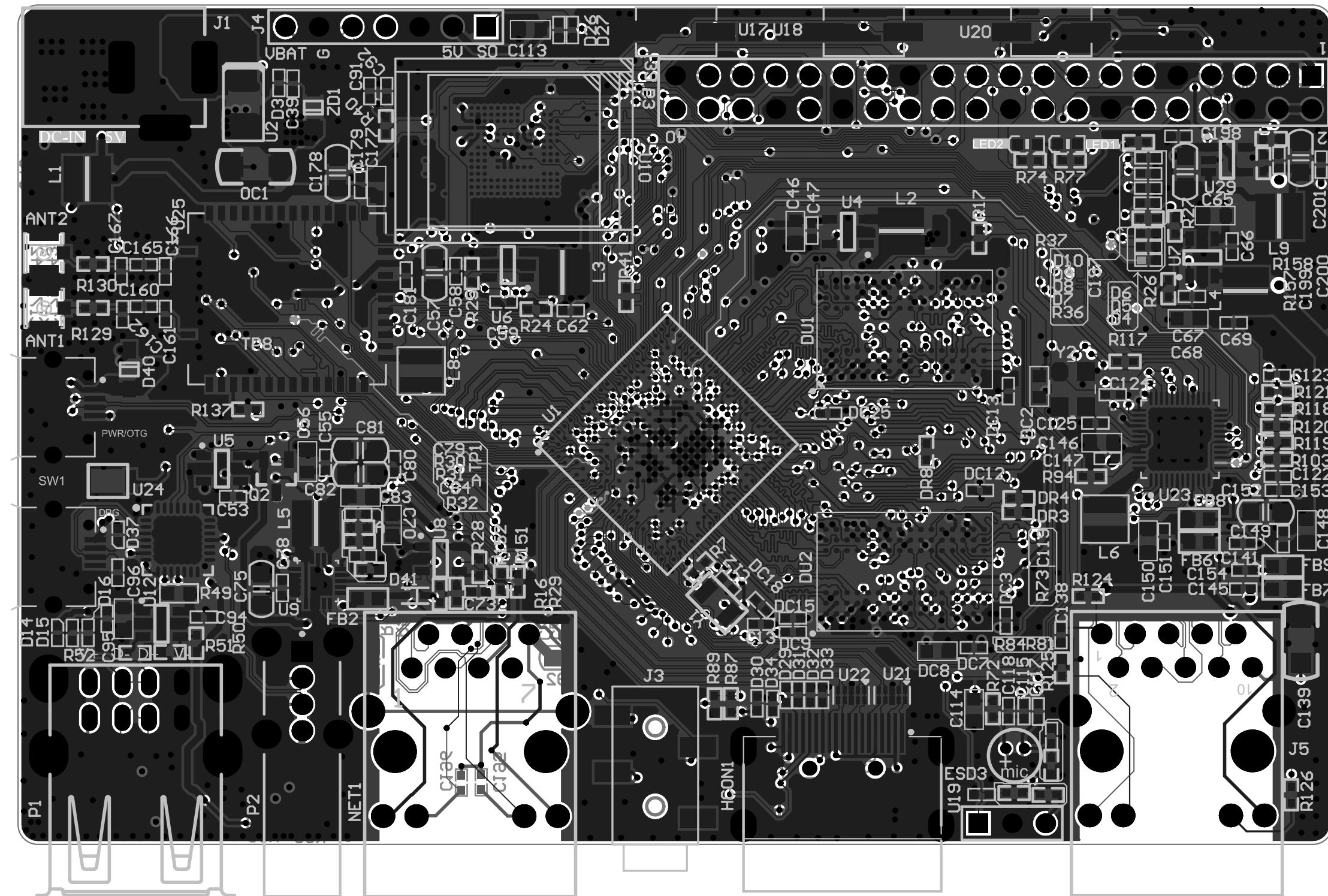
D

A

B

C

D



# Board Stack Report