UNIT 13

Analysis of Clocked Sequential Circuits

This chapter includes:

13.1 A Sequential Parity Checker
13.2 Analysis by Signal Tracing and Timing Charts
13.3 State Tables and Graphs
13.4 General Models for Sequential Circuits

Learning Objectives

1. Analyze a sequential circuit by signal tracing.
2. Given a sequential circuit, write the next-state equations for the flip-flops and derive the state graph or state table. Using the state graph, determine the state sequence and output sequence for a given input sequence.
3. Explain the difference between a Mealy machine and a Moore machine.
4. Given a state table, construct the corresponding state graph, and conversely.

Learning Objectives

5. Given a sequential circuit or a state table and an input sequence, draw a timing chart for the circuit. Determine the output sequence from the timing chart, neglecting any false outputs.

6. Draw a general model for a clocked Mealy or Moore sequential circuit. Explain the operation of the circuit in terms of these models. Explain why a clock is needed to ensure proper operation of the circuit.

A Sequential Parity Checker

Parity:

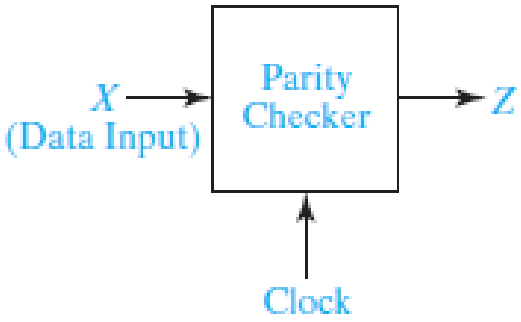
- When binary data is transmitted or stored, an extra bit (called a **parity bit**) is frequently added for purposes of error detection.
- When the total number of 1 bits in the block (including the parity bit) is odd, we say that the parity is **odd**.
- The parity bit could be chosen such that the total number of 1's in the block is even, in which case we would have **even parity**.
- If any single bit in the word is changed from 0 to 1 or vice versa, the parity changes.
- If any single bit error occurs in transmission, the presence of this error can be detected by change in parity.

A Sequential Parity Checker

Parity Checker:

- When a sequence of 0's and 1's is applied to the X input, the output of the circuit should be Z = 1 if the total number of 1 inputs received is odd.
- If data which originally had odd parity is transmitted to the circuit, a final output of Z = 0 indicates that an error in transmission has occurred.

FIGURE 13-1
Block Diagram
for Parity Checker

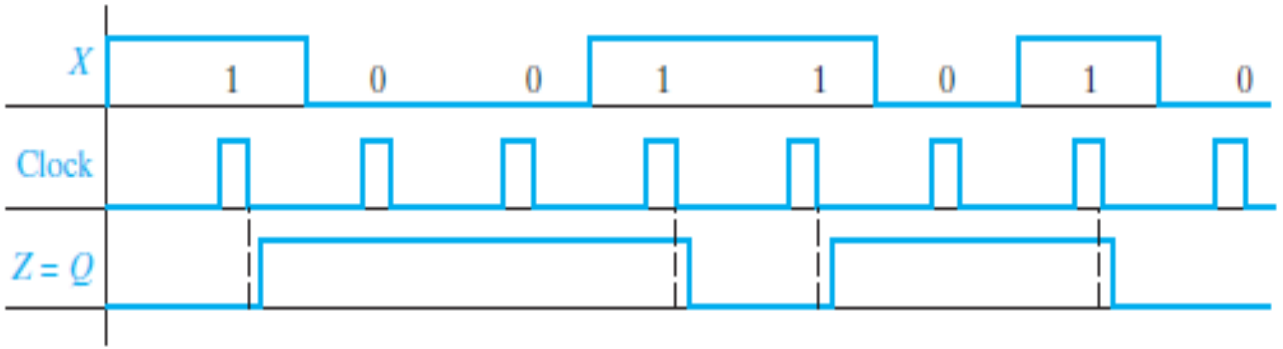


A Sequential Parity Checker

Parity Checker Clock Input:

- The value of X is read at the time of the active clock edge.
- The X input must be synchronized with the clock so that it assumes its next value before the next active clock edge.
- The clock input is necessary in order to distinguish consecutive 0's or consecutive 1's on the X input.

FIGURE 13-2
Waveforms for Parity Checker



A Sequential Parity Checker

FIGURE 13-3
State Graph for Parity Checker

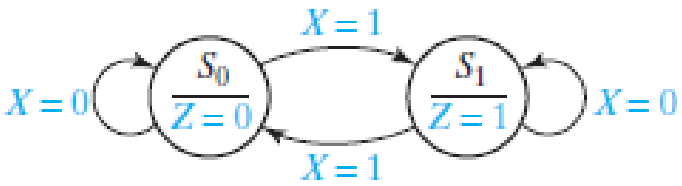


FIGURE 13-4
Parity Checker

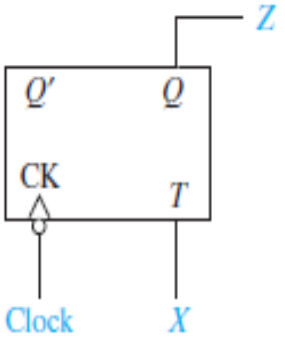


TABLE 13-1
State and Transition Tables for Parity Checker

(a)

Present State	Next State $X=0$	Next State $X=1$	Present Output
S_0	S_0	S_1	0
S_1	S_1	S_0	1

(b)

Q	Q^+ $X=0$	Q^+ $X=1$	T $X=0$	T $X=1$	Z
0	0	1	0	1	0
1	1	0	0	1	1

Analysis By Signal Tracing and Timing Charts

Basic Procedure to Find the Output Sequence By Tracing 0 and 1 Signals through the Circuit:

1. Assume an initial state of the flip-flops (all flip-flops reset to 0 unless otherwise specified).
2. For the first input in the given sequence, determine the circuit output(s) and flip-flop inputs.
3. Determine the new set of flip-flop states after the next active clock edge.
4. Determine the output(s) that corresponds to the new states.
5. Repeat 2, 3, and 4 for each input in the given sequence.

Analysis By Signal Tracing and Timing Charts

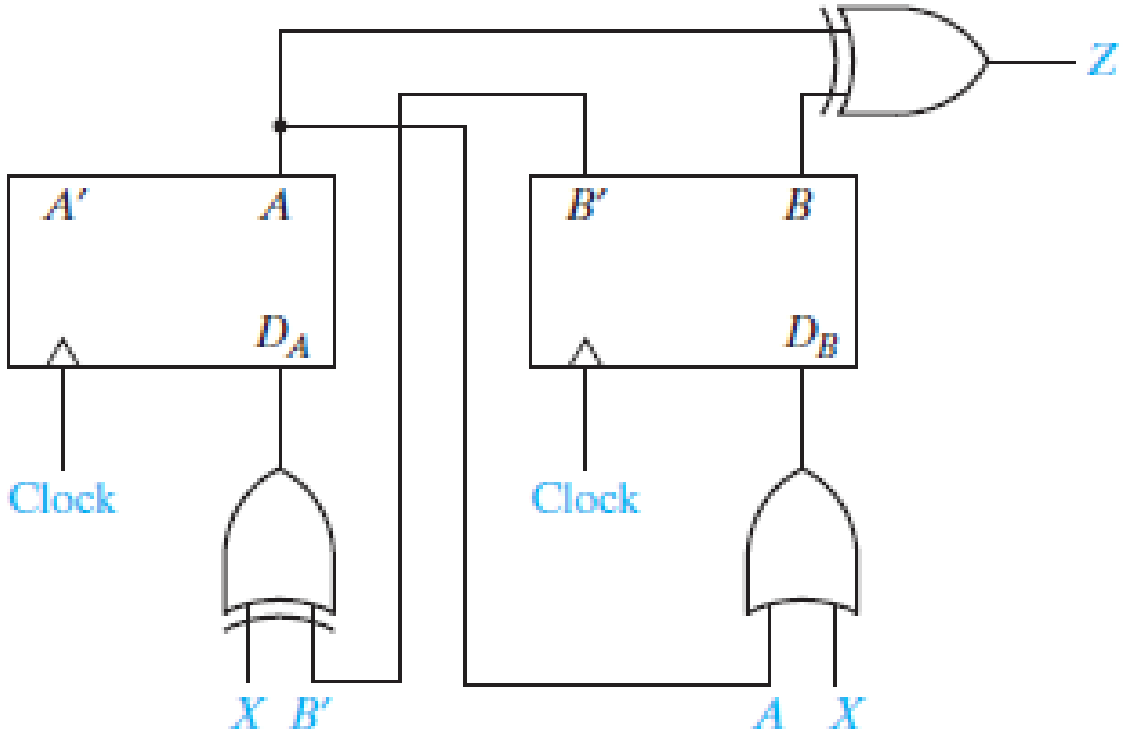
Moore and Mealy Machines:

- If the output of a sequential circuit is a function of the present state only, the circuit is often referred to as a **Moore machine**.
- The state graph for a Moore machine has the output associated with the state.
- If the output is a function of both the present state and the input, the circuit is referred to as a **Mealy machine**.
- The state graph for a Mealy machine has the output associated with the arrow going between states.

Analysis By Signal Tracing and Timing Charts

Moore Machine Example:

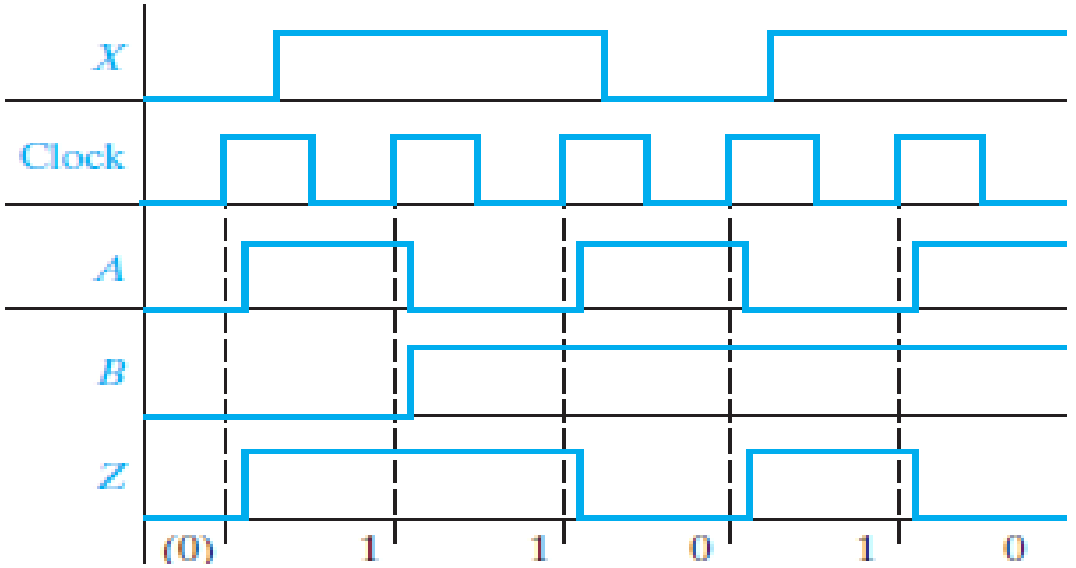
FIGURE 13-5
Moore Sequential Circuit to Be Analyzed



Analysis By Signal Tracing and Timing Charts

Moore Machine Example (continued):

FIGURE 13-6
Timing Chart for Figure 13-5

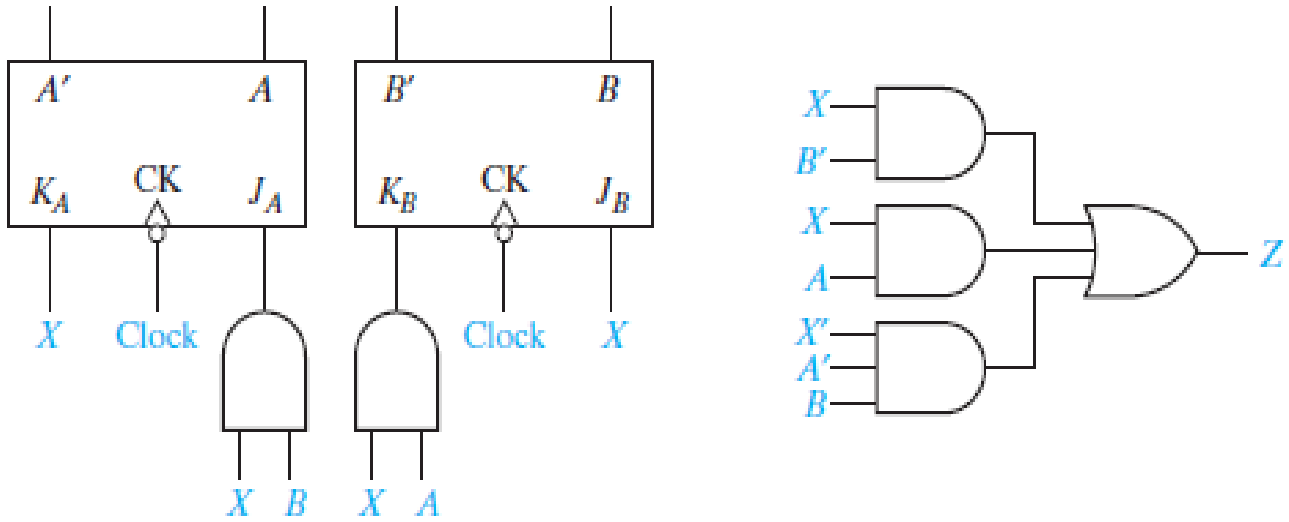


❖Note that for the Moore circuit, the output which results from application of a given input does not appear until after the active clock edge; therefore, the output sequence is displaced in time with respect to the input sequence.

Analysis By Signal Tracing and Timing Charts

Mealy Machine Example:

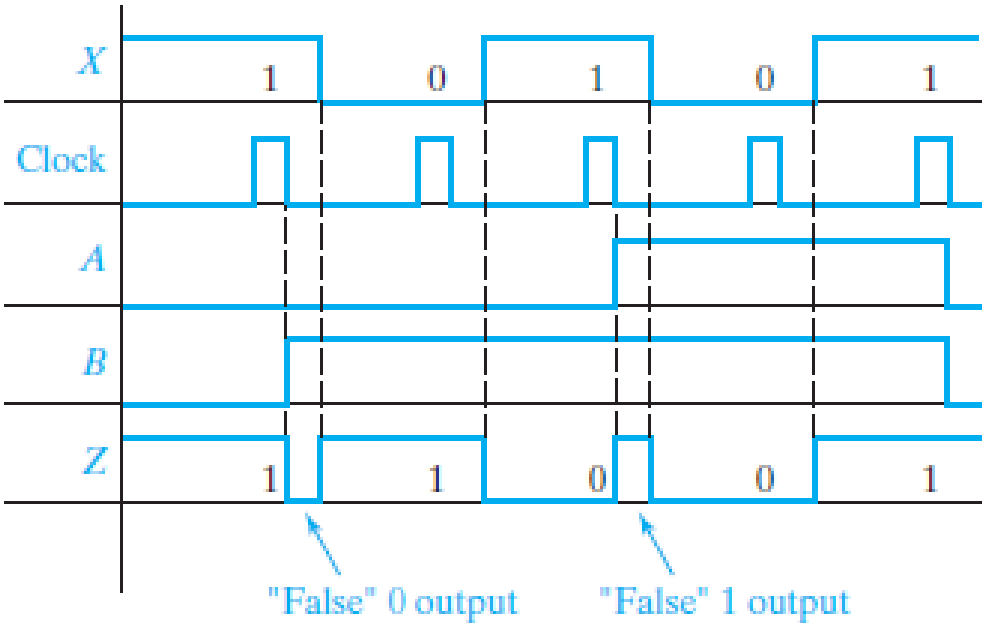
FIGURE 13-7
Mealy Sequential Circuit to Be Analyzed



Analysis By Signal Tracing and Timing Charts

Mealy Machine Example (continued):

FIGURE 13-8
Timing Chart for Circuit of Figure 13-7



Analysis By Signal Tracing and Timing Charts

False Outputs:

- After the circuit has changed state and before the input is changed, the output may temporarily assume an incorrect value, which we call a false output.
- In one case the output Z momentarily goes to 0 and returns to 1 before the active clock edge (glitch).
- In the other case, the output Z momentarily goes to 1 and returns to 0 before the active edge (spike).

State Tables and Graphs

Procedure to Construct Transition Table:

1. Determine the flip-flop input equations and the output equations from the circuit.
2. Derive the next-state equation for each flip-flop from its input equations, using one of the following relations:

D flip-flop	$Q^+ = D$	(13-1)
D-CE flip-flop	$Q^+ = D \cdot CE + Q \cdot CE'$	(13-2)
T flip-flop	$Q^+ = T \oplus Q$	(13-3)
S-R flip-flop	$Q^+ = S + R'Q$	(13-4)
J-K flip-flop	$Q^+ = JQ' + K'Q$	(13-5)

3. Plot a next-state map for each flip-flop.
4. Combine these maps to form the transition table. Such a transition table, which gives the next state of the flip-flops as a function of their present state and the circuit inputs.

- See pages 425- 426 for an application of this procedure.

State Tables and Graphs

Mealy Machine Example From Figure 13-7:

TABLE 13-3
Mealy Transition and State Tables for Figure 13-7

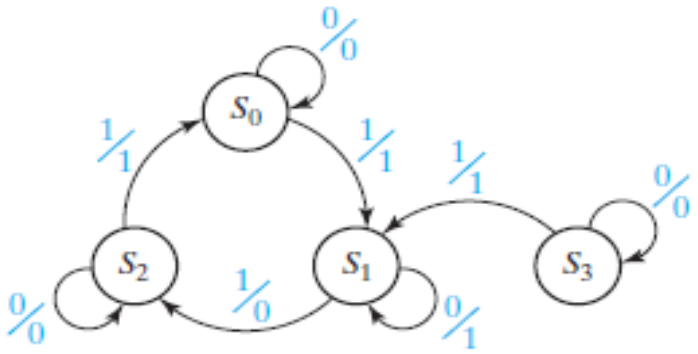
(a)

	A^+B^+		Z	
AB	$X=0$	1	$X=0$	1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

(b)

Present State	Next State $X=0$	1	Present Output $X=0$	1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

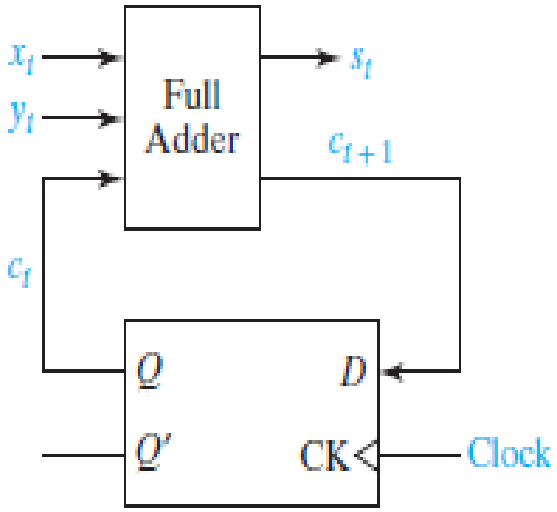
FIGURE 13-11
Mealy State Graph for Figure 13-7



State Tables and Graphs

Serial Adder Example:

FIGURE 13-12
Serial Adder



(a) With D flip-flop

x_i	y_i	c_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(b) Truth table

State Tables and Graphs

Serial Adder Example (continued):

FIGURE 13-13
Timing Diagram for Serial Adder

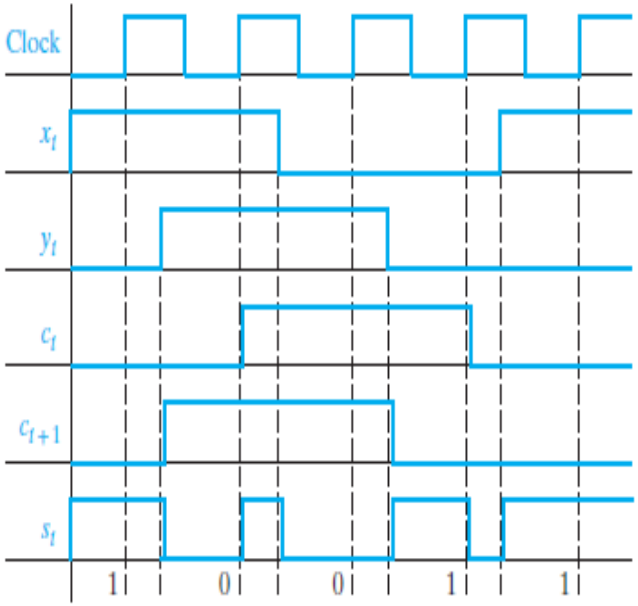
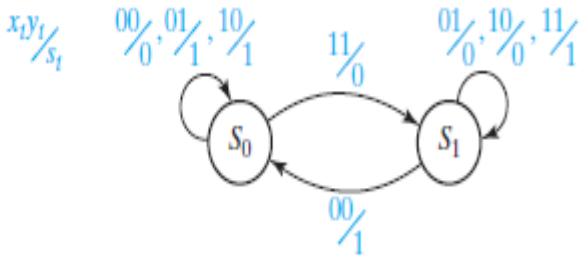


FIGURE 13-14
State Graph for Serial Adder



State Tables and Graphs

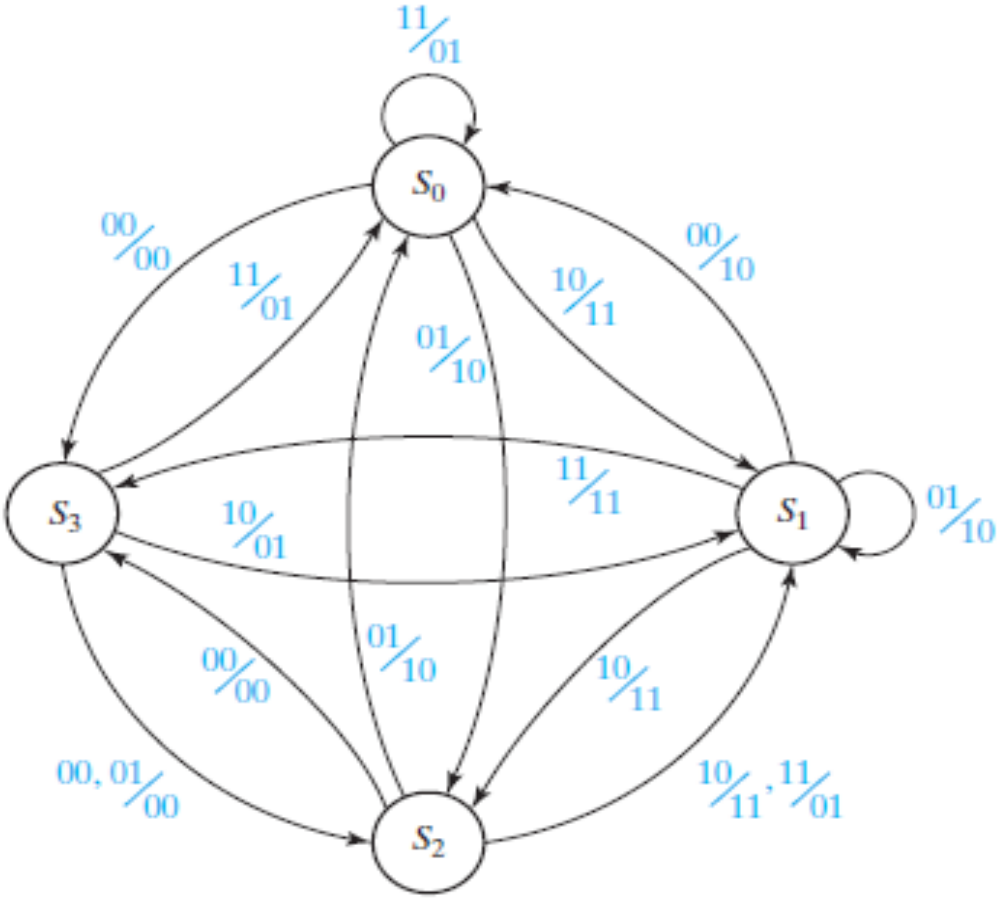
Mealy Sequential Circuit with Two Inputs and Two Outputs:

TABLE 13-4
A State Table with Multiple Inputs and Outputs

Present State	Next State X_1X_2 = 00	01	10	11	Present Output (Z_1Z_2) X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

State Tables and Graphs

FIGURE 13-15
State Graph for Table 13-4



State Tables and Graphs

Procedure to Construct and Interpret Timing Charts:

1. When constructing timing charts, note that a state change can only occur after the rising (or falling) edge of the clock, depending on the type of flip-flop used.
2. The input will normally be stable immediately before and after the active clock edge.
3. For a Moore circuit, the output can change only when the state changes, but for a Mealy circuit, the output can change when the input changes as well as when the state changes. A false output may occur between the time the state changes and the time the input is changed to its new value. (In other words, if the state has changed to its next value, but the old input is still present, the output may be temporarily incorrect.)
4. False outputs are difficult to determine from the state graph, so use either signal tracing through the circuit or use the state table when constructing timing charts for Mealy circuits.

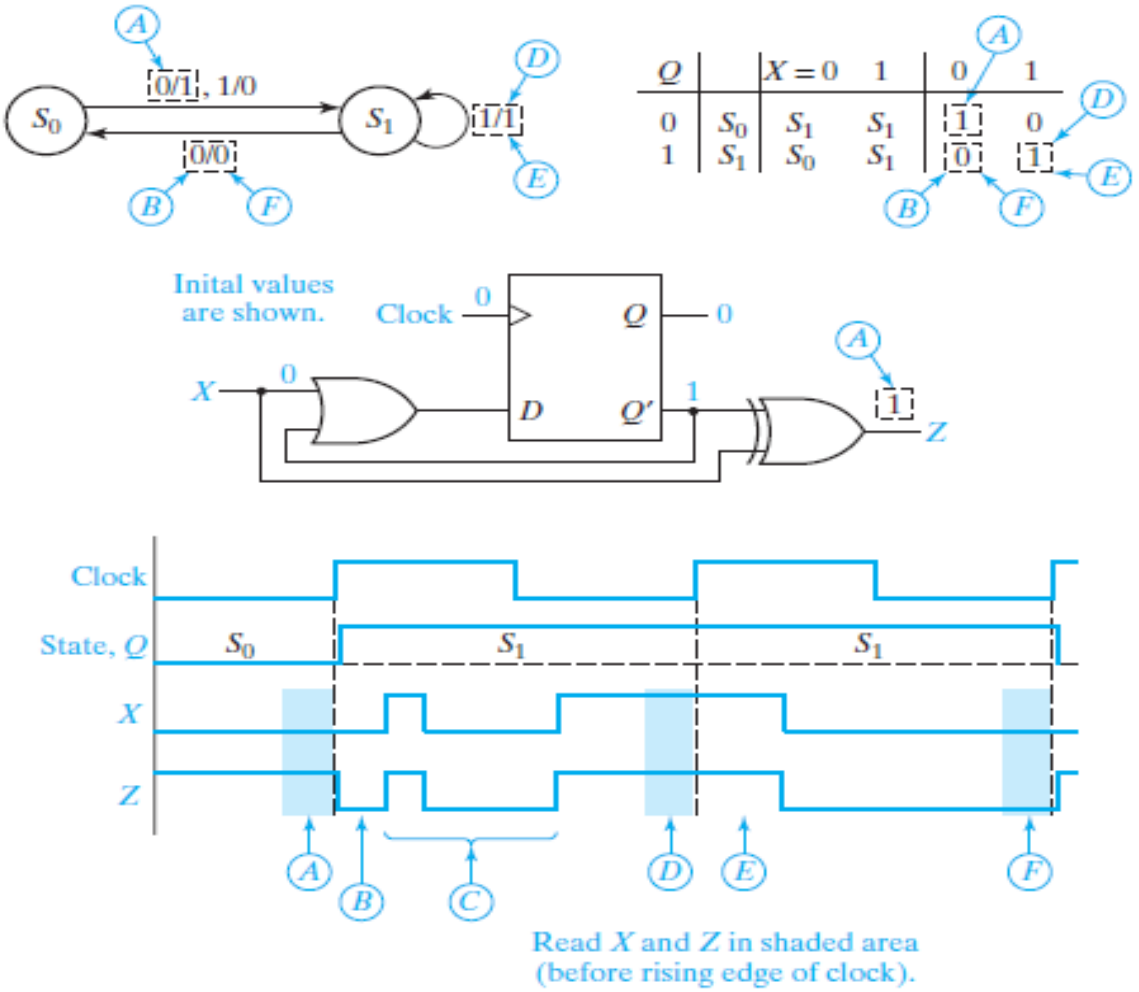
State Tables and Graphs

Procedure to Construct and Interpret Timing Charts (continued):

5. When using a Mealy state table for constructing timing charts, the procedure is as follows:
   (a) For the first input, read the present output and plot it.
   (b) Read the next state and plot it (following the active edge of the clock pulse).
   (c) Go to the row in the table which corresponds to the next state and read the output under the old input column and plot it. (This may be a false output.)
   (d) Change to the next input and repeat steps (a), (b), and (c).
   (Note: If you are just trying to read the correct output sequence from the table, step (c) is naturally omitted.)
6. For Mealy circuits, the best time to read the output is just before the active edge of the clock, because the input(s) must be stable at that time and the output will be correct.

State Tables and Graphs

FIGURE 13-16



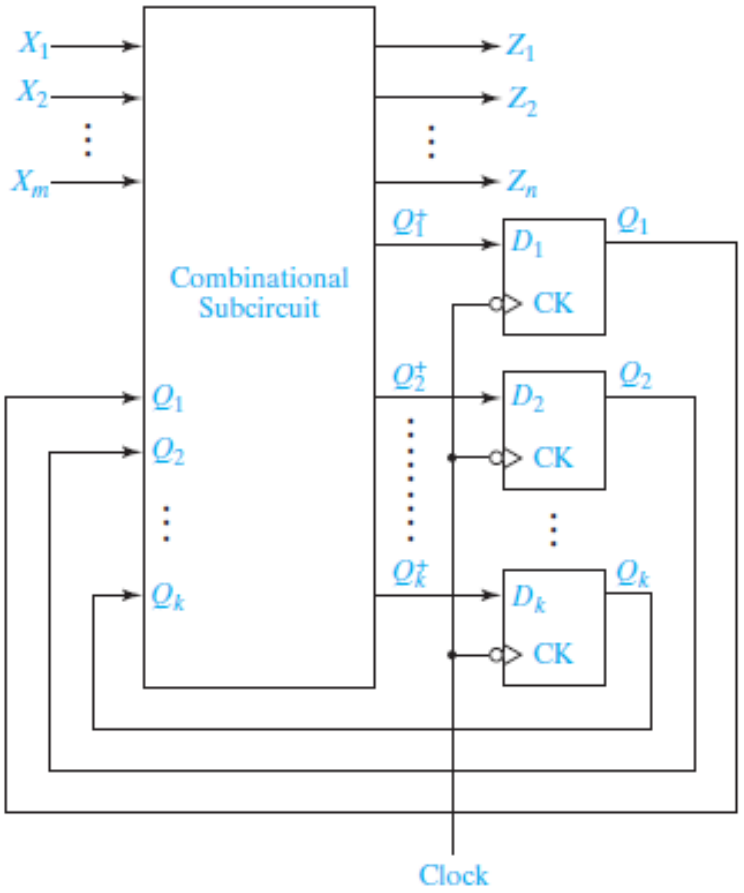
General Models for Sequential Circuits

General Form:

- A sequential circuit can be divided conveniently into two parts—the flip-flops (which serve as memory) and combinational logic which realizes the input and output functions.
- The combinational logic may be implemented with gates, with a ROM, or with a PLA.
- Figure 13-17 (next slide) illustrates the general model for a clocked Mealy sequential circuit with m inputs, n outputs, and k clocked D flip-flops used as memory.

General Models for Sequential Circuits

FIGURE 13-17
General Model for Mealy Circuit Using Clocked D Flip-Flops



General Models for Sequential Circuits

The combinational circuit realizes the n output functions and the k next-state functions, which serve as inputs to the D flip-flops:

$$\left.\begin{aligned} Z_1 &= f_1(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ Z_2 &= f_2(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ &\vdots \\ Z_n &= f_n(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \end{aligned}\right\} \; n \text{ output functions}$$

$$\left.\begin{aligned} Q_1^+ = D_1 &= g_1(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ Q_2^+ = D_2 &= g_2(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \\ &\vdots \\ Q_k^+ = D_k &= g_k(X_1, X_2, \ldots, X_m, Q_1, Q_2, \ldots, Q_k) \end{aligned}\right\} \; k \text{ next-state functions}$$

General Models for Sequential Circuits

Determining Minimum Clock Period:

- The minimum clock period is:

$$t_{clk}(min) = t_p + t_c + t_{su}$$

assuming X inputs are stable after $t_c + t_{su}$.

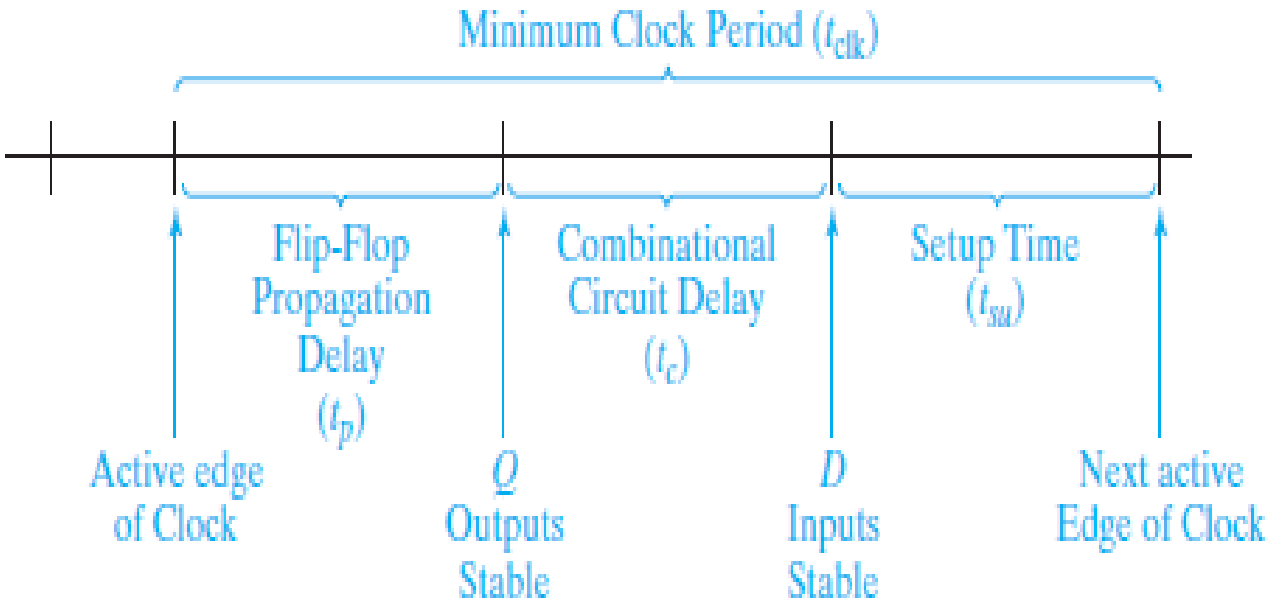
- If this isn't the case, the expression below is used to find the minimum clock period.

$$t_{clk}(min) = t_x + t_c + t_{su}$$

where t_x is the time after the active clock edge at which the X inputs are stable.

General Models for Sequential Circuits

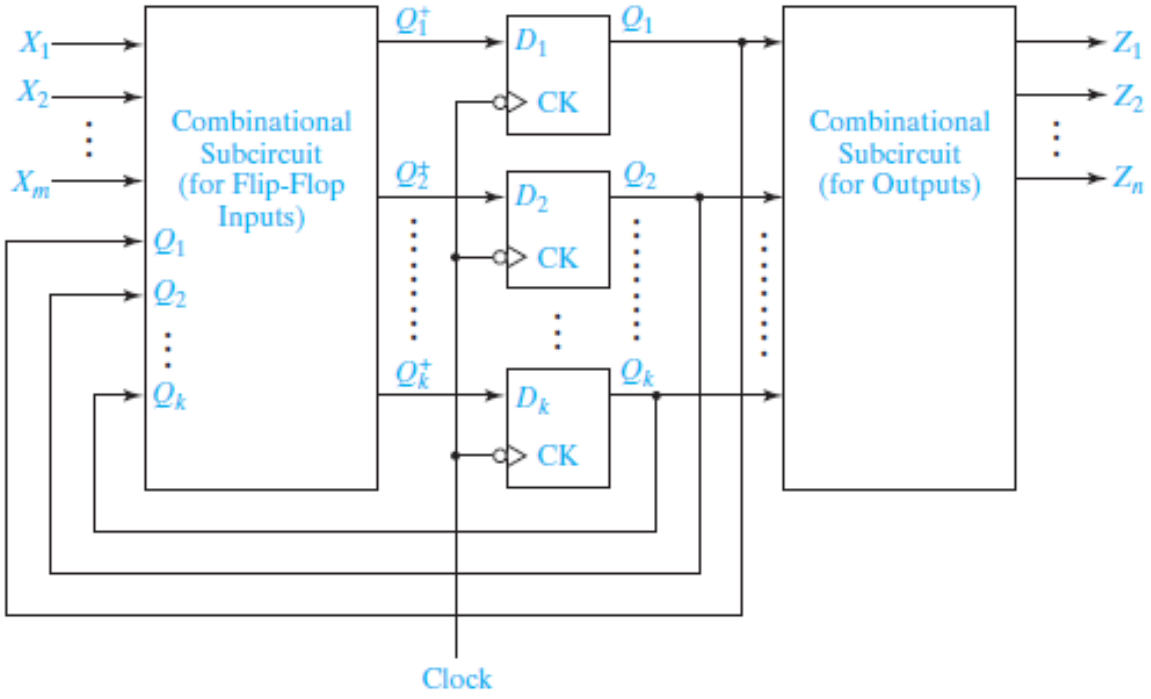
FIGURE 13-18
Minimum Clock Period for a Sequential Circuit



General Models for Sequential Circuits

General Model for Moore Circuit Using Clocked D Flip-Flops:

FIGURE 13-19
General Model for Moore Circuit Using Clocked D Flip-Flops



General Models for Sequential Circuits

TABLE 13-5
State Table with Multiple Inputs and Outputs

Present State	Next State $X=0$	1	2	3	Present Output (Z) $X=0$	1	2	3
S_0	S_3	S_2	S_1	S_0	0	2	3	1
S_1	S_0	S_1	S_2	S_3	2	2	3	3
S_2	S_3	S_0	S_1	S_1	0	2	3	1
S_3	S_2	S_2	S_1	S_0	0	0	1	1