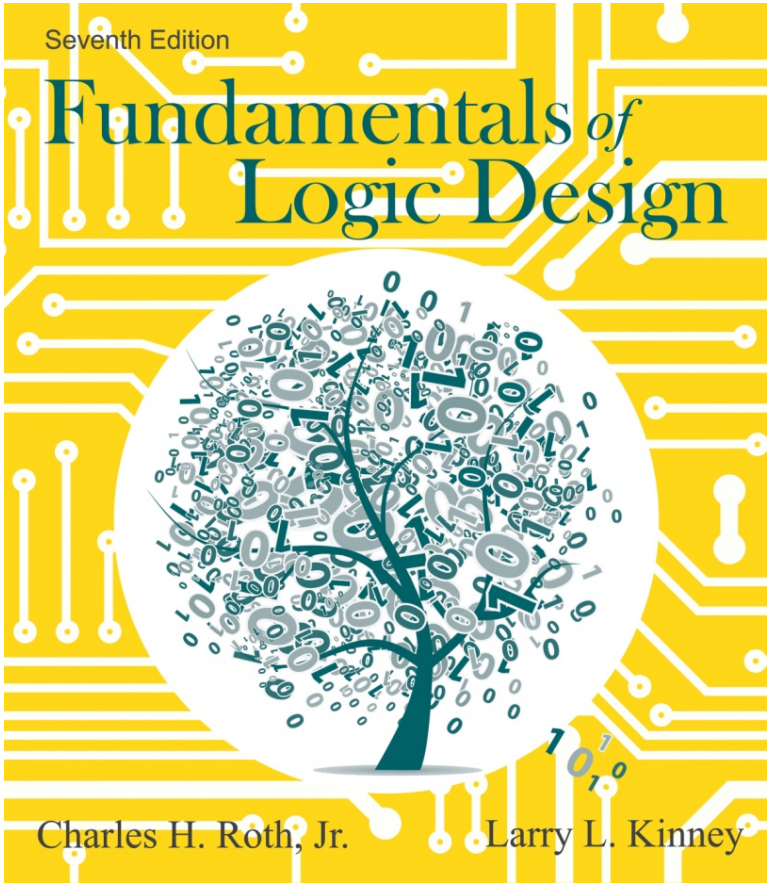



# UNIT 11

## Latches and Flip-Flops

***This chapter includes:***

# Learning Objectives

1. Explain in words the operation of S-R and gated D latches.
2. Explain in words the operation of D, D-CE, S-R, J-K, and T flip-flops.
3. Make a table and derive the characteristic (next-state) equation for such latches and flip-flops. State any necessary restrictions on the input signals.
4. Draw a timing diagram relating the input and output of such latches and flip-flops.
5. Show how latches and flip-flops can be constructed using gates. Analyze the operation of a flip-flop that is constructed of gates and latches.

# Introduction

- **Sequential switching circuits** have the property that the output depends not only on the present input but also on the past sequence of inputs.
- In effect, these circuits must be able to "remember" something about the past history of the inputs in order to produce the present output.
- **Latches** and **flip-flops** are commonly used memory devices in sequential circuits.
- Basically, latches and flip-flops are memory devices which can assume one of two stable output states and which have one or more inputs that can cause the output state to change.

# Introduction

**Flip-Flops and Latches:**

- In synchronous digital systems, it is common practice to synchronize the operation of all flip-flops by a common clock or pulse generator.
- Each of the flip-flops has a clock input, and the flip-flops are memory devices that can only change output in response to a clock input, not data inputs.
- A memory element that has no clock input is often called a latch, and we will follow this practice.

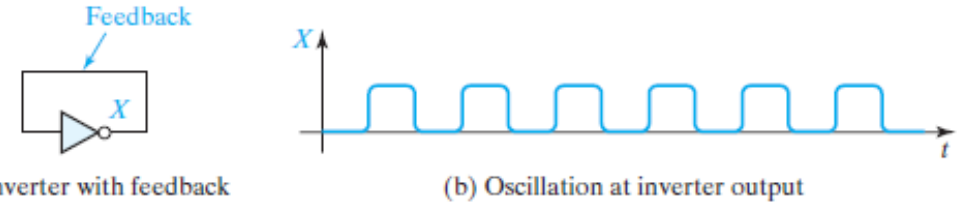
# Introduction

## Feedback:

- By feedback we mean that the output of one of the gates is connected back into the input of another gate in the circuit so as to form a closed loop.

FIGURE 11-1






(a) Inverter with feedback (b) Oscillation at inverter output

FIGURE 11-2




(a) (b)

# Set-Release Latch

**S-R Latch Explanation:**

- We can construct a simple latch by introducing feedback into a NOR-gate circuit, as seen in Figure 11-3(a).
- As indicated, if the inputs are $S=R=0$, the circuit can assume a stable state with $Q=0$ and $P=1$.
- Now if we change $S$ to 1, $P$ will become 0. This is an unstable condition or state of the circuit because both the inputs and output of the second gate are 0; therefore $Q$ will change to 1, leading to the stable state shown in Figure 11-3(b).

# Set-Release Latch

**S-R Latch Explanation (continued):**

- If *S* is changed back to 0, the circuit will not change state because *Q*=1 feeds back into the first gate, causing *P* to remain 0, as shown in Figure 11-4(a).
- Note that the inputs are again *S*=*R*=0, but the outputs are different than those with which we started. Thus, the circuit has two different stable states for a given set of inputs.
- If we now change *R* to 1, *Q* will become 0 and *P* will then change back to 1, as seen in Figure 11-4(b). If we then change *R* back to 0, the circuit remains in this state and we are back where we started.

# Set-Release Latch

**FIGURE 11-3**



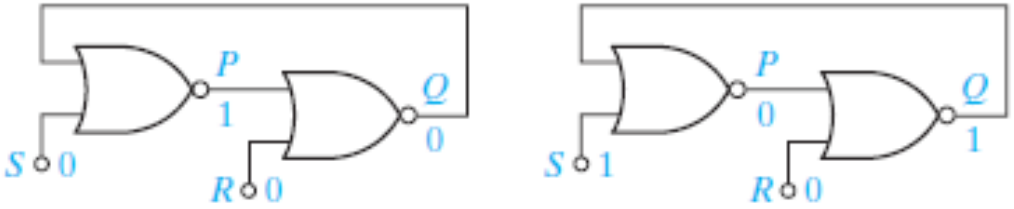
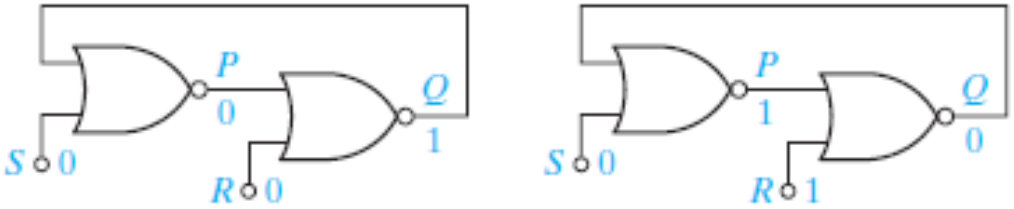



**FIGURE 11-4**





# Set-Release Latch

## Cross-Coupled Form of S-R Latch and S-R Latch Timing Diagram:

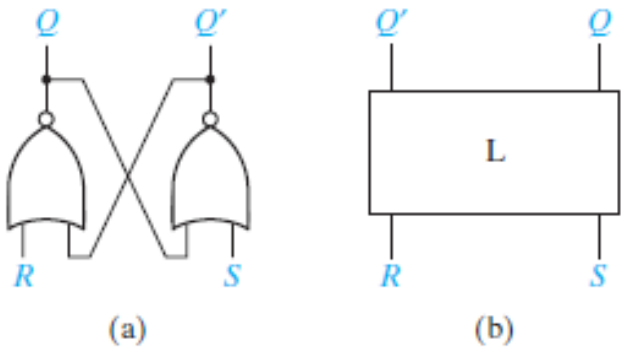



**FIGURE 11-5**
S-R Latch



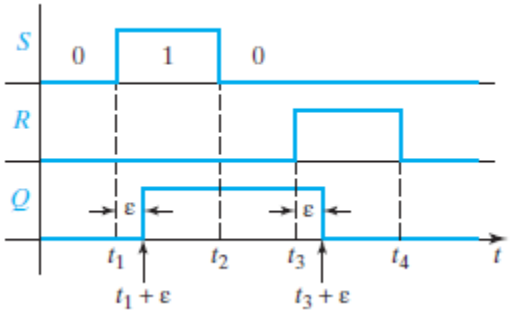



**FIGURE 11-7**
Timing Diagram for S-R Latch

# Set-Release Latch

**Present and Next States:**

- The term **present state** (Q(t)) is used to denote the state of the *Q* output of the latch or flip-flop at the time any input signal changes.
- The term **next state** (Q(t+ε)) to denote the state of the *Q* output after the latch or flip-flop has reacted to the input change and stabilized.

TABLE 11-1
S-R Latch Next State and Output



| Present State | Next State $Q^+$ | | | | Present Output *P* | | | |
|---|---|---|---|---|---|---|---|---|
| | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* |
| *Q* | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 0 | ⓪ | ⓪ | ⓪ | 1 | 1 | 1 | 0 | 0 |
| 1 | ① | 0 | 0 | ① | 0 | 0 | 0 | 0 |

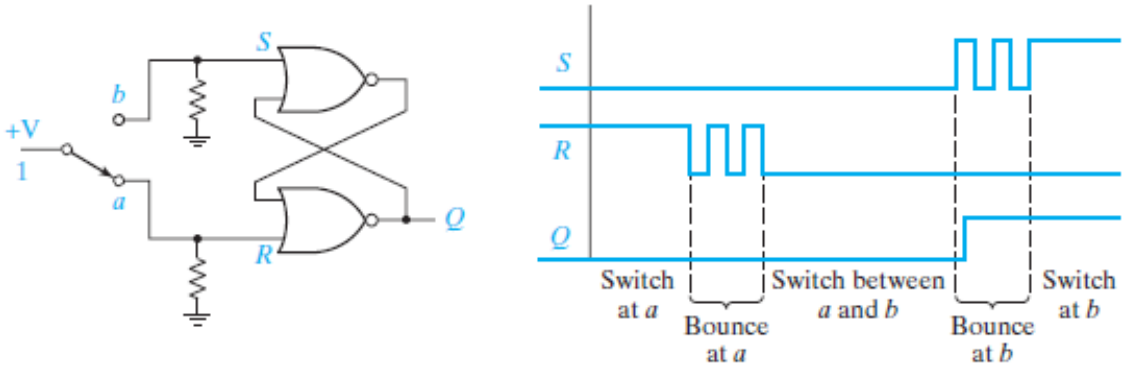
# Set-Release Latch

**Switch Debouncing:**

A useful application of the S-R Latch involves **switch debouncing**- switch contacts tend to vibrate or bounce open and closed several times before settling down to their final position, producing a noisy transition, and this noise can interfere with the proper operation of a logic circuit.

FIGURE 11-9
Switch Debouncing with an S-R Latch



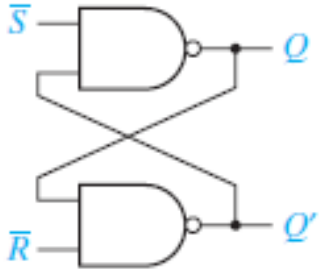


# Set-Release Latch

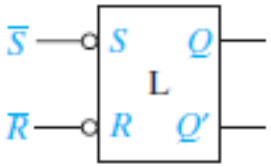
## S-R Latch using NAND Gates:

FIGURE 11-10
$\overline{S}$-$\overline{R}$ Latch






(a)




(b)

| $\overline{S}$ | $\overline{R}$ | $Q$ | $Q^+$ | |
|---|---|---|---|---|
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 1 | |
| 0 | 0 | 0 | – | Inputs not allowed |
| 0 | 0 | 1 | – | |

(c)

# Gated Latches

**Gated Latches:**

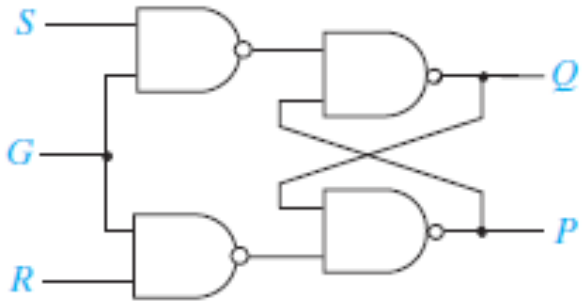
- Gated latches have an additional input called the gate or enable input.
- When the gate input is inactive, which may be the high or low value, the state of the latch cannot change.
- When the gate input is active, the latch is controlled by the other inputs and operates as indicated in the preceding section.

# Gated Latches

## Gated S-R Latch:

FIGURE 11-11
NAND-Gate Gated S-R Latch






The next-state equation is

$$Q^+ = SG + Q(R' + G')$$

and the equation for the $P$ output is

$$P = Q' + RG$$

# Gated Latches

## Gated S-R Latch:

**TABLE 11-2**
Next-State and Output of Gated S-R Latch



Next State $Q^+$

| Present State | $G = 0$ | | | | $G = 1$ | | | |
|---|---|---|---|---|---|---|---|---|
| | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* |
| *Q* | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 0 | (0) | (0) | (0) | (0) | (0) | (0) | 1 | 1 |
| 1 | (1) | (1) | (1) | (1) | (1) | 0 | (1) | (1) |

Present Output P

| Present State | $G = 0$ | | | | $G = 1$ | | | |
|---|---|---|---|---|---|---|---|---|
| | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* |
| *Q* | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

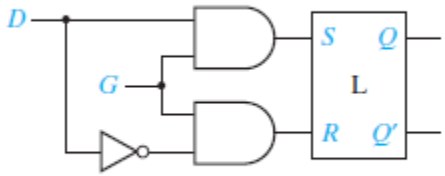
# Gated Latches

## Gated D- Latch:

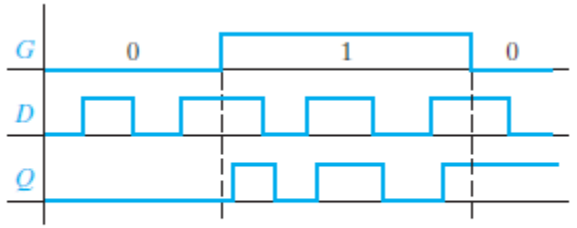
This latch is also referred to as a **transparent latch** since *Q* becomes equal to *D* while *G* is active.

FIGURE 11-14
Gated D Latch





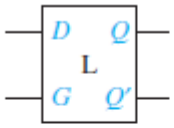

(a)



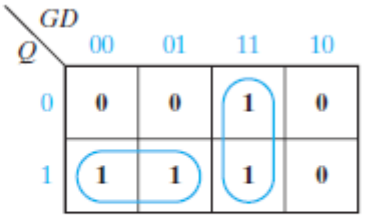

(b)

FIGURE 11-15
Symbol and Truth Table for Gated Latch






| G | D | Q | $Q^+$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |




$Q^+ = G'Q + GD$

# Gated Latches

**Edge-Triggered and Master-Slave Flip-Flops:**

- If the inputs to the flip-flop only need to be stable for a short period of time around the clock edge, then we refer to the flip-flop as **edge-triggered**.
- The term **master-slave** flip-flop refers to a particular implementation that uses two gated latches in such a way that the flip-flop outputs only change on a clock edge.

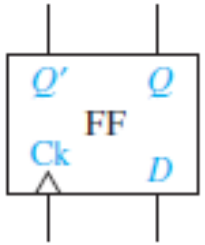
# Edge-Triggered D Flip-Flop

- A D flip-flop (Figure 11-17) has two inputs, *D* (data) and Ck (clock). The small arrowhead on the flip-flop symbol identifies the clock input.
- If the output can change in response to a 0 to 1 transition on the clock input, we say that the flip-flop is triggered on the **rising edge** (or positive edge) of the clock.
- If the output can change in response to a 1 to 0 transition on the clock input, we say that the flip-flop is triggered on the **falling edge** (or negative edge) of the clock.

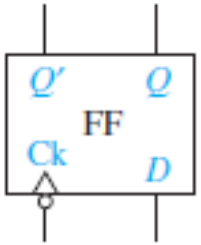
# Edge-Triggered D Flip-Flop

**FIGURE 11-17**
D Flip-Flops






(a) Rising-edge trigger




(b) Falling-edge trigger

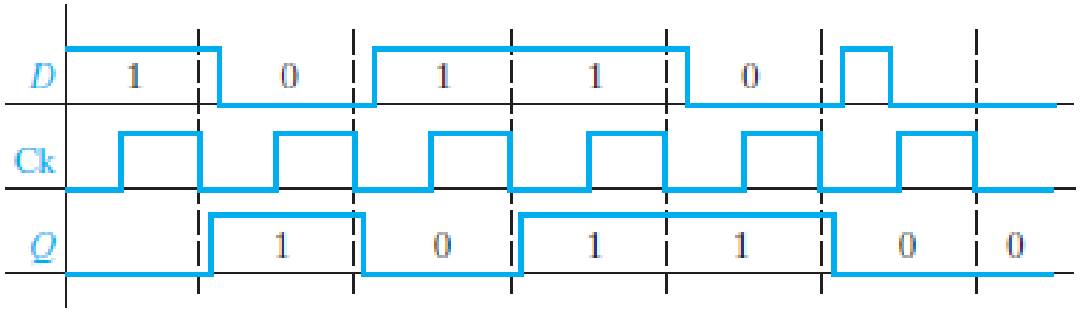
| D Q | $Q^+$ |
|---|---|
| 0 0 | 0 |
| 0 1 | 0 |
| 1 0 | 1 |
| 1 1 | 1 |

(c) Truth table

$Q^+ = D$

**FIGURE 11-18**
Timing for D Flip-Flop (Falling-Edge Trigger)



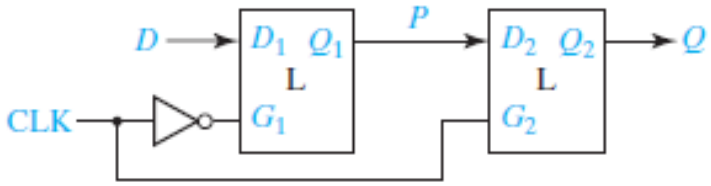


# Edge-Triggered D Flip-Flop

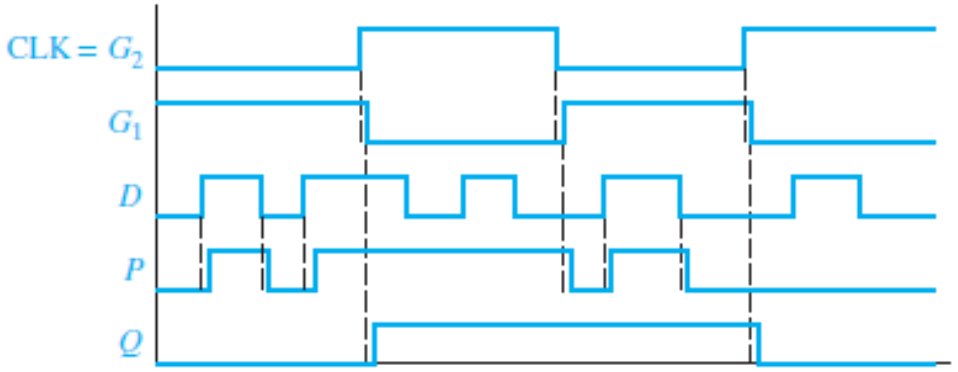
## D Flip-Flop (Rising-Edge Trigger):

FIGURE 11-19
D Flip-Flop (Rising-Edge Trigger)






(a) Construction from two gated D latches

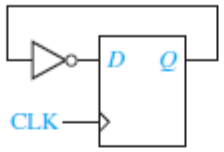



(b) Timing analysis

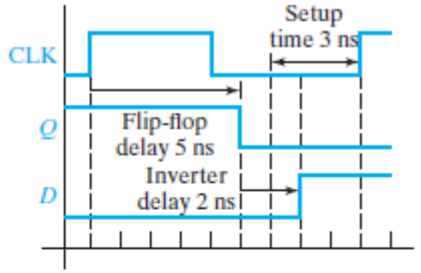
# Edge-Triggered D Flip-Flop

**FIGURE 11-21**
Determination of Minimum Clock Period

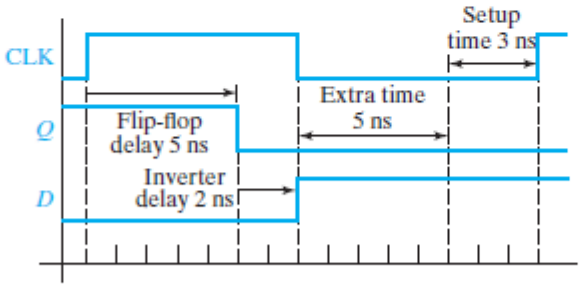




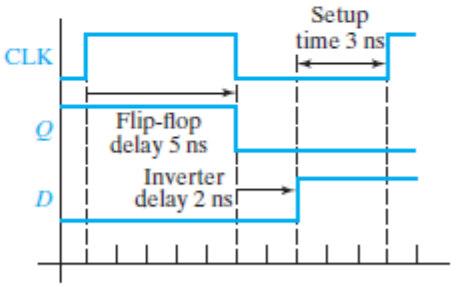

(a) Simple flip-flop circuit




(b) Setup time not satisfied




(c) Setup time satisfied

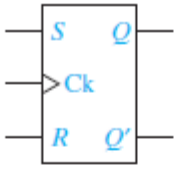



(d) Minimum clock period

# S-R Flip-Flop

**FIGURE 11-22**
**S-R Flip-Flop**



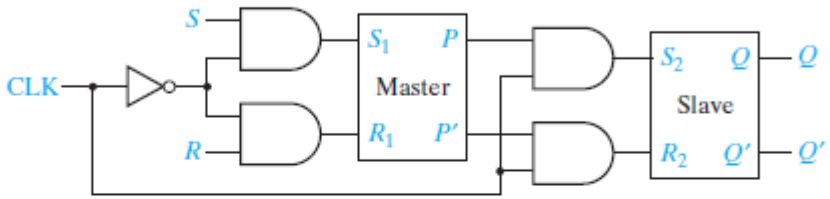



Operation summary:

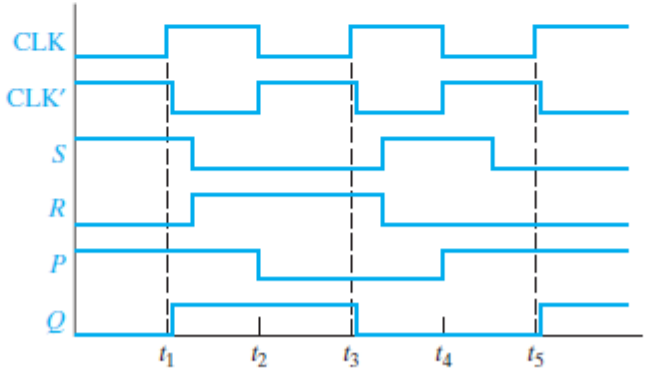
| | |
|---|---|
| $S = R = 0$ | No state change |
| $S = 1, R = 0$ | Set $Q$ to 1 (after active Ck edge) |
| $S = 0, R = 1$ | Reset $Q$ to 0 (after active Ck edge) |
| $S = R = 1$ | Not allowed |

**FIGURE 11-23**
**S-R Flip-Flop Implementation and Timing**






(a) Implementation with two latches

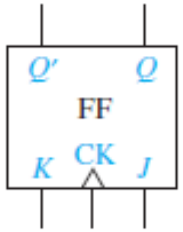



(b) Timing analysis

# J-K Flip-Flop

**FIGURE 11-24**
J-K Flip-Flop
(*Q* Changes on the Rising Edge)



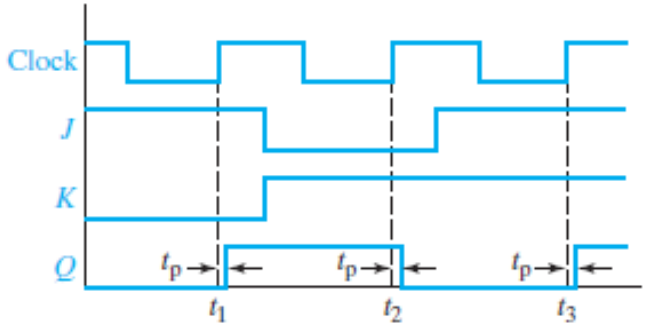



(a) J-K flip-flop

| J K Q | $Q^+$ |
|---|---|
| 0 0 0 | 0 |
| 0 0 1 | 1 |
| 0 1 0 | 0 |
| 0 1 1 | 0 |
| 1 0 0 | 1 |
| 1 0 1 | 1 |
| 1 1 0 | 1 |
| 1 1 1 | 0 |

$$Q^+ = JQ' + K'Q$$

(b) Truth table and characteristic equation

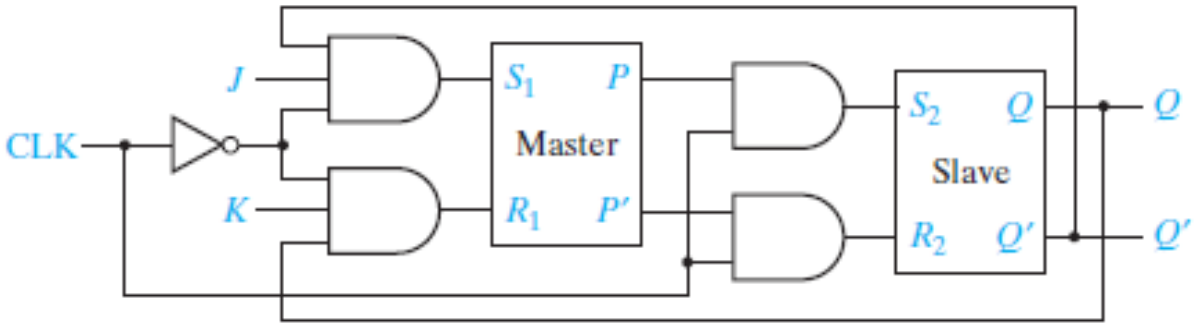



(c) J-K flip-flop timing

# J-K Flip-Flop

**FIGURE 11-25**
Master-Slave J-K Flip-Flop (*Q* Changes on Rising Edge)

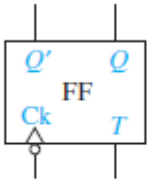




# J-K Flip-Flop

FIGURE 11-26
T Flip-Flop






(a)

| T Q | $Q^+$ |
|---|---|
| 0 0 | 0 |
| 0 1 | 1 |
| 1 0 | 1 |
| 1 1 | 0 |

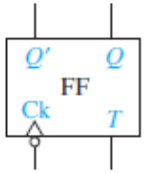
(b)

$$Q^+ = T'Q + TQ' = T \oplus Q$$

# T Flip-Flop

**FIGURE 11-26**
T Flip-Flop






(a)

| T Q | $Q^+$ |
|---|---|
| 0 0 | 0 |
| 0 1 | 1 |
| 1 0 | 1 |
| 1 1 | 0 |

(b)

$$Q^+ = T'Q + TQ' = T \oplus Q$$

**FIGURE 11-27**
Timing Diagram for T Flip-Flop (Falling-Edge Trigger)



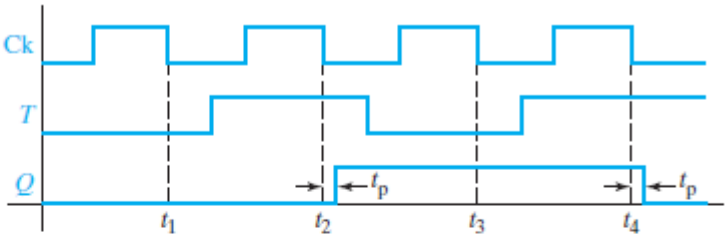
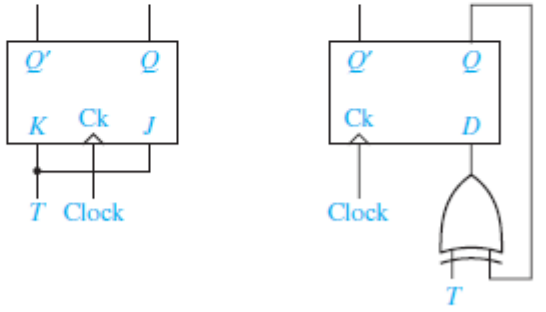



**FIGURE 11-28**
Implementation of T Flip-Flops






(a) Conversion of J-K to $T$ (b) Conversion of $D$ to $T$

Characteristic Equation For T Flip-Flop:

$$Q^+ = JQ' + K'Q = TQ' + T'Q$$

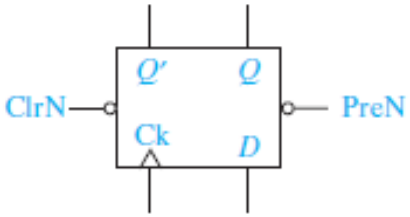
# Flip-Flops with Additional Inputs

**Flip-Flops with Additional Inputs:**

- Flip-flops often have additional inputs which can be used to set the flip-flops to an initial state independent of the clock.

FIGURE 11-29
D Flip-Flop with Clear and Preset






(a)

| Ck | D | PreN | ClrN | $Q^+$ |
|---|---|---|---|---|
| x | x | 0 | 0 | (not allowed) |
| x | x | 0 | 1 | 1 |
| x | x | 1 | 0 | 0 |
| ↑ | 0 | 1 | 1 | 0 |
| ↑ | 1 | 1 | 1 | 1 |
| 0,1,↓ | x | 1 | 1 | $Q$ (no change) |

(b)

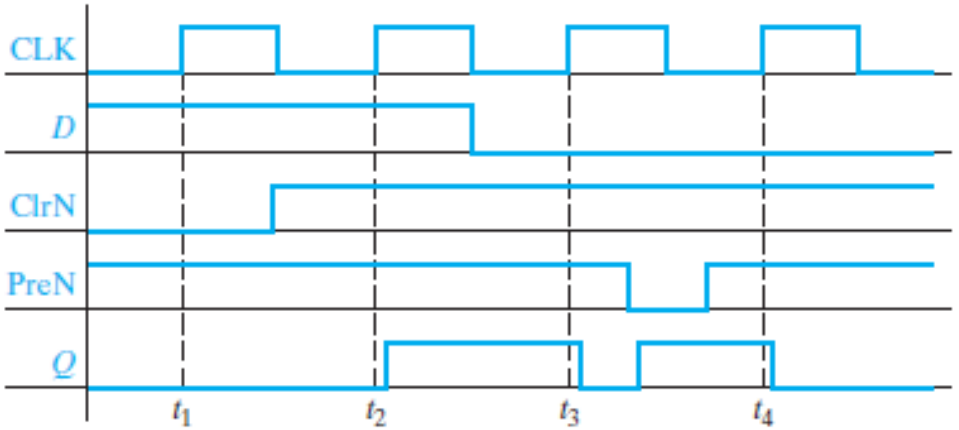
# Flip-Flops with Additional Inputs

**Asynchronous Clear and Preset:**

- ClrN and PreN are often referred to as **asynchronous** clear and preset inputs because their operation does not depend on the clock.

FIGURE 11-30
Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset



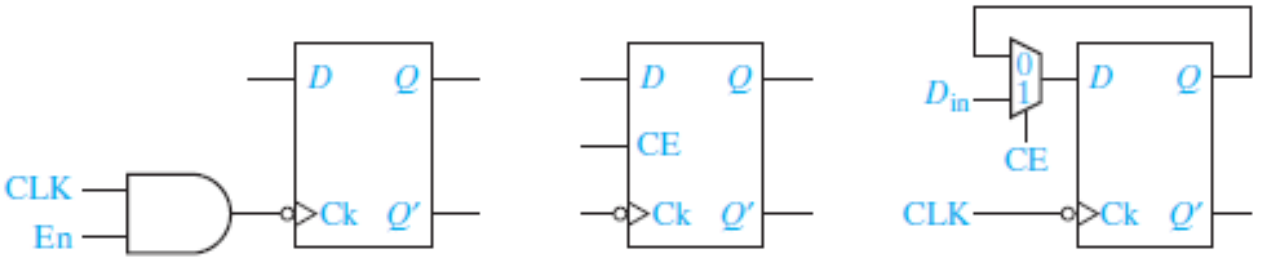


# Flip-Flops with Additional Inputs

## D Flip-Flop with Clock Enable:

FIGURE 11-31
D Flip-Flop with Clock Enable






(a) Gating the clock (b) D-CE symbol (c) Implementation

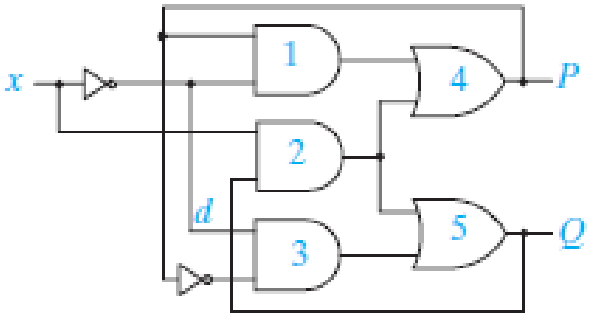
# Asynchronous Sequential Circuits

## Asynchronous Sequential Circuits:

- In **asynchronous** sequential circuits the state of the circuit can change whenever any input changes.

FIGURE 11-32
Asynchronous Circuit






(a)

| PQ \ x | 0 | 1 |
|---|---|---|
| 00 | 01 | (00) |
| 01 | (01) | 11 |
| 11 | 10 | (11) |
| 10 | (10) | 00 |

(b)

# Asynchronous Sequential Circuits

**Hazards and Incorrect State Transitions:**

- Even if the circuit is free of hazards, delays in the "wrong" places in the circuit can cause incorrect state transitions.
- Essential hazards are properties of the next-state table; they cannot be eliminated by modifying the circuit's logic.

# Asynchronous Sequential Circuits

## Multiple Input Change and Multiple-State Variable Change Examples:

FIGURE 11-33
Multiple Input Change Example



| PQ \ xy | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | (00) | (00) | 01 | (00) |
| 01 | 11 | 00 | (01) | 11 |
| 11 | (11) | 10 | (11) | (11) |
| 10 | 00 | (10) | 11 | 00 |

FIGURE 11-34
Multiple-State Variable Change Example



| PQR \ x | 0 | 1 |
|---|---|---|
| 000 | (000) | 011 |
| 001 | 101 | (001) |
| 011 | 101 | (011) |
| 010 | 000 | 011 |
| 110 | 000 | (110) |
| 111 | 101 | (111) |
| 101 | (101) | 110 |
| 100 | (100) | 110 |

# Summary

**Procedure to find Characteristic Equation:**

1. Make a truth table that gives the next state ($Q+$) as a function of the present state ($Q$) and the inputs. Any illegal input combinations should be treated as don't-cares.

2. Plot a map for $Q+$ and read the characteristic equation from the map.

# Summary

**Characteristic Equations for Various Flip-Flops / Latches:**

$Q^+ = S + R'Q \ (SR = 0)$ (S-R latch or flip-flop) (11-6)

$Q^+ = GD + G'Q$ (gated D latch) (11-7)

$Q^+ = D \cdot CE + Q \cdot CE'$ (D-CE flip-flop) (11-9)

$Q^+ = JQ' + K'Q$ (J-K flip-flop) (11-10)

$Q^+ = T \oplus Q = TQ' + T'Q$ (T flip-flop) (11-11)