pr5 Simulator - Part 4 (Optimizations)

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Deadline: 27-Nov 2024, 23:59 hrs

Lab Assignment 6 (Graded)

In this lab, you are required to implement branch prediction to the 5-stage pipelined RISC-V processor developed so far. The detailed specification that your implementation should (mandatory) adhere to is given below:

- Implement a Branch Target Buffer (BTB) that maintains the target address (or target PC) for each branch instruction that is encountered so far. The BTB entry should be updated only if the branch is taken. If a branch is predicted as not taken, the BTB need not have an entry for it. Assume the BTB can hold only 16 entries (and not more).
- You should implement at least three different branch predictor designs:
  1. **BP1:** Statically predict branches as taken
  2. **BP2:** A dynamic branch predictor that maintains just one (global) saturating counter (across all branches)
  3. **BP3:** A dynamic branch predictor that maintains a saturating counter per branch. The number of counters should be the same as the number of entries in the BTB.
- Take an additional command-line argument with the option identifier `--bp` as input, which specifies the branch predictor to be used for the current simulation. For example, the commands below uses the simulator `BP1` when simulating `1-even.r5o`.

```
$ python3 src/main.py --bp BP1 programs/bins/1-even.r5o
```