Arm® Mali™ - IV009 implementation Base Enablement Package User Guide

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Change history

Revision	Date	Change
r0p0-00lac0	December 2017	Initial release
r0p0-00eac0	March 2018	Directory structure and the addition of reference to the Register_Cloning_Avoidance.pdf
r0p0-00rel0	September 2018	Revision ID updated

Contents

1 INTRODUCTION

1.1 Overview

This document describes the contents of the implementation Base Enablement Package (iBEP) and example floorplans for the Mali-IV009 ISP

1.2 EDA Vendor Support

1.2.1 Cadence

For those implementing this IP using a Cadence-based flow, please check with your Cadence support team about Cadence rapid adoption kits (RAKs) for Arm-based IP. These comprise tuned scripts and digital flows, developed to reach particular power, performance, and area (PPA) design goals. More information about RAKs is available at https://www.cadence.com/go/arm-rak . If there is no specific Cadence RAK for this IP, your local Cadence AE team will be able to help you.

1.2.2 Synopsys

When implementing this IP using Synopsys tools, we suggest you download an appropriate set of tool scripts from Synopsys at https://www.synopsys.com/Arm. If Synopsys offers a QuickStart Implementation Kit (QIK) for this IP, then you may use that directly; if not, then we suggest you download a similar QIK and also the Synopsys tool Recommended Methodology (RM) scripts from SolvNet at https://solvnet.synopsys.com/rmgen. Use the downloaded QIK and RM scripts together as a starting point.

1.3 Directory Structure

The directory structure used by the implementation Base Enablement Package is shown below.

```
mali_iv009
       |-- logical
       |   `-- models
       |       |-- tsmc_cln16fpll001_clkgate                    (sample ICG integration RTL files)
       |       `-- tsmc_cln16fpll001_modules                    (sample RAM integration RTL files)
       `-- iBEP
           |-- constraints                                      (timing constraints and RTL filelist)
           |-- Register_Cloning_Avoidance.pdf
           '-- Arm_Mali-IV009_r0p0_00rel0_iBEP_user_guide.pdf   (this document)
```

2 FILES

2.1 Timing Constraints

The supplied timing constraints are SDC constraints for the design implemented separately, not including technology specific constraints or clock latencies constraints:

- clocks.sdc
- exceptions.sdc
- io.sdc

The user is entitled to review the constraints and revisit the files by adding specific constraints that match the implementation strategy and sign-off criteria.

2.2 DFT signals

The timing constraints for the DFT signals can be modified to suit your own implementation.

The Mali-IV009 ISP comes with a scantest_enable for control of the scan enable of the registers and clock gates.

2.3 Sample technology specific RTL files

Sample technology specific RTL files have been provided and can be used as a reference for your own implementation.

Please refer to section 7 of the Configuration and Integration Manual for inserting technology specific clock gate cell.

2.4 RTL filelist

The supplied RTL filelist contains lists of the VHDL and Verilog files and their locations that are required to build the Mali-IV009 ISP. Both Cadence encrypted and Synopsys encrypted RTL filelists are supplied.

The filelists include references to the sample technology specific RTL files. You will need to modify this for your own implementation.

Refer to section 4.5 of the Configuration and Integration Manual for the RTL file list.

3 GUIDANCE

3.1 Register Cloning

Automatic cloning, replication or duplication of non-reset registers is potentially dangerous and you are strongly advised to ensure that this feature is explicitly disabled in your physical implementation flows.

The following switches can be used in your synthesis tool:

Cadence:

```
set_attr iopt_sequential_duplication false /
```

Synopsys:

```
set_app_var compile_register_replication false
set compile_register_replication_across_hierarchy false
```

Please refer to the Arm document – “Register Cloning Avoidance” – for more details.

3.2 VCKE port considerations

When placing the vcke port, consideration should be taken for the register driving this port.

The register should be placed as close to the Mali-IV009 ISP vcke port as possible to help with timing inside the Mali-IV009 ISP.

3.3 Gray code considerations

Considerations for the gray code registers should be made during CTS for their clock domain crossing with regards to meta stability.
The transfer of data between Q-D of the registers will need to be within 1 clock cycle of the fasted clock, minus the max skew across the source registers plus the max skew across the destination registers.
The skew for each source and destination pair should be kept to a minimum across the bus.

For Example: Max Delay = Fastest clock period - (Source register max skew + Destination registers max skew)

The source and destination registers for each pair should be placed close together with no buffering between the source registers Q pin and destination registers D pin.

This guidance should be applied across each instance of gray code register pairing.
The pairings of which can be found in the table below.

Details	Src/Dest	Register Name Pairs	Clock
DMA Writer			
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	VCLK

Details	Src/Dest	Register Name Pairs	Clock
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	ACLK
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	VCLK
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	ACLK
	Source	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	VCLK
	Destination	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	ACLK
	Source	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	VCLK
	Destination	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	ACLK
	Source	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	VCLK
	Destination	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	ACLK
	Source	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	VCLK
	Destination	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	ACLK
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	ACLK
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	VCLK
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	ACLK
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	VCLK
	Source	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	ACLK

Details	Src/Dest	Register Name Pairs	Clock
	Destination	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	VCLK
	Source	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	ACLK
	Destination	mali_iv009_isp_core_nomem_i/gen_ds_pile_en.inst_ds_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	VCLK
	Source	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	ACLK
	Destination	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	VCLK
	Source	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	ACLK
	Destination	mali_iv009_isp_core_nomem_i/inst_fr_isp_output_cluster/inst_uv_dma_writer/inst_dma_writer/inst_writer/wrfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	VCLK
DMA reader			
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	ACLK
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	VCLK
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/wfifo_wr_addr_gray_del_reg[*]/Q	ACLK
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/rfifo_wr_addr_gray_r1_reg[*]/D	VCLK
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	VCLK
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_lsb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	ACLK
	Source	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/rfifo_rd_addr_gray_del_reg[*]/Q	VCLK
	Destination	mali_iv009_isp_core_nomem_i/inst_isp_nr_cluster/inst_temper_dma_msb_reader/inst_dma_reader/inst_reader/rdfifo/apical_fifo/wfifo_rd_addr_gray_r1_reg[*]/D	ACLK

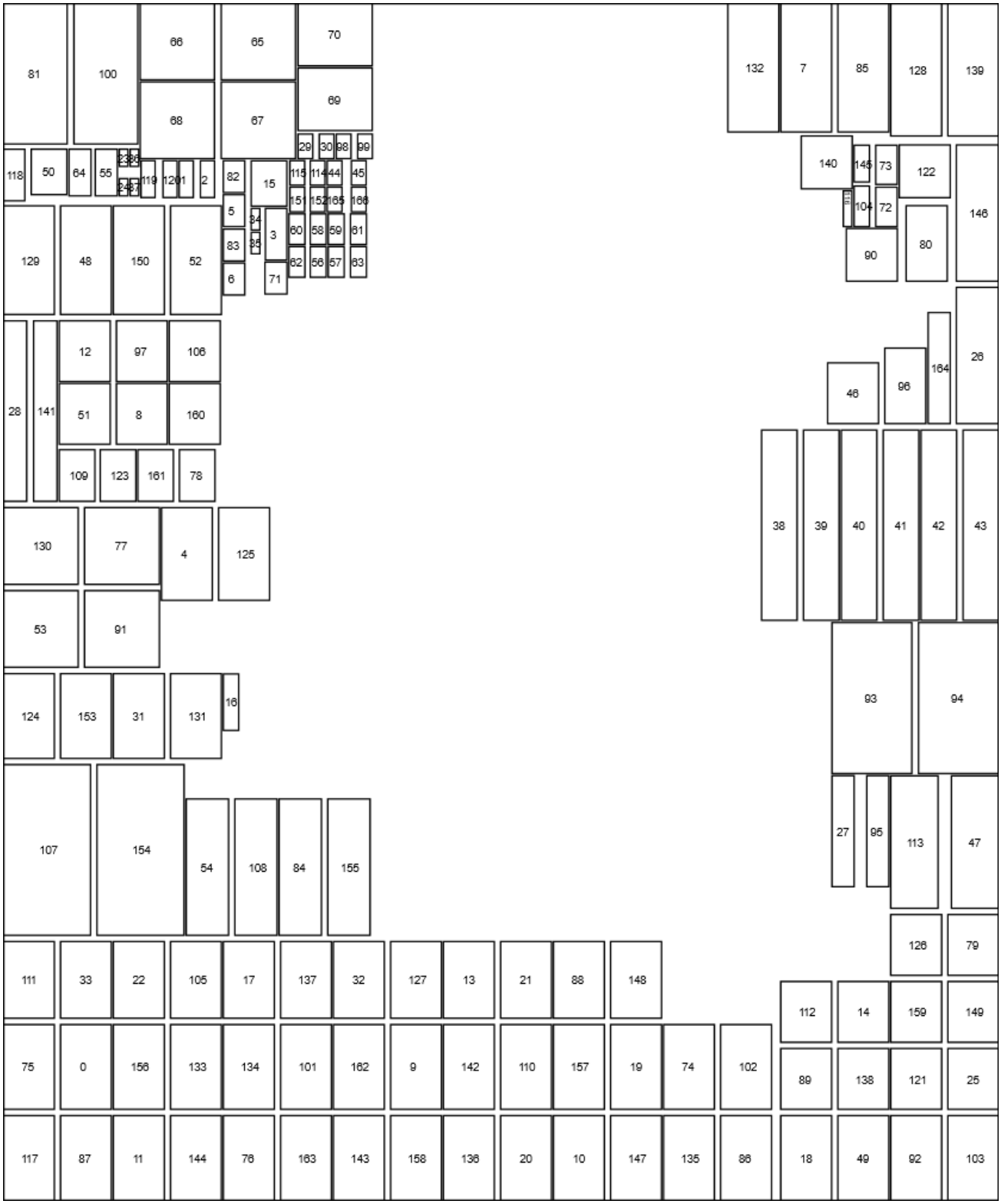
3.4 Example floorplans

The floorplan is strongly influenced by the macro placement due to the large amount of memories in the design.

You must take care in the placement of the memories, because they occupy a large area of the floorplan and because they require significant routing resources. The placement of the memories also affects the optimum standard cell placement.

- Consider creating large memories from banks of smaller memory.
- Use register file memories where applicable.
- Consider using a keepout margin for the memories to avoid routing congestions.
- Consider channels between large banks of memories to avoid timing and max transition violations.
- Use the flylines feature if it is available in the floorplanning tool.
- The aspect ratios shown for memories in the featured diagrams are arbitrary. They might not be achievable using your memory compiler.
- It might be necessary to adjust the floorplan if your technology prevents you from routing over the memory blocks.

3.4.1 ISP Default Floorplan



The following table shows a key for the ISP Default floorplan example.

Number	Full name
0	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_16
1	mem_top_i/inst_mem_decompander1_pong_mem
2	mem_top_i/inst_mem_decompander1_pong_mem2
3	mem_top_i/inst_mem_ihist_stats_mem2
4	mem_top_i/inst_mem_iridix_delay_line_data_mem_1
5	mem_top_i/inst_mem_radial_shading_pong_mem
6	mem_top_i/inst_mem_radial_shading_pong_mem2
7	mem_top_i/inst_mem_uv_mean_rfilter_mem
8	mem_top_i/inst_mem_frame_stitch_dly2_mem_1
9	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_05
10	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_21
11	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_29
12	mem_top_i/inst_mem_frame_stitch_dly1_mem_0
13	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_05
14	mem_top_i/inst_mem_demosaic_dly_mem_1
15	mem_top_i/inst_mem_ihist_stats_mem
16	mem_top_i/inst_mem_af_scratch_mem
17	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_03
18	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_15
19	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_09
20	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_22
21	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_04
22	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_09
23	mem_top_i/inst_mem_decompander0_ping_mem
24	mem_top_i/inst_mem_decompander0_ping_mem2
25	mem_top_i/inst_mem_demosaic_dly_mem_7
26	mem_top_i/inst_mem_ds_dma_writer_wfifo_mem
27	mem_top_i/inst_mem_ds_sharpen_dly2_mem_1
28	mem_top_i/inst_mem_frame_stitch_lc2_mem
29	mem_top_i/inst_mem_iridix_fp2_pong_mem
30	mem_top_i/inst_mem_iridix_fp2_pong_mem2
31	mem_top_i/inst_mem_rfe_dly_mem_0
32	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_07
33	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_10
34	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_filter_ping_mem
35	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_filter_pong_mem
36	mem_top_i/inst_mem_decompander0_pong_mem

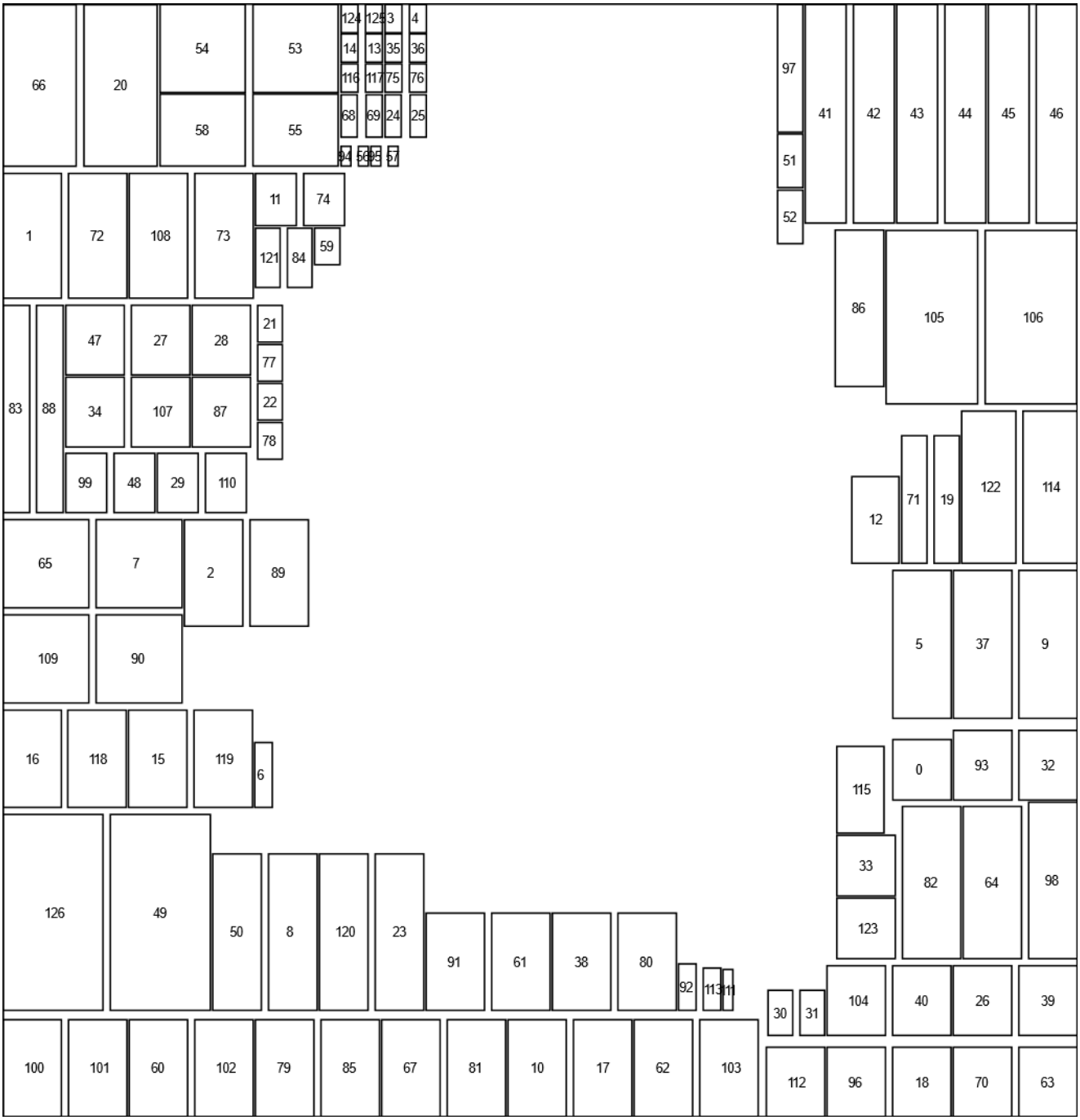
Number	Full name
37	mem_top_i/inst_mem_decompander0_pong_mem2
38	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_0
39	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_1
40	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_2
41	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_3
42	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_4
43	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_5
44	mem_top_i/inst_mem_iridix_fp2_ping_mem
45	mem_top_i/inst_mem_iridix_fp2_ping_mem2
46	mem_top_i/inst_mem_mirror_mem
47	mem_top_i/inst_mem_ds_sharpen_dly1_mem_1
48	mem_top_i/inst_mem_frame_stitch_dly3_mem_1
49	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_11
50	mem_top_i/inst_mem_aexp_hist_stats_mem
51	mem_top_i/inst_mem_frame_stitch_dly2_mem_0
52	mem_top_i/inst_mem_frame_stitch_dly3_mem_3
53	mem_top_i/inst_mem_iridix_mem2_3
54	mem_top_i/inst_mem_temper_fb_msb_wfifo_mem
55	mem_top_i/inst_mem_ds_scaler_hfilt_coefmem
56	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_0
57	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_1
58	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_2
59	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_3
60	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_4
61	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_5
62	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_6
63	mem_top_i/sinter3_rams_lut.inst_mem_lut3d_mem_7
64	mem_top_i/inst_mem_ds_scaler_vfilt_coefmem
65	mem_top_i/inst_mem_mesh_shading_pong_mem
66	mem_top_i/inst_mem_mesh_shading_ping_mem
67	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_mesh_pong_mem
68	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_mesh_ping_mem
69	mem_top_i/inst_mem_dpc_pong_mem
70	mem_top_i/inst_mem_dpc_ping_mem
71	mem_top_i/inst_mem_cmd_queues
72	mem_top_i/inst_mem_lumvar_stats_pong_mem
73	mem_top_i/inst_mem_lumvar_stats_ping_mem
74	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_10
75	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_17

Number	Full name
76	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_27
77	mem_top_i/inst_mem_iridix_mem2_0
78	mem_top_i/inst_mem_iridix_mem_0
79	mem_top_i/inst_mem_af_delay_line_mem_0
80	mem_top_i/inst_mem_fr_uv_dma_writer_wfifo_mem
81	mem_top_i/inst_mem_metering_stats_pong_mem
82	mem_top_i/inst_mem_radial_shading_ping_mem
83	mem_top_i/inst_mem_radial_shading_ping_mem2
84	mem_top_i/inst_mem_temper_fb_lsb_rfifo_mem
85	mem_top_i/inst_mem_uv_var_rfilter_mem
86	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_18
87	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_30
88	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_01
89	mem_top_i/inst_mem_demosaic_dly_mem_4
90	mem_top_i/inst_mem_fr_sharpen_dly2_mem_1
91	mem_top_i/inst_mem_iridix_mem2_2
92	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_12
93	mem_top_i/inst_mem_ds_scaler_lb_fifo_mem1_0
94	mem_top_i/inst_mem_ds_scaler_lb_fifo_mem1_1
95	mem_top_i/inst_mem_ds_sharpen_dly2_mem_0
96	mem_top_i/inst_mem_ds_uv_dma_writer_wfifo_mem
97	mem_top_i/inst_mem_frame_stitch_dly1_mem_1
98	mem_top_i/inst_mem_iridix_rp_ping_mem
99	mem_top_i/inst_mem_iridix_rp_ping_mem2
100	mem_top_i/inst_mem_metering_stats_ping_mem
101	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_03
102	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_13
103	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_14
104	mem_top_i/inst_mem_aexp_scratch_mem
105	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_08
106	mem_top_i/inst_mem_frame_stitch_dly1_mem_2
107	mem_top_i/inst_mem_temper_delay_line_mem_1
108	mem_top_i/inst_mem_temper_fb_msb_rfifo_mem
109	mem_top_i/inst_mem_iridix_mem_3
110	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_07
111	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_11
112	mem_top_i/inst_mem_demosaic_dly_mem_0
113	mem_top_i/inst_mem_ds_sharpen_dly1_mem_0
114	mem_top_i/inst_mem_iridix_fp1_pong_mem

Number	Full name
115	mem_top_i/inst_mem_iridix_fp1_pong_mem2
116	mem_top_i/inst_mem_lumvar_scratch_mem
117	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_31
118	mem_top_i/inst_mem_aexp_hist_stats_mem2
119	mem_top_i/inst_mem_decompander1_ping_mem
120	mem_top_i/inst_mem_decompander1_ping_mem2
121	mem_top_i/inst_mem_demosaic_dly_mem_6
122	mem_top_i/inst_mem_fr_cs_conv_dly_mem
123	mem_top_i/inst_mem_iridix_mem_1
124	mem_top_i/inst_mem_rfe_dly_mem_1
125	mem_top_i/inst_mem_iridix_delay_line_data_mem_0
126	mem_top_i/inst_mem_af_delay_line_mem_1
127	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_06
128	mem_top_i/inst_mem_fr_sharpen_dly1_mem_0
129	mem_top_i/inst_mem_frame_stitch_dly3_mem_0
130	mem_top_i/inst_mem_iridix_mem2_1
131	mem_top_i/inst_mem_rfe_dly_mem_3
132	mem_top_i/inst_mem_seg_mean_rfilter_mem
133	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_01
134	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_02
135	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_19
136	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_23
137	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_02
138	mem_top_i/inst_mem_demosaic_dly_mem_5
139	mem_top_i/inst_mem_fr_sharpen_dly1_mem_1
140	mem_top_i/inst_mem_fr_sharpen_dly2_mem_0
141	mem_top_i/inst_mem_frame_stitch_lc1_mem
142	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_06
143	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_25
144	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_28
145	mem_top_i/inst_mem_awb_scratch_mem
146	mem_top_i/inst_mem_fr_dma_writer_wfifo_mem
147	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_20
148	mem_top_i/sinter3_rams_cac.inst_mem_ca_correction_delay_line_mem_00
149	mem_top_i/inst_mem_demosaic_dly_mem_3
150	mem_top_i/inst_mem_frame_stitch_dly3_mem_2
151	mem_top_i/inst_mem_iridix_fp1_ping_mem
152	mem_top_i/inst_mem_iridix_fp1_ping_mem2
153	mem_top_i/inst_mem_rfe_dly_mem_2

Number	Full name
154	mem_top_i/inst_mem_temper_delay_line_mem_0
155	mem_top_i/inst_mem_temper_fb_lsb_wfifo_mem
156	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_00
157	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_08
158	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_24
159	mem_top_i/inst_mem_demosaic_dly_mem_2
160	mem_top_i/inst_mem_frame_stitch_dly2_mem_2
161	mem_top_i/inst_mem_iridix_mem_2
162	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_04
163	mem_top_i/sinter3_rams.inst_mem_sinter3_delay_line_mem_26
164	mem_top_i/inst_mem_ds_cs_conv_dly_mem
165	mem_top_i/inst_mem_iridix_rp_pong_mem
166	mem_top_i/inst_mem_iridix_rp_pong_mem2

3.4.2 ISP LITE floorplan



The following table shows a key for the ISP LITE floorplan example.

Number	Full name
0	mem_top_i/inst_mem_fr_cs_conv_dly_mem
1	mem_top_i/inst_mem_frame_stitch_dly3_mem_0
2	mem_top_i/inst_mem_iridix_delay_line_data_mem_1
3	mem_top_i/inst_mem_iridix_rp_ping_mem
4	mem_top_i/inst_mem_iridix_rp_ping_mem2
5	mem_top_i/inst_mem_seg_mean_rfilter_mem
6	mem_top_i/inst_mem_af_scratch_mem
7	mem_top_i/inst_mem_iridix_mem2_0
8	mem_top_i/inst_mem_temper_fb_msb_rfifo_mem
9	mem_top_i/inst_mem_uv_var_rfilter_mem
10	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_12
11	mem_top_i/inst_mem_aexp_hist_stats_mem
12	mem_top_i/inst_mem_ds_uv_dma_writer_wfifo_mem
13	mem_top_i/inst_mem_iridix_fp1_pong_mem
14	mem_top_i/inst_mem_iridix_fp1_pong_mem2
15	mem_top_i/inst_mem_rfe_dly_mem_0
16	mem_top_i/inst_mem_rfe_dly_mem_1
17	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_13
18	mem_top_i/inst_mem_demosaic_dly_mem_5
19	mem_top_i/inst_mem_ds_sharpen_dly2_mem_0
20	mem_top_i/inst_mem_metering_stats_ping_mem
21	mem_top_i/inst_mem_radial_shading_ping_mem
22	mem_top_i/inst_mem_radial_shading_ping_mem2
23	mem_top_i/inst_mem_temper_fb_lsb_wfifo_mem
24	mem_top_i/inst_mem_decompander1_pong_mem
25	mem_top_i/inst_mem_decompander1_pong_mem2
26	mem_top_i/inst_mem_demosaic_dly_mem_2
27	mem_top_i/inst_mem_frame_stitch_dly1_mem_1
28	mem_top_i/inst_mem_frame_stitch_dly1_mem_2
29	mem_top_i/inst_mem_iridix_mem_2
30	mem_top_i/inst_mem_lumvar_stats_ping_mem
31	mem_top_i/inst_mem_lumvar_stats_pong_mem
32	mem_top_i/inst_mem_af_delay_line_mem_0
33	mem_top_i/inst_mem_fr_sharpen_dly2_mem_1
34	mem_top_i/inst_mem_frame_stitch_dly2_mem_0
35	mem_top_i/inst_mem_iridix_fp2_ping_mem
36	mem_top_i/inst_mem_iridix_fp2_ping_mem2
37	mem_top_i/inst_mem_uv_mean_rfilter_mem

Number	Full name
38	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_09
39	mem_top_i/inst_mem_demosaic_dly_mem_3
40	mem_top_i/inst_mem_demosaic_dly_mem_1
41	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_0
42	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_1
43	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_2
44	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_3
45	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_4
46	mem_top_i/inst_mem_ds_scaler_vfilt_linemem1_5
47	mem_top_i/inst_mem_frame_stitch_dly1_mem_0
48	mem_top_i/inst_mem_iridix_mem_1
49	mem_top_i/inst_mem_temper_delay_line_mem_0
50	mem_top_i/inst_mem_temper_fb_msb_wfifo_mem
51	mem_top_i/inst_mem_ds_scaler_hfilt_coefmem
52	mem_top_i/inst_mem_ds_scaler_vfilt_coefmem
53	mem_top_i/inst_mem_mesh_shading_pong_mem
54	mem_top_i/inst_mem_mesh_shading_ping_mem
55	mem_top_i/inst_mem_dpc_pong_mem
56	mem_top_i/inst_mem_decompander0_pong_mem
57	mem_top_i/inst_mem_decompander0_pong_mem2
58	mem_top_i/inst_mem_dpc_ping_mem
59	mem_top_i/inst_mem_cmd_queues
60	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_02
61	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_08
62	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_15
63	mem_top_i/inst_mem_demosaic_dly_mem_7
64	mem_top_i/inst_mem_fr_sharpen_dly1_mem_1
65	mem_top_i/inst_mem_iridix_mem2_1
66	mem_top_i/inst_mem_metering_stats_pong_mem
67	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_06
68	mem_top_i/inst_mem_decompander1_ping_mem
69	mem_top_i/inst_mem_decompander1_ping_mem2
70	mem_top_i/inst_mem_demosaic_dly_mem_6
71	mem_top_i/inst_mem_ds_sharpen_dly2_mem_1
72	mem_top_i/inst_mem_frame_stitch_dly3_mem_1
73	mem_top_i/inst_mem_frame_stitch_dly3_mem_3
74	mem_top_i/inst_mem_ihist_stats_mem
75	mem_top_i/inst_mem_iridix_rp_pong_mem
76	mem_top_i/inst_mem_iridix_rp_pong_mem2

Number	Full name
77	mem_top_i/inst_mem_radial_shading_pong_mem
78	mem_top_i/inst_mem_radial_shading_pong_mem2
79	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_04
80	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_10
81	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_11
82	mem_top_i/inst_mem_fr_sharpen_dly1_mem_0
83	mem_top_i/inst_mem_frame_stitch_lc2_mem
84	mem_top_i/inst_mem_ihist_stats_mem2
85	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_05
86	mem_top_i/inst_mem_ds_dma_writer_wfifo_mem
87	mem_top_i/inst_mem_frame_stitch_dly2_mem_2
88	mem_top_i/inst_mem_frame_stitch_lc1_mem
89	mem_top_i/inst_mem_iridix_delay_line_data_mem_0
90	mem_top_i/inst_mem_iridix_mem2_2
91	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_07
92	mem_top_i/inst_mem_aexp_scratch_mem
93	mem_top_i/inst_mem_af_delay_line_mem_1
94	mem_top_i/inst_mem_decompander0_ping_mem
95	mem_top_i/inst_mem_decompander0_ping_mem2
96	mem_top_i/inst_mem_demosaic_dly_mem_4
97	mem_top_i/inst_mem_ds_cs_conv_dly_mem
98	mem_top_i/inst_mem_fr_dma_writer_wfifo_mem
99	mem_top_i/inst_mem_iridix_mem_3
100	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_00
101	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_01
102	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_03
103	mem_top_i/sinter2p5_rams.inst_mem_sinter2p5_delay_line_mem_14
104	mem_top_i/inst_mem_demosaic_dly_mem_0
105	mem_top_i/inst_mem_ds_scaler_lb_fifo_mem1_0
106	mem_top_i/inst_mem_ds_scaler_lb_fifo_mem1_1
107	mem_top_i/inst_mem_frame_stitch_dly2_mem_1
108	mem_top_i/inst_mem_frame_stitch_dly3_mem_2
109	mem_top_i/inst_mem_iridix_mem2_3
110	mem_top_i/inst_mem_iridix_mem_0
111	mem_top_i/inst_mem_lumvar_scratch_mem
112	mem_top_i/inst_mem_mirror_mem
113	mem_top_i/inst_mem_awb_scratch_mem
114	mem_top_i/inst_mem_ds_sharpen_dly1_mem_1
115	mem_top_i/inst_mem_fr_uv_dma_writer_wfifo_mem

Number	Full name
116	mem_top_i/inst_mem_iridix_fp1_ping_mem
117	mem_top_i/inst_mem_iridix_fp1_ping_mem2
118	mem_top_i/inst_mem_rfe_dly_mem_2
119	mem_top_i/inst_mem_rfe_dly_mem_3
120	mem_top_i/inst_mem_temper_fb_lsb_rfifo_mem
121	mem_top_i/inst_mem_aexp_hist_stats_mem2
122	mem_top_i/inst_mem_ds_sharpen_dly1_mem_0
123	mem_top_i/inst_mem_fr_sharpen_dly2_mem_0
124	mem_top_i/inst_mem_iridix_fp2_pong_mem
125	mem_top_i/inst_mem_iridix_fp2_pong_mem2
126	mem_top_i/inst_mem_temper_delay_line_mem_1