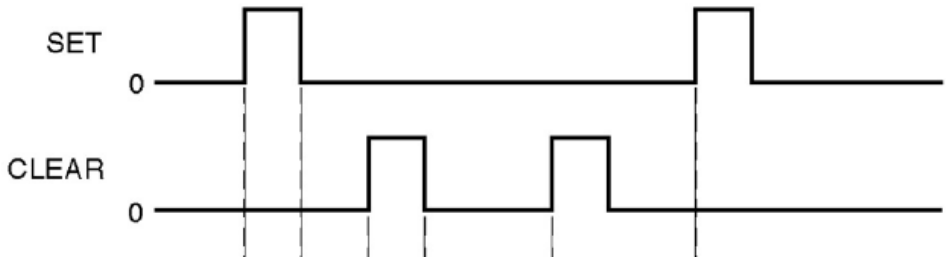
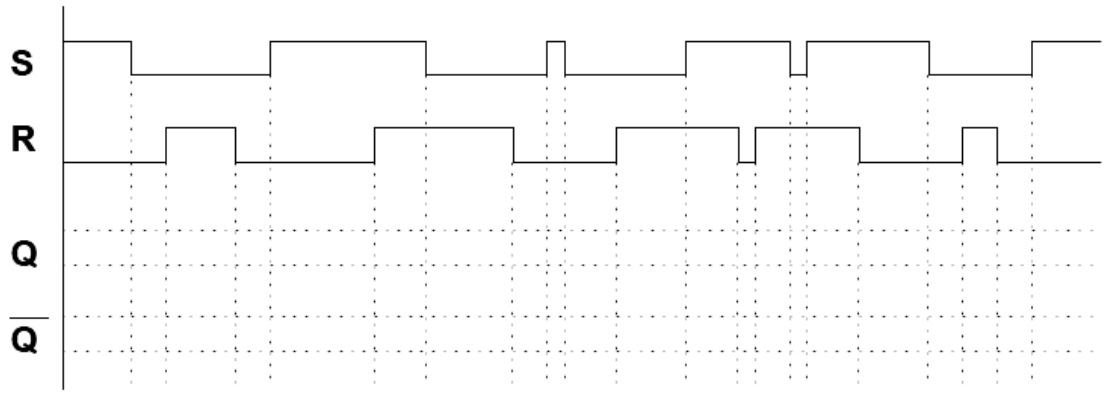
Circuitos Sequenciais

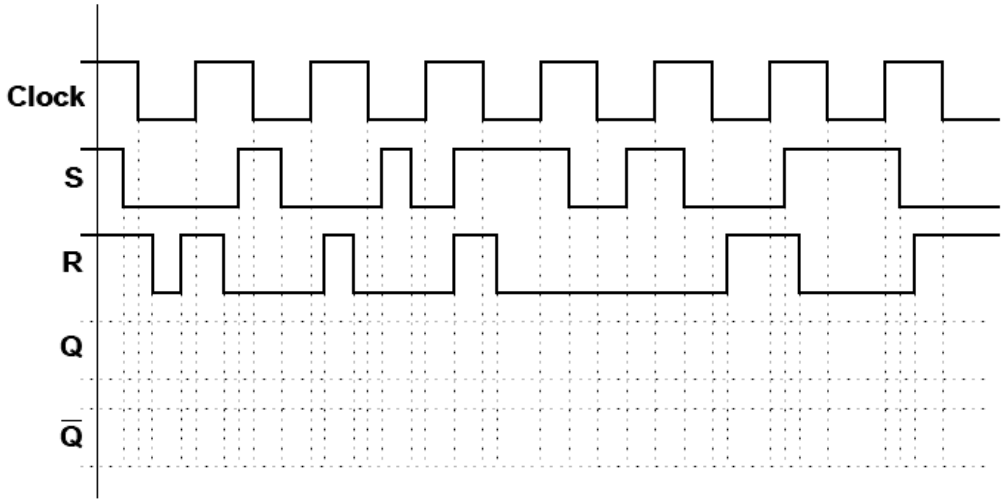
1. Represente as saídas do Latch SR assíncrono correspondente ao seguinte diagrama temporal



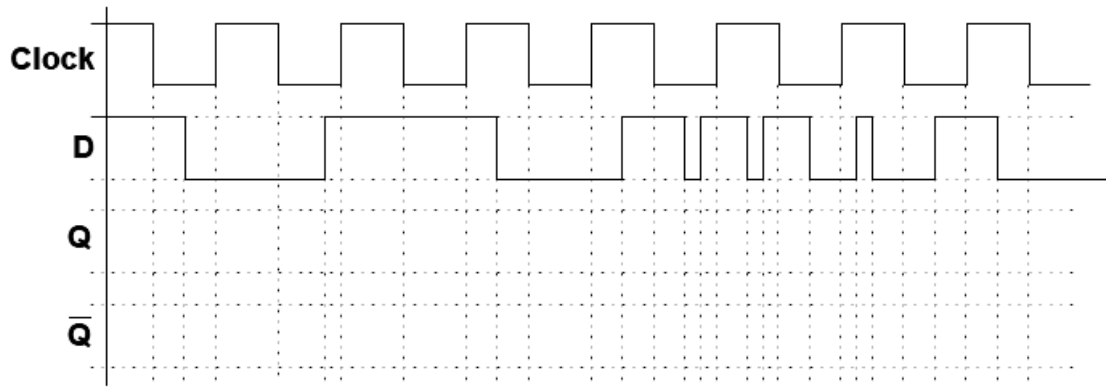
2. Complete o diagrama temporal do Latch RS assíncrono



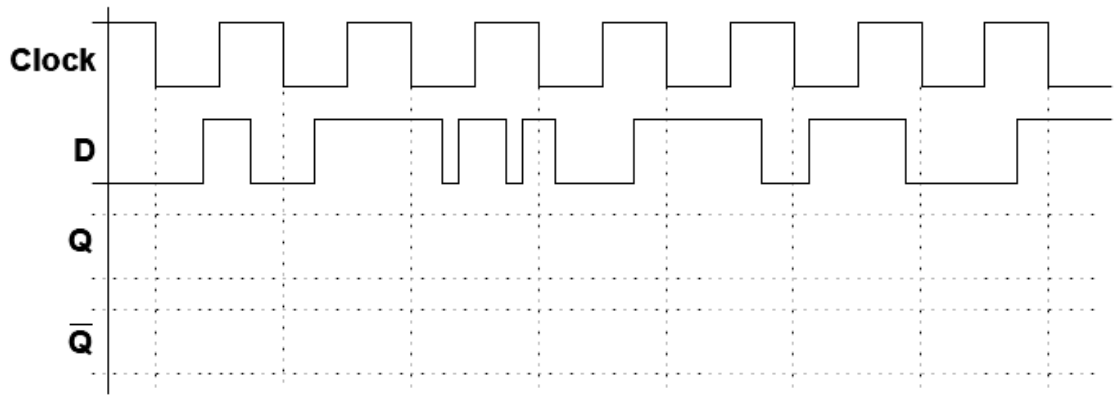
3. Complete o diagrama temporal do Latch SR síncrono sensível ao nível zero



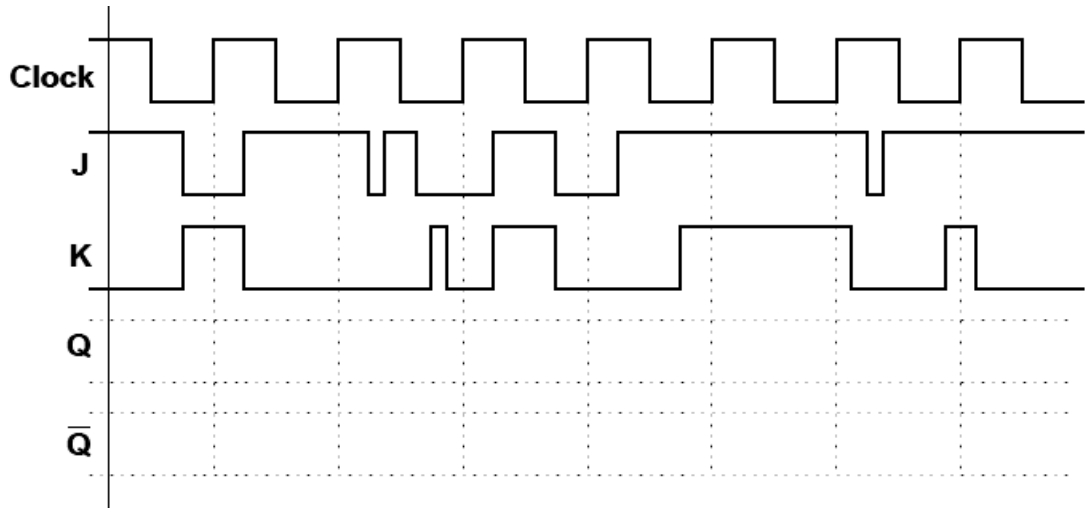
4. Complete o diagrama temporal do Latch D sensível ao nível alto



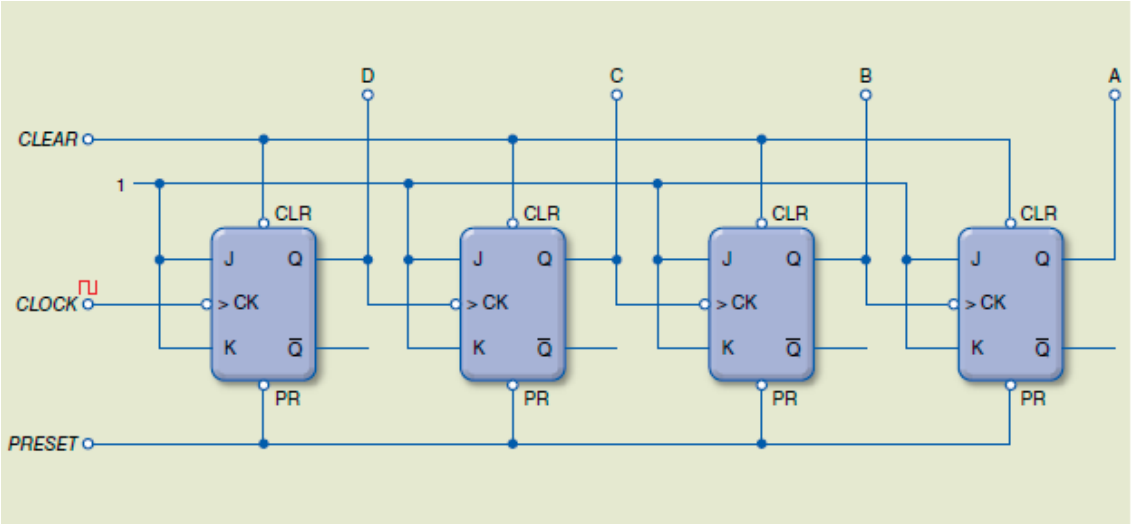
5.Complete o diagrama de tempo do latch D Síncrono sensível ao flanco descendente:



6. Complete o diagrama temporal do flip-flop ativo no flanco ascendente



7. Desenhe as saídas D, C, B e A



8. Complete o diagrama temporal do Latch T