1. Description

1.1. Project

Project Name	Stealth
Board Name	NUCLEO-F401RE
Generated with:	STM32CubeMX 6.9.2
Date	12/08/2023

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F401
MCU name	STM32F401RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration
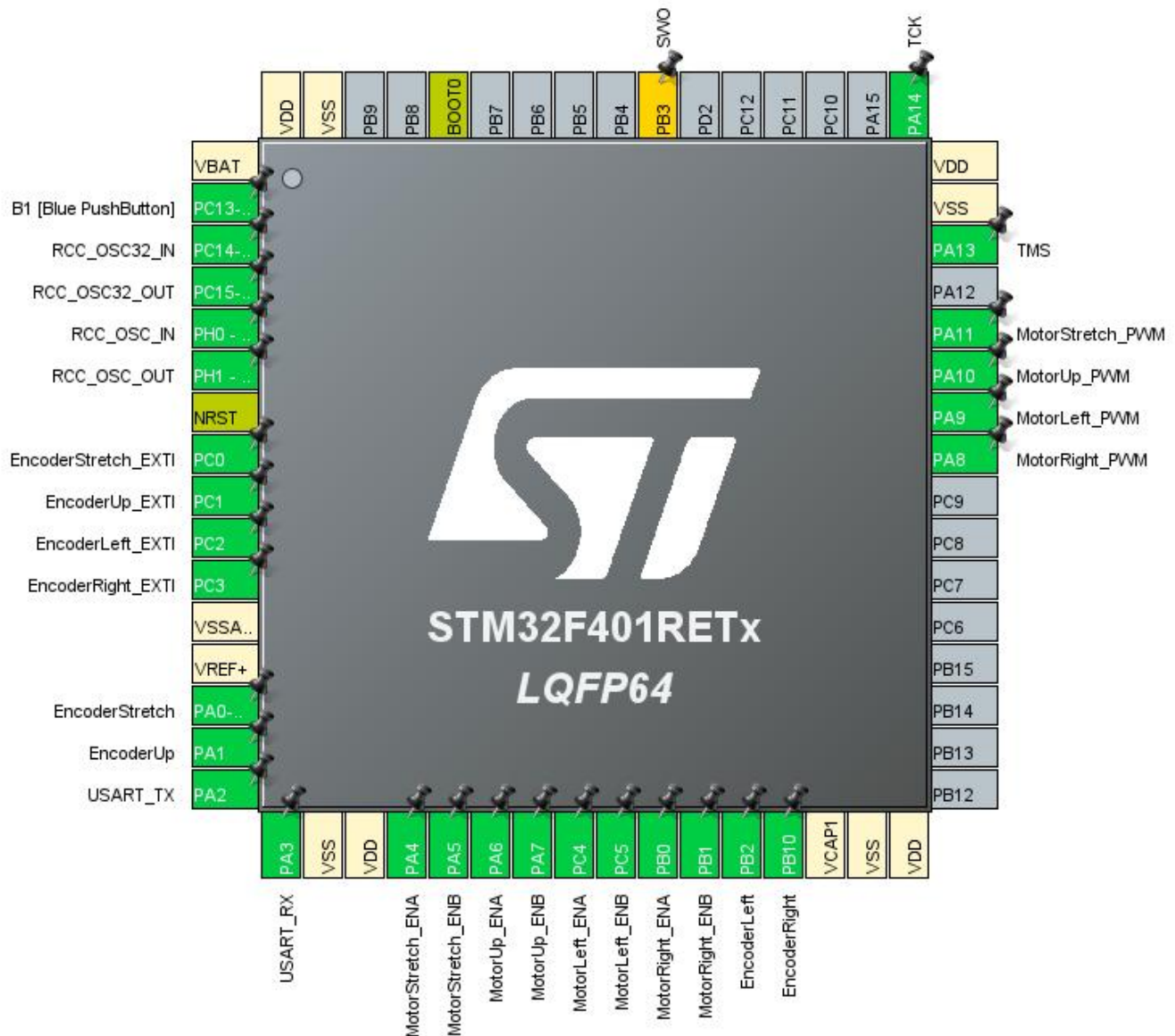
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	GPIO_EXTI0	EncoderStretch_EXTI
9	PC1	I/O	GPIO_EXTI1	EncoderUp_EXTI
10	PC2	I/O	GPIO_EXTI2	EncoderLeft_EXTI
11	PC3	I/O	GPIO_EXTI3	EncoderRight_EXTI
12	VSSA/VREF-	Power		
13	VREF+	Power		
14	PA0-WKUP *	I/O	GPIO_Input	EncoderStretch
15	PA1 *	I/O	GPIO_Input	EncoderUp
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	MotorStretch_ENA
21	PA5 *	I/O	GPIO_Output	MotorStretch_ENB
22	PA6 *	I/O	GPIO_Output	MotorUp_ENA
23	PA7 *	I/O	GPIO_Output	MotorUp_ENB
24	PC4 *	I/O	GPIO_Output	MotorLeft_ENA
25	PC5 *	I/O	GPIO_Output	MotorLeft_ENB
26	PB0 *	I/O	GPIO_Output	MotorRight_ENA
27	PB1 *	I/O	GPIO_Output	MotorRight_ENB
28	PB2 *	I/O	GPIO_Input	EncoderLeft
29	PB10 *	I/O	GPIO_Input	EncoderRight
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
41	PA8	I/O	TIM1_CH1	MotorRight_PWM
42	PA9	I/O	TIM1_CH2	MotorLeft_PWM
43	PA10	I/O	TIM1_CH3	MotorUp_PWM
44	PA11	I/O	TIM1_CH4	MotorStretch_PWM

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

 * The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration
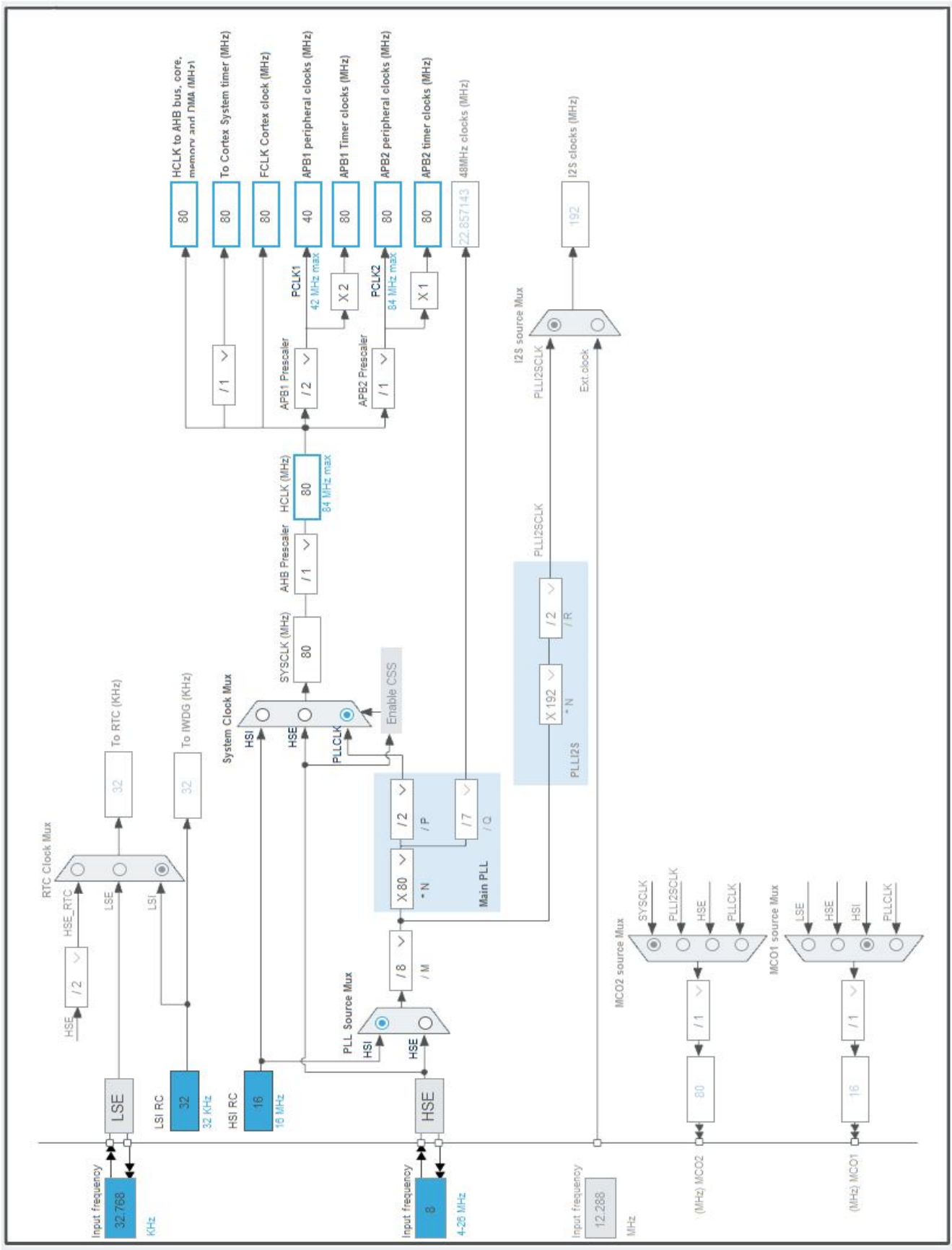
5. Software Project

5.1. Project Settings

Name	Value
Project Name	Stealth
Project Folder	D:\STM32CubeIDE\workspace_1.13.2\Stealth
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART2_UART_Init	USART2
4	MX_TIM1_Init	TIM1

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F401
MCU	STM32F401RETx
Datasheet	DS10086_Rev3

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale2-Medium	No Scale
Fetch Type	FLASH/ART/PREFETCH	n/a
CPU Frequency	84 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	21.6 mA	10 µA
Duration	0.1 ms	0.9 ms
DMIPS	105.0	0.0
Ta Max	101.44	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.17 mA
Battery Life	2 months, 4 days, 8 hours	Average DMIPS	105.0 DMIPS

1.6. Chart

Consumption Profile by Step
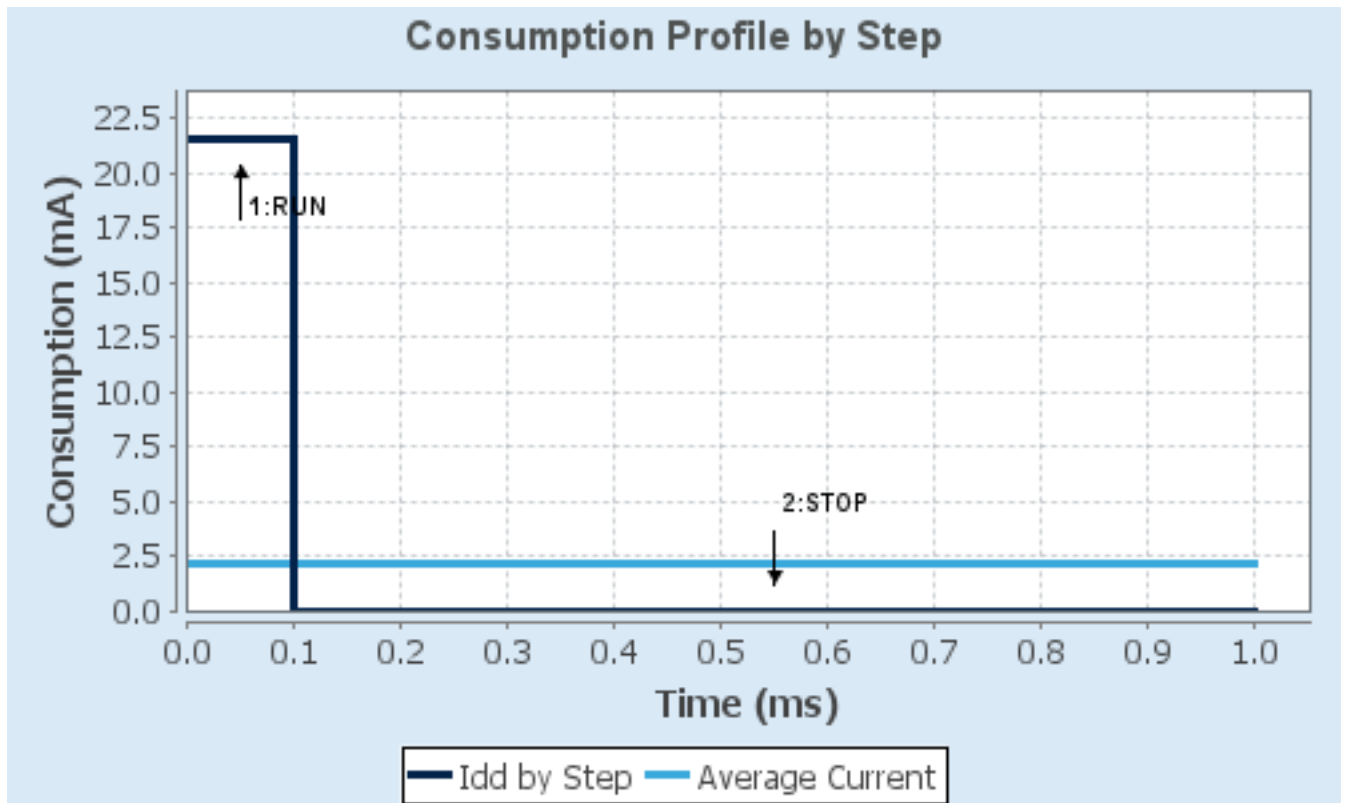
2. Peripherals and Middlewares Configuration

2.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

2.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 2

2.2. SYS

Debug: Serial Wire

Timebase Source: TIM5

2.3. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

2.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**7999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

auto-reload preload   Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)   Disable (Trigger input effect not delayed)

Trigger Event Selection   Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State   Disable

BRK Polarity   High

Break And Dead Time management - Output Configuration:

Automatic Output State   Disable

Off State Selection for Run Mode (OSSR)   Disable

Off State Selection for Idle Mode (OSSI)   Disable

Lock Configuration   Off

PWM Generation Channel 1:

Mode   PWM mode 1

Pulse (16 bits value)   0

Output compare preload   Enable

Fast Mode   Disable

CH Polarity   High

CH Idle State   Reset

PWM Generation Channel 2:

Mode   PWM mode 1

Pulse (16 bits value)   0

Output compare preload   Enable

Fast Mode   Disable

CH Polarity   High

CH Idle State   Reset

PWM Generation Channel 3:

Mode   PWM mode 1

Pulse (16 bits value)   0

Output compare preload   Enable

Fast Mode   Disable

CH Polarity   High

CH Idle State   Reset

PWM Generation Channel 4:

Mode   PWM mode 1

Pulse (16 bits value)   0

Output compare preload   Enable

Fast Mode   Disable

CH Polarity   High

CH Idle State   Reset

2.4. USART2
Mode: Asynchronous
2.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

2.5. FREERTOS
Interface: CMSIS_V1
2.5.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled

USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

2.5.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled

vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.5.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

* User modified value

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	MotorRight_PWM
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	MotorLeft_PWM
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	MotorUp_PWM
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	MotorStretch_PWM
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	USART_RX
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13-ANTI_TAMP	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EncoderStretch_EXTI
	PC1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EncoderUp_EXTI
	PC2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EncoderLeft_EXTI
	PC3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	EncoderRight_EXTI
	PA0-WKUP	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EncoderStretch
	PA1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EncoderUp
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorStretch_ENA
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorStretch_ENB
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorUp_ENA
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorUp_ENB

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorLeft_ENA
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorLeft_ENB
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorRight_ENA
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MotorRight_ENB
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EncoderLeft
	PB10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EncoderRight

3.2. DMA configuration

nothing configured in DMA service

3.3. NVIC configuration

3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line0 interrupt	true	5	0
EXTI line1 interrupt	true	5	0
EXTI line2 interrupt	true	5	0
EXTI line3 interrupt	true	5	0
EXTI line[15:10] interrupts	true	5	0
TIM5 global interrupt	true	15	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
USART2 global interrupt	unused		
FPU global interrupt	unused		

3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pendable request for system service	false	false	false
System tick timer	false	false	true
EXTI line0 interrupt	false	true	true
EXTI line1 interrupt	false	true	true
EXTI line2 interrupt	false	true	true
EXTI line3 interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM5 global interrupt	false	true	true

* User modified value

4. System Views

4.1. Category view

4.1.1. Current

5. Docs & Resources

Type   Link