NOTE: If architecture diag is asked, then first write features of that processor then draw.

PAGE NO.
DATE | 11 / 7 / 19

8085
→ | 8 bit | →

8086 16 bit
6 BQ → | BIU | EU | → ~~EU~~

80386   32 bit
16 BQ → | BIU | Decode | EU | →

32 bit
64×2 BQ → | BIU | D1 | D2 | EU | WB |
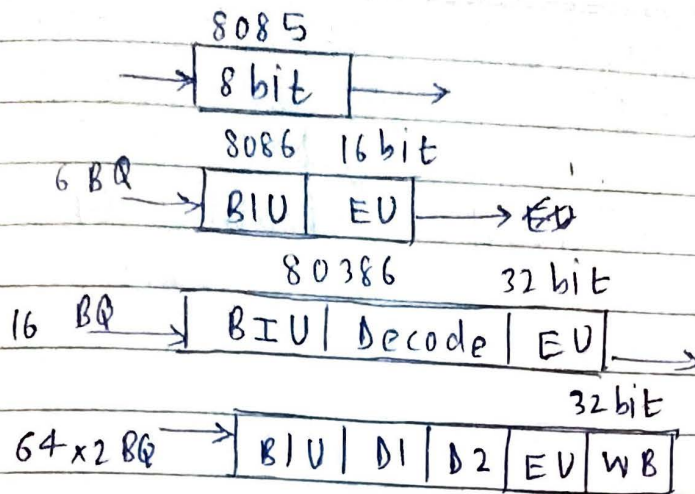
* Features of 80386 DX Processor:
① 32-bit microprocessor
② 8-bit addr bus and 32 bit data bus.
③ 8-bit data type
④ Very large addr space
⑤ 4GB physical memory.
⑥ 64TB virtual memory
⑦ Supports 16k no of segments
⑧ Integrated memory management unit
  (i) Virtual Memory Support
  (ii) Optional on-chip paging
  (iii) 4 levels of protection
⑨ Fully compatible with 80286 processor
⑩ Optimized for system performance
  (i) Pipeline System
  (ii) On-chip addr translation cache
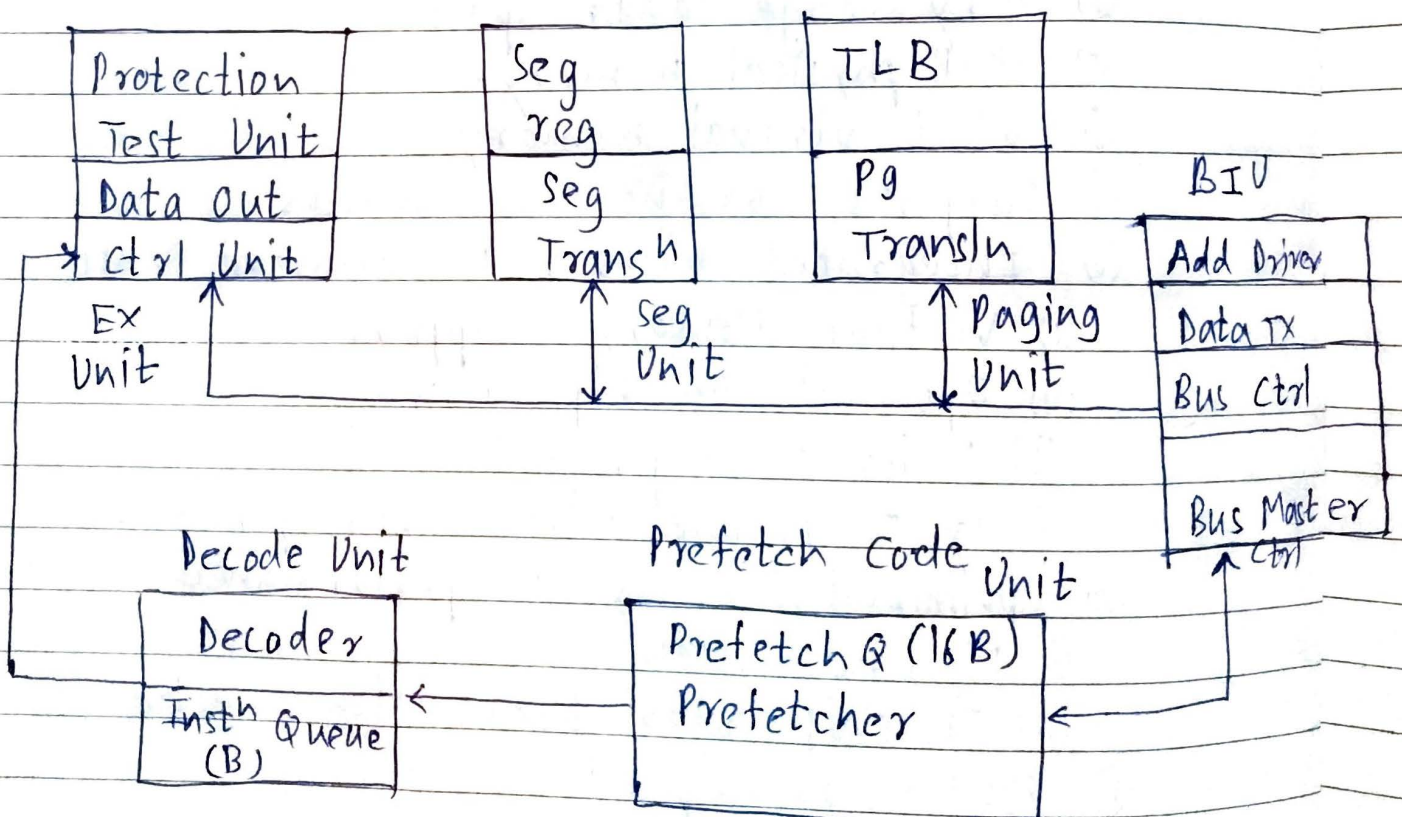⑪ Modes of Operation:
  (i) Real
  (ii) Protected

80386

SX   EX   DX

single DB   Embedded   Double DB
16 bit   32 bit
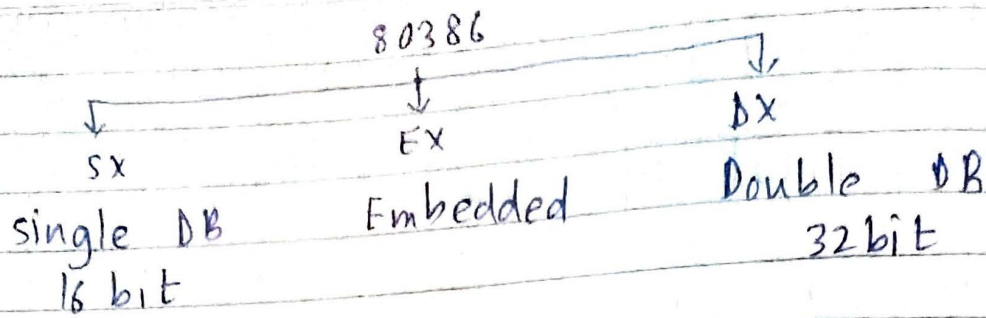
32 uP
32 AB
32 DB
4GB → physical Mem
64TB → virtual Mem

Internal Architecture 80386 Dx processor:

Protection Test Unit Data Out Ctrl Unit	Seg reg Seg Trans^h	TLB Pg Transl^n	BIU Add Driver

EX Unit   Seg Unit   Paging Unit   Data TX

Bus Ctrl

Bus Master Ctrl

Decode Unit   Prefetch Code Unit

| Decoder | | Prefetch Q (16B) |
| Inst^h Queue (B) | ← | Prefetcher |

* Operating Nodes

$$PE = 1$$

Real $\longrightarrow$ Protected
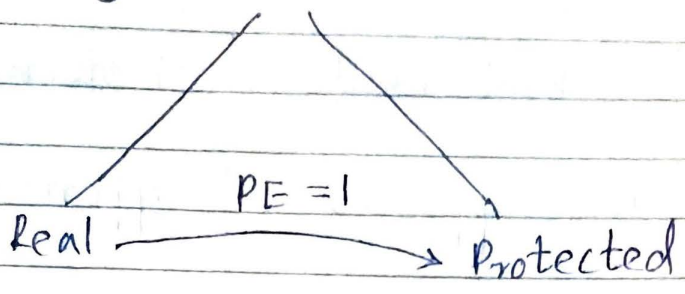
same as   — Multitasking
    8086 $PE = 0$ — VM
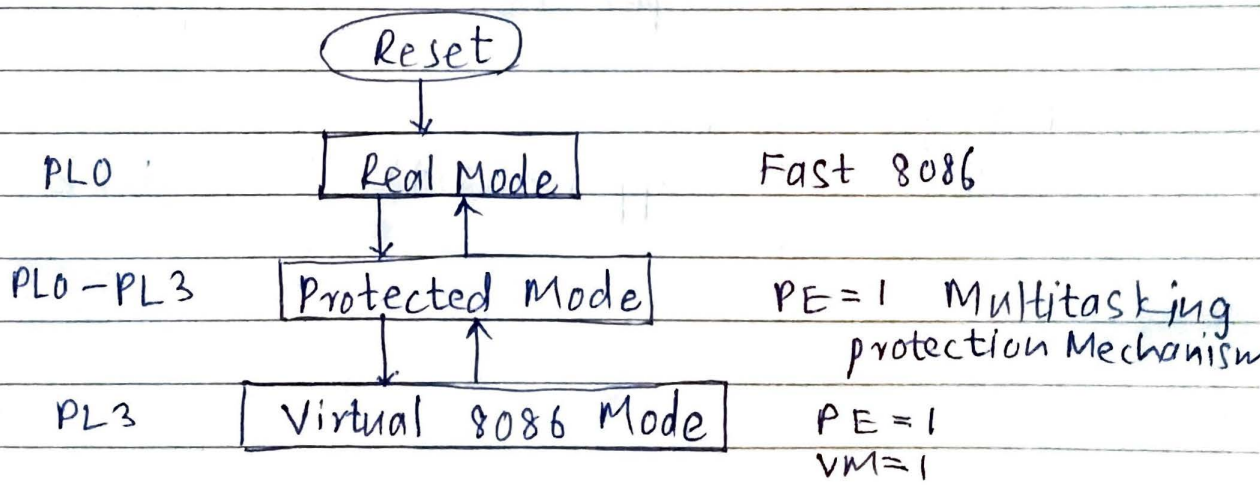   — Protection Mechanism
1 task $PE = 1$
                                    $VM = 0$

* Operating Model:

                 (Reset)

PLO | Real Mode | Fast 8086

PLO — PL3 | Protected Mode | $PE = 1$ Multitasking
                                       protection Mechanism

PL3 | Virtual 8086 Mode | $PE = 1$
                                       $VM = 1$

Mode Transition Diagram