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COS10004 - Computer Systems – Lab 2 Submission

Part 1

Screenshot of the circuit for the first row of the table

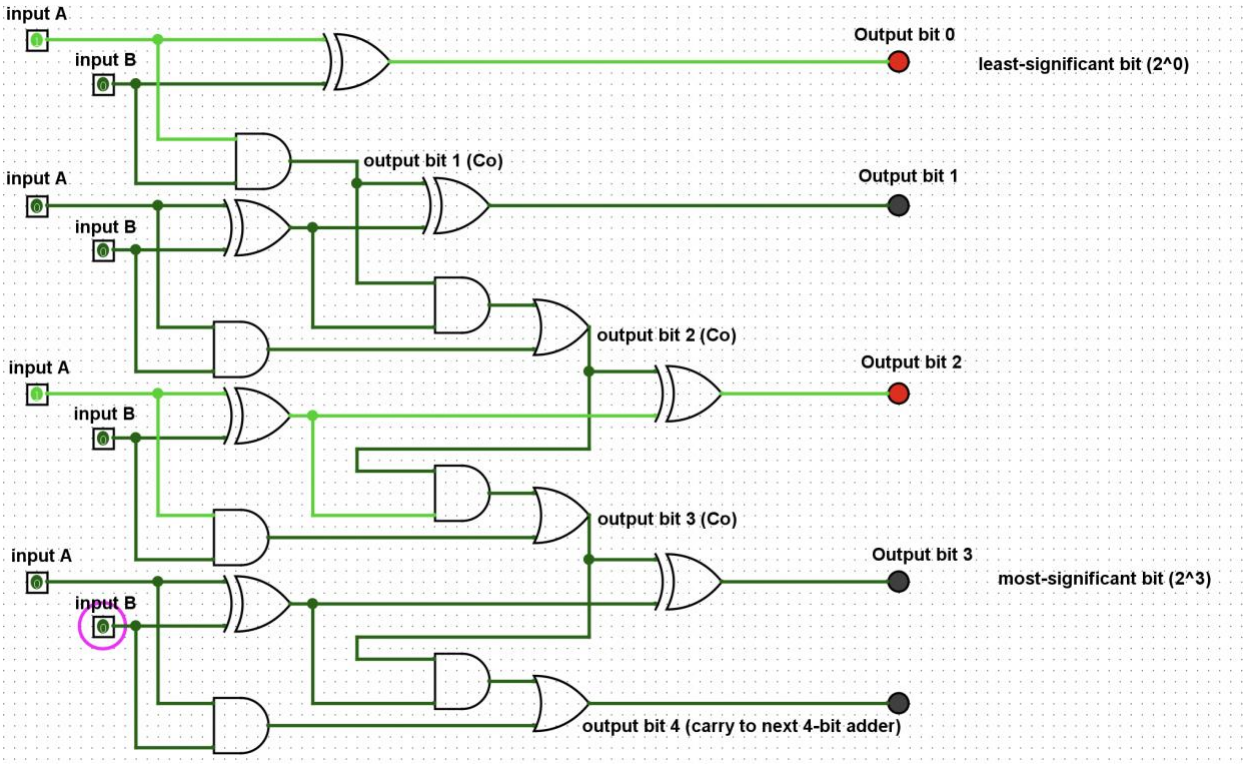

Figure 1. Circuit for the first-row data
Screen captured from my Mac on September 22nd, 2022

Truth table

Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

Part 2
Screenshot of RS Flip Flop using 2-input NOR gates

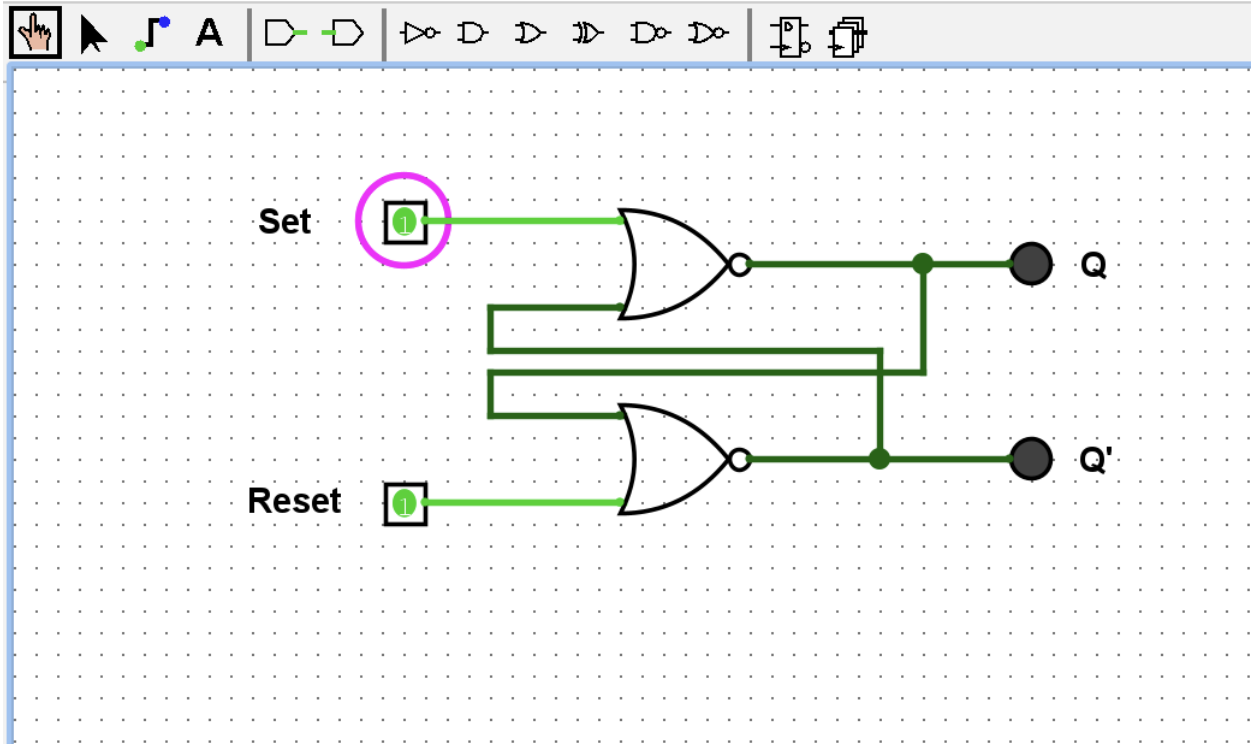

Figure 2. RS Flip Flop using 2-input NOR gates
Screen captured from my Mac on September 22nd, 2022

Truth table

Set	Reset	Q	Q'
1	0	0	1
0	0	0	1
0	1	1	0
1	1	0	0

Description of the behaviors of the circuit above when one of the inputs is 1

If we open the Set and close the Reset, Q will be 0 and Q' will be 1.
Similarly, when two inputs are closed, the output will be no different from the previous case.
However, if we open the Reset and close the Set, Q will be 1 and Q' will be 0.

If we set both inputs to 1

Two gates will race each other to feedback their new outputs infinitely and we cannot know which one will win.

Screenshot of D Flip Flop

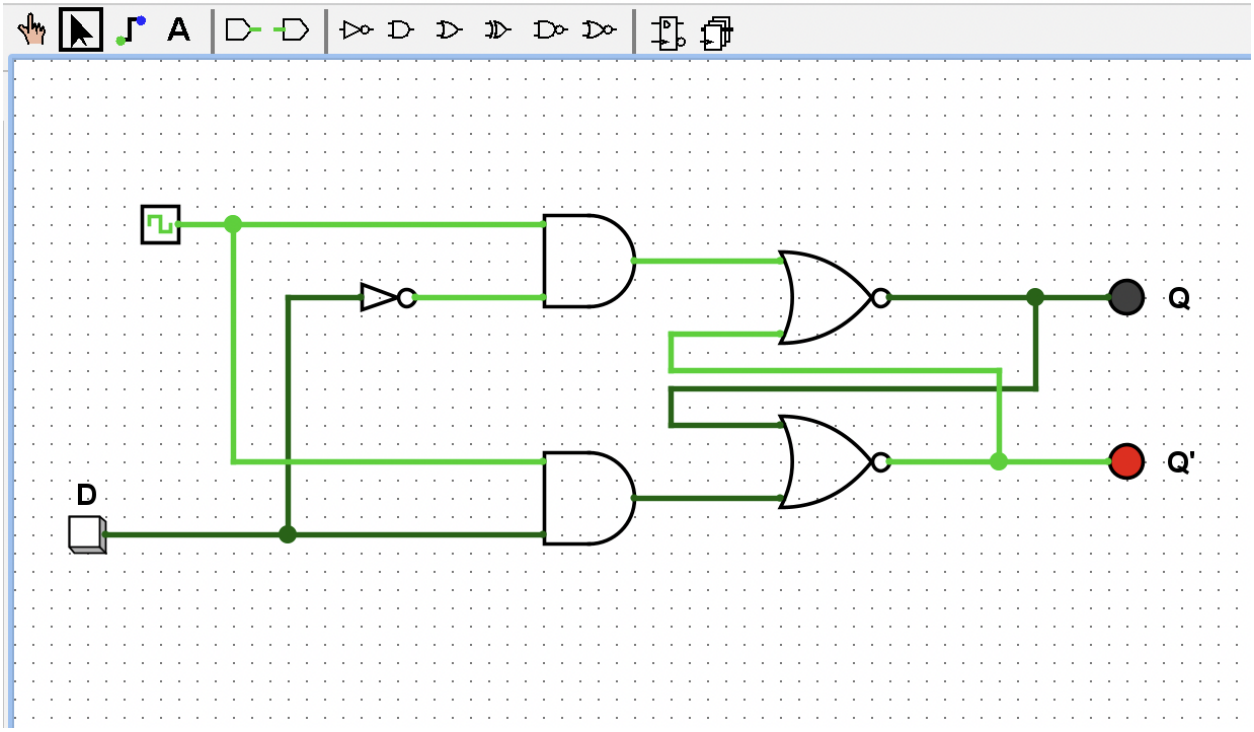

Figure 3. D Flip Flop
Screen captured from my Mac on September 22nd, 2022

Truth table for D Flip Flop

Clock	Pin	Q	Q’
0	**0**	0	1
0	**1**	0	1
1	**1**	1	0
1	**0**	0	1

Description of the behaviors of D Flip Flop

This D Flip Flop has only 1 input with the manipulation of the clock, when the input is set to 1,

In case the clock is 1:

- if the input is set to 1, Q will be 1 and Q' will be 0
- if the input is set to 0, Q will be 0 and Q' will be 1

In case the clock is 0: we cannot modify Q and Q' despite changing input D

Leverage: Input D can be considered as an input with two functions: Set and Reset

Role of the clock and its impact

The clock impacts the input data and the output not only depends on input data but also clock's status. It guarantees the synchronization of data input and ensures the predictability.

Why is it generally preferred over the R-S Flip Flop ?

Because the D Flip Flop guarantees that there are no indeterminant state with both active inputs in the R-S Flip Flop.

Screenshot of JK Flip Flop

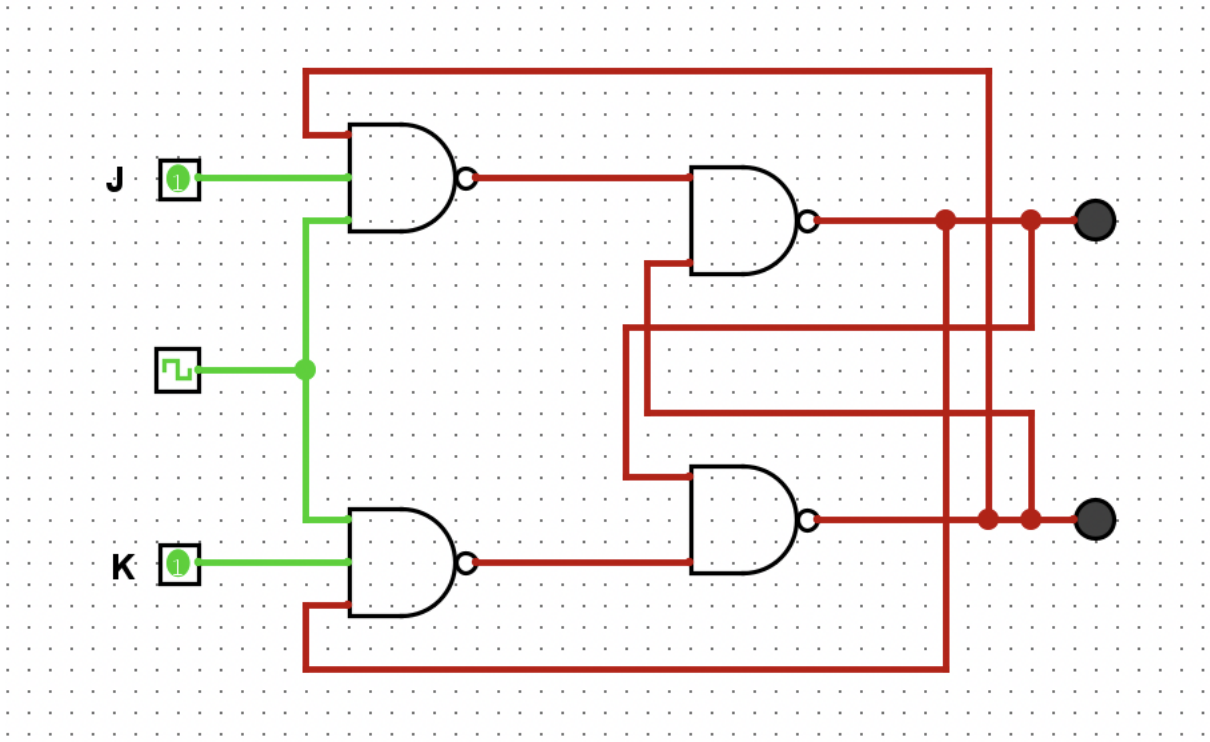

Figure 3. JK Flip Flop
Screen captured from my Mac on September 22nd, 2022

Truth table for JK Flip Flop

J	K	Q (when clocked)	Q' (when clocked)
0	0	No change	No change
1	0	1	0
0	1	0	1
1	1	Toggle	Toggle

Making JK Flip Flop behave like D Flip Flop

We can do this by driving the J and K inputs with D input, also, a NOT gate is required for this process.

J-K Flip Flop be made to behave like a toggle

When J and K are set to be 1