Electronic Workshop 2

Manikya Pant
2023112024
manikya.pant@research.iiit.ac.in

Harshit Goyal
2023102054
harshit.goyal@students.iiit.ac.in

I. Introduction

The aim of this project was to build an audio amplifier with the following specifications:

- Supply Voltage: ± 12V
- Input small signal voltage: 10–20 mV (peak-to-peak)
- Gain: $G \geq 500$ (Pre-amplifier and Gain stage)
- Frequency Range: Audible range (20 Hz to 20 kHz)
- Power Output: ≥ 1.5 W
- Filter should not attenuate the input signal
- Load: $10, \Omega$
- Power amplifier should not provide voltage gain

II. Pre Amp Stage

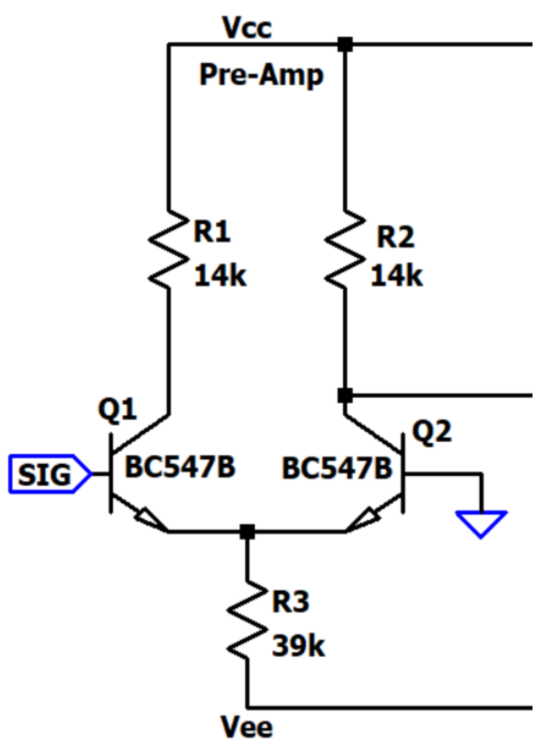


Fig. 1. Pre Amp circuit

We want the input impedance of the first stage to be low, as the microphone can't supply a high value of current. So we used a differential amplifier, as it also helps us to remove the noise by the nature of the differential amplifier. This stage is serving as an initial gain and removing noise from the inputs.

We use a single input unbalanced output differential amplifier configuration. In this, the signal is applied only to one of , while the other terminal is grounded.

This configuration gives the voltage gain of -$g_m R_c$

The values of $R_c = 14k\Omega$ and $R_e = 39k\Omega$. Simulation-wise this gives us a gain of 23.1

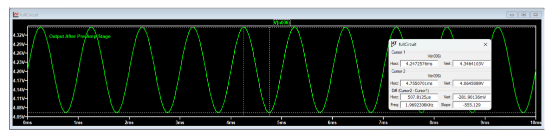


Fig. 2. Output of preamp stage giving a gain ratio of 23.1

On breadboard we get a gain ratio of around 21 , which is close to the value simulated

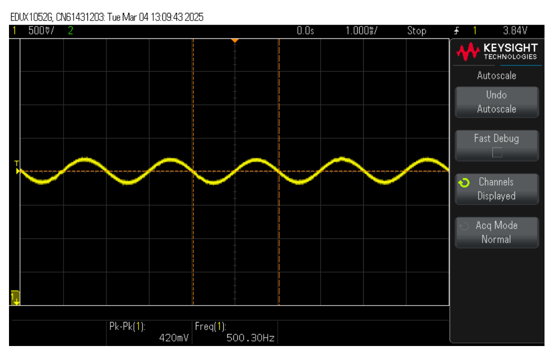


Fig. 3. Output of preamp stage giving a gain ratio of 21

From simulation we try to find the CMRR of the signal. Ideally the common mode gain of the differential amplifier should be 0, as it rejects common mode noise, but due to non idealness it has some finite value

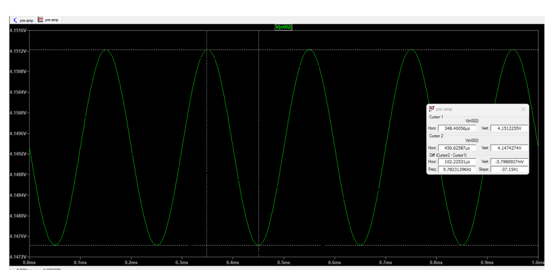


Fig. 4. Commom mode gain

The common mode gain ratio of the pre amp is $\frac{3.79}{20} = 0.18$
The differential gain ratio of the pre amp is 23.1
CMRR= $20\log\frac{A_d}{A_c} = 20log\frac{23.1}{0.18} = 42.16$

III. Common Emitter Amplifier

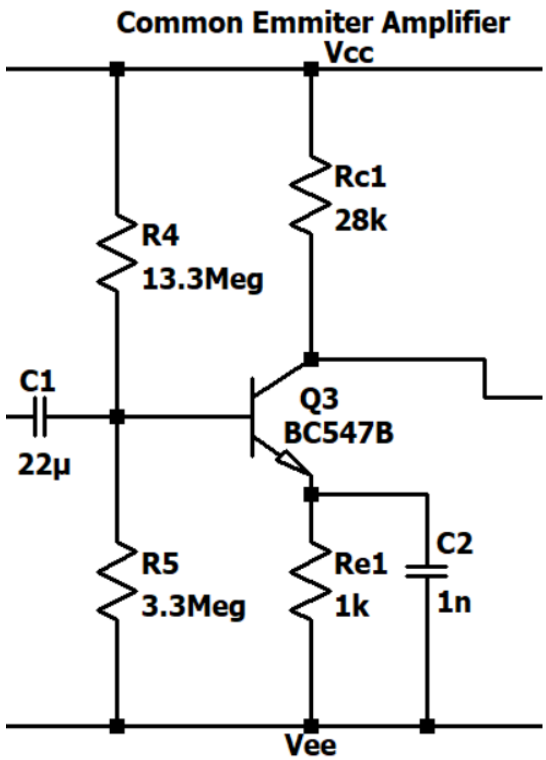


Fig. 5. Common Emitter (CE) amplifier circuit.

The common emitter (CE) amplifier stage receives the output signal from the pre-amplifier and further amplifies it, completing the overall amplification process. The input signal is coupled to the CE stage via a coupling capacitor, which blocks the DC component from the pre-amplifier's output, ensuring only the AC signal is amplified.

To minimize loading effects on the preceding stages, the biasing resistances were chosen in the order of mega-ohms. This design choice eliminates the need for an additional buffer stage, resulting in a more power-efficient circuit.

The voltage gain of the CE amplifier is given by:

$$A_v = -\frac{R_c}{\frac{1}{g_m} + R_e}$$

For large values of R_e, the term $\frac{1}{g_m}$ becomes negligible, simplifying the gain equation to:

$$A_v \approx -\frac{R_c}{R_e}$$

This approximation provides a straightforward relationship between the gain and the resistor values, making the design and analysis of the amplifier more intuitive.

A. Simulation Results

Simulation of the circuit yielded a voltage gain of approximately 22, as shown in Figure 6.

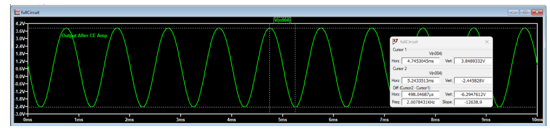


Fig. 6. Simulation results of the CE amplifier with input from the pre-amplifier stage.

B. Experimental Results

The breadboard implementation of the circuit produced a voltage gain of 20.6, as shown in Figure 7. The input signal had a peak-to-peak amplitude of 210 mV, resulting in an output signal consistent with the expected gain.

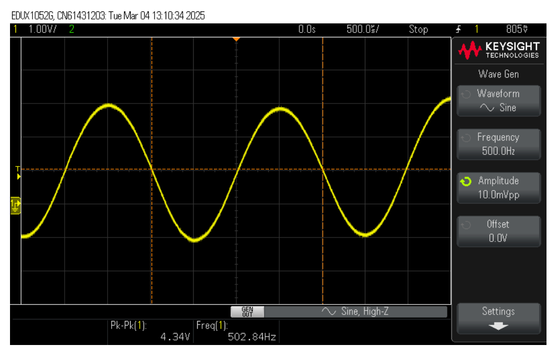


Fig. 7. Experimental results of the CE amplifier with input from the pre-amplifier stage.

The experimental gain of 20.6 is in close agreement with the simulated gain of 22, validating the design and implementation of the CE amplifier stage.
This makes our total gain ratio of around **434** , combining both the gain stages, as the further stages don't provide any gain

a) Definition:: The stability factor (S) quantifies how much the **collector current** (I_C) changes with **changes in current gain** (β). It is commonly defined as:

$$S = \frac{dI_C}{d\beta}$$

The ideal value of S is **1**, which indicates **no change** in collector current despite variations in β. Higher values indicate **less stability**.

1) Why Is Stability Important in Audio Amplifiers?:

1) **Temperature Variations:**
   - Amplifiers generate heat during operation, causing changes in **transistor parameters**, especially (β).
   - A high stability factor can cause **thermal runaway**, leading to **distorted audio output or damage** to the amplifier.
2) **Component Aging:**

- As components age, their parameters may change, particularly **transistors** and **capacitors**.
- An amplifier with a **low stability factor** is more robust against these changes.

3) **Feedback and Stability:**
   - Audio amplifiers often use **negative feedback** to **improve stability** and reduce distortion.
   - Proper feedback design reduces the **sensitivity of the output to variations** in transistor parameters.

IV. Active Band-Pass Filter

In the design of an audio amplifier, it is essential to ensure that only audible frequencies are present in the output. The human hearing range typically spans from 20 Hz to 20 kHz. To achieve this, we employ an **active band-pass filter** that allows frequencies within this range to pass while attenuating frequencies outside it.

Active filters are preferred over passive RC filters for several reasons: - **High Input Impedance and Low Output Impedance**: This minimizes loading effects between circuit stages, ensuring that the filter does not significantly affect the signal source or the load. - **Gain Control**: Active filters provide better control over the gain within the passband. - **Precision**: They offer more precise control over the filter's characteristics, such as cutoff frequencies and bandwidth.

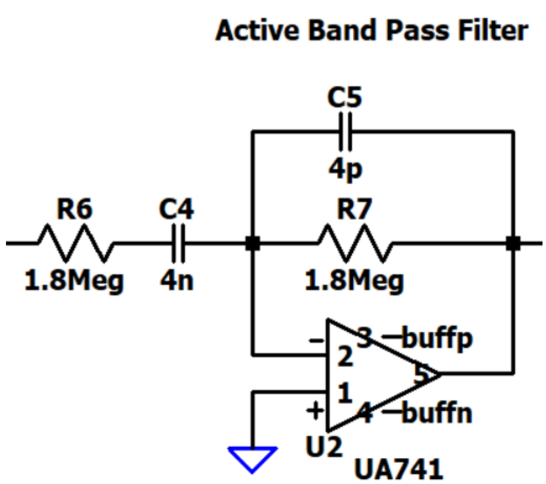


Fig. 8. Active band-pass filter circuit.

A. Circuit Design

The active band-pass filter is essentially a combination of a **high-pass filter** and a **low-pass filter**. The cutoff frequencies for these filters are given by:

$$f_{c1} = \frac{1}{2\pi R_1 C_1} \quad \text{(High-pass cutoff)}$$

$$f_{c2} = \frac{1}{2\pi R_2 C_2} \quad \text{(Low-pass cutoff)}$$

For our design, the cutoff frequencies (3 dB points) are set to **20 Hz** and **20 kHz**, corresponding to the lower and upper limits of the audible frequency range. Due to the unavailability of exact resistor and capacitor values to achieve these precise frequencies, we selected components that provide close approximations.

The gain in the passband region is given by:

$$A_v = \frac{-R_2}{R_1}$$

To simplify the design, we chose $R_1 = R_2$, resulting in a gain of **-1** in the passband. The values that we have selected theoretically gives cutoff at 22hZ and 22khZ

B. Simulation Results

The simulation results confirm the expected behavior of the filter: - The gain in the passband is approximately **-1**. - The cutoff frequencies are close to **20 Hz** and **20 kHz**.

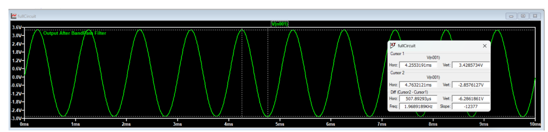


Fig. 9. Output waveform of the band-pass filter from simulation.

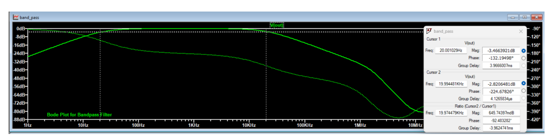


Fig. 10. Frequency response of the band-pass filter from simulation.

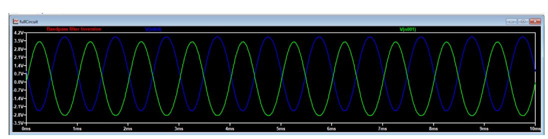


Fig. 11. Inverted output of the filter with unity gain

C. Experimental Results

The circuit was implemented on a breadboard, and the following results were obtained: - The measured cutoff frequencies were **19.7 Hz** and **20.3 kHz**, which are in close agreement with the design specifications. - The gain in the passband was consistent with the expected value of **-1**.

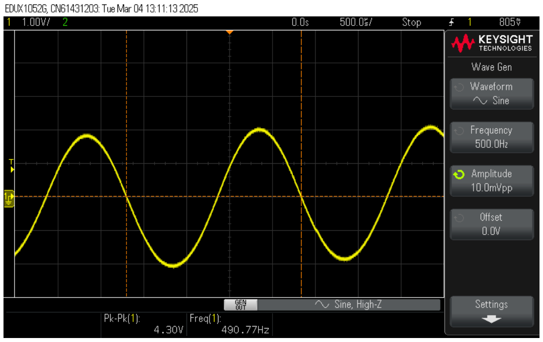


Fig. 12. Output waveform of the band-pass filter from the breadboard implementation.

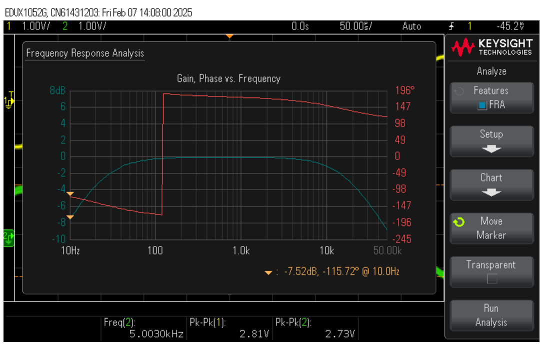


Fig. 13. Frequency response of the band-pass filter from the breadboard implementation.

D. Conclusion

The active band-pass filter successfully isolates the audible frequency range (20 Hz to 20 kHz) while providing a stable gain of **-1**. Both simulation and experimental results demonstrate close agreement with the design specifications, validating the effectiveness of the filter in the audio amplifier circuit. Experimentally we got the cutoff to be 19.7hZ and 20.3Khz.

V. Power Amplifier

Since we need to drive a speaker load with our amplified signal , the signal should have power above some minimum value. The design requirements asked us to have a power of more than 1.5W. The class AB power amplifier receives the amplified and filtered output from the preceding stages, and amplifies the current thus amplifying the overall power being supplied to the speaker at the output. The Class AB power amplifier has been designed using TIP-31 and TIP-32 power transistors, since they can handle large amounts of current flowing through them and they have faster switching speeds unlike normal transistors. We have also used heat sinks along with the transistors. Since Class AB amplifiers do not operate at full power continuously, they generate less heat compared to Class A amplifiers. This makes them more suitable for portable and high-power applications where heat dissipation is a concern.

Class B amplifiers suffer from crossover distortion, which occurs when the input signal crosses zero and there is a delay in switching between the two complementary transistors. Class AB amplifiers bias the transistors slightly into conduction, eliminating this distortion and providing smoother output waveforms. Class AB amplifiers operate in a region where both transistors are partially conducting, even at low signal levels. This results in better linearity and lower distortion compared to Class B amplifiers, which completely turn off one transistor during half of the input cycle.

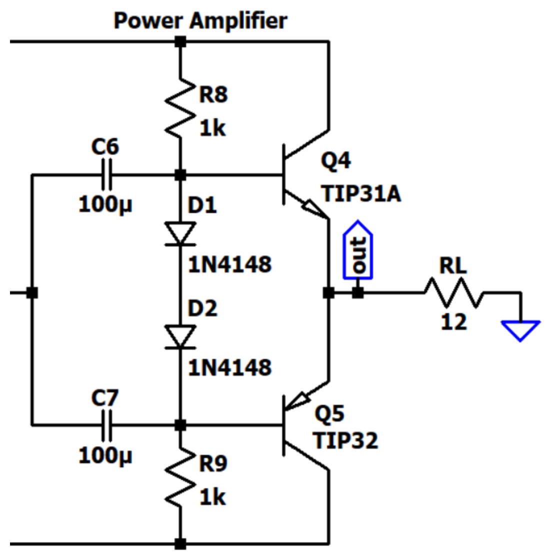


Fig. 14. Power amp circuit

The diodes tend to have a potential difference as same as that of V_{be} so that cross over distortion doesn't happen , making both the transistors on. We have used 1k resistors in order to bias the transitors.

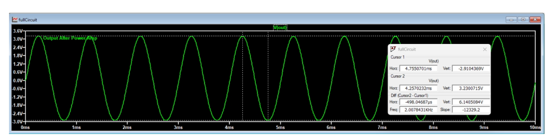


Fig. 15. Output of power amp

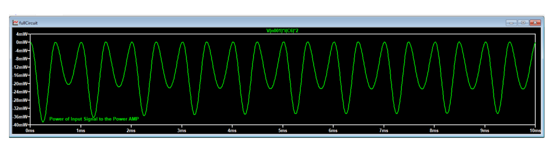


Fig. 16. Input power to the power amplifier

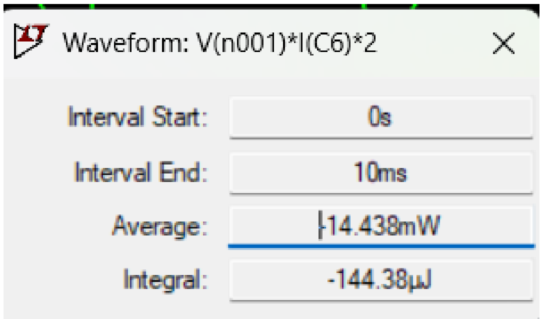


Fig. 17. average Input power to the power amplifier

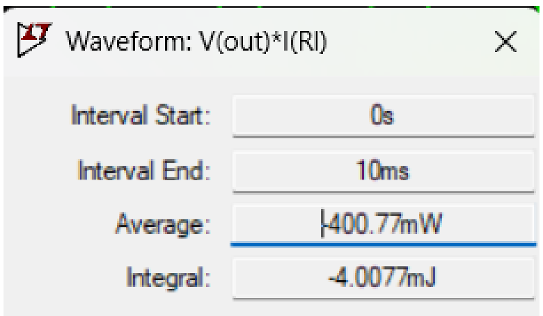


Fig. 18. Average output power of the power amplifier

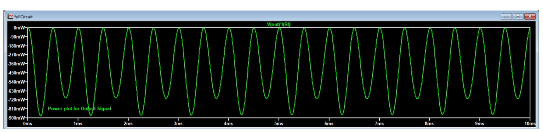


Fig. 19. Output power to the power amplifier

We can clearly see that the output power has increased and can now be used to drive the speaker load.

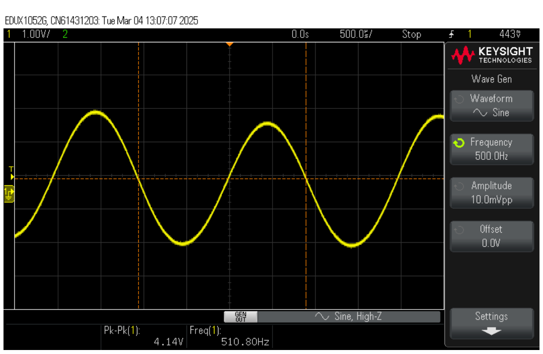


Fig. 20. Output of the power amplifier

VI. Full Circuit

A. Simulation results

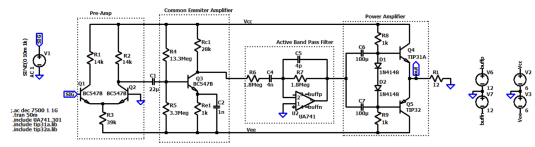


Fig. 21. Full circuit

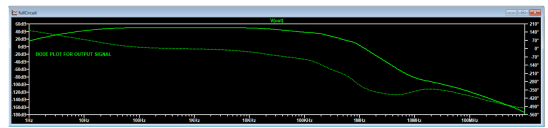
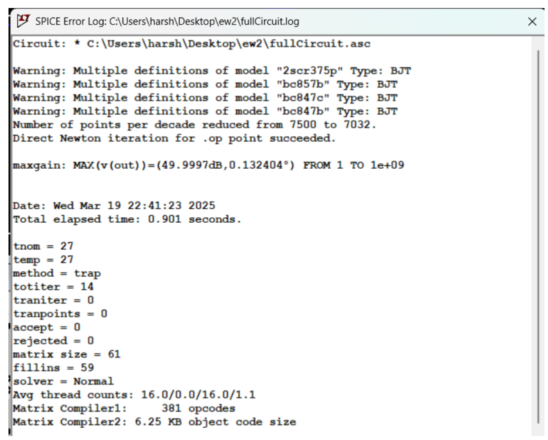


Fig. 22. Bode plot of the full circuit



```
SPICE Error Log: C:\Users\harsh\Desktop\ew2\fullCircuit.log
Circuit: * C:\Users\harsh\Desktop\ew2\fullCircuit.asc

Warning: Multiple definitions of model "2scr375p" Type: BJT
Warning: Multiple definitions of model "bc857b" Type: BJT
Warning: Multiple definitions of model "bc847c" Type: BJT
Warning: Multiple definitions of model "bc847b" Type: BJT
Number of points per decade reduced from 7500 to 7032.
Direct Newton iteration for .op point succeeded.

maxgain: MAX(v(out))=(49.9997dB,0.132404°) FROM 1 TO 1e+09


Date: Wed Mar 19 22:41:23 2025
Total elapsed time: 0.901 seconds.

tnom = 27
temp = 27
method = trap
totiter = 14
traniter = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 61
fillins = 59
solver = Normal
Avg thread counts: 16.0/0.0/16.0/1.1
Matrix Compiler1:     381 opcodes
Matrix Compiler2: 6.25 KB object code size
```

Fig. 23. Maximum gain of the circuit

B. Experimental results

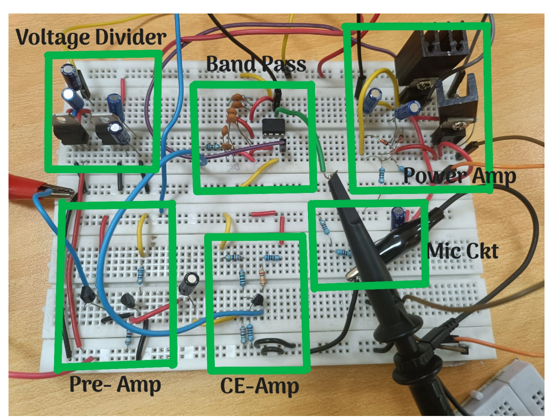


Fig. 24. Full circuit

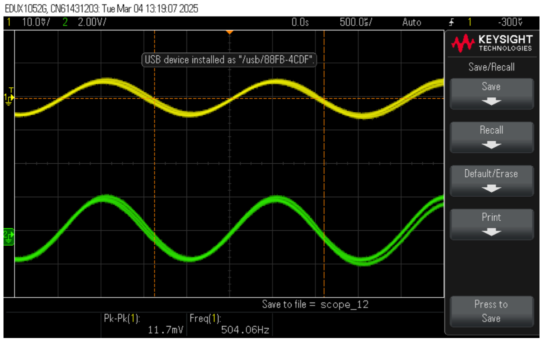


Fig. 25. Input and output of the circuit

We can see that the output is the amplified inphase version of the input signal, we can see the difference in scale of the 2 signals.

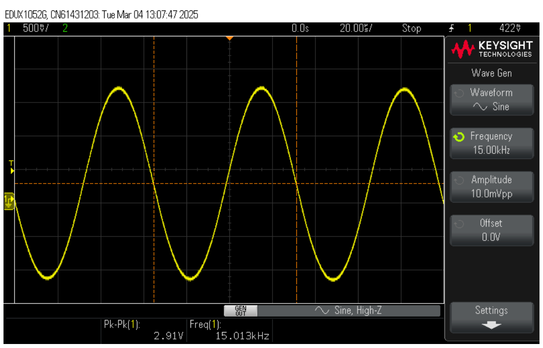


Fig. 26. Output when input is of 15khZ and 10mVpp

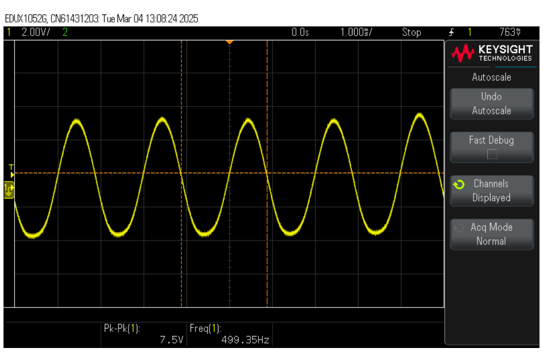


Fig. 27. Output when input is of 500HZ and 20mvpp

The lower cutoff of the final circuit is 22Hz, below is the plot of it .

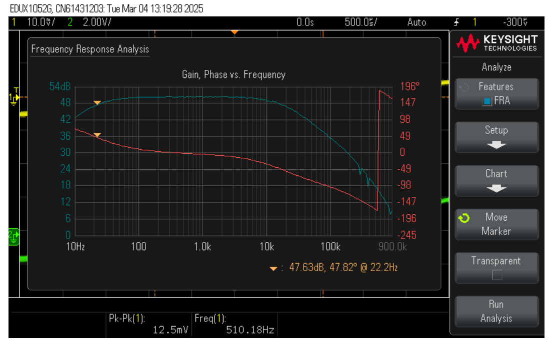


Fig. 28. Bode plot of the full circuit showing lower cutoff

The upper cutoff of the final circuit is 19.70Khz , below is the plot of it

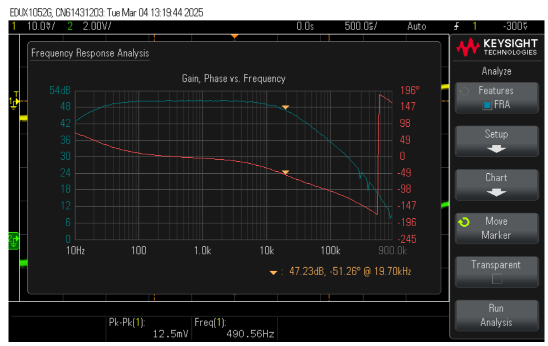


Fig. 29. Bode plot of the full circuit showing upper cutoff

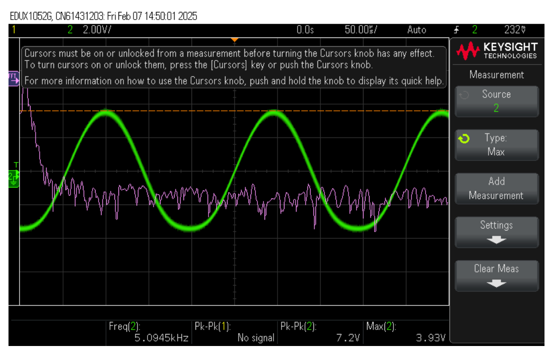


Fig. 30. FFT of the output signal

FFT of the output signal, shows that the frequency of the output signal is same as that of the input.

VII. Circuit Parameters

A. Total harmonic distortion

Distortion Analysis is done to figure out the amount of unwanted harmonic content in the frequency content of a signal. It can further elaborate on the behaviour of the circuit at different frequencies. Since the amplifier operates in the non linear, there will be components of other harmonics present in the output signal. Having a large THD leads to distortion in the output amplified signal, which can be manifested in the

form of skewed or flat regions in the signal. This is disastrous for an audio signal as any skewing or slewing in the input signal can lead to complete destruction of the quality of the audio of the output.
A lower THD also means higher efficiency magnification of the signal, and a higher quality output.
THD can be improved by trying to minimise the circuit interference and by adding filters to shut down higher unwanted harmonic currents in the system. Resistive capacitive filters effectively kill the higher order harmonics, improving the THD of the circuit

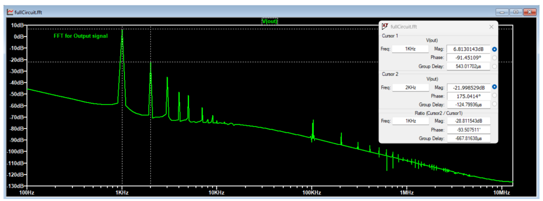


Fig. 31. Frequency analysis of the output

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n_{\text{RMS}}}^2}}{V_{f_{\text{RMS}}}}$$

Given the frequency response data:

Frequency (Hz)	Amplitude (dB)
1k (Fundamental)	5.69
2k (2nd Harmonic)	-21
3k (3rd Harmonic)	-35.5
4k (4th Harmonic)	-47
5k (5th Harmonic)	-49

$$V_1 = 10^{\frac{5.69}{20}} = 10^{0.2845} \approx 1.92$$
$$V_2 = 10^{\frac{-21}{20}} = 10^{-1.05} \approx 0.089$$
$$V_3 = 10^{\frac{-35.5}{20}} = 10^{-1.775} \approx 0.0168$$
$$V_4 = 10^{\frac{-47}{20}} = 10^{-2.35} \approx 0.00447$$
$$V_5 = 10^{\frac{-49}{20}} = 10^{-2.45} \approx 0.00355$$

$$V_2^2 = (0.089)^2 \approx 0.00792$$
$$V_3^2 = (0.0168)^2 \approx 0.000282$$
$$V_4^2 = (0.00447)^2 \approx 0.000020$$
$$V_5^2 = (0.00355)^2 \approx 0.0000126$$

$$\text{Sum} = V_2^2 + V_3^2 + V_4^2 + V_5^2$$
$$\approx 0.00792 + 0.000282 + 0.000020 + 0.0000126 \approx 0.00823$$

$$\sqrt{\text{Sum}} = \sqrt{0.00823} \approx 0.0907$$

$$\text{THD} = \frac{0.0907}{1.92} \times 100\% \approx 4.72\%$$

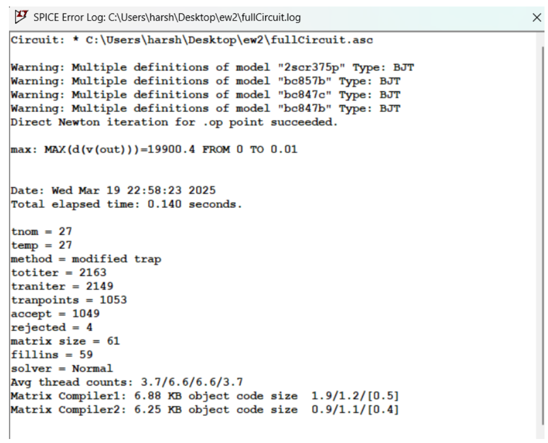
The **Total Harmonic Distortion (THD)** for the given data is approximately $\boxed{4.72\%}$.

This output is not distorted that much showing a good performance of the circuit.

B. Slew rate

Slew Rate is defined as the maximum change in output voltage divided by the change in time. S.R= max $\frac{\delta V_{out}}{\delta t}$

The maximum slew rate observed in simulation is the following:



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SPICE Error Log: C:\Users\harsh\Desktop\ew2\fullCircuit.log
Circuit: * C:\Users\harsh\Desktop\ew2\fullCircuit.asc

Warning: Multiple definitions of model "2scr375p" Type: BJT
Warning: Multiple definitions of model "bc857b" Type: BJT
Warning: Multiple definitions of model "bc847c" Type: BJT
Warning: Multiple definitions of model "bc847b" Type: BJT
Direct Newton iteration for .op point succeeded.

max: MAX(d(v(out)))=19900.4 FROM 0 TO 0.01


Date: Wed Mar 19 22:58:23 2025
Total elapsed time: 0.140 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2163
traniter = 2149
tranpoints = 1053
accept = 1049
rejected = 4
matrix size = 61
fillins = 59
solver = Normal
Avg thread counts: 3.7/6.6/6.6/3.7
Matrix Compiler1: 6.88 KB object code size  1.9/1.2/[0.5]
Matrix Compiler2: 6.25 KB object code size  0.9/1.1/[0.4]
```

Fig. 32. Slew rate

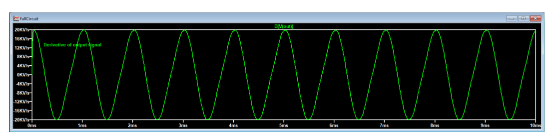

Fig. 33. Derivative of output

VIII. Other Parts

Since we were restricted to using only ± 12 V power supplies, we incorporated voltage regulator ICs to provide stable ± 5 V supplies to the differential amplifier, common emitter (CE) amplifier, and power amplifier circuits. For this purpose, we used the **LM7805** (for $+5$ V) and **LM7905** (for -5 V) voltage regulator ICs.

Additionally, we included a microphone circuit to convert audio signals into electrical signals. The microphone circuit produced an output signal in the range of **10–20 mV$_{\text{pp}}$** (millivolts peak-to-peak), which was then fed into the amplification stages for further processing.

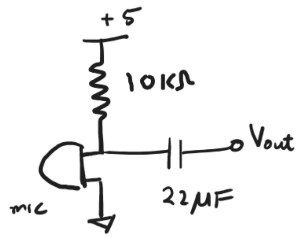

Fig. 34. Mic circuit used

A. Observations

B. Load Balancing

While each stage of the circuit might function perfectly in isolation with a specific set of component values, connecting multiple stages together can lead to **loading effects**. This occurs when one stage loads another, causing unexpected behavior in the output. To address this issue, there are two common approaches:

- Using buffers between stages to isolate them.
- Load balancing the stages by carefully selecting component values to minimize loading effects.

In our design, we opted for **load balancing** to ensure that each stage operates correctly when connected to the next, without the need for additional buffer circuits.

C. Frequency Response Considerations

Each stage in the circuit has its own **frequency response characteristics**. When these stages are cascaded, the overall frequency response of the system becomes the **product of the individual responses** of each stage. This can lead to an undesired frequency response for the entire system if not properly accounted for during the design phase.

While designing the audio amplifier, it is crucial to consider not only the frequency response of the filters but also the **high-frequency behavior of all components**, including transistors, capacitors, and resistors. This ensures that the amplifier performs as intended across the entire audible frequency range (20 Hz to 20 kHz).

D. Thermal Noise

Thermal noise is an inherent phenomenon in electronic circuits, caused by the random motion of electrons in conductive materials. This noise is present in all stages of the circuit and can affect the output signal. As a result, the **theoretical output** of the circuit may differ from the **actual output** due to the presence of thermal noise.

To mitigate the impact of thermal noise, careful design practices, such as proper grounding, shielding, and the use of low-noise components, are essential. However, it is important to note that some level of noise is unavoidable in practical circuits.

IX. Conclusion

A. Audio Amplifier Performance

We successfully built an audio amplifier with a **gain ratio of 434**, which was capable of driving the load effectively. This high gain ensures that even weak input signals, such as those from a microphone, are amplified to a level suitable for driving speakers or other output devices.

B. Bandpass Filter and Environmental Noise

The bandpass filter in our design has a **lower cutoff frequency of 20 Hz**, which falls within the audible range. However, environmental noise at **50 Hz** (e.g., mains hum) is also within the passband of the filter, allowing it to pass through the circuit. To address this issue, we could have adjusted the **lower cutoff frequency** to a slightly higher value (e.g., 40 Hz or 50 Hz) to attenuate the 50 Hz noise while still preserving the audible frequency range.

C. Improved Roll-Off with Higher-Order Filters

To achieve a **steeper roll-off** and better attenuation of unwanted frequencies, we could have used a **higher-order filter** (e.g., a second-order or fourth-order filter). Higher-order filters provide a sharper transition between the passband and stopband, ensuring that unnecessary frequencies are more effectively suppressed. This would have improved the overall performance of the amplifier by reducing interference from out-of-band signals.

D. Power Amplifier Considerations

While we used a **Class AB power amplifier** in our design, a **Class D power amplifier** could have been employed for better efficiency and performance. Class D amplifiers are known for their high efficiency, making them ideal for battery-powered or low-power applications. However, they typically consume more power during operation and require more complex circuitry, which could have increased the overall complexity and cost of the design.

E. Video Link

To check the video demonstration of the circuit use this link: CLICK HERE