QN8005/6/7B Hardware Application Note

April, 2010

REVISION HISTORY

Revision	Summary of Changes	Date
0.1	Draft.	2009-7-13
0.2	1. Update the grammar and syntax; 2. Add PA circuit for QN8006/7B; 3. Modify from 75 ohm to 5k ohm in Section 2.8	2009-12-7
0.3	Update reference design, add Tx/Rx antenna sharing	2010-4-2

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1 Overview

The QN8005/6/7B series are high performance, low power, full featured single-chip stereo FM receiver, transceiver and transmitter ICs designed for cell phones, MP3 players, and portable radios. The QN8005/6/7B also supports RDS/RBDS data reception and transmits.

1.1 Main Feature for QN8005/6/7B

- Support FM RX(QN8005/6), FM TX(QN8006/7)
- Support 2-wire, 3-wire control interface
- Support I^2S audio interface
- Crystal: MHz clocks, internal adjustable load capacitor, supports external clock injection
- RDS supported
- Interrupt supported
- Auto seek for RX
- Clear channel scan for TX
- Audio AGC

2 Hardware Design

Please refer to the Chapter 3 for the reference design schematics.

2.1 Power Supply

QN8005/6/7B has an integrated regulator, the VCC can accept the voltage range from 2.7 V ~ 5 V. Bypass capacitors are suggested to be placed near the VCC pin. The proposed values are 10uF, 1uF, 0.01uF.

The VIO pin is used to define the IO voltage which specifies the voltage limit for all digital pins. Its maximum voltage is to 3.6 V. And to keep the power supply clean, a 10pF Bypass capacitor is suggested.

	MAX	MIN
VCC	5.0V	2.7V
VIO	3.6V	1.6V

VIO supplies power to digital IO block, and also define the threshold of input (Vih and Vil), including CEN pin.

Once the VCC pin is connected to power supply, VIO should also be powered to assure QN8005/6/7B can enter power down mode with CEN=low MOD=low.

2.2 Control Interface

QN8005/6/7B has 5 control interface pins. The functions are shown in the following table.

Table 1: Function description for interface setting

CEN	MOD	SEB	Function description
'L'	'L'	X	Chip power off
'H'	'H'	X	Chip uses 3 wire interface
'H'	'L'	'L'	Chip uses 2-wire interface and the device address is '0101011
'H'	'L'	'H'	Chip uses 2-wire interface and the device address is the value in register R02, which the default value is '0101010
NOTE: 'H' means high voltage defined by VIO pin; 'L' means low voltage defined by VIO pin.			

The SEB pin is used as bus enable signal in 3-wire mode and will be used as 2-wire device address select signal in 2-wire mode.

SDA pin is the data bus and SCL pin is the clock bus. Pull up resistors are required on these two bus lines and the resistor values should be set according to the 2-wire rate.

2.3 Interrupt Interface

QN8005/6/7B uses pin 14(DOUT)/ pin 20(DIN) as an interrupt signal output. They are shared with I^2S interface. In FMR mode, pin 20(DIN) will be used as the interrupt pin. In FMT mode, pin 14(DOUT) will be used as the interrupt pin.

When the chip functions “clear channel scan”, “auto seek”, and RDS have received or sent out a group data, this pin 14(DOUT)/ pin 20(DIN) will generate an interrupt signal. In normal mode this pin will output a high voltage. When the function is finished, this pin will send out a low voltage for 4.5ms.

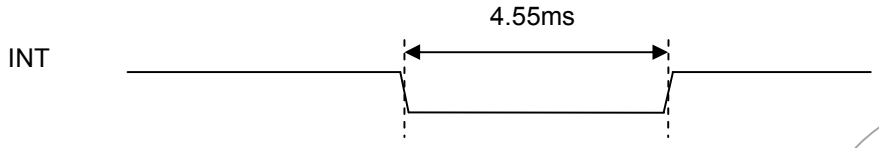

Figure 1. Interrupt Timing

2.4 Clock Interface

Pin 18 “XTAL2”, pin 17 “XTAL1” and pin 16 “XCLK” are used as input clock signals. QN8005/6/7B can accept a crystal or an external clock source. The accepted frequency range is in MHz. Please refer to the QN8005/6/7B datasheets for more information.

In the crystal mode, the load capacitors have been integrated in the chip, and the capacitor range is 10p ~ 30pF with the default setting at 20pF. Therefore, the crystal can connect to the chip directly without external load capacitors.

In the external clock mode, the clock interface (pin16) can be set to IO mode to accept an external clock.

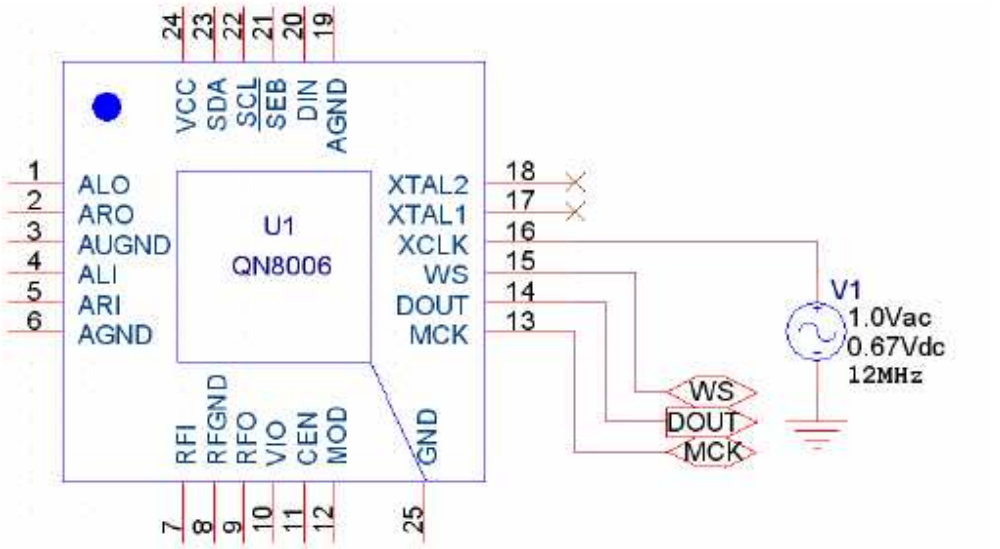

Figure2. External Clock Connection

If the external clock is a square ware and the voltage range is between 0 to VCC, the clock can connect to XCLK pin directly. If the external clock is sine wave, the clock requires a DC offset when it connects to the XCLK pin.

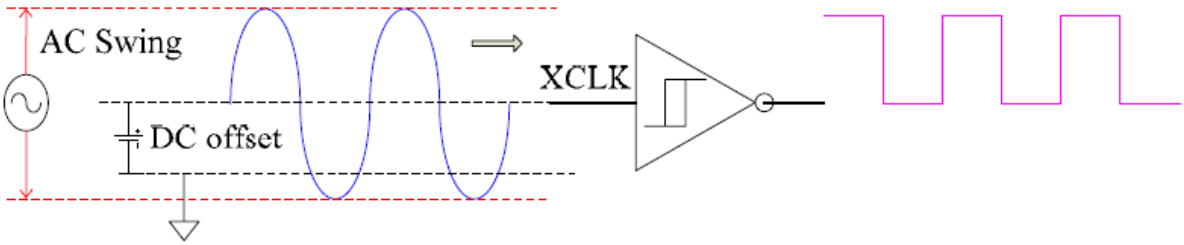

Figure 3. Working Principle of External Clock

For the external clock to work the peak-peak voltage swing of the clock should be equal to VCC and the DC offset should be half of VCC. For example, if the chip power supply is 3V, the external clock should have a 3V peak-peak voltage swing and the DC offset should be about 1.5V.

2.5 Audio Output Interface

QN8005/6/7B can't drive a 16ohm load directly. If the system needs to drive a 16ohm or 32ohm load, an external audio driver is necessary.

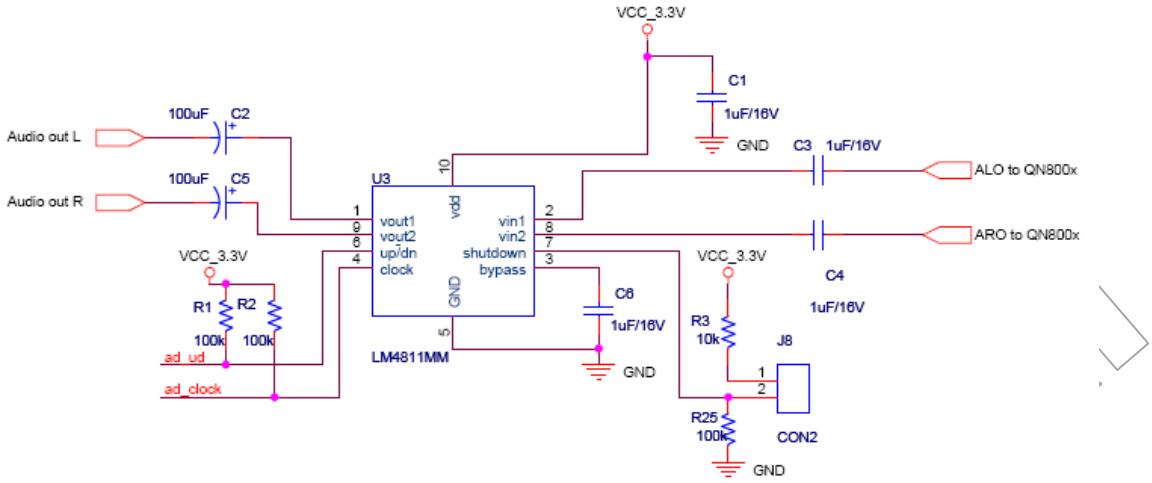

Figure 4. External Audio Driver Circuit

2.6 Audio Input Interface

The QN8005/6/7B includes an integrated VGA for FMT audio input. The chip default setting allows the maximum input voltage to be about 500mV peak.

To reject common-mode noise, such as TDMA noise, an external differential audio input circuit may be added.

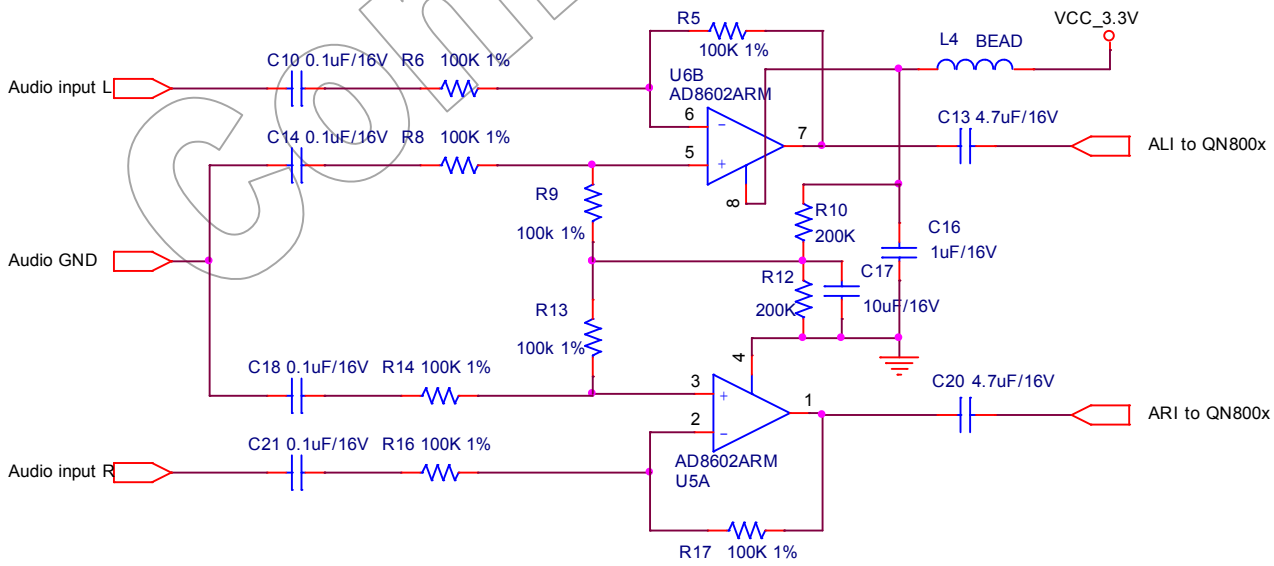

Figure 5. External Audio Input Circuit

2.7 I²S Interface

The I²S interface has four pins: MCK, WS, DOUT, and DIN. On the QN8005/6/7B, pins DOUT, DIN have been shared with interrupt interface. When in the FMR mode, I²S will use the pins MCK, WS and DOUT, and the pin DIN will be used as interrupt output. When in the FMT mode, I²S will use MCK, WS and DIN pins, and pin DOUT will be used as interrupt output.

2.8 FM Receiver Antenna Interface

The QN8005/6/7B LNA has two impedance modes. The default setting of the impedance is about 5k ohm. In this case, the following matching network is suggested.

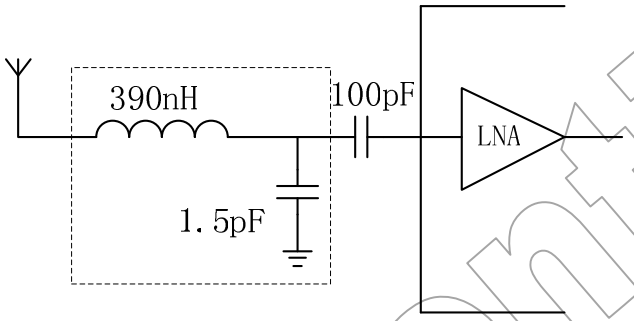

Figure 6. Matching Network for LNA High Impedance Setting

The LNA input is not DC coupled so a 100pF capacitor is required to block the DC voltage.

When using the long line of the headphone as the receiver antenna, it's necessary to include ferrite beads or large inductors on the audio traces and audio ground, in order to avoid RF signal leakage from these traces.

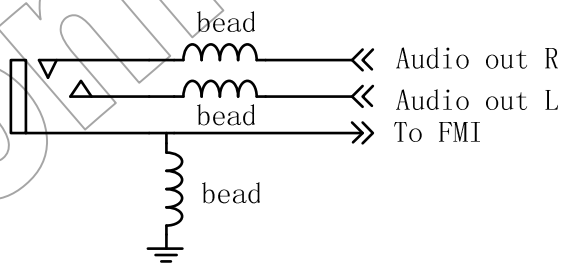

Figure 7. Circuit for Using Headphone Line as Receiver Antenna

2.9 FM Transmitter Antenna Interface

The PA structure of QN8005/6/7B requires an external inductor to resonate with the integrated capacitor and to provide a DC return for the PA output.

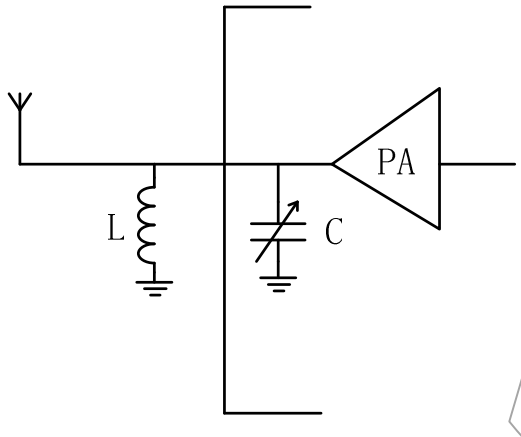

Figure 8. PA output Circuit

The inductor should be assembled as close as possible to the chip.

The integrated capacitor is adjustable and according to the equation $f = \frac{1}{2\pi\sqrt{LC}}$.

In order to cover the frequency range from 76MHz ~ 108MHz, a 100nH inductor is suggested. The inductor value may be adjusted to compensate for the additional capacitance which results from the board layout and the antenna type.

2.10 Power Amplifier Circuit for QN8006/7B

QN8006/7B has an integrated power amplifier. If the output power still can't meet the requirement, it can add an external power amplifier outside of RFO pin.

The circuit is shown in following:

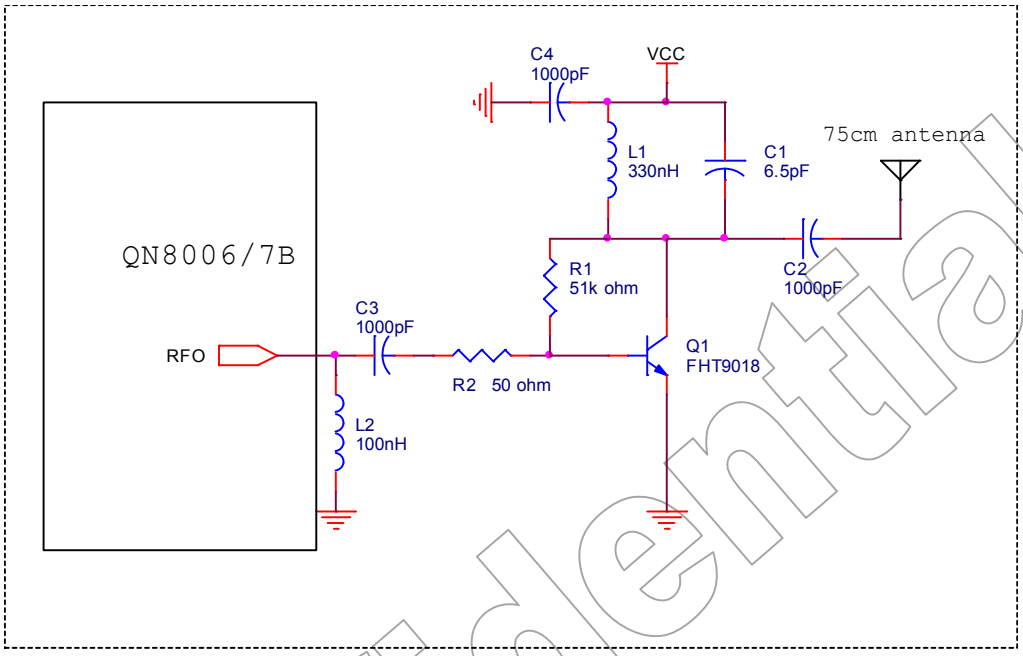

Figure 9. External PA Reference Circuit for 75cm Antenna

***Note:** *In the figure, RFO connects to QN8006/7B pin 9 directly.*

The reference circuit is designed based on QN8006/7B EVB, and with the PA circuit, RF output power increases about 15dB. When the circuit is used on practical product, the parameters of the components need to modify according to the layout of the FM transmitter output trace.

2.11 QN8005/6/7 A1 to B1 Transform

When changing the design from QN8005/6/7 A1 to QN8005/6/7 B1, the pins definition and application also need to be done the corresponding changes. The detailed information please refer to the document “QN800x Rev A1 to B1 Application Note_V0 3_051109.pdf”.

3 Schematic of QN8005B Reference Design

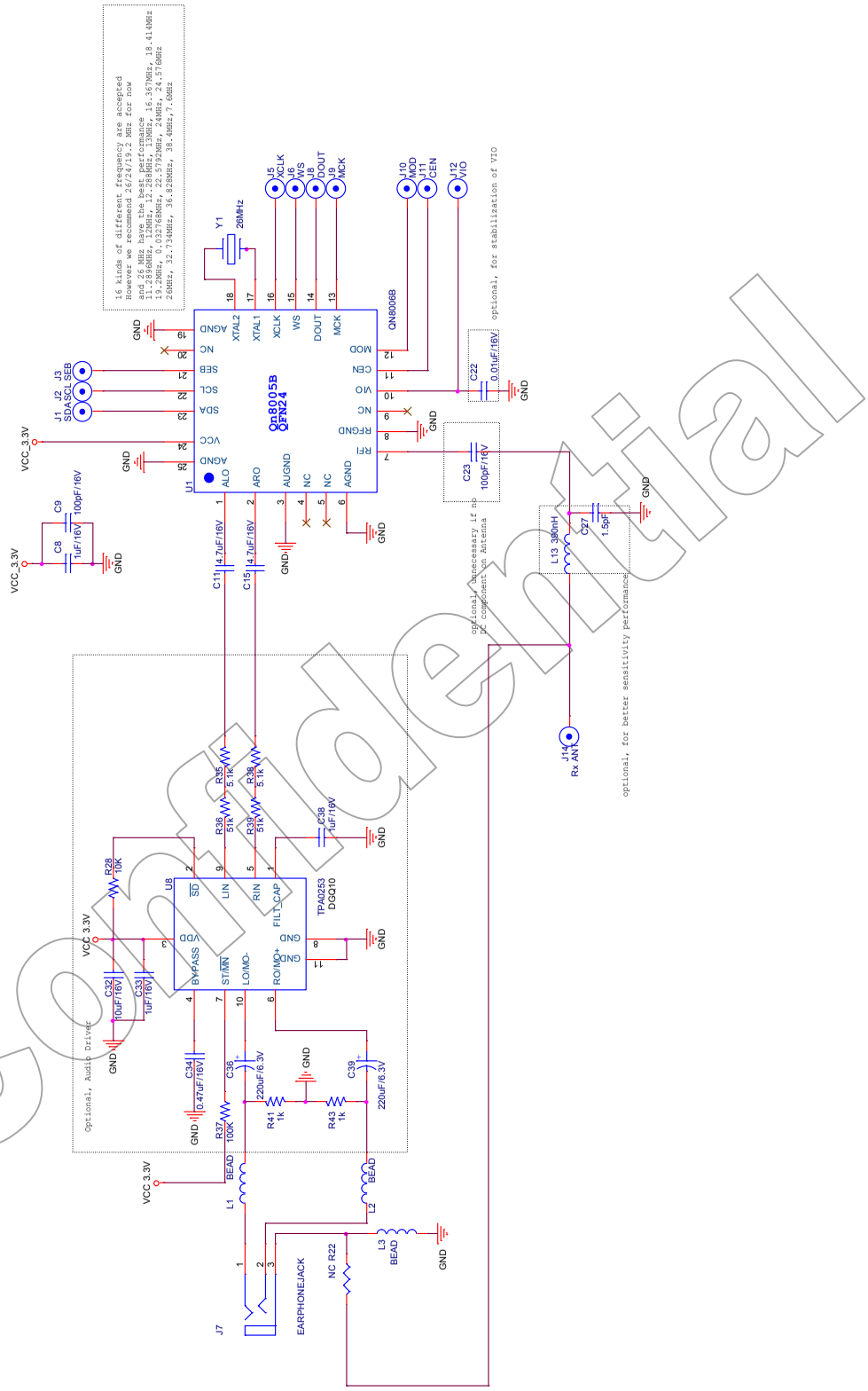

Figure 10. Schematic of QN8005B Reference Design

4 Schematic of QN8006B Reference Design with two antenna

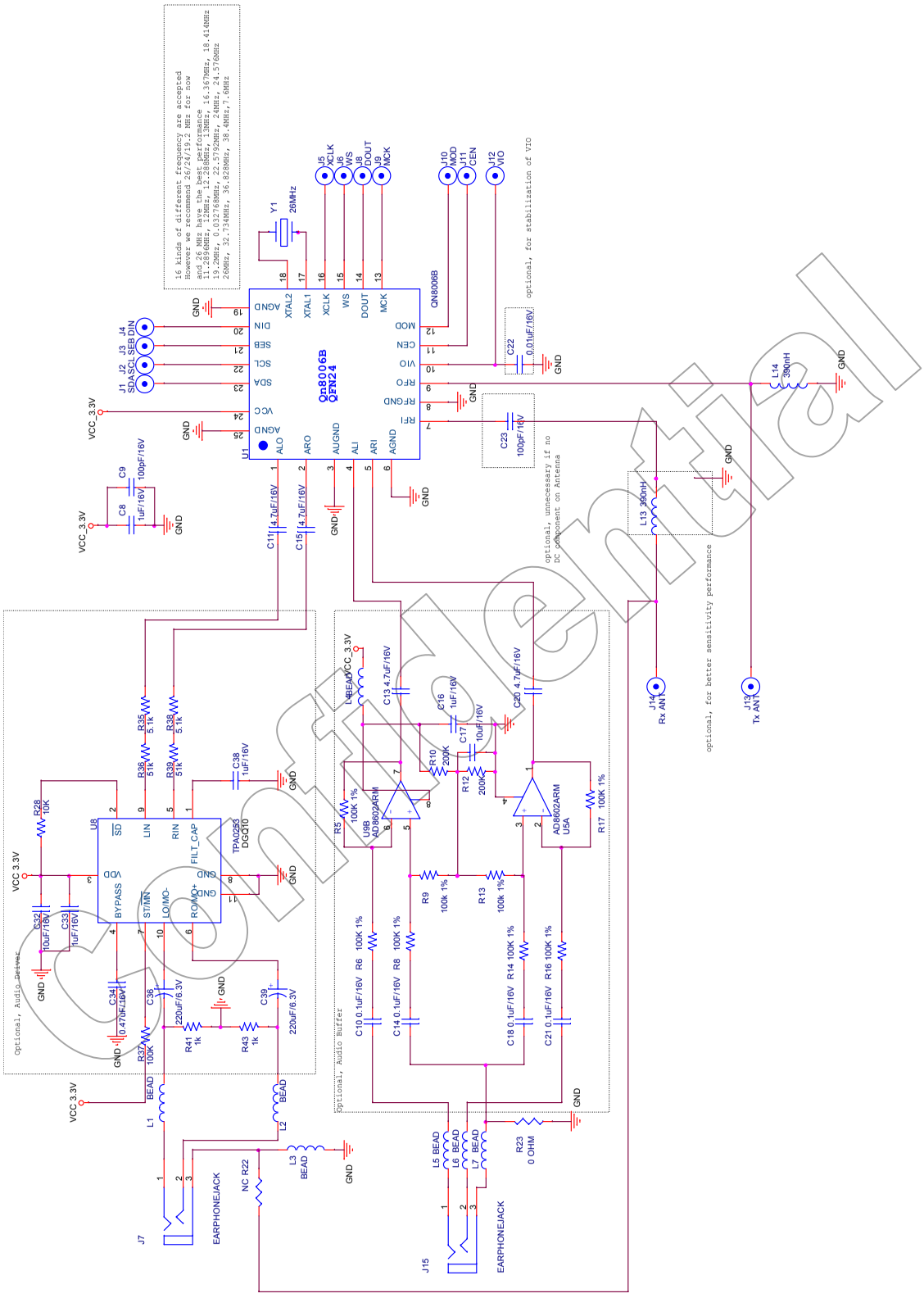

Figure 11. Schematic of QN8006B Reference Design with two antenna

5 Schematic of QN8006B Reference Design with one antenna

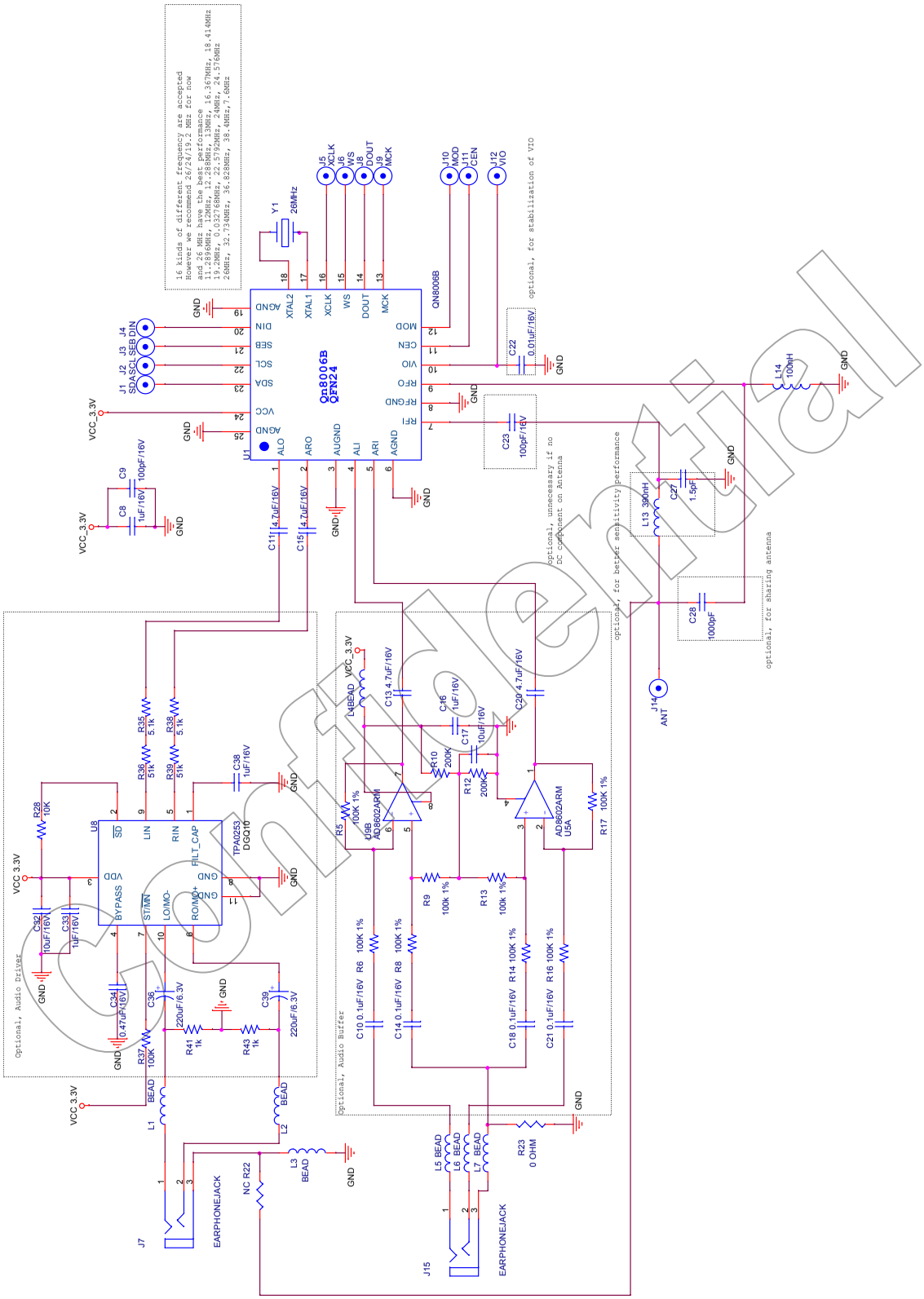

Figure 12. Schematic of QN8006B Reference Design with one antenna

6 Schematic of QN8007B Reference Design

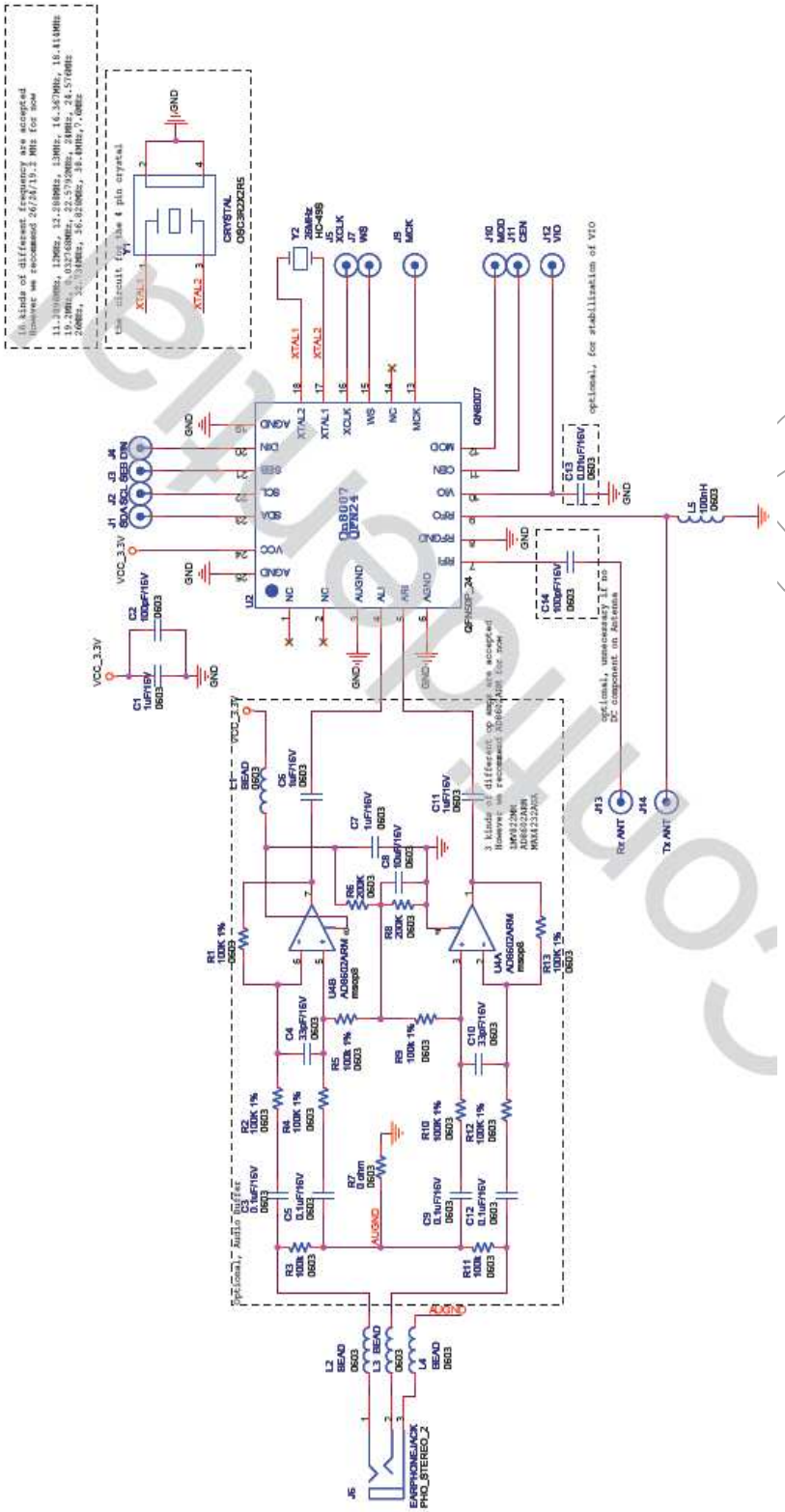

Figure 13. Schematic of QN8007B Reference Design

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