Zero-Voltage-Switching Interleaved Two-Switch Forward Converter with Phase-Shift Control

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***Abstract* -- In this paper, a zero-voltage switching (ZVS) interleaved two-switch forward (ITSF) converter employing a phase-shift control is proposed. Since the proposed converter is based on a two-switch forward (TSF) topology, it has no chance to be a short circuit causing device failure. Furthermore, the interleaving operation of two TSF converters reduces the output filter size. In addition, by applying the phase-shift control on the common clamping diode structure at the primary side, all primary switches can be turned on under ZVS conditions. The operational principle, theoretical analysis, and design consideration are presented. To confirm the performance of the proposed circuit, experimental results from a 480 W, 100 kHz, and 400 V to 48 V prototype are presented.**

***Index Terms*—Interleaved two-switch forward converter, phase-shift control, zero-voltage-switching.**

I. INTRODUCTION

In telecom and server power systems, a distributed power system (DPS) is widely used since it has many advantages such as standardization, reliability, and efficiency [1], [2]. The isolated dc-dc stage of the DPS converts the high voltage dc bus about 400V into the tightly regulated low voltage dc bus such as 48V and 12V [3]. In most cases, topologies for the isolated dc-dc stage are restricted by the high input voltage. A half-bridge, full-bridge, and two-switch forward (TSF) converters are suitable candidates for the isolated dc-dc stage since their voltage stress on the primary switches can be clamped at the input voltage level. Although the half-bridge and full-bridge have advantage of soft switching capability [4]-[7], they have low reliability because the primary switches are connected in totem pole structure. Once two switches are turned on at the same time due to noise or radiation, destructive device failure will be occurred.

Compared with the half-bridge and full-bridge, the TSF converter has no destructive device failure problem since the primary switches are not connected in totem pole structure. However, it has disadvantages such as hard-switching and large output filter size for the price of the high reliability. The output filter size can be reduced by the interleaving operation of two TSF converters. However, it still suffers from hard-switching.

The TSF converter presented in [8] can operate under zero-voltage-switching (ZVS) conditions. However, the authors consider the operation only under a fixed input voltage and do not describe the control method to achieve ZVS under the wide input-voltage range caused by hold up time requirement. In addition, since the circuit has no output filter inductor, it has a non-linear voltage conversion ratio. Due to the non-linear voltage conversion ratio, the circuit has small duty cycle at the nominal input voltage of 400V. The small duty cycle will cause increased current ripples and conduction losses [9]. Therefore, this converter is not suitable for the isolated dc-dc stage of the DPS which has the wide input-voltage range and high-current output.

In this paper, a ZVS interleaved two-switch forward (ITSF) converter well-suited to the isolated dc-dc stage of the DPS is proposed. The proposed converter reduces the output filter size by the interleaving scheme. Moreover, by employing the phase-shift control on the common clamping diode structure at the primary side, ZVS can be achieved for the wide input-voltage variation. Therefore, the proposed converter can effectively overcome above-mentioned problems and provide high reliability and efficiency.

II. PROPOSED CONVERTER

A. Features of the Proposed Converter

The circuit diagram of the proposed converter is shown in Fig. 1. The circuit consists of the two transformers (T_1 and T_2), four primary switches (Q_1~Q_4), two clamping diodes (D_{p1} and D_{p2}), two rectifier diodes (D_{s1} and D_{s2}), output filter inductor (L_o), and output filter capacitor (C_o). The features of the proposed circuit are summarized as follows:

1) Low voltage stress on the switches: The voltage stress on the primary switches can be clamped at the input voltage level because it is based on the TSF topology.

2) High reliability: Since the primary switches are not connected in totem pole structure, it has no destructive device failure problem.

3) Reduced output filter size: Due to the interleaving operation of the two TSF converters, the output filter size can be reduced.

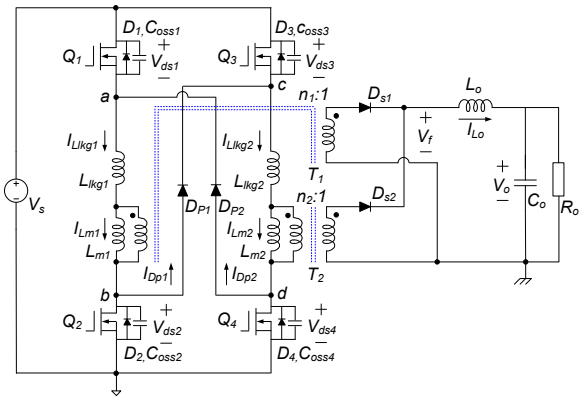


Fig. 1. Circuit diagram of the proposed converter

4) Soft switching by the phase-shift control: By adjusting effective duty ratio with the phase-shift control according to the input voltage variation, the proposed converter not only regulates the output voltage but also achieves ZVS.

5) Reduced number of the clamping diodes: The common clamping diode structure at the primary side to achieve ZVS also reduces the number of clamping diodes.

B. Operation Principles

Fig. 2 shows switching sequences and key waveforms of the proposed converter in the steady-state. Q_1 (Q_2) and Q_4 (Q_3) are switched in a complementary fashion with 50% duty ratio. To regulate the output voltage, Q_2 (Q_3) is turned on after Q_1 (Q_4) is turned on with the phase difference ΦT_s. For the analytic purpose several assumptions are made as follows:

- The two transformers (T_1 and T_2) are identical ($L_{m1} = L_{m2}$, $L_{lkg1} = L_{lkg2}$, and $n_1 = n_2 = n$).
- The primary switches (Q_1~Q_4) are ideal except for the internal diodes (D_1~D_4) and output capacitances (C_{oss1}~$C_{oss4} = C_{oss}$).
- The primary clamping diodes (D_{p1} and D_{p2}) and secondary rectifier diodes (D_{s1} and D_{s2}) are ideal.
- The magnetizing current (I_{Lm1} and I_{Lm2}) and filter inductor current (I_{Lo}) are considered as constant current sources in switching transition durations.
- The output voltage (V_o) is constant.
- All parasitic components except those specified in Fig. 1 are neglected.

One switching period is divided into the two half periods (t_0~t_4 and t_4~t_8). Since the operation of each half period is symmetric, only the operation of the first half period is explained. Topological equivalent circuits are shown in Fig. 3.

Mode 1 (t_0~t_1): Before t_0, Q_1 and Q_2 are turned on. When the commutation of D_{s1} and D_{s2} is completed at t_0, mode 1 begins. T_1 transfers the input power to the output side through Q_1, Q_2, D_{s1}, and L_o. Since V_s and $V_s/n_1 - V_o$ are applied to L_{m1} and L_o respectively, I_{Lm1} and I_{Lo} increase. I_{Llkg1} which

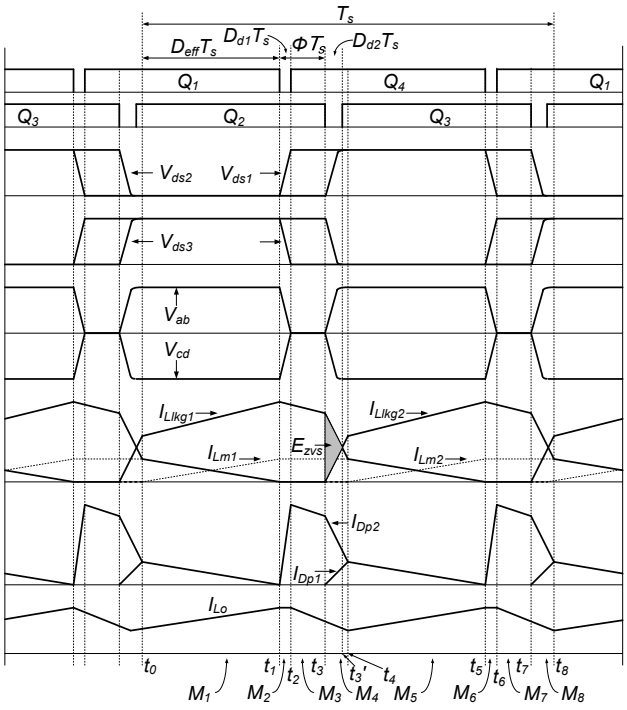


Fig. 2. Key waveforms of the proposed converter

comprises I_{Lm1} and I_{Lo}/n_1 also increases. At the same time, T_2 is reset by the applied negative voltage through D_{p1} and D_{p2}. Therefore, I_{Lm1}, I_{Lm2}, I_{Lo}, and I_{Llkg1} are expressed as follows:

$$I_{Lm1}(t) = \frac{V_s}{L_{m1}}(t - t_0) \tag{1}$$

$$I_{Lm2}(t) = I_{Lm2}(t_0) - \frac{V_s}{L_{m2}}(t - t_0) \tag{2}$$

$$I_{Lo}(t) = I_{Lo}(t_0) + \left(\frac{V_s / n_1 - V_o}{L_o}\right)(t - t_0) \tag{3}$$

$$I_{Llkg1}(t) = \frac{V_s}{L_{m1}}(t - t_0) + \frac{\left(I_{Lo}(t_0) + \left(\frac{V_s / n_1 - V_o}{L_o}\right)(t - t_0)\right)}{n_1}. \tag{4}$$

Mode 2 (t_1~t_2): After Q_1 is turned off at t_1, I_{Llkg1} which can be considered as the constant current source discharges C_{oss4} and charges C_{oss1}. Provided that the effect of L_{lkg1} is small enough, V_{ds1} is increased and V_{ds4} is decreased linearly. Therefore, V_{ds1}, V_{ds2}, and V_f are calculated as follows:

$$V_{ds1}(t) = \frac{I_{Llkg1}(t_1)}{2 \cdot C_{oss}}(t - t_1) \tag{5}$$

$$V_{ds4}(t) = V_s - \frac{I_{Llkg1}(t_1)}{2 \cdot C_{oss}}(t - t_1) \tag{6}$$

$$V_f(t) = \frac{V_s - \frac{I_{Llkg1}(t_1)}{2 \cdot C_{oss}}(t - t_1)}{n_1}. \tag{7}$$

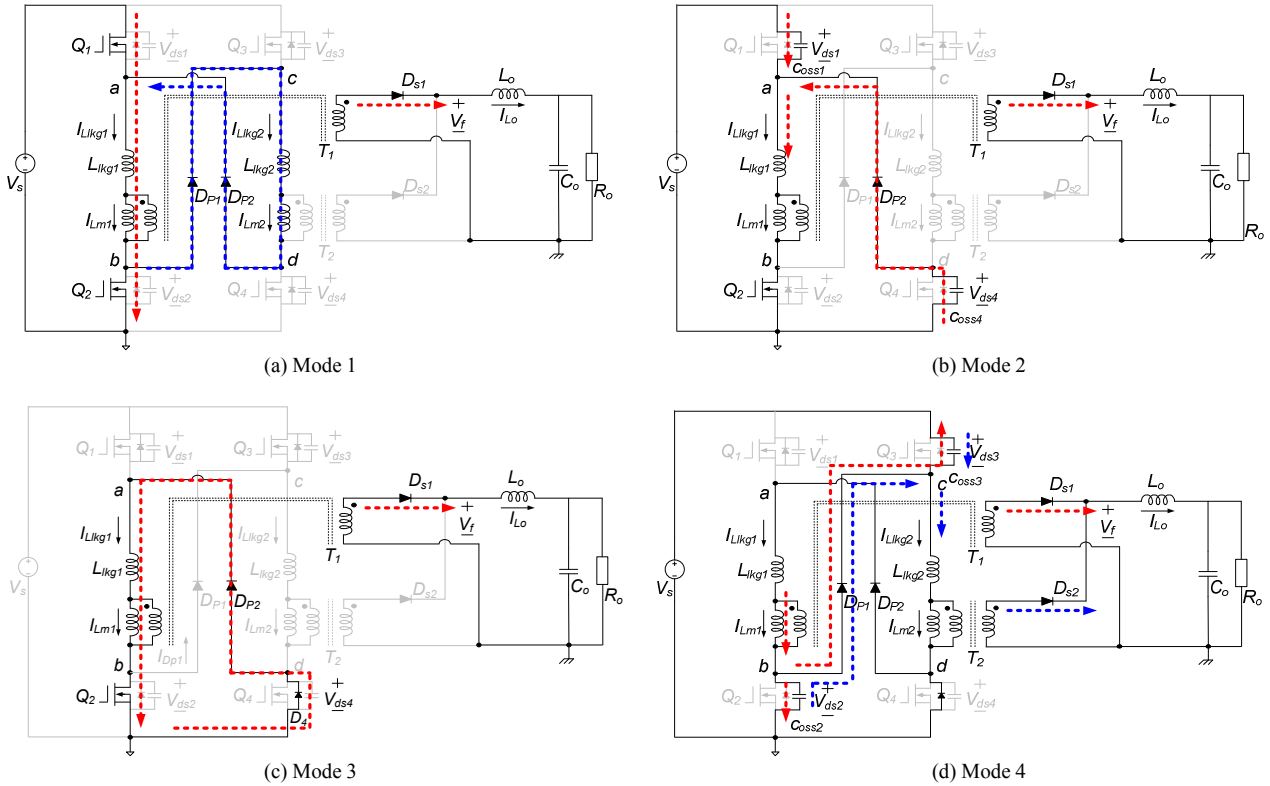


Fig. 3. Topological equivalent circuits of the proposed converter

Mode 2 ends when V_{ds4} becomes zero.

Mode 3 (t_2~t_3): D_4 starts conducting when V_{ds4} becomes zero. I_{Llkg1} is freewheeling through D_{p2}, Q_2, and D_4. After D_4 begins to conduct, Q_4 can be turned on under a ZVS condition. Since the ZVS of Q_4 is accomplished by the large primary current which comprises the magnetizing current and the reflected filter inductor current ($I_{Lm1} + I_{Lo}/ n_1$), it is easy to achieve ZVS. I_{Lm1}, I_{Llkg1}, and I_{Lo} are obtained as follows:

$$I_{Lm1}(t) = I_{Lm1}(t_2) \tag{8}$$

$$I_{Lo} = I_{Lo}(t_2) + \frac{-V_o}{L_o}(t - t_2) \tag{9}$$

$$I_{Llkg1}(t) = I_{Lm1}(t_2) + \frac{\left(I_{Lo}(t_2) - \frac{V_o}{L_o}(t - t_2)\right)}{n_1}. \tag{10}$$

Mode 4 (t_3~t_4): After Q_2 is turned off at t_3, I_{Llkg1} will continue to flow and begin to discharge C_{oss3} and charge C_{oss2} in a sinusoidal fashion. If the energy stored in the leakage inductor is large enough V_{ds3} will resonate down to zero and V_{ds2} will resonate up to V_s. Switching Q_3 at the precise moment when V_{ds3} is zero is called ZVS. When the commutation of D_{s1} and D_{s2} is completed at t_4, mode 4 ends and the other half cycle will be begun.

III. Analysis and Design of the Proposed Converter

A. Voltage Conversion Ratio

To calculate the voltage conversion ratio, the dead time between Q_1 and Q_4, as well as Q_2 and Q_3, and the effect of the leakage inductor are neglected. From the voltage-second balance across L_o, the voltage conversion ratio can be obtained as

$$\frac{V_o}{V_s} \simeq \frac{2}{n} \cdot D_{eff}. \tag{11}$$

B. Transformer Turn Ratio

To regulate the output voltage under the wide input-voltage range, the highest dc voltage gain needs to be designed at the minimum input voltage ($V_{s,min}$). The maximum available duty cycle ($D_{eff,max}$) is less than 0.5 because of the duty cycle loss by the leakage inductance. Therefore, the transformer turn ratio to guarantee the output voltage under the minimum input voltage can be calculated as follow:

$$\frac{1}{n} = \frac{1}{2} \cdot \frac{V_o}{V_{s,min}} \cdot \frac{1}{D_{eff,max}}. \tag{12}$$

From (11) and (12) the effective duty ratio in a normal condition can be obtained. Compared with the converters

which have non-linear voltage conversion ratios, the proposed converter has larger effective duty cycle in the normal condition since it has a linear voltage conversion ratio.

C. Output Filter Inductor

The worst case ripple current occurs at minimum effective duty cycle and maximum output power. Thus, output filter inductance can be calculated as follow:

$$L_o = \frac{(0.5 - D_{eff}) \cdot V_o}{\Delta I_{Lo} \cdot f_s}. \quad (13)$$

Due to the frequency doubling effect by the interleaving operation, the proposed converter can reduce the output filter inductor size.

D. ZVS Conditions

The ZVS of Q_1 and Q_4 is achieved by the transformer primary current which comprises the magnetizing current and the reflected filter inductor current. At t_1 when Q_1 is turned off, the value of the transformer primary current has its maximum value. From (4), This value ($I_{Llkg1,max}$) can be calculated as

$$I_{Llkg1,max} = \frac{V_s \cdot D_{eff}}{L_{m1} \cdot f_s} + \frac{1}{n} \cdot \left(I_o + \frac{(0.5 - D_{eff}) \cdot V_o}{2 \cdot L_o \cdot f_s} \right). \quad (14)$$

where I_o is average load current.

If the effect of the leakage inductance is small enough, C_{oss1} is charged and C_{oss4} is discharged linearly by $I_{Llkg1,max}$. Thus, the dead time ($D_{d1}T_s$) to achieve the ZVS of Q_1 and Q_4 is obtained as follow:

$$D_{d1}T_s = \frac{2 \cdot C_{oss} \cdot V_s}{I_{Llkg1,max}}. \quad (15)$$

It is easy to achieve the ZVS of $Q_1$and Q_4 even at the light load because the ZVS is accomplished by the large reflective filter inductor current.

On the other hand, the ZVS of Q_2 and Q_3 is achieved by the energy stored in the leakage inductor. Assume that the filter inductor current is constant in switching transition durations the primary current at t_3 ($I_{Llkg,t3}$) can be obtained from (10) as

$$I_{Llkg1,t3} = \frac{V_s \cdot D_{eff}}{L_{m1} \cdot f_s} + \frac{1}{n} \cdot \left(I_o - \frac{(0.5 - D_{eff}) \cdot V_o}{2 \cdot L_o \cdot f_s} \right). \quad (16)$$

After Q_2 is turned off, I_{Llkg1} decreases from $I_{Llkg1,t3}$ to I_{Lm1}. I_{Llkg2} increases from zero to the reflected filter inductor current (I_{Lo}/n). C_{oss2} is charged and C_{oss3} is discharged by the difference between I_{Llkg1} and I_{Llkg2}. At t_3'I_{Llkg1} and I_{Llkg2} have the same value ($I_{Llkg,t3}/2$). From t_3' to t_4, since I_{Llkg2} is larger than I_{Llkg1}, C_{oss2} is discharged and C_{oss3} is charged. Thus, to achieve ZVS, Q_3 must be turned on at t3'. Therefore, the dead time ($D_{d2}T_s$) to achieve the ZVS of Q_2 and Q_3 is obtained as follow:

$$D_{d2}T_s = \frac{L_{lkg1} \cdot I_{Llkg1,t3}}{2 \cdot V_s}. \quad (17)$$

The energy available for charging C_{oss2} and discharging C_{oss3} (E_{zvs}) is shown in Fig. 2 as the shaded area and calculated as follow:

$$E_{zvs} = \frac{1}{4} L_{lkg1} \cdot I_{Llkg,t3}^2. \quad (18)$$

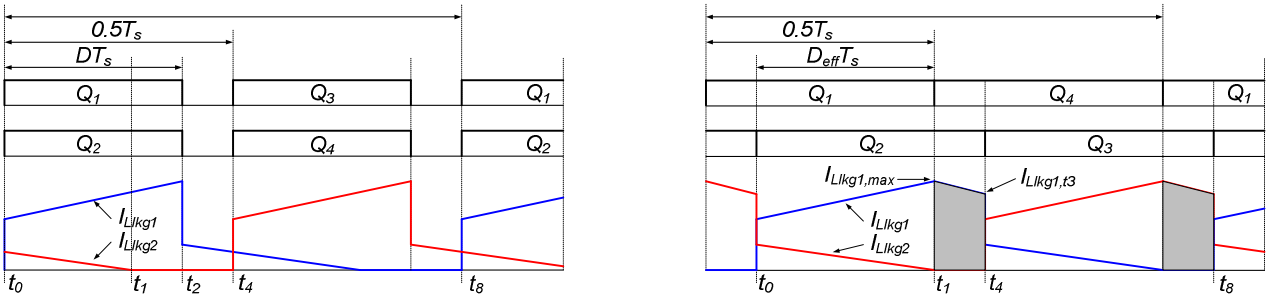
Therefore, ZVS conditions of Q_2 and Q_3 are obtained as follow:

$$\frac{1}{4} L_{lkg} \cdot I_{Llkg,t3}^2 \geq \frac{1}{2} (C_{oss2} + C_{oss3}) \cdot V_s^2. \quad (19)$$

As shown in (19), it is hard to achieve the ZVS of Q_2 and Q_3 at the light load.

E. Comparisons with the Conventional Hard-Switching Interleaved Two-Switch Forward Converter

The simplified primary current waveforms of the proposed converter and the conventional hard-switching ITSF converter are compared as shown in Fig. 4. In the conventional circuit, when the primary current becomes zero at t_1, resonance between the magnetizing inductance and output capacitance begins and the drain-to-source voltage becomes $V_s/2$. Thus, the switching losses (Q_{swloss}) of the conventional circuit can be calculated as



(a) Conventional hard-switching interleaved TSF converter

(b) Proposed converter

Fig. 4. Comparison of simplified primary current waveforms

$$Q_{swloss} = 4 \cdot \left(\frac{1}{2} C_{oss} \cdot \left(\frac{V_s}{2} \right)^2 \right) \cdot f_s + 4 \cdot \left(\langle V_{ds} \rangle \cdot \langle I_{sw} \rangle \cdot t_{on} \right) \cdot f_s \quad (20)$$

where $<V_{ds}>$ and $<I_{sw}>$ are average voltage and current of switches respectively during the switching transition interval, t_{on} is turn-on time which comprises turn-on delay time and turn-on rise time. Due to the switching losses, high frequency operation of the conventional circuit is limited.

The proposed converter has the freewheeling interval to achieve ZVS. Due to this freewheeling interval, the proposed converter has rather larger conduction losses. However, this is not so serious problem in high input-voltage and low input-current applications such as server and telecom power systems. Increased conduction losses are shown in Fig. 7 (b) as shaded area and can be calculated as follows:

$$D_{p\_cond} = 2 \cdot \left(V_{Dp,\,fwd} \cdot 0.5 \cdot \left(I_{Llkg\,1,max} + I_{Llkg\,1,t3} \right) \cdot \left(0.5 - D_{eff} \right) \right) \quad (21)$$

$$Q_{1\_cond} = 2 \cdot \left(V_{Q,\,body} \cdot 0.5 \cdot \left(I_{Llkg\,1,max} + I_{Llkg\,1,t3} \right) \cdot \left(0.5 - D_{eff} \right) \right) \quad (22)$$

$$Q_{2\_cond} = 2 \cdot R_{ds\_on} \cdot \left(0.5 - D_{eff} \right) \times \left(I_{Llkg,max}^2 + I_{Llkg,max} \cdot I_{Llkg\,1,t3} + I_{Llkg\,1,t3}^2 \right) / 3 \quad (23)$$

where D_{p_cond} is increased conduction losses of the clamping diode, Q_{1_cond} is increased conduction losses of Q_1 and Q_4, Q_{2_cond} is increased conduction losses of Q_2 and Q_3, $V_{Dp,fwd}$ is forward voltage drop of the clamping diode, $V_{Q,body}$ is anti-parallel diode voltage drop of the primary switches, R_{ds_on} is on resistance of the primary switches. The proposed converter can operate in high frequency due to the soft-switching capability. Thus, the size of the proposed converter can be reduced. Furthermore, as the switching frequency increases, reduced switching losses by ZVS are larger than increased conduction losses due to the freewheeling interval. Therefore, efficiency can be improved.

IV. Experimental Results

To verify the proposed converter, a prototype was built with following specifications: input voltage = 320V~400V, output voltage = 48V, rated power = 480W, switching frequency = 100kHz, ZVS range = from full load to half load, Q_1~Q_4 = FCP7N60, D_{p1} and D_{p2} = RURP860, D_{s1} and D_{s2} = 60CPQ150, L_o = 40uH, C_o = 330uF, L_{lkg1} and L_{lkg2} = 45uH, L_{m1} and L_{m2} = 2mH, n_1:1 and n_2:1 = 6:1 (60:10). Fig. 5 shows the key waveforms for the nominal input voltage of 400V and full load. It can be seen that all waveforms agree well with the theoretical analysis.

Fig. 6 shows the gate-to-source and drain-to-source voltages of Q_1 (Q_4) and Q_2 (Q_3) at different load conditions. The ZVS of Q_1 (Q_4) is easily achieved by the large reflected filter inductor current over load range from 10% to 100%. On the other hand, as the load current is decreased, the ZVS of Q_2 (Q_3) cannot be obtained. It can be seen that the ZVS of Q_2 (Q_3) is achieved from full load to half load conditions as defined in the specification.

In Fig. 7, the efficiencies of the proposed converter and the conventional hard-switching ITSF converter are compared according to the load variation. The efficiency of the proposed converter, through all load range, is improved about 0.5%~1% over the conventional hard-switching ITSF converter. This is because reduced switching losses by the ZVS are larger than increased conduction losses due to the freewheeling interval.

V. Conclusion

This paper proposes a ZVS ITSF converter employing the phase-shift control. Since the proposed converter is based on the TSF topology, it has high reliability. Moreover, the output filter size can be reduced by adopting interleaving scheme. In addition, by employing the phase-shift control on the common clamping diode structure at the primary side, all switches can be turned on under ZVS conditions. The efficiency of the proposed converter, through all load ranges, is improved about 0.5%~1% over the conventional hard-switching ITSF converter. Therefore, the proposed converter can be a strong candidate for the isolated dc-dc stage of the DPS which requires high reliability and efficiency.

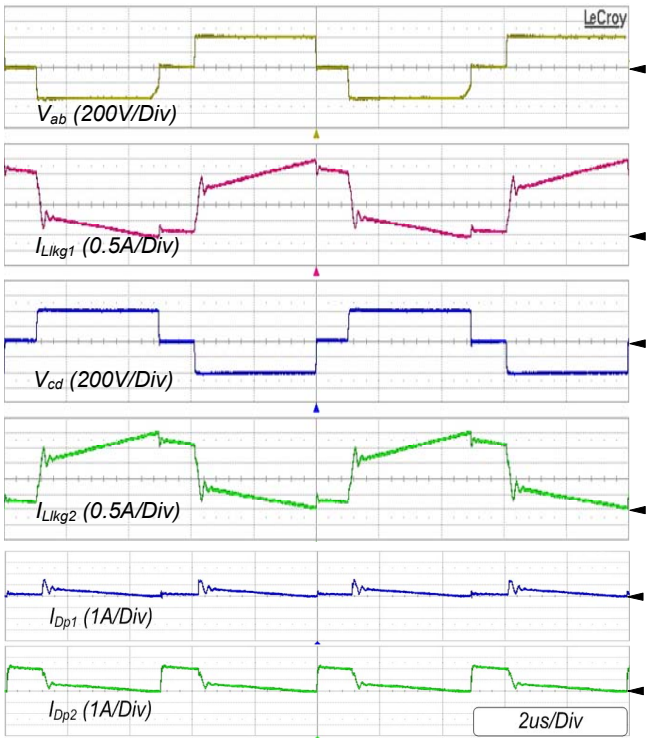
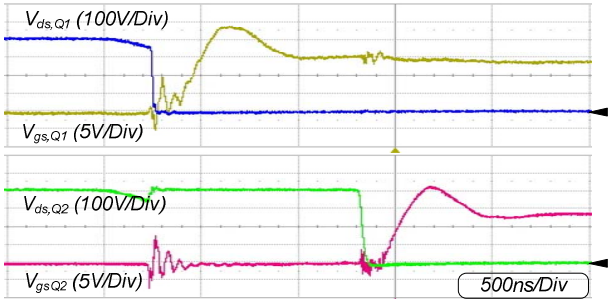
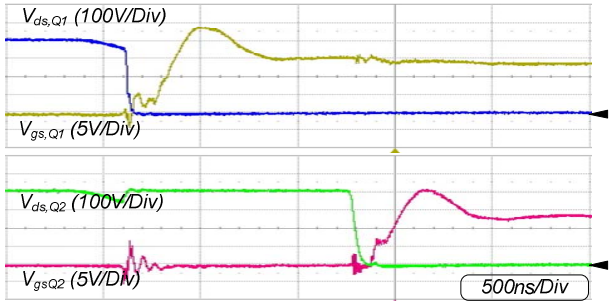


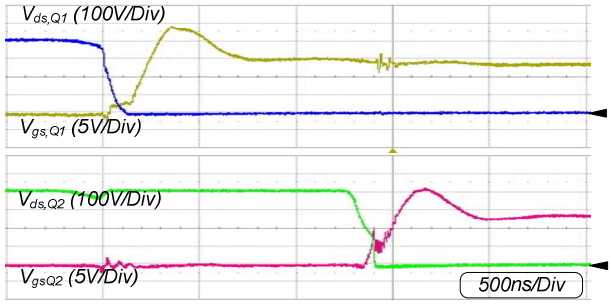
Fig. 5. Key waveforms



(a) Full load



(b) Half load



(c) 10% load

Fig. 6. ZVS waveforms

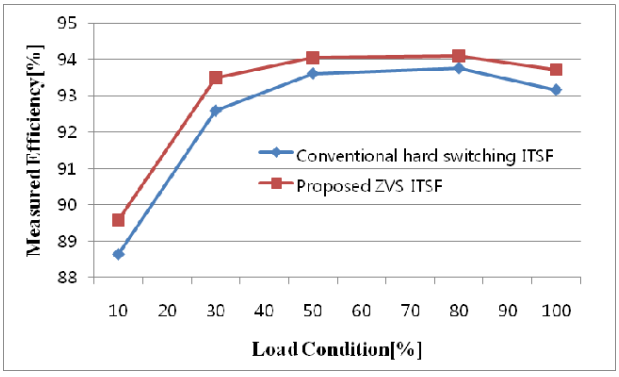


Fig. 7. Measured efficiency

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