

## N-Channel Enhancement-Mode MOSFET

Designed for handheld two-way radio applications with frequencies from 136 to 941 MHz. The high gain, ruggedness and Broadband performance of this device make it ideal for large-signal, common-source amplifier applications in handheld radio equipment.

**136–941 MHz, 0.15W, 3.7 V  
BROADBAND RF POWER  
TRANSISTOR**

### Typical Broadband EVB Performance ( $I_{DQ}=90\text{mA}$ , $T_A = 25^\circ\text{C}$ , CW)

$V_{DS}$	Freq.	Gmax	Pout		PAE
[V]	[MHz]	[dB]	[dBm]	[mW]	[%]
3.7	400	17.5	22.0	160	53.4
	440	16.0	23.2	210	67.4
	480	15.4	23.2	210	64.4
	520	13.8	23.0	200	61.3

Capable of Handling 20:1 VSWR @ 6.0 Vdc, 0.2 Watts, CW

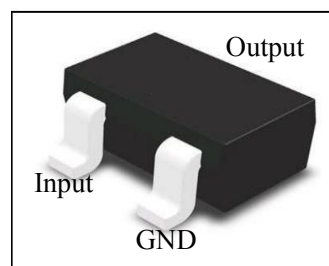


Figure 1. Pin Connections

## Features

- Characterized for Operation from 136 to 941 MHz
- Unmatched Input and Output Allowing Broad Frequency Range Utilization
- Integrated ESD Protection
- Broadband – Full Power Across the Band
- Exceptional Thermal Performance
- Extreme Ruggedness

## Typical Applications

- Output Stage VHF Band Handheld Radio
- Output Stage UHF Band Handheld Radio
- Output Stage for 700–800 MHz Handheld Radio
- Driver for 10–1000 MHz Applications

# HPL09S0P1T2

## RF Power Field Effect Transistor

**Table1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +20	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +8	Vdc
Operating Voltage	$V_{DD}$	0, +6	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	-40 to +150	°C
Operating Junction Temperature	$T_J$	-40 to +150	°C
Power Dissipation (@TC=25°C)	PD	0.25	Watts

**Table 2. ESD Protection Characteristic**

Test Methodology	Class
Human Body Model (per JESD22--A114)	2, passes 2500 V
Machine Model (per EIA/JESD22--A115)	A, passes 100 V
Charge Device Model (per JESD22--C101)	IV, passes 2000 V

**Table 3. Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Characteristic	Symbol	Min	Typ.	Max	Unit
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### Off Characteristics

Gate-Source Leakage Current ( $V_{GS}=5\text{Vdc}$ , $V_{DS}=0\text{Vdc}$ )	$I_{GSS}$	-	-	500	nAdc
Zero Gate Voltage Drain Leakage Current ( $V_{DS}=16\text{Vdc}$ , $V_{GS}=0\text{Vdc}$ )	$I_{DSS}$	-	-	100	nAdc
Zero Gate Voltage Drain Leakage Current ( $V_{DS}=3.7\text{Vdc}$ , $V_{GS}=0\text{Vdc}$ )	$I_{DSS}$	-	-	100	nAdc

### On Characteristics

Gate Threshold Voltage ( $V_{DS}=3.7\text{Vdc}$ , $I_D=1\text{mA}$ )	$V_{GS(th)}$	1.6	1.8	2.0	Vdc
Gate Quiescent Voltage ( $V_{DD}=3.7\text{Vdc}$ , $I_D=90\text{mA}$ Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.6	2.8	Vdc
Drain-Source On-Voltage ( $V_{GS}=5\text{Vdc}$ , $I_D=100\text{mA}$ )	$V_{DS(ON)}$	-	0.28	-	Vdc

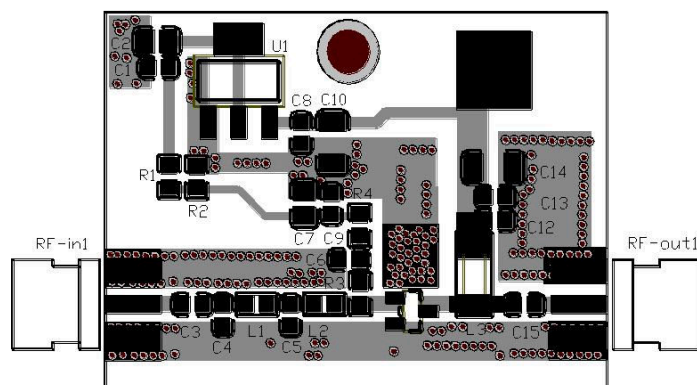
### Dynamic Characteristics

Reverse Transfer Capacitance ( $V_{DG}=3.7\text{V}$ , Level=30mVac@1MHz)	$C_{rss}$	-	0.25	-	pF
Output Capacitance ( $V_{DS}=3.7\text{V}$ , Level=30mVac@1MHz)	$C_{oss}$	-	1.8	-	pF
Input Capacitance ( $V_{GS}=5\text{V}$ , Level=30mVac@1MHz)	$C_{iss}$	-	8.0	-	pF

### Typical Performances (In DuSemi Narrowband Test DEMO, 50 Ohm system)

Frequency=440MHz,  $V_{DD}=3.7\text{Vdc}$ ,  $I_{D(Q)}=90\text{mA}$ ,  $P_{in}=7\text{dBm}$ ,  $T_A=25^{\circ}\text{C}$

Output Power	$P_{out}$	-	151	-	mW
Power Gain	$G_{PS}$	-	15	-	dB
Drain Efficiency	$\eta_D$	-	50	-	%

**Broad Band Evaluation Circuit (@VDD = 3.7V, f = 440 MHz)**

Test Circuit Component Layout

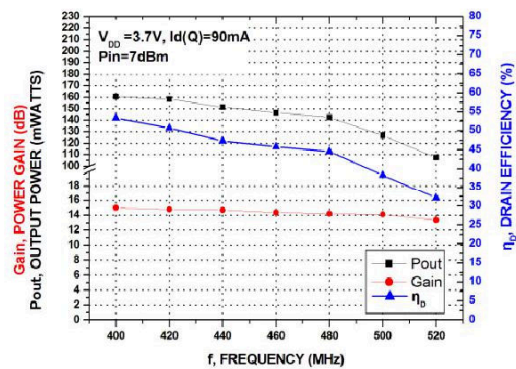
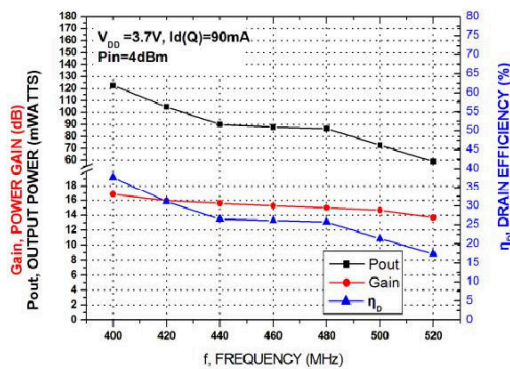
**Table 5. Test Circuit Component Designations and Value**

Part	Description	Part Number	Manufacturer
R3	470Ohm	—	—
R4	6.8KOhm	—	—
L1, L2	4.7nH	—	—
L3	8 Turns D: 0.5 mm, φ 2.4 mm Enamel Wire	—	—
C3,C15,	100pF Chip Capacitors	GQM21P5C1H101JB01	Murata
C4	18pF Chip Capacitors	GRM1885C1H201JA01	Murata
C12, C9	1000pF Chip Capacitors	GRM1885C1H102JA01	Murata
C10, C14,C7	10uF,25VChip Capacitors	—	—
C5	24pF Chip Capacitors	—	Murata
R1,R2,C1,C2,C8,C6	NC	—	—
U1	LM1117	—	—
PCB	FR-4 ,1.6mm, $\epsilon_r$ 4.5	—	—

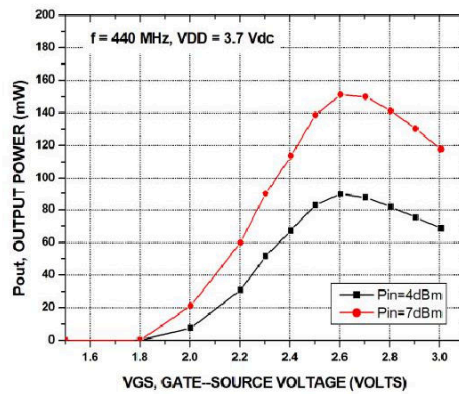
## TYPICAL CHARACTERISTICS

## 1. Power Gain, Drain Efficiency and Output Power versus Frequency at a Constant Pin

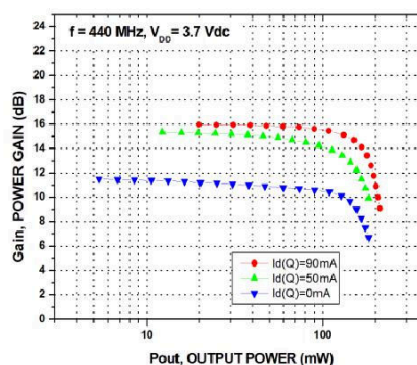
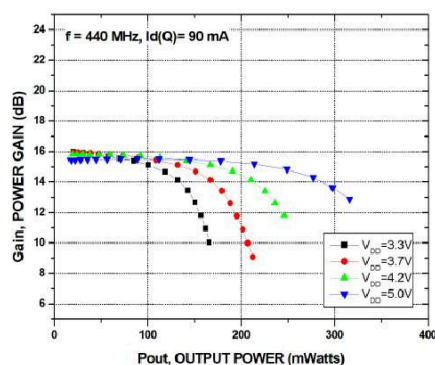
$V_{DD}$	$I_{D(Q)}$	$P_{in}$	Freq	Pout		Gain	$\eta_D$
[V]	[mA]	[dBm]	[MHz]	[dBm]	[mW]	[dB]	[%]
3.7	90	7	400	22.1	161	15.0	53.4
			440	21.8	151	14.7	47.4
			480	21.5	142	14.2	44.6
			520	20.3	107	13.4	32.1



## 2. Output Power versus Gate-Source Voltage @440MHz

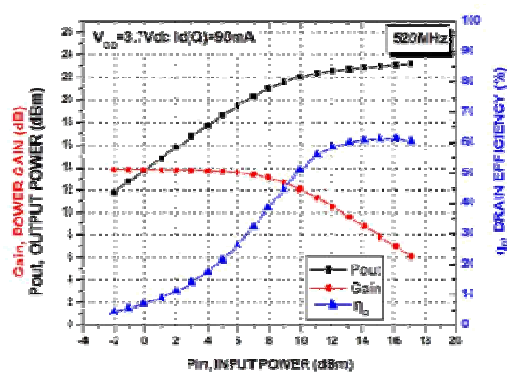
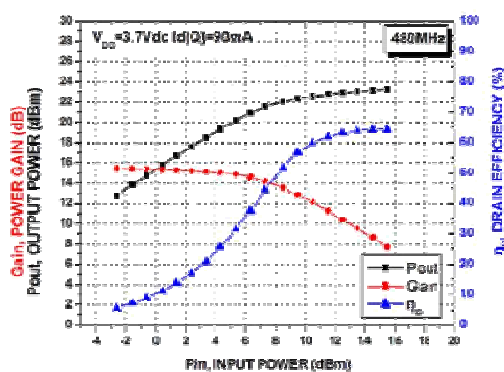
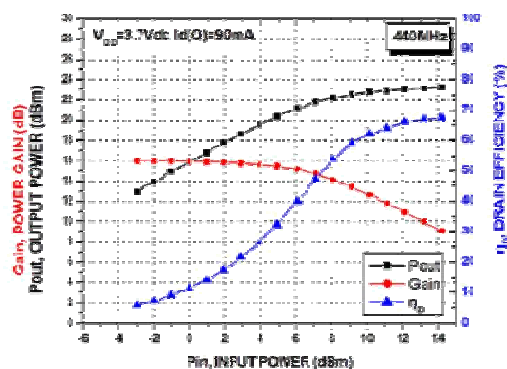
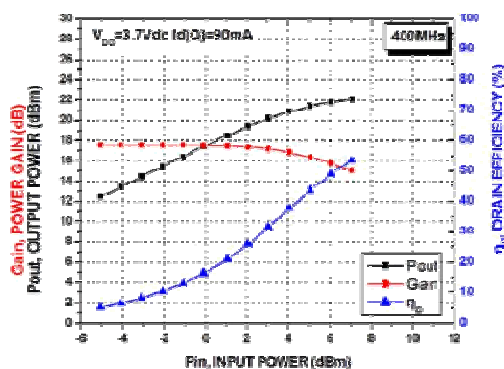


## 3. Power Gain versus Output Power@440MHz



## 4. Power Gain, Drain Efficiency and Output Power versus Input Power

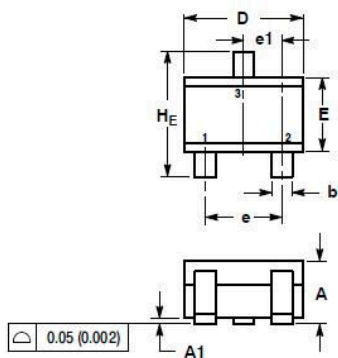
$V_{DS}$	$I_d(Q)$	Freq.	Gain	Pout		$\eta_D$
[V]	[mA]	[MHz]	[dB]	[dBm]	[mW]	[%]
3.7	90	400	17.5	22.0	160	53.4
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### PACKAGE

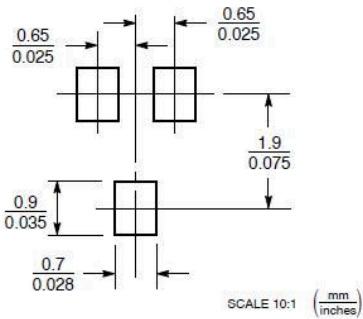


NOTES:

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.85 BSC			0.026 BSC		
L	0.20	0.38	0.58	0.008	0.015	0.022
He	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 3:  
PIN 1.gate  
2.source  
3.drain

#### SOLDERING FOOTPRINT\*



**REVISION HISTORY**

The following table summarizes revisions to this document.

<b>Revision</b>	<b>Date</b>	<b>Description</b>
1.0	July 2018	Initial Release of Data Sheet