CMOSTEK

CMT2113A

Low-Cost 240 – 480 MHz (G)FSK/OOK Transmitter

Features

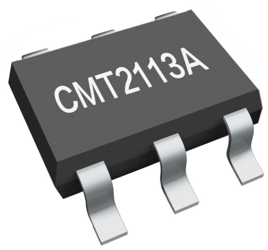
- Embedded EEPROM
  - Very Easy Development with RFPDK
  - All Features Programmable
- Frequency Range: 240 to 480 MHz
- OOK, FSK and GFSK Modulation
- Symbol Rate:
  - 0.5 to 30 ksps (OOK)
  - 0.5 to 100 ksps (FSK)
- Deviation: 1.0 to 200 kHz
- Output Power: -10 to +13 dBm
- Supply Voltage: 1.8 to 3.6 V
- Sleep Current: < 20 nA
- FCC/ETSI Compliant
- RoHS Compliant
- 6-pin SOT23-6 Package

Applications

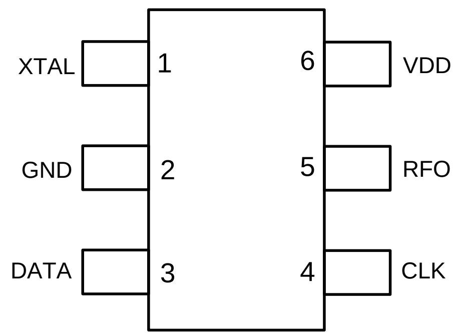
- Low-Cost Consumer Electronics Applications
- Home and Building Automation
- Remote Fan Controllers
- Infrared Transmitter Replacements
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Remote Keyless Entry (RKE)

Ordering Information

Part Number	Frequency	Package	MOQ
CMT2113A-ESR	433.92 MHz	SOT23-6	3,000 pcs
More Ordering Info: See Page 21			



SOT23-6



CMT2113A

Descriptions

The CMT2113A is ultra low-cost, highly flexible, high performance, single-chip (G)FSK/OOK transmitters for various 240 to 480 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. With very low current consumption, the device modulates and transmits the data which is sent from the host MCU. An embedded EEPROM allows the frequency, output power and other features to be programmed into the chip using the CMOSTEK USB Programmer and RFPDK. Alternatively, in stock product of 433.92 MHz is available for immediate demands without the need of EEPROM programming. The CMT2113A uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. The device can deliver up to +13 dBm output power. It operates from a supply voltage of 1.8 V to 3.6 V, consumes 23.5 mA (FSK) when transmitting at +10 dBm output power; and leaks only 20 nA when it is in sleep state, providing superior operation life for battery powered applications. The CMT2113A transmitter together with the CMT2213A receiver enables an ultra low cost FSK RF link.

Typical Application

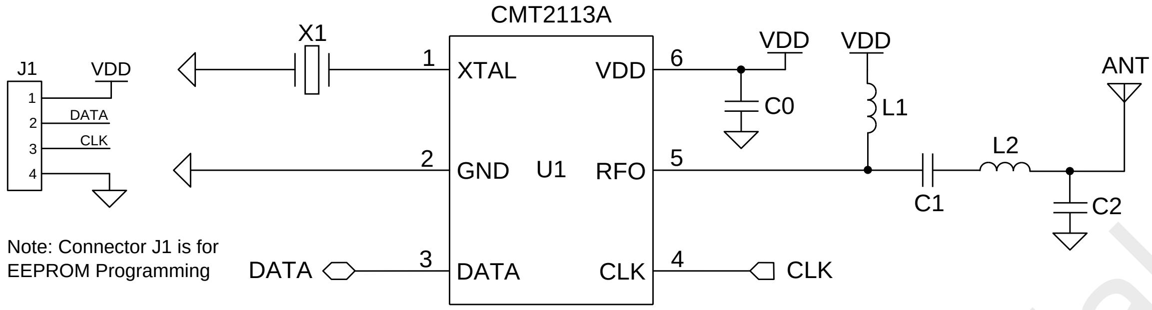


Figure 1. CMT2113A Typical Application Schematic

Table 1. BOM of 315/433.92 MHz Low-Cost Application

Designator	Descriptions	Value		Unit	Manufacturer
		315 MHz	433.92 MHz		
U1	CMT2113A, low-cost 240 – 480 MHz (G)FSK/OOK transmitter	-		-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26		MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	82	82	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	10	9	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	47	27	nH	Murata LQG18

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
GFSK	Gauss Frequency Shift Keying
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PN	Phase Noise
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
SR	Symbol Rate
TWI	Two-wire Interface
Tx	Transmission, Transmitter
Typ	Typical
USB	Universal Serial Bus
XO/XOSC	Crystal Oscillator
XTAL	Crystal
PA	Power Amplifier

Table of Contents

1. Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 433.92 MHz, FSK modulation, output power is +10 dBm terminated in a matched 50 Ω impedance, unless otherwise noted.

1.1 Recommended Operating Conditions

Table 2. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		1.8		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

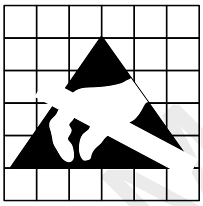
1.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Transmitter Specifications

Table 4. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}		240		480	MHz
Synthesizer Frequency Resolution	F_{RES}			198		Hz
Symbol Rate	SR	OOK	0.5		30	ksps
		(G)FSK	0.5		100	ksps
Deviation	F_{DEV}		1		200	kHz
Maximum Output Power	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
PA Ramping Time[2]	t_{RAMP}		0		1024	us
Current Consumption @ 315 MHz	I_{DD-315}	OOK, 0 dBm, 50% duty cycle		5.5		mA
		OOK, +10 dBm, 50% duty cycle		11.5		mA
		OOK, +13 dBm, 50% duty cycle		14.7		mA
		FSK, 0 dBm, 9.6 ksps		8.6		mA
		FSK, +10 dBm, 9.6 ksps		20.9		mA
		FSK, +13 dBm, 9.6 ksps		27.2		mA
Current Consumption @ 433.92 MHz	$I_{DD-433.92}$	OOK, 0 dBm, 50% duty cycle		6.7		mA
		OOK, +10 dBm, 50% duty cycle		13.4		mA
		OOK, +13 dBm, 50% duty cycle		17.4		mA
		FSK, 0 dBm, 9.6 ksps		10.5		mA
		FSK, +10 dBm, 9.6 ksps		23.5		mA
		FSK, +13 dBm, 9.6 ksps		32.5		mA
Sleep Current	I_{SLEEP}			20		nA
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise @433.92 MHz	$PN_{433.92}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		200 kHz offset from F_{RF}		-82		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Harmonics Output for 433.92 MHz[3]	$H2_{433.92}$	2^{nd} harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	$H3_{433.92}$	3^{rd} harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
OOK Extinction Ration				60		dB

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. 0 and 2^n us, n = 0 to 10, when set to "0", the PA output power will ramp to its configured value in the shortest possible time.

[3]. The harmonics output is measured with the application shown as Figure 10.

1.4 Crystal Oscillator

Table 5. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency[1]	F_{XTAL}		26	26	26	MHz
Crystal Tolerance[2]				±20		ppm
Load Capacitance[3]	C_{LOAD}		12		20	pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[4]	t_{XTAL}			400		us

Notes:

[1]. The CMT2113A can directly work with external 26 MHz reference clock input to XTAL pin (a coupling capacitor is required) with amplitude 0.3 to 0.7 Vpp.

[2]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[3]. The required crystal load capacitance is integrated on-chip to minimize the number of external components.

[4]. This parameter is to a large degree crystal dependent.

2. Pin Descriptions

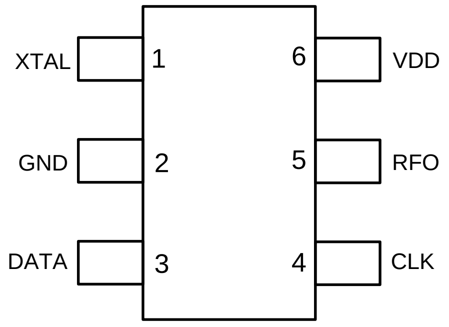


Figure 2. CMT2113A Pin Assignments

Table 6. CMT2113A Pin Descriptions

Pin Number	Name	I/O	Descriptions
1	XTAL	I	26 MHz single-ended crystal oscillator input or External 26 MHz reference clock input
2	GND	I	Ground
3	DATA	IO	Data input to be transmitted or Data pin to access the embedded EEPROM Pulled down internally to GND when configured as Transmission Enabled by DATA Pin Falling Edge and used as input pin Pulled up internally to VDD when configured as Transmission Enabled by DATA Pin Rising Edge and used as input pin
4	CLK	I	Clock pin to control the device Clock pin to access the embedded EEPROM Pulled up internally to VDD
5	RFO	O	Power amplifier output
6	VDD	I	Power supply input

3. Typical Performance Characteristics

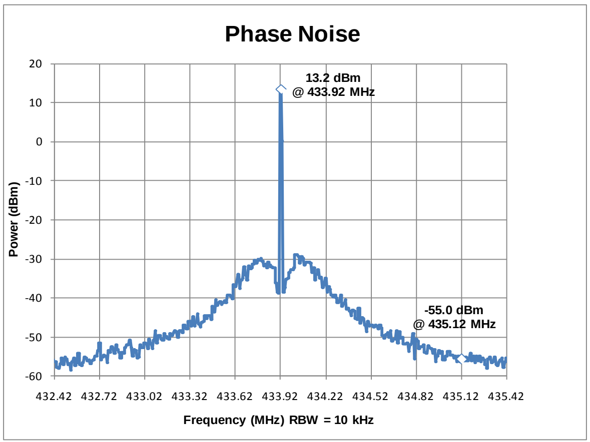


Figure 4. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Unmodulated

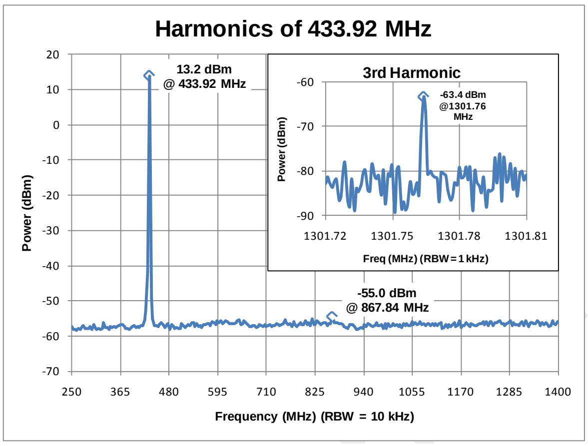


Figure 3. Harmonics of 433.92 MHz, P_{OUT} = +13 dBm

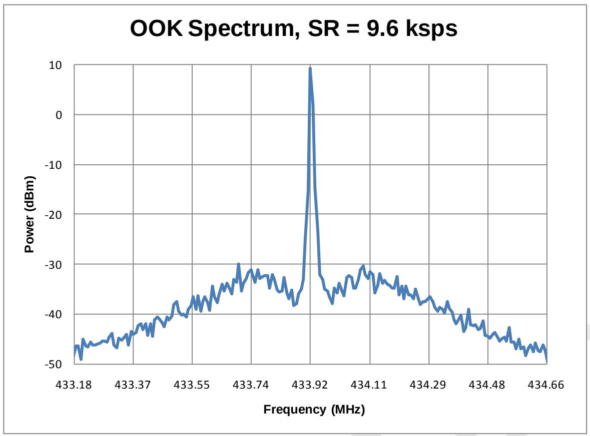


Figure 5. OOK Spectrum, SR = 9.6 ksps, P_{OUT} = +10 dBm, t_{RAMP} = 32 us

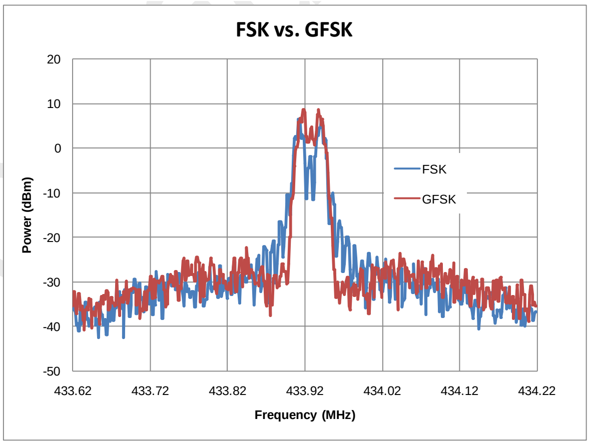


Figure 6. FSK/GFSK Spectrum, SR = 9.6 ksps, F_{DEV} = 15 kHz

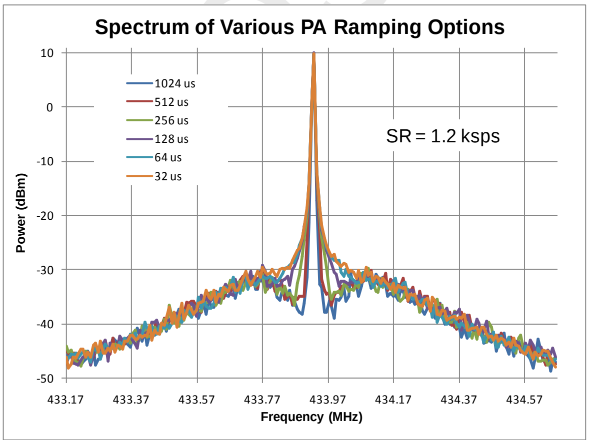


Figure 7. Spectrum of PA Ramping, SR = 1.2 ksps, P_{OUT} = +10 dBm

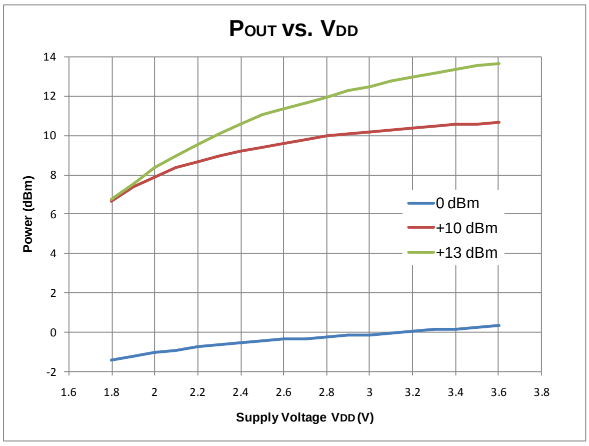


Figure 8. Output Power vs. Supply Voltages, F_{RF} = 433.92 MHz

4. Typical Application Schematics

4.1 Low-Cost Application Schematic

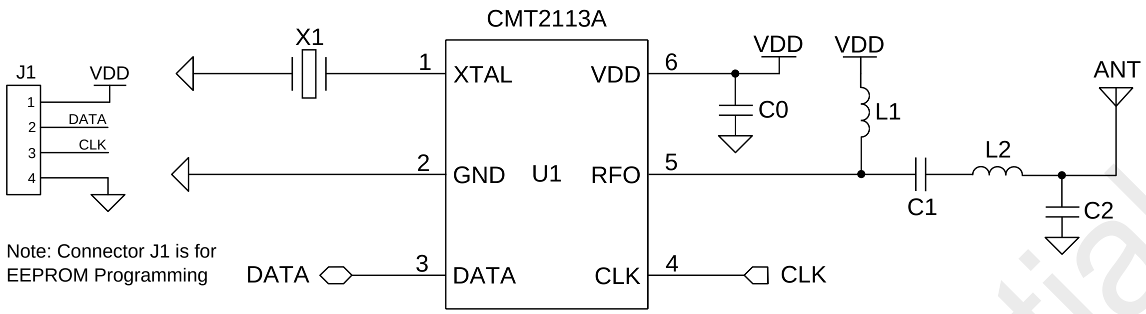


Figure 9. Low-Cost Application Schematic

Notes:

1. Connector J1 is a must for the CMT2113A EEPROM access during development or manufacture.
2. The general layout guidelines are listed below. For more design details, please refer to “AN101 CMT211xA Schematic and PCB Layout Design Guideline”
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2113A as possible for better filtering.
3. The table below shows the BOM of 315/433.92 MHz Low-Cost Applications. For the BOM of more applications, please refer to “AN101 CMT211xA Schematic and PCB Layout Design Guideline”.

Table 7. BOM of 315/433.92 MHz Low-Cost Application

Designator	Descriptions	Value		Unit	Manufacturer
		315 MHz	433.92 MHz		
U1	CMT2113A, low-cost 240 – 480 MHz (G)FSK/OOK transmitter	-		-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26		MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	82	82	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	10	9	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	47	27	nH	Murata LQG18

4.2 FCC/ETSI Compliant Application Schematic

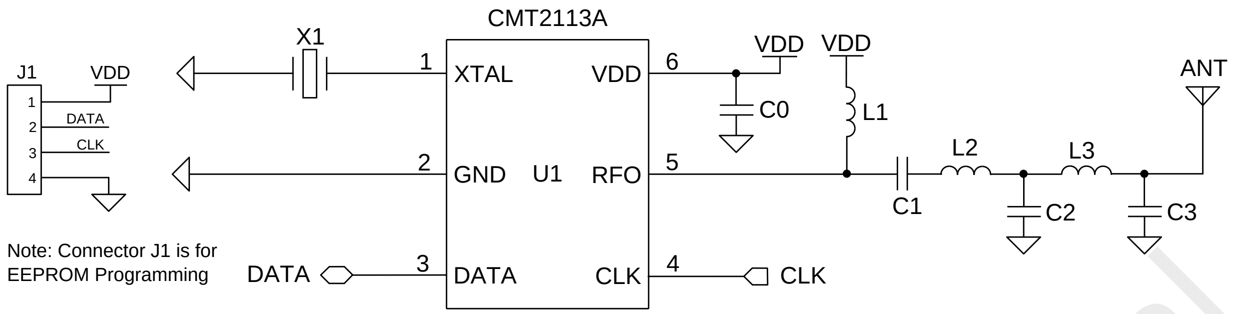


Figure 10. FCC/ETSI Compliant Application Schematic

Notes:

1. Connector J1 is a must for the CMT2113A EEPROM access during development or manufacture.
2. The general layout guidelines are listed below. For more design details, please refer to "AN101 CMT211xA Schematic and PCB Layout Design Guideline".
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2113A as possible for better filtering.
3. The table below shows the BOM of 315/433.92 MHz FCC/ETSI Compliant Application. For the BOM of other applications, please refer to "AN101 CMT211xA Schematic and PCB Layout Design Guideline".

Table 8. BOM of 315/433.92 MHz FCC/ETSI Compliant Application

Designator	Descriptions	Value		Unit	Manufacturer
		315 MHz	433.92 MHz		
U1	CMT2113A, low-cost 240 – 480 MHz (G)FSK/OOK transmitter	-			CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26		MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1		uF	Murata GRM15
C1	±5%, 0402 NP0, 50 V	68	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	18	15	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	18	15	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	180	180	nH	Murata LQG18
L2	±5%, 0603 multi-layer chip inductor	62	36	nH	Murata LQG18
L3	±5%, 0603 multi-layer chip inductor	27	18	nH	Murata LQG18

5. Functional Descriptions

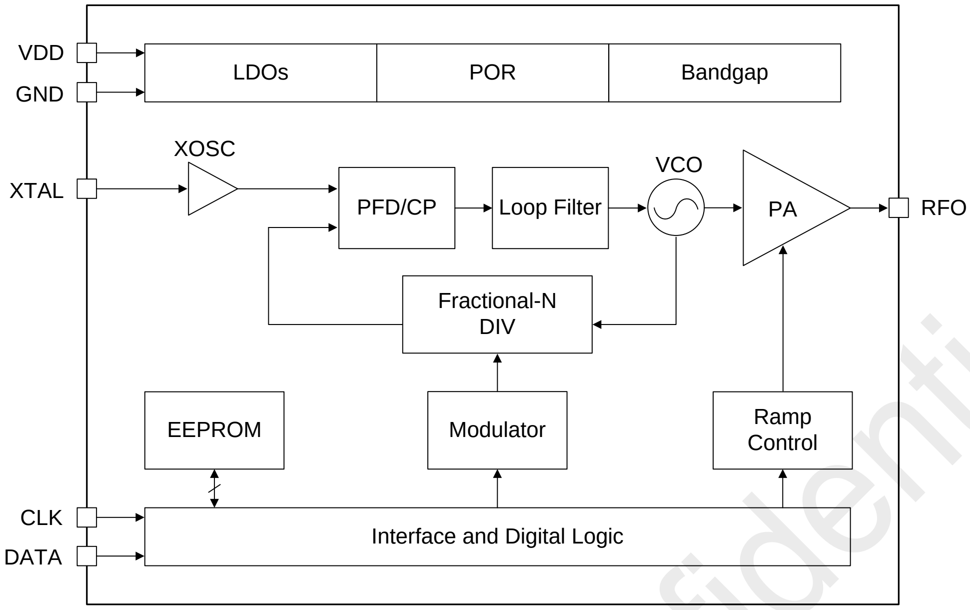


Figure 11. CMT2113A Functional Block Diagram

5.1 Overview

The CMT2113A is an ultra low-cost, highly flexible, high performance, single-chip (G)FSK/OOK transmitter for various 240 to 480 MHz wireless applications. It is part of the CMOSTEK NextGenRF^{TM} family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the CMT2113A is shown in the figure above. The CMT2113A is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the reference voltage generated by Bandgap. The calibration can help the chip to finely work under different temperatures and supply voltages. The CMT2113A uses the DATA pin for the host MCU to send in the data. The input data will be modulated and sent out by a highly efficient PA which output power can be configured from -10 to +13 dBm in 1 dB step size. RF Frequency, PA output power and other product features can be programmed into the embedded EEPROM by the RFPDK and USB Programmer. This saves the cost and simplifies the product development and manufacturing effort. Alternatively, in stock product of 433.92 MHz is available for immediate demands with no need of EEPROM programming. The CMT2113A operates from 1.8 to 3.6 V so that it can finely work with most batteries to their useful power limits. It only consumes 12.4 mA when transmitting +10 dBm power under 3.3 V supply voltage.

5.2 Modulation, Frequency, Deviation and Symbol Rate

The CMT2113A supports GFSK/FSK modulation with the symbol rate up to 100 ksps, as well as OOK modulation with the symbol rate up to 30 ksps. The supported deviation of the (G)FSK modulation ranges from 1 to 200 kHz. The the CMT2113A covers the frequency range from 240 to 480 MHz, including the license free ISM frequency band around 315 MHz and 433.92 MHz. The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz. See the table below for the modulation, frequency and symbol rate specifications.

Table 9. Modulation, Frequency and Symbol Rate

Parameter	Value	Unit
Modulation	(G)FSK/OOK	-
Frequency	240 to 480	MHz
Deviation	1 to 200	kHz
Frequency Resolution	<198	Hz
(G)FSK Symbol Rate	0.5 to 100	ksps
OOK Symbol Rate	0.5 to 30	ksps

5.3 Embedded EEPROM and RFPDK

The RFPDK (RF Products Development Kit) is a very user-friendly software tool delivered for the user configuring the CMT2113A in the most intuitional way. The user only needs to fill in/select the proper value of each parameter and click the "Burn" button to complete the chip configuration. No register access and control is required in the application program. See the figure below for the accessing of the EEPROM and Table 10 for the summary of all the configurable parameters of the CMT2113A in the RFPDK.

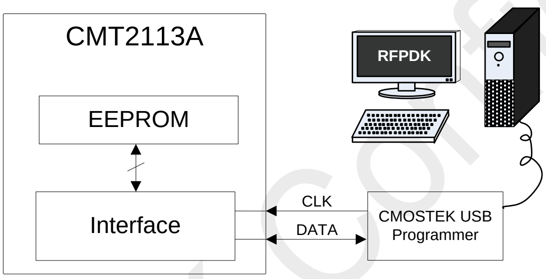


Figure 12. Accessing Embedded EEPROM

For more details of the CMOSTEK USB Programmer and the RFPDK, please refer to "AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide". For the detail of CMT2113A configurations with the RFPDK, please refer to "AN122 CMT2113A Configuration Guideline".

Table 10. Configurable Parameters in RFPDK

Category	Parameters	Descriptions	Default	Mode
RF Settings	Frequency	To input a desired transmitting radio frequency in the range from 240 to 480 MHz. The step size is 0.001 MHz.	433.92 MHz	Basic Advanced
	Modulation	The option is FSK or GFSK or OOK.	FSK	Basic Advanced
	Deviation	The (G)FSK frequency deviation. The range is from 1 to 200 kHz.	35 kHz	Basic Advanced
	Tx Power	To select a proper transmitting output power from -10 dBm to +14 dBm, 1 dB margin is given above +13 dBm.	+13 dBm	Basic Advanced
	Xtal Load	On-chip XOSC load capacitance options: from 10 to 22 pF. The step size is 0.33 pF.	15.00 pF	Basic Advanced
	Data Representation	To select whether the frequency “Fo + Fdev” represent data 0 or 1. The options are: 0: F-high 1: F-low, or 0: F-low 1: F-high.	0: F-low 1: F-high	Advanced
	PA Ramping	To control PA output power ramp up/down time, options are 0 and 2^n us (n from 0 to 10).	0 us	Advanced
Transmitting Settings	Start by	Start condition of a transmitting cycle, by Data Pin Rising/Falling Edge.	Data Pin Rising Edge	Advanced
	Stop by	Stop condition of a transmitting cycle, by Data Pin Holding Low for 2 to 90 ms.	Data Pin Holding Low for 2 ms	Advanced

5.4 Power Amplifier

A highly efficient single-ended Power Amplifier (PA) is integrated in the CMT2113A to transmit the modulated signal out. Depending on the application, the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in “Chapter 4 Typical Application Schematic”. For the schematic, layout guideline and the other detailed information please refer to “AN101 CMT211xA Schematic and PCB Layout Design Guideline”.

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the CMOSTEK USB Programmer and RFPDK.

5.5 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The CMT2113A has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 13. When the option is set to “0”, the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

CMOSTEK recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping “rate”, as shown in the formula below.

$$SR_{Max} \leq 0.5 * \left(\frac{1}{t_{RAMP}}\right)$$

In which the PA ramping “rate” is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by formula below.

$$t_{RAMP} \leq 0.5 * \left(\frac{1}{SR_{MAX}}\right)$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than “0.5 * ($1/SR_{Max}$)”, it will possibly bring additional challenges to the OOK demodulation of the Rx device. For more detail of calculating t_{RAMP}, please refer to “AN122 CMT2113A Configuration Guideline”.

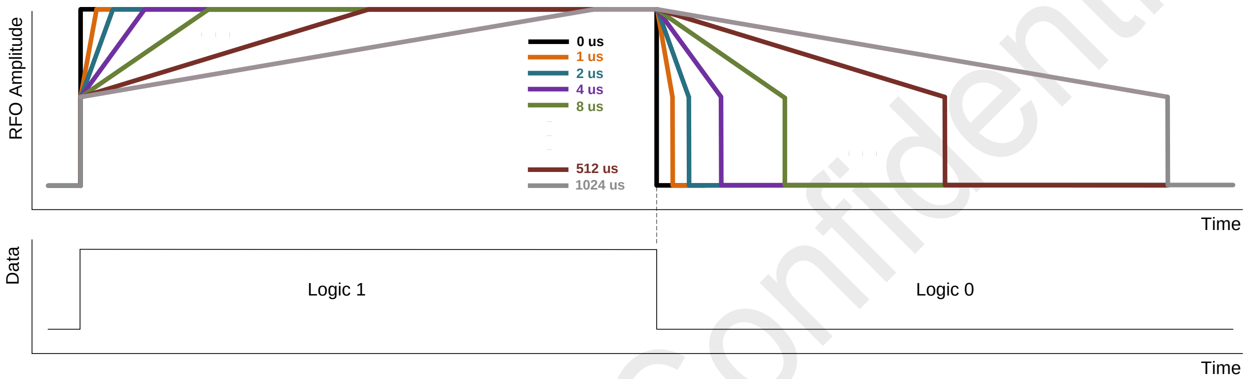
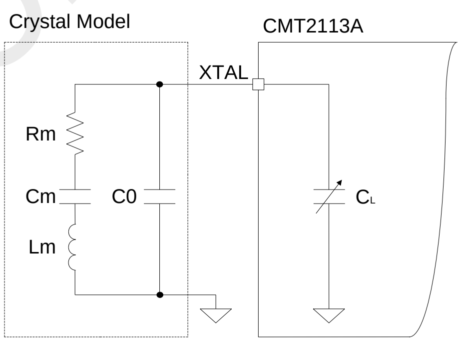


Figure 13. PA Ramping Time

5.6 Crystal Oscillator and RCLK

The CMT2113A uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 14 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is 26 MHz with ±20 ppm, ESR (Rm) < 60 Ω, load capacitance C_{LOAD} ranging from 12 to 20 pF. To save the external load capacitors, a set of variable load capacitors C_L is built inside the CMT2113A to support the oscillation of the crystal.

The value of load capacitors is configurable with the CMOSTEK USB Programmer and RFPDK. To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO frequency. Please refer to “AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide” for the method of choosing the right value of C_L.



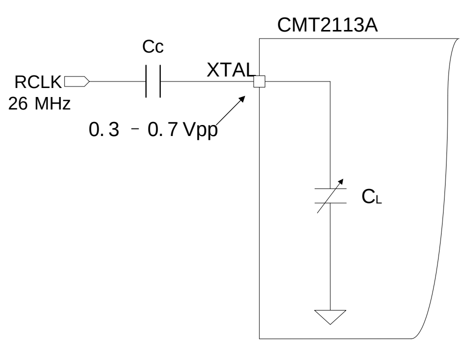


Figure 14. XTAL Circuitry and Crystal Model

Figure 15. RCLK Circuitry

If a 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2113A by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 15 for the RCLK circuitry.

6. Working States and Transmission Control Interface

6.1 Working States

The CMT2113A has 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the CMT2113A is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized to 20 nA typically.

XO-STARTUP

After detecting a valid control signal on DATA pin, the CMT2113A goes into the XO-STARTUP state, and the internal XO starts to work. The valid control signal can be a rising or falling edge on the DATA pin, which can be configured on the RFPDK. The host MCU has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in Table 11.

TUNE

The frequency synthesizer will tune the CMT2113A to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the incoming data only after the TUNE state is done, before that the incoming data will not be transmitted. See Figure 16 and Figure 17 for the details.

TRANSMIT

The CMT2113A starts to modulate and transmit the data coming from the DATA pin. The transmission can be ended in 2 methods: firstly, driving the DATA pin low for t_{STOP} time, where the t_{STOP} can be configured from 2 to 90 ms on the RFPDK; secondly, issuing SOFT_RST command over the two-wire interface (TWI), this will stop the transmission in 1 ms. See section 6.2.3 for details of the TWI.

Table 11. Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop The Transmission[2]	t_{STOP}	2		90	ms

Notes:

[1]. This parameter is to a large degree crystal dependent.

[2]. Configurable from 2 to 9 in 1 ms step size and 20 to 90 ms in 10 ms step size.

6.2 Transmission Control Interface

The CMT2113A uses the DATA pin for the host MCU to send in data for modulation and transmission. The DATA pin can be used as pin for EEPROM programming, data transmission, as well as controlling the transmission. The transmission can be started by detecting rising or falling edge on the DATA pin, and stopped by driving the DATA pin low for t_{STOP} as shown in the table above. Besides communicating over the DATA pin, the host MCU can also communicate with the device over the TWI, so that the transmission is more robust, and consumes less current.

Please note that the user is recommended to use the Tx Enabled by DATA pin Rising Edge, which is described in Section 6.2.1.

6.2.1 Tx Enabled by DATA Pin Rising Edge

As shown in the Figure 16, once the CMT2113A detects a rising edge on the DATA pin, it goes into the XO-STARTUP state. The user has to pull the DATA pin high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the DATA pin. The logic state of the DATA pin is "Don't Care" from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission.

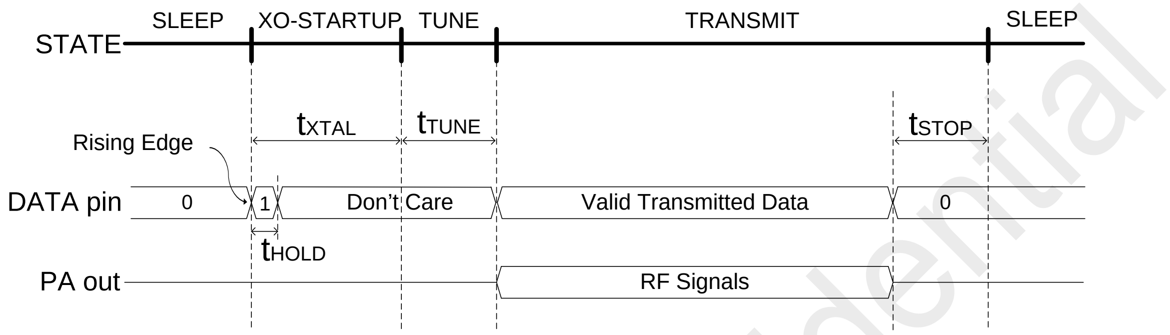


Figure 16. Transmission Enabled by DATA Pin Rising Edge

6.2.2 Tx Enabled by DATA Pin Falling Edge

As shown in the Figure 17, once the CMT2113A detects a falling edge on the DATA pin, it goes into XO-STARTUP state and the XO starts to work. During the XO-STARTUP state, the DATA pin needs to be pulled low. After the XO is settled, the CMT2113A goes to the TUNE state. The logic state of the DATA pin is "Don't Care" during the TUNE state. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission. Before starting the next transmit cycle, the user has to pull the DATA pin back to high.

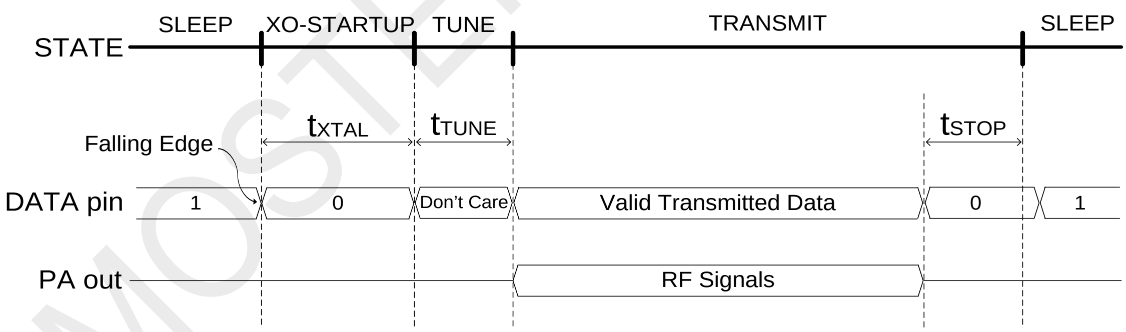


Figure 17. Transmission Enabled by DATA Pin Falling Edge

6.2.3 Two-wire Interface

For power-saving and reliable transmission purposes, the CMT2113A is recommended to communicate with the host MCU over the TWI: DATA and CLK. The TWI is designed to operate at a maximum of 1 MHz. The timing requirement and data transmission control through the TWI are shown in this section.

Table 12. TWI Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	V_{IH}		0.8			V_{DD}
Digital Input Level Low	V_{IL}				0.2	V_{DD}
CLK Frequency	F_{CLK}		10		1,000	kHz
CLK High Time	t_{CH}		500			ns
CLK Low Time	t_{CL}		500			ns
CLK Delay Time	t_{CD}	CLK delay time for the first falling edge of the TWI_RST command, see Figure 20	20		15,000	ns
DATA Delay Time	t_{DD}	The data delay time from the last CLK rising edge of the TWI command to the time DATA return to default state			15,000	ns
DATA Setup Time	t_{DS}	From DATA change to CLK falling edge	20			ns
DATA Hold Time	t_{DH}	From CLK falling edge to DATA change	200			ns

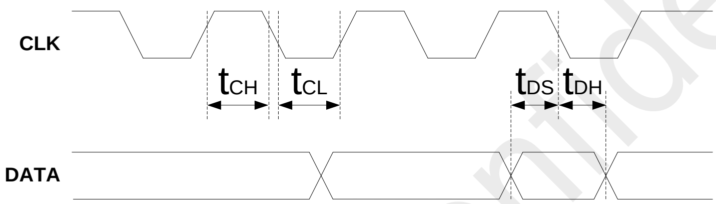


Figure 18. Two-wire Interface Timing Diagram

Once the device is powered up, TWI_RST and SOFT_RST should be issued to make sure the device works in SLEEP state robustly. On every transmission, TWI_RST and TWI_OFF should be issued before the transmission to make sure the TWI circuit functions correctly. TWI_RST and SOFT_RST should be issued again after the transmission for the device going back to SLEEP state reliably till the next transmission. The operation flow with TWI is shown as the figure below.

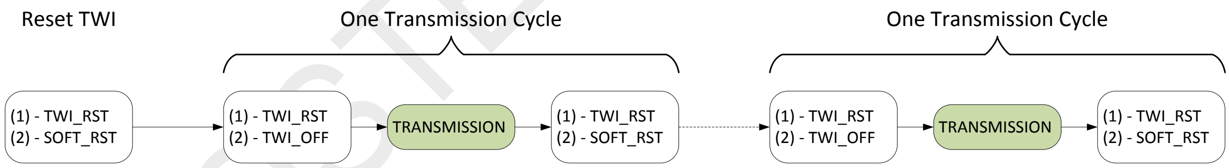


Figure 19. CMT2113A Operation Flow with TWI

Table 13. TWI Commands Descriptions

Command	Descriptions
TWI_RST	Implemented by pulling the DATA pin low for 32 clock cycles and clocking in 0x8D00, 48 clock cycles in total. It only resets the TWI circuit to make sure it functions correctly. The DATA pin cannot detect the Rising/Falling edge to trigger transmission after this command, until the TWI_OFF command is issued. **Notes:** a) Please ensure the DATA pin is firmly pulled low during the first 32 clock cycles. b) When the device is configured as Transmission Enabled by DATA Pin Falling Edge, in order to issue the TWI_RST command correctly, the first falling edge of the CLK should be sent t_{CD} after the DATA falling edge, which should be longer than the minimum DATA setup time 20 ns, and shorter than 15 us,

Command	Descriptions
	as shown in Figure 20. c) When the device is configured as Transmission Enabled by DATA Pin Rising Edge, the default state of the DATA is low, there is no t_{CD} requirement, as shown in Figure 21.
TWI_OFF	Implemented by clocking in 0x8D02, 16 clock cycles in total. It turns off the TWI circuit, and the DATA pin is able to detect the Rising/Falling edge to trigger transmission after this command, till the TWI_RST command is issued. The command is shown as Figure 22.
SOFT_RST	Implemented by clocking in 0xBD01, 16 clock cycles in total. It resets all the other circuits of the chip except the TWI circuit. This command will trigger internal calibration for getting the optimal device performance. After issuing the SOFT_RST command, the host MCU should wait 1 ms before sending in any new command. After that, the device goes to SLEEP state. The command is shown as Figure 23.

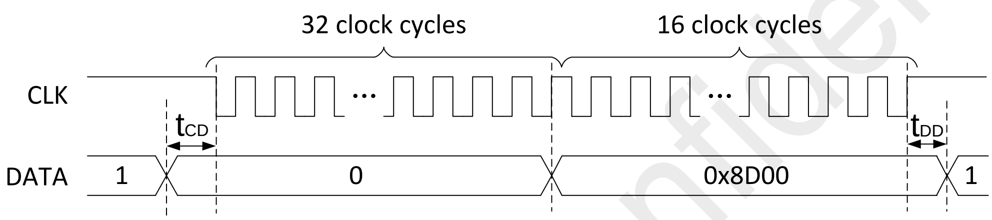


Figure 20. TWI_RST Command When Transmission Enabled by DATA Pin Falling Edge

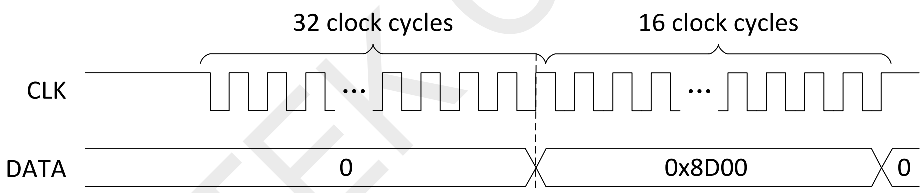


Figure 21. TWI_RST Command When Transmission Enabled by DATA Pin Rising Edge

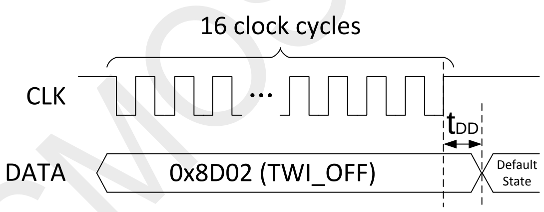


Figure 22. TWI_OFF Command

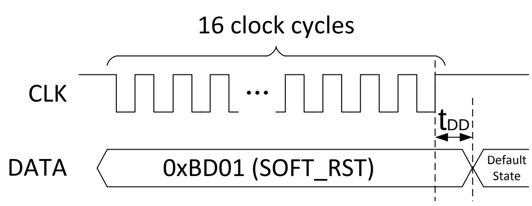


Figure 23. SOFT_RST Command

The DATA is generated by the host MCU on the rising edge of CLK, and is sampled by the device on the falling edge. The CLK should be pulled up by the host MCU during the TRANSMISSION shown in Figure 19. The TRANSMISSION process should refer to Figure 16 or Figure 17 for its timing requirement, depending on the "Start By" setting configured on the RFPDK.

The device will go to SLEEP state by driving the DATA low for t_{STOP}, or issuing SOFT_RST command. A helpful practice for the device to go to SLEEP is to issue TWI_RST and SOFT_RST commands right after the useful data is transmitted, instead of waiting the t_{STOP}, this can save power significantly.

7. Ordering Information

Table 14. CMT2113A Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2113A-ESR[1]	Low-Cost 240-480 MHz (G)FSK/OOK Transmitter	SOT23-6	Tape & Reel	1.8 to 3.6 V, -40 to 85 ℃	3,000

Notes:

[1]. "E" stands for extended industrial product grade, which supports the temperature range from -40 to +85 ℃.
"S" stands for the package type of SOT23-6.
"R" stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 3,000 pieces.
The default frequency for CMT2113A-ESR is 433.92 MHz, for the other settings, please refer to the Table 10 of Page 14.

Visit www.cmostek.com/products to know more about the product and product line.
Contact sales@cmostek.com or your local sales representatives for more information.

8. Package Outline

The 6-pin SOT23-6 illustrates the package details for the CMT2113A. The table below lists the values for the dimensions shown in the illustration.

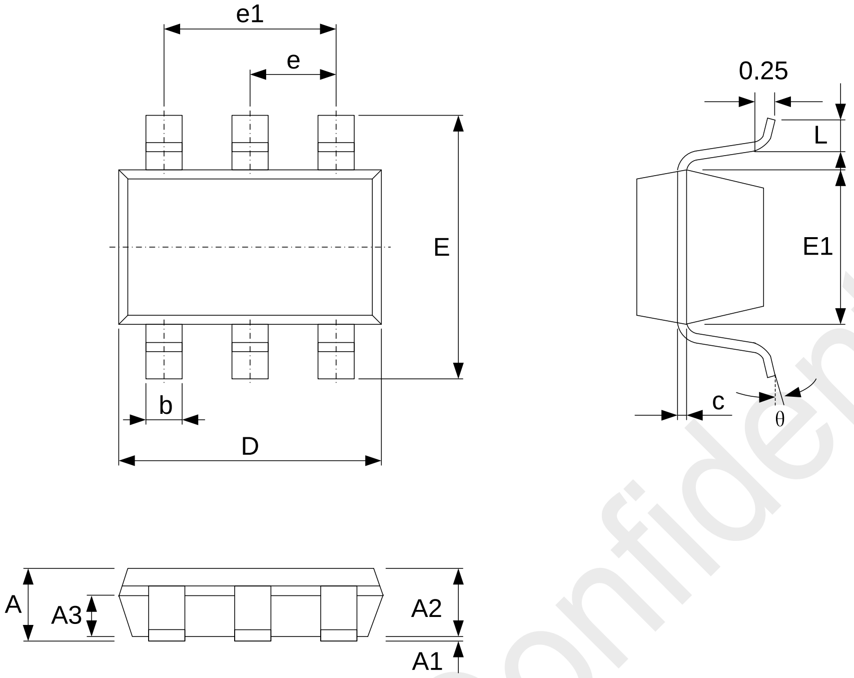


Figure 24. 6-Pin SOT23-6

Table 15. 6-Pin SOT23-6 Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	—	—	1.35
A1	0.04	—	0.15
A2	1.00	1.10	1.20
A3	0.55	0.65	0.75
b	0.38	—	0.48
C	0.08	—	0.20
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	—	0.60
θ	0	—	8°

9. Top Marking

9.1 CMT2113A Top Marking

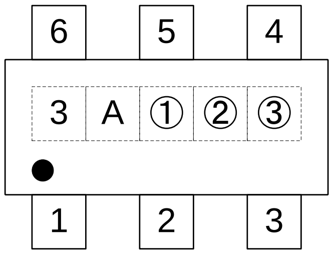


Figure 25. CMT2113A Top Marking

Table 16. CMT2113A Top Marking Explanation

Top Mark	3A①②③
Mark Method	Laser
Font Size	0.6 mm, right-justified
1st letter	3, represents CMT2113
2nd letter	A: represents revision A
3rd – 5th letter	①②③: Internal reference for data code tracking, assigned by the assembly house

10. Other Documentations

Table 17. Other Documentations for CMT2113A

Brief	Name	Descriptions
AN101	CMT211xA Schematic and PCB Layout Design Guideline	Details of CMT2110/13/17/19A PCB schematic and layout design rules, RF matching network and other application layout design related issues.
AN122	CMT2113A Configuration Guideline	Details of configuring CMT2113A features on the RFPDK.
AN103	CMT211xA-221xA One-Way RF Link Development Kits Users Guide	User's Guides for CMT211xA and CMT221xA Development Kits, including Evaluation Board and Evaluation Module, CMOSTEK USB Programmer and the RFPDK.

11. Document Change List

Table 18. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.8	All	Initial Released	2015-01-27

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