Sub GHz FSK/OOK Transmitter Module DATASHEET

KEY PRODUCT FEATURES

- Optional Chip Feature Configuration Schemes
  - On-Line Registers Configuration
  - Off-Line EEPROM Programming
- Frequency Range: 240 to 960 MHz
- FSK, GFSK and OOK Modulation
- Symbol Rate:
  - 0.5 to 100 ksps (FSK/GFSK)
  - 0.5 to 30 ksps (OOK)
- Deviation: 1.0 to 200 kHz
- Two-wire Interface for Registers Accessing and EEPROM Programming
- Output Power: -10 to +13 dBm
- Supply Voltage: 1.8 to 3.6 V
- Sleep Current: < 20 nA
- FCC/ETSI Compliant
- RoHS Compliant

APPLICATIONS

- Low-Cost Consumer Electronics Applications
- Home and Building Automation
- Remote Fan Controllers
- Infrared Transmitter Replacements
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Remote Keyless Entry (RKE)

GENERAL DESCRIPTION

The HC220 is a high performance, highly flexible, low-cost, single-chip (G)FSK/OOK transmitter for various 240 to 960 MHz wireless applications. It is a part of the NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The HC220 provides the simplest way to control the data transmission. The transmission is started when an effective level turnover is detected on the DATA pin, while the transmission action will stop after the DATA pin holding level low for a defined time window, or after a two-wire interface (TWI) command is issued. The chip features can be configured in two different ways: setting the configuration registers through the TWI, or programming the embedded EEPROM with USB Programmer and the RFPDK. The device operates from a supply voltage of 1.8 V to 3.6 V, consumes 27.6 mA (FSK @ 868.35 MHz) when transmitting +10 dBm output power, and only leak 20 nA when it is in sleep state.

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
GFSK	Gauss Frequency Shift Keying
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PN	Phase Noise
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
SR	Symbol Rate
TWI	Two-wire Interface
Tx	Transmission, Transmitter
Typ	Typical
USB	Universal Serial Bus
XO/XOSC	Crystal Oscillator
XTAL	Crystal
PA	Power Amplifier

Table of Contents Page

Index of Figures Page

Index of Tables

Page

1 Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 868.35 MHz, FSK modulation, output power is +10 dBm terminated in a matched 50 Ω

impedance, unless otherwise noted.

1.1 Recommended Operating Conditions

Table 1 Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		1.8		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

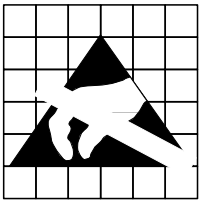
1.2 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Transmitter Specifications

Table 3 Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}		240		960	MHz
Synthesizer Frequency Resolution	F_{RES}	F_{RF} ≤ 480 MHz		198		Hz
		F_{RF} > 480 MHz		397		Hz
Symbol Rate	SR	FSK/GFSK	0.5		100	ksps
		OOK	0.5		30	ksps
(G)FSK Modulation Deviation Range	F_{DEV}		1		200	kHz
Bandwidth-Time Product	BT	GFSK modulation	-	0.5	-	-
Maximum Output Power	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
OOK PA Ramping Time[2]	t_{RAMP}		0		1024	us
Current Consumption @ 433.92 MHz	$I_{DD-433.92}$	OOK, 0 dBm, 50% duty cycle		6.7		mA
		OOK, +10 dBm, 50% duty cycle		13.4		mA
		OOK, +13 dBm, 50% duty cycle		17.4		mA
		FSK, 0 dBm, 9.6 ksps		10.5		mA
		FSK, +10 dBm, 9.6 ksps		23.5		mA
		FSK, +13 dBm, 9.6 ksps		32.5		mA
Current Consumption @ 868.35 MHz	$I_{DD-868.35}$	OOK, 0 dBm, 50% duty cycle		8.0		mA
		OOK, +10 dBm, 50% duty cycle		15.5		mA
		OOK, +13 dBm, 50% duty cycle		19.9		mA
		FSK, 0 dBm, 9.6 ksps		12.3		mA
		FSK, +10 dBm, 9.6 ksps		27.6		mA
		FSK, +13 dBm, 9.6 ksps		36.1		mA
Sleep Current	I_{SLEEP}			20		nA
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise @ 433.92 MHz	$PN_{433.92}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Phase Noise @ 868.35 MHz	$PN_{868.35}$	100 kHz offset from F_{RF}		-74		dBc/Hz
		600 kHz offset from F_{RF}		-92		dBc/Hz
		1.2 MHz offset from F_{RF}		-101		dBc/Hz
Harmonics Output for 433.92 MHz[3]	$H2_{433.92}$	2nd harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	$H3_{433.92}$	3rd harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
Harmonics Output for 868.35 MHz [3]	$H2_{868.35}$	2nd harm @ 1736.7 MHz, +13 dBm P_{OUT}		-67		dBm
	$H3_{868.35}$	3rd harm @ 2605.05 MHz, +13 dBm P_{OUT}		-55		dBm
OOK Extinction Ration				60		dB

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. 0 and 2^n us, n = 0 to 10, when set to "0", the PA output power will ramp to its configured value in the shortest possible time.

[3]. The harmonics output is measured with the application shown as Figure 10.

1.4 Crystal Oscillator

Table 4 Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency[1]	F_{XTAL}		26	26	26	MHz
Crystal Tolerance[2]				±20		ppm
Load Capacitance[3]	C_{LOAD}		12		20	pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[4]	t_{XTAL}			400		us

Notes:

[1]. The HC220 can directly work with external 26 MHz reference clock input to XTAL pin (a coupling capacitor is required) with amplitude 0.3 to 0.7 Vpp.

[2]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[3]. The required crystal load capacitance is integrated on-chip to minimize the number of external components.

[4]. This parameter is to a large degree crystal dependent.

2 Pin Configuration

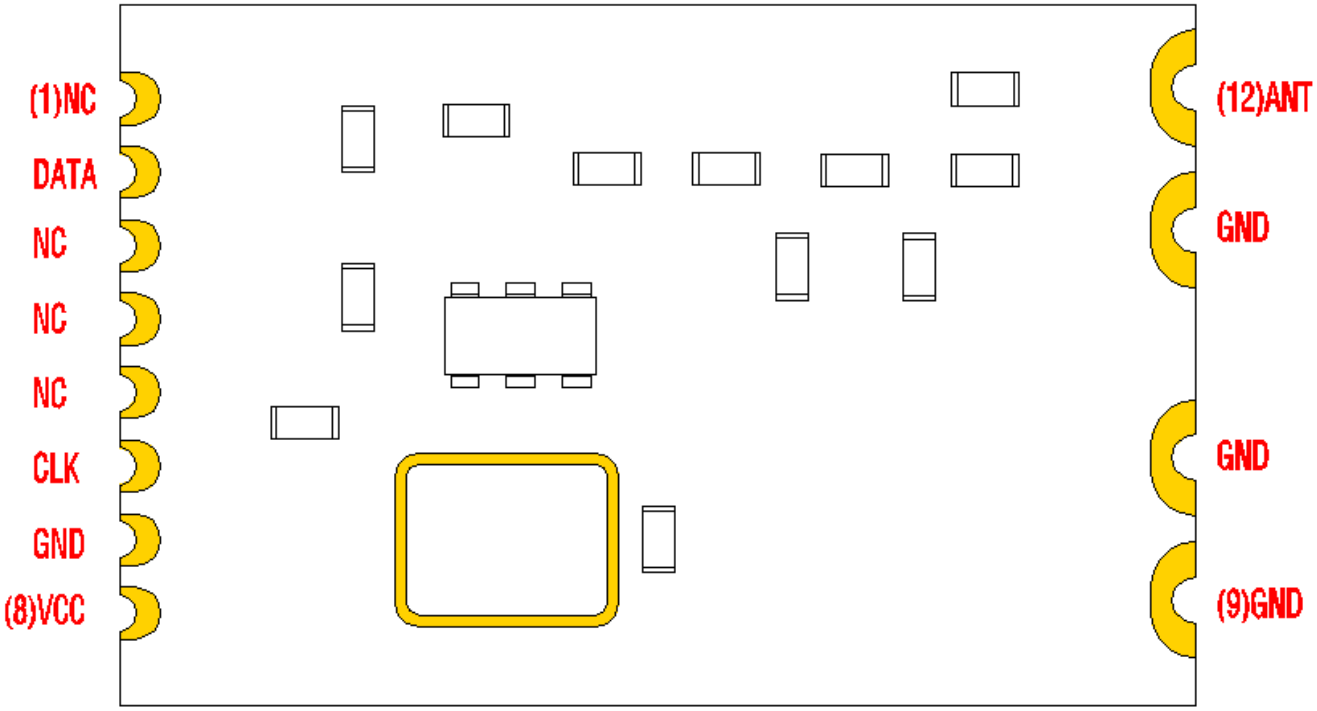


Figure 1. Pin Configuration

Table 5 HC220 Pin Descriptions

Pin Number	Name	I/O	Descriptions
1, 3, 4, 5	NC	–	–
2	DATA	IO	Data input to be transmitted or Data pin to access the embedded EEPROM Pulled down internally to GND when configured as Transmission Enabled by DATA Pin Falling Edge and used as input pin Pulled up internally to VDD when configured as Transmission Enabled by DATA Pin Rising Edge and used as input pin
6	CLK	I	Clock pin to control the device Clock pin to access the embedded EEPROM Pulled up internally to VDD
7, 9, 10, 11	GND	I	Ground
8	VCC	I	Power supply input
12	ANT	O	Module Antenna terminal, Default terminal

3 Typical Performance Characteristics

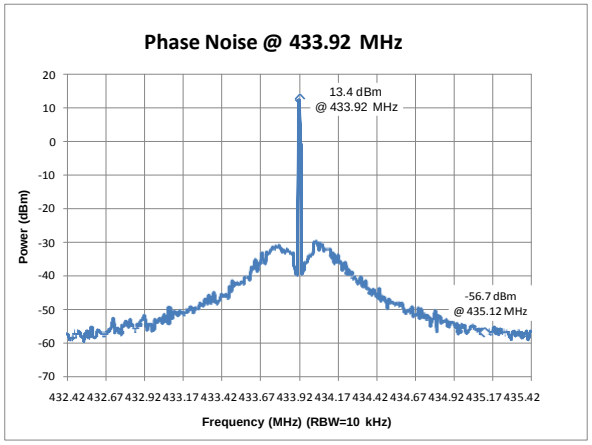


Figure 2. Phase Noise, F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm, Unmodulated

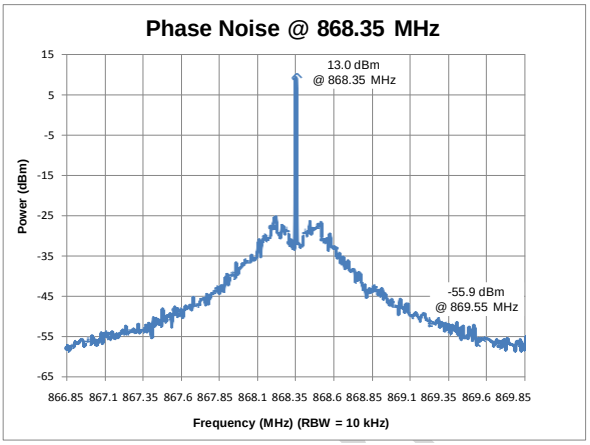


*Figure 3. Phase Noise, F_{RF} = 868.35 MHz, **P_{OUT} = +13 dBm, Unmodulated***

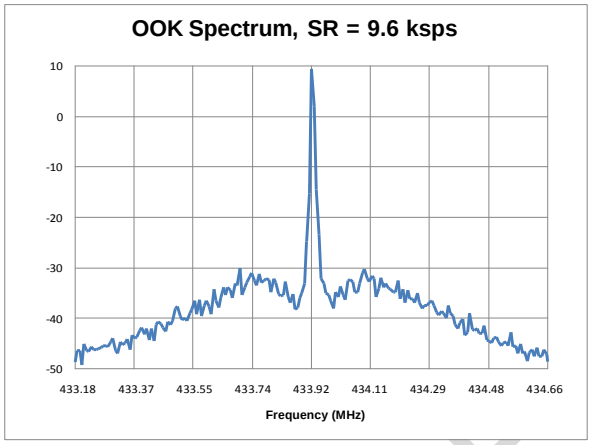


*Figure 4. OOK Spectrum, SR = 9.6 ksps **P_{OUT} = +10 dBm, t_{RAMP} = 32 us***

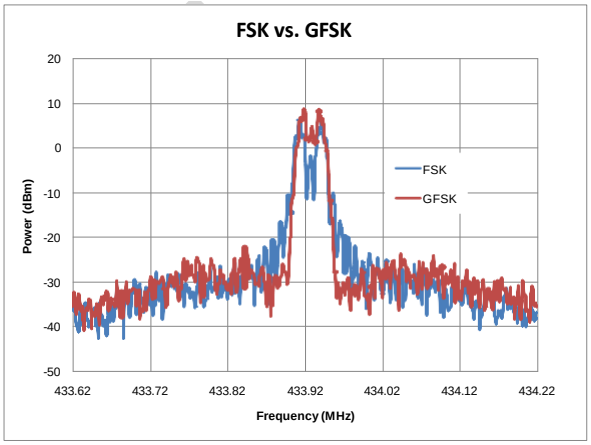


Figure 5. FSK/GFSK Spectrum, SR = 9.6 ksps, F_{DEV} = 15 kHz

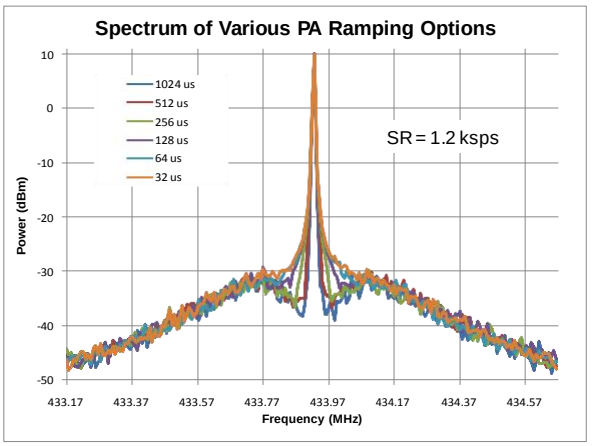


Figure 6. Spectrum of PA Ramping, SR = 1.2 ksps, P_{OUT} = +10 dBm

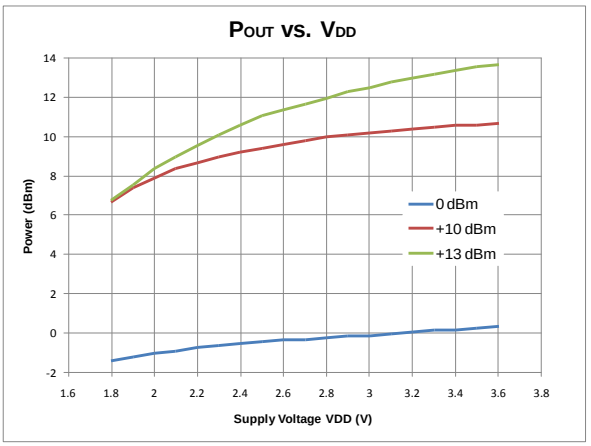


Figure 7. Output Power vs. Supply Voltages, F_{RF} = 433.92 MHz

4 Functional Descriptions

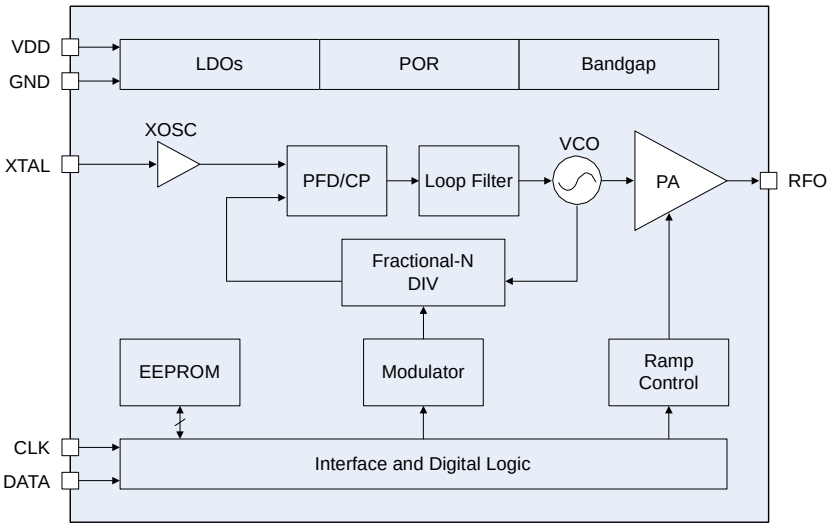


Figure 8. HC220 Functional Block Diagram

4.1 Overview

The HC220 is a high performance, highly flexible, low-cost, single-chip (G)FSK/OOK transmitter for various 240 to 960 MHz wireless applications. It is part of the NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the HC220 is shown in the figure above. The HC220 is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the internal voltage reference. The calibration can help the chip to finely work under different temperatures and supply voltages. The HC220 uses the DATA pin for the host MCU to send in the data. The input data will be modulated and sent out by a highly efficient PA, which output power can be configured from -10 to +13 dBm in 1 dB step size

The user can directly use the HC220 default configuration for immediate demands. If that cannot meet the system requirement, on-line register configuration and off-line EEPROM programming configuration are available for the user to customize the chip features. The on-line configuration means there is an MCU available in the application to configure the chip registers through the 2-wire interface, while the off-line configuration is done by the USB Programmer and the RFPDK. After the configuration is done, only the DATA pin is required for the host MCU to send in the data and control the transmission. The HC220 operates from 1.8 to 3.6 V so that it can finely work with most batteries to their useful power limits. It only consumes 15.5 mA (OOK @ 868.35 MHz) / 27.6 mA (FSK @ 868.35 MHz) when transmitting +10 dBm power under 3.3 V supply voltage.

4.2 Modulation, Frequency, Deviation and Symbol Rate

The HC220 supports GFSK/FSK modulation with the symbol rate up to 100 ksps, as well as OOK modulation with the symbol rate up to 30 ksps. The supported deviation of the (G)FSK modulation ranges from 1 to 200 kHz. The HC220 continuously covers the frequency range from 240 to 960 MHz, including the license free ISM frequency band around 315 MHz,
433.92 MHz, 868.35 MHz and 915 MHz. The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz when the frequency is less than 480 MHz, and is about 397 Hz

when the frequency is larger than 480 MHz. See the table below for the modulation, frequency and symbol rate specifications.

Table 6 Modulation, Frequency and Symbol Rate

Parameter	Value	Unit
Modulation	(G)FSK/OOK	-
Frequency	240 to 960	MHz
Deviation	1 to 200	kHz
Frequency Resolution (F_{RF} ≤ 480 MHz)	198	Hz
Frequency Resolution (F_{RF} > 480 MHz)	397	Hz
Symbol Rate (FSK/GFSK)	0.5 to 100	ksps
Symbol Rate (OOK)	0.5 to 30	ksps

4.3 Embedded EEPROM and RFPDK

The RFPDK (RF Products Development Kit) is a very user-friendly software tool delivered for the user configuring the HC220 in the most intuitional way. The user only needs to fill in/select the proper value of each parameter and click the "Burn" button to complete the chip configuration. See the figure below for the accessing of the EEPROM and Table 10 for the summary of all the configurable parameters of the HC220 in the RFPDK.

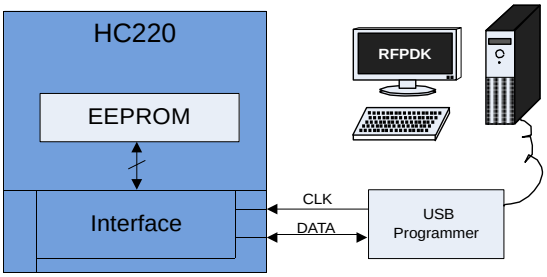


Figure 9. Accessing Embedded EEPROM

For more details of the USB Programmer and the RFPDK, please refer to "AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide". For the detail of HC220 configurations with the RFPDK, please refer to "AN122 CMT2113/19A Configuration Guideline".

Table 7 Configurable Parameters in RFPDK

Category	Parameters	Descriptions	Default	Mode
RF Settings	Frequency	To input a desired transmitting radio frequency in the range from 240 to 960 MHz. The step size is 0.001 MHz.	868.35 MHz	Basic Advanced
	Modulation	The option is FSK or GFSK and OOK.	FSK	Basic Advanced
	Deviation	The FSK frequency deviation. The range is from 1 to 100 kHz.	35 kHz	Basic Advanced
	Symbol Rate	The GFSK symbol rate. The user does not need to specify symbol rate for FSK and OOK modulation.	2.4 ksps	Basic Advanced
	Tx Power	To select a proper transmitting output power from -10 dBm to +14 dBm, 1 dB margin is given above +13 dBm.	+13 dBm	Basic Advanced
	Xtal Load	On-chip XOSC load capacitance options: from 10 to 22 pF. The step size is 0.33 pF.	15 pF	Basic Advanced
	Data Representation	To select whether the frequency "Fo + Fdev" represent data 0 or 1. The options are: 0: F-high 1: F-low, or 0: F-low 1: F-high.	0: F-low 1: F-high	Advanced
	PA Ramping	To control PA output power ramp up/down time for OOK transmission, options are 0 and 2^n us (n from 0 to 10).	0 us	Advanced
Transmitting Settings	Start by	Start condition of a transmitting cycle, by Data Pin Rising/Falling Edge.	Data Pin Rising Edge	Advanced
	Stop by	Stop condition of a transmitting cycle, by Data Pin Holding Low for 2 to 90 ms.	Data Pin Holding Low for 20 ms	Advanced

4.4 On-line Register Configuration

The on-line register configuration means there is an MCU available in the application to configure the chip registers through the TWI: CLK and DATA. The value of the registers, which is originally copied from the EEPROM at the chip's power-up, will remain its value until part or all of the registers are modified by the host MCU. The register value will be lost after the chip's power-down, and re-configuration is necessary when it is powered up again.

For the detail of the on-line register configuration flow, please refer to Chapter 7.

4.5 Power Amplifier

A highly efficient single-ended Power Amplifier (PA) is integrated in the HC220 to transmit the modulated signal out. Depending on the application, the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in "Chapter 4 Typical Application Schematic". For the schematic, layout guideline and the other detailed information please refer to "AN101 CMT211xA Schematic and PCB Layout Design Guideline".

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the USB Programmer and RFPDK.

4.6 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The HC220 has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 13. These options are only available when the modulation type is OOK. When the option is set to “0”, the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping “rate”, as shown in the formula below.

$$SR_{Max} \leq 0.5 * \left(\frac{1}{t_{RAMP}}\right)$$

In which the PA ramping “rate” is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by formula below.

$$t_{RAMP} \leq 0.5 * \left(\frac{1}{SR_{MAX}}\right)$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than "0.5 * (1/SR_{Max})", it will possibly bring additional challenges to the OOK demodulation of the Rx device. For more detail of calculating t_{RAMP}, please refer to "AN122 CMT2113/19A Configuration Guideline".

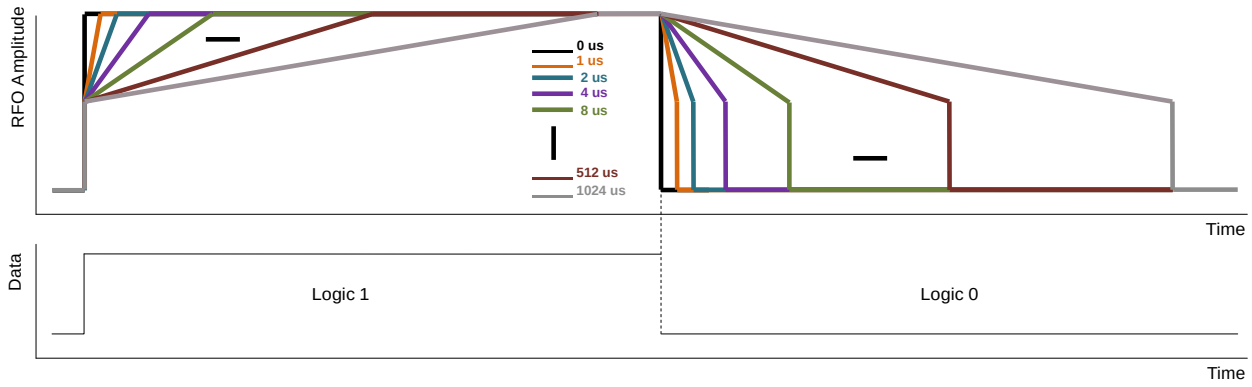


Figure 10. PA Ramping Time

5 Working States and Transmission Control Interface

5.1 Working States

The HC220 has following 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the HC220 is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized to 20 nA typically.

XO-STARTUP

After detecting a valid control signal on DATA pin, the HC220 goes into the XO-STARTUP state, and the internal XO starts to work. The valid control signal can be a rising or falling edge on the DATA pin, which can be configured on the RFPDK. The host MCU has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in the Table 11.

TUNE

The frequency synthesizer will tune the HC220 to the desired frequency in the time t_{TUNE}. The PA can be turned on to transmit the incoming data only after the TUNE state is done, before that the incoming data will not be transmitted. See Figure 16 and Figure 17 for the details.

TRANSMIT

The HC220 starts to modulate and transmit the data coming from the DATA pin. The transmission can be ended in 2 methods: firstly, driving the DATA pin low for t_{STOP} time, where the t_{STOP} can be configured from 20 to 90 ms on the RFPDK; secondly, issuing SOFT_RST command over the two-wire interface, this will stop the transmission in 1 ms. See Section 6.2.3 for details of the two-wire interface.

Table 8 Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop the Transmission[2]	t_{STOP}	2		90	ms

Notes:
[1]. This parameter is to a large degree crystal dependent.
[2]. Configurable from 2 to 9 in 1 ms step size and 20 to 90 ms in 10 ms step size.

5.2 Transmission Control Interface

The HC220 uses the DATA pin for the host MCU to send in data for modulation and transmission. The DATA pin can be used as pin for EEPROM programming, data transmission, as well as controlling the transmission. The transmission can be started by detecting rising or falling edge on the DATA pin, and stopped by driving the DATA pin low for t_{STOP} as shown in the table above. Besides communicating over the DATA pin, the host MCU can also communicate with the device over the two-wire interface, so that the transmission is more robust, and consumes less current.

Please note that the user is recommended to use the Tx Enabled by DATA pin Rising Edge, which is described in Section 6.2.1.

5.2.1 Tx Enabled by DATA Pin Rising Edge

As shown in the figure below, once the HC220 detects a rising edge on the DATA pin, it goes into the XO-STARTUP state. The user has to pull the DATA pin high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the DATA pin. The logic state of the DATA pin is "Don't Care" from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission.

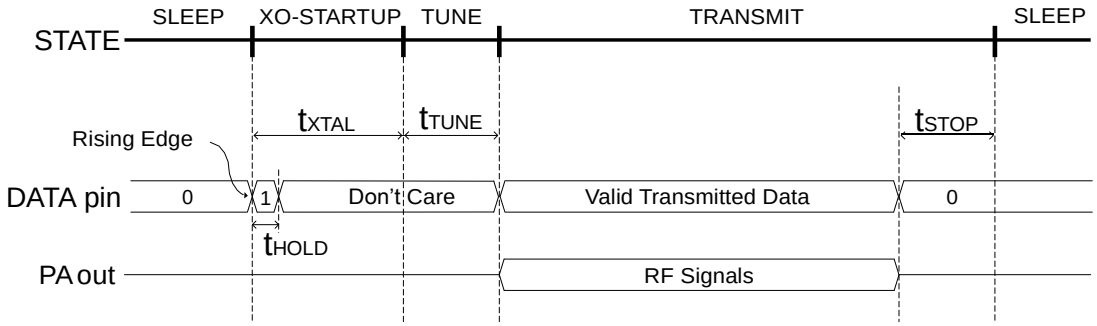


Figure 13. Transmission Enabled by DATA Pin Rising Edge

5.2.2 Tx Enabled by DATA Pin Falling Edge

As shown in the figure below, once the HC220 detects a falling edge on the DATA pin, it goes into XO-STARTUP state and the XO starts to work. During the XO-STARTUP state, the DATA pin needs to be pulled low. After the XO is settled, the HC220 goes to the TUNE state. The logic state of the DATA pin is "Don't Care" during the TUNE state. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the DATA pin low for t_{STOP} in order to end the transmission. Before starting the next transmit cycle, the user has to pull the DATA pin back to high.

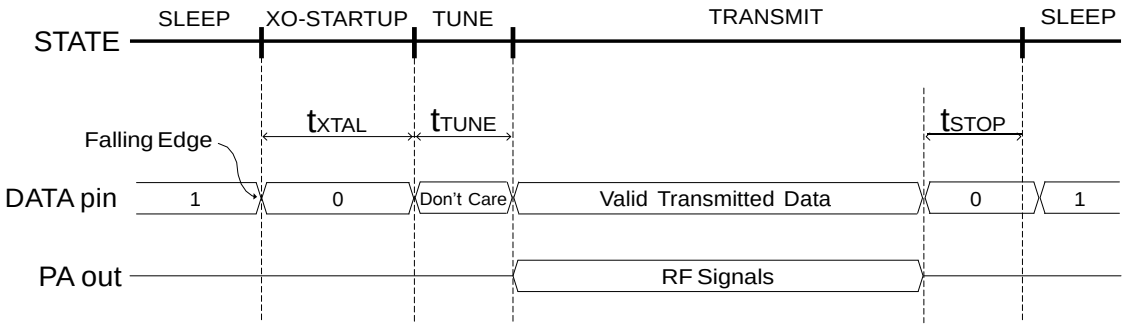


Figure 14. Transmission Enabled by DATA Pin Falling Edge

5.2.3 Two-wire Interface

For power-saving and reliable transmission purposes, the HC220 is recommended to communicate with the host MCU over a two-wire interface (TWI): DATA and CLK. The TWI is designed to operate at a maximum of 1 MHz. The timing requirement and data transmission control through the TWI are shown in this section.

Table 9 TWI Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	V_{IH}		0.8			V_{DD}
Digital Input Level Low	V_{IL}				0.2	V_{DD}
CLK Frequency	F_{CLK}		10		1,000	kHz
CLK High Time	t_{CH}		500			ns
CLK Low Time	t_{CL}		500			ns
CLK Delay Time	t_{CD}	CLK delay time for the first falling edge of the TWI_RST command, see Figure 20	20		15,000	ns
DATA Delay Time	t_{DD}	The data delay time from the last CLK rising edge of the TWI command to the time DATA return to default state			15,000	ns
DATA Setup Time	t_{DS}	From DATA change to CLK falling edge	20			ns
DATA Hold Time	t_{DH}	From CLK falling edge to DATA change	200			ns

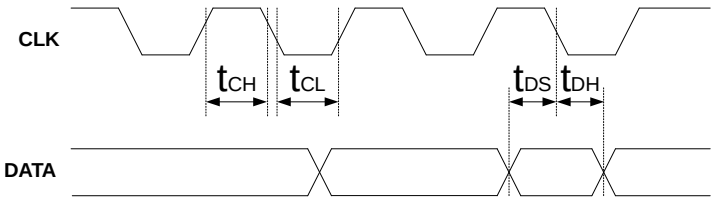


Figure 15. Two-wire Interface Timing Diagram

Once the device is powered up, TWI_RST and SOFT_RST should be issued to make sure the device works in SLEEP state robustly. On every transmission, TWI_RST and TWI_OFF should be issued before the transmission to make sure the TWI circuit functions correctly. TWI_RST and SOFT_RST should be issued again after the transmission for the device going back to SLEEP state reliably till the next transmission. The operation flow with TWI is shown as the figure below.

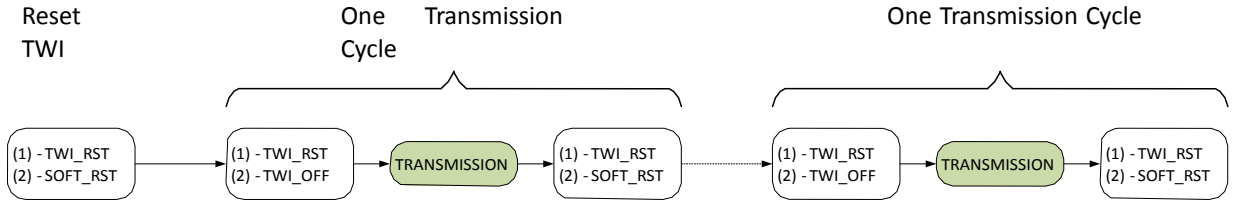


Figure 16. HC220 Operation Flow with TWI

Table 10 TWI Commands Descriptions

Command	Descriptions
TWI_RST	Implemented by pulling the DATA pin low for 32 clock cycles and clocking in 0x8D00, 48 clock cycles in total. It only resets the TWI circuit to make sure it functions correctly. The DATA pin cannot detect the Rising/Falling edge to trigger transmission after this command, until the TWI_OFF command is issued. **Notes:** 1. Please ensure the DATA pin is firmly pulled low during the first 32 clock cycles. 2. When the device is configured as Transmission Enabled by DATA Pin Falling Edge, in order to issue the TWI_RST command correctly, the first falling edge of the CLK should be sent t_{CD} after the DATA

Command	Descriptions
	as shown in Figure 20. 3. When the device is configured as Transmission Enabled by DATA Pin Rising Edge, the default state of the DATA is low, there is no t_{CD} requirement, as shown in Figure 21.
TWI_OFF	Implemented by clocking in 0x8D02, 16 clock cycles in total. It turns off the TWI circuit, and the DATA pin is able to detect the Rising/Falling edge to trigger transmission after this command, till the TWI_RST command is issued. The command is shown as Figure 22.
SOFT_RST	Implemented by clocking in 0xBD01, 16 clock cycles in total. It resets all the other circuits of the chip except the TWI circuit. This command will trigger internal calibration for getting the optimal device performance. After issuing the SOFT_RST command, the host MCU should wait 1 ms before sending in any new command. After that, the device goes to SLEEP state. The command is shown as Figure 23.

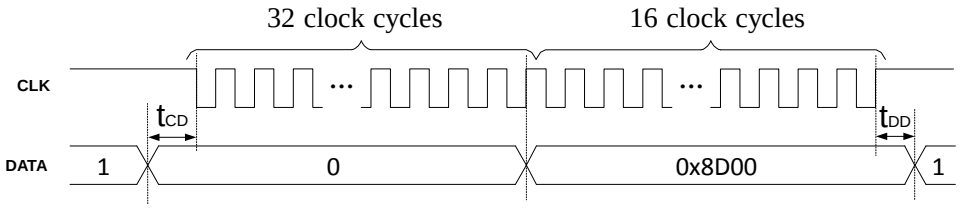


Figure 17. TWI_RST Command When Transmission Enabled by DATA Pin Falling Edge

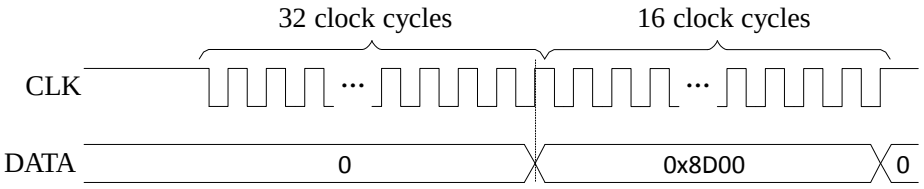


Figure 18. TWI_RST Command When Transmission Enabled by DATA Pin Rising Edge

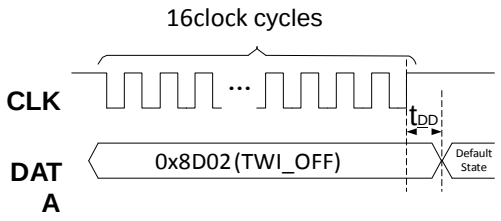


Figure 19. TWI_OFF Command

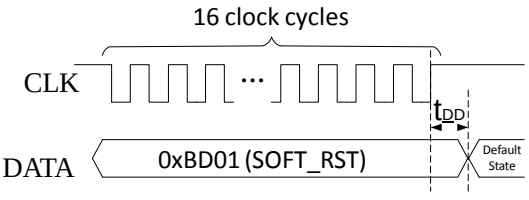


Figure 23. SOFT_RST Command

The DATA is generated by the host MCU on the rising edge of CLK, and is sampled by the device on the falling edge. The CLK should be pulled up by the host MCU during the TRANSMISSION shown in Figure 19. The TRANSMISSION process should refer to Figure 16 or Figure 17 for its timing requirement, depending on the "Start By" setting configured on the RFPDK.

The device will go to SLEEP state by driving the DATA low for t_{STOP}, or issuing SOFT_RST command. A helpful practice for the device to go to SLEEP is to issue TWI_RST and SOFT_RST commands right after the useful data is transmitted, instead of waiting the t_{STOP}, this can save power significantly.

6 On-Line Register Configuration Flow

Besides off-line EEPROM programming to tailor the chip features, on-line register configuration through the two-wire interface can do the work in another way, which is mentioned in Section 5.4. This chapter gives more details on accessing chip registers with TWI.

6.1 Accessing Registers with TWI

The TWI includes an input port CLK and a bi-directional port DATA. A complete Write/Read (W/R) process has 16 clock cycles. For the first 8 clock cycles, the DATA is used as input port for writing register address; and for the last 8 clock cycles, the DATA is used as input port during write process, and output port during read process. The timing chart for the TWI W/R is shown as the figure below. Please note that the TWI_RST command is a special command which does not apply to the guidelines introduced below. The TWI_RST command is introduced in Table 13, Figure 20 and Figure 21in details.

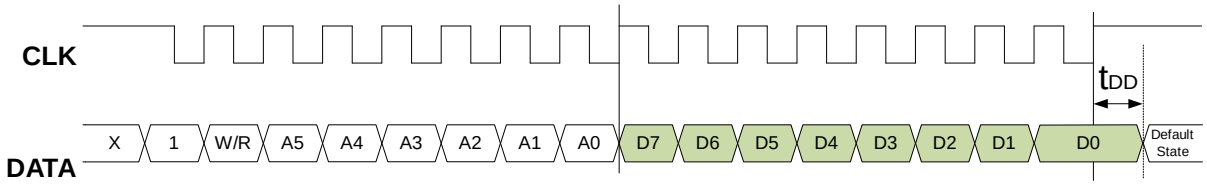


Figure 20. TWI W/R Timing Chart (Except for TWI_RST Command)

Notes:

1. The timing requirement is shown as Table 12.
2. At the end of each command, the DATA should return to its default state after the last CLK rising edge within the time t_{DD}.
3. The command always start with “1”, the first 8 clock cycle includes the W/R control and address bits A[5:0]. It is a Read command when W/R is 1, and Write command when W/R is 0. The range of the address bits is from 0x00 to 0x3F.
4. In a Write command, D[7:0] is the data to be written into the register. In a Read command, D[7:0] is the data to be read from the register.
5. The DATA pin is a bi-directional port, and it will be switched to output port in the last 8 clock cycle of a Read command. At this time, the host MCU should switch the corresponding port which is connected to the DATA pin to input port at the coming CLK rising edge, shown as dash line in the middle of Figure 24, so that there is no voltage conflict between the two ports and the read out function is correctly behaved.
6. To simplify the expression, this datasheet is using the TWI_WRREG and TWI_RDREG to represent the write and read command to specified registers, as shown in the table below.

Table 11 TWI_WRREG and TWI_RDREG

Command	Description
TWI_WRREG	TWI write command. TWI_WRREG(XX, YY) means clocking in 16b’10xx xxxx yyyy yyyy, which xx xxxx is the register address to be written, ranging from 0x00 to 0x3F; yyyy yyyy is the register content to be written ranging from 0x00 to 0xFF. For example, TWI_WRREG(0x12, 0xAA) means clocking in 0x92AA.
TWI_RDREG	TWI read command, TWI_RDREG(XX, ZZ) means clocking in 8b’11xx xxxx and read out zzzz zzzz, which xx xxxx is the register address to be written, ranging from 0x00 to 0x3F; zzzz zzzz is the read out value from the register, ranging from 0x00 to 0xFF For example, TWI_RDREG(0x2A, DAT), means clocking in 0xEA, and read out DAT which is an 8-bit value.

7. Specific commands TWI_RST, TWI_OFF and SOFT_RST are also used in the on-line register configuration, refer to Table 13 for the definition of the 3 commands.

6.2 Configuration Flow

The user should follow below flow chart for the on-line register configuration.

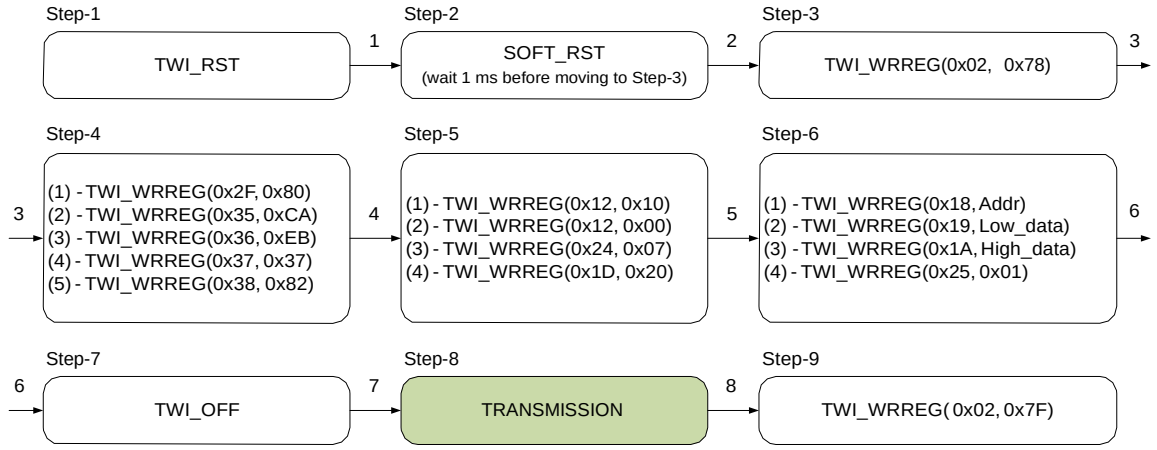


Figure 21. On-line Register Configuration Flow

Notes:

1. In step-2, the host MCU issues the SOFT_RST command and needs to wait 1 ms before moving to step-3.
2. The feature registers are 16-bit wide, which address is indicated as Addr in step-6. The host MCU needs to first write the Addr to register 0x18. After that, the host MCU divides the feature register content into two 8-bit parts: Low_data and High_data, then write them into two temporary registers, which addresses are 0x19 and 0x1A, and finally overwrite the target 16-bit register by issuing TWI_WRREG(0x25, 0x1) to complete the feature register writing, as shown in step-6. Repeat step-6 if multiple feature registers are need to configured.

   For example, if the user wants to write 0xC3F6 to feature register which address is 0x02, the user should issue the commands shown in step-6, and listed as below.

   a) TWI_WRREG(0x18, 0x02); // Write the Addr 0x02 to register 0x18
   b) TWI_WRREG(0x19, 0xF6); // Write the Low_data 0xF6 to register 0x19
   c) TWI_WRREG(0x1A, 0xC3); // Write the High_data 0xC3 to register 0x1A
   d) TWI_WRREG(0x25, 0x01); // Trigger the overwriting to the feature register, the writing process completes

3. As a specific feature could be related to several registers, in order to change the feature correctly, the user is recommended to find out the corresponding registers by Export function on the RFPDK, as shown in Figure 26 . For more RFPDK details, refer to “AN103 CMT211xA-221xA One-Way RF Link Development Kits Users Guide”. An example of changing the frequency from 433.92 MHz to 868 MHz is listed below.

   a) Configure the device to work in 433.92 MHz, use the Export function on the RFPDK to generate the configuration file named as 433.92MHz.exp.
   b) Configure the device to work in 868 MHz, generate the configuration file named as 868MHz.exp in the same way.
   c) Compare the 868MHz.exp file with the 433.92MHz.exp file and find out the registers being changed, as shown in Figure 27. Please note that the address of the registers starts from 0x00 and ends at 0x15 (21 registers in total).
   d) Apply the corresponding register value and address in the flow shown in Figure 25.

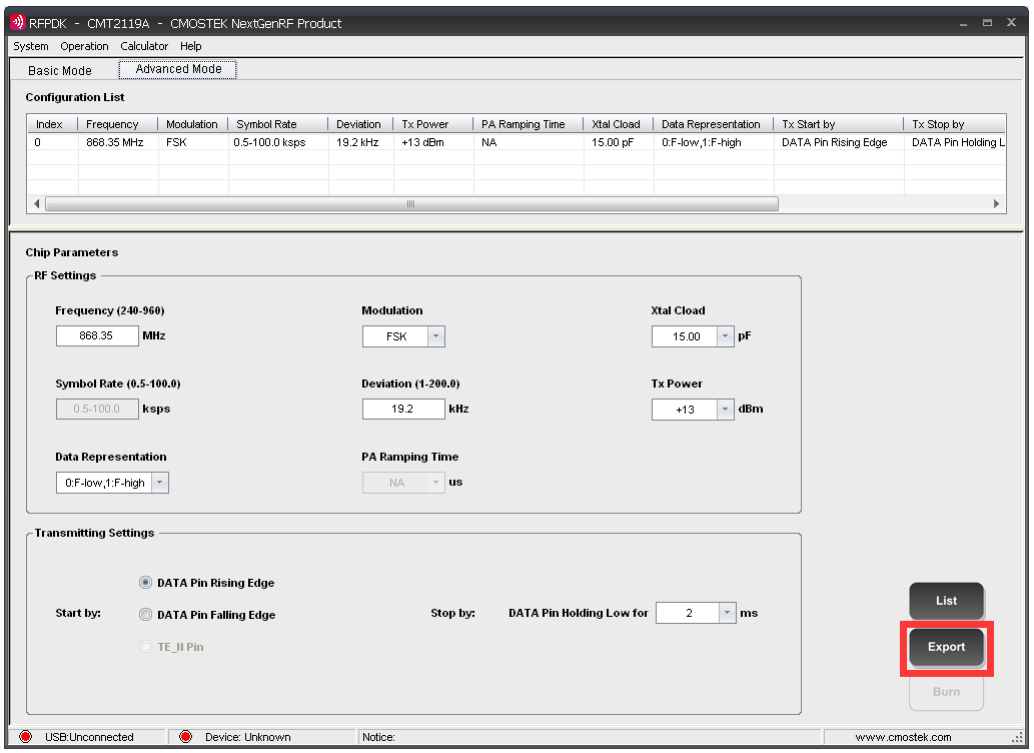


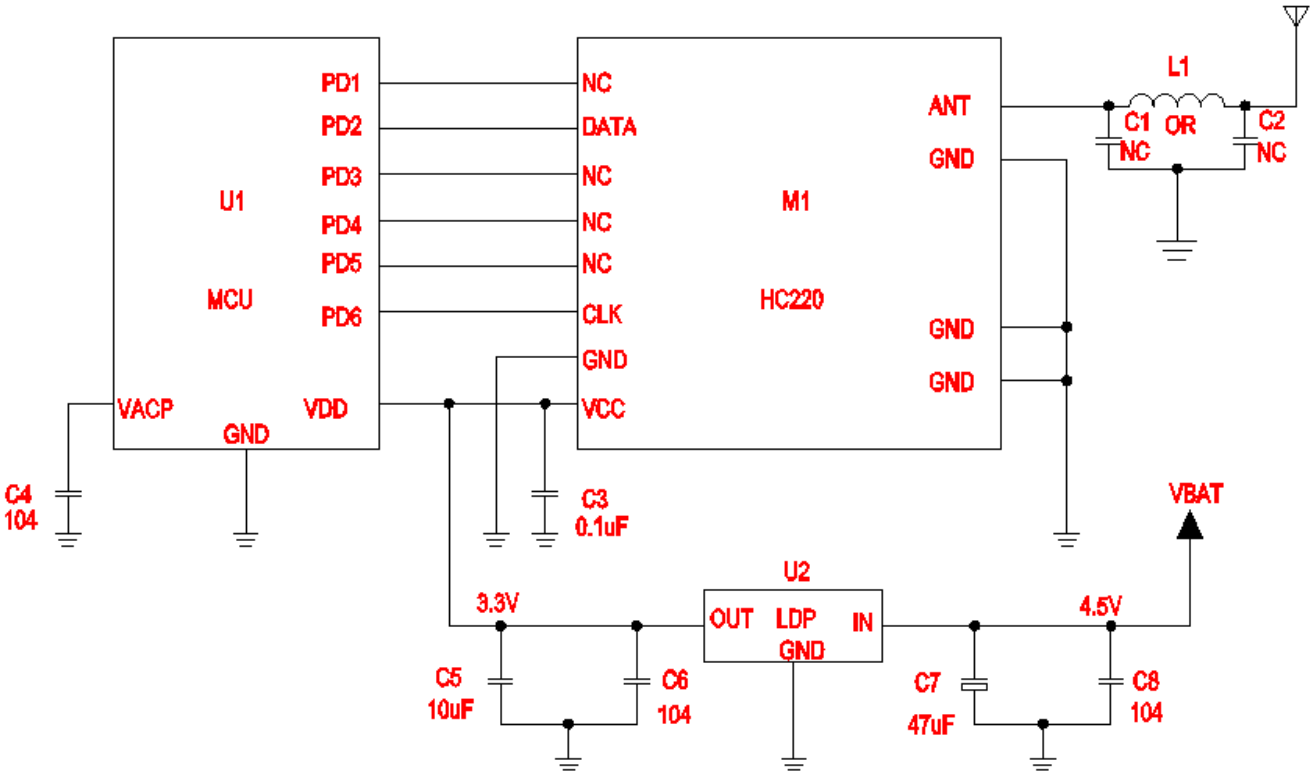
Figure 22. Export Button on the RFPDK

```
;  CMT2119A Configuration File
;  Generated by CMOSTEK RFPDK
;  2014.12.22 17:22
;----------------------------------------
;  Mode                = Advanced
;  Part Number         = CMT2119A
;  Frequency           = 433.92 MHz
;  Modulation          = FSK
;  Symbol Rate         = 0.5-100.0 ksps
;  Tx Power            = +13 dBm
;  Deviation           = 19.2 kHz
;  PA Ramping Time     = NA
;  Xtal Cload          = 15.00 pF
;  Data Representation = 0:F-low,1:F-high
;  Tx Start by         = DATA Pin Rising Edge
;  Tx Stop by          = DATA Pin Holding Low For 2 ms
;----------------------------------------
;  The following are the EEPROM contents
;----------------------------------------
0x007F
0x5400
0x0000
0x0000
0x0000
0xF000
0x0000
0xC1C5
0x4200
0x00BF
0x2401
0x0081
0x8000
0x0000
0xFFFF
0x0020
0x5FD9
0xB6D6
0x0E13
0x0019
0x0000
;----------------------------------------
```

```
;  CMT2119A Configuration File
;  Generated by CMOSTEK RFPDK
;  2014.12.22 17:14
;----------------------------------------
;  Mode                = Advanced
;  Part Number         = CMT2119A
;  Frequency           = 868.00 MHz
;  Modulation          = FSK
;  Symbol Rate         = 0.5-100.0 ksps
;  Tx Power            = +13 dBm
;  Deviation           = 19.2 kHz
;  PA Ramping Time     = NA
;  Xtal Cload          = 15.00 pF
;  Data Representation = 0:F-low,1:F-high
;  Tx Start by         = DATA Pin Rising Edge
;  Tx Stop by          = DATA Pin Holding Low For 2 ms
;----------------------------------------
;  The following are the EEPROM contents
;----------------------------------------
0x007F
0x5000
0x0000
0x0000
0x0000
0xF000
0x0000
0xC4EC
0x4200
0x005F
0x2401
0x0081
0x8000
0x0000
0xFFFF
0x0020
0x5F1E
0xB6D6
0x0E13
0x0019
0x0000
;----------------------------------------
```

Figure 23. Examples of Changing Frequency

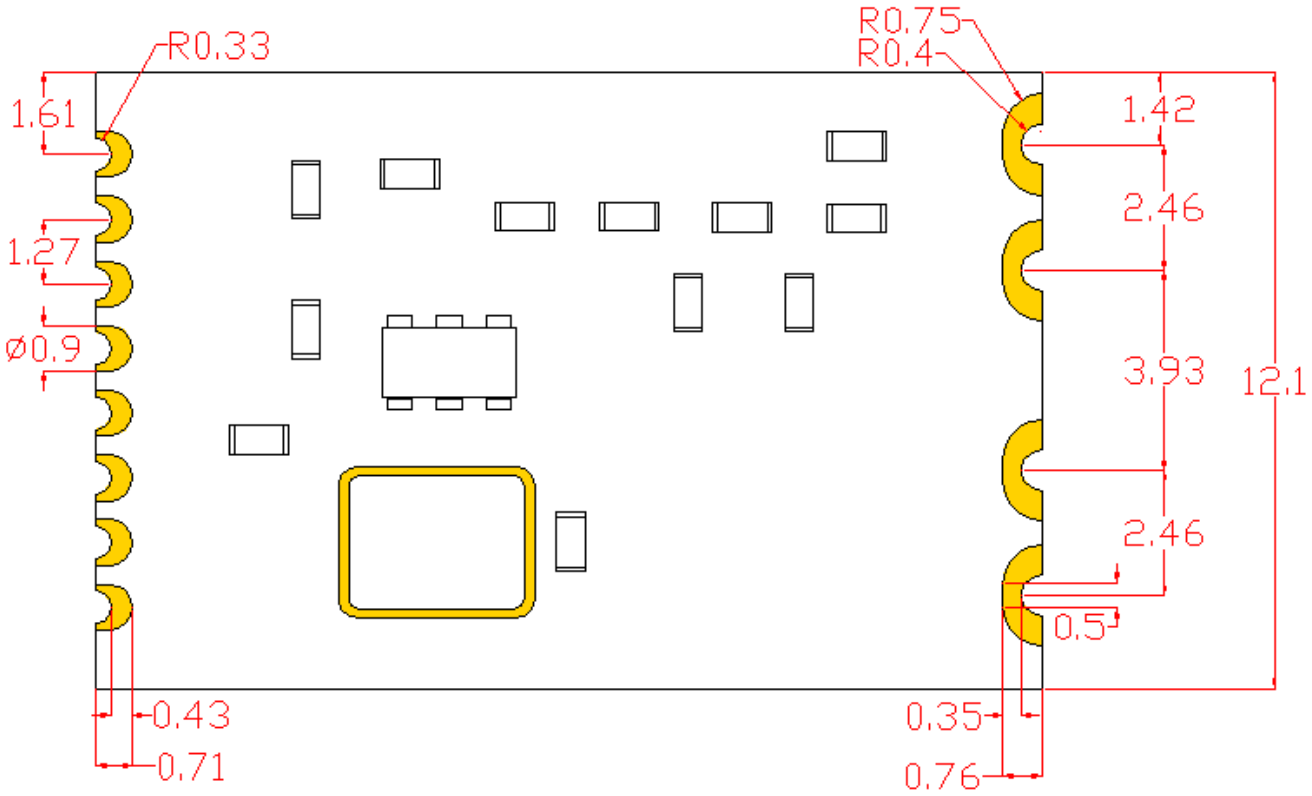
7 Application Information

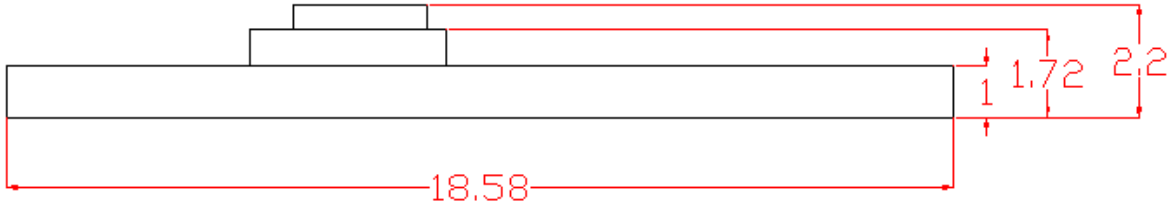


Designator	Descriptions	Manufacturer
M1	Module HC220 18.58*12.1*2.2mm RoHS	LJ ELECTRONICS
U1	IC 8 BIT MCU STM8S003F3 SSOP20 RoHS	MICROICHIP
U2	IC LDO XC6206P33PR 3.3V SOT-23 RoHS	TOREX
L1	Thick film resistor0R 5% 1/16W 0402 RoHS	ROHM
C1	CAP CER 0402 DO NOT FIT	
C2	CAP CER 0402 DO NOT FIT	
C3	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C4	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C5	CAP CER 10uF/16V 20% X5R 0402 RoHS	MURATA
C6	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA
C7	CAP CER 47uF/16V 20% X5R 1206 RoHS	MURATA
C8	CAP CER 0.1uF/25V 20% X7R 0402 RoHS	MURATA

8 Module Package OutlineDrawing

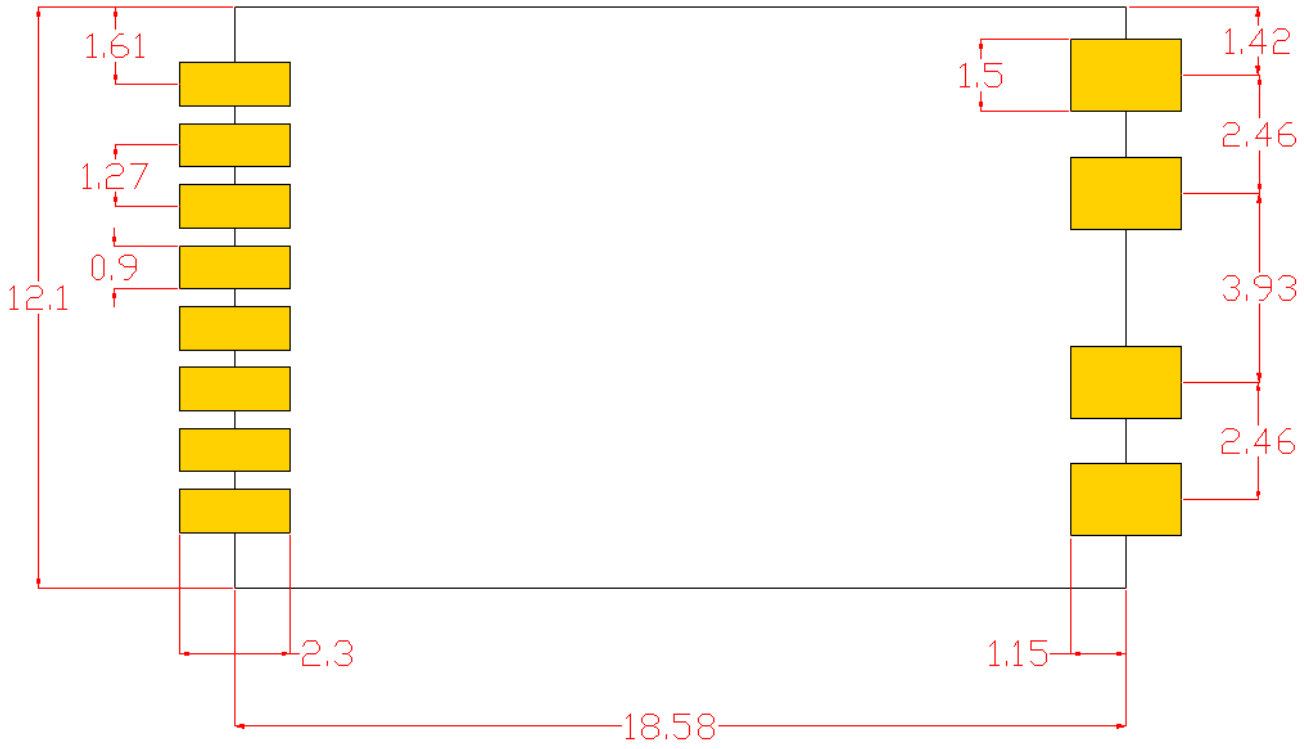
Unit: mm





9 Recommended PCB Land Pattern

Unit: mm



10 Tray Packaging

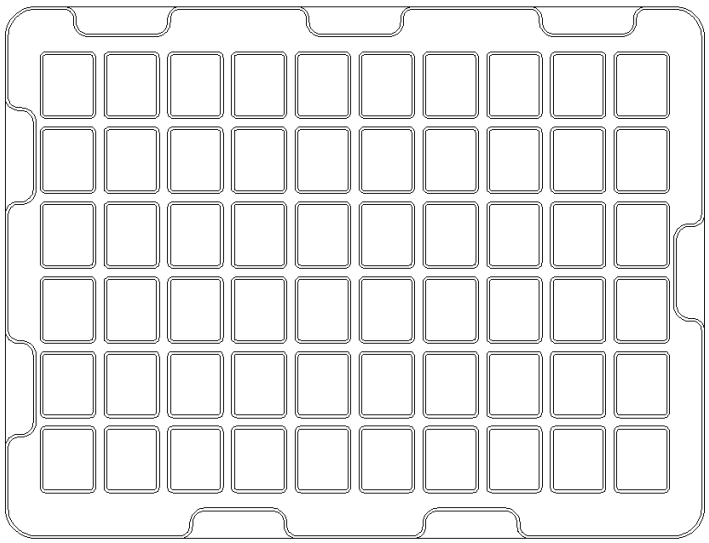
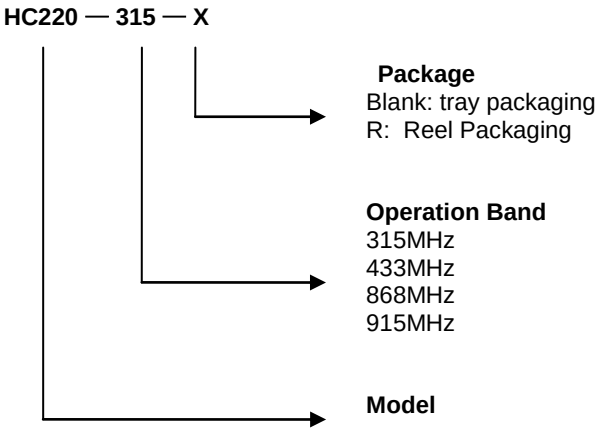


Figure 24. Package Outline Drawing

Note:

tray packaging, 60pcs/tray.

11 Ordering Information:



12 Module Revisions:

Table 12 Revision History

Revisions	Date	Updated History
Rev1.0	Nov 2017	The first final release
Rev1.1	Jun 2018	Add product pictures

13 Contact us:

LJ ELECTRONICS TECHNOLOGY LIMITED

Address: The 2nd Floor (west side),JieAn Industrial Park, The 1st Industrial Road,

TuTang Village,ChangPing Town,DongGuan City, GuangDong, China

TEL: 0769-81096302 0769-81096303 FAX: 0769-81096306

E-mail: sales@ljelect.com

Http://www. ljelect.com