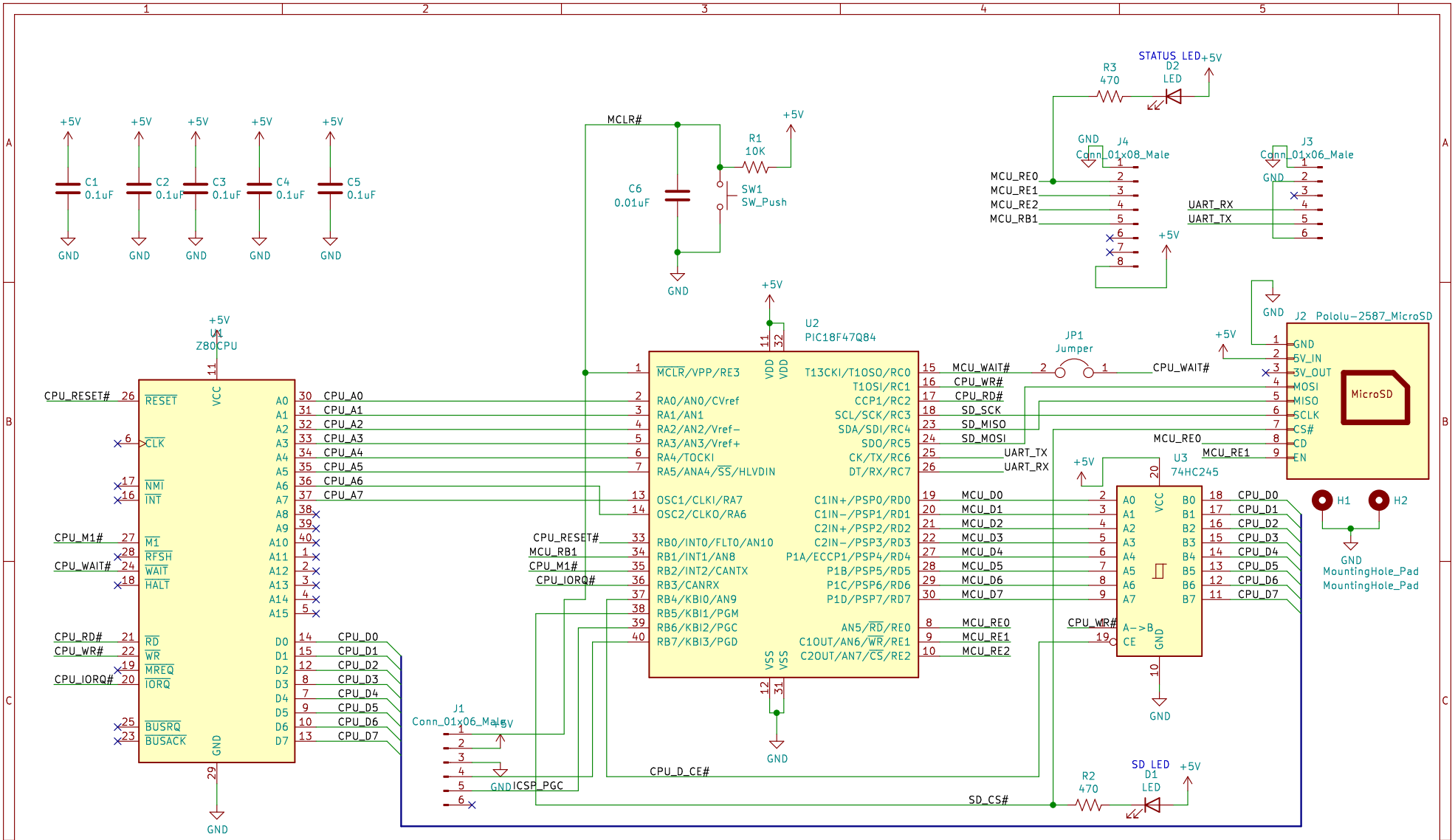


**CLC1**

CLCIN5 = CPU_A7
CLCIN4 = CPU_A6
CLCIN1 = CPU_A5
CLCIN0 = CPU_A4

CLCOUT1 = ADDR Match

**CLC2**

CLCIN2 = CPU_IORQ# = RB3
CLCOUT1 = Address Match
CLCIN6 = CPU_M1# = RB2
CLCIN7 = RB1

CLCOUT2 = WAIT# = RC0

**CLC3**

Same inputs as CLC2

CLCOUT3 = CPU_D_CE# = RB4

# Z80 SSD Controller

(c) 2021, Howard M. Harte – WZ2Q
https://github.com/hharte/z80_ssd

Sheet: /
File: z80_ssd.sch

**Title:**

| | | |
|---|---|---|
| Size: A | Date: October 23, 2021 | Rev: 1 |
| KiCad E.D.A. kicad (5.1.10)-1 | | Id: 1/1 |