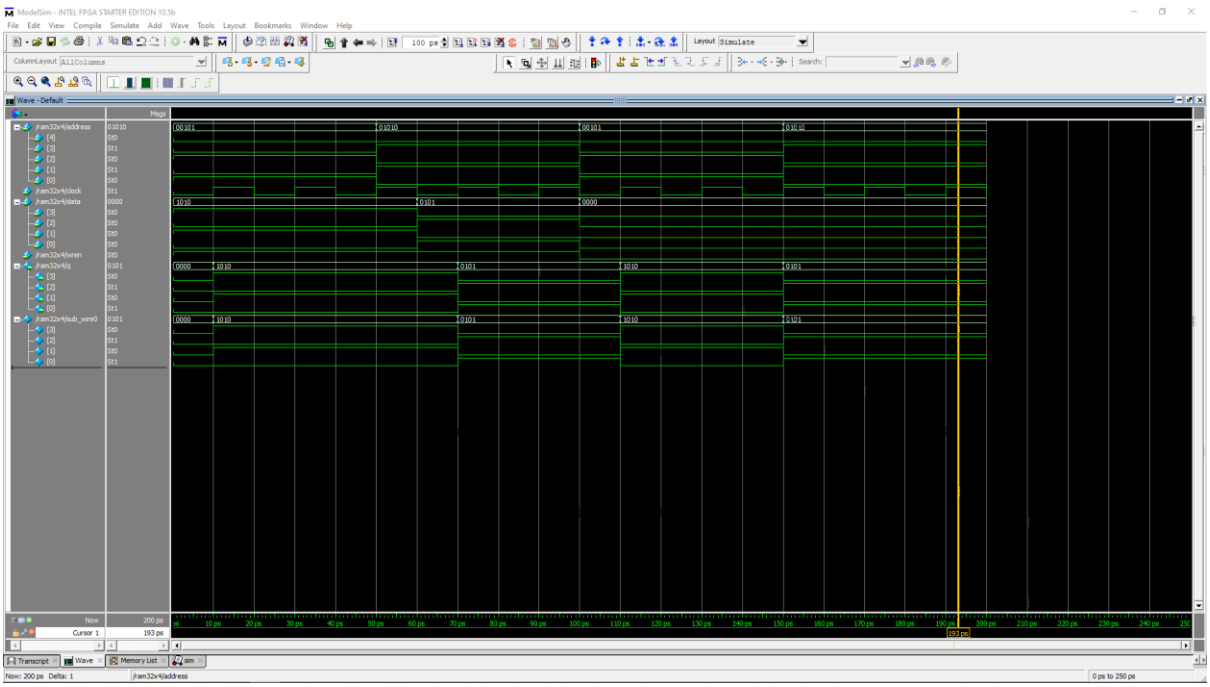
Part I:

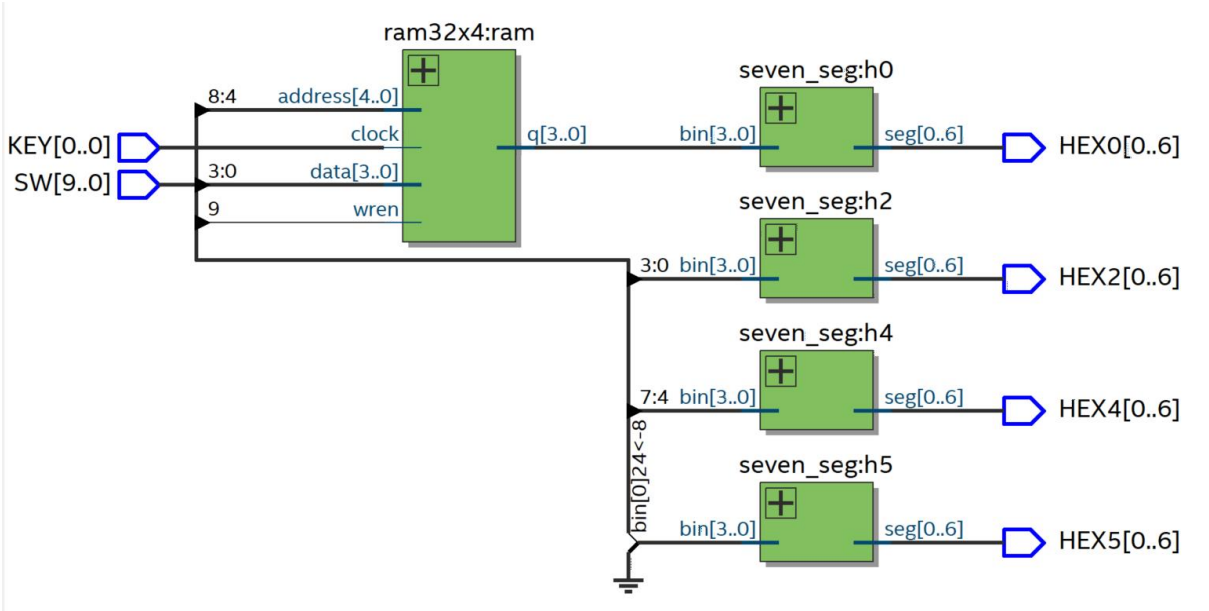
Ram module created and is attached in top level file.

9.



Simulation for the ram module.

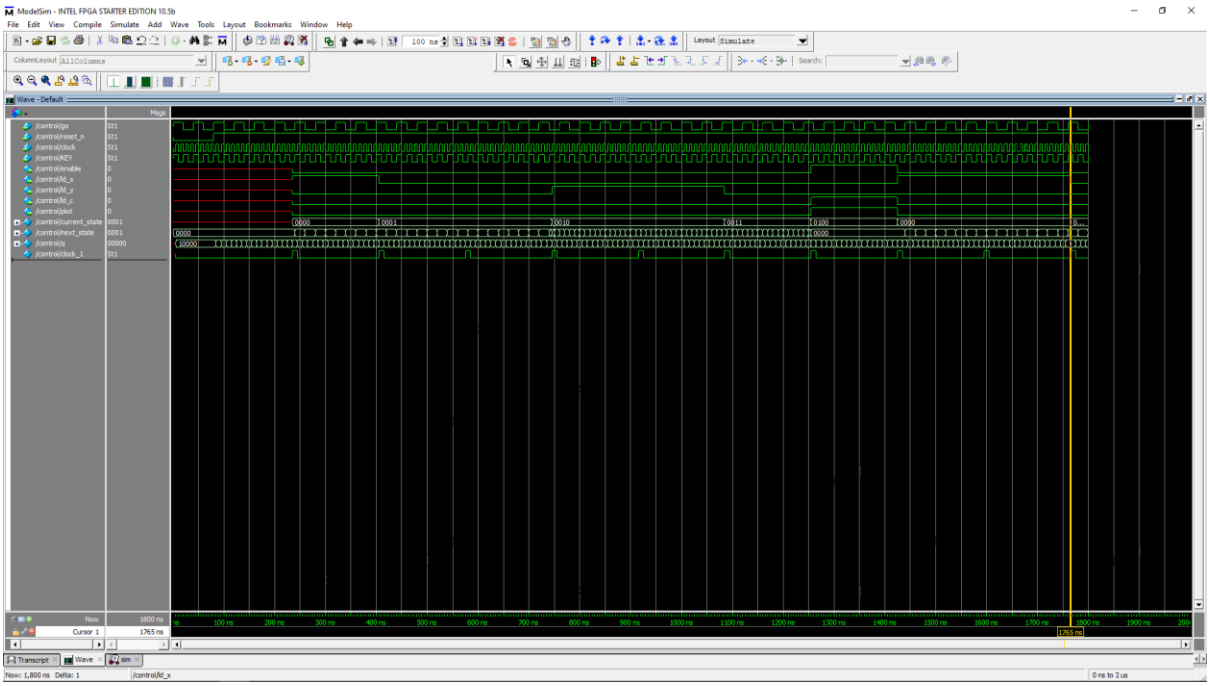
11.



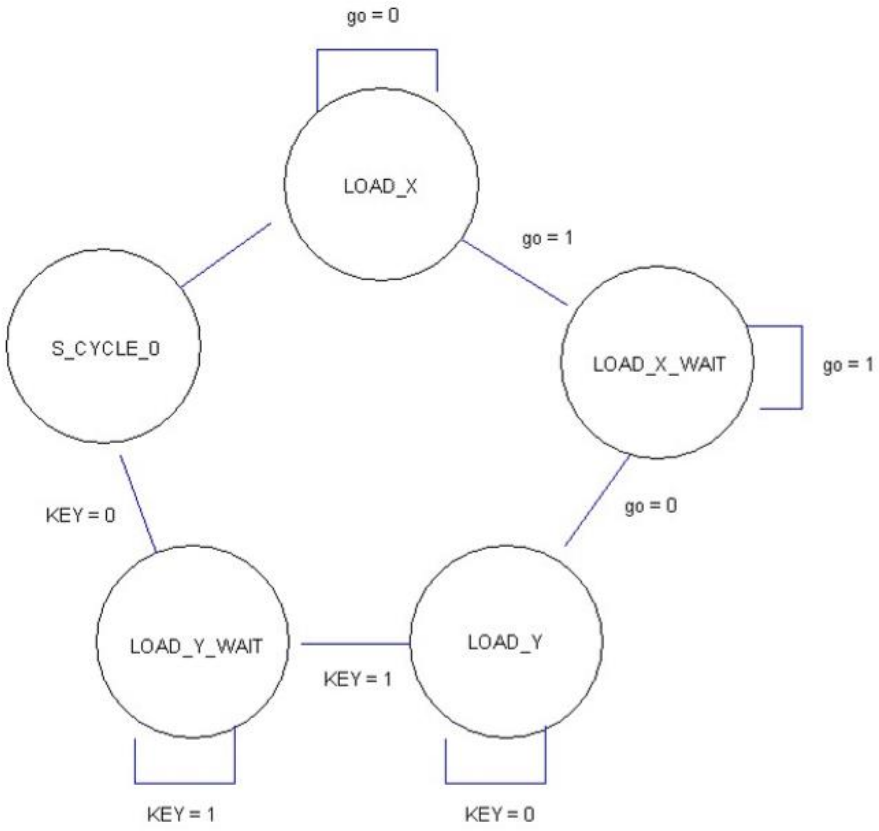
Schematic for the circuit, with the Keys and switches connected to relevant modules.

Part II:

1. Code submitted on Quercus.
   Simulation image:



2. State diagram:



State table:

F_n	GO	KEY	F_{n+1}
LOAD_X	0		LOAD_X
LOAD_X	1		LOAD_X_WAIT
LOAD_X_WAIT	0		LOAD_Y
LOAD_X_WAIT	1		LOAD_X_WAIT
LOAD_Y		0	LOAD_Y
LOAD_Y		1	LOAD_Y_WAIT
LOAD_Y_WAIT		0	S_CYCLE_0
LOAD_Y_WAIT		1	LOAD_Y_WAIT
S_CYCLE_0			LOAD_X
S_CYCLE_0			LOAD_X

Simulation of combined circuit: