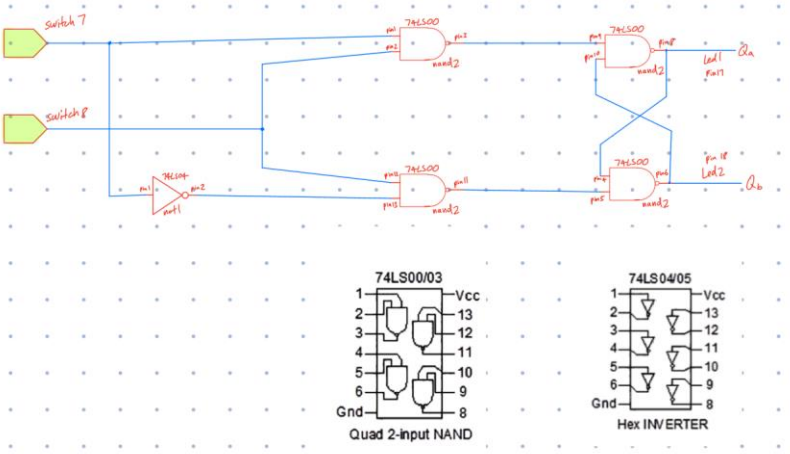
Part I:

1. 

Digital Board Header Pin Assignment

Pin#	Description		Description	Pin#
1	Switch #1		Switch #2	2
3	Switch #3		Switch #4	4
5	Switch #5		Switch #6	6
7	Switch #7		Switch #8	8
9	Ground		NC	10
11	Ground		NC	12
13	Ground		NC	14
15	Ground		NC	16
17	LED #1		LED #2	18
19	LED #3		LED #4	20
21	LED #5		LED #6	22
23	LED #7		LED #8	24
25	Ground		NC	26
27	Ground		NC	28
29	Ground		NC	30
31	Ground		NC	32
33	Clock		NC	34
35	NC		NC	36
37	NC		Pulse Button	38
39	NC		NC	40

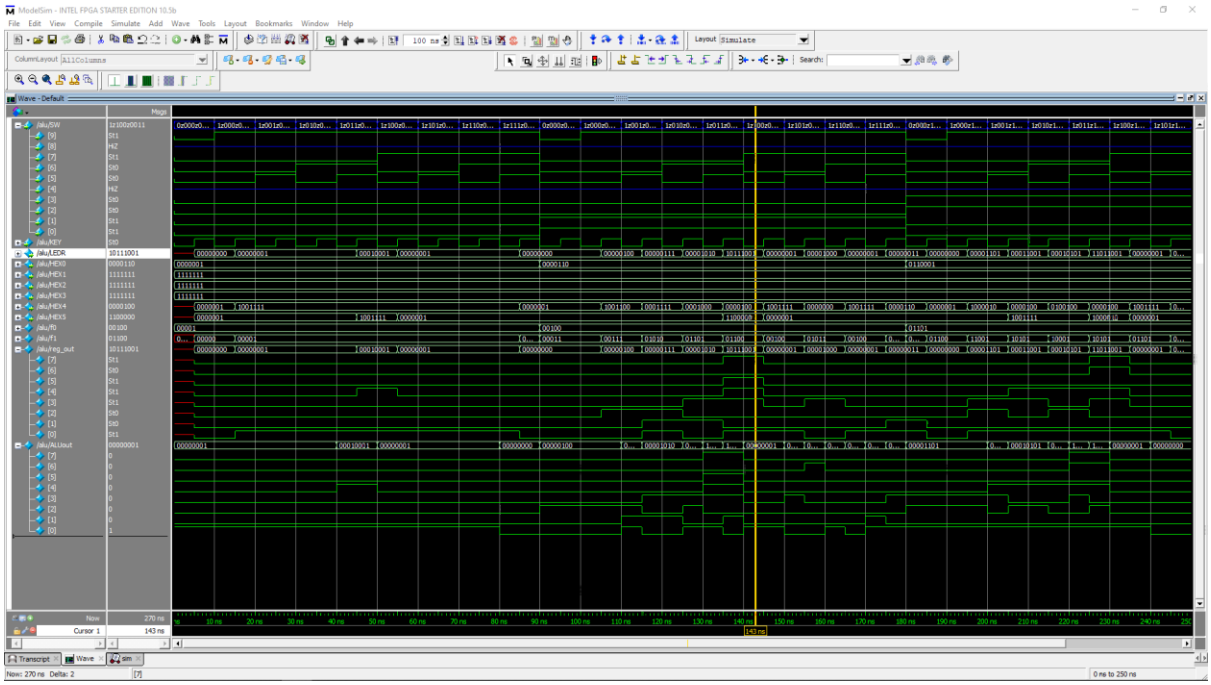
Figure 4: Digital board header pin assignment

Schematic of gated D latch labelled with connecting pins and outputs.

4. No, a gated D latch does not experience the issue of indeterminate states, so if the outputs are not fed back into any of the inputs, any combination of Clk and D can be tested. However, it needs to be noted that clk needs to be high for a change in output to be seen. So initial testing should not be done when clk is at 0.

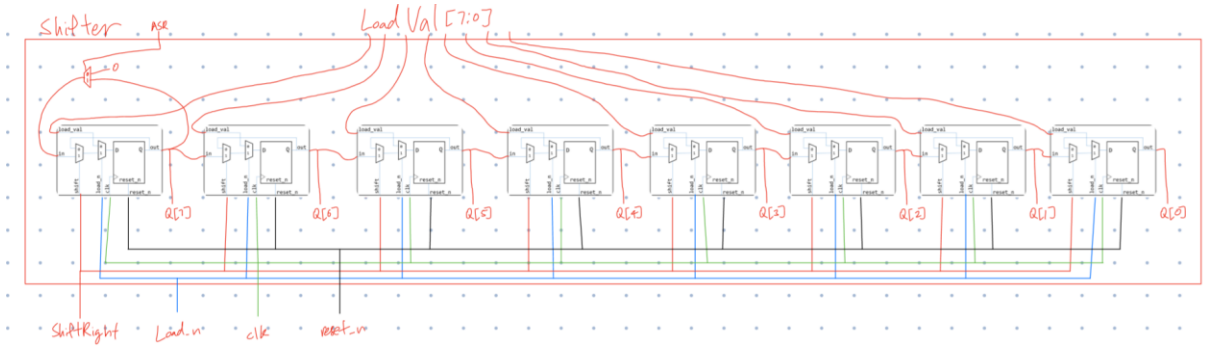
Part II:

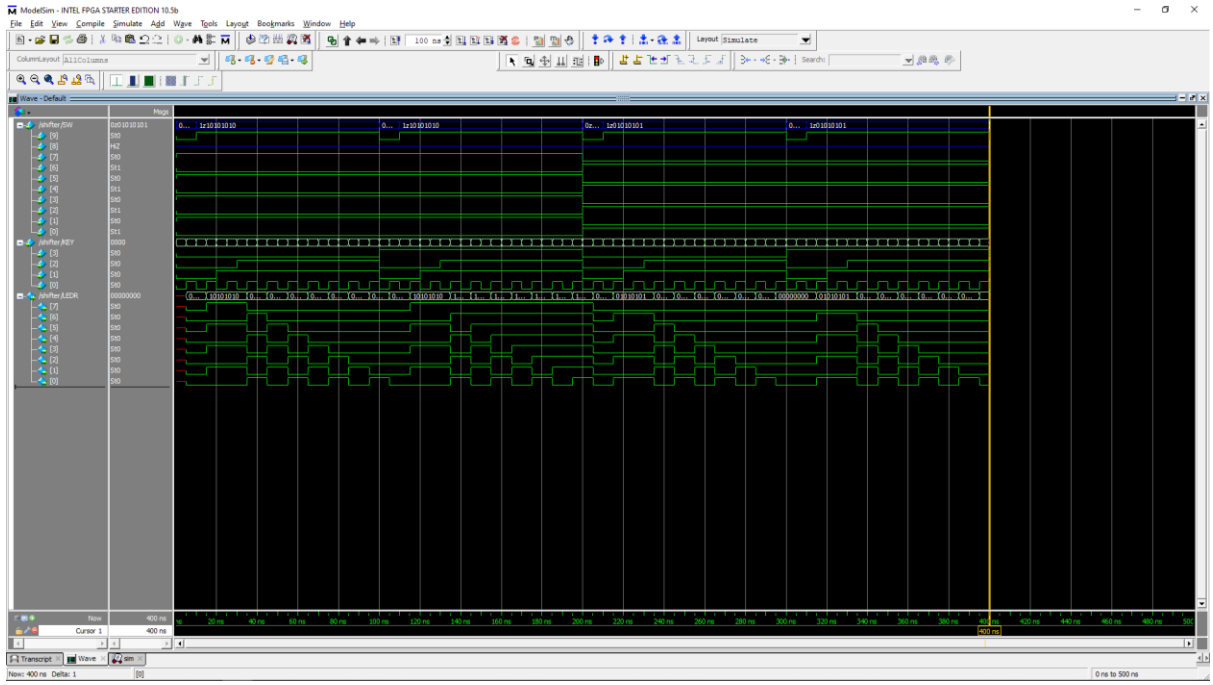
1. Verilog and test code submitted on Quercus.

2. 

Modelsim simulation for ALU register over various inputs. We can see that the reg_out trails ALUout by 5 ns when the reset_n value is high, as expected. Other inputs behave as expected.

Part III:

1. As no values are loaded and nothing is being shifted, the shift register should display a constant 8'b00000000, meaning all the LED's should be off.
2. 

Schematic of the 8-bit shifter.
3. Code for 1 bit shifter included in shifter.v code as shiftbit module and submitted on Quercus.
4. Code for 8 bit shifter included as top module shifter in shifter.v code submitted on Quercus.
5. 
Simulation done with shifter with both leading 1 and leading 0 inputs and tested on both ASR and non-ASR shifts. Outputs work as expected.