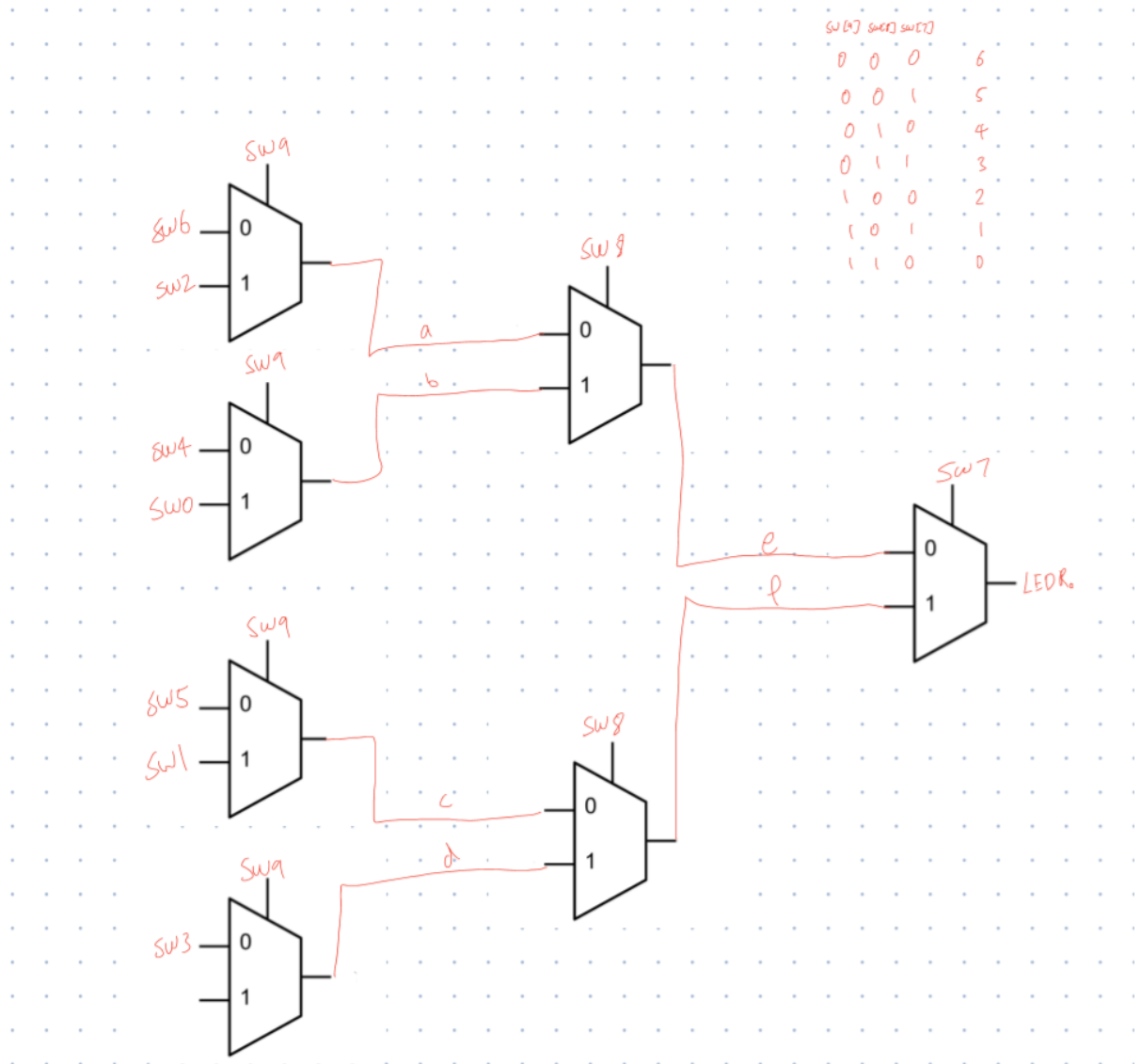
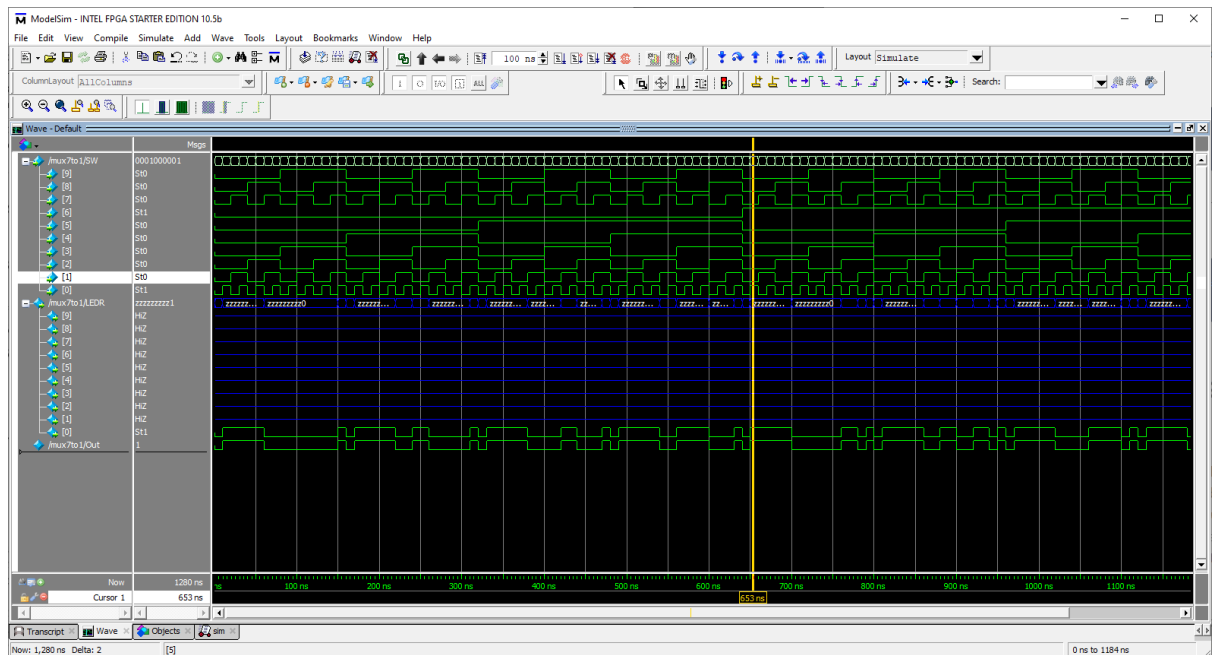


Lab 3 prelab

Part I:

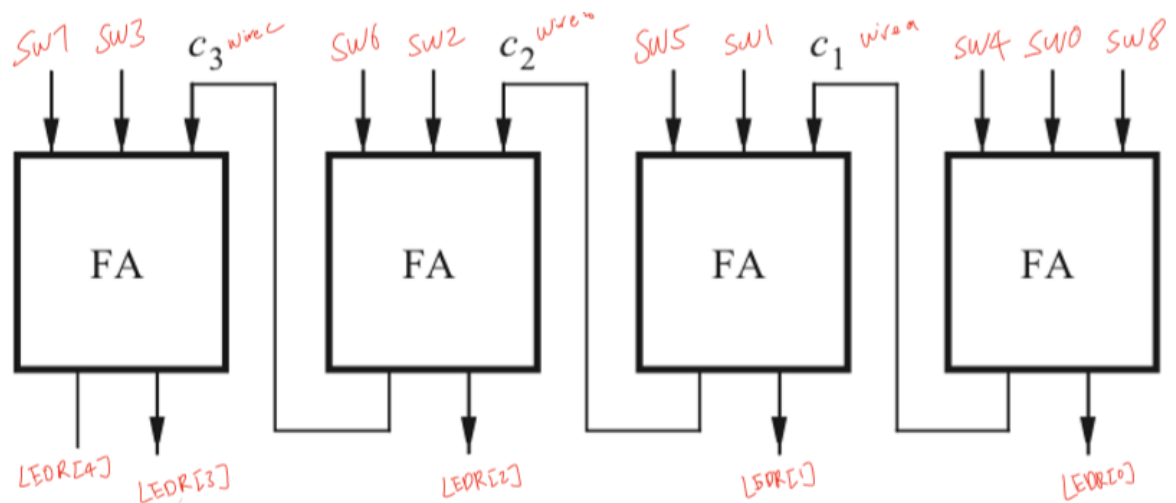


1. Schematic for 7to1 multiplexer
2. Submitted mux7to1.v on Quercus

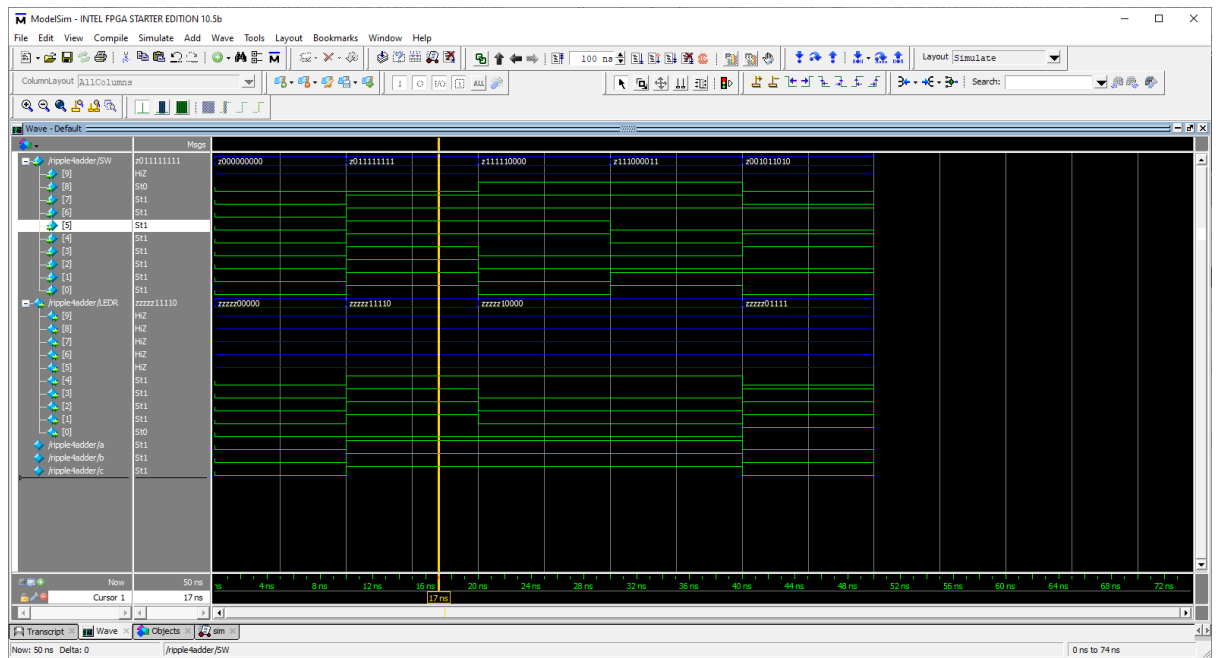


- Simulation of 7to1 multiplexer.

Part II:

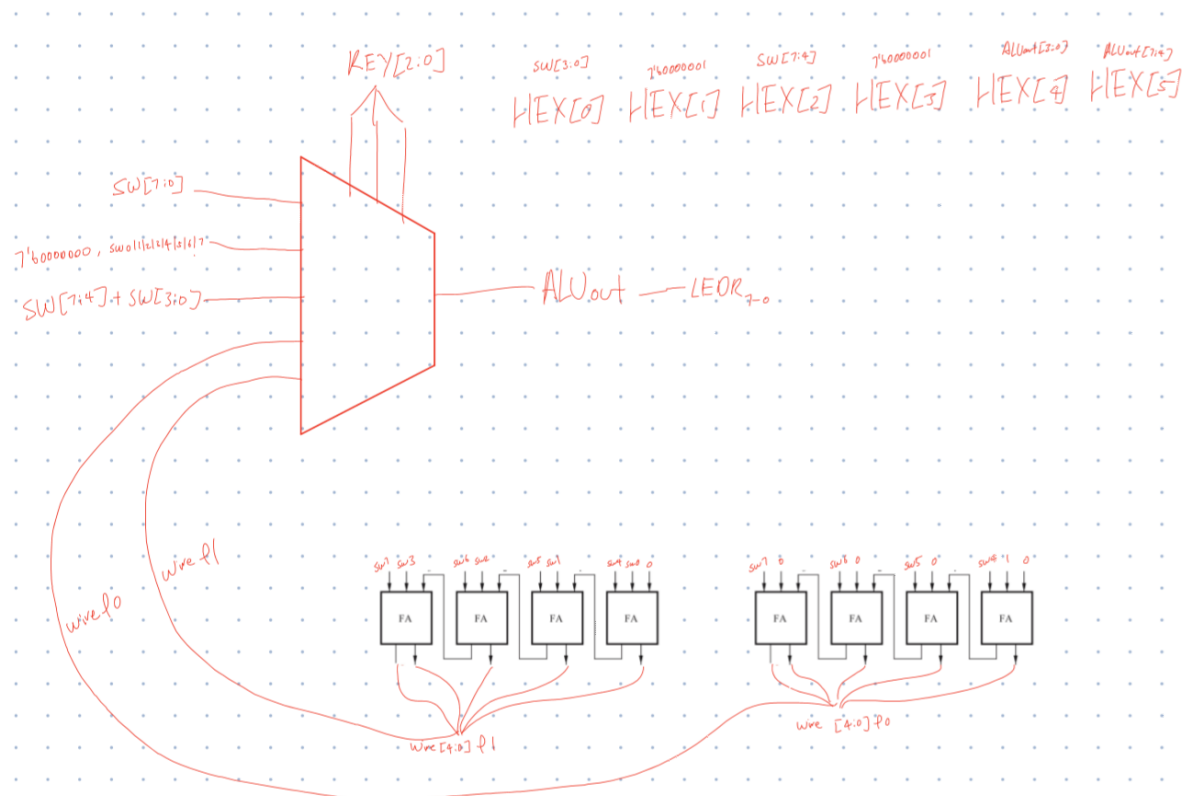


- Schematic of 4-bit ripple carry adder
- Verilog modules submitted on Quercus.

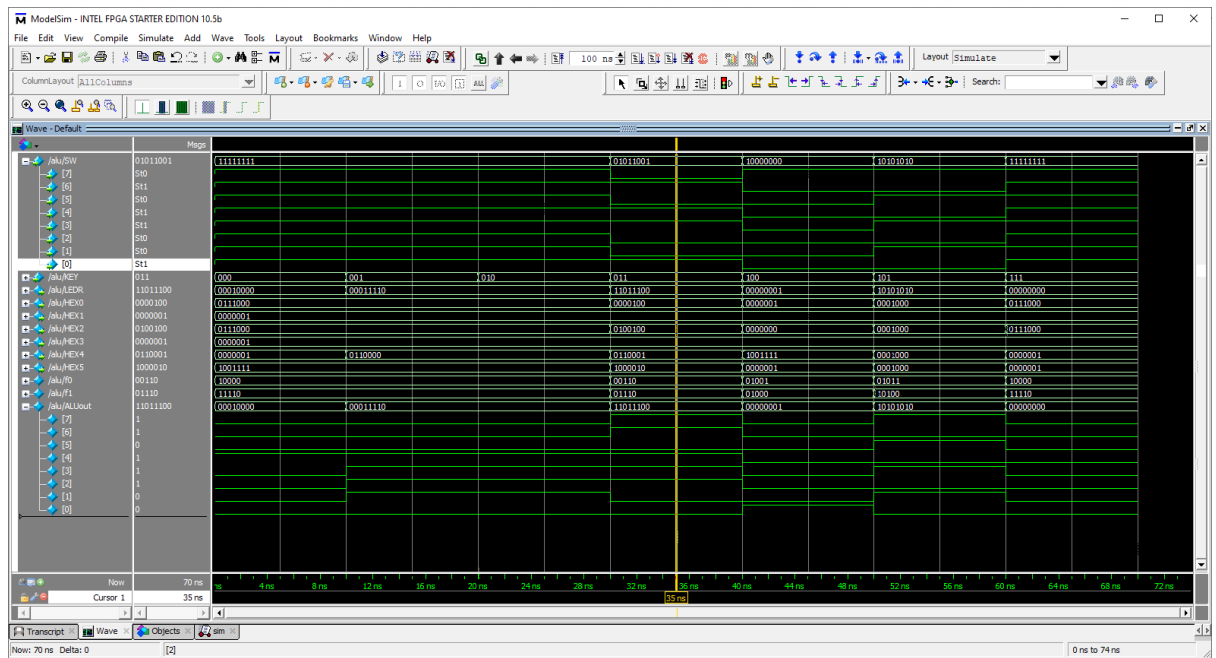


- Simulation for 4-bit ripple carry adder. Test cases tested that the carry was working, and that circuit was not carrying unintentionally.

Part III:



- Schematic for Arithmetic Logic Unit (ALU)
- Code for ALU submitted on Quercus.



- Simulation for ALU. All possible function cases tested, including default.