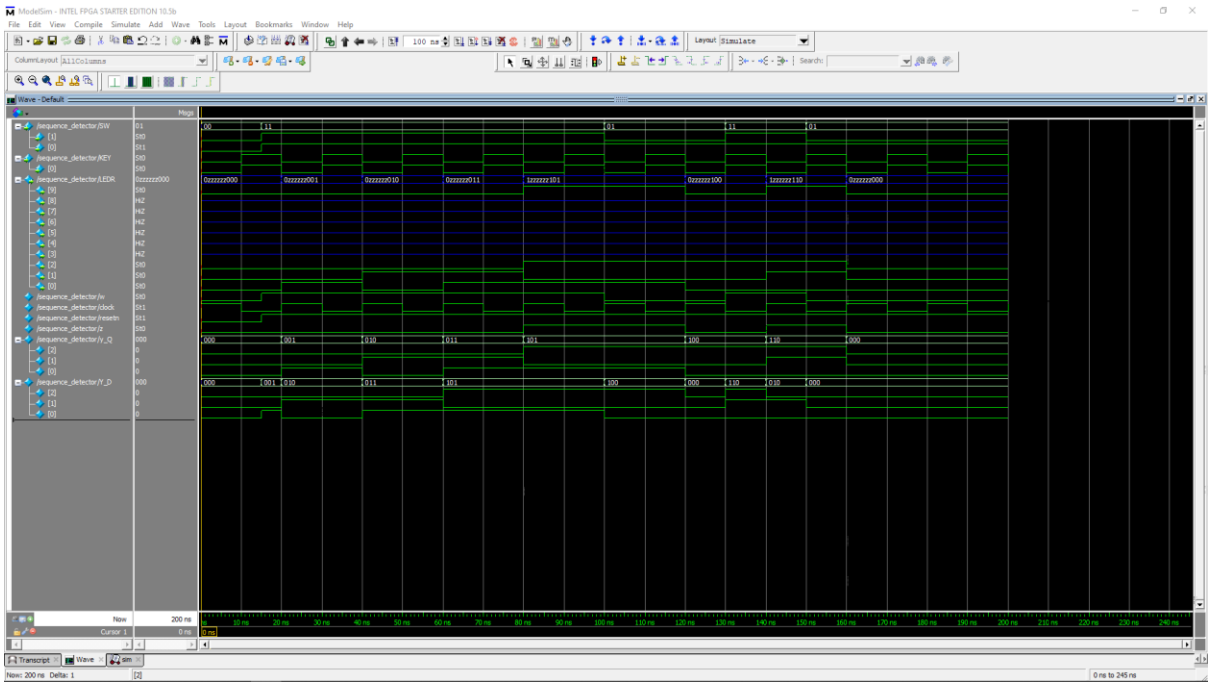
Part I:

2. Resetn is a synchronous active low signal. To reset the FSM, force resetn to be 0.

3. Code submitted on Quercus.

4.



Simulation for 1111 and 1101 inputs, we can see that the output LED goes high for both.

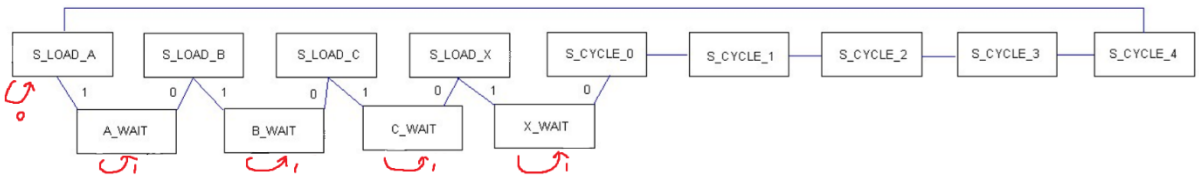
Part II:

2.

F_n	out	a	b	c	x	r	sa	sb	op	go	F_{n+1}
S_LOAD_A	0	1	0	0	0	0	00	00	0	0	S_LOAD_A
S_LOAD_A	0	1	0	0	0	0	00	00	0	1	S_LOAD_A_WAIT
S_LOAD_A_WAIT	0	1	0	0	0	0	00	00	0	0	S_LOAD_B
S_LOAD_A_WAIT	0	1	0	0	0	0	00	00	0	1	S_LOAD_A_WAIT
S_LOAD_B	0	0	1	0	0	0	00	00	0	0	S_LOAD_B
S_LOAD_B	0	0	1	0	0	0	00	00	0	1	S_LOAD_B_WAIT
S_LOAD_B_WAIT	0	0	1	0	0	0	00	00	0	0	S_LOAD_C
S_LOAD_B_WAIT	0	0	1	0	0	0	00	00	0	1	S_LOAD_B_WAIT
S_LOAD_C	0	0	0	1	0	0	00	00	0	0	S_LOAD_C
S_LOAD_C	0	0	0	1	0	0	00	00	0	1	S_LOAD_C_WAIT
S_LOAD_C_WAIT	0	0	0	1	0	0	00	00	0	0	S_LOAD_X
S_LOAD_C_WAIT	0	0	0	1	0	0	00	00	0	1	S_LOAD_C_WAIT
S_LOAD_X	0	0	0	0	1	0	00	00	0	0	S_LOAD_X
S_LOAD_X	0	0	0	0	1	0	00	00	0	1	S_LOAD_X_WAIT
S_LOAD_X_WAIT	0	0	0	0	1	0	00	00	0	0	S_CYCLE_0
S_LOAD_X_WAIT	0	0	0	0	1	0	00	00	0	1	S_LOAD_X_WAIT
S_CYCLE_0	1	1	0	0	0	0	00	11	1	0	S_CYCLE_1
S_CYCLE_0	1	1	0	0	0	0	00	11	1	1	S_CYCLE_1
S_CYCLE_1	1	1	0	0	0	0	00	11	1	0	S_CYCLE_2
S_CYCLE_1	1	1	0	0	0	0	00	11	1	1	S_CYCLE_2
S_CYCLE_2	1	1	0	0	0	0	01	11	1	0	S_CYCLE_3
S_CYCLE_2	1	1	0	0	0	0	01	11	1	1	S_CYCLE_3
S_CYCLE_3	1	1	0	0	0	0	00	10	0	0	S_CYCLE_4
S_CYCLE_3	1	1	0	0	0	0	00	10	0	1	S_CYCLE_4
S_CYCLE_4	0	0	0	0	0	1	00	01	0	0	S_LOAD_A
S_CYCLE_4	0	0	0	0	0	1	00	01	0	1	S_LOAD_A

State table for new computation.

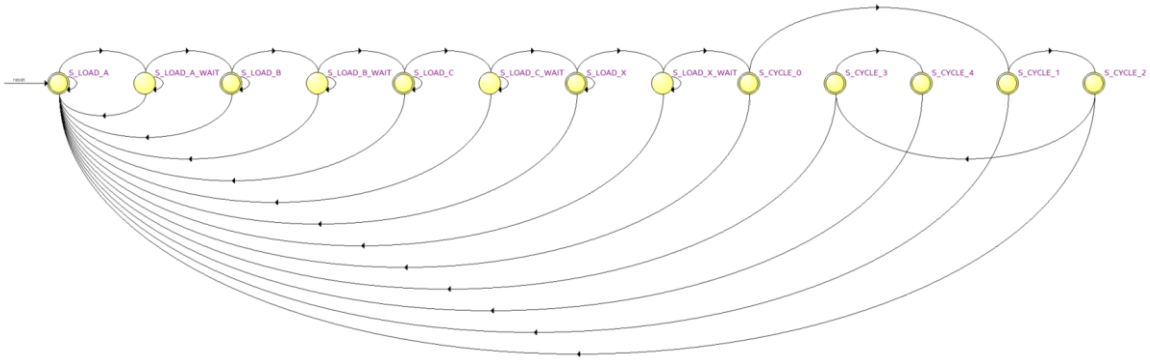
3.



State diagram.

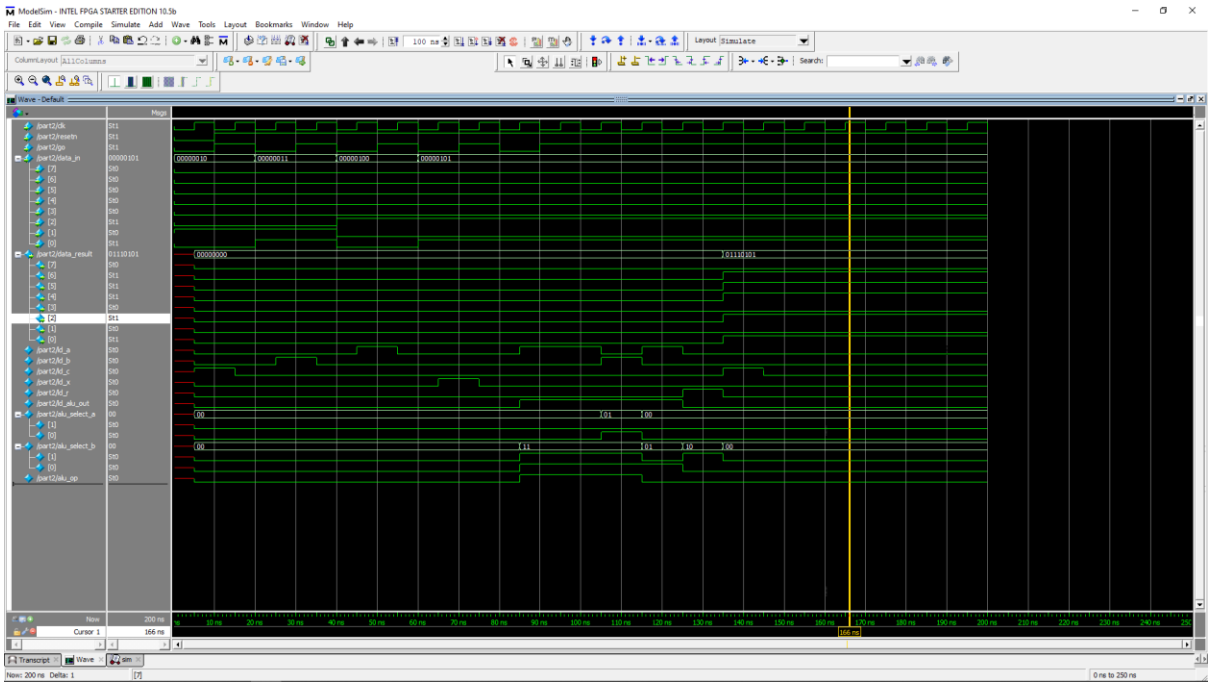
4. Verilog code submitted on Quercus.

5.

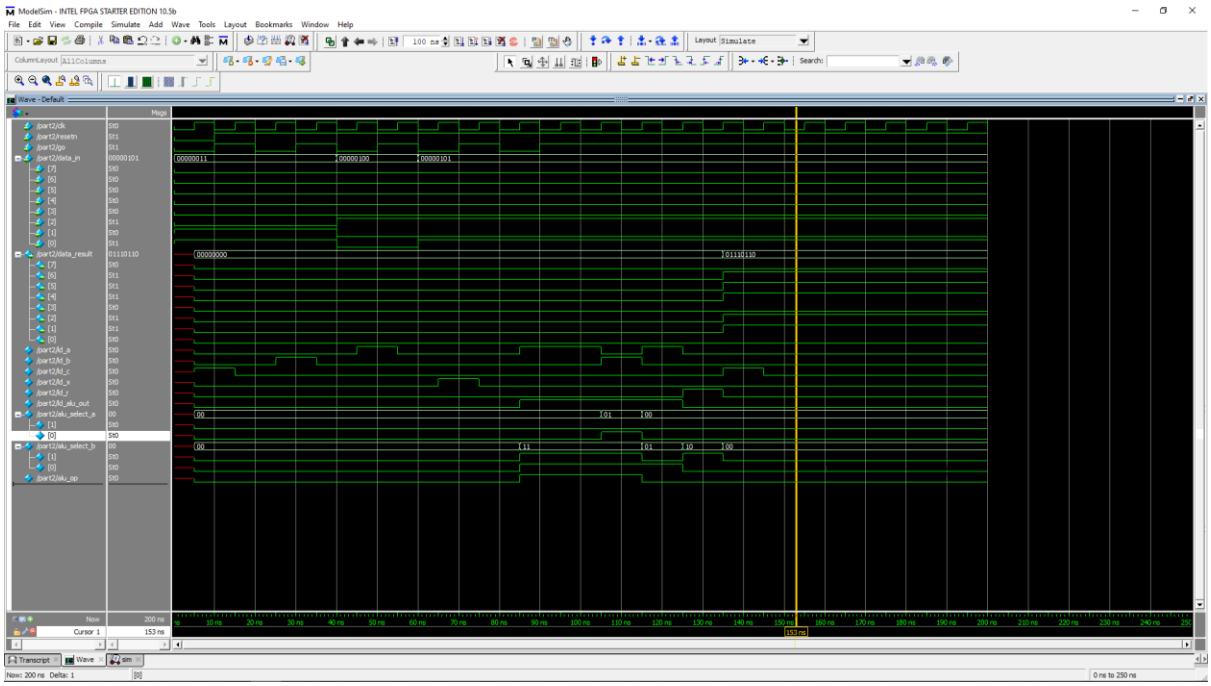


Generated FSM.

6.



Modelsim tests, with A = 2, B = 3, C = 4, x = 5, output 117



Modelsim tests, with A = 3, B = 3, C = 4, x = 5, output 118