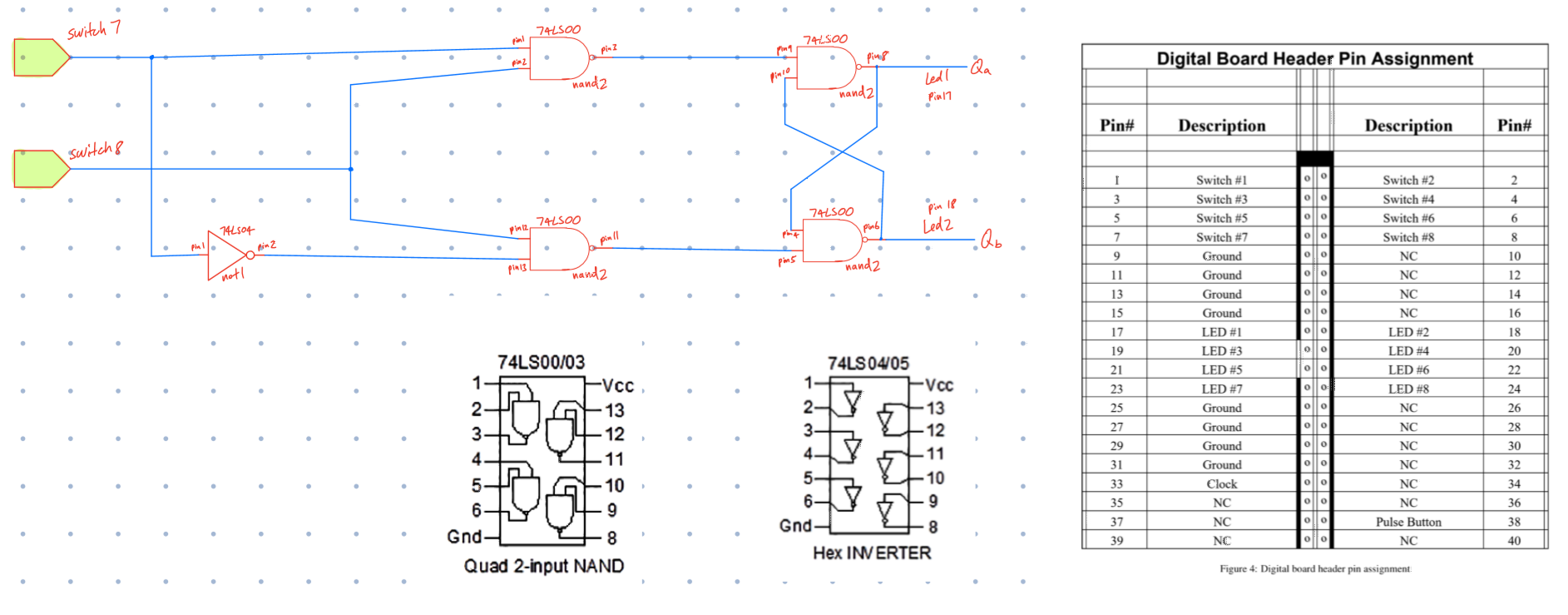
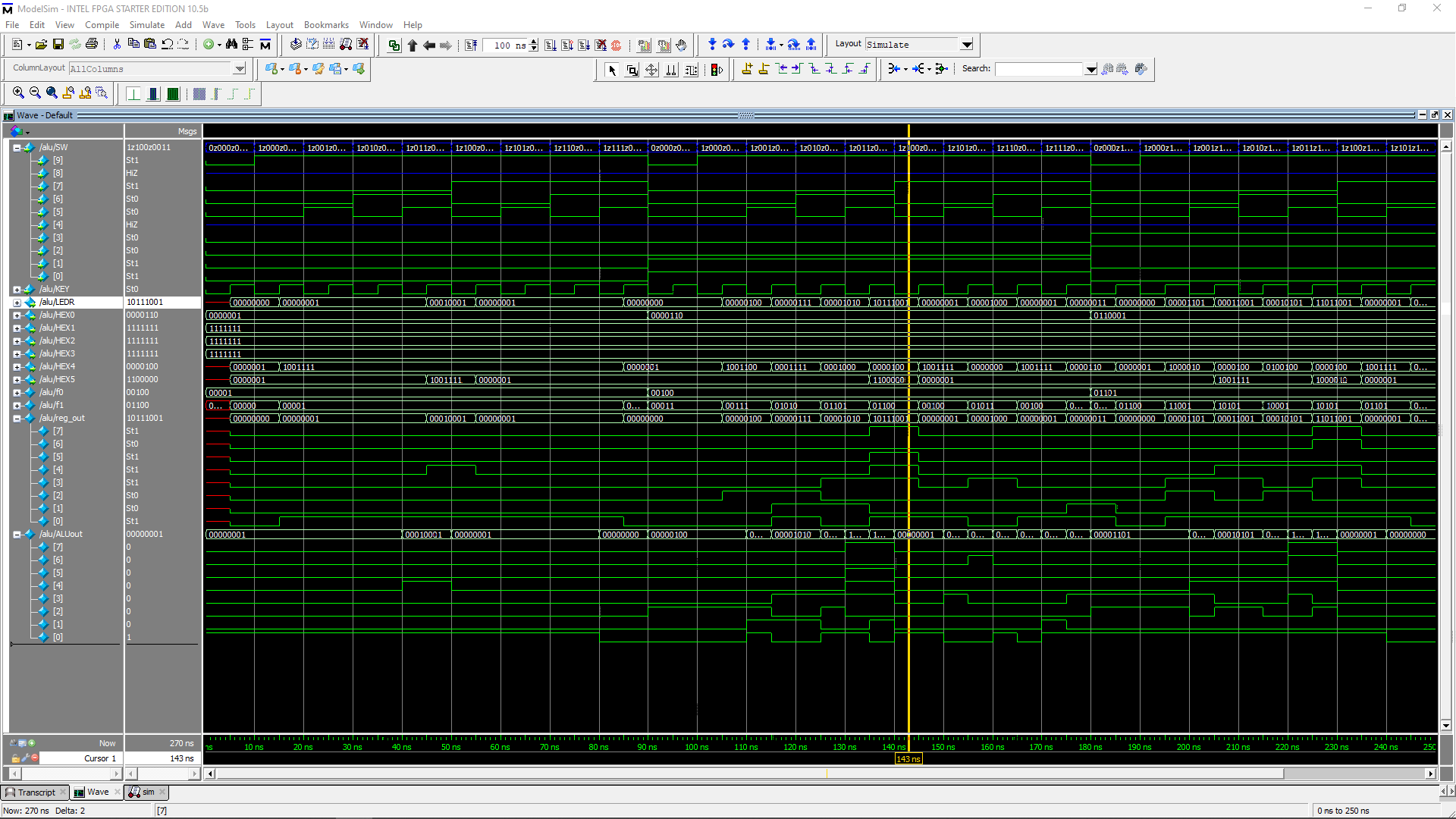
Part I:

1. 

Schematic of gated D latch labelled with connecting pins and outputs.

4. No, a gated D latch does not experience the issue of indeterminate states, so if the outputs are not fed back into any of the inputs, any combination of Clk and D can be tested. However, it needs to be noted that clk needs to be high for a change in output to be seen. So initial testing should not be done when clk is at 0.

Part II:

1. Verilog and test code submitted on Quercus.
2. 

Modelsim simulation for ALU register over various inputs. We can see that the reg\_out trails ALUout by 5 ns when the reset\_n value is high, as expected. Other inputs behave as expected.