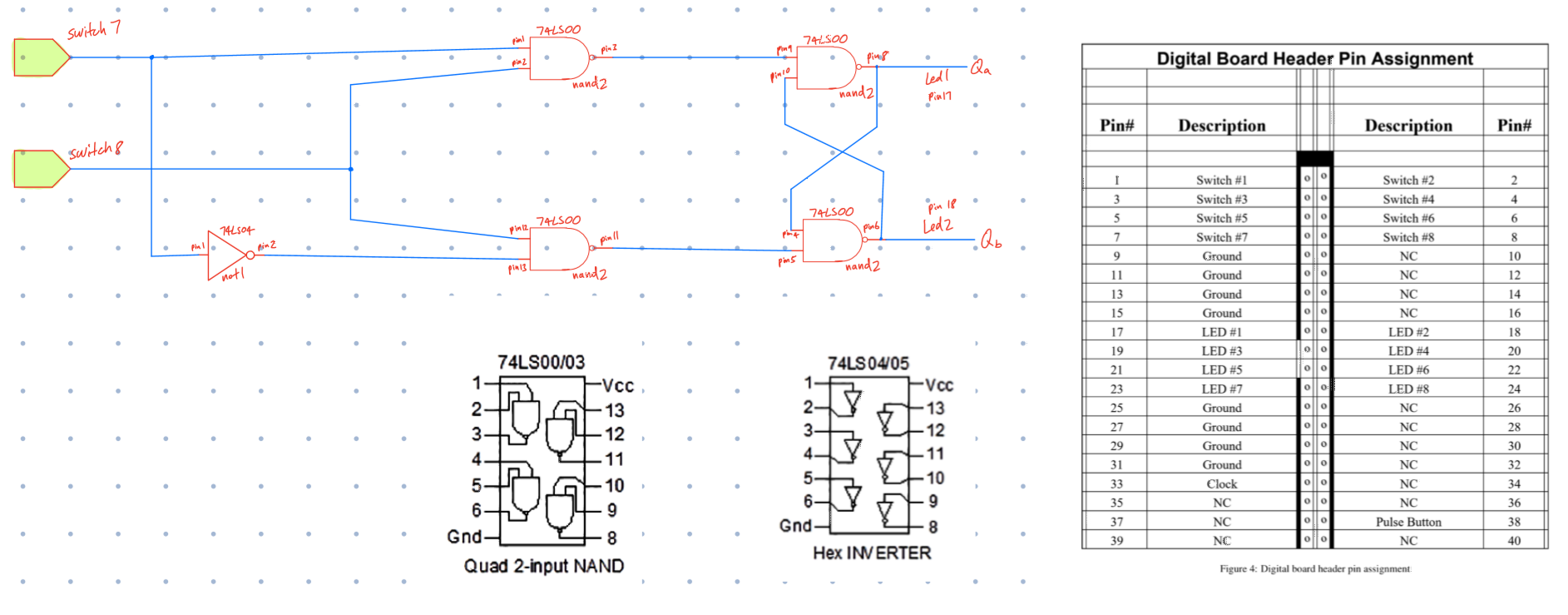
Part I:

1. 

Schematic of gated D latch labelled with connecting pins and outputs.

4. No, a gated D latch does not experience the issue of indeterminate states, so as long as the outputs are not fed back into any of the inputs, any combination of Clk and D can be tested.