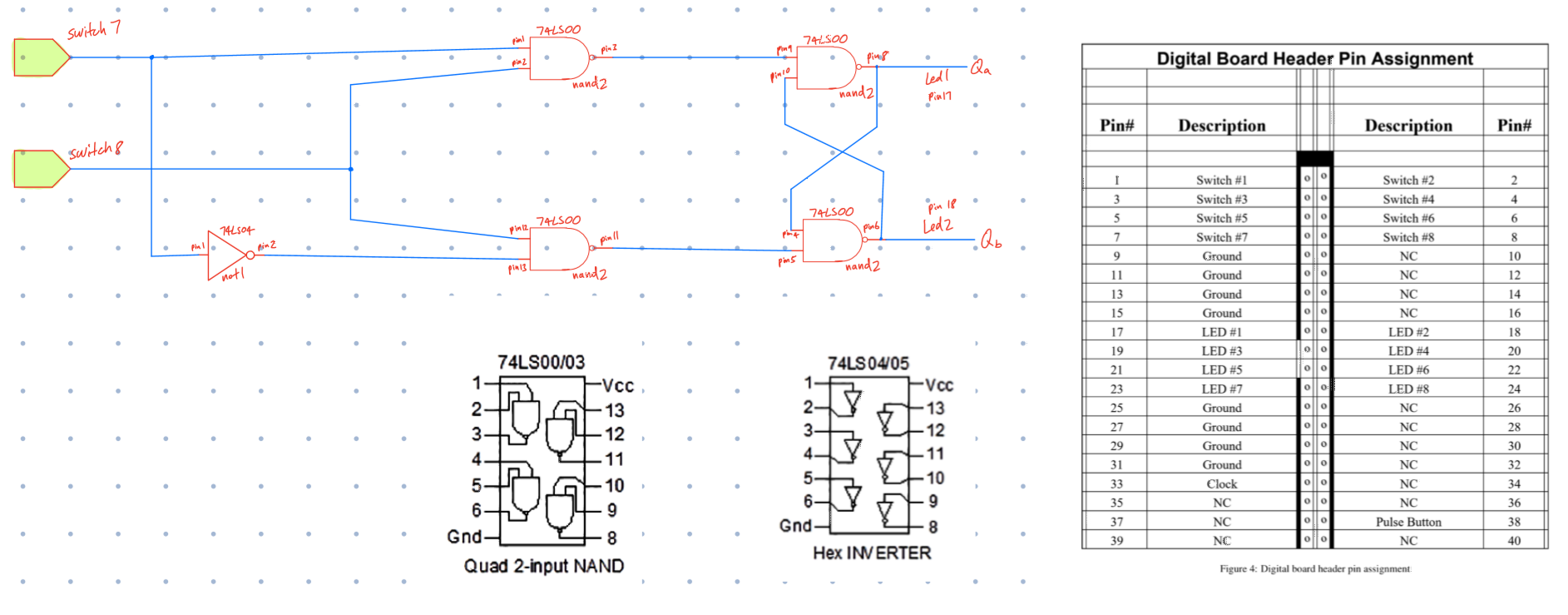
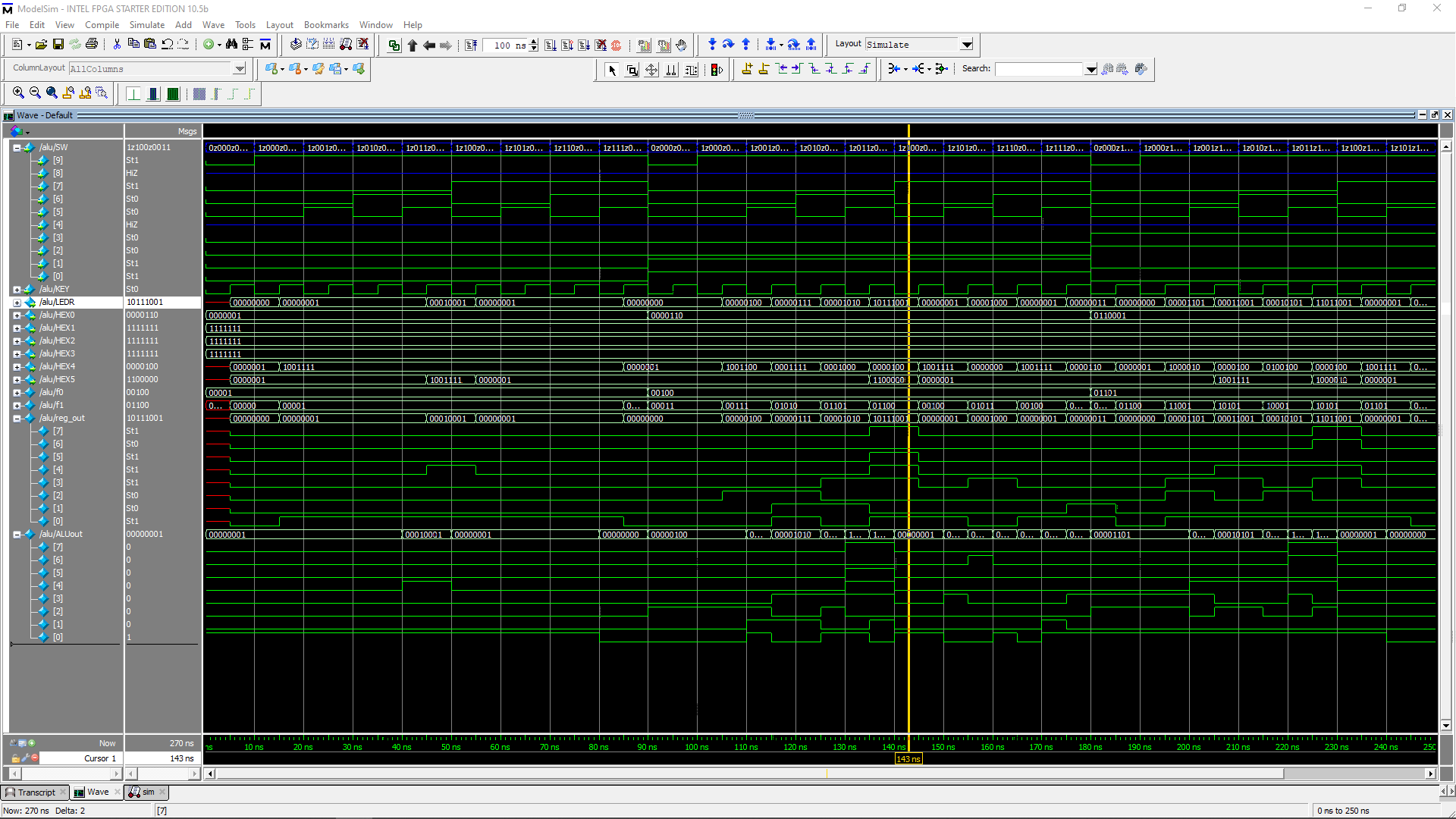
Part I:

1. 

Schematic of gated D latch labelled with connecting pins and outputs.

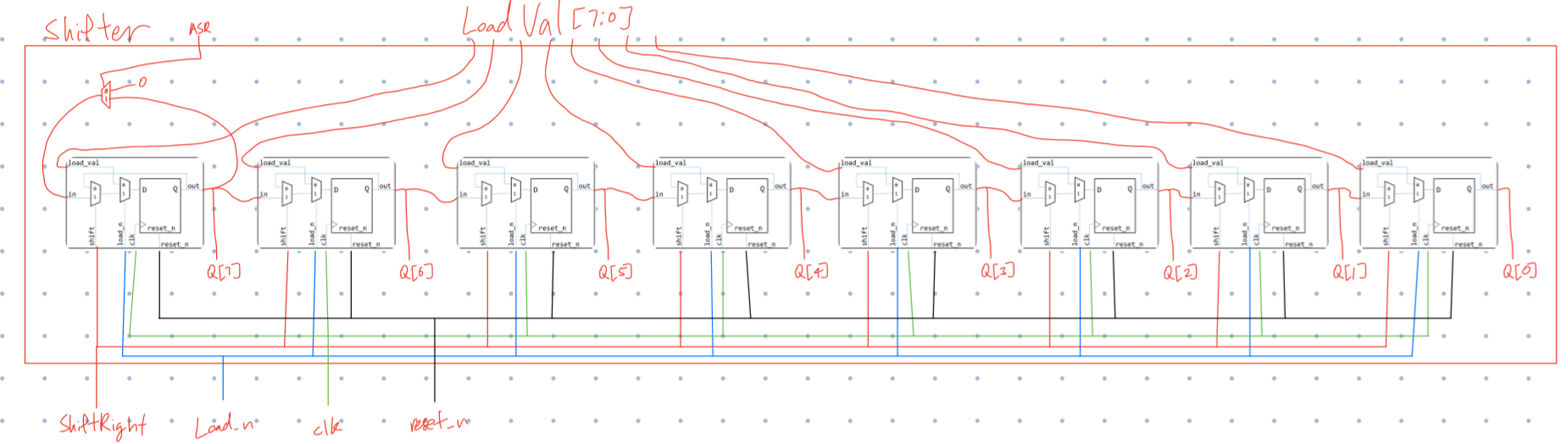
4. No, a gated D latch does not experience the issue of indeterminate states, so if the outputs are not fed back into any of the inputs, any combination of Clk and D can be tested. However, it needs to be noted that clk needs to be high for a change in output to be seen. So initial testing should not be done when clk is at 0.

Part II:

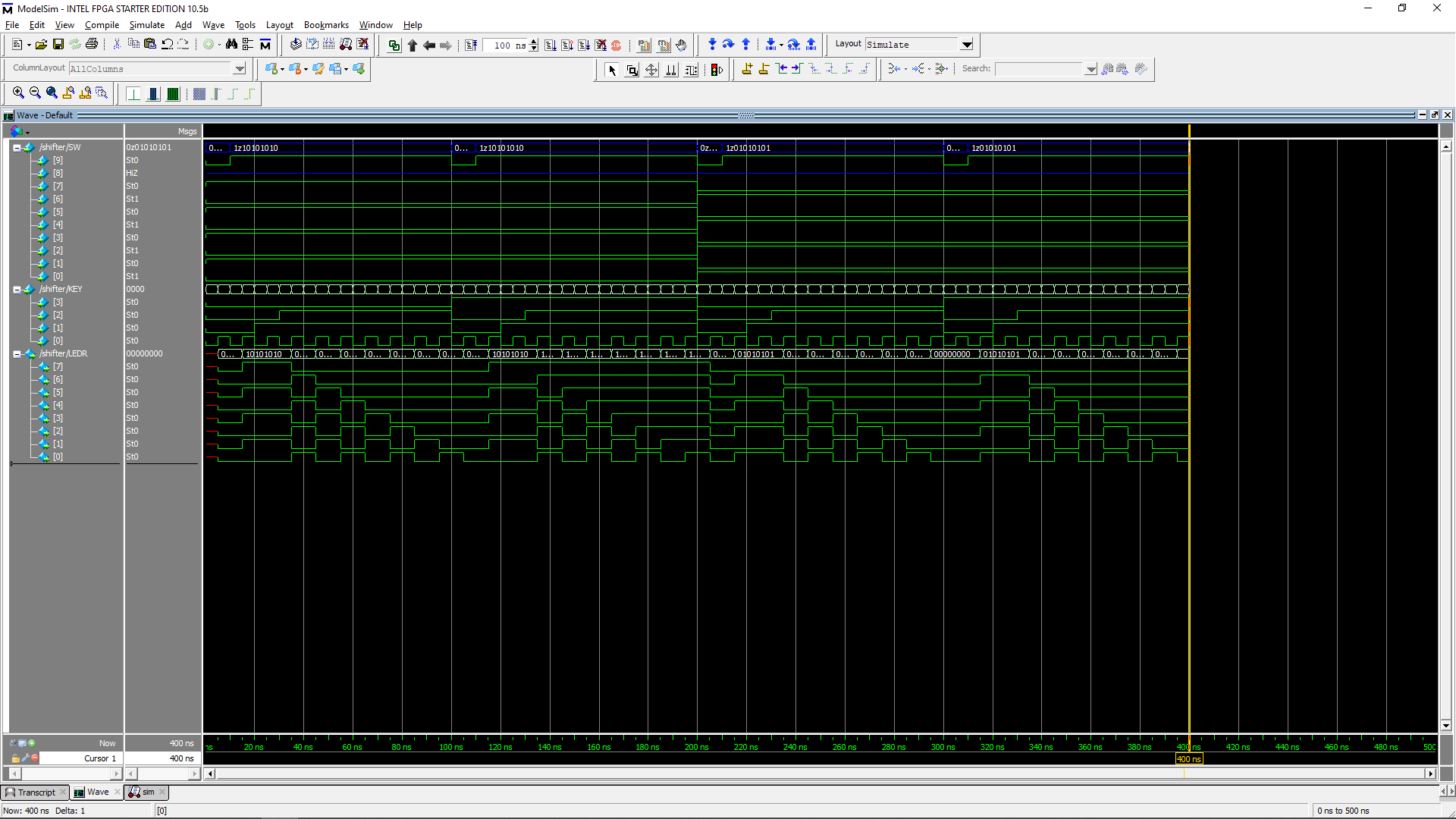
1. Verilog and test code submitted on Quercus.
2. 

Modelsim simulation for ALU register over various inputs. We can see that the reg\_out trails ALUout by 5 ns when the reset\_n value is high, as expected. Other inputs behave as expected.

Part III:

1. As no values are loaded and nothing is being shifted, the shift register should display a constant 8’b00000000, meaning all the LED’s should be off.
2. 

Schematic of the 8-bit shifter.

1. Code for 1 bit shifter included in shifter.v code as shiftbit module and submitted on Quercus.
2. Code for 8 bit shifter included as top module shifter in shifter.v code submitted on Quercus.
3. 

Simulation done with shifter with both leading 1 and leading 0 inputs and tested on both ASR and non-ASR shifts. Outputs work as expected.