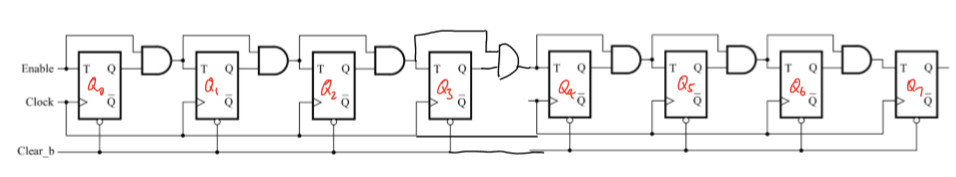
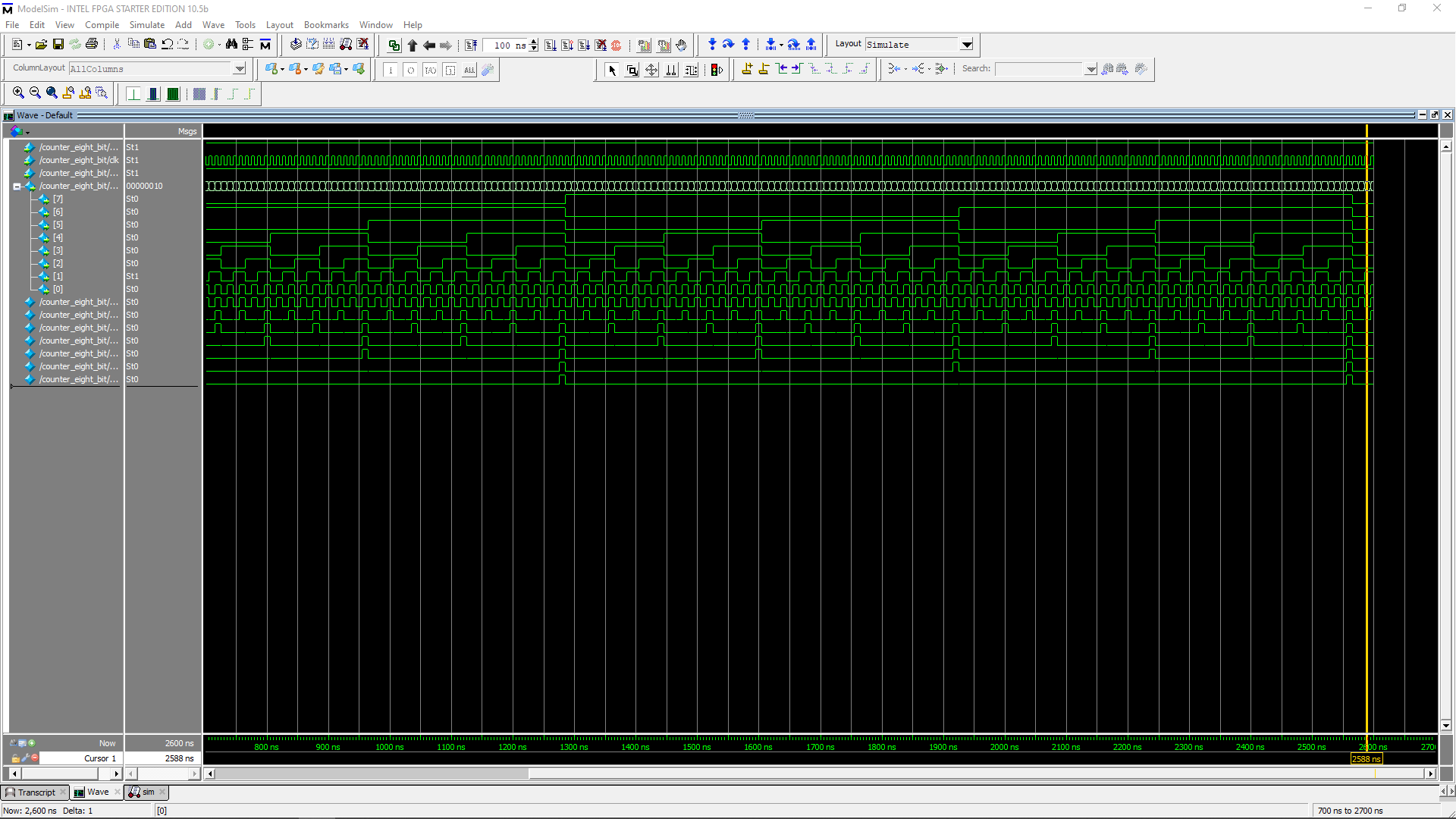
Part I:

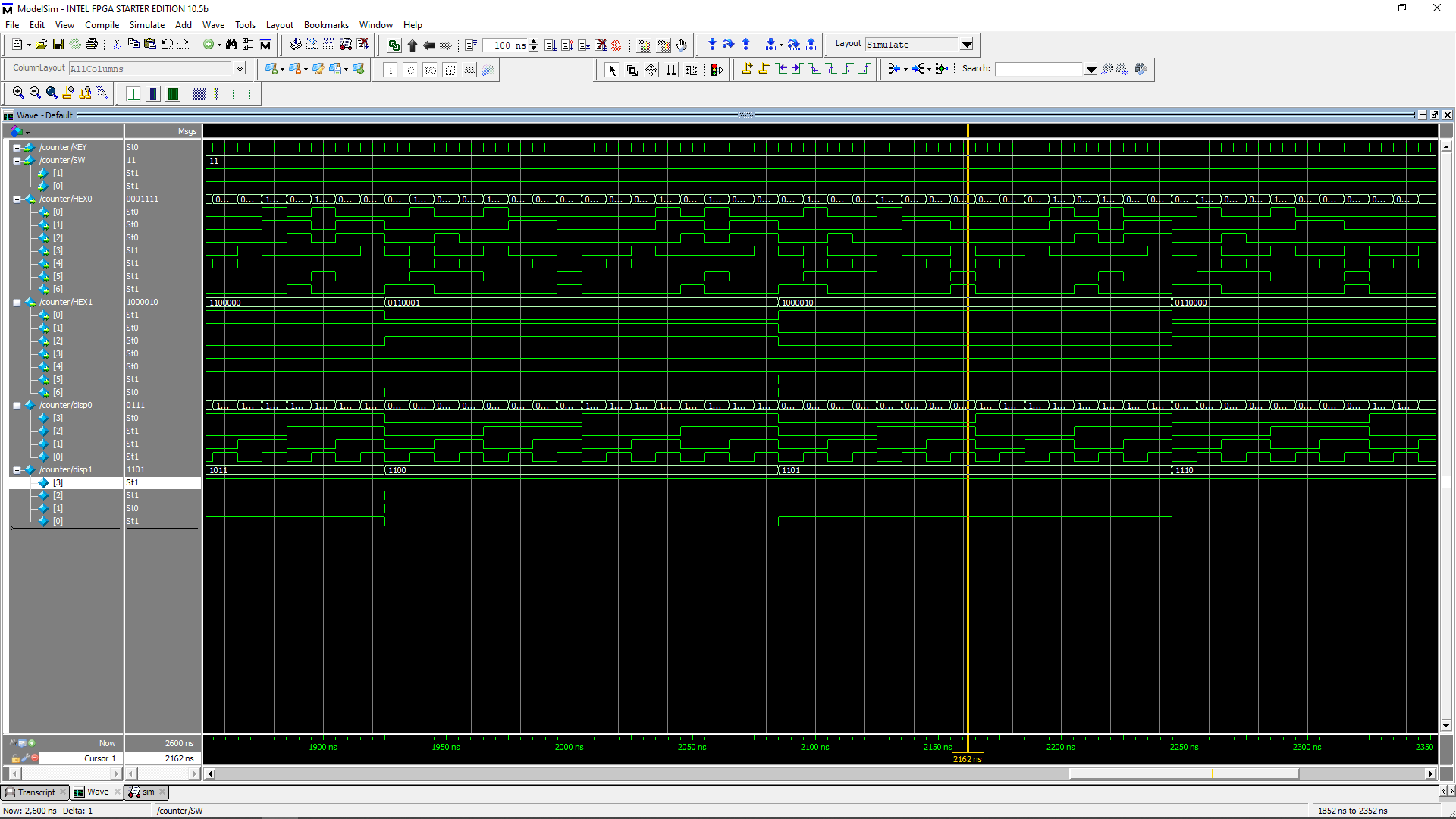
Q1&2:

Schematic for 8-bit counter.

3. Verilog code included in final counter.v file. 8bit counter is defined as counter\_eight\_bit and T flip flop is tflipflop.

4. 

Simulation for the eight bit counter, it counts correctly and resets at the end when number overflows.

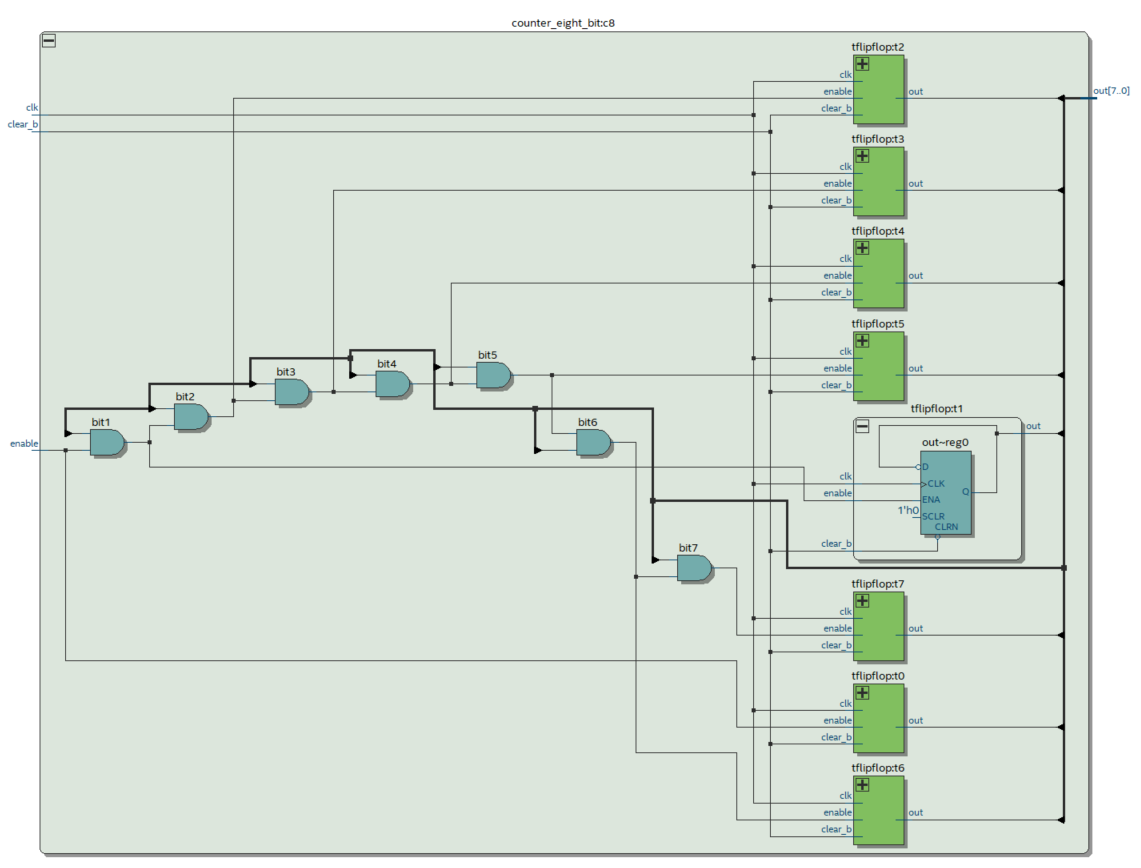
5. 

Connected inputs properly, hex displays 0 and 1 now show output of counter with KEY[0] as clk. Verilog code submitted on Quercus.

6.

a) Logic utilization is 13/32070 ( < 1% ), and 8 registers are in use. The size of the circuit is much smaller than the size of the FPGA.

b) 621.89 Mhz

7. 

The circuitry is roughly the same, except that there are 8 output lanes and 8 flipflops instead of 4.