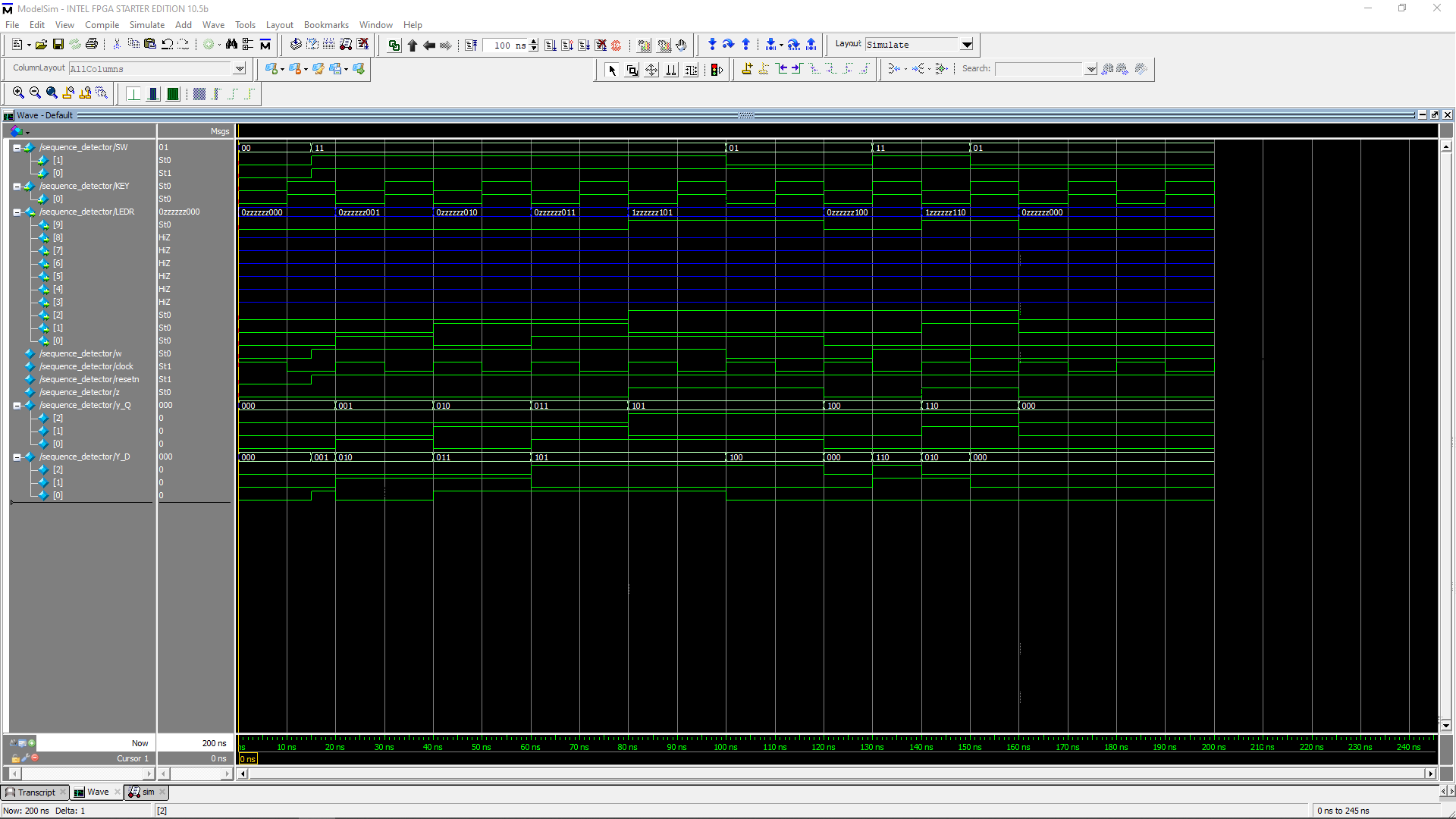
Part I:

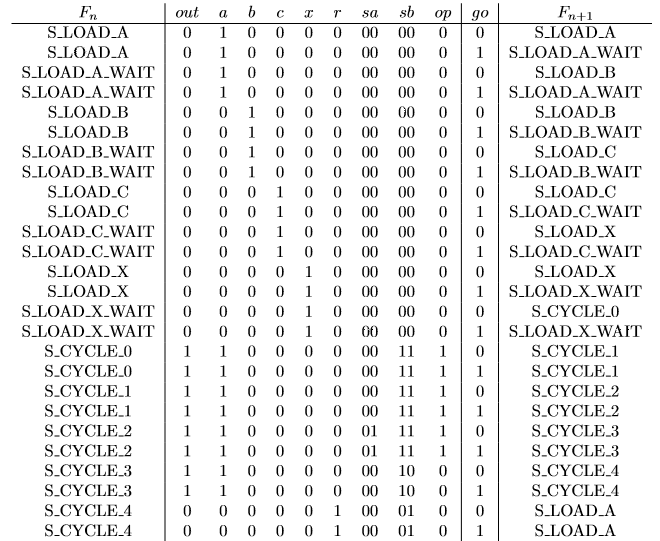
2. Resetn is a synchronous active low signal. To reset the FSM, force resetn to be 0.

3. Code submitted on Quercus.

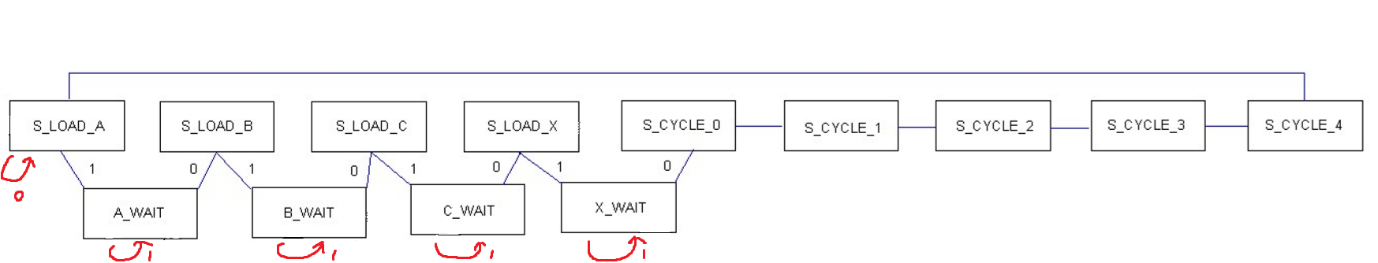
4. 

Simulation for 1111 and 1101 inputs, we can see that the output LED goes high for both.

Part II:

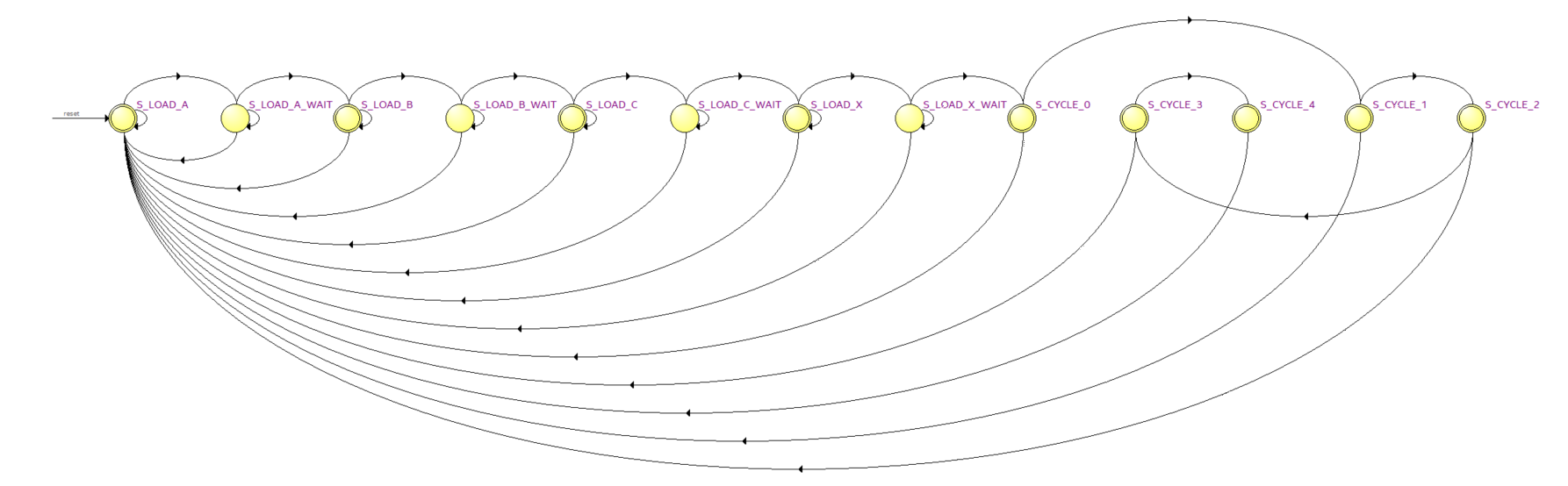
2. 

State table for new computation.

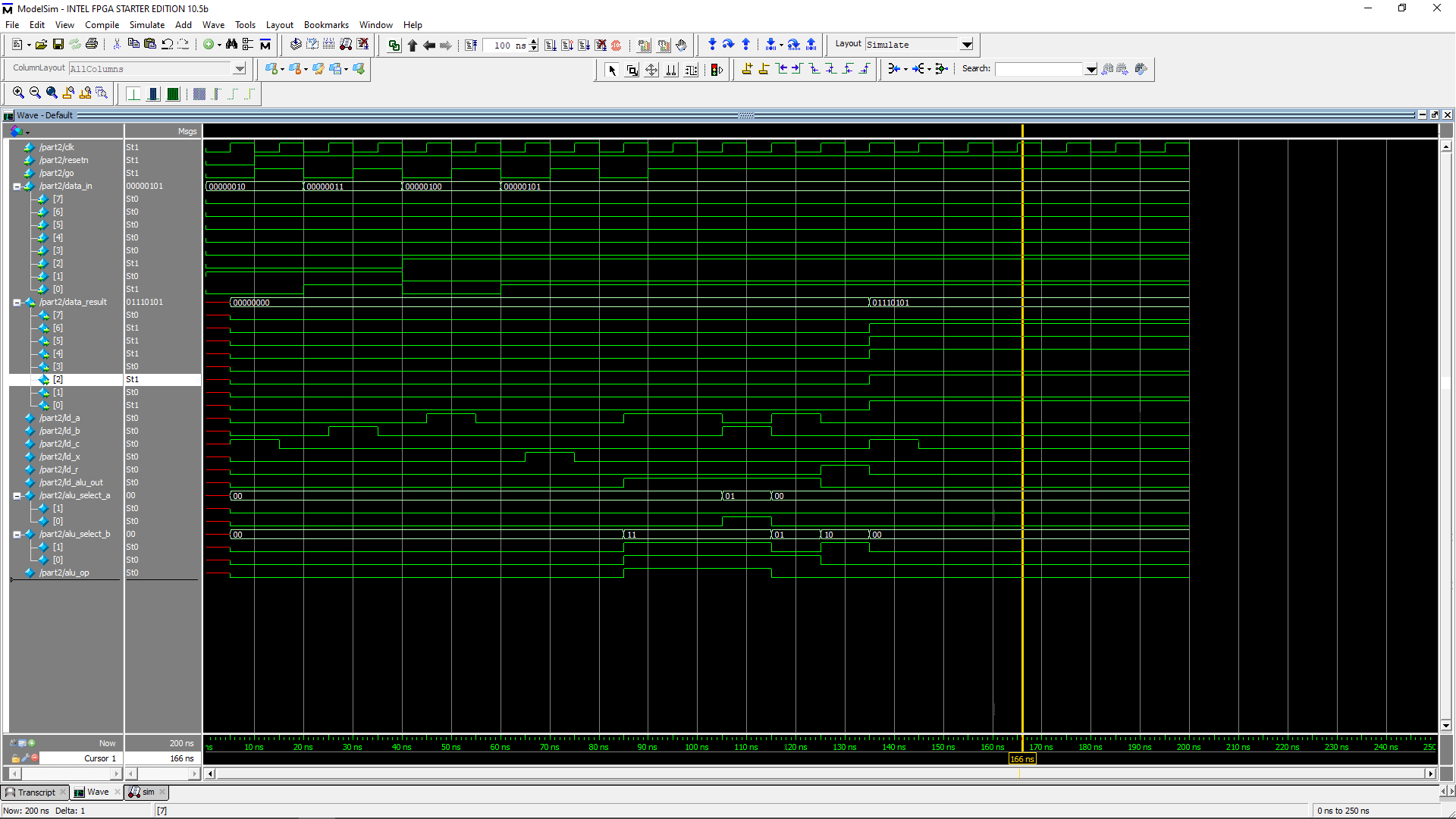
3. 

State diagram.

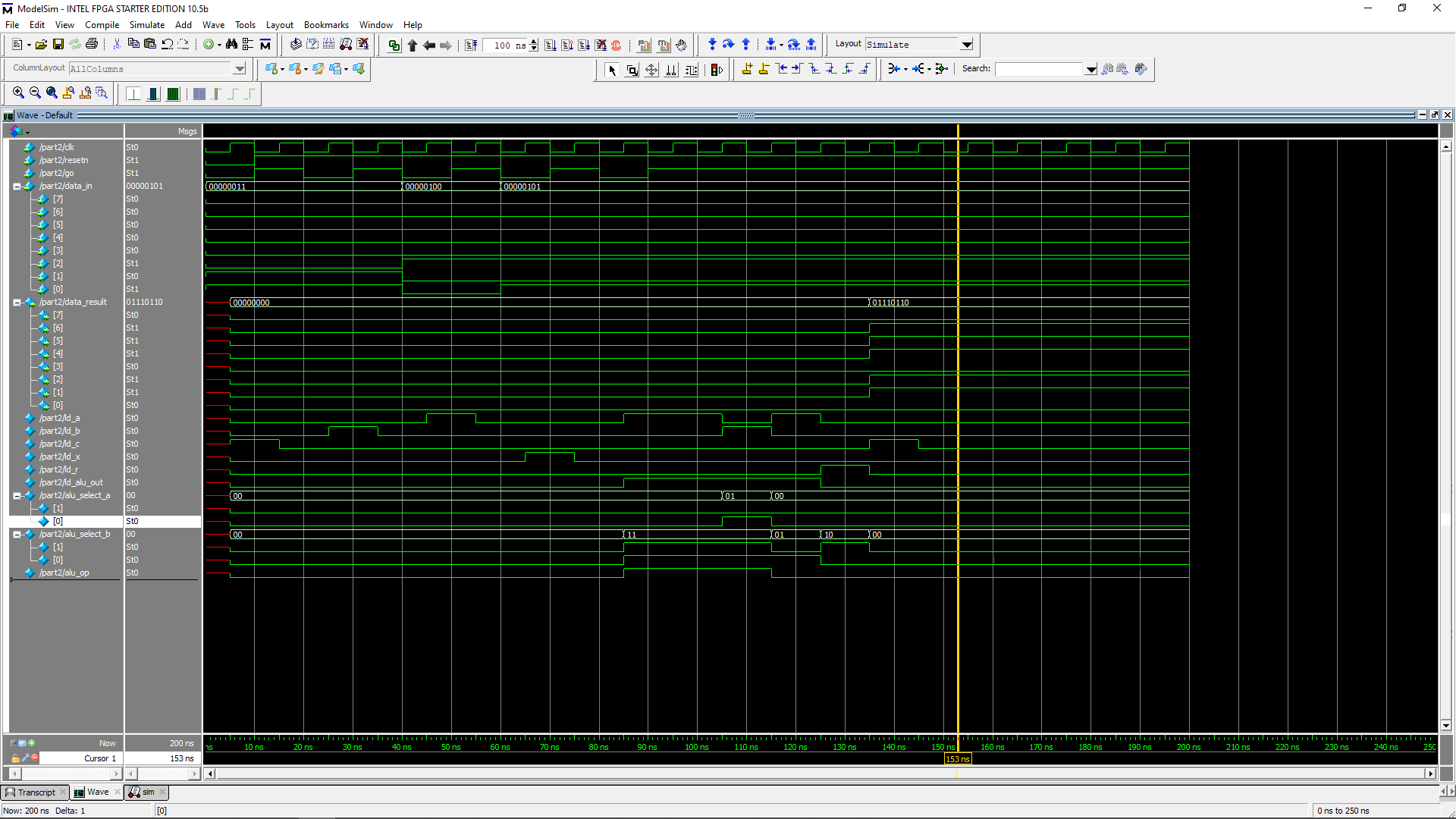
4. Verilog code submitted on Quercus.

5. 

Generated FSM.

6. 

Modelsim tests, with A = 2, B = 3, C = 4, x = 5, output 117



Modelsim tests, with A = 3, B = 3, C = 4, x = 5, output 118