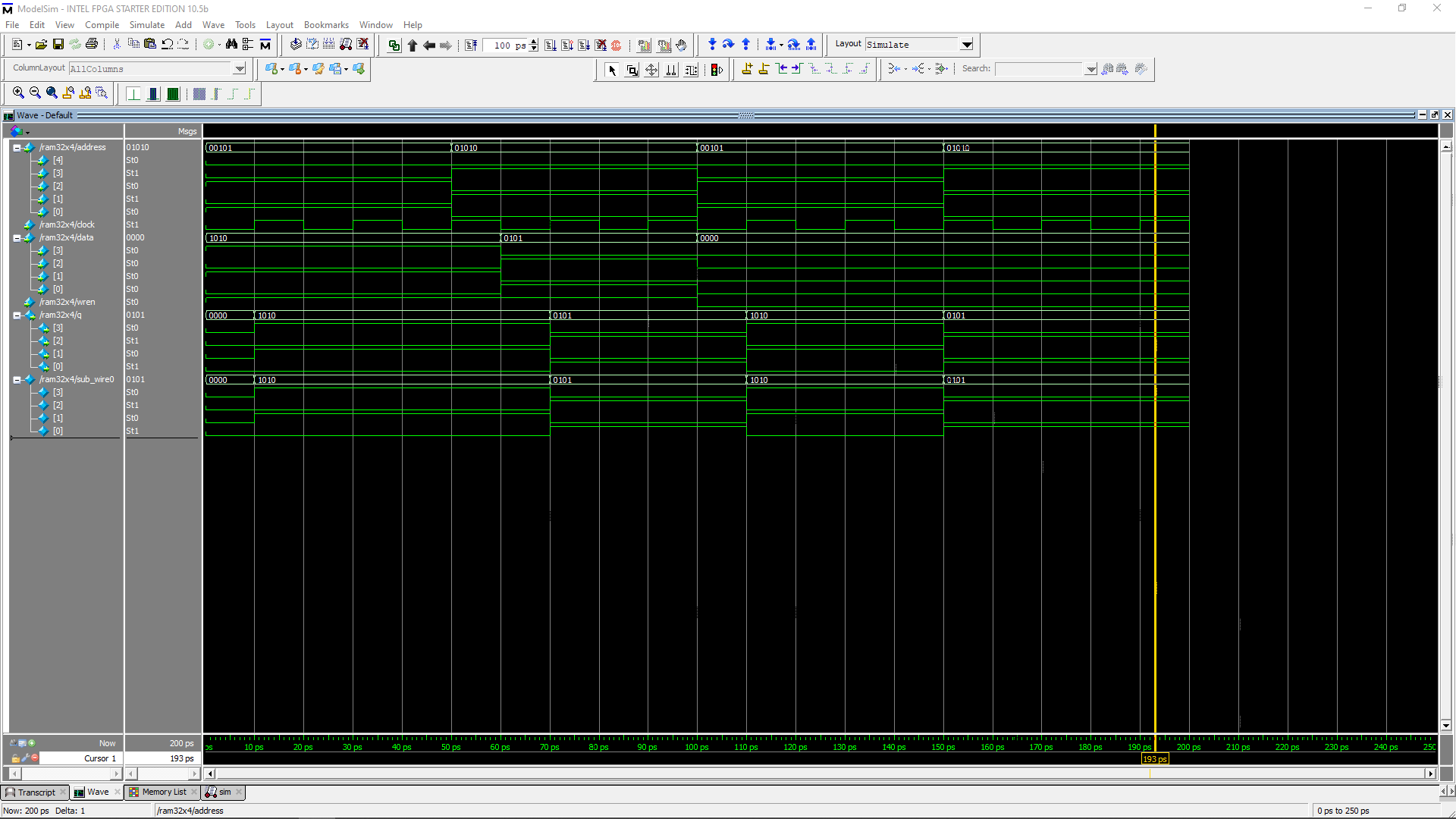
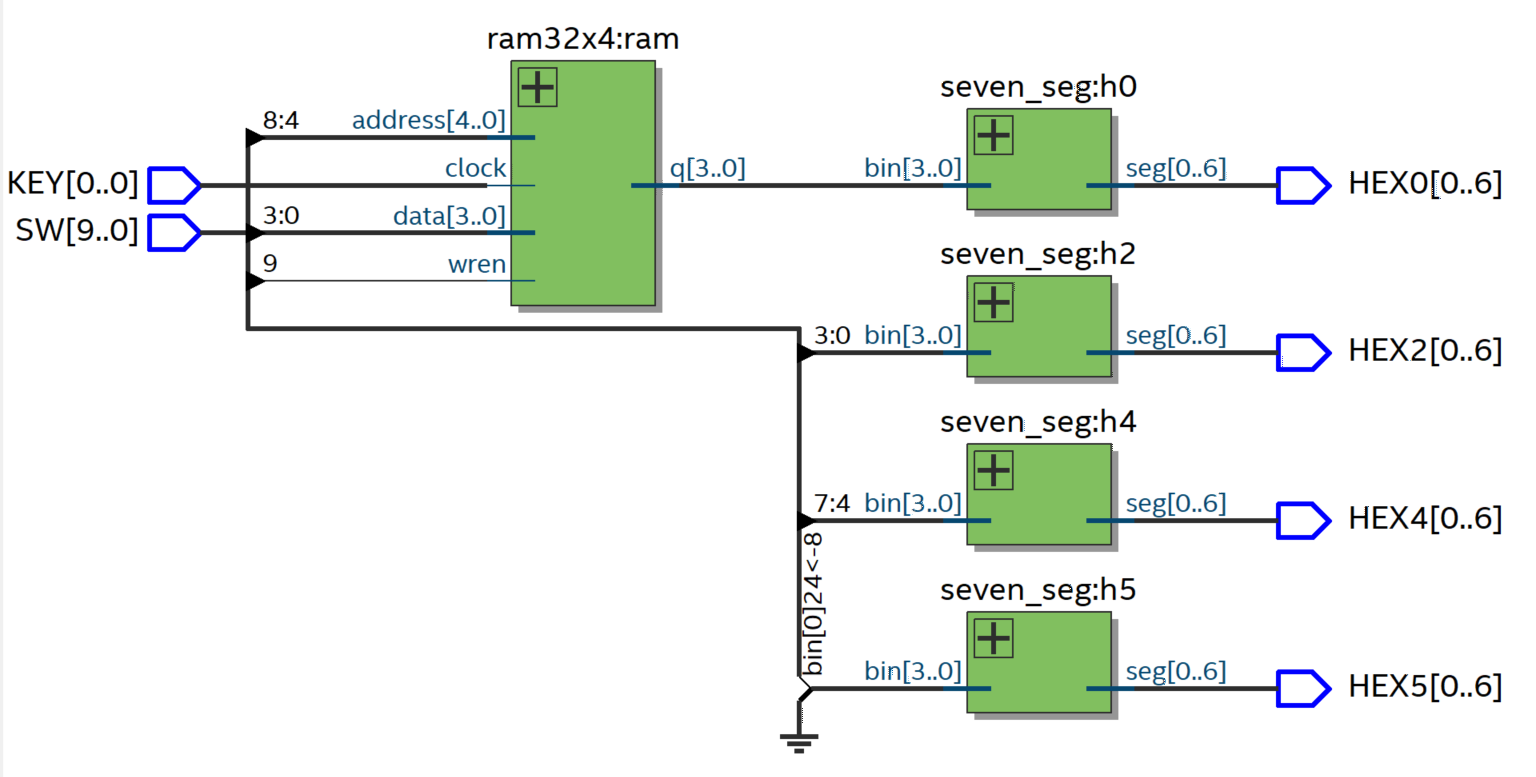
Part I:

Ram module created and is attached in top level file.

9. Simulation for the ram module.

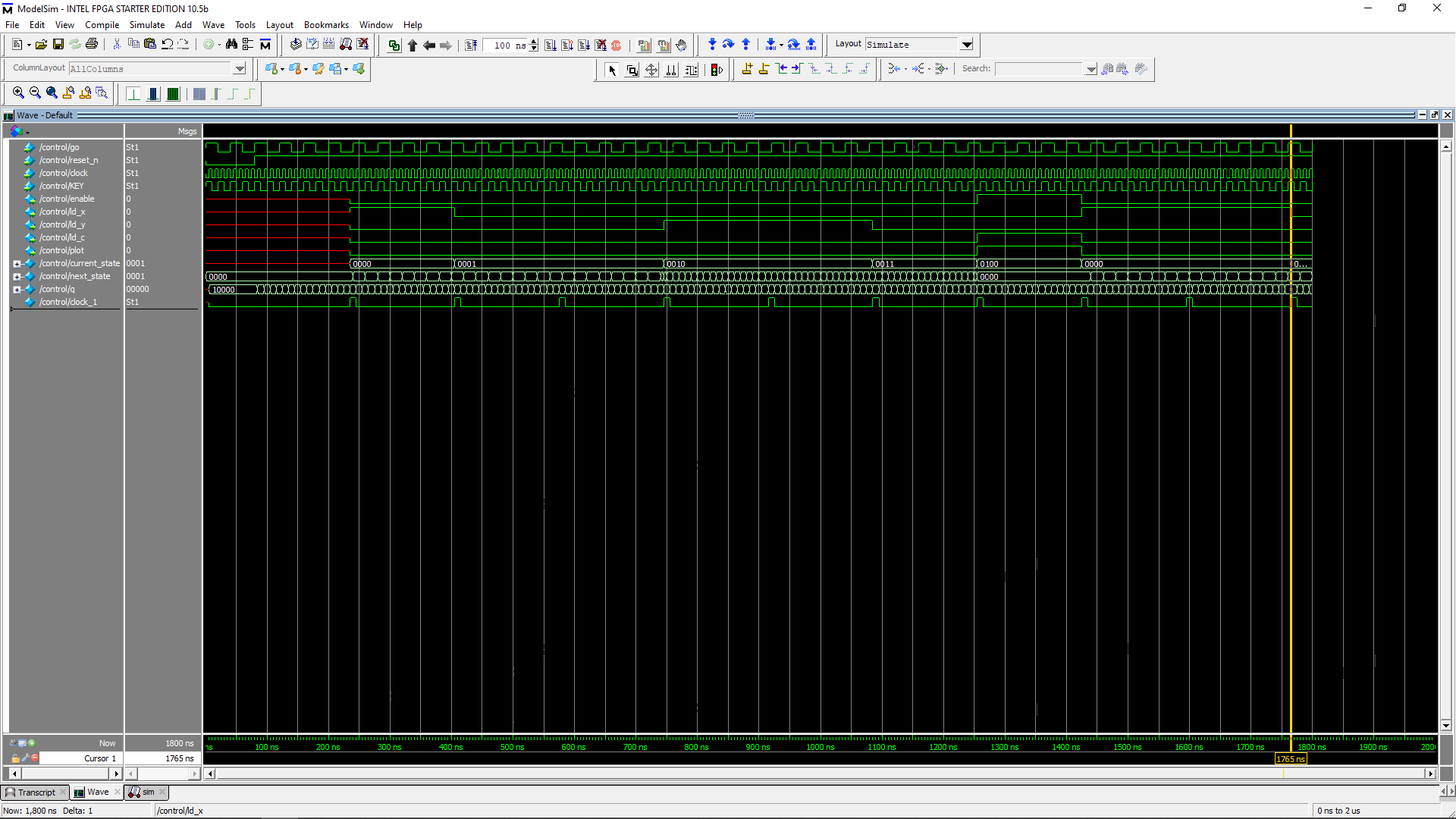
11. 

Schematic for the circuit, with the Keys and switches connected to relevant modules.

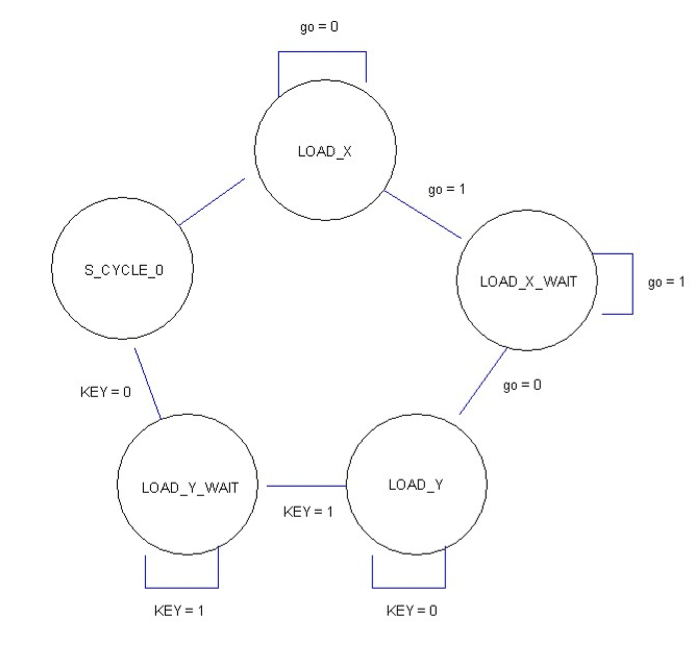
Part II:

1. Code submitted on Quercus.

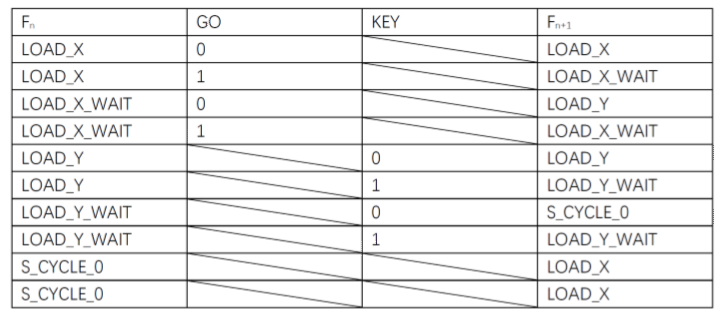
Simulation image:



1. State diagram:



State table:



Simulation of combined circuit:

