EMCR 350 – PMOS Process – Level 1

Oxidation, Lithography, Ion Implantation, RTP/furnace annealing

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PMOS Process

ABSTRACT

The goal of this experiment is to learn the manufacturing process of PMOS transistors and learn the different steps needed to produce functioning PMOS transistors. This paper includes the steps taken to produce the source and drain regions on the transistor (level 1). In order to define the source and drain region a masking oxide is grown, a pattern is transferred to photoresist on the wafer using photolithography, the masking oxide is etched so that the pattern transferred to the photoresist is transferred to the oxide, the photoresist is stripped from the wafer, an ion implantation is carried out and lastly surface anneal is carried out to activate the dopant and repair damage to the silicon surface. Throughout the manufacturing of the first level several process characteristics are measured and discussed.

Keywords: RCA clean, oxidation, lithography, ion implantation, RTP processing, furnace processing, annealing, wet etch, grove and stain

1. INTRODUCTION

Transistors are the basic building block of modern integrated circuits. It is crucial to understand the current process of manufacturing transistors in order to improve the process in the future. In this experiment, the transistors manufactured are p-channel metal-oxide-semiconductor field-effect (PMOS) transistors. The transistors were made on (100) n-type 6 inch wafers. Five wafers are being processed, three of them devices are being built on, and two are control wafers which allow for characterization of different processes.

2. THEORY

2.1 Wafer Preparation – RCA Clean

In order to ensure that the wafer is free of all contaminates a RCA clean is preformed on the wafers several times throughout the whole PMOS process. Removal of contaminates is critical before a high temperature process, else contaminates will diffuse into the silicon crystal, altering the electrical properties. The RCA clean consists of three major steps, removal of organic contaminates, removal of the native oxide, and removal of ionic contamination. Between each step the wafers are rinsed with deionized (DI) water for 5 minutes. The removal of organic contaminates is done by a chemical bath of water (H_2O), ammonium hydroxide (NH_4OH) and hydrogen peroxide (N_2O_2). This bath is often referred to as APM for ammonium-peroxide-mixture. Wafers are put into the APM bath for 10 minutes at 75 degrees Celsius. To remove the thin native oxide from the wafers, the wafers are put into a diluted bath of hydrofluoric acid (HF) for 5 minutes at room temperature. The last step of removing ionic contaminants is preformed with a bath of water (H_2O), hydrogen peroxide (N_2O_2), and hydrochloric acid (HCl). This bath is referred to HPM for hydrochloric-peroxide-mixture. The wafers are put into the HPM bath for 10 minutes at 75 degrees Celsius.

2.2 Oxidation Growth

Silicon dioxide (SiO_2) is used for several purposes throughout the manufacturing process. In the PMOS process silicon dioxide is used as a masking layer for ion implantation, an insulating layer and for the gate-oxide. In order to grow a high quality thick oxide quickly the wafers must be exposed to a high temperature for the interaction of oxygen and silicon to occur. A tube furnace or rapid thermal processing can be used to grow the oxide on the wafer. For this experiment a tube furnace was used in this PMOS process. The rate at which silicon dioxide grows depends on the ambient in the tube and the surface on which the silicon dioxide is being grown on. Two common ambient gases used in the furnace is oxygen, known as dry oxidation, and water, known as steam or wet oxidation. Figure 1 through 3 shows the growth rates of silicon dioxide of dry,

steam, and wet oxidation. It can be seen that steam and wet oxidation grows silicon dioxide much faster than a dry oxidation. The steam oxidation is slightly faster than the wet oxidation.

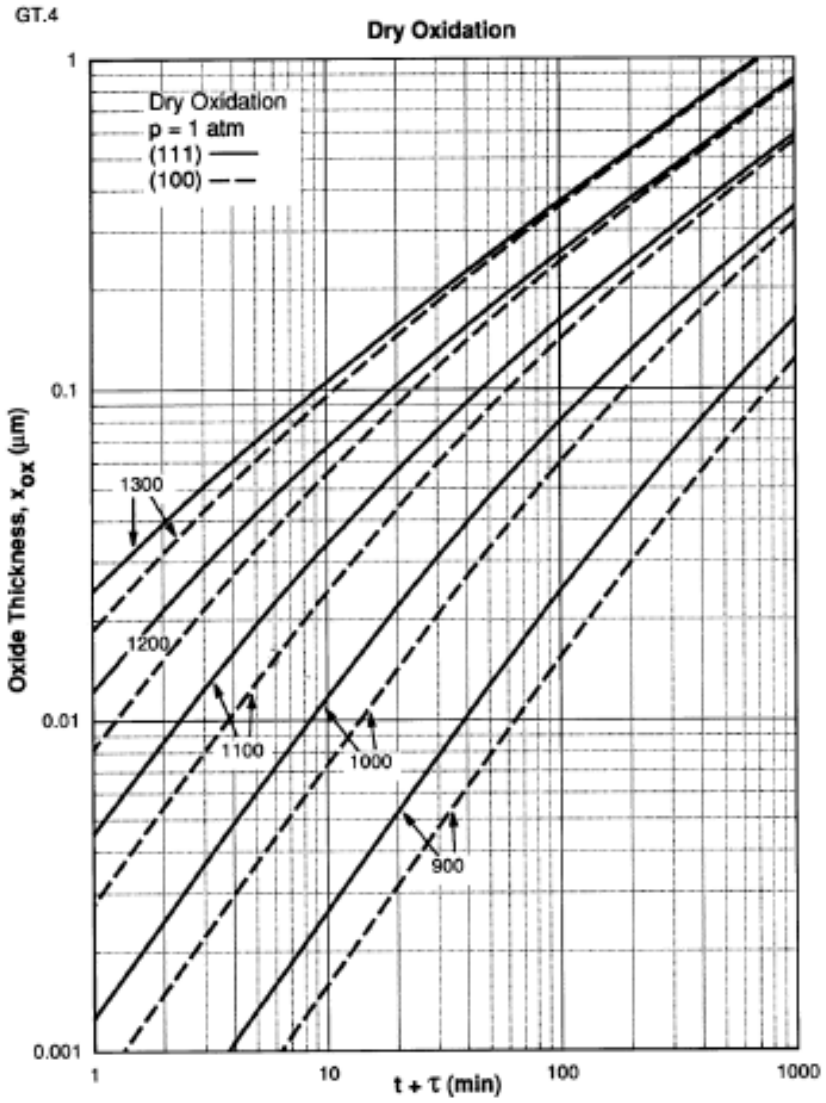

Figure 1. Oxide thickness vs. time of a dry oxidation. [1]

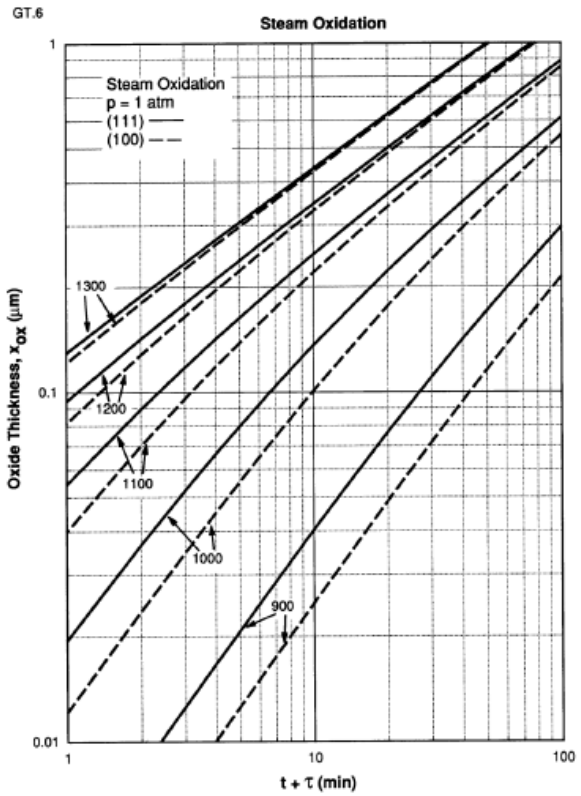

Figure 2. Oxide thickness vs. time of a steam oxidation. [1]

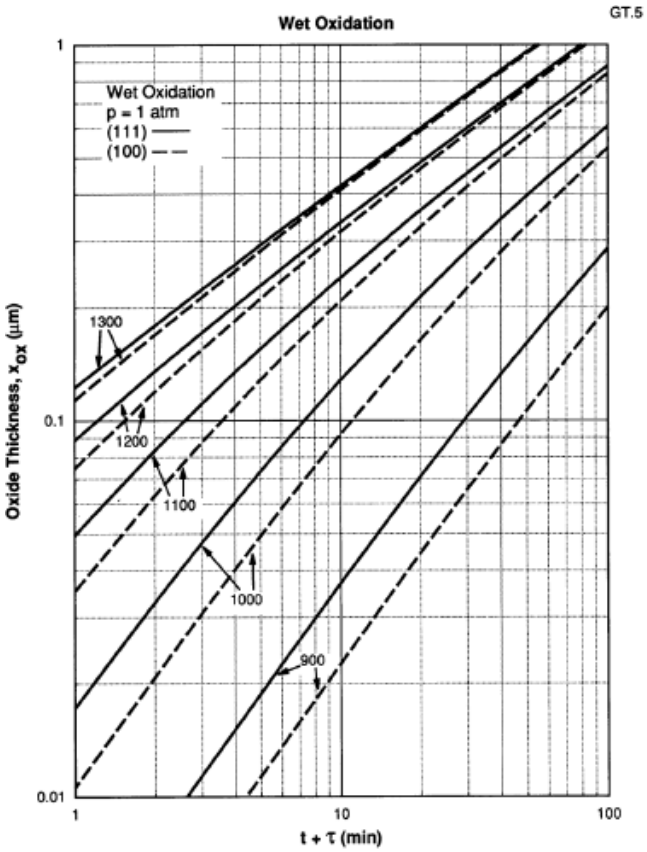

Figure 3. Oxide thickness vs. time of a wet oxidation. [1]

2.3 Substrate Measurements

In order to measure the dopant levels in the substrate a sheet resistance measurement is carried out. A four point probe is used to measure the sheet resistance. The two outer probes induce a current through the wafer, and the two inner probes measure the resulting voltage as a result of the current. Using a modified version of ohm's law to account for the spreading of the current in all directions the sheet resistance is found. Equation 1 shows the modified ohm's law. R_s is the sheet resistance with unites of ohms per square. V is the voltage in volts. I is the current in amps. And $\pi/\ln(2)$ is the adjustment for the spreading of the current.

$$R_s = \frac{V}{I} * \frac{\pi}{ln(2)} \tag{1}$$

Sheet resistance is related to resistivity (ρ), sheet resistance (R_s) and thickness of the wafer (t) by equation 2.

$$\rho = R_S * t \tag{2}$$

Measuring sheet resistance is useful because the sheet resistance is dependent on the carrier mobility and concentration of the dopant. Equation 3 shows how these terms are all related. A numerical analysis approach is required to solve the equation however because the mobility depends on the concentration. This equation assumes that the minority carrier's affect is negligible.

$$R_S = \frac{1}{\int_0^{x_j} \mu q N(x) dx} \tag{3}$$

To measure the oxide thickness the Nanometrics Spectrophotometer, often referred to as Nanospec, is used. The NanoSpec uses monochromatic light to measure the intensity of the reflected light. The intensity depends on the interference that occurs in the oxide. As a result the film thickness can be calculated based on the incident light and intensity of the reflected light.

In order to measure junction depth created by the ion implant a groove and stain process is used. A cylindrical wheel is used to groove the wafer. After the groove is created a stain is used that when it bonds to the doping atom it changes the color of the doped region, allowing for measurement of the p and n regions. The junction depth can be found using equation 4. The junction depth is represented by x_j. The width of the stained area is represented by m and the width in between the two stained areas is represented as n.

$$x_j \approx \frac{m * n}{d} \tag{4}$$

Figure 4 shows an isometric and a top-down view of the wafer after being grooved and stained.

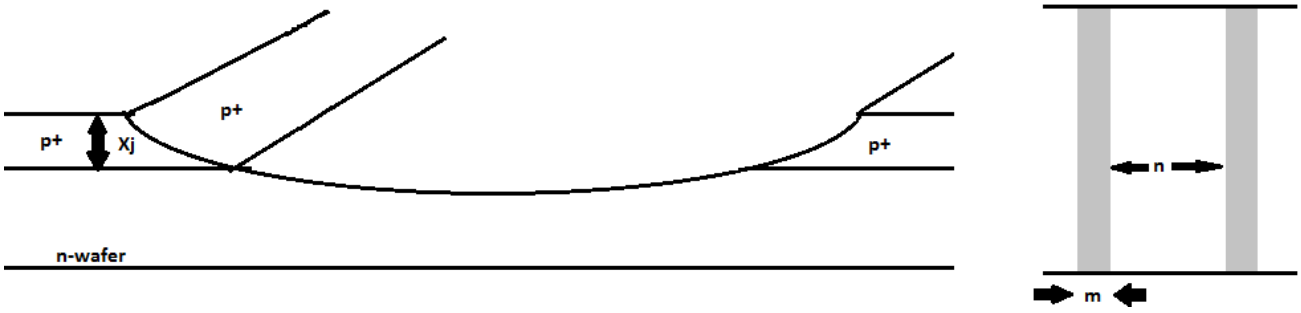

Figure 4. Shows the effects of the groove and stain and what is being measured. Not to scale.

2.4 Lithography

The lithography process allows for the transfer of images from a mask to the wafer. Photoresist is applied to the wafers typically with an automated process using a tool such as a SSI track. First the wafers are primed

with hexamethyldisilazane (HMDS) at 140 degrees Celsius to encourage bonding of the photoresist to the silicon dioxide surface. HMDS drives away any water that may be on the wafer as well. The wafer is then put on a chill plate to ensure it not warm while photoresist is applied. The photoresist is dispensed in the center of the wafer and spins to spread uniformly across the wafer. The wafer is then soft baked at 100 degrees Celsius to reduce the solvent concentration to about 5%. This ensures that the photoresist doesn't spread or move. The photoresist is then exposed to ultraviolet light using a stepper. The wafers are then developed with the SSI track. A post-exposure bake is done at 100 degrees Celsius. The exposure process causes standing waves in the resist-film causing an uneven distribution of the photoactive compound (PAC). The post-exposure bake causes the PAC to diffuse which averages the PAC across the exposed and unexposed boundary. The wafer is put on a chill plate after the bake. Once chilled, CD-26 Developer, based on Tetramethyl Ammonium Hydroxide (TMAH), is used to develop. The developing removes the exposed resist and leaves only the unexposed resist. A hard bake at 140 degrees Celsius is preformed on the wafers after developing. The hard bake drives out any remaining solvent and deactivates the PAC.

2.5 Oxide Etch

After a lithography process the oxide may be patterned to provide a stronger mask than photoresist provides. For example, this is useful for the ion implantation. If photoresist is used as a mask in ion implantation the implant must be done at lower energy or else the photoresist will burn. Oxide is able to handle high temperatures making it useful for a mask layer for ion implantation. In order to pattern the oxide the oxide must be etched. This is done either in a dry or wet etch. A dry etch involves using ions to chemically and physically etch way the oxide. The dry etch is anisotropic and will etch only in one direction. A wet etch is a chemical process done in a bath. The wet etch is an isotropic etch meaning that it will etch in all directions at the same rate. A wet etch main chemical is HF. The bath consists of NH_4F, HF and H_2O in a 5:2:1 ratio, which is called a buffered oxide etch (BOE). The BOE theoretically provides an etch rate of about 1000 angstroms/minute. Depending on when the bath was last made and how much of the chemicals in the bath have been consumed, the etch rate will be variable due to the ratio changing over time and use.

2.6 Ion Implantation

In order to form the source and drain regions on the wafer some areas of the wafer need to be doped p type. In order to dope these areas an ion implanter is used to implant the wafers. Ions are formed by turning a gas source into plasma. The ions are extracted from the plasma by applying an electric field. The extraction voltage is typically around 30 kilovolts. An analyzing magnet is used to extract the desired ions. The Lorentz force from a magnetic field causes the ions to take a curved path depending on the mass of the ion. By adjusting an aperture only the desired ions continue through the rest of the ion implanter. The ions are accelerated using an electric field from 0 to 175 kilovolts. The ion beam is focused with electric fields. Neutral ions are extracted from the beam by using a magnet to apply a slight curvature to charged ions. Electrostatic scanners are used to make the beam scan across the wafer in horizontal and vertical directions. By making the beam scan across the wafer a very uniform doping of ions is achieved.

The dose (ϕ) of the injected ions is a function of the beam current (I), time (t), the ion charge (m), the area (A) of the wafer and the charge of an electron (q), which is defined in equation 5.

$$\phi = \frac{\int Idt}{m * A * q} \tag{5}$$

If the beam current is constant the equation can be simplified and is defined in equation 6.

$$\phi = \frac{It}{m * A * q} \tag{6}$$

The ion implant can be adjusted with the use of a screen oxide. The screen oxide is a thin layer of oxide. The oxide allows for the peak of the dopant to be adjusted, the randomness of the path of ion is increased which decreases tunneling and provides a dopant cap which prevents the dopant from diffusing from the silicon to the ambient air. Tunneling occurs when the dopant ion enters a tunnel in the silicon, and "bounces" around in the tunnel rather than hitting silicon atoms and stopping. This results in the dopant ion to go further into the material.

The resulting concentration of dopant atoms is defined by several characteristics. The doping concentration tends to follow a Gaussian curve. This curve is described by the peak concentration (N_{Rp}), the depth into the silicon (x), the straggle (ΔR_p) or in statistical terms the standard deviation, and the projected range (R_p), or in statistical terms, the average projected range. Equation 7 shows the concentration as a function of distance into the silicon.

$$N(x) = N_{Rp} * \exp\left[\frac{-(x - R_p)^2}{2\Delta {R_p}^2}\right] \tag{7}$$

The peak concentration is a function of the straggle and dose and is defined in equation 8.

$$N_{Rp} = \frac{\phi}{\sqrt{2\pi}\Delta R_p} \tag{8}$$

The projected range and straggle is a function of the ion's kinetic energy and mass as it comes into contact with the wafer. This function can be seen in figure 5 and 6.

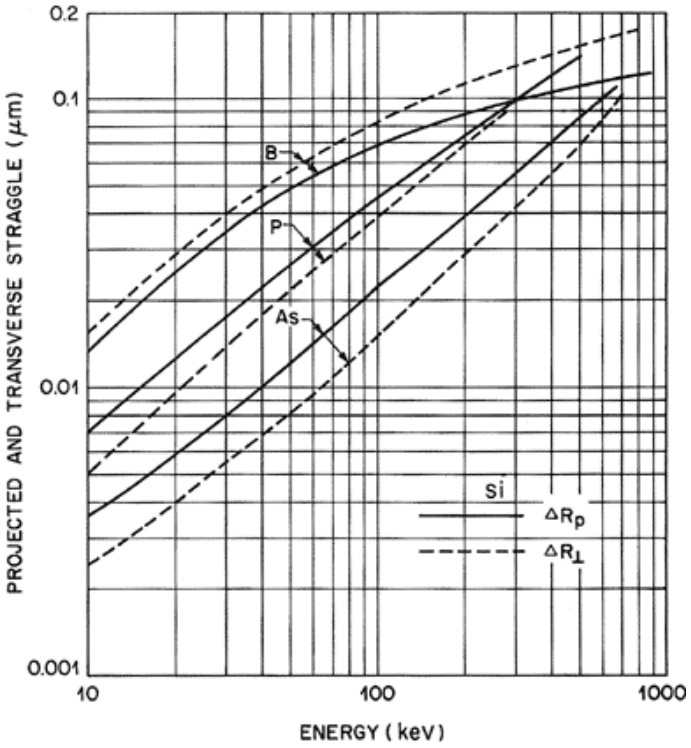

Figure 5. The projected and transverse straggle as function of atom and energy. [2]

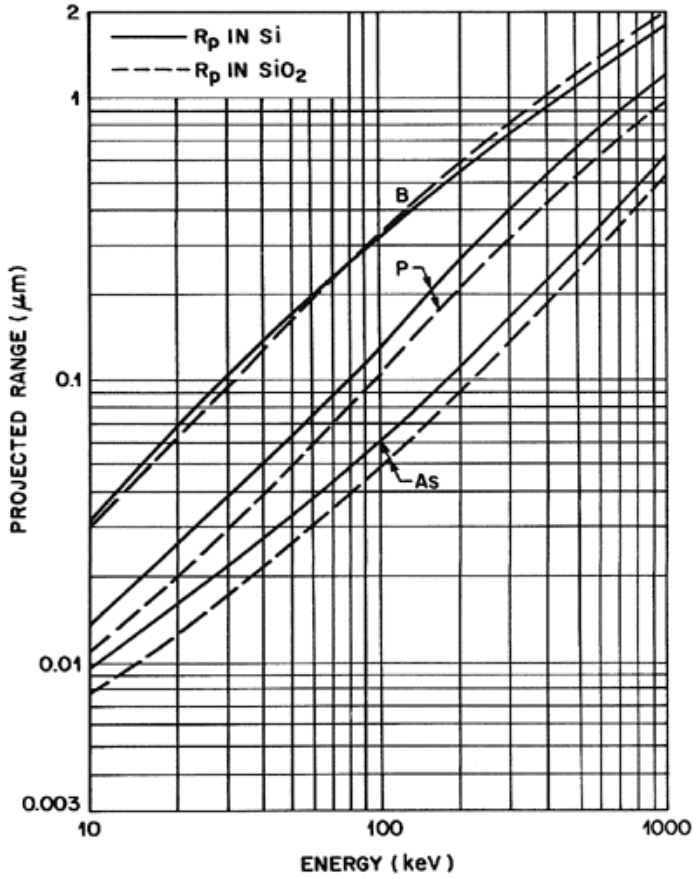

Figure 6. The Projected range as a function of energy and atom. [2]

2.7 Furnace and Rapid Thermal Anneal

The ion implantation damages the surface of the layer which causes it to behave like amorphous silicon. Amorphous silicon does not conduct electricity well. The dopants are not part of the crystal after implanting them into the wafer as well. In order to repair damage and make the dopants become part of the silicon crystal structure the wafer must be annealed. To anneal the wafer it can be placed in a furnace at high temperature or put through a rapid thermal process which rapidly heats the wafer to the desired temperature for short period of time and then rapidly cools the wafer.

3. EXPERIMENTAL PROCEDURE

Throughout the experiment there are five different 6 inch wafers being processed. Two of the wafers are control wafers (C1 and C2) which are being used to measure and characterize the different processes throughout the experiment. The other three wafers are device wafers that will be eventually be used to measure and characterize the transistors that are produced. All of the wafers were first characterized by measuring the sheet resistance. The sheet resistance was measured by using the CDE ResMap. After characterizing of the wafers they were put through an RCA clean to remove any contaminates. The first level of the PMOS process involves creating drain and source regions on the wafer. In order to define the source and drain regions a masking oxide is grown in a wet furnace. Furnace recipe 406 was used on the Bruce Furnace in tube one. The oxidation recipe is for 6500 angstroms of silicon dioxide. For furnace recipe details refer to the appendix.

After growing oxide on the wafers the first level of the transistor is patterned on the device wafers through a lithography process. The SSI track was used to coat the wafers with the HPR 504 positive photoresist. The GCA 6700 stepper was used to expose the device wafers. After exposing the wafers the SSI track was used to develop them. The wafers were inspected under a microscope to confirm that the pattern transferred to the photoresist and provided a good pattern. After development of the photoresist on the device wafers were etched using a BOE. Before etching the device wafers a control wafer was used to do a step etch. Every 30 seconds the wafer being step etched was lowered in the BOE etch another step. The step etched wafer allows for a measurement of the etch rate of the BOE. The device wafers and the other control wafer were etched for eight minutes to ensure the silicon dioxide was completely etched. After rinsing and spin drying the etched wafers they were inspected under the microscope to ensure the oxide completely etched. The photoresist was then stripped from the wafers and again the wafers were inspected under the microscope.

The photoresist was stripped from the wafers using the Branson Asher. The Branson Asher uses oxygen plasma to remove the photoresist. The photoresist is removed from the wafers in order to prepare them for ion implantation. Leaving the photoresist on the wafers would have required a lower beam current to be used by the ion implanter; otherwise the photoresist would burn and leave undesired residues. In order to get the same dose, it would have taken longer to implant the wafers.

The Varian 350D Implanter was used to implant the device wafers and the control wafers with Boron-11. The desired implantation dose is 2E15 cm^{-2}. The energy used to expose the wafers was 75 keV.

In order to repair silicon crystal damage and electrically activate the dopants the device wafers are annealed in a wet oxidation. A wet oxidation was used to anneal because the next step of the PMOS process was to build a thin gate oxide. In order to define the thin gate oxide it is needed to have silicon dioxide on the whole wafer for level 2 lithography. By using a wet oxide to anneal the oxide is grown at the same time, effectively combining the two steps. The wet oxide growth was done in the Bruce Furnace tube 1, with recipe #341 which grows 4000 angstroms of oxide. For details on the recipe see the appendix.

The control wafer that was previously stepped etch, photoresist was applied to the wafer in stripes perpendicular to the steps in order to provide a ruler for where the steps exist. The step etched control wafer was then etched to remove all of the silicon dioxide. The sheet resistance was measured for each step. The other control wafer was implanted everywhere (no masking oxide). This control wafer was used to measure the sheet resistance after implantation and furnace annealing. A new wafer (RTP wafer) was introduced in order to characterize the rapid thermal anneal. This wafer was implanted with the rest of the wafers and was not annealed in the furnace like the other wafers. The RTP wafer went through rapid thermal annealing in the AG 610 Rapid Thermal Annealer. The recipe used to rapid thermally anneal can be seen in the appendix. After the RTP wafer was annealed the sheet resistance was measured.

The step etched wafer was used to measure the junction depth of the doping by using a groove and stain process. After grooving and staining the wafer, the Unitron TM8-3959 was used to measure the width of the dosed and not dosed parts of the groove. The step etched wafer is not used in any future parts of the experiment after being grooved and stained.

4. RESULTS AND ANALYSIS

The wafers were provided with information from the manufacturers of the wafers. The dopant used in the ingot growth was phosphorus and thus the wafers are n-type. The resistivity of the wafers are anywhere from

4 to 7 ohm centimeters. The oxygen level in the wafers is 25.5 to 30.5 ppm. The wafer thickness is 610-640 micrometers. From here on out wherever the thicknesses of the wafers are required it will be assumed that they are 625 micrometers. In order to characterize the resistivity and sheet resistance of the wafers the ResMap was used. The results that the ResMap generates can be seen in figure 7.

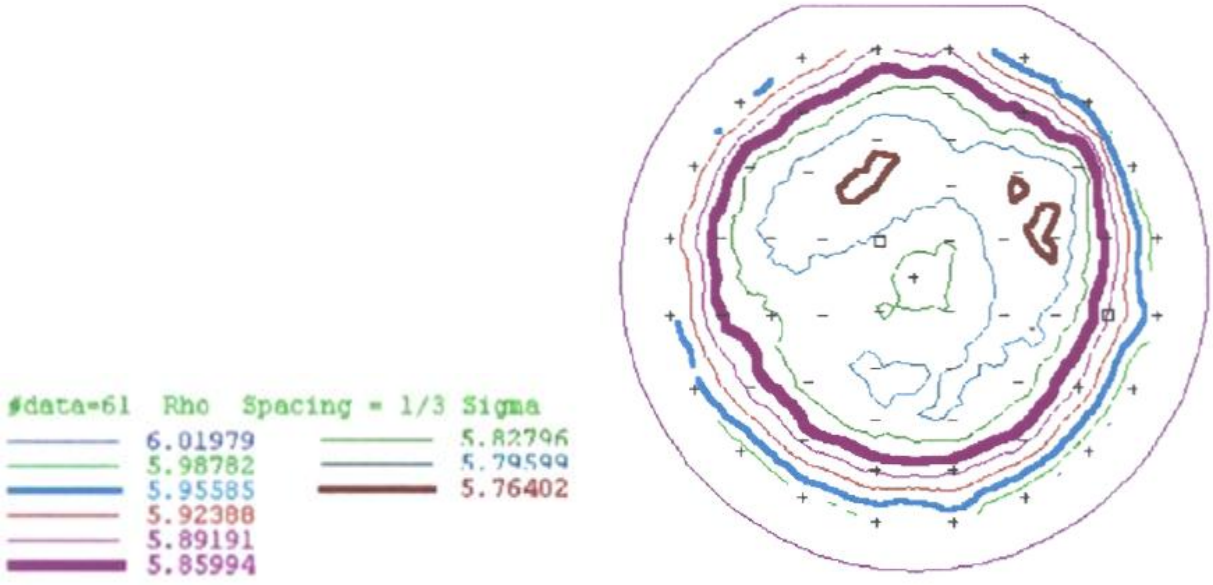

Figure 7. The ResMap generated from a 61 point measurement. Has a bull-eye pattern.

The results that the ResMap for the incoming wafers all have a similar bulls-eye pattern seen in figure 7. The bulls-eye pattern is a result of how a Czochralski(CZ) crystal is grown. A CZ crystal is grown from a crucible full of molten silicon with some initial dopant. A seed crystal is lowered into the crucible and pulls out of the molten silicon while spinning. The spin causes the crystal to grow in a cylindrical shape and also stirs the dopants around. The edges of the crystal will be moving faster causing more stirring motion than the center. As a result, the resistivity reflects the dopant concentration that results from the CZ crystal growth. The measurement program used and the results of the measurement can be seen in table 1. It is seen that the resistivity of the wafers are very similar to each other. As a result when the transistors are characterized there will likely be little variation in behavior of the transistors because the dopant levels are about the same amongst the wafers.

Wafer	Program	Avg. Resistivity (ohm cm)	Std. Dev.
C1	61 pt	5.860	95.914m
C2	61 pt	5.958	0.1165
D1	1 pt	5.855	N/A
D2	1 pt	5.865	N/A
D3	1 pt	6.135	N/A

Table 1. Shows the measurement results of the ResMap on the incoming wafers.

After oxide growth the Spectromap was used to measure the oxide thickness. The Prometrix Spectramap works in the same way as the Nanospec described in the theory section except it is automated and measures several spots on the wafer and generates some basic statistics of the oxide. Table 2 shows the measurement results for the control wafers. The device wafers were not measured because they were already being processed for lithography. The oxide recipe read 6500 angstroms of growth; the wafers ended up with about 200 more angstroms which is acceptable because it is a masking oxide for implantation.

Wafer	Avg. Oxide Thickness (Angstroms)	Std Dev. (Angstroms)	Max (Angstroms)	Min (Angstroms)
C1	6707.6	27.104	6736.7	6665.0
C2	6697.3	20.078	6740.4	6660.0

Table 2. Shows the measurement results from the Spectramap.

The wafers were exposed to the level 1 pattern using the GCA stepper. The exposure time per die was 2.8 seconds. The vernier after photoresist development can be seen in figure 8. The verniers are equal lines of equal width and spacing. The lines are photoresist and the spaces are the silicon dioxide. It can be seen that the 1 micron lines are very close to each and most likely will not resolve once etched. The spaces are larger than the lines due to overexposure of the photoresist. This is acceptable for this process because the transistors being produced have large critical features. The minimum feature size that will be present after etching will be the 2 micron lines.

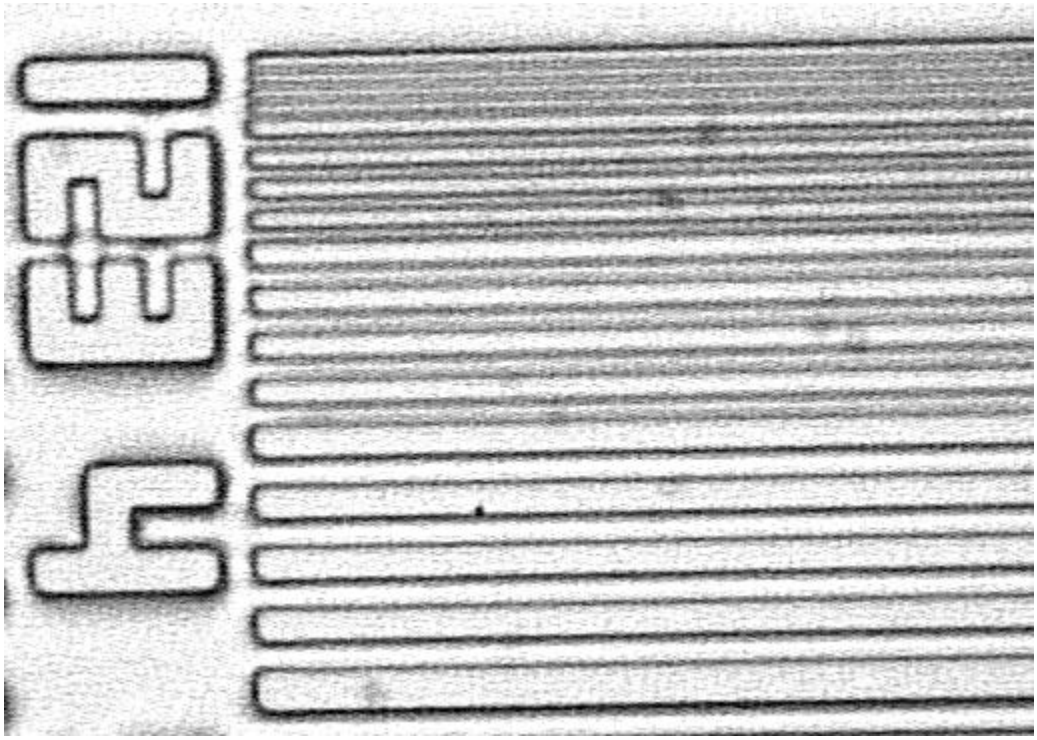

Figure 8. The level 1 verniers before etching SiO_2.

One of the control wafers (C1) were stepped etch in order to get a measurement of the etch rate of the buffered oxide etch (BOE). By graphing the oxide thickness and time etched it is possible to build a graph. Taking the slope of the data will provide an etch rate for the BOE. Figure 9 shows the oxide thickness vs. etch time. It is seen that the slope of the line is about -14. This equates to the BOE etching the SiO_2 at a rate of 14 angstroms/second which is about 840 angstroms/minute. This is somewhat lower than the expected 1000 angstroms/minute. This lower rater than expected can be a result of the ratio of HF, H_2O and NH_4F not being in balance. The ratio changes as chemicals are consumed from etching other wafers and from decomposing over time.

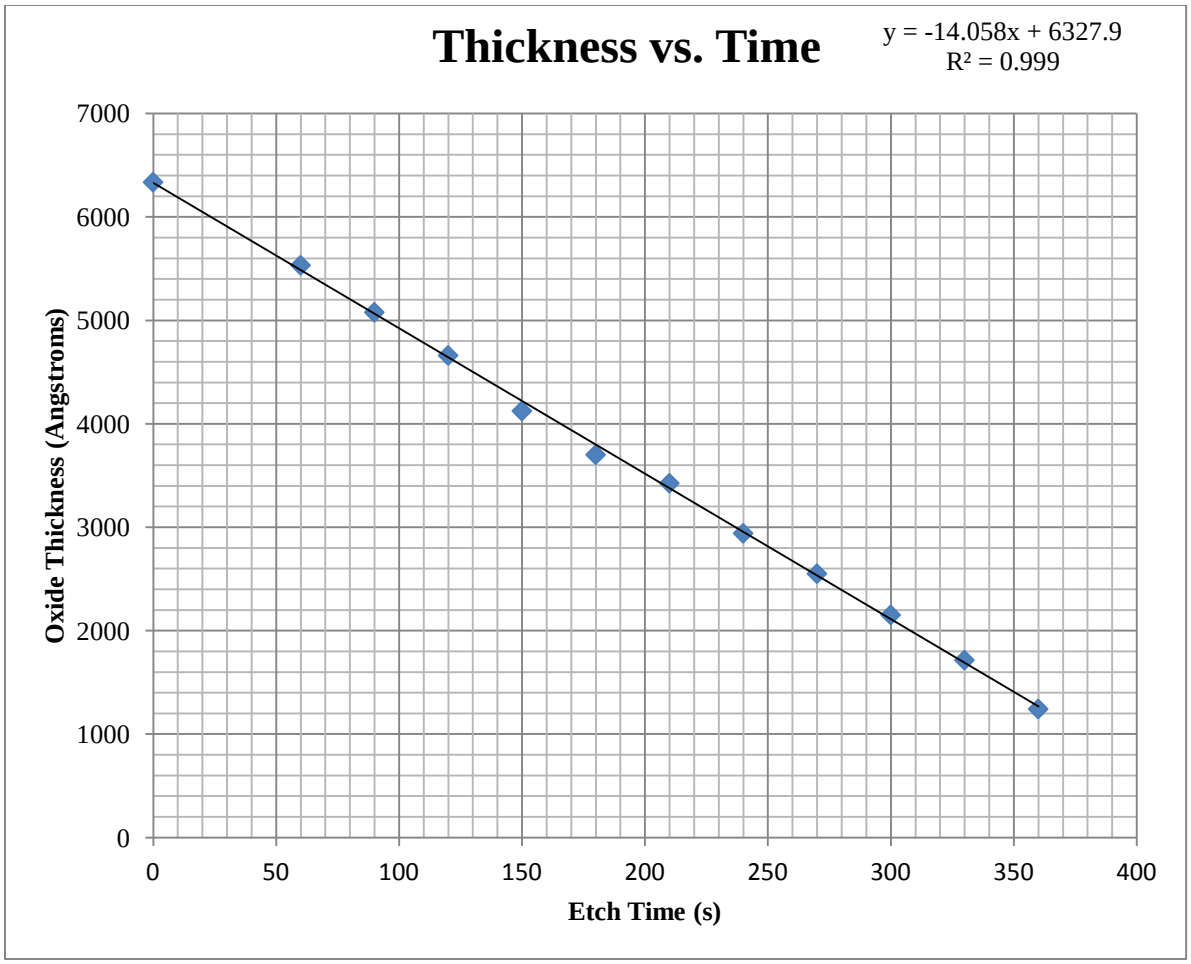

Figure 9. Oxide thickness vs. Time. The slope of the line is the etch rate.

The device wafers were etched for 8 minutes. At the time it was assumed the BOE etched at 1000 angstroms per minute. This would have been an over etch of about 20%. An over etch is typically conducted to ensure the wafer is completely etched. However the etch rate was found to be 840 angstroms per minute. This means there was very little over etch because the wafers had a oxide layer that was about 6700 angstroms. At an etch rate of 840 angstroms per minute the total amount etched would be 6720 angstroms. If there was a thin oxide layer remaining this would have been acceptable because the next step is an ion implant. The thin oxide layer would have simply acted like a screening oxide.

Figure 10 shows the etched verniers. The lines are silicon dioxide and the spaces are bare silicon. It can be seen that the 1 micron lines did not survive from the etching process. While there was photoresist defining the 1 micron lines, the wet etch process is isotropic. As a result, the wet etch undercut the photoresist. This resulted in larger spaces than the photoresist pattern showed.

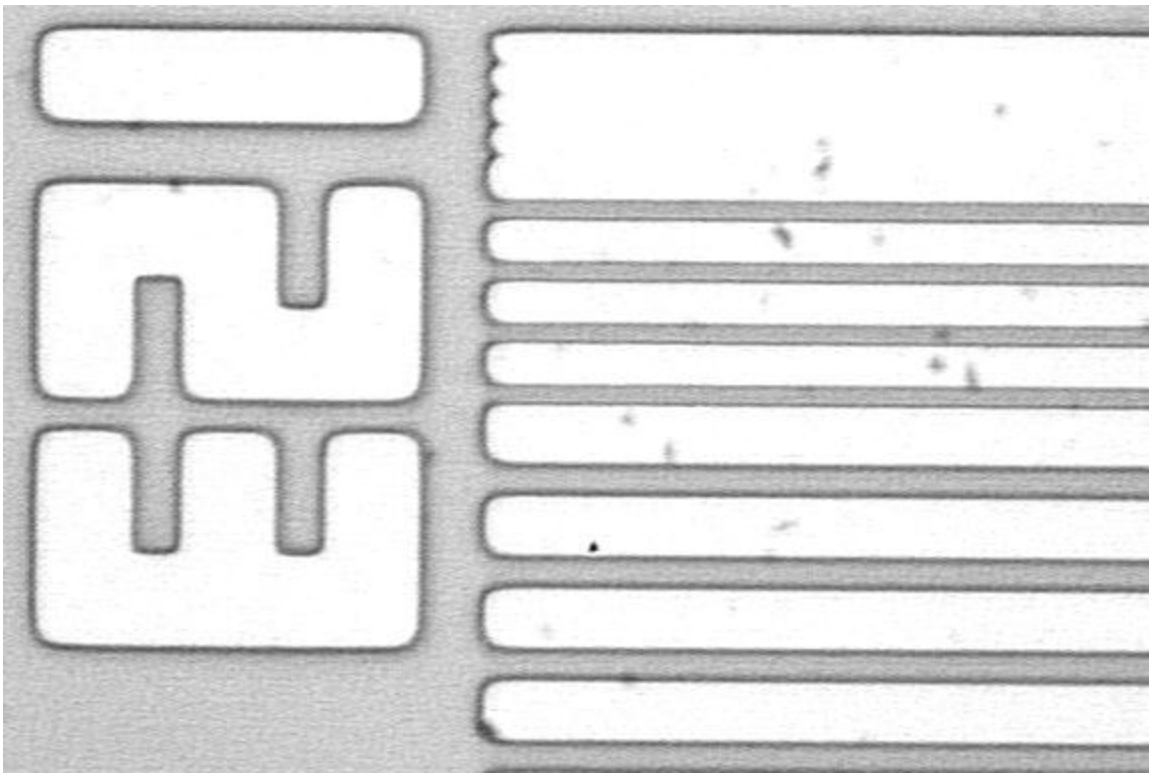

Figure 10. Level 1 Verniers post-etch.

The ion implantation was carried out on all of the wafers with Boron-11. The source gas used was BF_4. The desired dose was 2E15 cm^{-2}. The ion beam averages 90 microamps. The wafers were taking about 10 minutes each to be implanted. Before annealing the wafers there was observable clipping to the silicon dioxide. The damage was observable only because the damage altered the refractive index of the silicon dioxide. There was no observable damage on the bare silicon. Boron ions typically cause a damaged subsurface which is only observable through a sheet resistance measurement.

The wafers were annealed in the furnace with a goal oxide growth of 4000 angstroms. Silicon dioxide grows at different rates depending on the current oxide thickness. The bonding of the silicon and oxygen occurs at the silicon and silicon dioxide interface. As more silicon dioxide is present, the amount of oxygen that will diffuse through the silicon dioxide to the interface decreases. The areas where the 6500 angstroms of silicon dioxide will only grow about 1500 angstroms of silicon dioxide as a result, this totals to 8000 angstroms in these areas. The Spectramap was used to measure the silicon dioxide layer. Table 3 shows the measurement results from the Spectramap. It can be seen on C2 that the oxide thickness is near the goal of 400 angstroms and that on D1 the oxide thickness is near 8000 angstroms. It is acceptable to use the patterned device wafer for the oxide thickness because most of the wafer is the thicker oxide. The probably of the machine measuring a patterned part of the wafer is low.

Wafer	Mean (Angstroms)	Std. Dev. (Angstroms)	Max (Angstroms)	Min (Angstroms)
C2	3863.2	20.614	3900.0	3821.6
D1	7888.6	26.627	7942.5	7834.0

Table 3. The Spectramap results of oxide thickness post anneal.

A new wafer was implanted with no oxide and was not annealed in the steam furnace. This was annealed using a rapid thermal process. The rapid thermal anneal quickly ramps the temperature up to about 1000 degrees Celsius and then ramps back down. Before the repaid thermal anneal, measurement of sheet resistance was attempted using the four point probe. However the four point probe was unable to measure a sheet resistance. This is because of surface damage from the ion implant and the inactive dopants. The four point probe measured a resistivity of 4.8 ohm centimeters on the backside of the wafer. This is slightly lower than the resistivity measured on the control and device wafers. This could be a result of the backside of the wafer not being polished, or the wafer came from a different part of the silicon ingot. The wafer was put through a rapid thermal anneal. After the rapid thermal anneal the ResMap was used to generate a sheet resistance map and generate some basic statistics about the sheet resistance of the wafer. Figure 11 shows the sheet resistance map. Based on the legend of the sheet resistance map it is seen that the sheet resistance is very uniform.

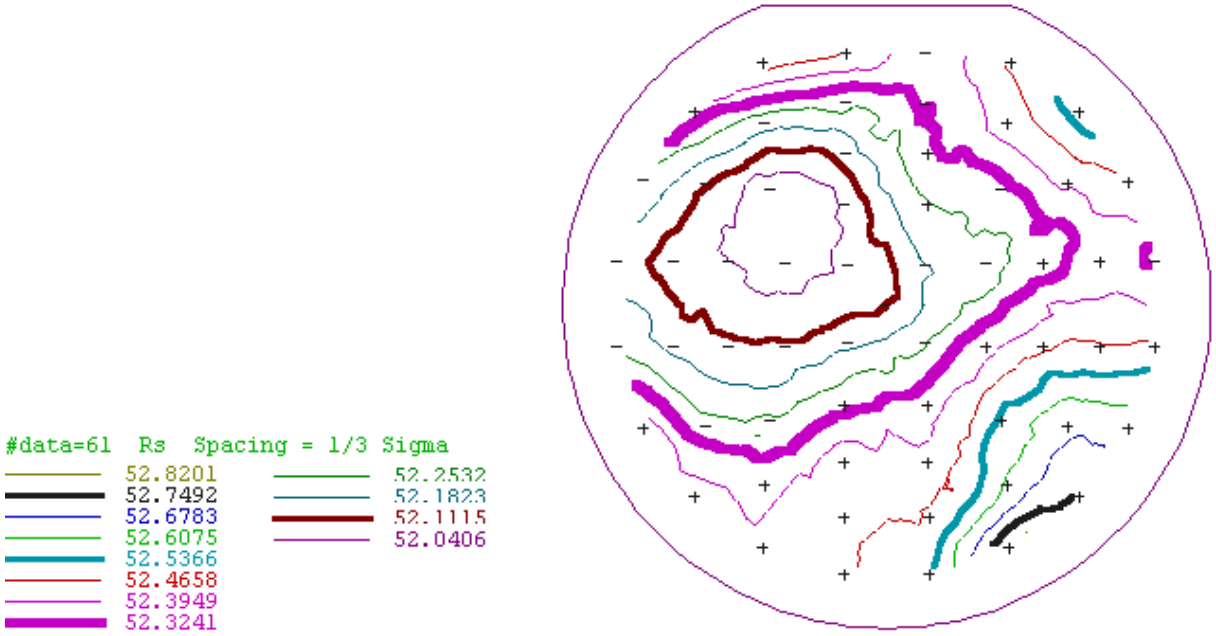

Figure 11. Shows the sheet resistance map of the RTP wafer.

The second control wafer's oxide was stripped away from the wafer using a BOE. The ResMap was used in order to generate a sheet resistance map. Figure 12 shows the resulting sheet resistance. Based on the legend the sheet resistance varies largely compared to the sheet resistance of the RTP wafer. The pattern also resembles the bulls-eye pattern that was present at the beginning of the process but is more oval shaped than circular. This could be a result of the slow increase and decrease of temperature that the wafer experiences in the furnace tube.

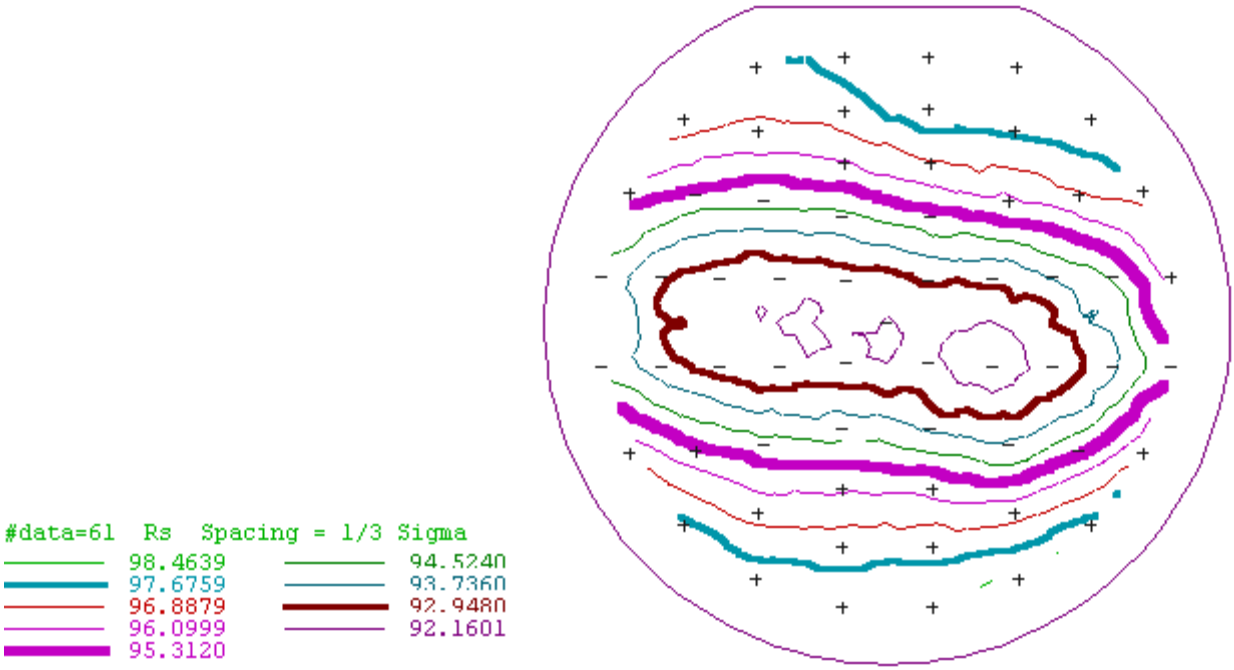

Figure 12. Sheet resistance map of Control Wafer 2.

A ResMap was generated for the backside of the C2 as well. The appearance of it was very similar to the front side of C2 and the values were very similar to the original front side of the wafer (pre-doping). The statistics generated during the ResMap of the RTP wafer and C2 (front and back) are shown below in table 4. It can be seen that the variance of the sheet resistance in the RTP wafer is very low in comparison to the variance in sheet resistance of C2.

Wafer	Avg. Sheet Resistance (ohm/square)	Std. Dev. (ohm/square)	Max. (ohm/square)	Min. (ohm/square)
RTP	52.3241	0.21257	52.899	51.830
C2 (Front)	95.3120	2.36392	99.000	90.414
C2 (Back)	98.5660	1.69304	103.07	94.428

Table 4. ResMap values of the RTP wafer, C2 front and back after annealing.

It is seen that the sheet resistance from the front and back sides of C2 are very similar. This is a result of how dopant levels affect sheet resistance. By measuring the sheet resistance of C1 for each step it is possible to see how different amount of dopant levels affect the sheet resistance. The general trend is as the dopant increases the sheet resistance gradually increases. Once the dopant concentration reaches a certain point, the sheet resistance increases exponentially. Again, up to a certain point where it almost instantly drops back to the same sheet resistance before it exponentially increased. Figure 13 shows the graph of masking oxide thickness related to sheet resistance.

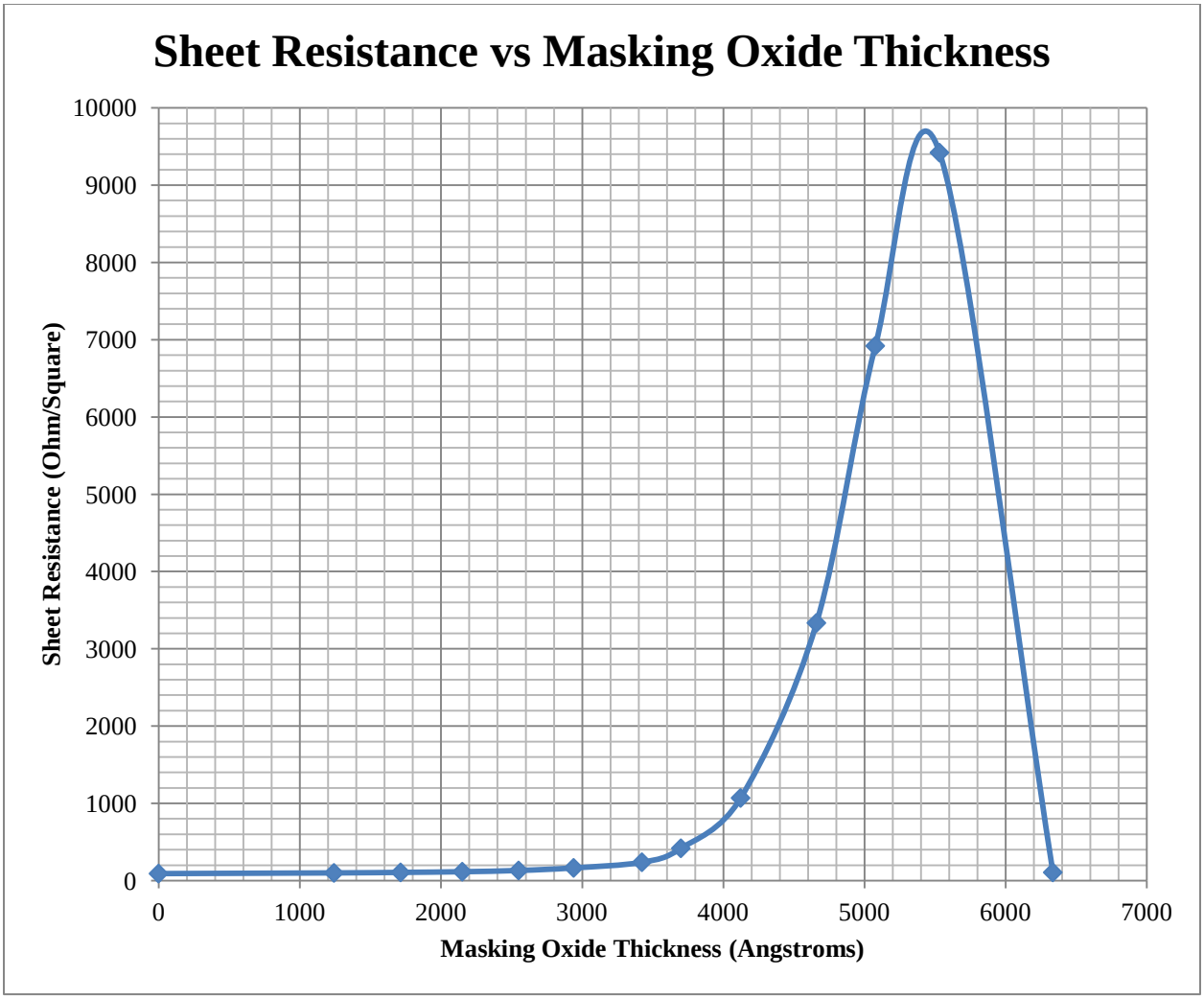

Figure 13. Masking oxide thickness vs. sheet resistance – constructed from data collected on C1.

As the p type dopant concentration increases it starts to approach n-type dopant's concentration. If the dopant levels are equal they will cancel each other, causing the net dopant to approach zero. The lack of doping causes the silicon to behave like intrinsic silicon. Intrinsic silicon behaves very much like an insulator, which has high resistance.

A groove and stain was carried out on control wafer 2. Several different groove and stains were carried out on C2. The results of the groove stain can be seen below in table 5. Equation 4 was used to solve for the junction depth. The wheel diameter was 1.532 inches.

Wafer	m (inches)	n (inches)	x_j (microns)	Time grooved for (s)
C2 – First measurement	0.00245	0.04117	1.67	~ 15
C2 – Second measurement	0.00388	0.03464	2.33	~ 10
RTP	0.00213	0.03015	1.06	~ 4 to 5

Table 5. The measurements from the groove and stain.

The time that the groove and stain takes place affects the depth the groove. The machine that creates the groove puts the wafer on a spring to provide constant force on the wafer into the wheel. If the groove becomes too deep, the small angle approximation used to define equation 4 will become invalid.

A simulation program called ATHENA is used to simulate the implant process. Figure 14 shows the implant profile prior to growing the silicon dioxide. It is seen that the graph does not follow a purely Gaussian curve. This is a result of the simulation using a Dual-Pearson approximation. ATHENA extracted a junction depth of 0.688 micrometers from the top of the silicon wafer. Using an online calculator[1] the substrates concentration is found to be 7.56E14 cm^{-3}. Using that value and equation 7 it is possible to calculate the theoretical junction depth of 0.6 micrometers. The theoretical calculation is different from the simulation because the theoretical calculation assumes a Gaussian distribution, while the simulation uses a Dual-Pearson distribution.

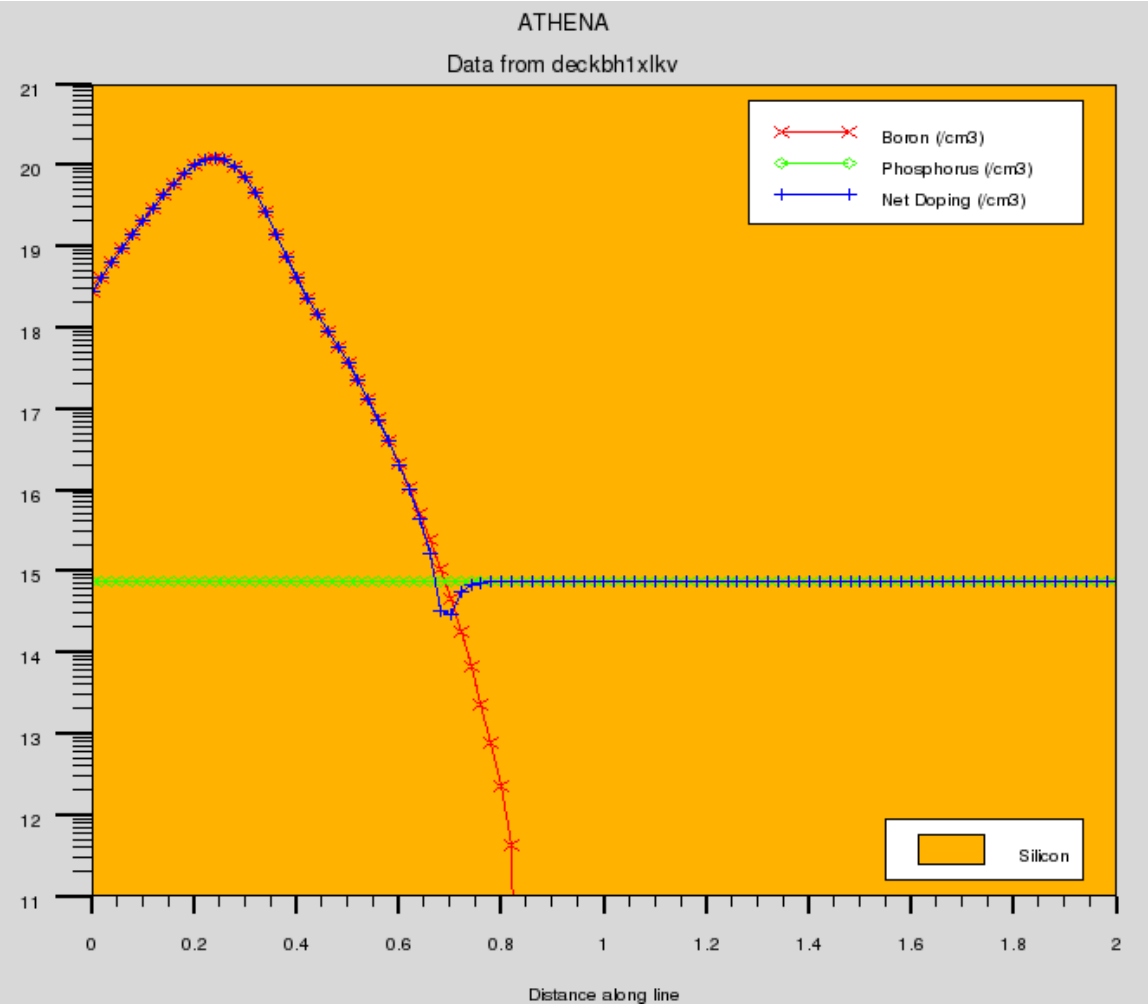

Figure 14. The simulated implant profile prior to oxide growth. The x- axis is distance in micrometers and the y-axis is concentration in cm^{-3}

ATHENA is used to simulate the annealing and oxide growth at 1100 degrees Celsius in a wet furnace for 25 minutes, which is similar to recipe 341. ATHENA found that 4161 angstroms is grown, slightly more than what was actually grown. ATHENA found the junction depth after oxide growth to be 1.239 micrometers. This value is closer to the first groove and stain measurement of 1.67 micrometers. There is a large amount of uncertainty associated with the groove and stain method, which is why the values are different. ATHENA calculates a sheet resistance of 96.59 ohms per square. The simulated value is very close to the sheet resistance measured on C2, which was 95.3 ohms per square. Figure 15 shows the ATHENA implant profile

[1] http://www.solecon.com/sra/rho2ccal.htm is the online calculator used to calculate the concentration of the substrate.

simulated after the oxide growth. It can be seen that about half of the implant dose absorbed by the silicon dioxide.

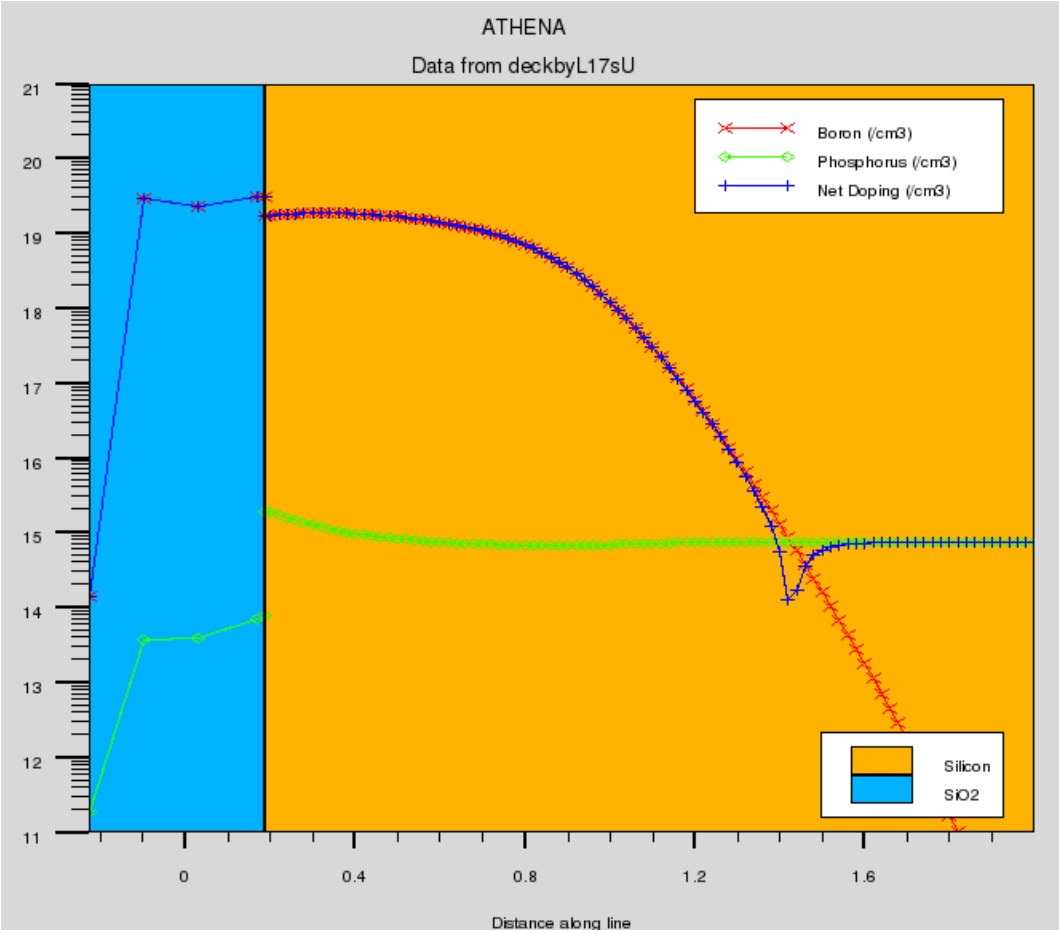

Figure 15. Simulated implant profile post oxide growth. The x- axis is distance in micrometers and the y-axis is concentration in cm^{-3}

5. CONCLUSIONS

By carrying out the first level of the PMOS manufacturing process, the steps involved in created the first level were explored. It was observed that Czochralski grown wafers have a bulls-eye pattern for the resistivity as a result of the spinning motion the crystal undergoes during growth. The initial wafers had a resistivity of about 5.9 ohm centimeters. Using an online calculator it was found that the substrate concentration of n-type dopant is 7.56E14 cm^{-3}. An oxide recipe that grows about 6500 angstroms of oxide was carried out. It was found that about 6700 angstroms of oxide actually grew on the wafers. The wafers were then patterned using lithography and then etched. It was found that the etch rate of the buffered oxide etch was 840 angstroms per minute. The wafers were then implanted with boron-11. The wafers were then annealed in the tube furnace with a recipe for 4000 angstroms of oxide. It was found that about 3800 angstroms of oxide grew on the wafers. After implant the wafers were found to have a sheet resistance of 95.312 ohms per square. The sheet resistance pattern resembled the initial pattern of the original substrate. A wafer was annealed with a rapid thermal process and it was seen that the sheet resistance was extremely uniform. With the step etched wafer it was seen that 6500 angstroms was the amount needed to block the implant enough for the electrons to remain the majority carrier in the n-type regions. In future processing it might be desired to grow a thicker masking oxide layer, because the masking oxide was almost not thick enough. The junction depth of the

implant was found to be 1.67 microns from a groove and etch process. An ATHENA simulation was carried out and it was found that the theoretical junction depth is 1.239 microns.

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APPENDIX

Furnace recipe 406

Step	Time	Temperature (degrees Celsius)
Boat Out	0:00:00	25
Push In	0:12:00	25
Stabilize	0:15:00	800
Ramp to 1100	0:30:00	1100
02 Flood	0:05:00	1100
Soak	1:07:00	1100
N2 Purge	0:05:00	1100
Ramp Down	0:55:00	25
Pull Out	0:15:00	25

Furnace recipe 341

Step	Time	Temperature (degrees Celsius)
Boat Out	0:00:00	25
Push In	0:12:00	25
Stabilize	0:15:00	800
Ramp Up	0:30:00	1000
02 Flood	0:05:00	1100
Soak	0:25:00	1100
N2 Purge	0:05:00	1100
Ramp Down	0:60:00	25
Pull Out	0:15:00	25

Rapid thermal anneal recipe

Step	Time(s) or Rate(C/s)	C
Delay	5	
Ramp	50	1000
Steady State	60	1000
Ramp	50	
Delay	5	

Athena Code to produce simulation

```
go athena
#x simulation area
line x loc=0.00 spac=0.10
line x loc=1.00 spac=0.10
#y simulation area.
line y loc=0.00 spac=0.02
line y loc=2.00 spac=0.02

#initalize the wafer!
init silicon phosphor resistivity=6 orientation=100
#do the implant
implant boron dose=2.0e15 energy=75 tilt=7 rotation=45 crystal

#get the junction depth.
extract name="xj1" xj material="Silicon" mat.occno=1 x.val=.5 junc.occno=1

#get the rs1 value
extract name="rs1" p.sheet.res material="Silicon" mat.occno=1 x.val=.5 region.occno=1

#get the dose
extract name="dose" area from curve(depth,impurity="Boron" material="Silicon"
   mat.occno=1 x.val=.5)/10000

#graph it
tonyplot

#do the diffusion
diffus time=25 temp=1100 weto2
```

```
#graph it
tonyplot

#get oxide thickness
extract name="Xox" thickness material="SiO~2" mat.occno=1 x.val=.5

#get the junction depth after diffusion
extract name="xj2" xj material="Silicon" mat.occno=1 x.val=.5 junc.occno=1

#get the get the sheet resistance
extract name="rs2" p.sheet.res material="silicon" mat.occno=1 x.val=.5 region.occno=1

#get the dose!
extract name="dose2" area from curve(depth,impurity="Boron" material="Silicon"
   mat.occno=1 x.val=.5)/10000)

quit
```