EMCR 350 – SUPREM PMOS Simulations and IC Layout

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SUPREM PMOS Simulations and IC Layout

ABSTRACT

The goal of this experiment is to introduce the layout and simulation software and process for integrated circuits. IC Layout design rules are explored for transistors and resistors. Four devices are laid out using IC Layout, two resistors and two transistors. The PMOS process is simulated with ATHENA. By comparing the simulation results to the actual measurements of the process it is seen that the simulation accurately modals the manufacturing process results.

Keywords: Silvaco SUPREM-IV (ATHENA), IC Station (CAD), Design Rules, Diffusion, MOSFET, PMOS, PFET

1. INTRODUCTION

Transistors are the basic building block of modern integrated circuits. It is crucial to understand the process of simulating a certain manufacturing process, and how to layout the manufacturing processes such that it is easy to build the circuits with lithography. Simulating a PMOS process is useful to ensure that the process produces working transistors. It is much cheaper to simulate a process than carrying out the process; therefore one should have confidence in the process before attempting it. The simulation software used is ATHENA (based on SUPREM). ATHENA was used to simulate the process in 1D and 2D. IC Station, a Computer Aided Design (CAD) software, was used to layout the PMOS transistors and resistors. Using CAD software helps with ensuring that design rules are followed. Design rules help to ensure that all of the features of the device properly transfer to the wafer and the device properly works within tolerances. Once the devices are designed with IC Station it is possible to pattern to a mask for lithography processes.

2. THEORY

2.1 Computer Aided Design

In order to efficiently layout semiconductor devices CAD software is used to assist with the layout process. Laying out the devices in CAD software makes it easy to transfer the patterns to masks which can be used for lithography. In order to ensure that the layouts work well with the lithography process design rules are put into place. The main restriction that comes into play is minimum feature size and alignment issues between masks. The minimum feature size depends on the lithography technology being used to transfer the image to the wafer. The features of the device must be larger than the minimum feature size in order to ensure that the feature is transferred properly to the wafer. In order to ensure that devices work with some alignment error an alignment tolerance (λ) is defined. The mask must be laid out such that if they are off by a λ in any direction that the device will still function properly.

2.2 Process Simulation

Process simulation software allows one to model the outcome of a certain procedure. Often times the mathematical models for characterizing a process must be solved numerically, which involves several iterations in order to find the correct answer. Computers are very good at repetitive tasks and are much faster than solving the modals by hand. The computer simulation can also be more accurate to the real world situation as it often solves things in small increments and allows for changing values, where in hand calculations things are often held constant in order to simplify the modal.

2.3 Diffusion

One of the main parameters that are being looked at is the diffusion of the dopants and how much of the original dopant leaves the substrate. The diffusion of the dopant changes electrical properties and can make short channel devices not work well or not work at all. It is very difficult to model the dopant leaving the substrate. The modals for diffusion are based off of Fick's Laws of Diffusion. Combining Fick's first law, which states that the flux is equal to the diffusivity of the element times the concentration gradient, $\vec{F} = -D\,\partial N/\partial x$, and his second law which states the amount that the concentration changes with respect to time is equal to the negative of the change in flux with respect to distance, $\partial N/\partial t = -\partial F/\partial x$, results in the differential equation described by Equation 1.

$$\frac{dN}{dt} = D\frac{\partial^2 y}{\partial x} \tag{1}$$

Diffusivity (D) depends on the element being diffused through the diffusion coefficient (D_0) and the activation energy of the element (E_A) and at what temperature (T) the diffusion is taking place. Equation 2 describes the diffusivity. Boltzmann's constant is represented by a lowercase k.

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right) \tag{2}$$

In order to solve the differential equation described by Equation 1, boundary conditions must be defined. In respect to the PMOS process there is a limited source (ion implant). It is assumed that there is a fixed dose, for example, no out diffusion out of the surface, no segregation to the oxide, etc. The drive-in process is for a long time; therefore it is safe to assume that the distribution is a one-sided Gaussian and that all of the original doping is at the surface. While all of the doping doesn't start at all surface with an ion implant, the thermal budget (Dt, product of diffusivity and time) is much larger for the drive-in process than for the ion implant, therefore using this assumption is fine. Solving Equation 1 with the initial descriptions described results in Equations 3 and 4. Equation 3 describes the concentration over distance and time through the surface concentration (N_S), distance (x), and the thermal budget (Dt). Equation 4 relates the surface concentration to the original dose (Q_0) and the thermal budget.

$$N(x,t) = N_s \exp - \frac{x^2}{4Dt} \tag{3}$$

$$N_s = \frac{Q_0}{\sqrt{\pi Dt}} \tag{4}$$

3. RESULTS AND ANALYSIS

For the layout exercise four different devices were laid out. Two of the devices were transistors, one with a length of 20 micrometers and width of 80 micrometers (transistor A) and the other with a length of 90 micrometers and a width of 30 micrometers (transistor B). The other two devices laid out were resistors, one with a goal resistance of 1 kilo ohm and a width of 10 micrometers (resistor A), and the other with a resistance of 10 kilo ohms and a width of 20 micrometers (resistor B). The alignment tolerance (λ) for this layout was 10 micrometers.

The transistor layout consists of four layers. The first layer is the windows for the ion implant. The size of this layer is determined by the alignment tolerance and the width and length of the transistor. The width of the windows will be the width of the transistor plus an error tolerance of two. The second layer in the layout

is the etch widows for where the thin oxide will be grown. The channel is what defines the length and width of the transistor. The third level is the contact cuts for the transistor. The contact cuts are λ in width. They must be at least centered in the diffusion window such that they are at least λ away from all edges of the ion implant window. The last level is the aluminum metal. The aluminum must be at least λ away from other aluminum pathways. The minimum length for the aluminum is 3λ in order to ensure that the contact cuts and aluminum mask will line up within alignment tolerance. Figure one shows the layout for the transistor A with the design rules followed.

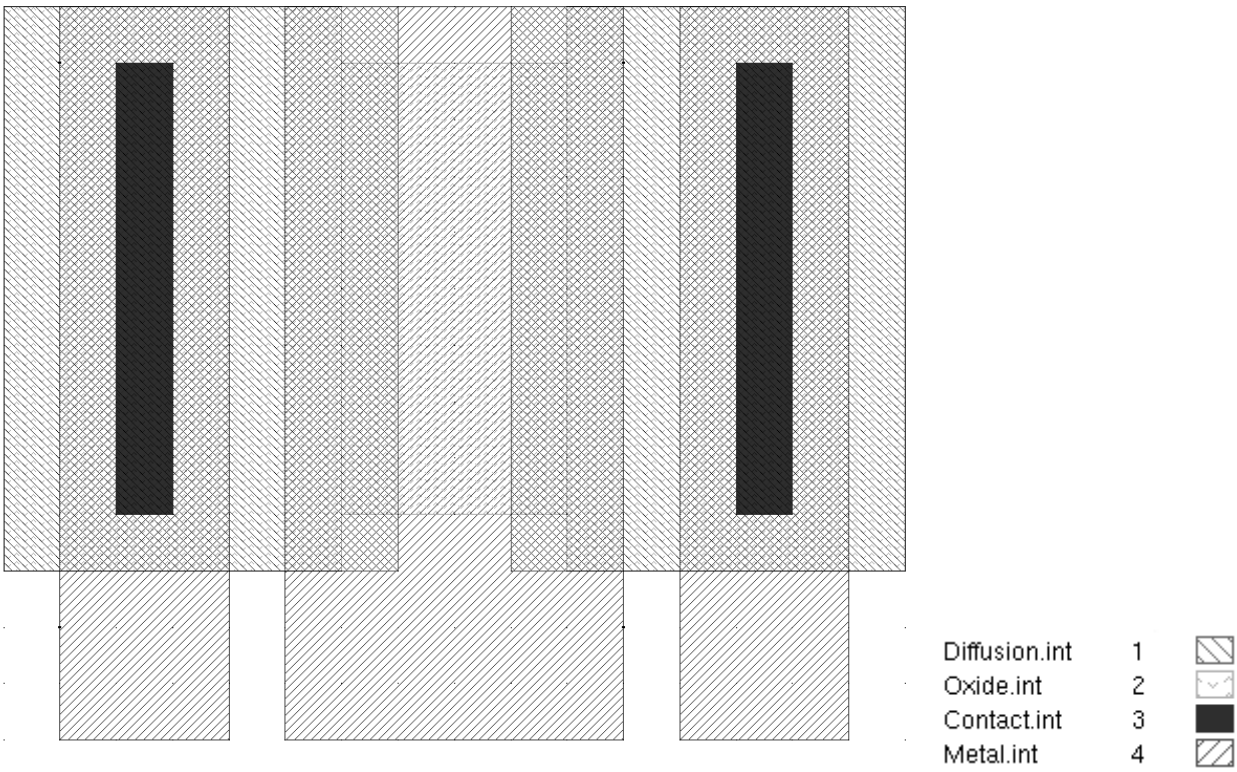

Figure 1. Transistor A layout. Length = 20 μm, Width = 80 μm, λ=10 μm

Figure 2 shows the layout for transistor B with the design rules followed.

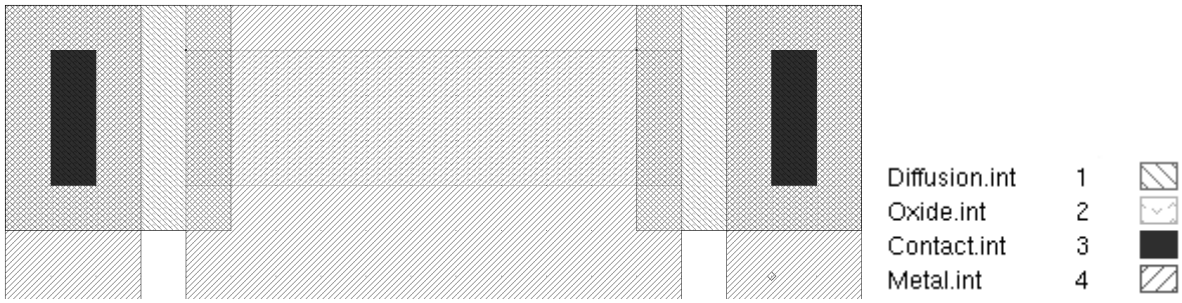

Figure 2. Transistor B layout. Length = 90 μm, Width = 30 μm, λ=10 μm

Designing the resistors is relatively simply compared to the transistors. A sheet resistance of 100 ohm/square was assumed while designing the resistors. This assumption is backed by data measured from the PMOS process and the simulation results of the final sheet resistance. The contact pads on the end of the resistor do contribute some resistance to the resistor, but the resistance added was assumed to be negligible compared to the overall resistance of the resistor. Only 3 lithography layers are required for the resistor. The first layer is

the windows for the ion implant. The second layer is the windows for the contact etch. And the last layer is the aluminum paths needed to have pads connect to the resistor. The third layer is not shown in the layout for simplicity. The aluminum paths would be over the contact pads and contact cuts. In order to construct resistor A with a sheet resistance of 100 ohms/square, 10 squares is needed. Figure 3 shows the layout for the resistor. The contact pads are 3λ by 3λ.

Figure 3. Resistor A layout. Width=10 μm, Length=100 μm, λ=10 μm

With a sheet resistance of 100 Ω/square, 100 squares are needed to form a resistor with a resistance of 10 kΩ. In order to fit the resistor on a small area, it is necessary to serpentine the structure. This will produce corners, which are assumed to be 0.5 squares. Each row of the serpentine is 19 squares long. The last square is a corner, which make for an effective 18.5 squares per row. The horizontal descend is 2 squares long, which is an effective 1.5 squares. This results in 20 squares per row with the vertical descend. In order to get 100 squares, 5 of these row and vertical descends are needed. However only 5 rows are needed, which will result in only 4 vertical descends. In order to make up for the two lost squares there is one extra square before the contact pad on both sides. Figure 4 shows the layout for resistor B.

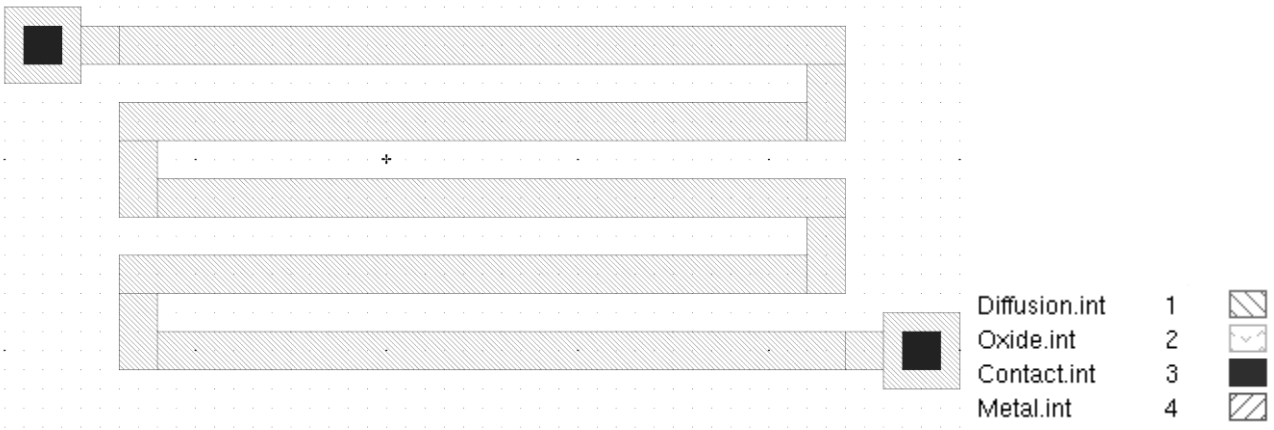

Figure 4. Resistor B layout. Width=20 μm, λ=10 μm

Using ATHENA the process was simulated in 1D and 2D. (The code for both can be seen in the appendix.) The process involves implanting the wafer with boron, diffusing the implanted atoms while growing a thick oxide, etching away the oxide for a thin gate oxide growth, growing the thin gate oxide, making contact cuts, and sputtering on aluminum and removing aluminum where desired. The parameters that are of interest are junction depth, sheet resistance, dopant dose, dopant gradient, sheet resistance, and the oxide thickness after growth. The results of the 1D simulation are shown below in table 1.

Process Step	**R_s (ohm/square)**	**X_j (μm)**	**Dose (cm^{-2})**	**Oxide Growth (Å)**
Post Implant	60.4172	0.688307	1.98452e15	N/A
Post Diffusion	90.4539	1.5928	1.06128e15	4253.27
Post Gate Oxide	100.53	1.72293	9.18747e14	709.931

Table 1. 1D Athena Simulation Results.

The dopant gradient can be seen in the Figures created by TONYPLOT. It is seen that the initial concentration from the ion implant, seen in Figure 5, does not follow a Gaussian distribution. After the diffusion process and gate oxide growth it is seen that the dopant concentration follows a one-sided Gaussian distribution. The final dopant concentration can be seen in Figure 6.

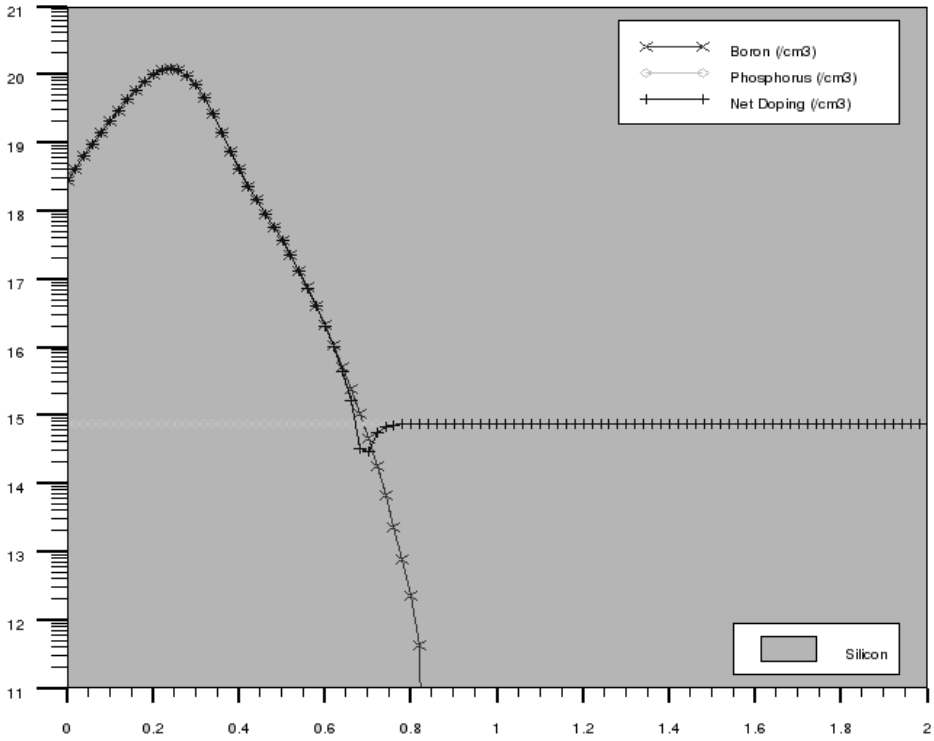

Figure 5. The initial dopant concentration produced by the ion implant.

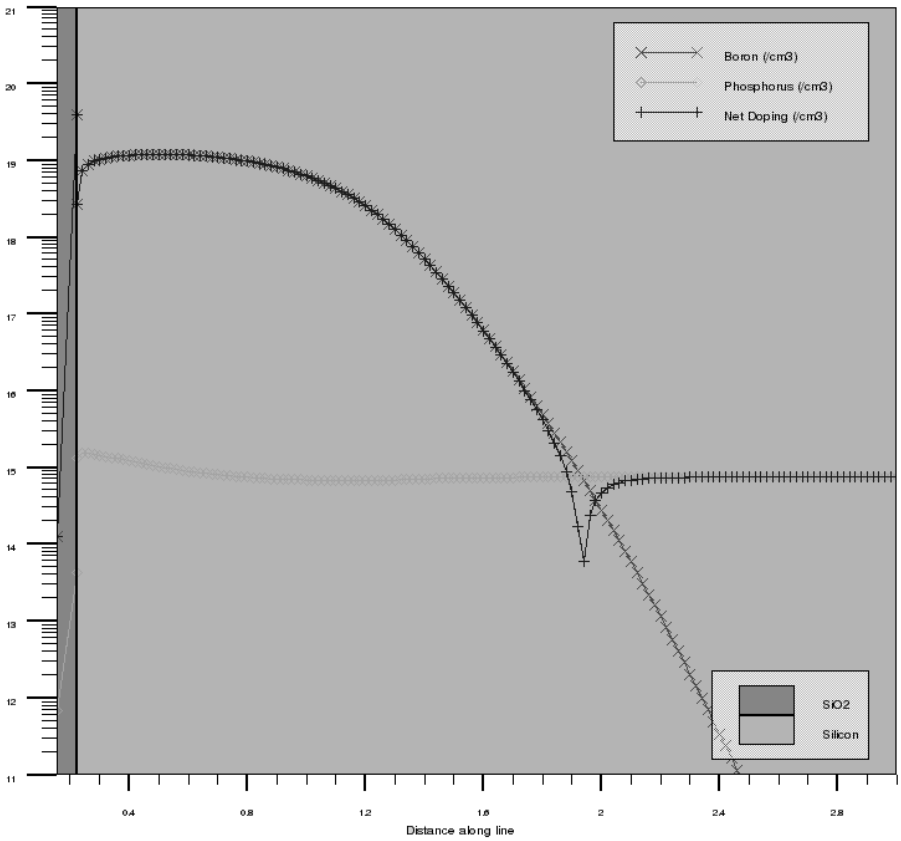

Figure 6. The final dopant concentration from a 1D ATHENA simulation.

The 1D simulation is useful for a quicker simulation time and checking the process steps as well as initial debugging of the code. In order to get a more accurate and side view of the process a 2D simulation is required. The initial dopant concentration from the ion implant shown in Figure 5 looks the same in the 2D simulation. Beyond that, the values and graphs change slightly because of the lateral diffusion that takes place in the more detailed simulation. In order to make the simulation code easier to write, only one half of the transistor were constructed at first. After constructing the first half, the device is mirrored such that the other is present, making the complete transistor. With the wafer cross section it is possible to view a heat map of the net dopant concentration. Figure 7 shows the 2D gradient of the initial ion implant. From this Figure it is seen that the majority of the implant is blocked by the masking oxide. Due to random scattering events some of the implant ends up underneath the oxide near the boundary between the masked and unmasked regions.

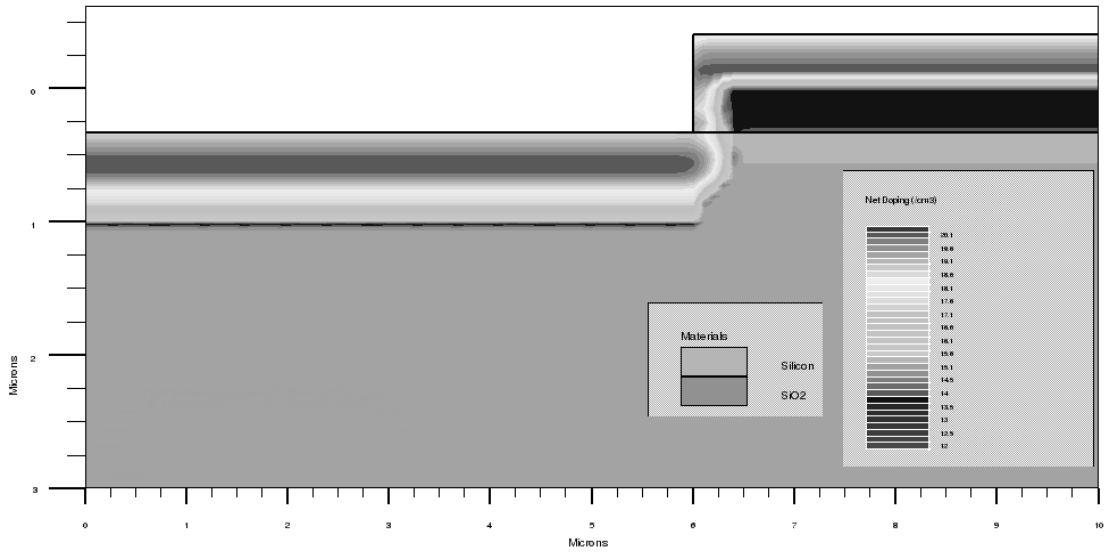

Figure 7. Post ion implant net doping concentration.

After implanting the wafer, a diffusion step takes place. Figure 8 shows the cross section of the wafer after the diffusion step. It is seen that through growing oxide that some of the silicon substrate is consumed. This is one reason why it is difficult to modal the diffusion step. The thick oxide on the right side of the cross section measures to be 8762.79 angstroms. The thinner oxide on the left side of the cross section measures to be 4269.54 angstroms.

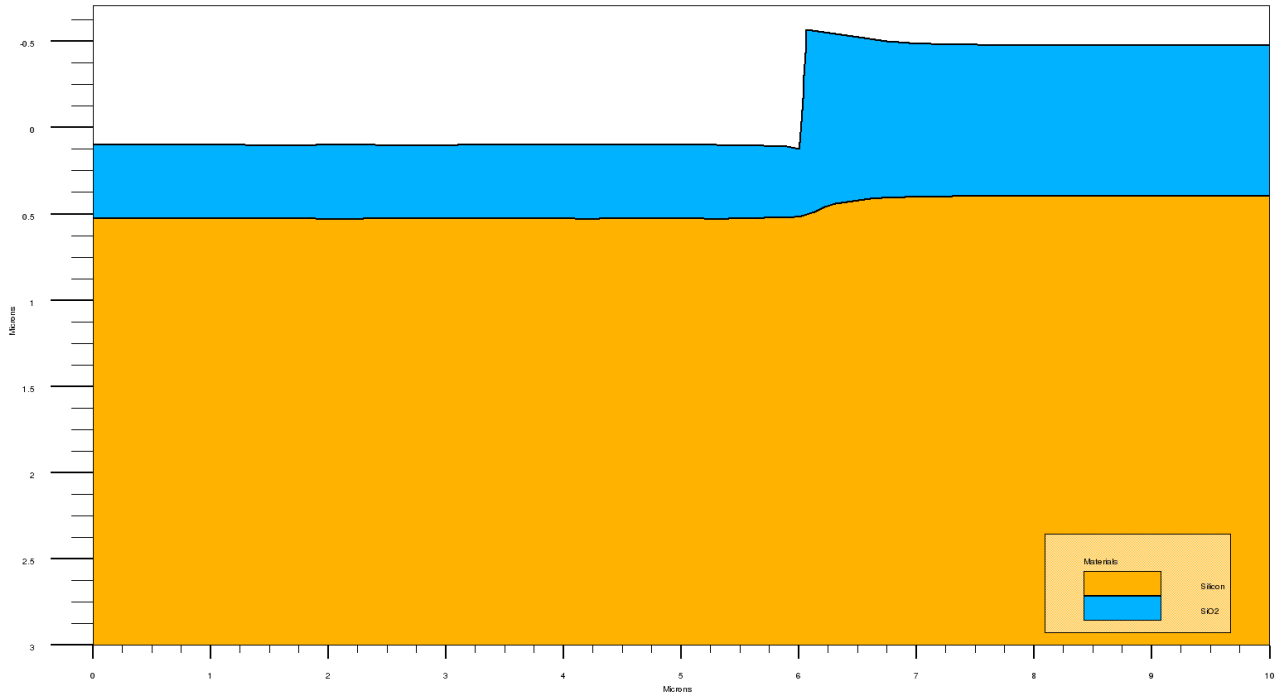

Figure 8. The 2D cross section of the wafer post diffusion.

Figure 9 shows the dopant concentration after the diffusion process. It is seen that the dopant diffused in comparison to Figure 7. It is also seen that the dopant in the masking oxide diffused slightly. It also seen that a considerable amount of the dopant from the wafer diffuses into the oxide.

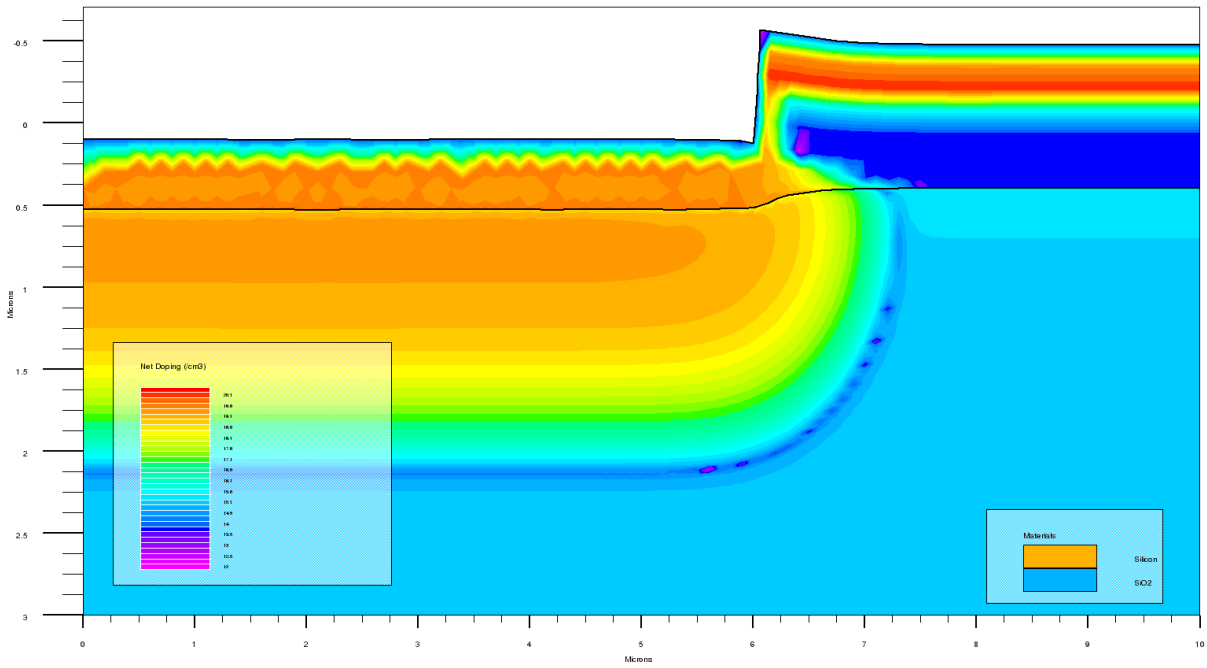

Figure 9. The 2D net dopant concentration after the diffusion step.

With the Tonyplot software that produces the 2D plot in Figure 8, it is possible to take a cut-line and produce a 1D plot at any point. A vertical cut-line is used to produce a graph at 4.6 micrometers. Figure 10 shows the plot that is created. It is seen that the dopant concentration follows a Gaussian curve after the diffusion step.

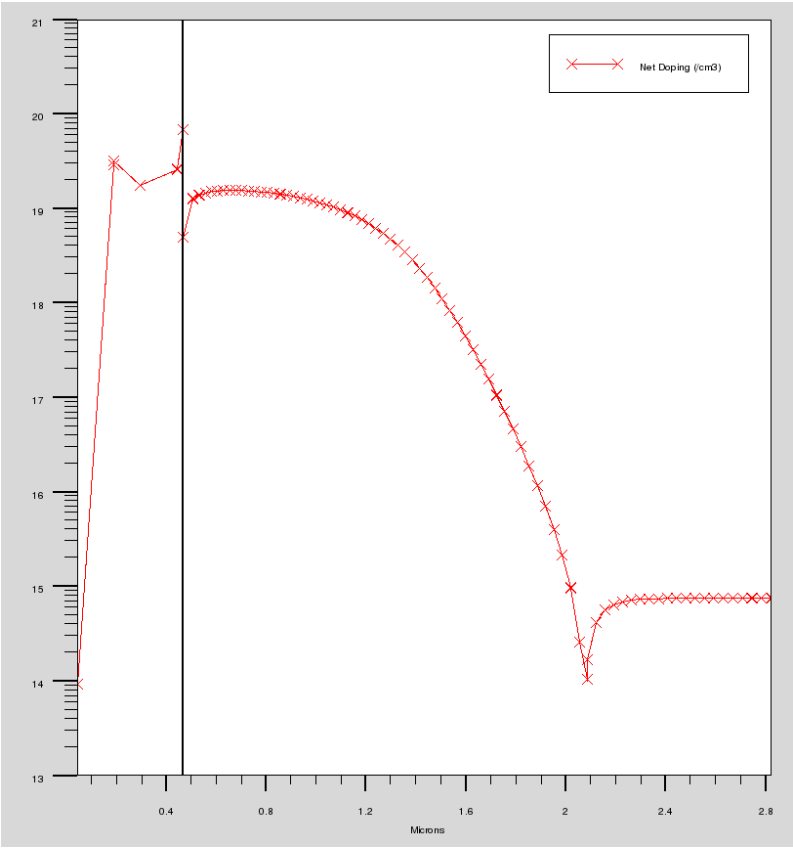

Figure 10. Cut line from the post diffusion/oxide growth. Cutline take at 4.6 µm

After the diffusion step the gate oxide must be grown. In order to grow the gate oxide, an oxide etch must be done to remove the current oxide where the gate oxide will be grown. Figure 11 shows the cross section of the wafer after the desired oxide is etched. It seen that the dopant concentration does not change after an oxide etch.

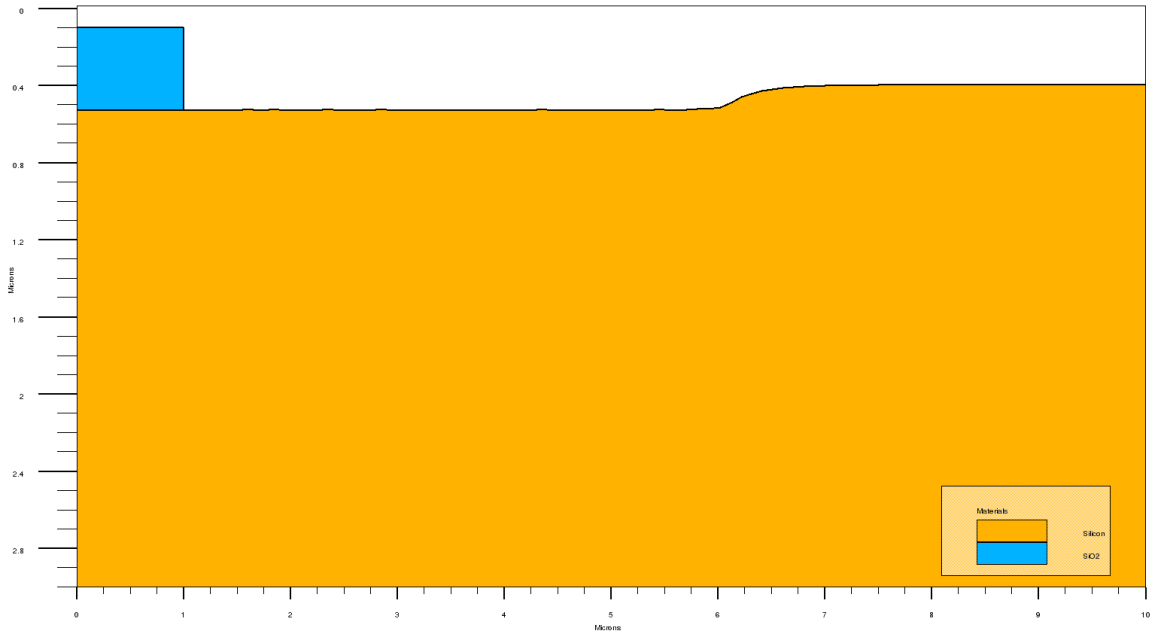

Figure 11. Post diffusion oxide etch, pre gate oxide growth.

The thin gate oxide is grown through a furnace process. The gate oxide is simulated to grow 696 angstroms. The cross section of the wafer after the thin gate oxide growth is shown in Figure 12.

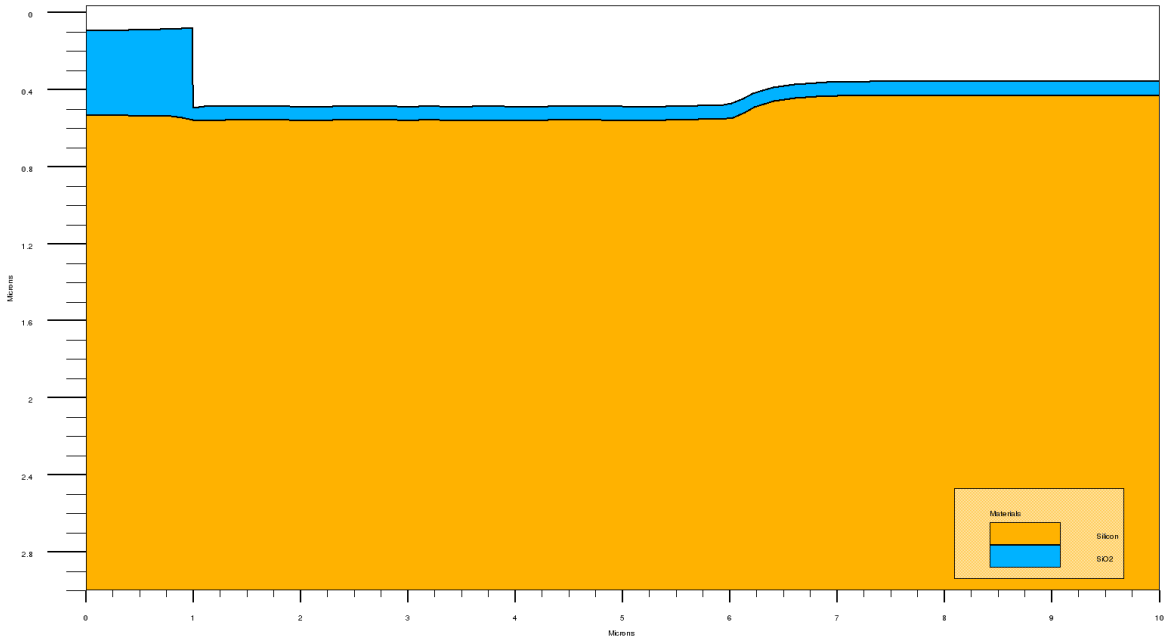

Figure 12. Cross section of the wafer post gate oxide growth.

Because a thermal step was done for the thin gate oxide, some diffusion will occur. This is the final high thermal step done in the simulation process. Therefore there is no more diffusion after the thin gate oxide growth. Figure 13 shows the 2D dopant concentration gradient. It is seen that dopant diffuses in the oxide that is grown.

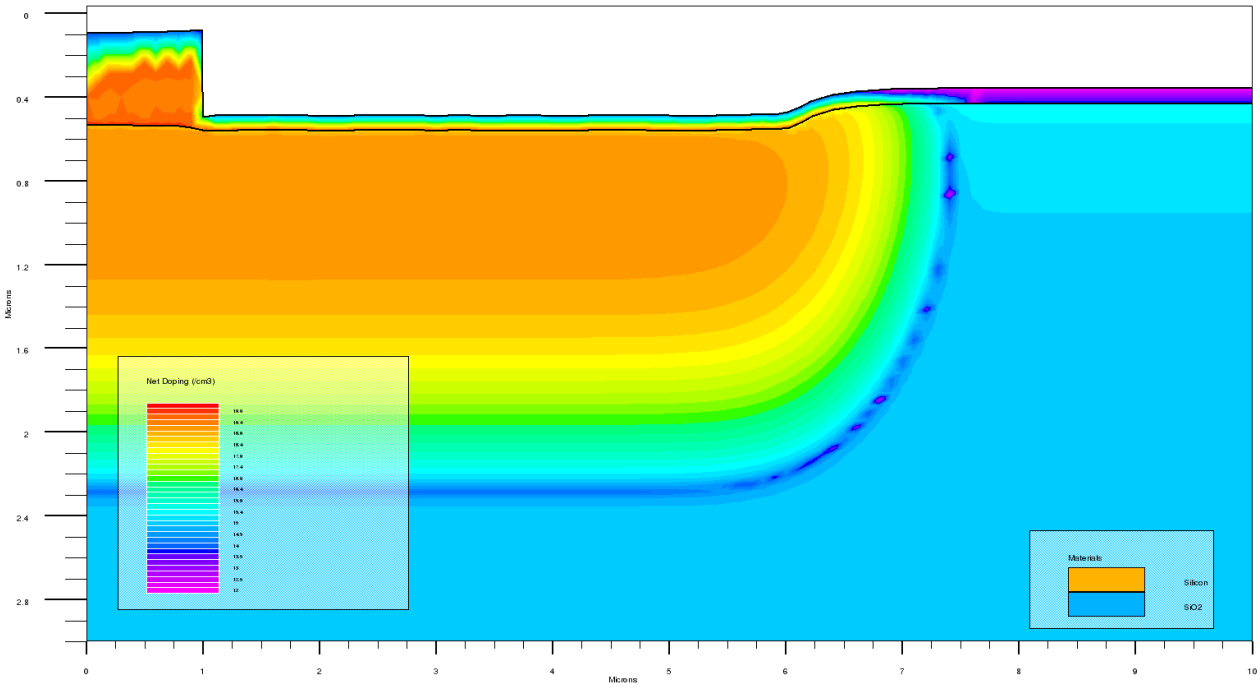

Figure 13. Cross section dopant concentration after gate oxide growth.

Figure 14 shows the net dopant concentration after the gate oxide growth step from a cut-line taken at 4 micrometers.

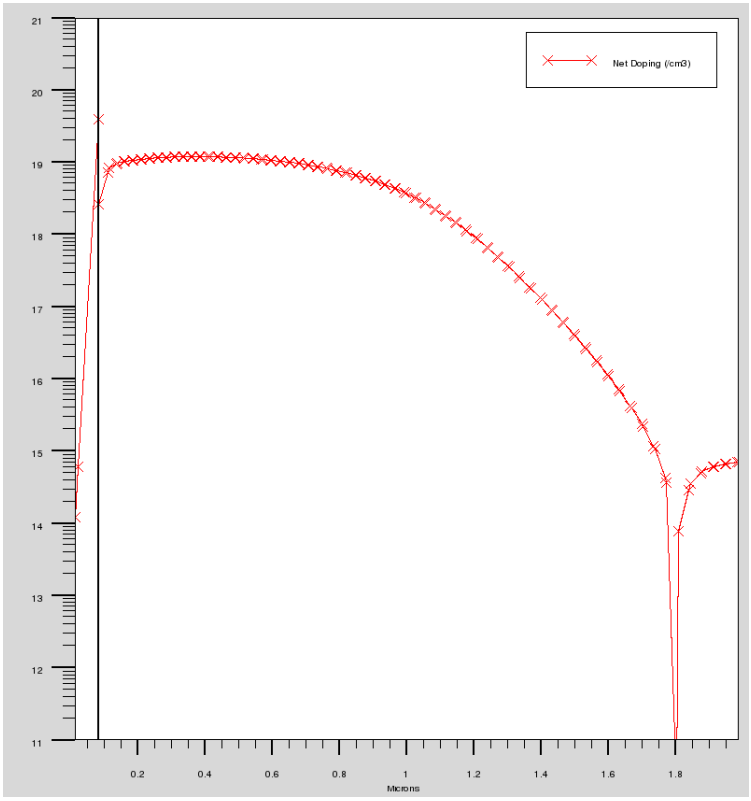

Figure 14. Net dopant concentration after the gate oxide growth. Cutline taken at 4 µm.

After the gate oxide growth the contact cuts are defined. Figure 15 shows the contact cuts etched.

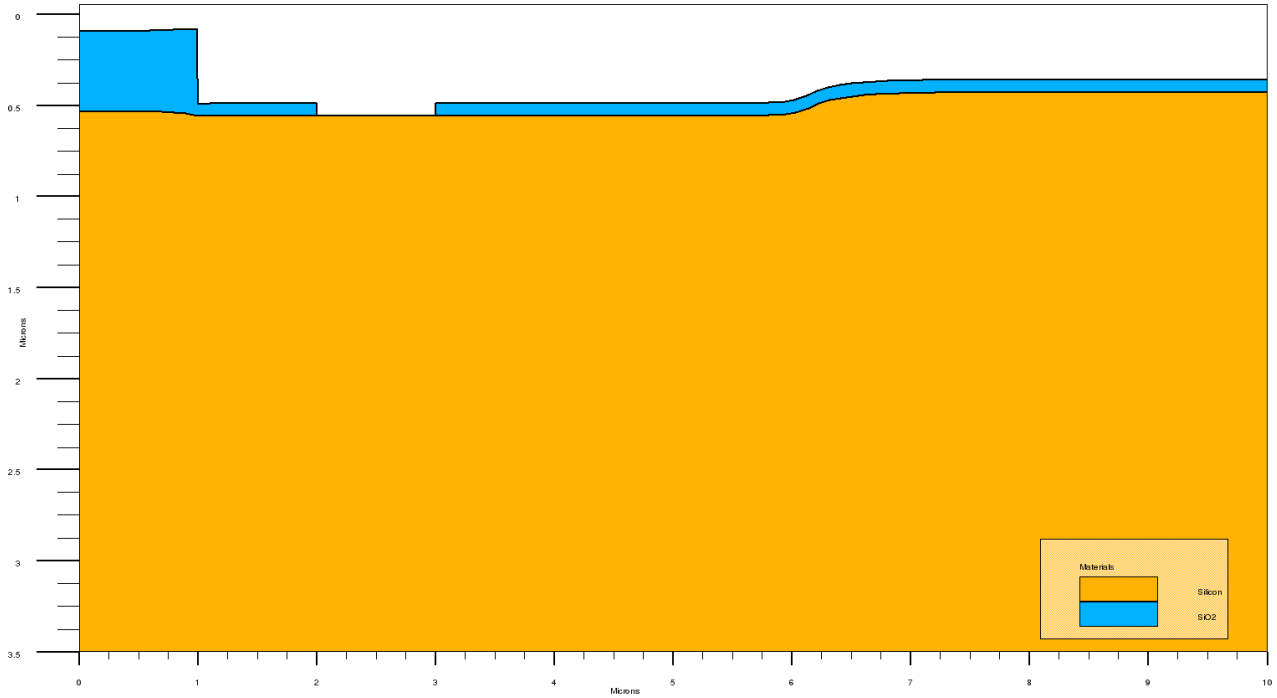

Figure 15. Cross section image of the device after device contact cuts.

After the contact cuts, an aluminum film is deposited onto the wafer. Figure 16 shows the aluminum film on the wafer.

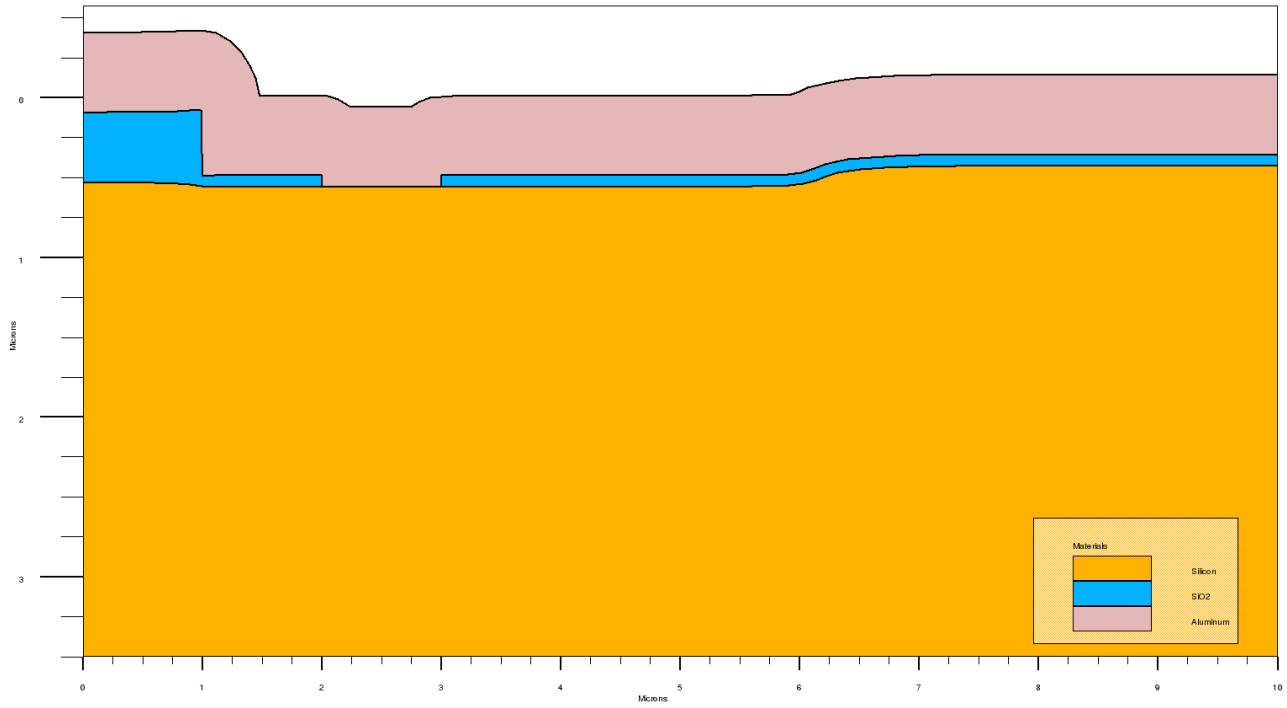

Figure 16. Cross section image of the device after aluminum film is deposited.

After depositing the aluminum film, the path ways are etched into the aluminum. Figure 17 shows the aluminum film after being etched.

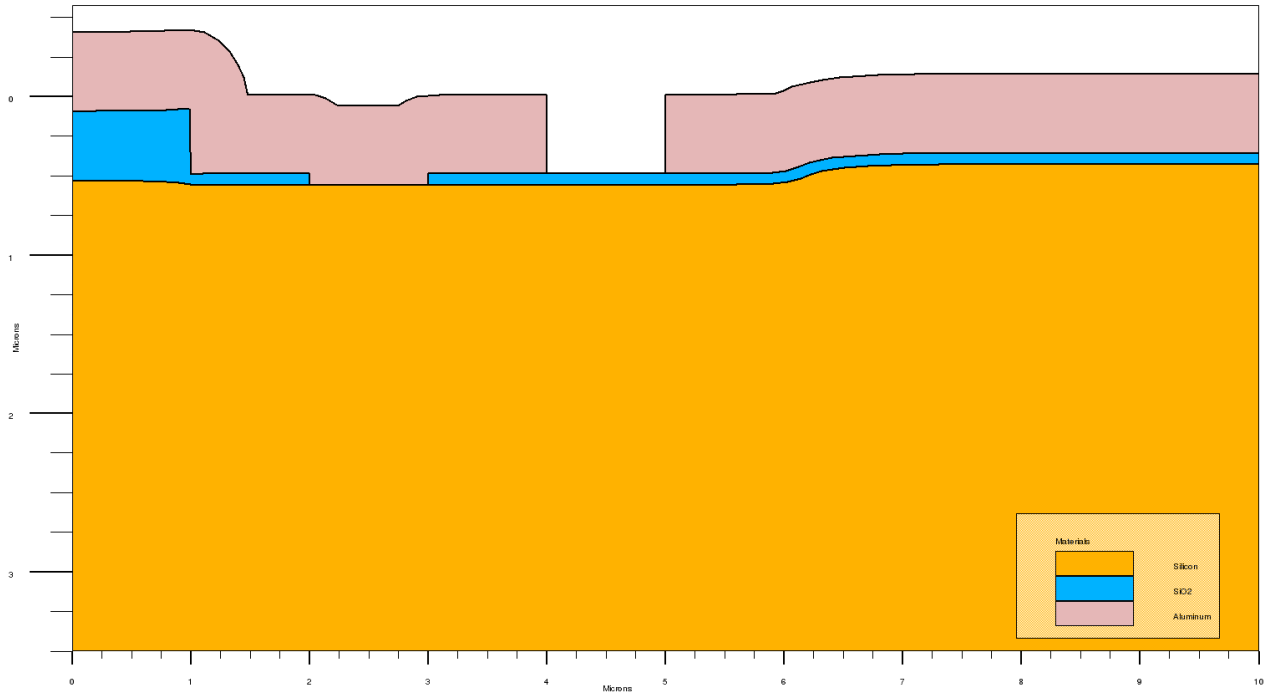

Figure 17. Cross section image of the device after aluminum etch.

In order to build the complete transistor device the simulation is mirrored. Figure 18 shows the device after the mirror step.

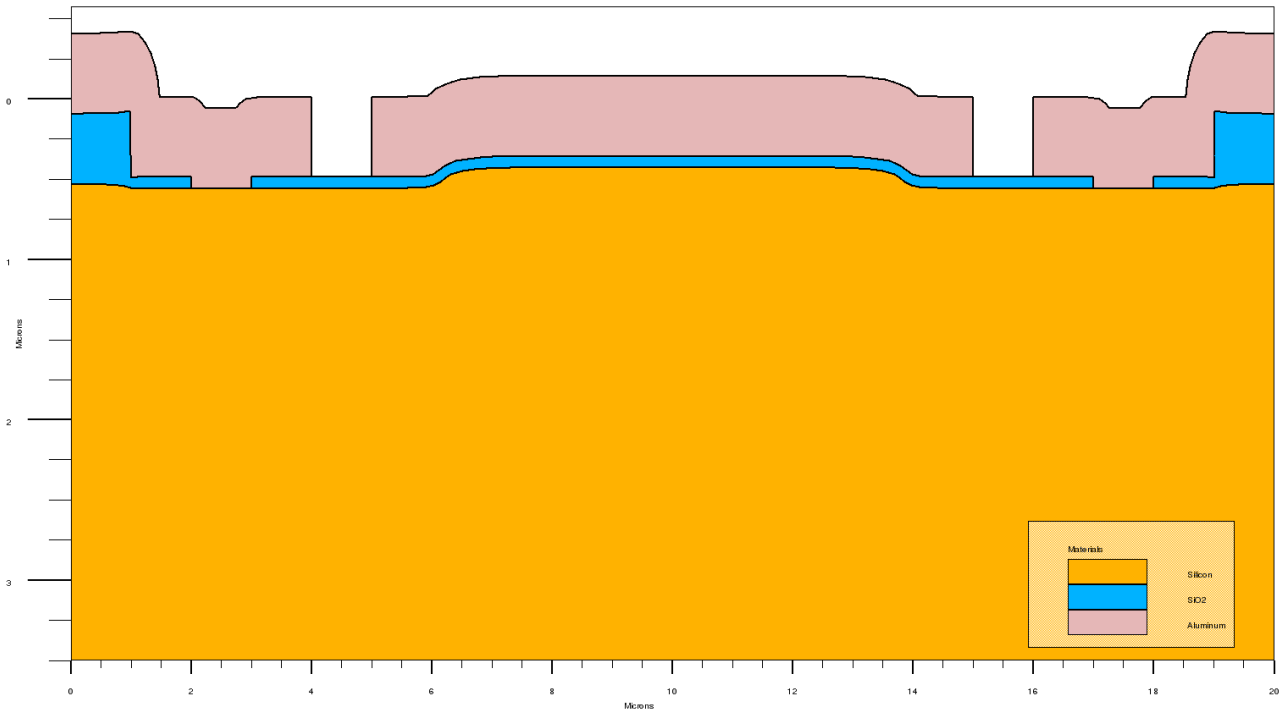

Figure 18. Cross section image of the complete transistor.

The final doping concentration for the whole device is shown in Figure 19. It is seen that there are distinct p-type and n-type regions in the device which ensures correct device operation.

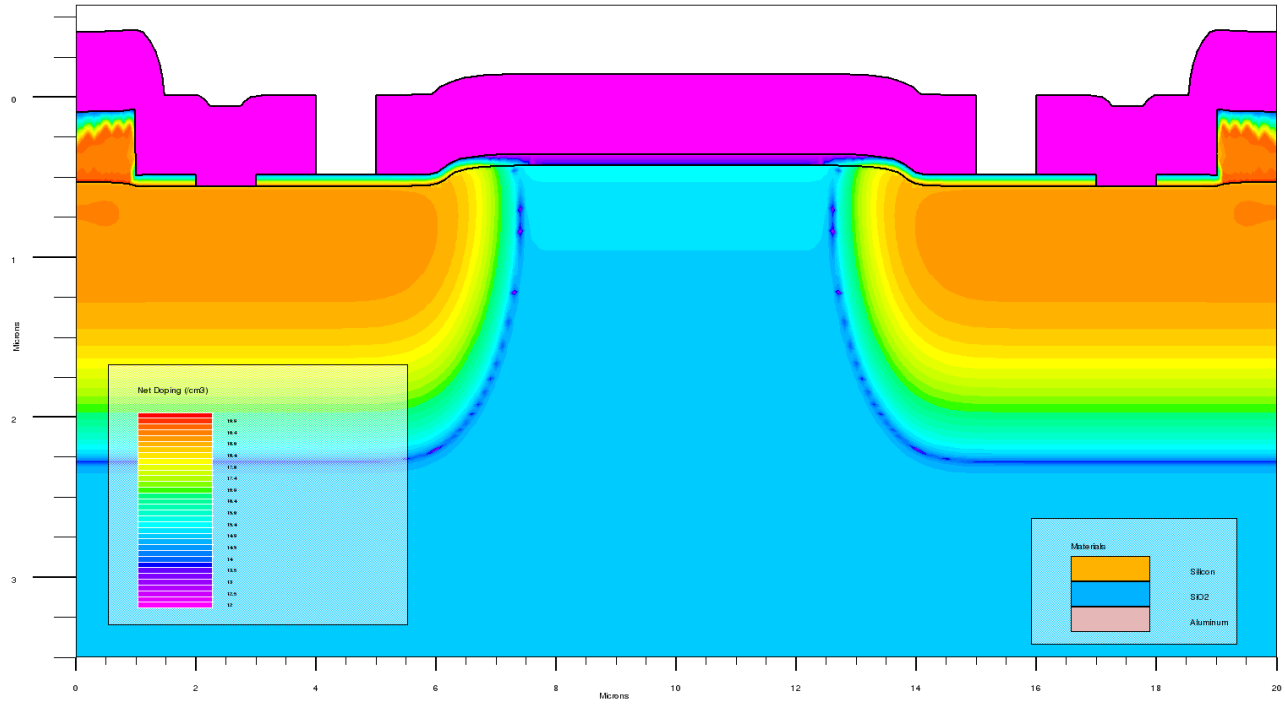

Figure 19. Cross section image of the complete transistor with net doping gradient.

At this point the threshold voltage of the transistor can be extracted. The threshold voltage is extracted to be 1.31072 volts. When characterizing the actual transistors the voltage threshold was found to be 1.34 volts. This is a very close match to measured and simulated threshold voltages.

Throughout the simulation several characteristics are extracted. Table 2 shows the sheet resistance (R_S), junction depth (X_j), the dose, and the oxide growth that resulted from the process. When comparing Table 1 and Table 2 it is seen that values extracted in the 1D and 2D simulations are very similar. The 2D simulations will be closer to the actual process values for it models the real world better.

Process Step	R_s (ohm/square)	X_j (µm)	Dose (cm^{-2})	Oxide Growth (Å)
Post Implant	60.4759	0.688333	1.98483e15	N/A
Post Diffusion	90.1945	1.60461	1.06494e15	4242.46
Post Gate Oxide	99.3558	1.72161	9.30005e14	695.852

Table 2. 2D simulation Results

The lab measurements are shown in table 3. The dose is calculated in a reverse manner based on the measured junction depth (X_j) and the measured sheet resistance (R_S) by using ECE Illinois' IRVIN.net[1] to get the surface concentration. With the surface concentration it is possible to use Equation 5 to find the thermal budget (Dt). With the calculated thermal budget Equation 4 is used to find the dose of the dopant. The ion implant was done at a dose of 2e15 cm^{-3}. A substrate concentration of 7.48e14 cm^{-3} was used for the dose calculations. The initial substrate concentration is based off the initial resistivity of the wafer that was measured to be 5.958 Ω cm. Solecon's resistivity and concentration calculator[2] was used to relate the resistivity and concentration. It should be noted that without a thermal process to electrically activate the dopant from the ion implant that a sheet resistance cannot be measured. In order to measure the sheet resistance after the ion implant a rapid thermal anneal was carried out on the wafer.

Process Step	R_s (ohm/square)	X_j (µm)	N_{sur} (cm^{-3})	Dose (cm^{-2})	Oxide Growth (Å)
Post Implant	52.3241	N/A	N/A	2e15	N/A
Post Diffusion	95.3120	1.67	2.12e19	9.799e14	3863.2
Post Gate Oxide	104.37	2.36	1.46e19	9.714e14	738.78

Table 3. Lab Measurements

By comparing the lab measurements seen in Table 3 with the 2D simulation results seen in Table 2 it seen that the simulation accurately simulates the actual process. The largest discrepancy is seen in the final junction depths. The junction depth was measured in lab through a groove and stain process, which is not an extremely accurate method of measuring the junction depth. The change in the dose between post diffusion and post gate oxide growth for the lab measurement is very small in comparison to the 2D simulation. This is most likely because the dose is a calculation based off of the sheet resistance and junction depth. Another possibility is there was less dopant migrated out of the actual silicon substrate than what was simulated.

It is possible to simulate the process to a greater degree of accuracy by adjusting some of the default parameters that ATHENA uses and by running a fully coupled simulation. Making these adjustments significantly increases simulation time.

[1] http://fabweb.ece.uiuc.edu/utilities/irvin/
[2] http://www.solecon.com/sra/rho2ccal.htm

4. CONCLUSIONS

Devices were designed with IC Station CAD software. CAD software is useful for laying out devices because it makes it simple to transfer the pattern to masks for lithography processes. It also allows for the software to check that the design rules were followed. The design rules that were followed for the layout exercise were to ensure that within a tolerated alignment error that the devices would still operate correctly. The PMOS manufacturing process was simulated with ATHENA. It is useful to simulate manufacturing processes because it allows for seeing what a certain process will produce. A simulation is much cheaper than carrying out the process on a wafer. It was seen that the 2D simulation accurately models the actual PMOS process.

REFERENCES

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[2] S. Wolf, Microchip Manufacturing, Sunset Beach: Lattice Press, 2004.

[3] R. C. Jaeger, Introduction to Microelectronic Fabrication, Upper Saddle River, New Jersey: Prentice Hall, 2002.

APPENDIX

1D ATHENA Simulation Code

```
go athena
#x simulation area
line x loc=0.00 spac=0.10
line x loc=1.00 spac=0.10
#y simulation area.
line y loc=0.00 spac=0.02
line y loc=3.00 spac=0.02
extract name="----NEW 1D SIMULATION--------"
#initalize the wafer!
init silicon phosphor resistivity=6 orientation=100
#do the implant
implant boron dose=2.0e15 energy=75 tilt=7 rotation=45 crystal
tonyplot
#get the junction depth.
extract name="xj1" xj material="Silicon" mat.occno=1 x.val=.5
junc.occno=1
#get the rs1 value
extract name="rs1" p.sheet.res material="Silicon" mat.occno=1 x.val=.5 region.occno=1
#get the dose
extract name="dose" area from curve(depth,impurity="Boron" material="Silicon" mat.occno=1
x.val=.5)/10000
#graph it
```

```
tonyplot
#do the diffusion
diffus time=30 temp=800 t.final=1100 dryo2
diffus time=5 temp=1100 dryo2
diffus time=25 temp=1100 weto2
diffus time=5 temp=1100 nitro
diffus time=45 temp=1100 t.final=800 nitro
extract name="--diffusion--"
#graph it
tonyplot
#get oxide thickness
extract name="Xox" thickness material="SiO~2" mat.occno=1 x.val=.5
#get the junction depth after diffusion
extract name="xj2" xj material="Silicon" mat.occno=1 x.val=.5 junc.occno=1
#get the get the sheet resistance
extract name="rs2" p.sheet.res material="Silicon" mat.occno=1 x.val=.5 region.occno=1
#get the dose!
extract name="dose2" area from curve(depth,impurity="Boron" material="Silicon" mat.occno=1
x.val=.5)/10000

#etch away existing oxide
etch oxide all
#grow the thin oxide (to sim the new xj)
diffus time=20 temp=800 t.final=1000 dryo2
diffus time=93 temp=1000 dryo2
diffus time=5 temp=1000 nitro
diffus time=40 temp=1000 t.final=800 nitro
extract name="--gate oxide grown--"
tonyplot
#get the new oxide thickness
extract name="tox_postgate" thickness material="SiO~2" mat.occno=1 x.val=.5
#get the junction depth
extract name="xj3" xj material="Silicon" mat.occno=1 x.val=.5 junc.occno=1
#get the sheet resistance
extract name="rs3" p.sheet.res material="Silicon" mat.occno=1 x.val=.5 region.occno=1
#get the dose!
extract name="dose3" area from curve(depth,impurity="Boron" material="Silicon" mat.occno=1
x.val=.5)/10000
quit
```

2D ATHENA Simulation Code

```
go athena
#define x
line x loc=0.00 spac=0.10
line x loc=10.00 spac=0.10
#define y
line y loc=0.00 spac=0.02
line y loc=3.50 spac=0.02
extract name="====NEW 2D SIMULATION==="
#initalize the wafer!
init silicon phosphor resistivity=6 orientation=100
#grow the masking oxide
diffus time=67 temp=1100 weto2
#plot it
tonyplot
```

```
#etch it where we want to
etch oxide left p1.x=6.00
#do the implant
implant boron dose=2.0e15 energy=75 tilt=7 rotation=45 crystal
extract name="--Post Implant"
#get the junction depth.
extract name="xj1" xj material="Silicon" mat.occno=1 x.val=3 junc.occno=1
#get the rs1 value
extract name="rs1" p.sheet.res material="Silicon" mat.occno=1 x.val=3 region.occno=1
#get the dose
extract name="dose" area from curve(depth,impurity="Boron" material="Silicon" mat.occno=1
x.val=3)/10000
#graph it
tonyplot
#do the diffusion
diffus time=30 temp=800 t.final=1100 dryo2
diffus time=5 temp=1100 dryo2
diffus time=25 temp=1100 weto2
diffus time=5 temp=1100 nitro
diffus time=45 temp=1100 t.final=800 nitro
extract name="--Post Diffusion"
#graph it
tonyplot
#get oxide thickness
extract name="Xox" thickness material="SiO~2" mat.occno=1 x.val=3
#get the junction depth after diffusion
extract name="xj2" xj material="Silicon" mat.occno=1 x.val=3 junc.occno=1
#get the get the sheet resistance
extract name="rs2" p.sheet.res material="Silicon" mat.occno=1 x.val=3 region.occno=1
#get the dose!
extract name="dose2" area from curve(depth,impurity="Boron" material="Silicon" mat.occno=1
x.val=3)/10000
#oxide etch
etch oxide right p1.x=1.00
#graph it!
tonyplot
#grow thin gate oxide
diffus time=20 temp=800 t.final=1000 dryo2
diffus time=93 temp=1000 dryo2
diffus time=5 temp=1000 nitro
diffus time=40 temp=1000 t.final=800 nitro
extract name="--Post gate oxide"
#plot it!
tonyplot
extract name="mask+gate" thickness material="SiO~2" mat.occno=1 x.val=.5
extract name="gate" thickness material="SiO~2" mat.occno=1 x.val=3
#get the junction depth after diffusion
extract name="xj2" xj material="Silicon" mat.occno=1 x.val=3 junc.occno=1
#get the get the sheet resistance
extract name="rs2" p.sheet.res material="Silicon" mat.occno=1 x.val=3 region.occno=1
extract name="dose3" area from curve(depth,impurity="Boron" material="Silicon" mat.occno=1
x.val=3)/10000
#etch contact
etch oxide start x=2.00 y=0.00
etch cont x=2.00 y=3.00
```

```
etch cont x=3.00 y=3.00
etch done x=3.00 y=0.00
#plot it
tonyplot
#deposit Al
deposit aluminum thick=0.50
#plot it
tonyplot
#etch al
etch aluminum start x=4.00 y=-1.00
etch cont x=4.00 y=1.00
etch cont x=5.00 y=1.00
etch done x=5.00 y=-1.00
#plot it
tonyplot
#mirror to make the other side
struct mirror right
#plot it
tonyplot
#get threshold voltage
extract name="Vt" 1dvt ptype x.val=9.9
quit
```