# Assignment-Module-I

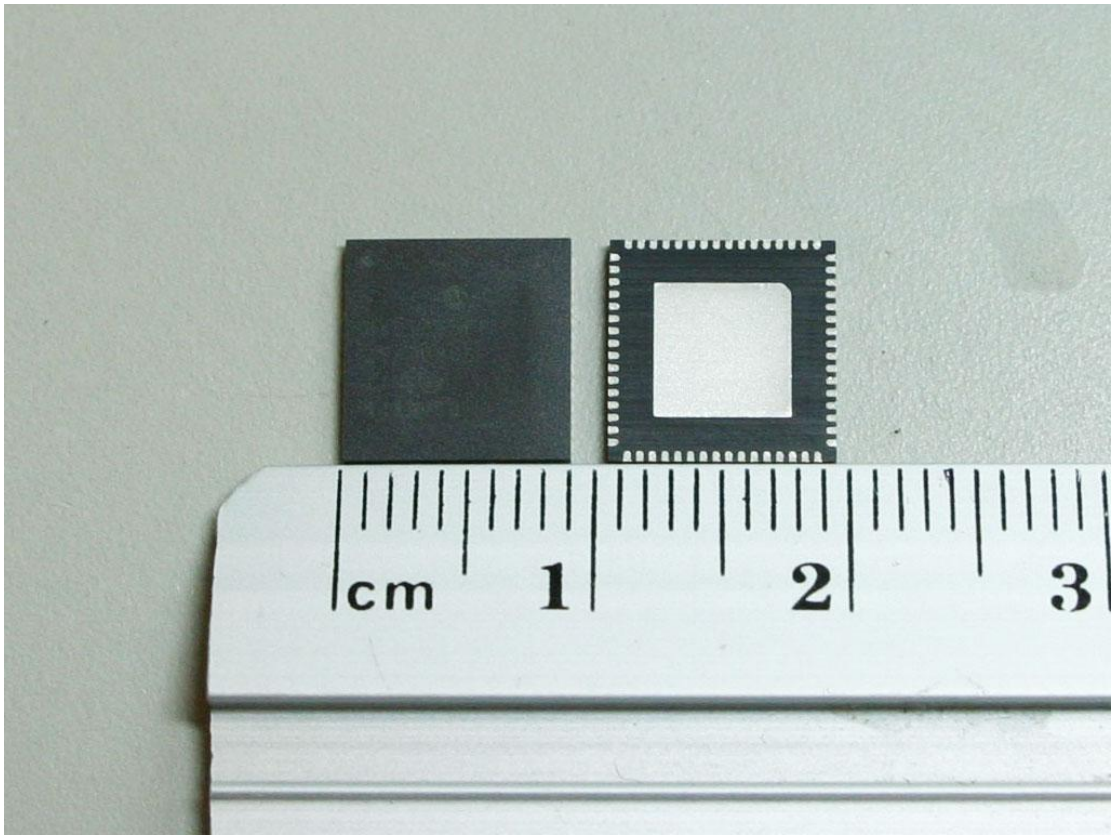
Qu Mingxuan

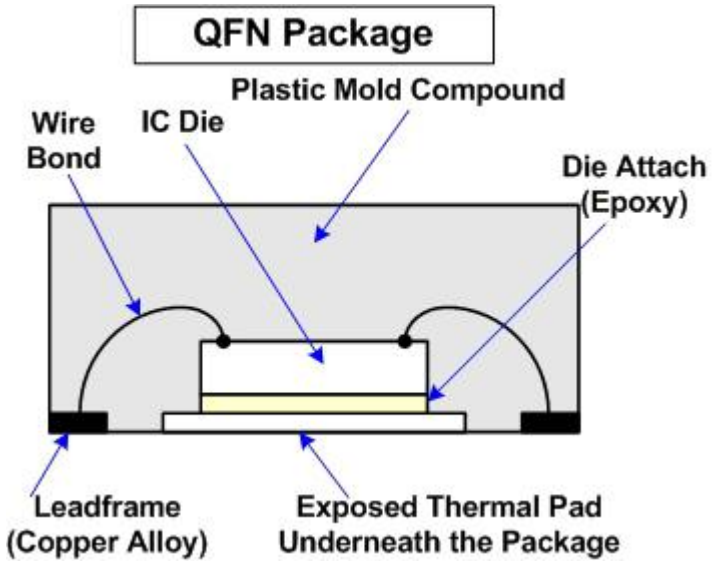
Xiao Sa

Song Yang

# Catalog

# QFN – Quad Flat No-lead



## Thermal implications

Flat no-lead packages include an exposed thermal pad to improve heat transfer out of the IC (into the PCB). Heat transfer can be further facilitated by metal vias in the thermal pad.

The exposed copper die-pad technology offers good thermal and electrical performance.

It also provides excellent thermal performance through exposed leadframe pads with a direct thermal path to dissipate heat from the package. The thermal pad is typically soldered directly to the board, and the thermal vias in the PCB help to dissipate excess power into the copper ground plane to absorb excess heat.

## Effects of vibrations

QFN stress issue should be caused by vibration effect due to leads resonance & mechanical bouncing. Normally worst affected area was at peripheral, but center units could also fail.

Certain clamping condition could cause significant amount of vibrations that affected stability of neighbor leads. The poor stability condition was believed to be one of the major impacting factors that worsen the resonance effect, generating more risks to wire stress issues. The better clamping condition was developed by optimization of clamping hardware design, and clamping force. The optimum clamping condition could reduce the mechanical vibration and hence keeping minimum impact to leads of neighbor units, especially during resonance effect.

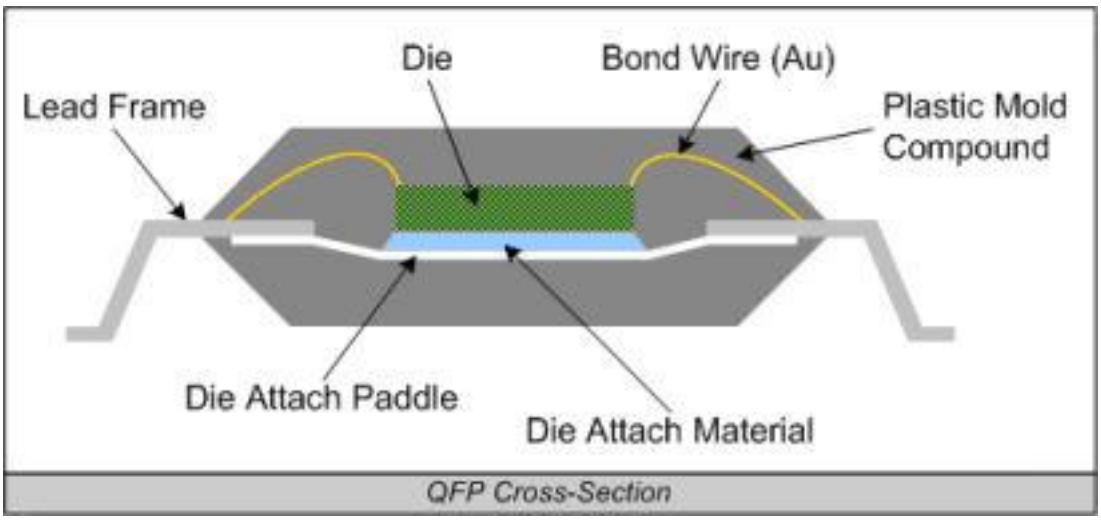
## Package size vs I/Os

Eliminated the external lead laterally protruding out of the package that consume lots of space. So this can make QFN as thin as possible. Because there is no extension lead, so it is hard to damage.

The number of I/Os approaches that of CSP/FBGA packages with the advantages of lower cost for portable and telecommunication applications.

**QFN package have advantages in package size and thermal implications.**

# QFP – Quad Flat Pack




## Thermal implications

QFP uses a buried metal sheet to improve heat dissipation and mostly used in high frequency circuits, but i think the thermal performance is not good at QFN because of the heat dissipation area.

A more challenging thermal issue is the thermal cyclic stress in a QFP component may experience during its operational life. When chips are running hotter, it increases the difference in

temperature between itself and the leads as well as solder material. Leads or solder joint fracture or fatigue failure always occur even through multiple electronic package designs kept trying to fix it . As package size shrinks, the heat generated in die is increasing the mismatch in the coefficients of thermal expansion (CTE) between the leads and solder material since the distance is closer between chip and leads which reduced the heat transfer process. The optimization for the package design with fine pitch leads is expected.

## Effects of vibrations

Due to the random vibration load conditions, the QFP device solder joints are subjected to alternating stress, resulting in solder joint failure.

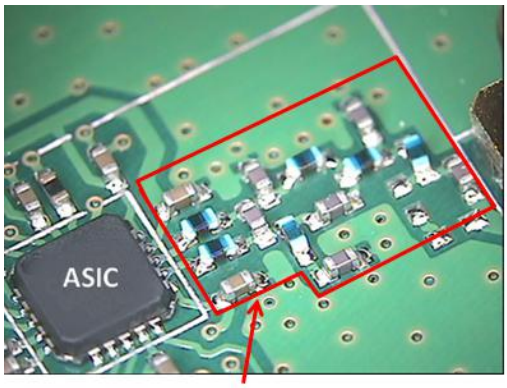
## Package size vs I/Os

The ratio between chip area and package area is small.

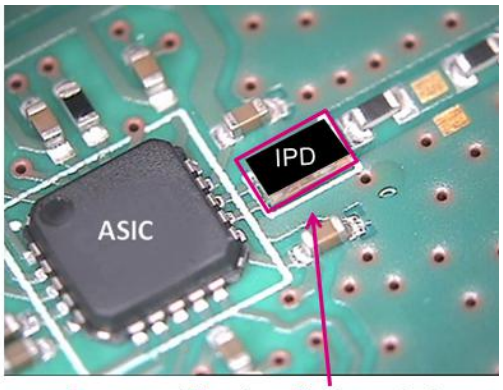
The technology realizes that the distance between the pins of the CPU chip is small, the pins are very thin, and the large-scale or very large-scale integrated circuits generally adopt this package form, and the number of pins thereof is generally above 100.

**QFP package have advantages in package size vs I/Os.**

# IPD – Integrated Passive Device




Discrete SMD Solution




Integrated Passives Device Solution

## Thermal implications

IPDs are generally fabricated using standard wafer fabrication technologies such as thin film and photolithography processing. IPDs can be designed as flip chip mountable or wire bondable components and the substrates for IPDs usually are thin film substrates like silicon, alumina or glass. Every passive components are separation and have enough space between each other to reduce the heating effects.

## Effects of vibrations

All passive components are soldered separately on the pads, so they reduce the vibrate effects.

## Package size vs I/Os

In my opinion, the package size is depend on the quality of passive components. It can reduce the I/O lead. The same I/O function of different component can be combine to one lead. The less I/O means it can be easy connect with the PCB and easy to fix.

**IPD package have advantages in thermal implement and package I/Os.**

# SIP – System in Package


## Thermal implications

Systems-in-package are like systems-on-chip (SoC) but less tightly integrated and not on a single semiconductor die. So it pulls down the distance between devices without reducing the functionality to better reduce the thermal impact.

## Package size vs I/Os and Effects of vibrations

SIP is a number of integrated circuits enclosed in a single chip carrier package. Dies containing integrated circuits may be stacked vertically on a substrate. They are internally connected by fine wires that are bonded to the package. Alternatively, with a flip chip technology, solder bumps are used to join stacked chips together. The volume is reduced, the protection property of the chip is improved, and the number of leads is reduced.

**SIP have advantages in package size and thermal implications.**

# SIB – System in Board

## Thermal implications

Because the size of the SIB is usually relatively large, the heat dissipation effect is better.

## Effects of vibrations

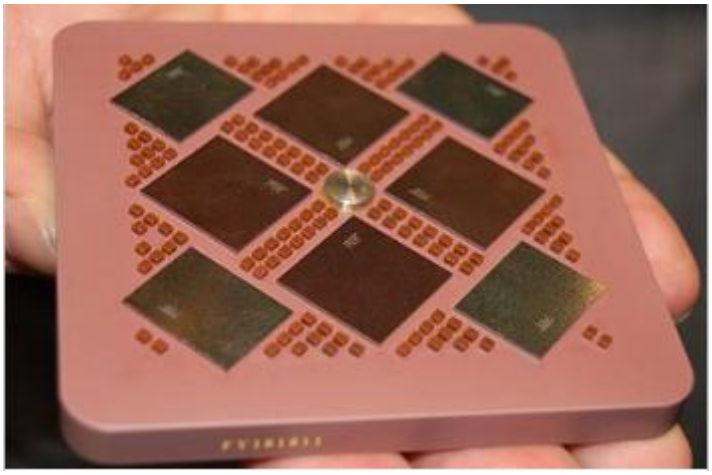
Since the SIB has many separate discrete components which are affected by vibration. Therefore the vibrate reliability is reduced.

## Package size vs I/Os

Due to the limitations of the chip, the size of the module and the power consumption, the PCB size and power consumption cannot be reduced without limit. Large package and traces cause large losses and parasitic parameters, which limits the system performance.

**SIB have advantages in thermal implications.**

# MCM – Multi Chip Module



A multi-chip module (MCM) is an electronic package consisting of multiple integrated circuits (ICs) assembled into a single device. An MCM works as a single component and is capable of handling an entire function. The various components of a MCM are mounted on a substrate, and the bare dies of the substrate are connected to the surface via wire bonding, tape bonding or flip-chip bonding. The module can be encapsulated by a plastic molding and is mounted on the printed circuit board. MCMs offer better performance and can reduce the size of a device considerably.

## Thermal implications

- Poor thermal conductivity of substrate
- Power dissipation heat
- No package to Single package has to be able to remove heat generated by all the ICs.

For some applications, the thermal properties are important. The first way to improve the thermal properties is to choose a substrate with a good thermal conductivity, like certain ceramic materials (beryllium oxide or silicon nitride), silicon or metal based substrates. If the substrate itself is not able to cope with the power, alternative heat paths have to be found. This can be to attach the chips to some type of heat sinks, and use natural or forced convection priciples to bring the die-temperature to the specified level.

## Effects of vibrations

Because of its high level of integration, it is easy to perform centralized shielding and protection, so it is more reliable than using discrete devices. Improved reliability by decreasing the number of interconnects between “components” and boards.

## Package size vs I/Os

An MCM offers a packaging efficiency of more than 30%. This packaging technology has Smaller overall packages; enables greater miniaturization, lower cost, lower power supply needed because of shorter interconnect lengths, and Simplify of complexity by putting several devices into a single package.

In most cases, modules with TAB are considered MCMs. Handling the tape carrier package (TCP) requires special care, the outer lead pitch is typically 10mil or less and requires a higher density interconnect substrate than traditional boards.

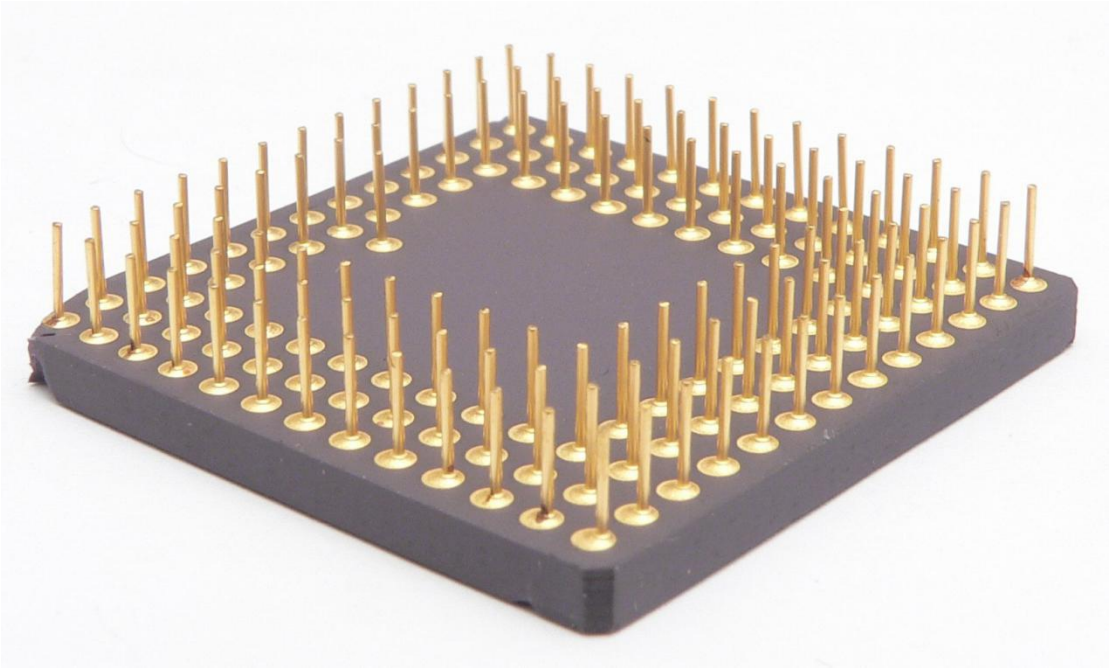
approach of single chip packages on circuit boards:

- Smaller size and less weight
- Higher performance
- Lower cost

One or more of these reasons plays a role in every application of MCM in production today.

**MCM have advantages in package size & thermal implications**

# PGA - Pin grid array



A pin grid array, often abbreviated PGA, is a type of integrated circuit packaging. In a PGA, the package is square or rectangular, and the pins are arranged in a regular array on the underside of the package.

## Thermal implications

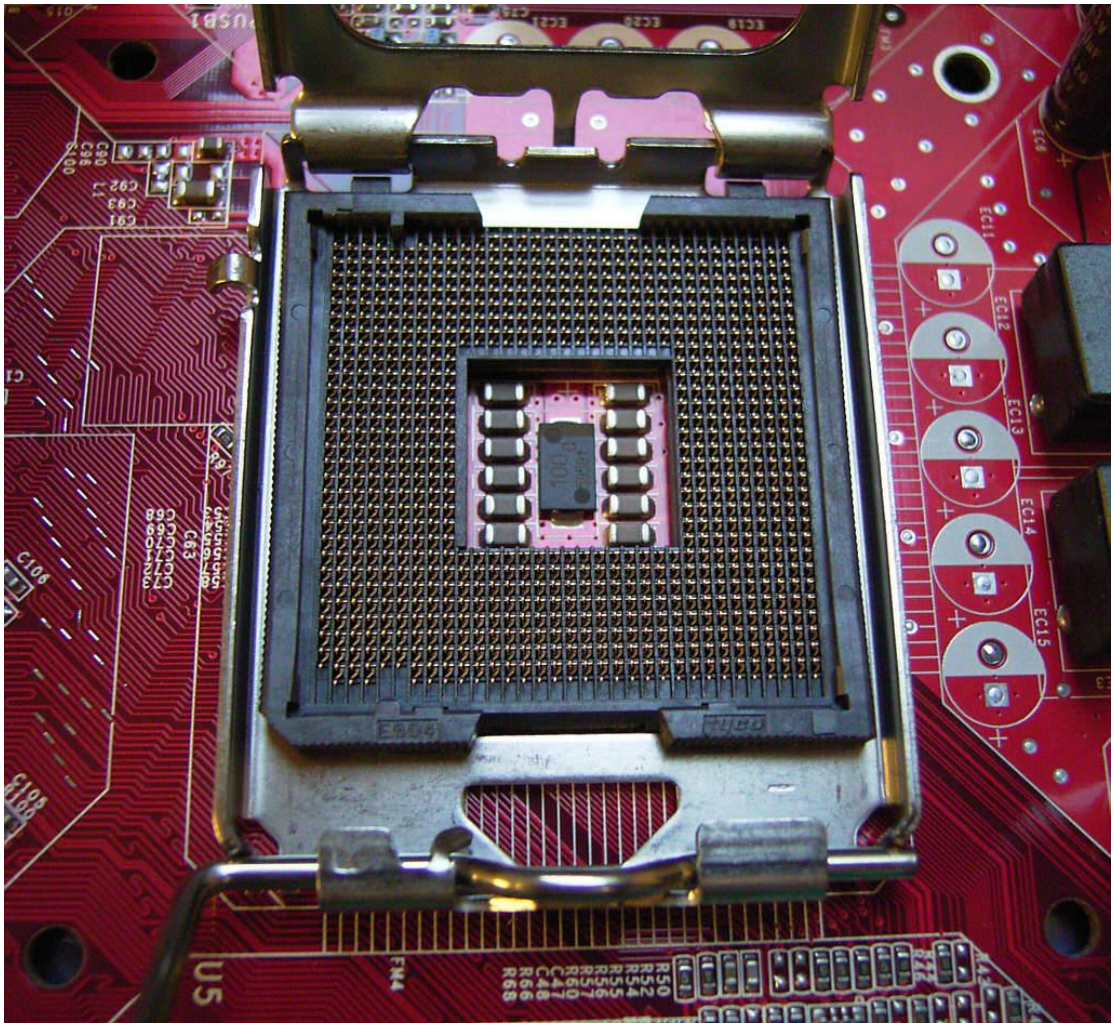
As the PGA gets bigger and dissipates more heat, the heat sink becomes larger and the heat sink is often combined or connected to the PGA.

## Effects of vibrations and Package size vs I/Os

The PGA concentrates the pins on the PCB of the CPU, so a bunch of pins can be seen on the CPU, and the motherboard only needs to provide a jack for inserting pins. And because it requires multiple movements, the PGA's stitches are relatively stronger, and even if they are bent, they can be recovered in a relatively simple way.

**PGA have advantages in package size vs I/Os**

# LGA - Land grid array



The land grid array (LGA) is a type of surface-mount packaging for integrated circuits (ICs) that is notable for having the pins on the socket (when a socket is used) rather than the integrated circuit.[1] An LGA can be electrically connected to a printed circuit board (PCB) either by the use of a socket or by soldering directly to the board.

## Thermal implications

There may not be enough room between an LGA package and the circuit board to accommodate a chip clip-on heat sink due to the lower stand-off height of LGA.

## Effects of vibrations

During the development of the loading mechanisms for LGA packages and sockets, socket pin contact to LGA pad under retention load, solder joint reliability under shock load, socket pin

fretting under vibration, and load degradation are some of the key structural risks.

### Package size vs I/Os

LGA can accommodate more I/O pins in a smaller package. Compared to PGA CPUs, LGA reduces the likelihood of the chip being damaged either before or during installation as there are no pins that can be accidentally bent.

**LGA have advantages in thermal implication.**

# DIP – Dual Inline Package

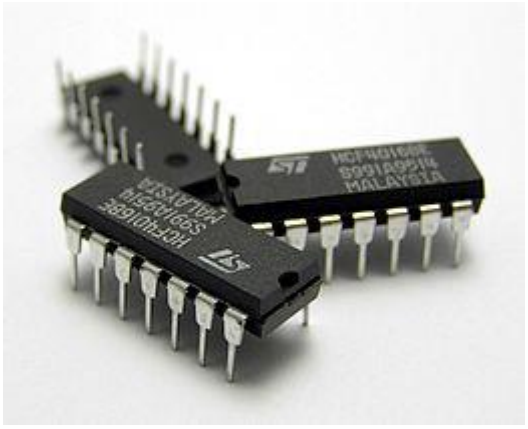


Fig.4000-series logic ICs in 0.3" wide 14-pin plastic DIP packages (DIP-14N), also known as PDIP (Plastic DIP)

Fig.0.3" wide DIP sockets with dual-wipe contacts for 16-, 14-, and 8-pin DIP ICs

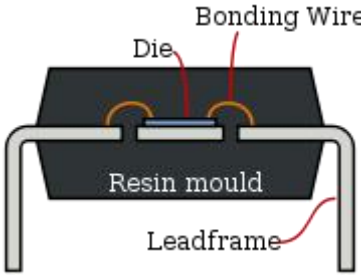



Fig.Side view of a dual in-line package (DIP) IC

## Thermal implications

the leadframe material and molding compound most dramatically impact \thetaJAwhile the leadframe design plays a secondary role. Other factors are of minor importance. The user's external cooling conditions are very important to properly utilizing a package's thermal capabilities. By optimizing material selection in a standard 16 pin plastic DIP while using natural convection cooling, its thermal performance can he potentially increased by a factor of three. A factor of seven improvement is possible when using both optimum cooling conditions and superior packaging materials.

DIP cooling conditions are often employed: 1) natural convection cooling, 2) artificially circulated air, and 3) cooling under a liquid or on a water cooled copper block. Natural convection is preferred by the user from cost, design, and space considerations but is quite ineffective since, for a package with superior thermal properties, the rate limiting step becomes removing heat from the case to the ambient. Artificially blown air is both more effective and more costly. The ideal liquid cooling is employed only in very high performance cases, but does utilize the package’s ultimate thermal capability.

heat dissipation capabilities of DIP, when forced convection is applied, are not influenced by mounting them on a PCB.

## Effects of vibrations

The equivalent stress tends to become larger and smaller as the height of the pin increases. The equivalent stress tends to decrease with the increase of the pin diameter. Reasonable selection of pin height and pin diameter is beneficial to reduce the maximum equivalent stress of DIP devices.

## Package size vs I/Os

DIP is suitable for perforated mounting of PCB. The volume of the DIP always be large. With the

requirements of market, the size of the package tends to be smaller and higher pin count. Here is a trends of the package.

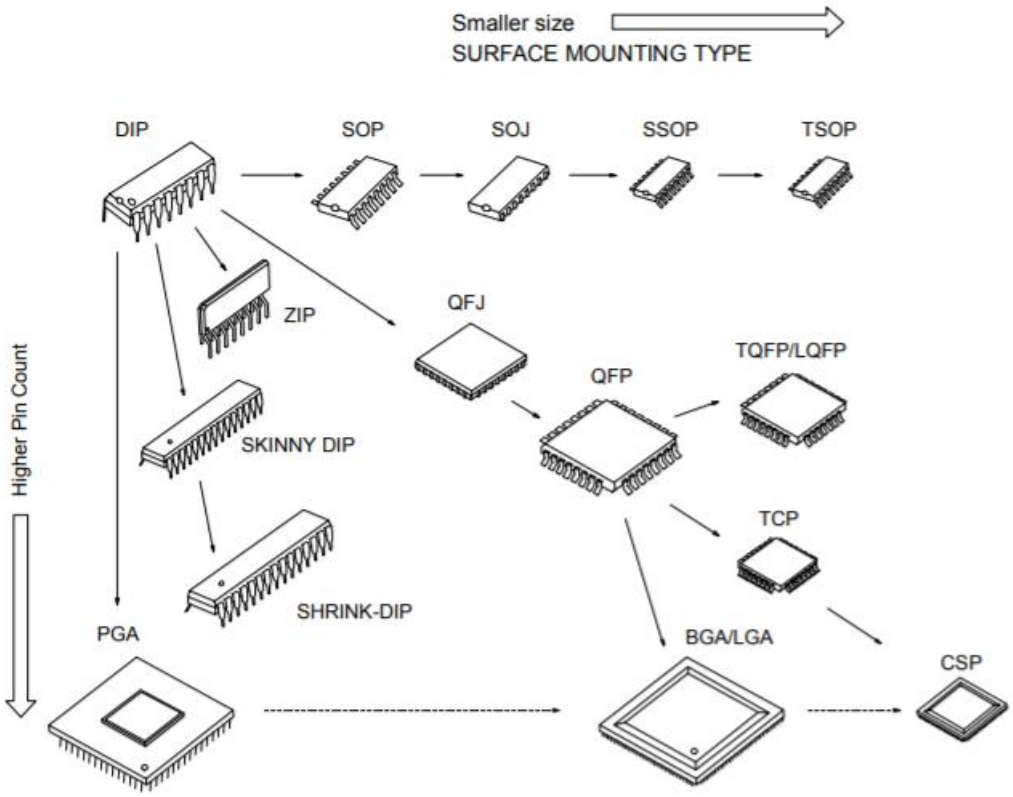



Fig.Packaging Trend

Ultra-miniature packages and with multi-pin I/O will be more popular in the future.

**DIP have advantage in thermal implication.**

# SOIC – Small Outline Integrated Circuit


Fig.SOIC-16

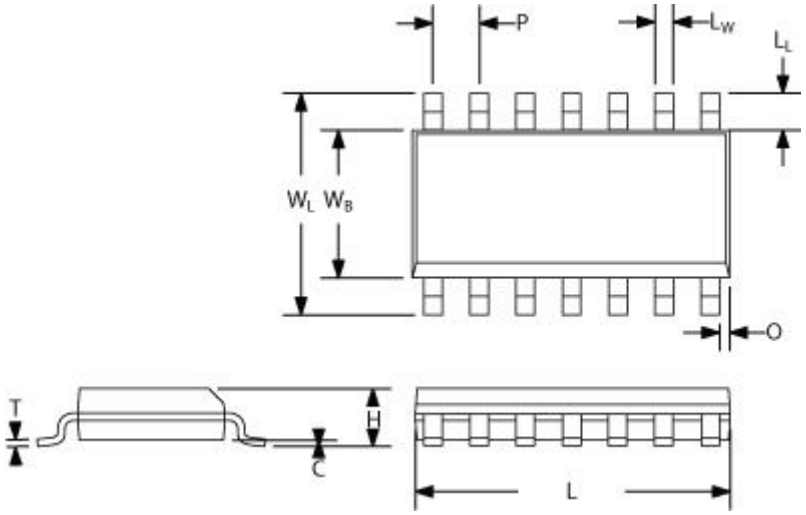



Fig.general shape of a SOIC narrow package

## Thermal implications

Comparing with the DIP, the size of SOIC is more small and the thermal conductivity is better.

## Effects of vibrations

SOIC has excellent performance and high reliability. It reduces the connection between various functional components, minimizes various losses and interferences between the connections. SOIC has gull wing lead, and the pin is exposed to the air. Comparing to the Mounting component,

the SOIC is more easy to get damage.

### Package size vs I/Os

SOIC is one of the surface mount integrated circuit packages that reduces space by approximately 30-50% compared to equivalent DIP packages and reduces thickness by approximately 70%. The SOIC package is shorter and narrower than the DIP package. For example, for the SOIC-14, the pin pitch on both sides is approximately 6 mm and the package width is 3.9 mm. These dimensions will vary slightly depending on the SOIC package. There are airfoil pins on both sides of the package and the two pins are spaced 1.27mm apart.

**SOIC package have advantages in effects of vibrations and package size.**

## Ball Grid Array

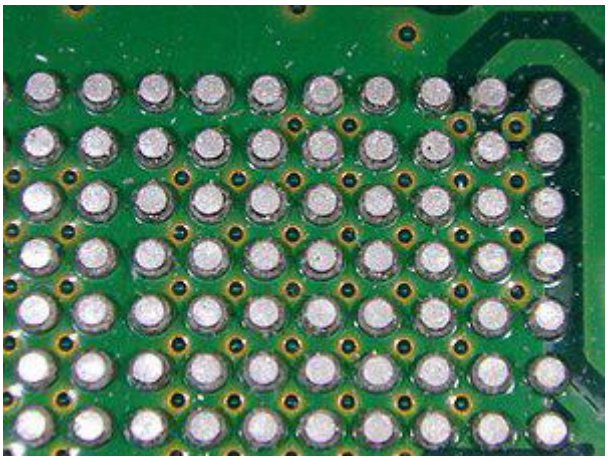


Fig.A grid array of solder balls under an integrated circuit chip, with the chip removed; the balls were left attached to the printed circuit board.

### Thermal implications

The array of spherical contacts facilitates heat dissipation. The contact surface with the substrate is large and short, which is conducive to heat dissipation

### Effects of vibrations

The BGA pin is rugged and does not have pin deformation problems like QFP. As expected from solder leads, the high stiffness of the connection makes the geometric stretch (Eq. 10) the main contributor to the fatigue damage.

### Package size vs I/Os

Although the number of I/O pins increases, the distance between the pins is much larger than that of the QFP package, and it improves the yield.

However, it occupies a large area of the substrate.

**BGA package have advantages in thermal implication and effects of vibrations.**

## Low Temperature Co-fired Ceramic

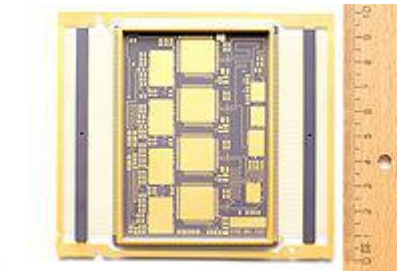


Fig.Low Temperature Co-fired Ceramic

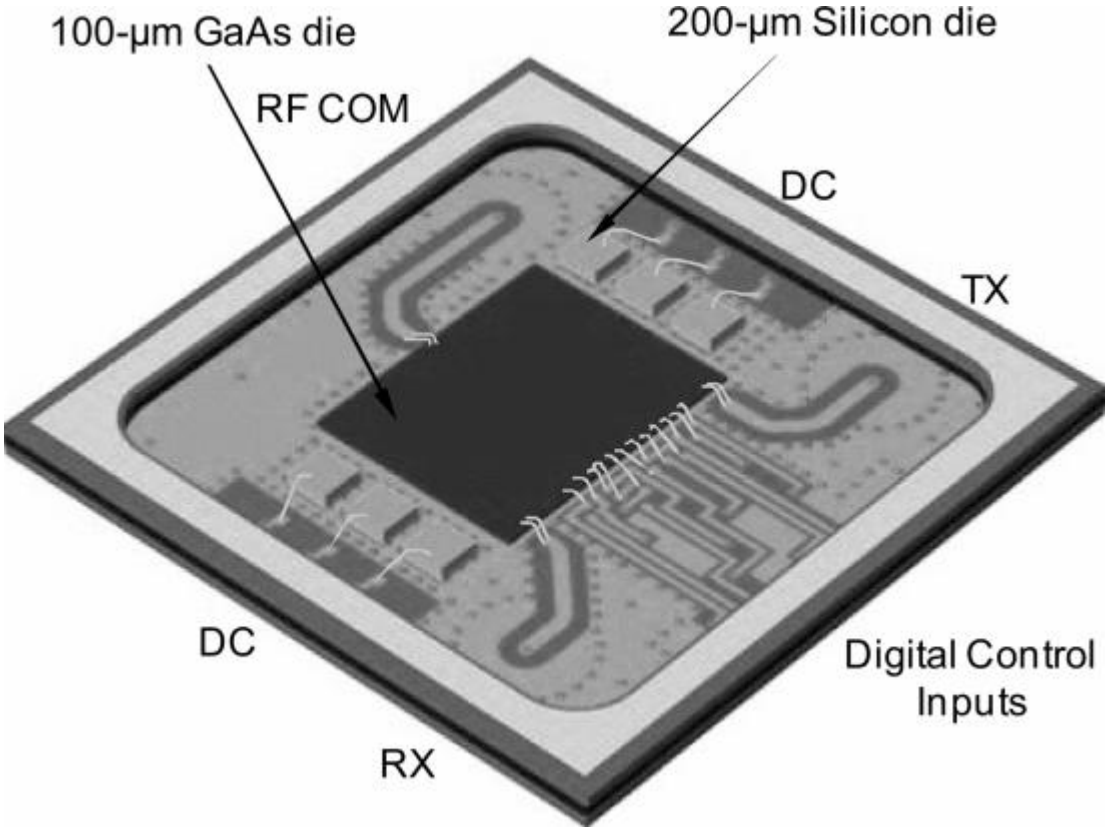
### Thermal implications

It can adapt to high current and high temperature resistance requirements, and has better thermal conductivity than ordinary PCB circuit substrates.

## Effects of vibrations

It has high reliability, can be applied to harsh environments, and prolongs its service life

## Package size vs I/Os




Front-side view of the 3 - layer LTCC package (size is 12 × 12 mm2) with MMIC die, decoupling capacitors and bond wires.

the following items are key considerations to realize a successful assembly of the entire package, namely LTCC + die + lid + BGA:

1.To define temperature profiles compatible between the different process steps (epoxy curing, lid attach-, balling reflows, etc.)

2.Determine optimum thickness for the LTCC stack to minimize shrinkage and achieve best coplanarity and substrate flatness

3.Define optimum lid and AuSn preform dimensions for a reliable hermetic seal

4.Optimize process to prevent ball bridging

The design and process trade-offs to address RF performance (loss, isolation, grounding, etc.), thermal aspects, SMT assembly and hermeticity, lead to the choice of a mutli-layer LTCC substrate coupled to a collective hermetic lid approach.

LTCC is easy to implement more wiring layers and increase assembly density. LTCC is easy to implement multi-layer wiring and package integration structure, further reducing the size and weight and improving reliability.

**LTCC package have advantages in thermal implication, effects of vibrations and package size and I/Os**

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