Comprehensive Power Loss Model of the Main Switch of the Flyback Converter

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Abstract—This paper advocates a comprehensive loss modeling of the DC- DC high switching frequency Flyback converter by taking into consideration of switching loss, conduction losses and gate charge losses of the main switch of the converter. For this aspect, it envisages a significant loss mechanism along with switching parameter. Effective Loss computation plays an important role to determine the performance of the converter to demonstrate with simple empirical equations. Finally, major losses along with the gate charge of the Flyback converter are included with simple explanations to boost up the overall performances and loss modeling of Flyback circuit. Due to above huge losses, the Flyback converter is used for low power industrial applications

Keywords—Flyback converter, Loss model, Switching losses, Conduction losses, Gate charge losses and performance analysis

I. INTRODUCTION

A loss of Flyback converter circuit reduces the efficiency and overall performances of the converter. The switching losses of main switch, leakage loss in the primary side of the Flyback transformer and Conduction losses of diode are prominent in the Flyback Converter. Due to above points, the Flyback converter is also used for low power applications. Basically loss modeling techniques are studied by the following ideas. Conduction losses are caused by the forward voltage drop when the power semiconductor is on. Conduction losses are the first area of evaluation. Conduction losses are grouped as dc losses incurred resistances in power path. As for example, I^2R, losses across on MOSFET and the current sense resistance. It is important to note that in determining the accurate value of loss term in the converter. Another very important mechanism is the switching losses. Switching losses characterized by the losses that are directly allied with frequency at which the circuit switches. Three significant switching loss mechanisms that were examined includes the MOSFET switching losses, transition losses occurring in the switch, secondary diode of the Flyback converter and finally leakage inductance losses. The second switching loss results from transition across both the switch and the diode. For example, at switch turn on, the voltage across the switch collapses as current in the switch increases. In other words, the current does not start to rise after the voltage across the switch collapses. Instead of two changes overlap and the crossover between voltage and current that leads to power loss. These losses are incurred both the turn on and off of the switch and the diode. It becomes very high for higher switching frequency operation. The third switching loss mechanism is a consequence of primary leakage inductance in the transformer. Leakage inductance is the term given to inductance inherent in the transformer that is not linked between primary and secondary. Leakage inductance exists between primary and secondary. In order to compute the leakage inductance present primary, secondary should be shorted. The consequential inductance in the primary side is the leakage inductance on the primary. Similarly secondary inductance is measured. The primary inductance normally is in the range of (1-5) % of the primary inductance. When the switch turns off, the primary leakage energy must be dissipated by the conventional snubber circuit to protect the power switch from excessive spurious spike voltage so that voltage rating of power MOSFET does not exceeds its the ratings based on availability of the power MOSFET without discussions of [1-13]

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II. DESIGN SPECIFICATIONS OF THE FLYBACK CONVERTER CIRCUIT

Range of input Voltage
V_{in} =180V-250V (DC)
Switching frequency of the converter, f_{sw}= 70 KHz,
Load = 2A
Magnetizing inductance L_m=400μH
Primary turns N_P =48
Secondary turns N_s=7
Load voltage V_o=24V

III. FUNDAMENTAL CONCEPTS OF LOSS MODEL

There are three major energy losses of the Flyback converter namely in the output diode rectifier, the conduction losses in the power MOSFET and loss due to leakage inductance of the coupled inductor (Flyback transformer) and switching losses of the maim switch of the converter. On the other hand gate charge and reverse recovery losses of the body diode of MOSFET may be included of the converter circuit based on these losses, simple mathematical expressions have been deduced by the fundamental equations with some assumptions of the Flyback power and control circuit combinable from where PWM signal will to

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regulate the load voltage and for tight regulations for the high switching frequency Flyback power converter circuit

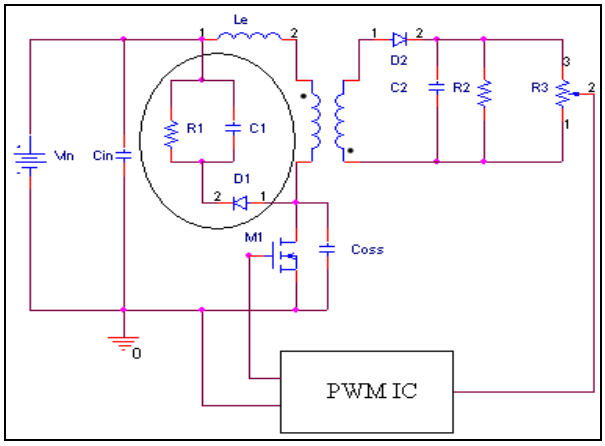

Fig. 1 Flyback converter with RCD clamp

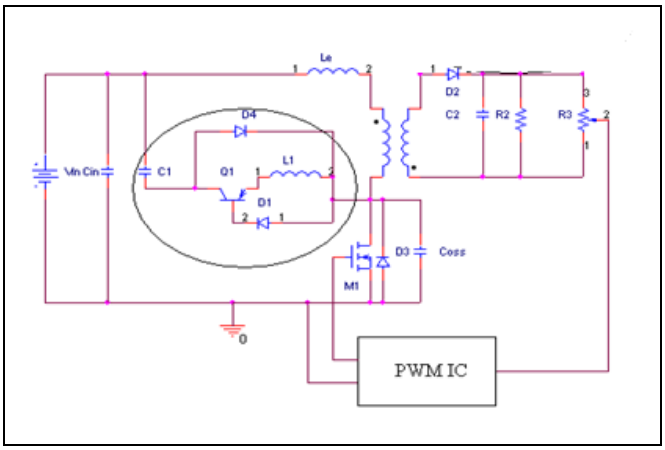

Fig. 2 Flyback converter with Transistorized clamp

IV. THEORY OF SWITCHING LOSSES

In order to work out the switching losses, considering the overlapping section as a triangle of small time (Δt) width shown below, the average power dissipated by the MOSFET at turn off is simple triangle area.

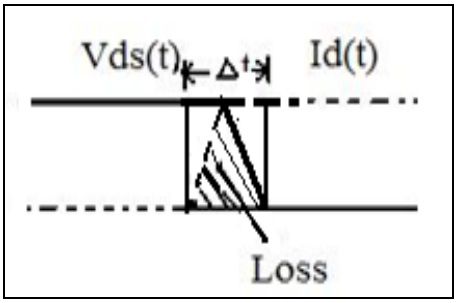

Fig. 3 Schematic Current and voltage overlap across power switch

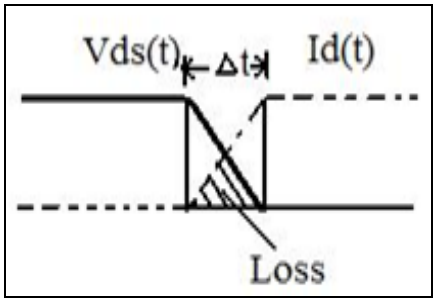

Fig. 4 Schematic Current and voltage overlap across power switch

Worst case takes place when the drain to source voltage, $V_{ds}(t)$ instantly rises up at the switch opening at Fig. 3. If some snubber exists to slow the voltage rise, the idealized at Fig. 4 can happen with more complimentary loss accounts.

$$P_{SW,Off} = \left[f_{SW} \left(\int_0^{\Delta t} i_d(t) v_{ds}(t) dt \right) \right] \quad (1)$$

Hard switching and its qualities have been discussed above in epigrammatic. Reduction of size and weight of converter systems need higher operating switching frequencies, which would reduces the sizes of inductors and capacitors. However, stresses on devices are seriously subjective by the switching frequencies accompanied by their switching losses. It is noticeable that switching-aid-networks do not alleviate the dissipation issues to a vast amount. Turn-on snubber though not discussed is rarely used. Even if used, it would not be able to prevent the energy stored in the junction capacitance to discharge into the switch at each turn-on. Soft switching techniques use resonant techniques to switch ON at zero voltage and to switch OFF at zero current. There are unimportant switching losses in the devices, though there is an important rise in conduction losses. There is no transfer of dissipation to the resonant circuit which is non-dissipative.

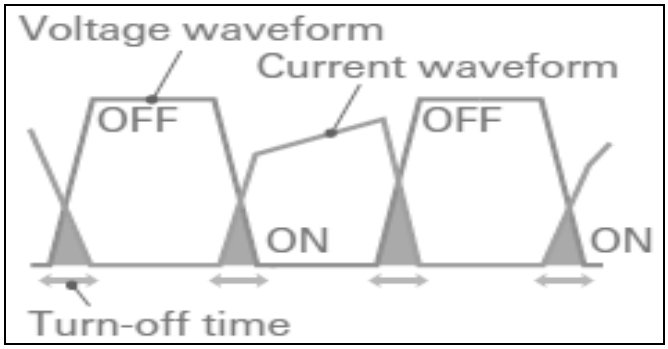

Fig. 5 Normal hard switching, the areas of overlap are switching losses (voltage current)

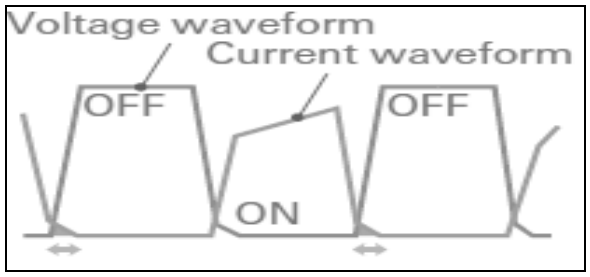

Fig. 6 normal soft switching, the areas of overlap are reduced and dead times created to reduce switching losses

The areas of overlap are reduced and dead times created to reduce switching losses. Soft switching is an advanced and highly industrial important technology that precisely controls the timing of the ON and OFF switching to reduce switching losses of power switches

V. COMPUTING SWITCHING LOSSES

The following Fig. 7 represents schematic switching losses MOSEFT. The curved line OHE and ABDGF indicates the current and voltage waveform during turn on condition respectively and it is to be considered straight line transient of the both current and voltage waveforms for simple computation. The overlapping area of the triangle, Δ0AB with current and voltage wave form represents the turn loss of the power MOSFET .The common expression of turn on switching loss is given by

$$P_{sw\,(on)} = f_{sw} \int_0^{T_{on}} i_d(t) v_{ds}(t).dt \qquad (2)$$

The switching loss plays a significant role for high frequency switching operation of power converter. The switching losses caused by the MOSFET during turn on and turn off while PWM pulse of gate signal is injected to gate to source for closed or open loop operation of the converter. For the diode, only the reverse recovery losses are considered because the other switching losses are very small and disappear in measurement noise. The diode switching losses seem to increase at currents above 1A. The reason for this performance is probably too much switching noise or measurement errors at high current.

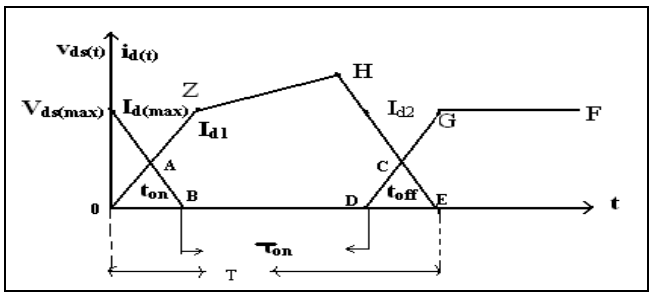

Fig. 7 Schematic voltage and current waveforms across the power MOSFET

From the Fig. 7, it can be written as in integral form

$$P_{sw\,(on)} = f_{sw}\left[\int_0^{t_{on}} \frac{I_d(max)}{t_{on}}\{V_{ds}(max)t - \frac{V_{ds}(max)t^2}{t_{on}}\}dt\right] \qquad (3)$$

$$P_{sw\,(on)} = f_{sw}\left[\frac{V_{ds}(max)I_d(max)t_{on}}{6}\right] \qquad (4)$$

Similarly, turn off loss represents the area ΔDCE of the triangle is given by

$$P_{sw\,(off)} = f_{sw}\left[\frac{V_{ds}(max)I_d(max)t_{off}}{6}\right] \qquad (5)$$

the turn off loss is highly pronounced compared to turn on loss of switching MOSFET. Hence, total switching losses given by

$$P_{sw\,(total)} = \frac{V_{ds}(max)I_d(max)(t_{on} + t_{off})f_{sw}}{6} \qquad (6)$$

Power losses during switching while current and voltage are non zero at the overlapping sector.

Due to the fact that a MOSFET does not turn on and off instantaneously, power is consumed during the transition of turning the switch off and on. These losses are known as switching losses. The second term of equation (7) takes into account the energy stored in the MOSFET's output capacitance that is internally dissipated during turn off. Now the first term of equation (7) makes the assumption that the drain to source voltage and current change linearly, and calculates the switching losses as the triangular area under the drain to source voltage and current transition periods,

$$\mathbf{P_{sw(total)}} = \frac{V_{ds}(max)I_d(max)(t_f + t_r)f_{sw}}{2} + \frac{1}{2}C_{OSS}V_{ds}^2(max)f_{sw} \qquad (7)$$

VI. COMPUTING CONDUCTION LOSS OF MOSFET

The conduction loss is simply given by, the integral of

$$P_{con} = \frac{1}{T}\int_0^{T_{on}} i^2(t)R_{dson}(t).dt \qquad (8)$$

The on time resistance (R_{dson}) of the MOSFET is temperature dependent. The conduction loss ends up with following closed form coming from the Fig.7. It has been expressed by considering particular operating temperature for R_{dson} and time period (T). Here T is equal to

$$T = \frac{1}{f_{sw}} \qquad (9)$$

$$P_{con} = (Id_1^2 + Id_1Id_2 + Id_2^2)\frac{T_{on}}{3T}R_{dson} \qquad (10)$$

For the surface mounted power MOSFET used in built Flyback converter, R_{dson} comparatively small of about 0.17E at a particular temperature. This gives a little conduction losses of the MOSFET though it will depend on input average current. The amount of energy is stored by leakage inductance (L_e) is given by as:

$$E_e = \frac{1}{2} L_e I_P^2 \quad (11)$$

Hence, power losses can be calculated by as:

$$P_e = \frac{1}{2} L_e I_P^2 f_{sw} \quad (12)$$

When the switch turns on, Leakage inductance produces very high voltage ringing. Their values depend on the input supply voltage and operating duty cycle. Typically it twice at 50% duty ratio following the following equation, voltage across leakage inductance given as:

$$V_e = \frac{V_{in}}{(1-D)} \quad (13)$$

This energy is recovered to the source by inserting the Transistorized clamp circuit converter at the primary side of the Flyback converter.

VII. CONDUCTION LOSS OF THE MOSFET BODY DIODE

This loss is only present when the MOSFET is turned off and the diode is freewheeling. The forward voltage drop (V_f) is to be found in data sheets, and for worst case scenario it will be held not constant but it depends on the duty ratio (D) for all loads follows as:

$$P_{diode} = (1\text{-}D)V_f I_o \quad (14)$$

Where V_f is the forward voltage drop of the body diode of power MOSFET and load current (I_o)

VIII. COMPUTING OTHER LOSSES IN THE MOSFET WITH CONDUCTION LOSSES

Total MOSFET's losses and maximum junction temperature, the choice of selecting a MOSFET is to reduce junction temperature go up by minimizing the power loss while being cost effective besides maximum voltage rating and maximum current rating others three vital parameters of a MOSFET are R_{dson}, gate threshold voltage, and gate capacitance. The switching MOSFET has three types of losses, conduction loss, switching loss, and gate charge losses. Conduction loss is equal to

$$P_c = I^2 R_{dson} D \quad (15)$$

Losses therefore the total resistance between the source and drain during the on state, R_{ds}on has to be as low as possible. Switching losses are equal to at switching frequency is given by generic form

$$P_s = V_{ds} I_d (t_r + t_f) f_{sw}. \quad (16)$$

Balancing core and winding losses

The switching time, rise time (t_r) and fall time (t_f) is a function of the gate to drain miller-charge of the MOSFET, Q_Gd, and the internal resistance of the driver and the threshold (Th) Voltage, V_{gs} (Th) the minimum gate voltage which enables the current through drain source of the MOSFET. Gate charge losses are caused by charging up the gate capacitance and then dumping the total charge to ground (Q_G) every cycle. The gate charge losses are equal to frequency

$$E_g = Q_G V_{ds} f_{sw} \quad (17)$$

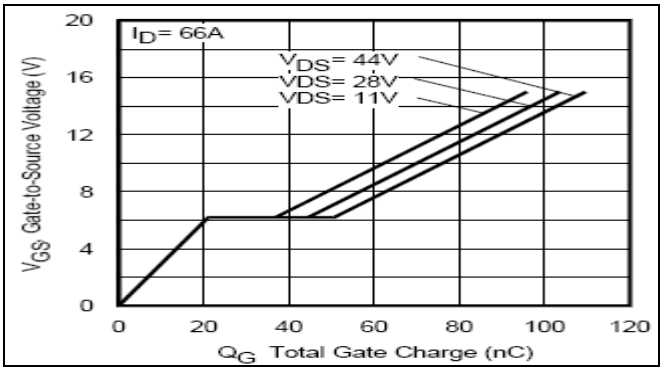

Fig. 8 Representation of MOSFET's V_{GS} vs. Q_G

Regrettably, the lowest on resistance devices tend to have higher gate capacitance. Because this loss is switching frequency dependent, in very high current supplies with very large MOSFET, with large gate capacitance, a more optimal design may effect from reducing operating frequency. Switching losses are also affected by gate capacitance. If the gate driver has to charge a larger capacitance, then the time the MOSFET expends in the linear area increases and the losses increase the faster the rise time, the lower the switching loss. Unfortunately, these cause high frequency noise.

When inductors are designed for the discontinuous mode, with imperative core loss, total loss is at abroad minimum when core and winding losses are approximately equal. But when inductors are designed for the continuous mode, core loss is often negligible, so that the total loss limit can be allocated entirely to the windings. Common considerations, core idyllic magnetic materials cannot store energy. Practical magnetic materials store very little energy, most of which ends up as loss. In order to accumulate and return energy to the circuit competently and with minimal physical dimension, a small non-magnetic gap is required in series with a high permeability magnetic core material. In ferrite or laminated metal alloy cores, the required gap is actually discrete, but in powdered metal cores, the gap is distributed among the metal particles. Paradoxically, approximately all of the magnetic energy is stored the so-called "non-magnetic" gap(s).The sole point of the high permeability core materialism to offer an easy, low reluctance flux path to link the energy stored in the gap to the winding, thus efficiently coupling the energy storage space or spot (the gap) to the external network or circuit The effect of a transistorized snubber as shown in the Fig. 2, in the encircled part, on the switch may be viewed as changing, or shaping, the load line on the switch for a particular purpose. An inductor in series with the transistor switch, a current snubber, presents the switch with an inductive load at turn-on so that it switches on with zero current. This is a modification of the load which would typically be somewhat

capacitive at turn-on. The same is true at turnoff with a voltage snubber. At turn-off the load on the switch will typically look inductive so a capacitor in shunt with the switch, a voltage snubber, will change the load line to be capacitive so that the switch can turn off at zero voltage

The main difference of the isolated compared to basic topology is large value of leakage inductance L_e of the high frequency power transformer, which can cause a destructive surge voltage on the power switch. To tyrannize this outcome, it is invented by the innovative snubber circuit, which causes no power losses in converter due to its energy recovery character in Fig. 3 shown alone when it is connected in Flyback converter properly to recover the leakage energy of the Flyback transformer.

From the literalized simple diagrams, the expression for evaluating the surge voltage can easily be derived on condition of zero voltage balance in L1 and zero current balance in C3 during the period assuming the equal forward voltage drop on the diode D1 and the base-emitter leads of transistor Q1, we finally receive very simple expression for calculating by the flowing empirical equation as shown below.

$$Le=7*L1*\Delta V_{BE}/9\Delta V_e \quad (18)$$

Alternatively, it can be measured by instrument by shorting the secondary of the transformer

$$I_C=\beta_1 I_B+(1+\beta_1)I_{C\,BO} \quad (19)$$

Where, ΔV_{BE}, is the change of base to emitter voltage,

ΔV_e= is the change of the emitter voltage of Q1 due to different primary current I_p and load current , I_C is the collector current, I_{CBO} is the collector to base leakage current and β_1 is gain of the power transistor (Q1) respectively. When the power MOSFET of the Flyback converter is on, the leakage energy (P_e) will be discharged by the inductor L1. When emitter voltage will be negative, base of the transistor is experienced on some voltage and collector terminal voltage will be positive. Then this transistor (Q1) will be on, leakage energy will send to source. When power switch of Flyback converter is off, the voltage (V_{off}) across it without consideration of spike voltage given by

$$V_{off}=V_{in}+NV_o \quad (20)$$

Energy stored by the capacitor C_{oss} is given by

$$E_2=0.5C_{oss}V^2_{off} \quad (21)$$

E_2 energy is slowly discharged through inductor, L1, giving rise also high positive emitter voltage compare to it base to emitter voltage for which the transistor (Q1) will be on to send the leakage energy to source and discharge it through diode D4 and MOSFET (M1) during on time. The capacitor (Coss) enhances the zero voltage switching operation and to improve the converter efficiency. The similar circuit with transistor (Q1) is placed across the output diode of the Flyback converter to reduce the partial conduction loss of diode by pronounced ZCS operation. C1 which is the voltage dumping capacitor to maintain a voltage source when discharge current coming from the inductor (L1) is connected with transistor (Q1) for the rectifier diode snubber. Diode D4 acts here voltage blocking diode to prevent the current path via source to Flyback MOSFET when the Flyback MOSFET is on. Neglecting on resistance of MOSFET, voltage is being nearly zero across the Flyback switch when the Flyback switch is on.

$$E_2=E_L=0.5L1\ i^2(t) \quad (22)$$

This energy will be balanced by the dump capacitor (C3) storing energy is given by

$$E_3=0.5C3V^2_{off} \quad (23)$$

This transistorized clamp circuit can reduce leakage loss of secondary side of the Flyback converter the switching losses conduction losses and reverse recovery losses of the Flyback diode (D2). The voltage across the Flyback diode (D2), (V_d) at the time of off condition of the diode is given by

$$V_d=N*V_0 \quad (24)$$

Where N is the turn's ratio of the Flyback converter and V_0 is the output voltage of the converter. Here, V_d will be negative due to presence of inductor (L1) and also as per Lenz law of electromagnetic induction. In this way transistor of snubber circuit will be will on when the diode (D2) is off and similar way reverse recovery effect and losses at this condition drastically eliminates and decreases to improve the circuit efficiency of the converter.

IX. SIMULATION RESULT

The below simulation graphs obtained by drawing and running circuit by using software Orcadrelease-9.2 show the confirmation of the ZV-ZCS with high efficiency of the prototype Flyback converter as described and shown below

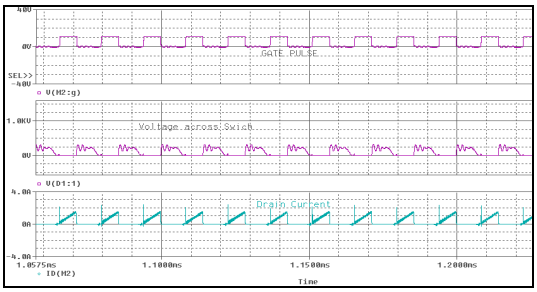

Fig. 8 Simulated switching waveforms of the main switch of the Flyback coveter for using Transistorized clamp for a load 1A

Gate pulse of the MOSFET, voltage across the power and its Drain current of MOSFET. The above Fig. 8 shows, there is trivial overlapping area between voltage and current waveform, so it reveals minimum switching power loss under ZVS and ZCS operation of the main power switch of the Flyback converters at the turn-on and turn-off state. Both ZVS and ZCS circumstance convince under different load conditions. The Fig. 8 also confirms of the ZVS at turn off condition and ZCS turn on of the prototype Flyback converter

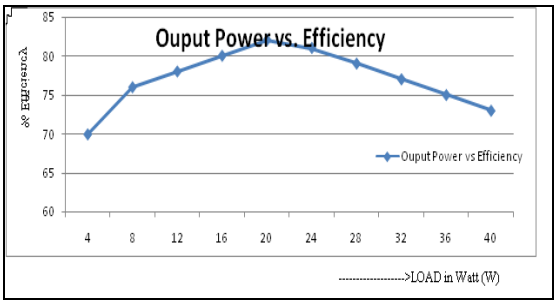

Fig. 9 Load vs. Efficiency curved using RCD clamp

In the Fig. 9, X-Axis represents percentage efficiency and Y-Axis represents the output power in watt of the Flyback converter using hard switching or RCD clamp circuit for its results

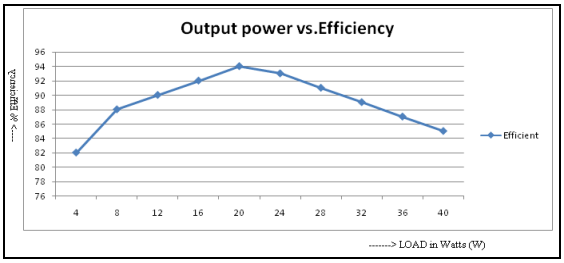

Fig. 10 Load vs. Efficiency curved using Transistorized clamp

In the Fig. 10, X-Axis represents percentage efficiency and Y-Axis represents the output power in watt of the Flyback converter using soft switching or using transistorized snubber circuit. At different load of the Flyback converter efficiency attained 94 %. The above experimental graphs show the confirmation of the ZV-ZCS using new transistorized clamp with higher converter efficiency. It can be used as a prototype of enhanced Flyback converter and industrial product as light weight, compact size, low cost and high converter efficiency

X. CONCLUSION

A qualitative approach for the computation of power losses in Flyback converters in the case of the discontinuous continuous conduction mode and for a constant switching frequency has been presented. The whole analysis has been based on the direct and indirect calculations. As it has been proved, for practical applications, appropriate in order to convince these demands, combining an optimum design and loss model strategy for the development of such converter circuit with high power, high circuit efficiency, high power density and adequate limited current, voltage stresses on the semiconducting devices

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