Power Topologies Review

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FAE Training
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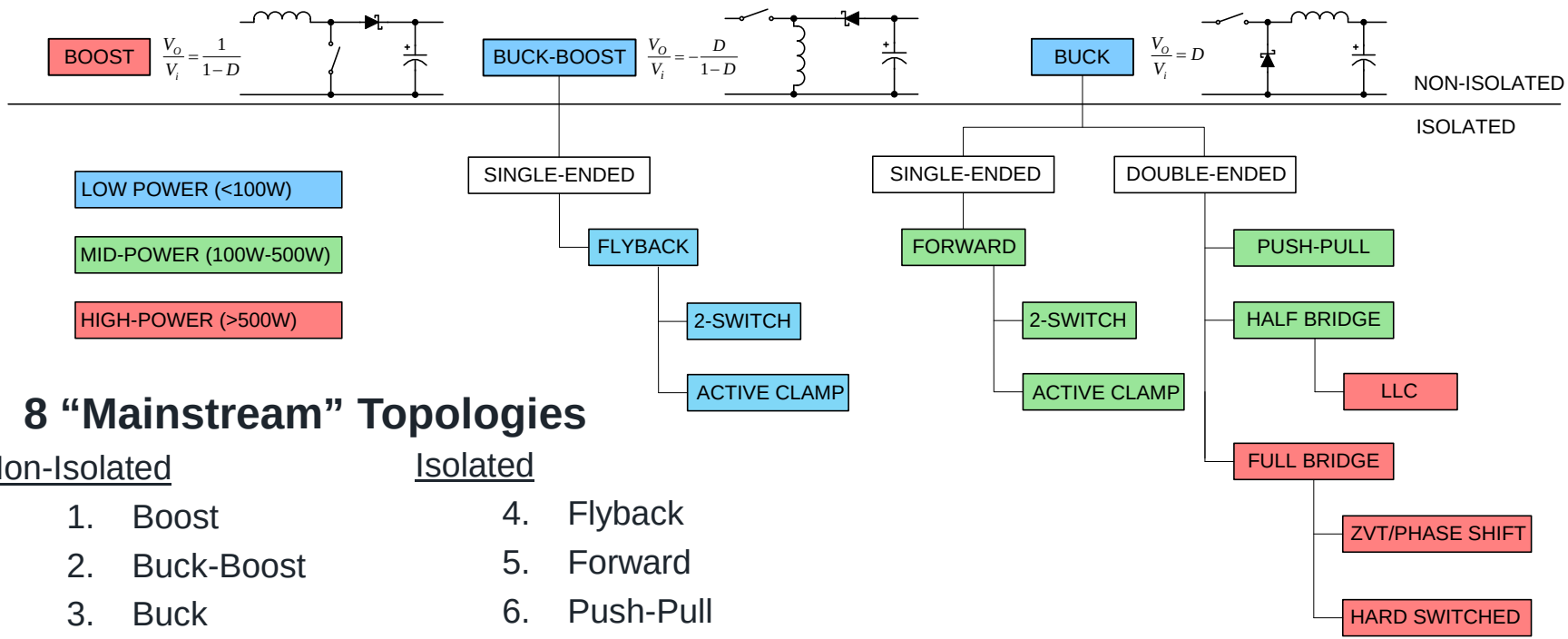
Agenda

- Non Isolated Converter Topologies and Their Isolated DC/DC Derivatives
  - PFC Boost
  - Buck
  - Buck-Boost
- Single Ended Converter Topologies
  - Transformer Reset Techniques
  - Forward Converter
  - Flyback Converter
- Double Ended Converter Topologies
  - Push Pull
  - Half Bridge
  - Full Bridge
  - Phase Shifted Full Bridge
- Synchronous Rectification
  - Current Doubler Rectifier

Isolated Power Topology Derivatives



- **8 "Mainstream" Topologies**

Non-Isolated

1. Boost
2. Buck-Boost
3. Buck

Isolated

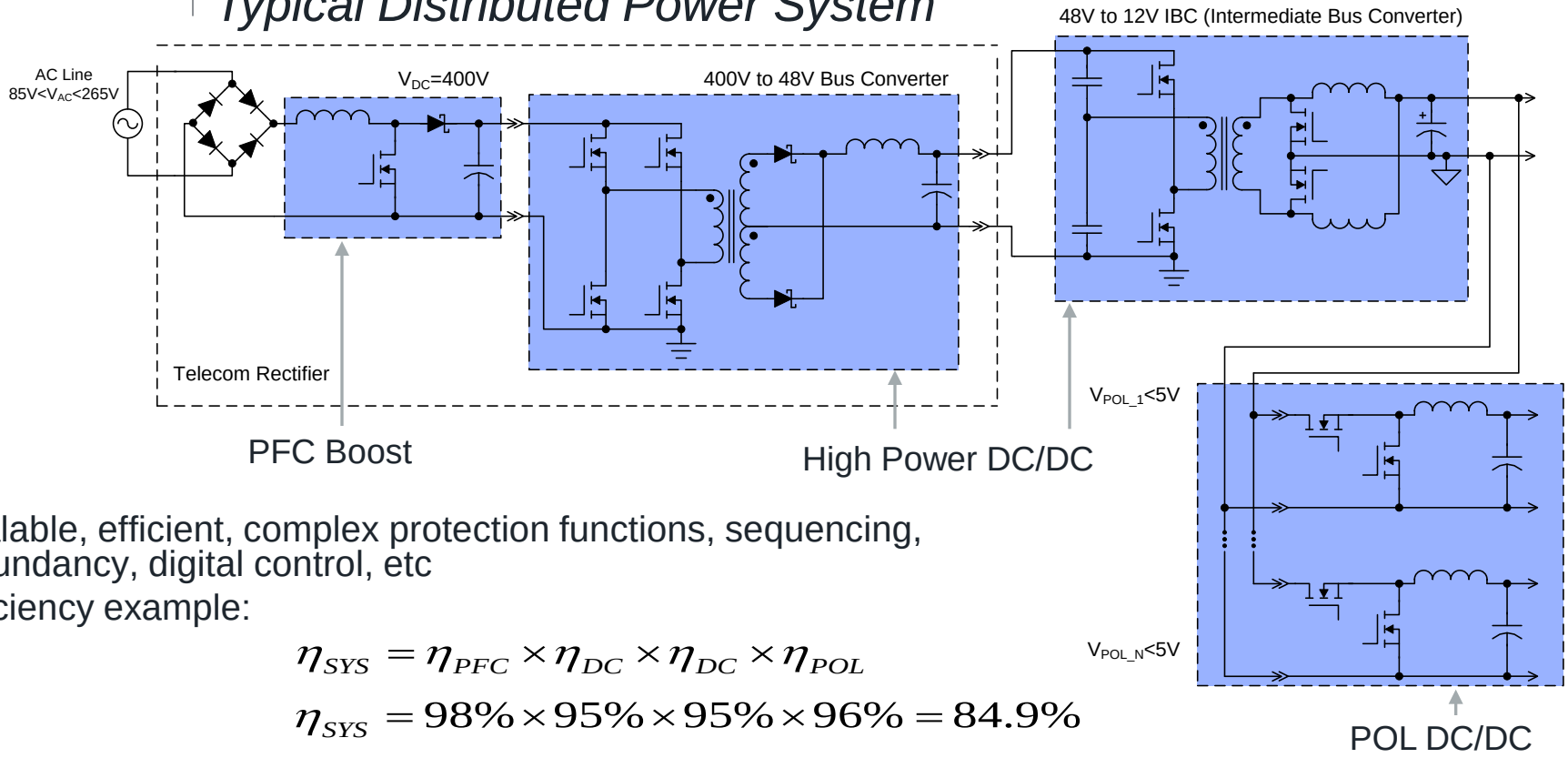
4. Flyback
5. Forward
6. Push-Pull
7. Half Bridge
8. Full Bridge

Other Topologies?

- Numerous Variations Exist
  - Sepic
  - Cuk
  - Current Fed Buck
  - Tapped Inductors
  - Multiple Outputs
  - Interleaving
  - More?
- Different Ways to Operate Them
  - Voltage Mode Control
  - Current Mode Control
  - Digital Control
  - Variable Frequency
  - CCM, DCM, BCM
  - ZVS
  - ZCS
  - Synchronous Rectification
- Some Practical Converter Topology Advice
  - *Most* power conversion requirements can be met using one or more of the 8 mainstream topologies
  - Save more difficult topologies for unique application requirements
  - Beware of publications proclaiming the “best” topology

Multi-Stage Topology

Typical Distributed Power System



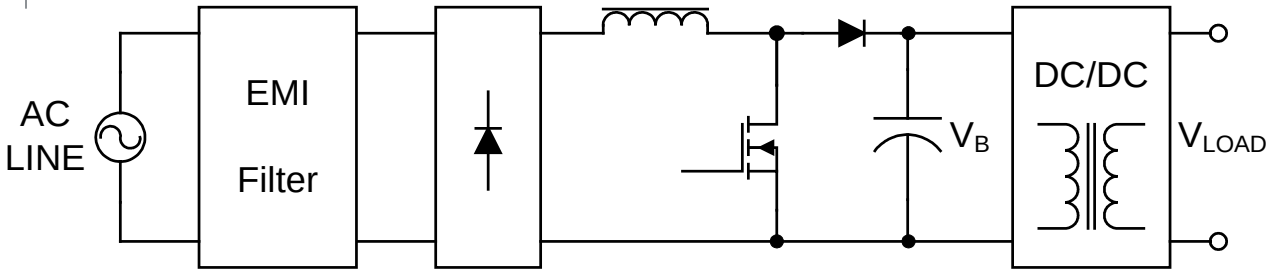
- Scalable, efficient, complex protection functions, sequencing, redundancy, digital control, etc
- Efficiency example:

$$\eta_{SYS} = \eta_{PFC} \times \eta_{DC} \times \eta_{DC} \times \eta_{POL}$$

$$\eta_{SYS} = 98\% \times 95\% \times 95\% \times 96\% = 84.9\%$$

- **Non-Isolated Converter Topologies**
- Single Ended Converter Topologies
- Double Ended Converter Topologies
- Synchronous Rectification

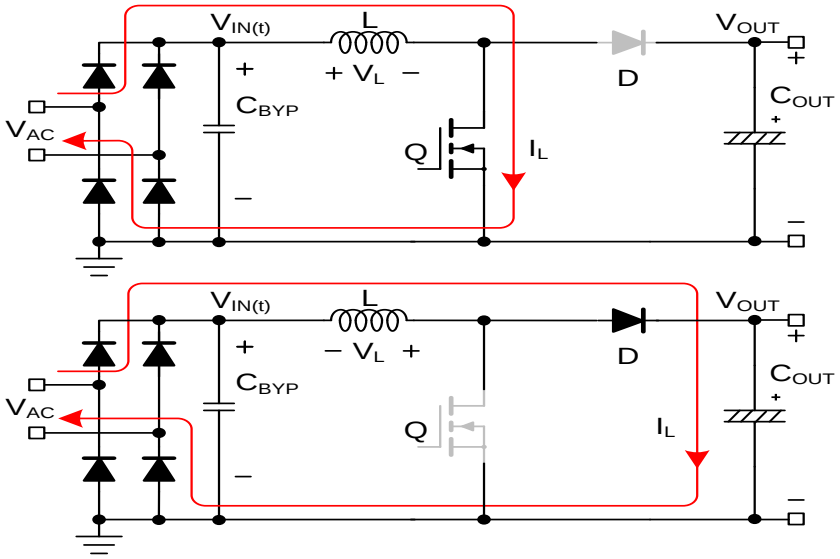
Boost Converter

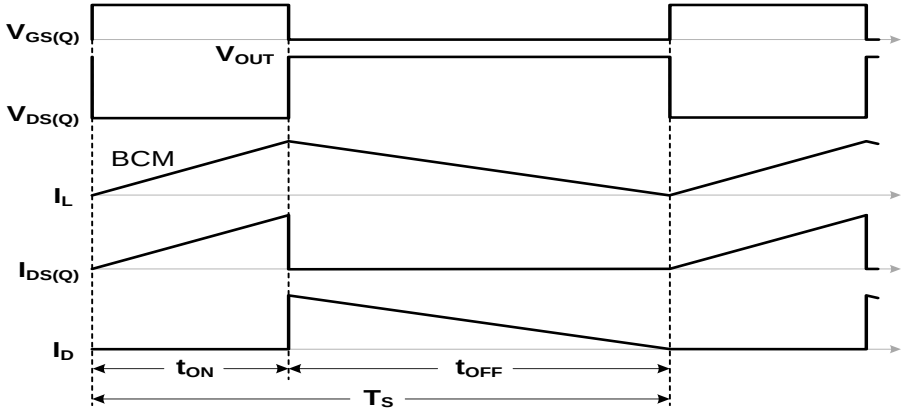


- Most popular topology for Power Factor Correction
  - Simple power stage
  - Efficient energy storage
  - Continuous input current waveform
  - $V_{IN}<V_{OUT}$
- Operating modes
  - CCM – fixed frequency, best PF and THD, Any Power Level
  - BCM – variable frequency, good PF and THD, <300W
  - DCM – never used intentionally but unavoidable at light load

    → Usually power factor correction capability is lost

Boost Converter





Boost transfer function:

$$\frac{V_{OUT}}{V_{IN(t)}} = \frac{T_S}{t_{OFF}} = \frac{1}{1-D}$$

Inductor volt-second balance:

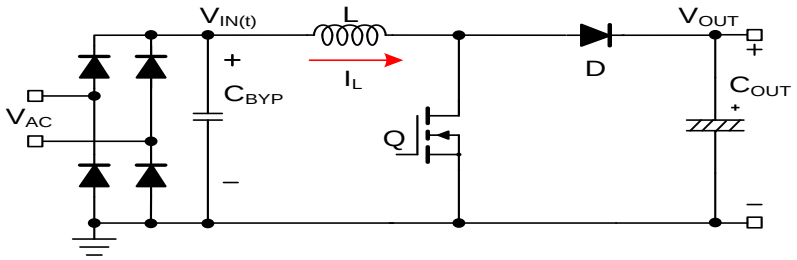
$$\langle V_L \rangle_{T_S} = V_{IN(t)} \times t_{ON} + \left[\left(V_{IN(t)} - V_{OUT} \right) \times t_{OFF} \right] = 0$$

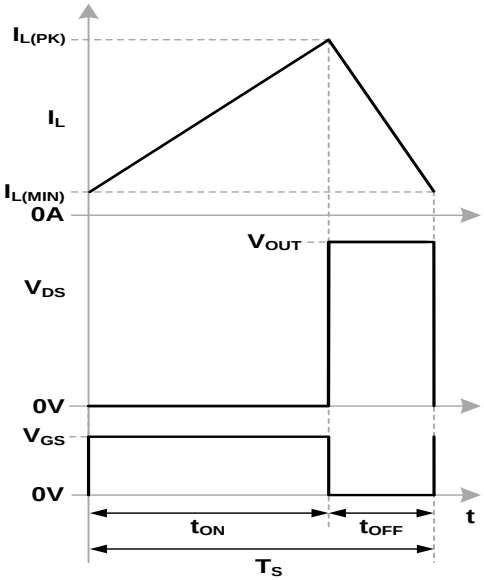
$$V_{IN(t)} \times (t_{ON} + t_{OFF}) = V_{OUT} \times t_{OFF}$$

$$V_{IN(t)} \times T_S = V_{OUT} \times t_{OFF}$$

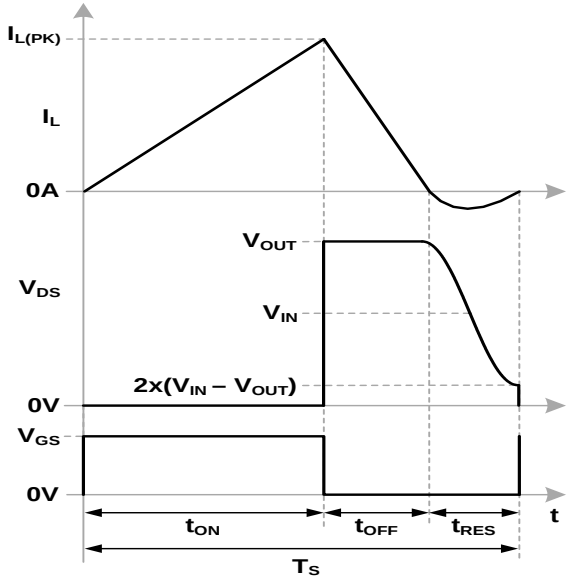
- V_{IN}<V_{OUT}
- Most efficient at lower D
- Continuous input current
- High PF, low THD
- CCM, BCM, DCM modes

Operating Mode

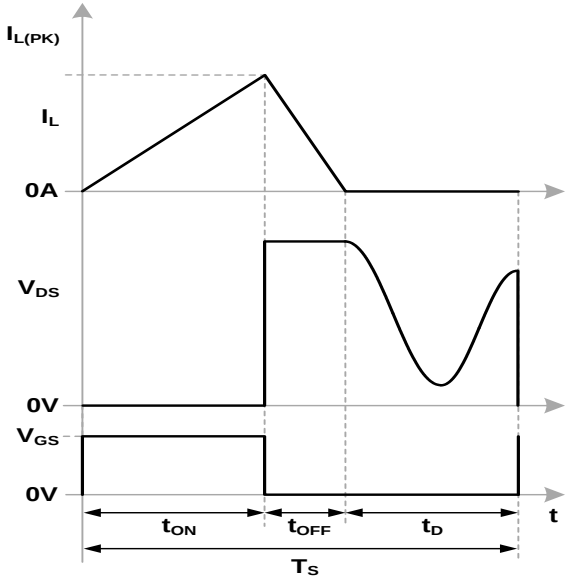




CCM

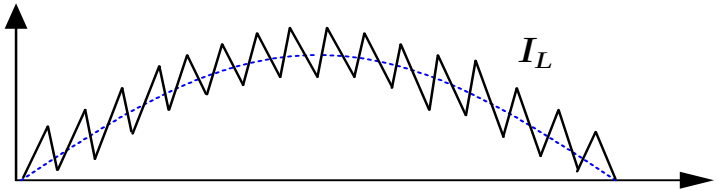


BCM



DCM

Continuous Conduction Mode (CCM) PFC



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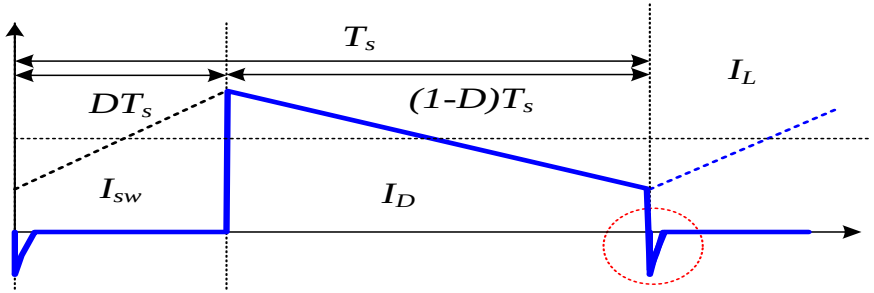
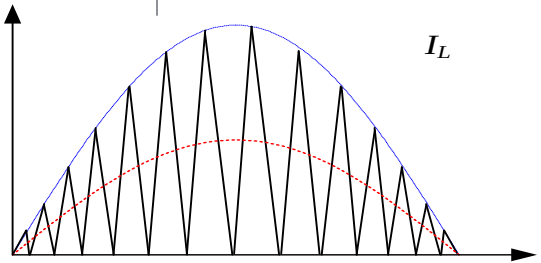


- Advantages
  - Low Ripple current: Lower core losses
  - Lower EMI : Smaller Input Filter
  - Simple inductor design
  - Fixed frequency operation, best PF and THD
  - Can be used at any power level
  - Easily interleaved for power levels up to many KW
- Disadvantages
  - Requires very fast boost diode with low I_{RR}
  - Silicon Carbide diodes are often used
  - Larger Inductor
  - MOSFET Switching Loss (hard switching)

Boundary Conduction Mode (BCM) PFC



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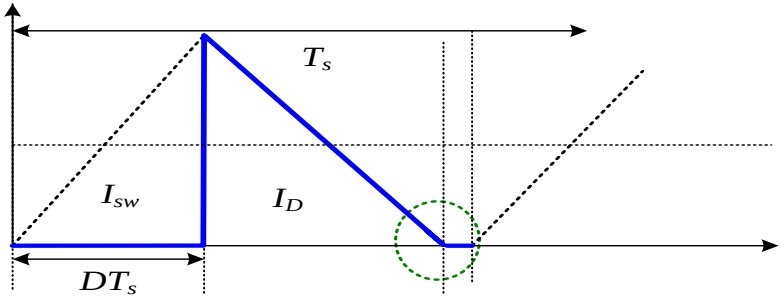
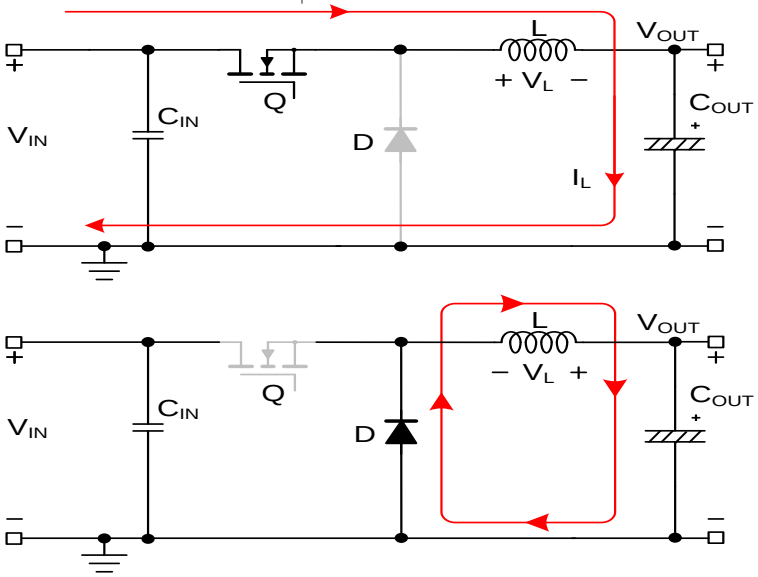
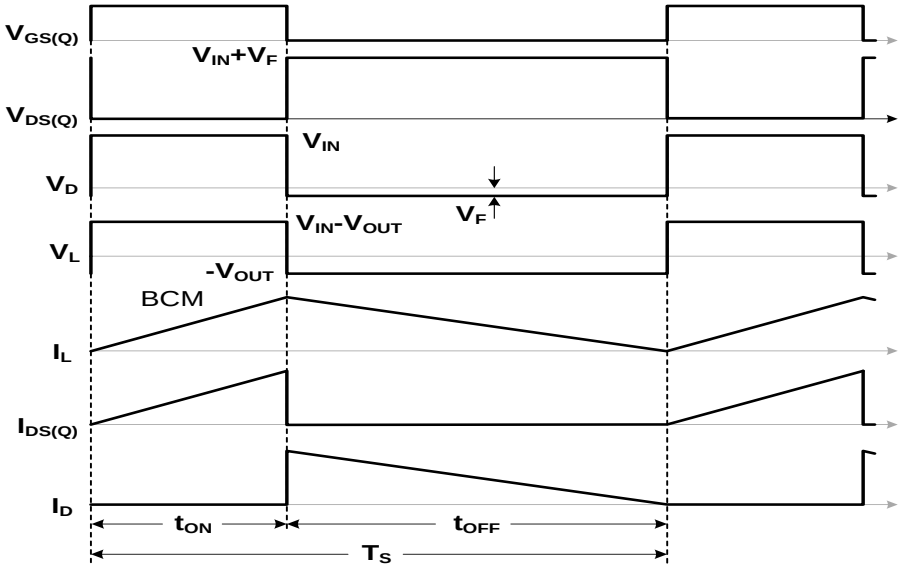


- Advantages
  - MOSFET turns on at zero current
  - ZVS/valley switching
  - No reverse recovery in boost diode (low cost, low V_F diode can be used)
  - Higher efficiency compared to CCM
- Disadvantages
  - Larger MOSFET conduction loss
  - Variable Frequency
  - Inductor design can be complex
  - High peak current limits practical use to ~300W (Impact on EMI filter)

Buck Converter





Inductor volt-second balance:

$$\langle V_L \rangle_{T_S} = [(V_{IN} - V_{OUT}) \times t_{ON}] - V_{OUT} \times t_{OFF} = 0$$

$$V_{IN} \times t_{ON} = V_{OUT} \times (t_{ON} + t_{OFF})$$

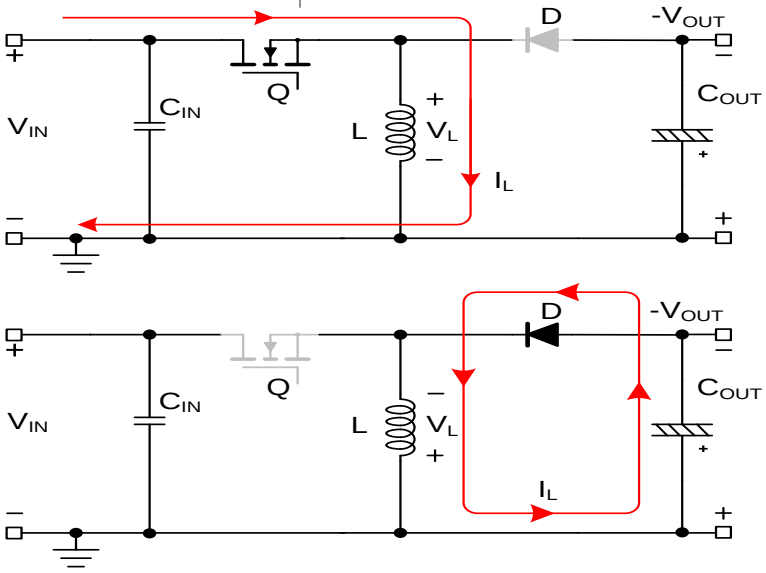
$$V_{IN} \times t_{ON} = V_{OUT} \times T_S$$

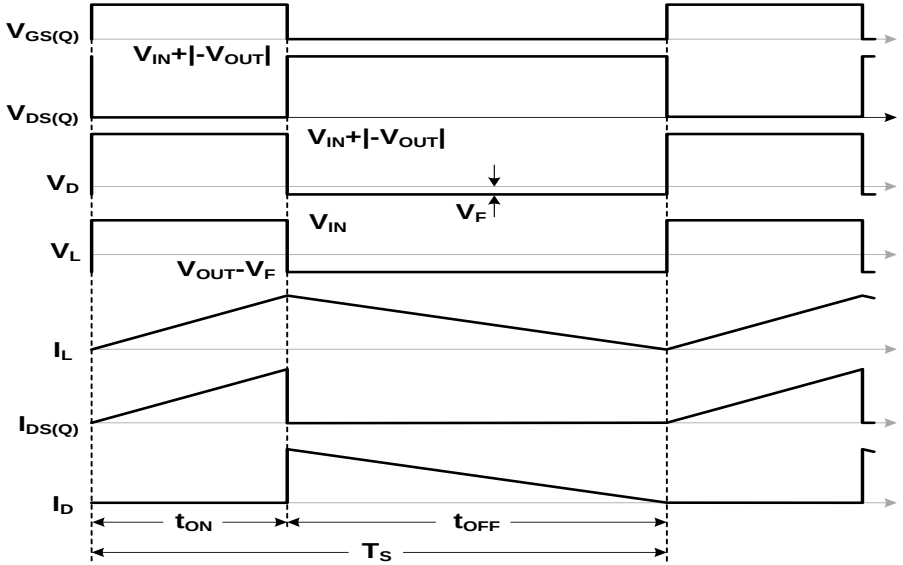
Buck transfer function:

$$\frac{V_{OUT}}{V_{IN}} = \frac{t_{ON}}{T_S} = D$$

- $V_{IN} > V_{OUT}$
- Most efficient at higher D

Buck-Boost Converter





Inductor volt-second balance:

$$\langle V_L \rangle_{T_S} = V_{IN} \times t_{ON} + V_{OUT} \times t_{OFF} = 0$$

$$V_{IN} \times t_{ON} = -(V_{OUT} \times t_{OFF})$$

$$\frac{V_{OUT}}{V_{IN}} = -\left(\frac{t_{ON}/T_S}{t_{OFF}/T_S}\right) = -\left[\frac{t_{ON}/T_S}{(T_S - t_{ON})/T_S}\right]$$

Buck-Boost transfer function:

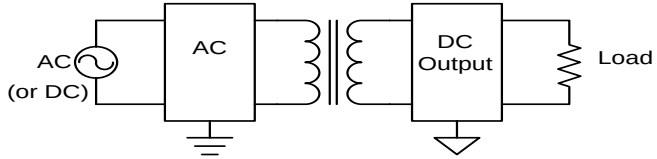
$$\frac{V_{OUT}}{V_{IN}} = -\left(\frac{D}{1-D}\right)$$

- V_{IN}<V_{OUT} or V_{IN}>V_{OUT}
- Used for negative V_{OUT}

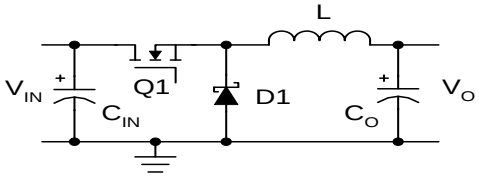
- Non-Isolated Converter Topologies
- **Single Ended Converter Topologies**
- Double Ended Converter Topologies
- Synchronous Rectification

Benefits of a Transformer

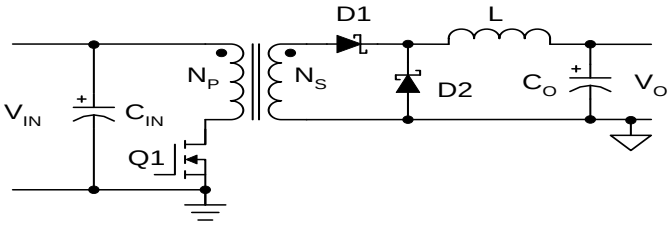
1. Provides primary to secondary safety isolation – subject to regulatory standards



2. Voltage conversion resolution



$$\frac{V_O}{V_{IN}} = D$$



$$\frac{V_O}{V_{IN}} = \frac{N_S}{N_P} D$$

Ex: For F_{SW}=300kHz (T_{SW}=3.33µs), N_P:N_S=4:1, 36V<V_{IN}<75 and V_O=5V

Buck Converter

6%<D<14%

200ns<t_{ON}<467ns

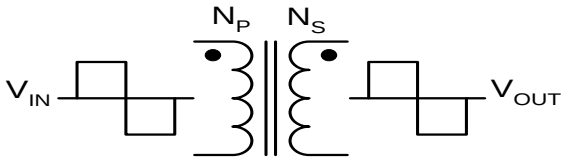
Isolated Buck (Forward) Converter

27%<D<55%

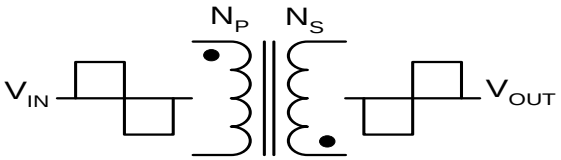
900ns<t_{ON}<1.8µs

3. Multiple outputs can be regulated/quasi-regulated

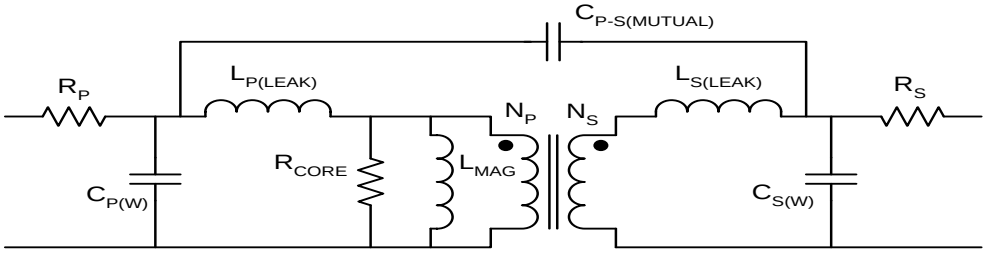
Transformer Characteristics



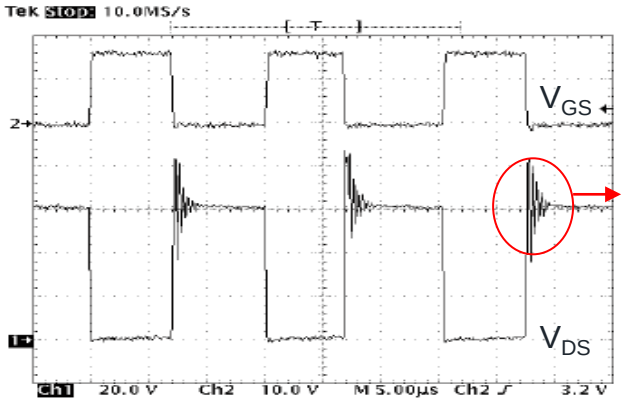
- Ideal transformer
  - Perfect coupling between N_p:N_S
  - No energy storage



- Flyback “transformer”
  - Really a coupled inductor
  - Primary energy stored during t_{ON}
  - Power transferred during t_{OFF}



Parasitic Transformer Model

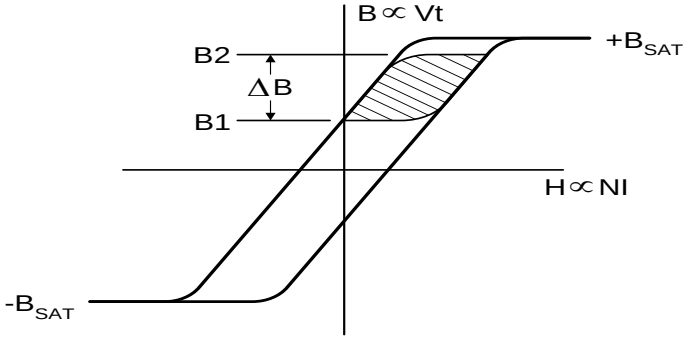


Overshoot/ringing due to Leakage Inductance

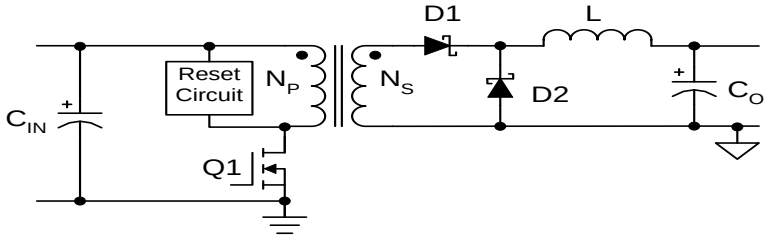
CCM Flyback

Single Ended Topologies Defined

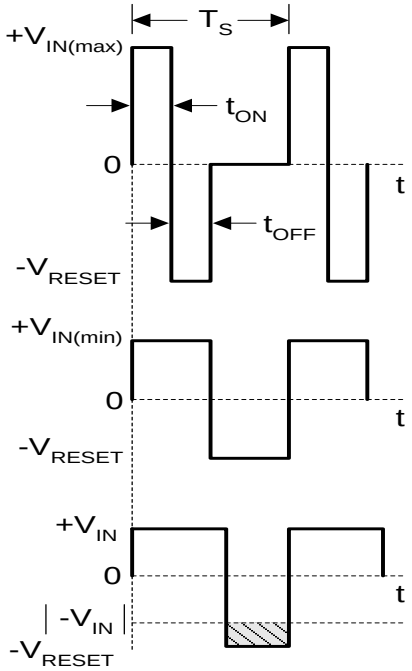
***Single Ended* – Transformer operation limited to first quadrant**



(a) Transformer Hysteresis



(b) Forward Converter



D=25%

$$|+V_{IN(max)} \times t_{ON}| = |-V_{RESET} \times t_{OFF}|$$

$$|+V_{IN(max)}| = |-V_{RESET}|$$

$$t_{ON} = t_{OFF}$$

$$V_{DS(Q1)} = 2 \times V_{IN}$$

D=50%

D>50%

$$|+V_{IN} \times t_{ON}| = |-V_{RESET} \times t_{OFF}|$$

$$|+V_{IN}| < |-V_{RESET}|$$

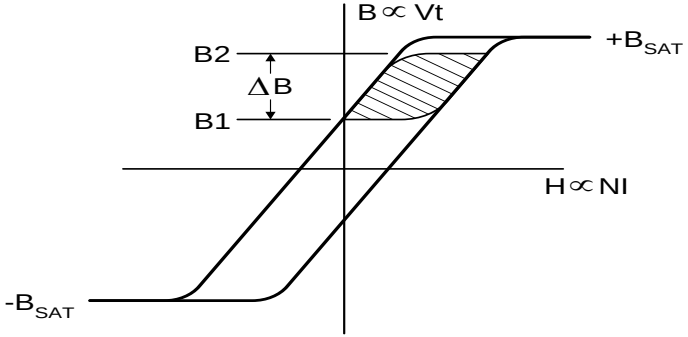
$$t_{ON} > t_{OFF}$$

$$V_{DS(Q1)} > 2 \times V_{IN}$$

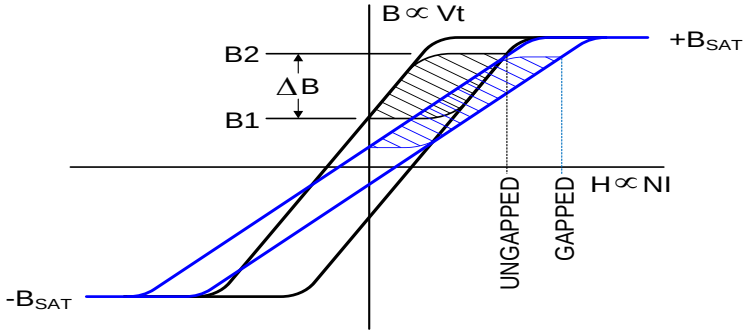
(c) Transformer Volt-Second Balance

Single Ended Topologies Defined

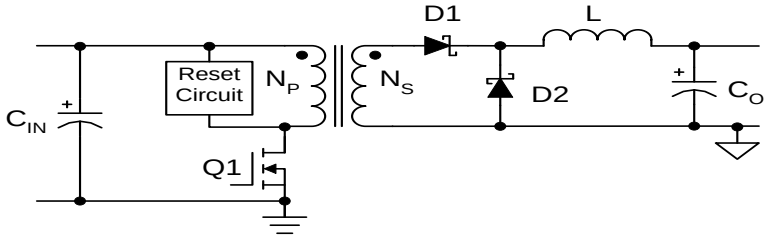
***Single Ended* – Transformer operation limited to first quadrant**



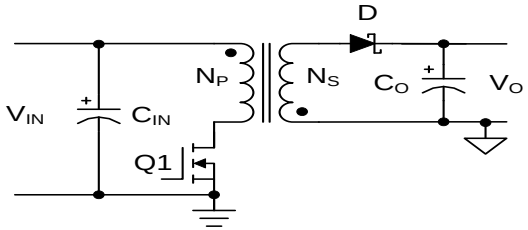
(a) Transformer Hysteresis



(c) Gapped Flyback “Transformer”

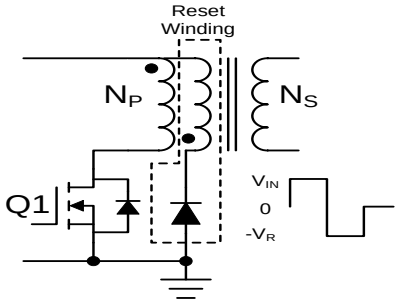


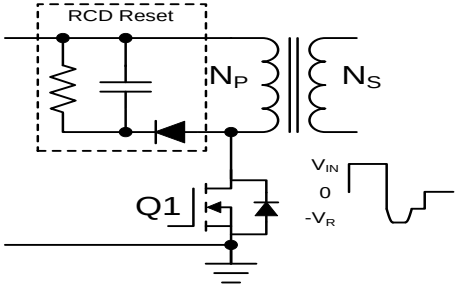
(b) Forward Converter

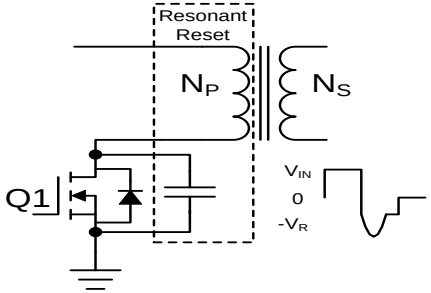


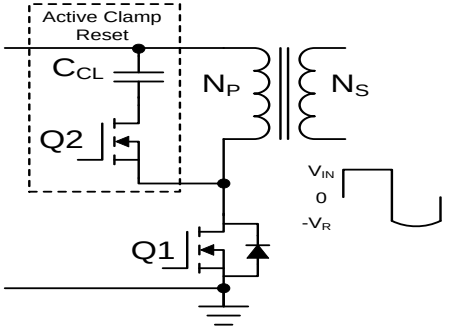
(d) Flyback Converter

Single Ended Transformer Reset Techniques









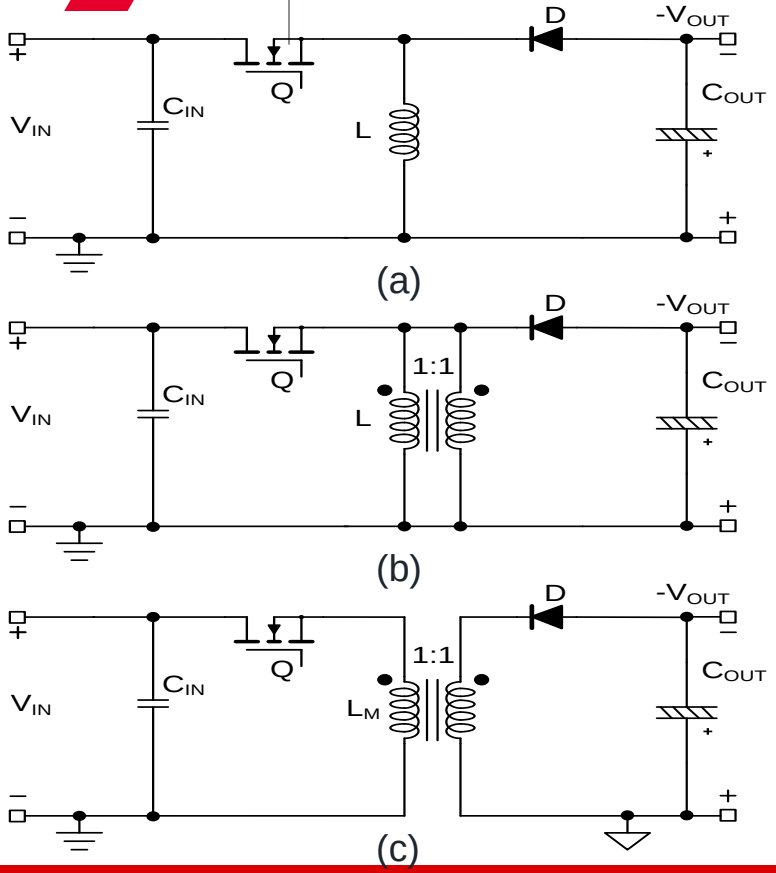
Reset Winding
+ Reset Energy Recycled
+ Simple Off-Line Solution
- 50% Duty Cycle Limit (1:1)
- Possible Core Saturation
- Transformer Structure
- Q1 Hard Switched

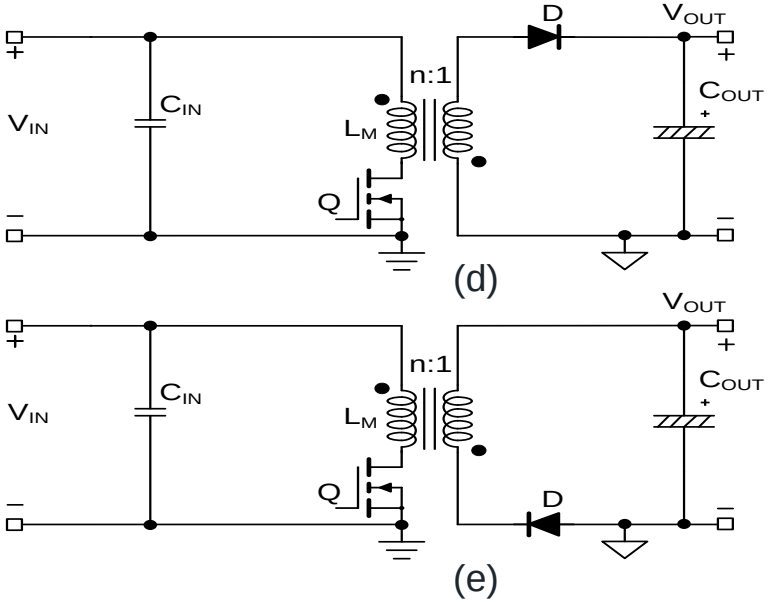
RCD Reset
+ Inexpensive Off-Line Solution
+ >50% Duty cycle Possible
- Reset Energy Dissipated
- Q1 Hard Switched

Resonant Reset
+ Reset Energy Recycled
+ Fewest Components
+ Simple Telecom Solution
- Repeatable Design Difficult
- High VDS Stress
- Not for Off-Line Power
- Not Suitable for Self-Driven SR
- Q1 Hard Switched

Active Clamp Reset
+ High Efficiency (ZVT)
+ Higher Frequency Operation
+ Lowest Vds Stress
+ Off-Line and Telecom
+ SR Gate Drive
- Q1, Q2 Gate Drive
- Higher Cost
- Limited PWM and/or Driver Choices

Flyback Converter Derivation





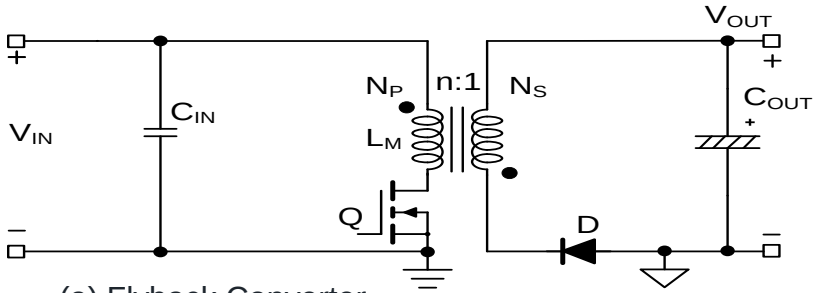
a) Non-isolated buck-boost
b) Coupled inductor buck-boost
c) Isolated buck-boost
d) Isolated flyback converter
e) D can be in return path

Flyback Converter Operating Modes

- Discontinuous Conduction Mode (DCM)
  - *Advantages (DCM):* Smaller transformer, trr of output rectifiers is less of an issue since current is zero before reverse voltage appears, single pole characteristic of the power circuit simplifies compensation
  - *Disadvantages (DCM):* Peak currents in the switch and diodes are considerably greater, ripple currents in output capacitors are much greater than continuous mode
- Continuous Conduction Mode (CCM)
  - *Advantages (CCM)* = Peak currents in the switching devices are lower, ripple currents in the output capacitors are lower
  - *Disadvantages (CCM)* = Larger transformer is required, right half plane zero (RHPZ) shows up in the control loop thereby complicating compensation
- Boundary Conduction Mode (BCM)
  - Variable frequency

Flyback Converter

CCM Operation

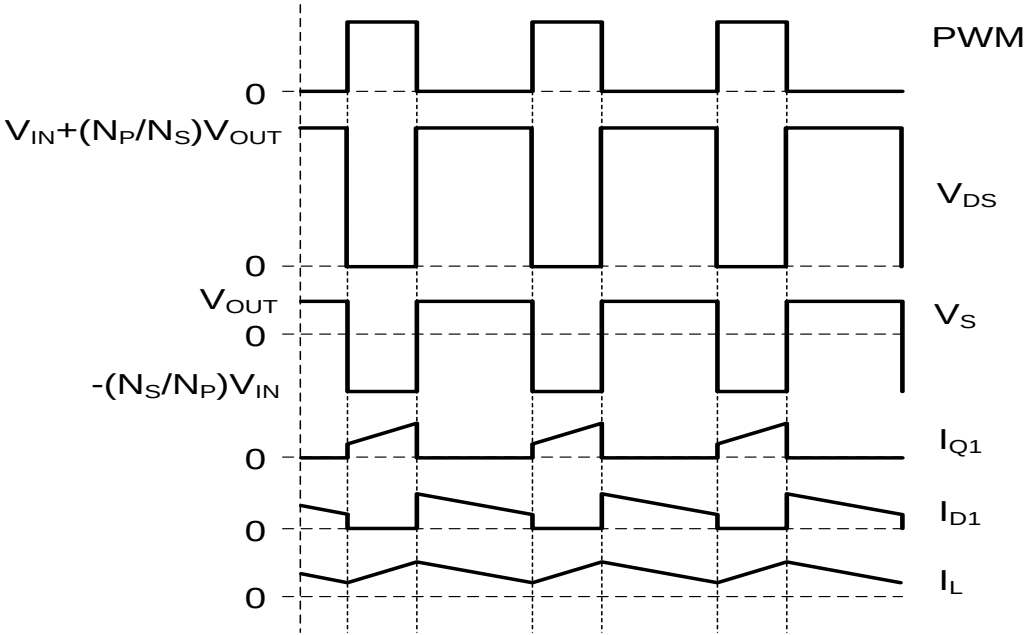


(a) Flyback Converter

- CCM Transfer Function

$$\frac{V_O}{V_{IN}} = \frac{N_S}{N_P} \times \frac{D}{1-D}$$

- Limitations
  - Q1 switching loss (hard switched)
  - D2 reverse recovery loss
  - Q1(V_{DS})>V_{IN}
  - 50% duty cycle limit
  - Right half plane zero in CCM

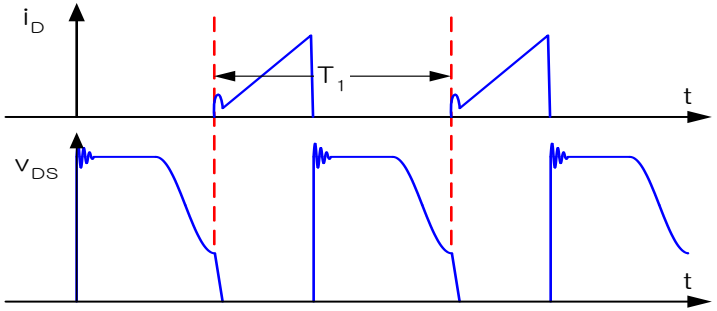


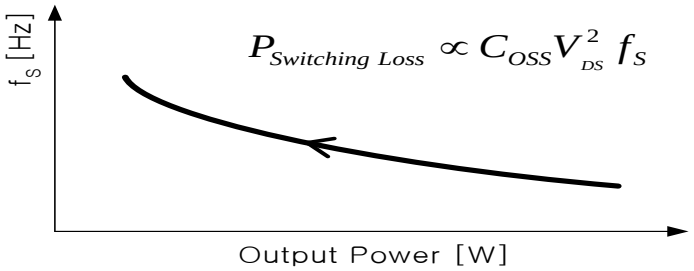
(b) CCM Waveforms

Quasi-Resonant Flyback

Conventional Valley Switching

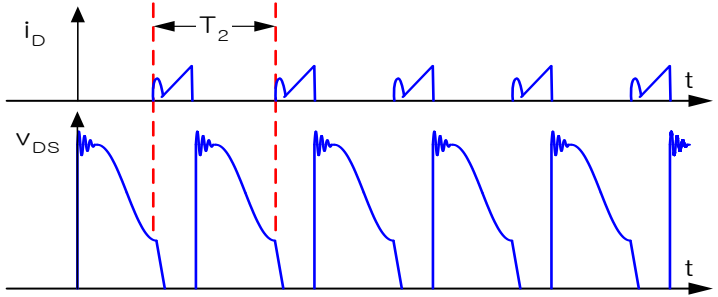
Wide frequency variation depends on output load condition





Output load decreases

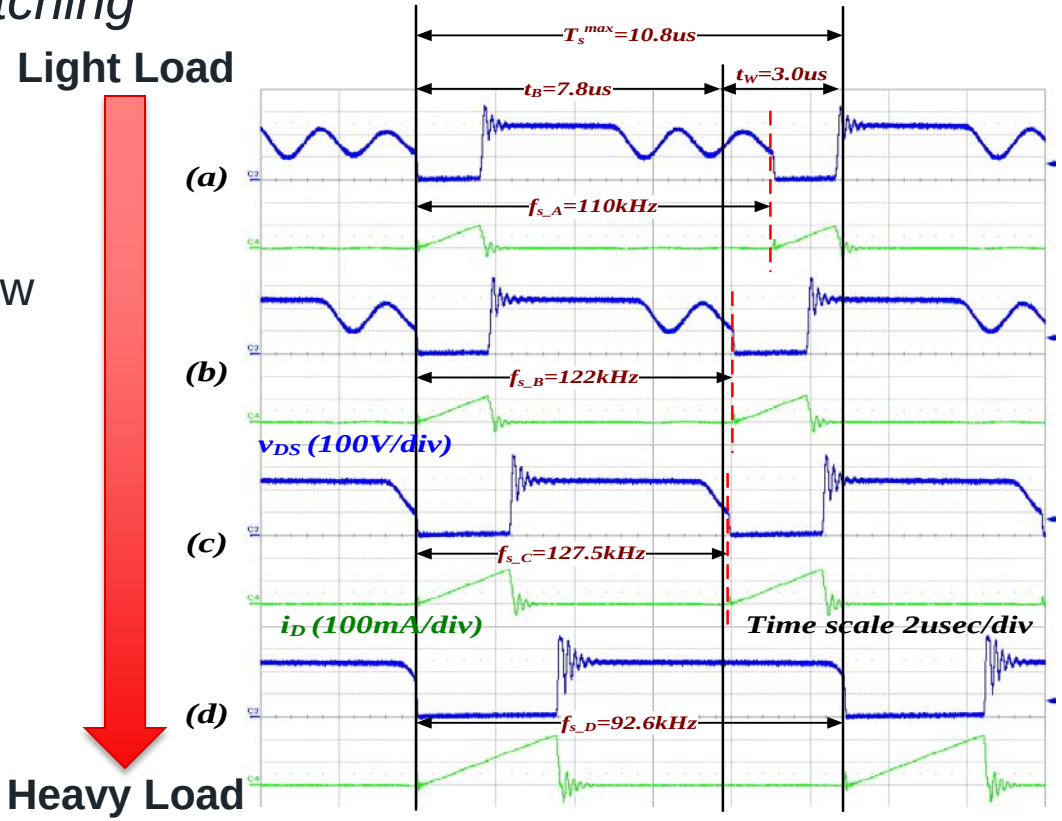
Operating frequency increases



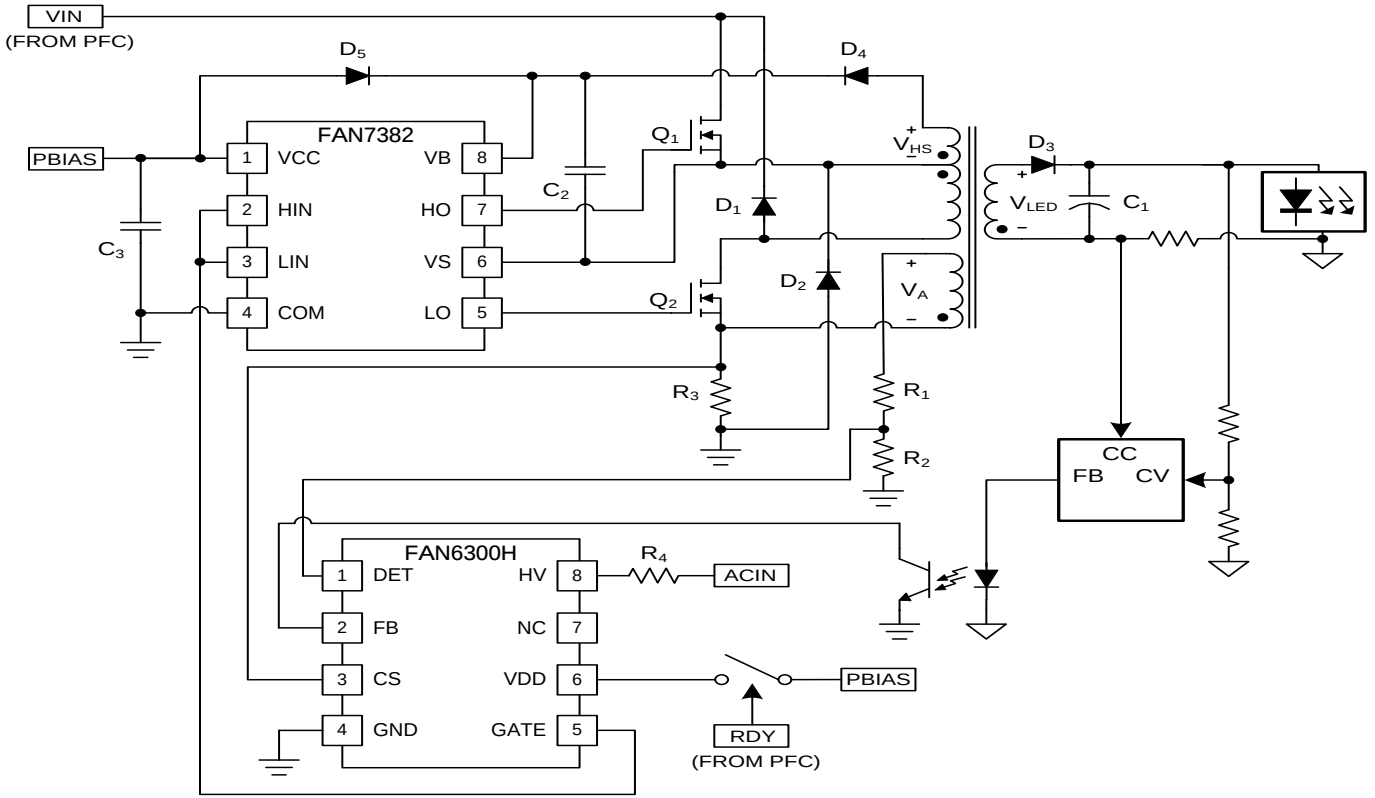
Quasi-Resonant Flyback

Window Valley Switching

- Frequency variation depends on output load conditions
- Operating frequency is within narrow variation (127.5 kHz ~ 92.6 kHz)

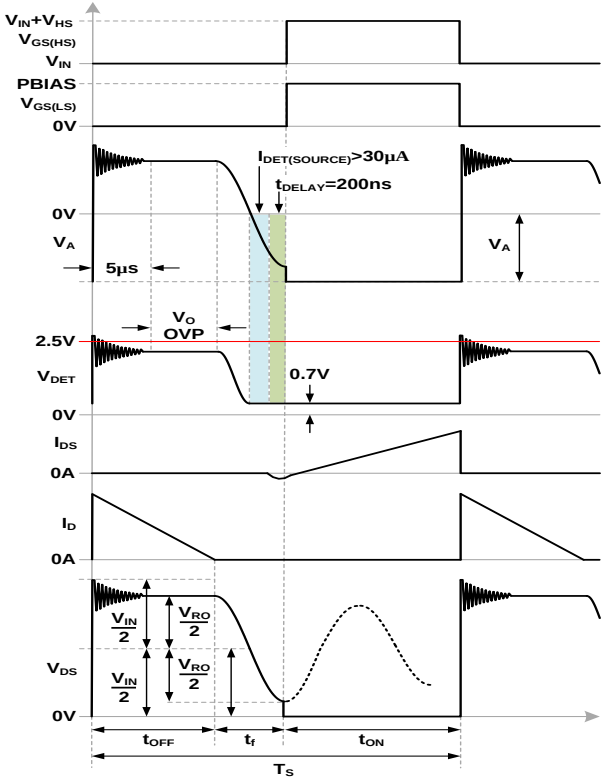


Two-Switch, Quasi-Resonant Flyback



Two-Switch, Quasi-Resonant Flyback

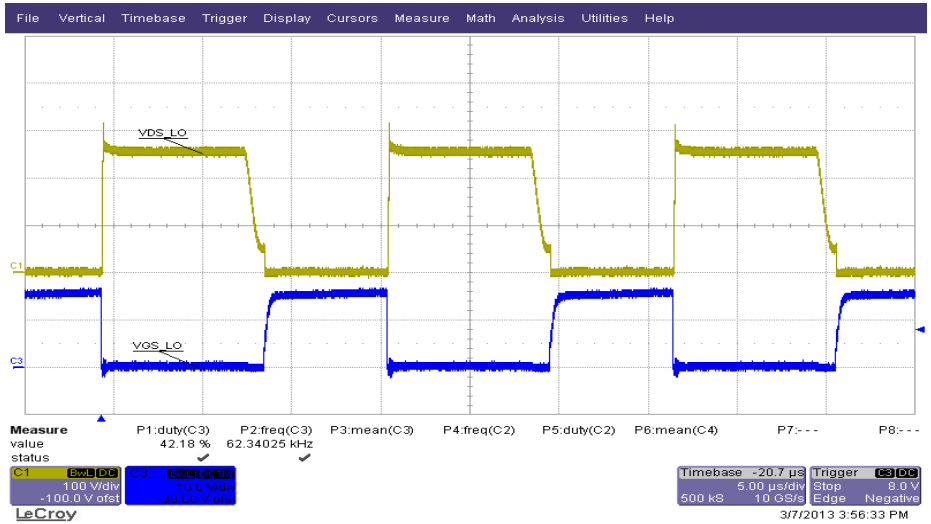
Switching Waveforms

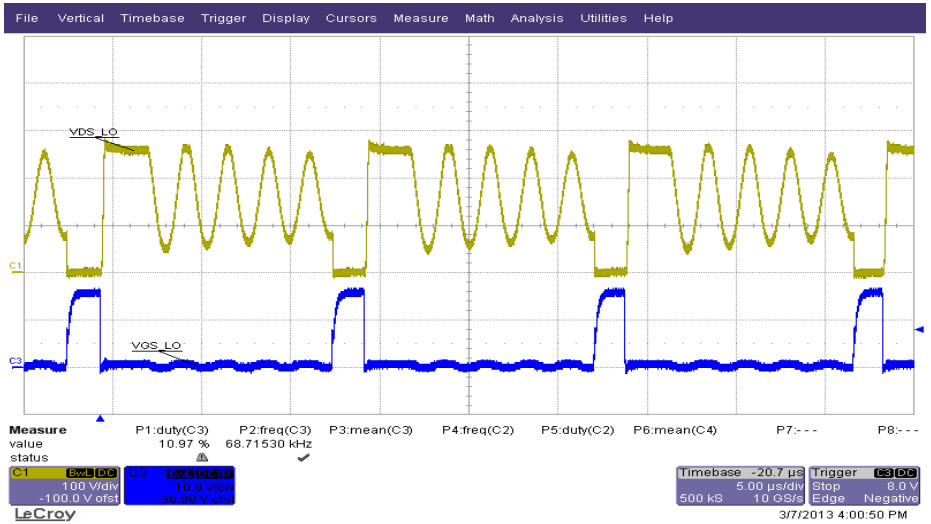


- Quasi-resonant, variable frequency
- HS and LS MOSFETs switch synchronously
- Switching period, $T_S=t_{OFF}+t_f+t_{ON}$
- Inductor current switches from 0A (ZCS) every switching cycle
- VDS
  - ZVS→$V_{OUT}>2\times V_{IN}$
  - Valley switching→otherwise
  - Window valley switching

Two-Switch, Quasi-Resonant Flyback

Measured Waveforms

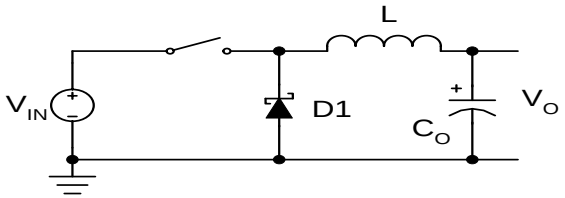




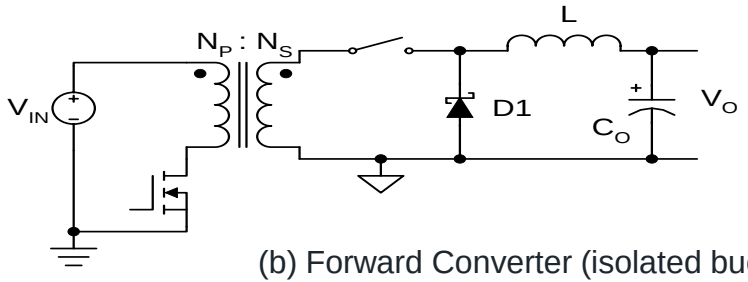
- V_{DS} Valley Switching on First Valley
  - V_{OUT}< ½ V_{IN}
  - D=42%
  - F_S=63kHz
  - P_{OUT}=85W

- Extended Window Valley Switching
  - V_{OUT}< ½ V_{IN}
  - D=11%
  - F_S=68kHz
  - P_{OUT}=24W

Buck Derived Transfer Functions

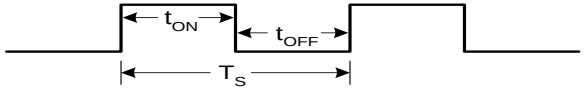


(a) Buck Converter



(b) Forward Converter (isolated buck)

$$\text{Duty Cycle} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{t_{ON}}{T_S}$$



$$(V_{IN} - V_O) \times t_{ON} = V_O \times t_{OFF}$$

$$V_O = D \times V_{IN}$$

Buck Converter Transfer Function

$$\frac{V_O}{V_{IN}} = D$$

Forward Converter Transfer Function

$$\frac{V_O}{V_{IN}} = \frac{N_S}{N_P} \times D$$

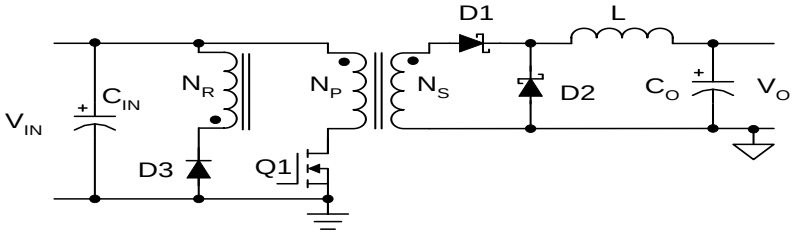
All Isolated Single Ended Buck Converters

$$\frac{V_O}{V_{IN}} = \frac{N_S}{N_P} \times D$$

All Isolated Double Ended Buck Converters

$$\frac{V_O}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D$$

Forward Converter Basics

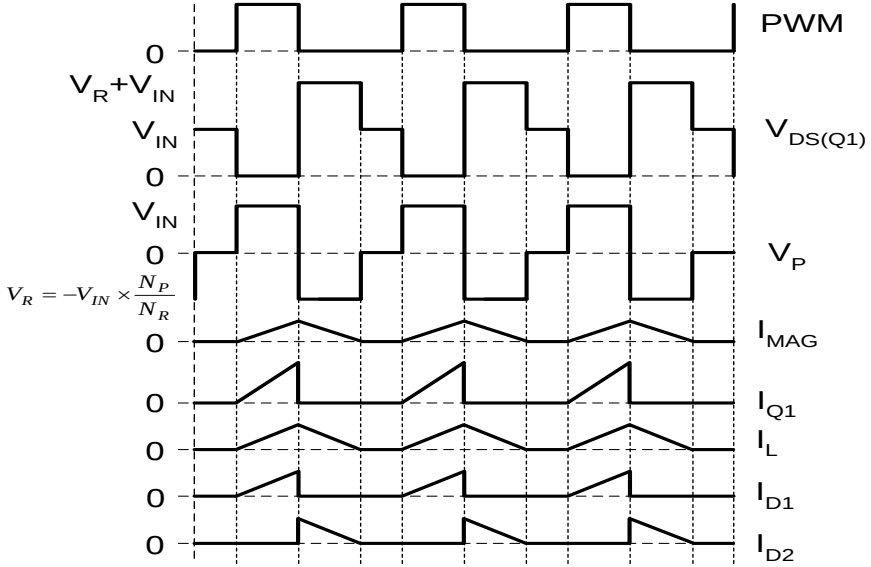


(a) Forward Converter with Reset Winding

- Really a transformer coupled buck
- Transfer function

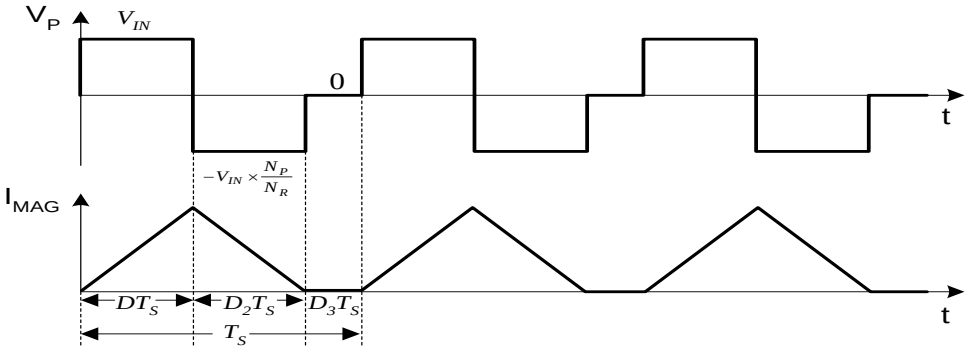
$$\frac{V_O}{V_{IN}} = \frac{N_S}{N_P} \times D$$

- Limitations
  - Q1 switching loss (hard switched)
  - D2 conduction loss
  - Q1(V_{DS})>2V_{IN}
  - 50% duty cycle limit (N_P:N_R = 1:1)



(b) DCM Waveforms (D<0.5)

Why 50% Duty Cycle Limit?



(a) Forward Converter: Transformer Voltage and Current

1. Average primary voltage must be zero over switching period

$$\langle V_p \rangle = D(V_{IN}) + D_2\left(-V_{IN}\frac{N_P}{N_R}\right) + D_3(0) = 0 \quad (1)$$

2. Solve (1) for D2

$$D_2 = D\frac{N_R}{N_P} \quad (2)$$

3. By definition

$$D + D_2 + D_3 = 1 \quad (3)$$

4. Solve (3) for D_3

$$D_3 = 1 - D - D_2 \geq 0 \quad (4)$$

5. Sub (2) into (4)

$$1 - D - D\frac{N_R}{N_P} \geq 0 \quad (5)$$

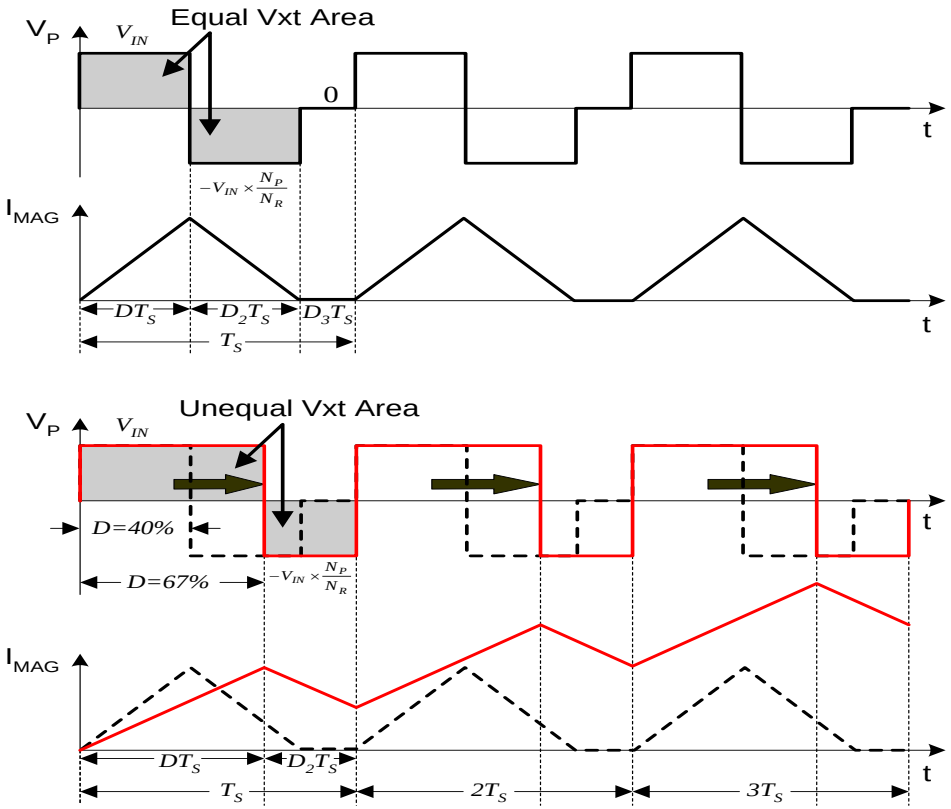
6. Solve (5) for D

$$D \leq \frac{1}{1+\frac{N_R}{N_P}} \quad (6)$$

7. For N_P:N_R=1:1 (common practice)

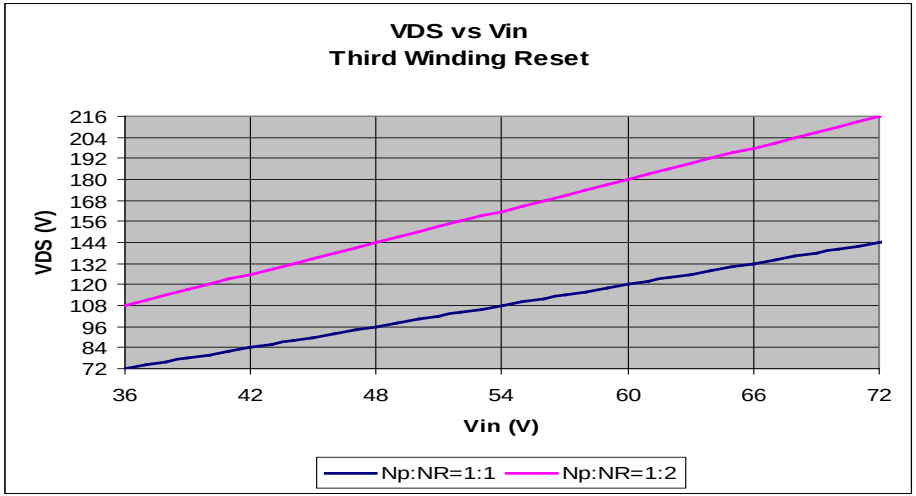
$$D \leq \frac{1}{2} \quad (7)$$

Problems with Duty Cycle > 50%

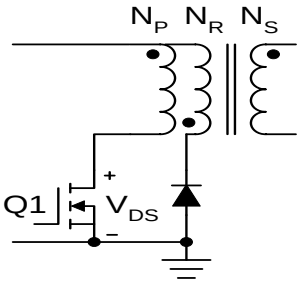


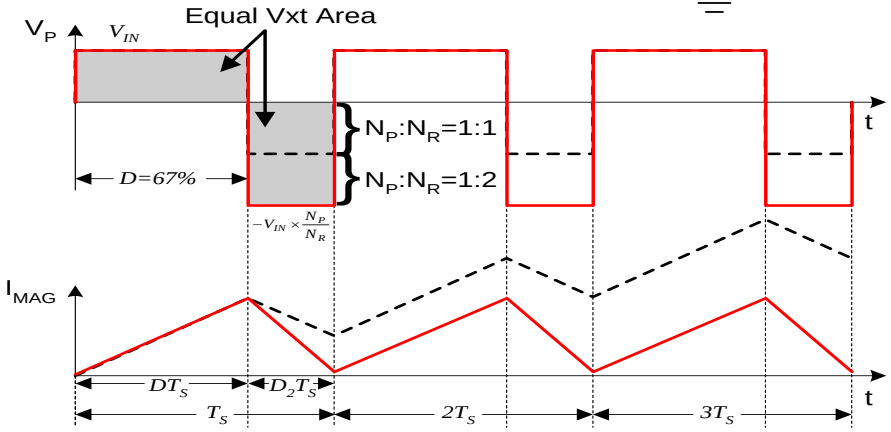
- Common practice is to use 1:1 bifilar transformer winding for N_P:N_R
- D=40%
  - Converter operates in DCM
  - Transformer is completely reset on every switching cycle
- D=67%
  - Converter wants to operate in CCM
  - Transformer can NOT reset on every switching cycle
  - I_{MAG} increases due to volt second product imbalance
  - Transformer saturation will result
  - Operation beyond D=50% requires additional reset voltage

Duty Cycle Greater Than 50%



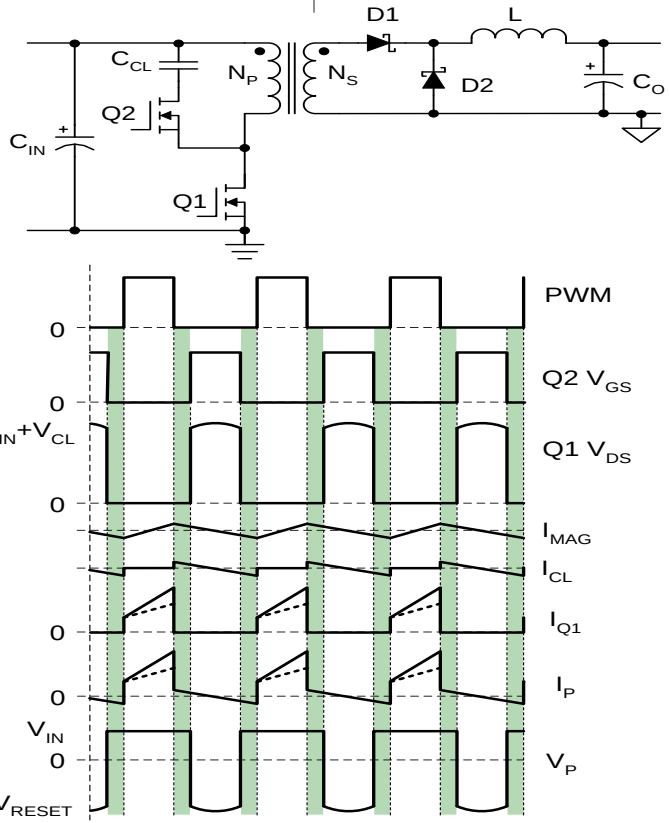
- For N_P:N_R=1:2
  $V_{DS}=3V_{IN}$





Conclusion: Reset winding technique, D>50% not practical for high V_{IN} applications due to additional MOSFET V_{DS} stress

Active Clamp Forward Converter

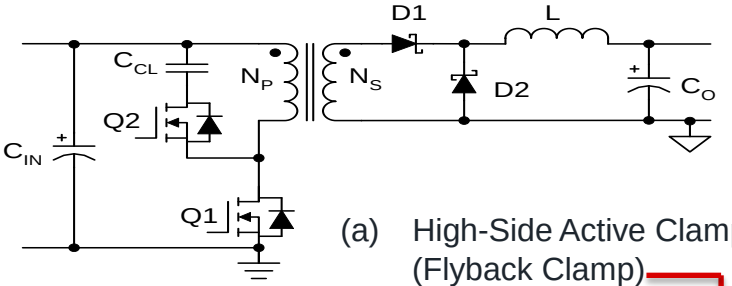


- Advantages
  - Reduced MOSFET V_{DS} voltage stress
  - Higher efficiency through ZVS
  - Use of parasitic elements
  - Higher frequency operation
  - Square wave transformer reset for SR applications
  - Suitable for off-line (HS clamp) or DC/DC (LS clamp)
- Disadvantages
  - Conditional ZVS only
  - Dual primary side gate drive with accurate dead-time control and max duty cycle clamp required
  - Poor transient response due to C_{CL}
- Transfer Function

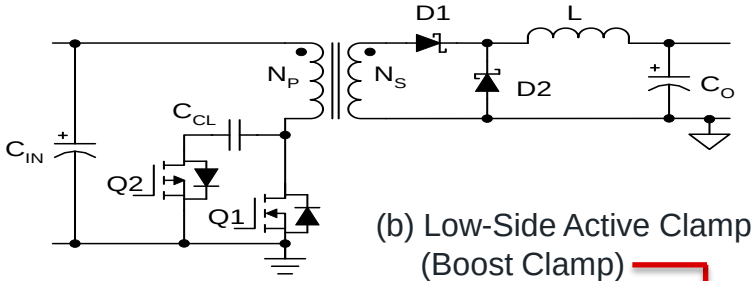
$$\frac{V_O}{V_{IN}} = \frac{N_S}{N_P} \times D$$

Active Clamp Forward Converter

Two Versions



(a) High-Side Active Clamp (Flyback Clamp)

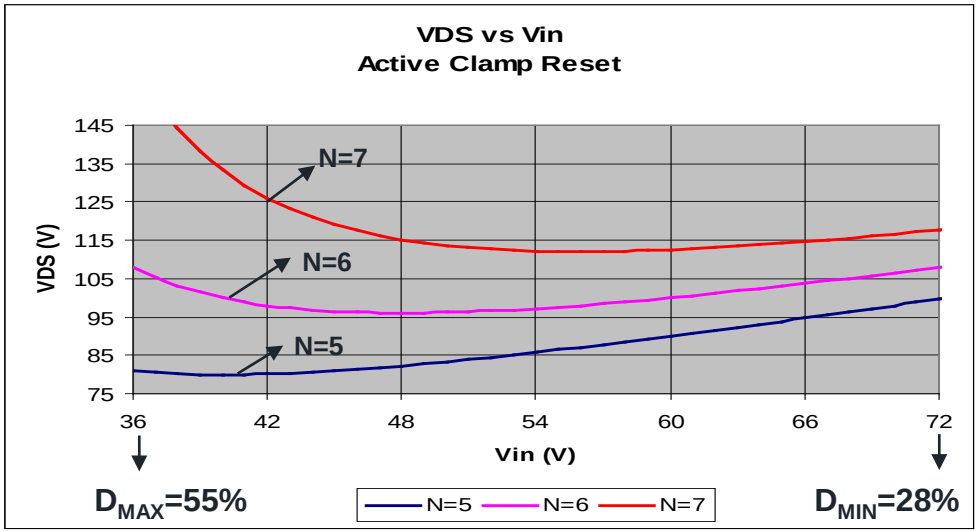


(b) Low-Side Active Clamp (Boost Clamp)

PARAMETER	HIGH-SIDE ACTIVE CLAMP (off-line)	LOW-SIDE ACTIVE CLAMP (telecom)
V_{DS}	$\left(\frac{1}{1-D}\right)\times V_{IN}$	$\left(\frac{1}{1-D}\right)\times V_{IN}$
V_{RESET}	$\left(\frac{D}{1-D}\right)\times V_{IN}$	$\left(\frac{D}{1-D}\right)\times V_{IN}$
V_{CL}	$\left(\frac{D}{1-D}\right)\times V_{IN}$	$\left(\frac{1}{1-D}\right)\times V_{IN}$
C_{CL} (applied voltage)	Lower voltage by V_{IN} volts Highest V_{CL} occurs at D_{MAX}	Higher voltage by V_{IN} volts Not practical for off-line
C_{CL} (cap value)	Same value as low-side for given ripple voltage	Same value as high-side for given ripple voltage
Clamp MOSFET (Q2)	N-Channel Can be used for >500V	P-Channel Can be used up to 500V
Gate Drive	Gate drive transformer required	Level shifting gate drive required

Active Clamp Forward Converter

V_{DS} Voltage Stress



$$V_{DS} = V_{IN} \times \frac{1}{1-D} = \frac{{V_{IN}}^2}{V_{IN} - N \times V_{SEC}} \quad , \quad where \; N = \frac{N_P}{N_S}$$

$$D = \frac{V_O \times N}{V_{IN}}$$

Telecom Converter Example

$$36V \le V_{IN} \le 72V$$

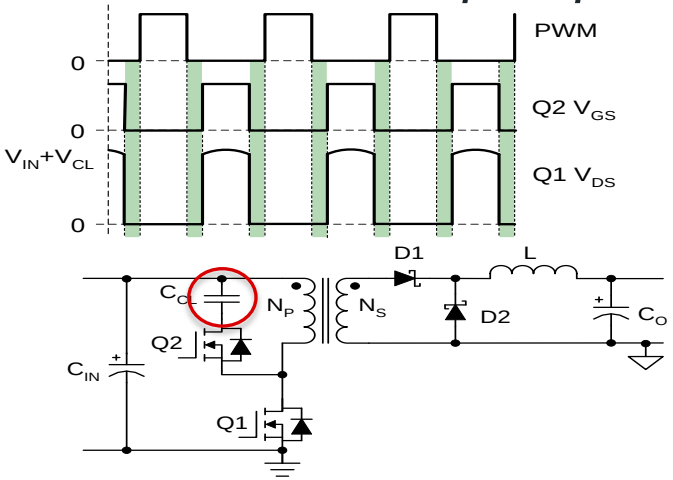
$$V_O = 3.3V$$

- Optimize transformer turns ratio, N, to minimize V_{DS} voltage stress over entire V_{IN} range
- For N=6
  - V_{DS}=108V at $V_{IN(MIN)}$ and $V_{IN(MAX)}$
  - $V_{DS} \le 1.5V_{IN}$ at $V_{IN(MAX)}$

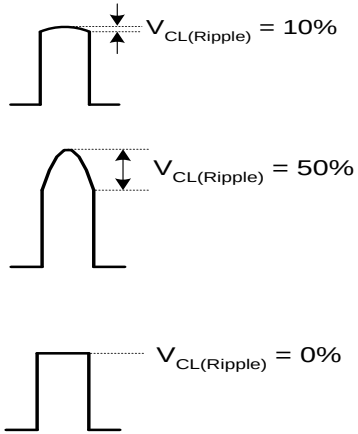
- **IMPORTANT** – Accurate max duty cycle clamp or volt-second clamp is necessary due to the parabolic nature of V_{DS} near D_{MAX}

Active Clamp Forward Converter

Clamp Capacitor



Q1 V_{DS} Waveforms verses Clamp Capacitor Value:



- Clamp capacitor optimal
  - $V_{CL(RIPPLE)}$ = 10%-20%
- Clamp capacitor too small
  - $V_{CL(RIPPLE)}$ = 50%
  - Better transient response
  - Increase V_{DS} stress
- Clamp capacitor too large
  - $V_{CL(RIPPLE)}$ = 0%
  - Lowest V_{DS} stress
  - Poor transient response

- Choosing Clamp Capacitor
  - Capacitor needs to be large enough to approximate the clamp voltage as DC
  - Initially calculate C_{CL} according to “Rule of Thumb”

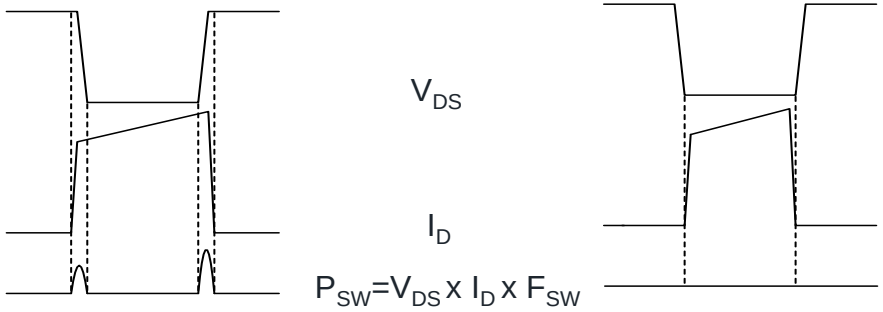
$$2\pi \times \sqrt{L_{MAG} \times C_{CL}} > t_{off\,(MAX)} \longrightarrow C_{CL} > 10 \times \frac{(1 - D_{MIN})^2}{L_{MAG} \times (2\pi \times F_{sw})^2}$$

  - Select C_{CL} voltage rating according to maximum clamp voltage *PLUS* allowable ripple voltage and safety margin

Active Clamp Forward Converter

Zero Voltage Switching (ZVS)

- ZVS occurs when the voltage across the MOSFET, V_{DS}, is positioned to “zero volts” prior to the start of the next switching cycle.
- Benefits of ZVS
  - Reduced switching losses
  - Higher operating frequency possible (smaller passive component size)
  - Higher converter efficiency
  - Increased reliability
  - Reduced radiated emissions (EMI)

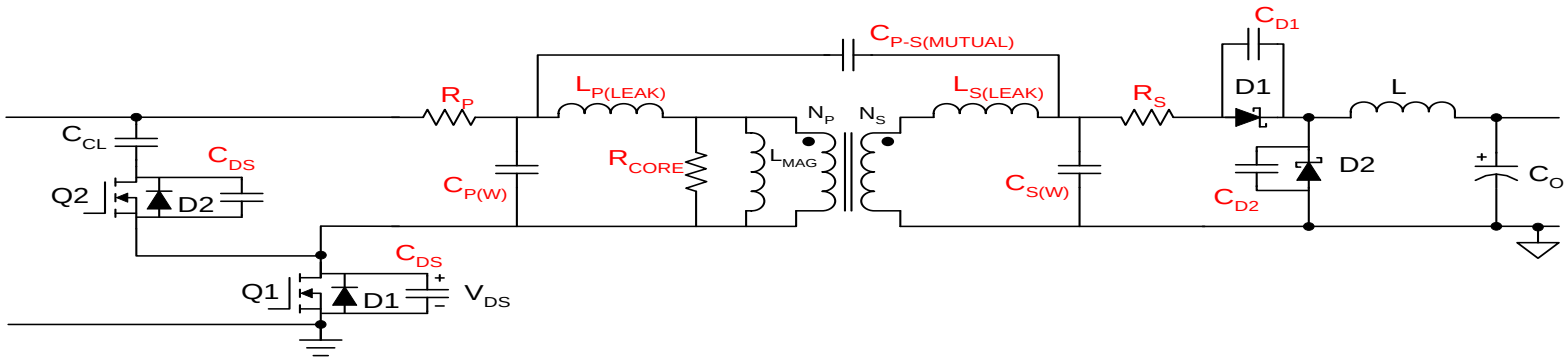


(a) Hard Switching (b) “Ideal” ZVS

Active Clamp Forward Converter

Zero Voltage Switching (ZVS)

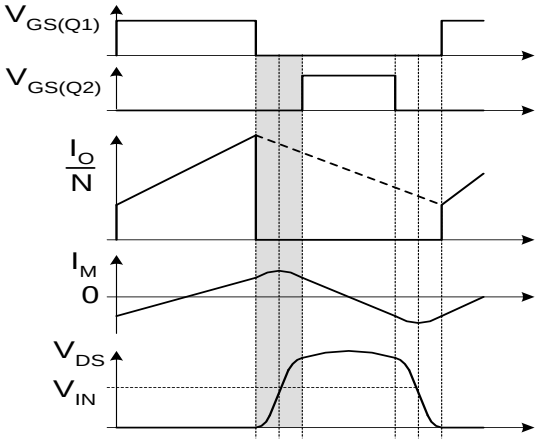
- Parasitic elements can be used to benefit ZVS



- Active Clamp Forward converter uses fixed frequency resonant transitions to achieve ZVS when specific operating conditions are met

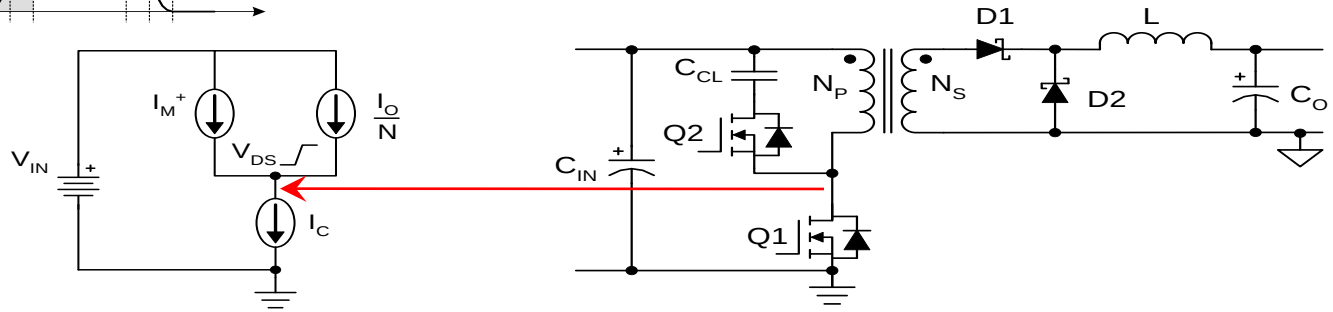
Active Clamp Forward Converter

Zero Voltage Switching, Q1 Turn-Off



- ZVS turn-off is easy
  - Magnetizing current, I_M^+, and reflected secondary current combine to fully charge the resonant capacitance, C

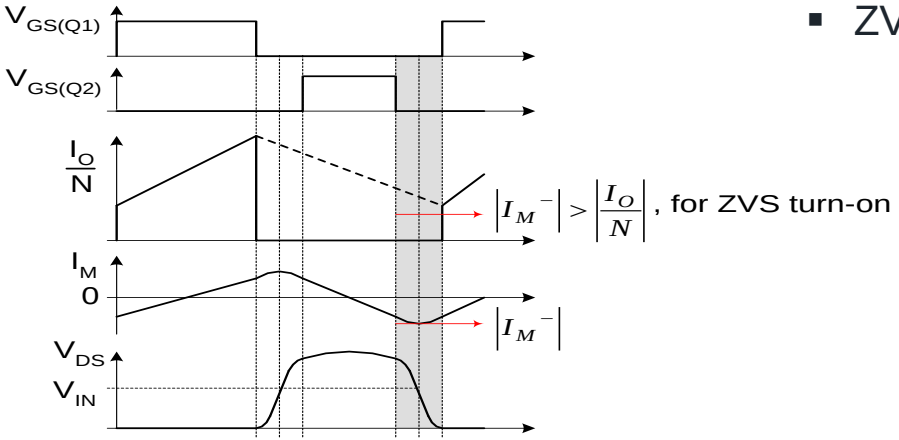
$$\frac{1}{2} L_M \left(\frac{I_O}{N} + I_M{}^+ \right)^2 > \frac{1}{2} C_{DS} (V_{IN} + V_{CL})^2$$

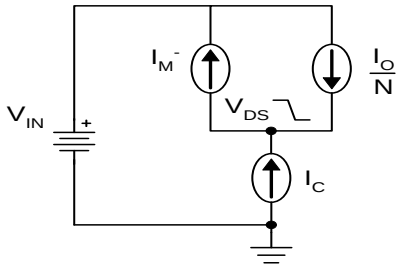


NOTE: leakage inductance is neglected for this analysis

Active Clamp Forward Converter

Zero Voltage Switching, Q1 Turn-On





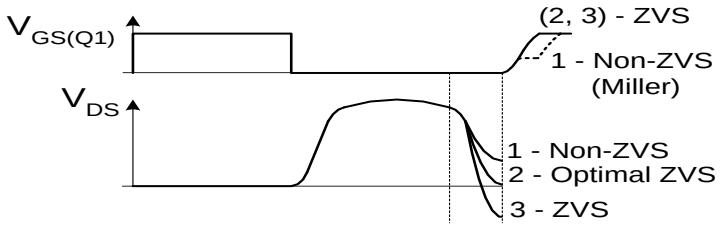
NOTE: leakage inductance is neglected for this analysis

- ZVS turn-on is difficult
  - Magnitude of I_M^- must be greater than the magnitude of the reflected secondary current during entire ZVS window

$$|I_M^-| > \left|\frac{I_O}{N}\right|$$

  - Must be enough resonant current to fully discharge C

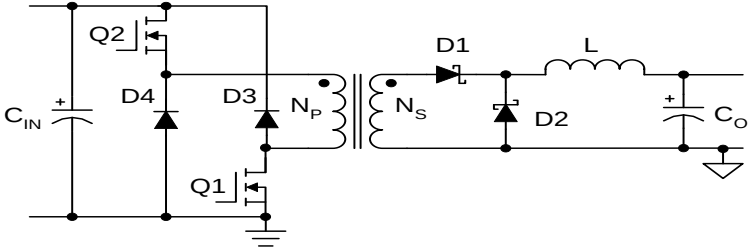
$$\frac{1}{2} L_M \left(\frac{I_O}{N} - I_M^-\right)^2 > \frac{1}{2} C_{DS} (V_{IN} + V_{CL})^2$$

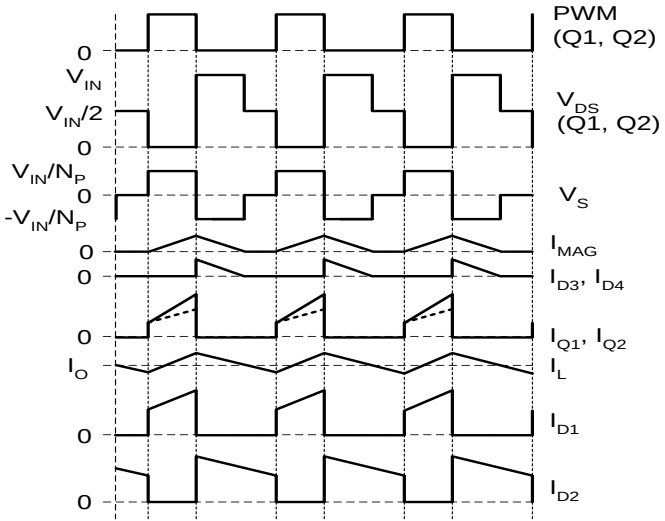


  - Must be enough dead time for the drain voltage to fully resonate to near zero volts $t_{RES} \geq \frac{\pi}{2}\sqrt{L_M \times C_{DS}}$

Single Ended (<500W)

2 Switch Forward Converter





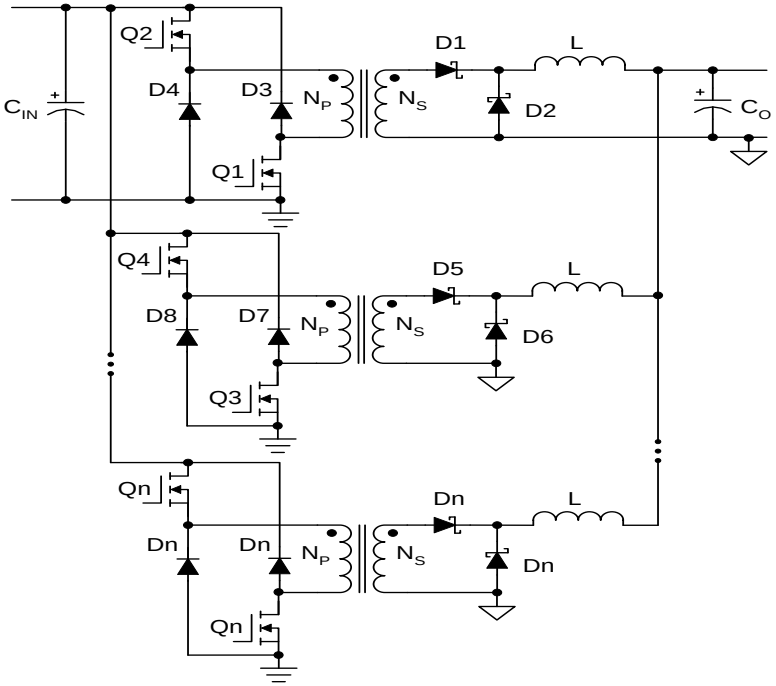
- Advantages
  - Ruggedness
  - MOSFET voltage stress limited to V_{IN}
  - Magnetizing energy recycled by D3, D4
  - Universal input, 150W<P<500W
- Disadvantages
  - Limited to less than 50% duty cycle
  - High side gate drive required for Q2
  - Hard switching
- Transfer Function

$$\frac{V_O}{V_{IN}} = \frac{N_S}{N_P} \times D$$

Single Ended (>1kW)

Interleaved 2 Switch Forward Converter

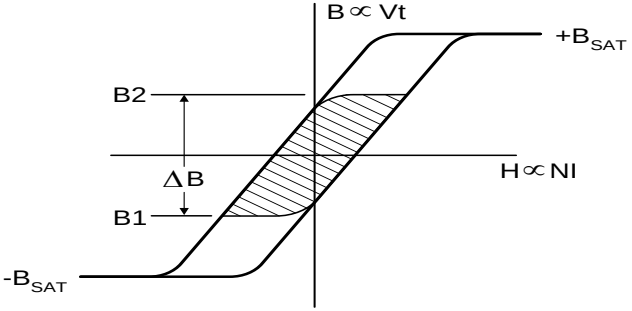
- Advantages
  - Can operate multiple power stages out of phase
  - Ripple current cancellation at output capacitor
  - Reduced RMS current at input capacitor
  - Multiple stages can add up to kW of power
  - Smaller output inductors can improve transient response
- Disadvantages
  - Design complexity
  - PCB layout can be challenging



- Non-Isolated Converter Topologies
- Single Ended Converter Topologies
- **Double Ended Converter Topologies**
- Synchronous Rectification

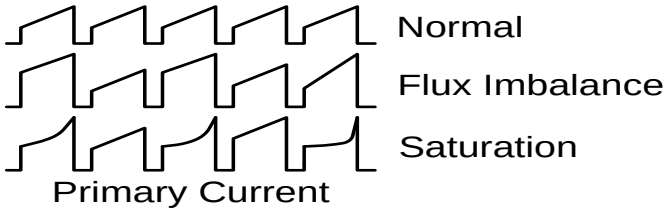
Double Ended Topologies Defined

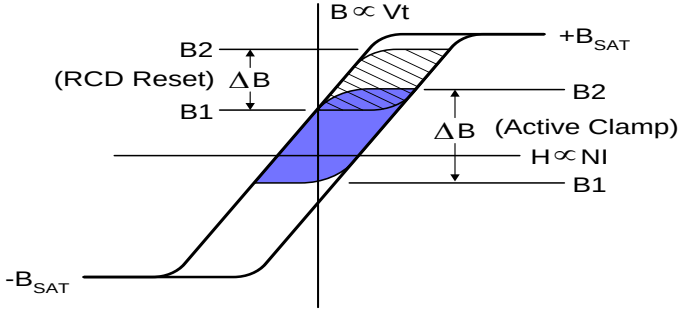
Double Ended – Transformer operation occurs in first and third quadrants



Half-Bridge, Full-Bridge

- Symmetrical operation between first and third quadrants
- No transformer reset circuitry required



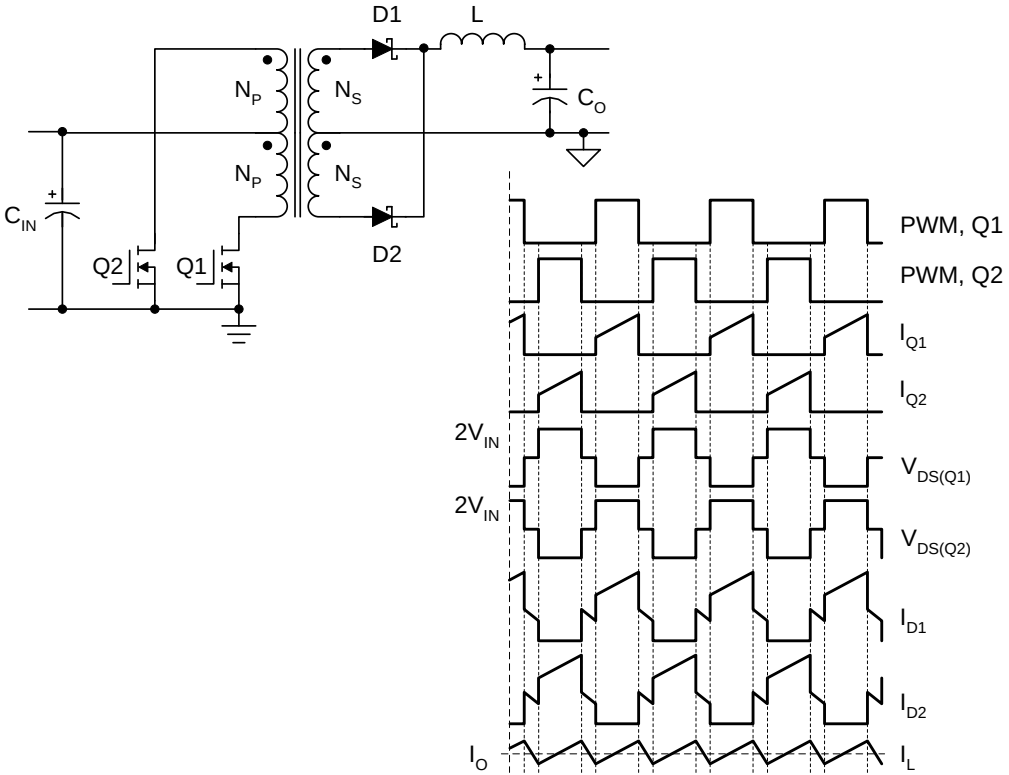


Active Clamp Forward

- "Single ended" *but* operates slightly into the third quadrant

Double Ended (<500W)

Push Pull Converter

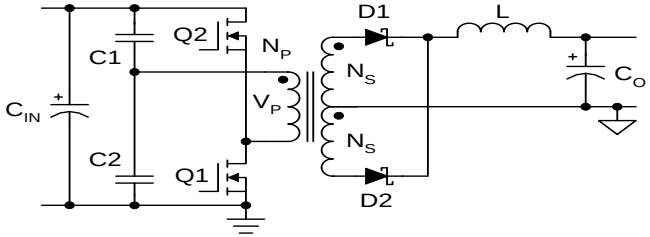


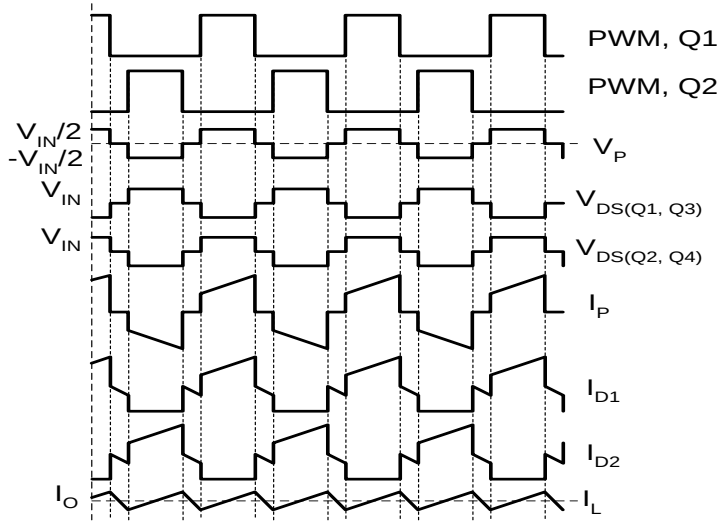
- Advantages
  - Lower primary current compared to HB
  - Best for lower V_{IN}, such as telecom DC/DC of US Line Voltage
  - Simple low-side gate drive
- Disadvantages
  - High voltage ($2xV_{IN}$) on primary MOSFETs
  - Transformer flux walking (VMC only)
  - Center tapped transformer structure
  - Hard switching
- Transfer Function

$$\frac{V_O}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D$$

Double Ended (<500W)

Half Bridge Converter (Symmetrical)

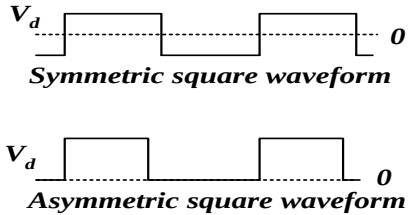


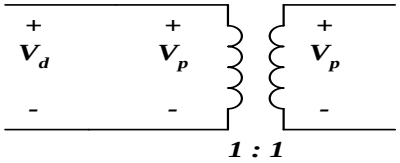


- Advantages
  - Better transformer utilization
  - MOSFET voltage stress limited to V_{IN}
  - Best for high V_{IN} off line applications up to 500W
  - Single winding primary
  - Transformer balanced by C1 and C2
  - Asymmetric and resonant versions can ZVS
- Disadvantages
  - Totem pole primary gate drive
  - High primary current
  - Possible cross conduction between Q1 and Q2
  - Hard switching
- Transfer Function

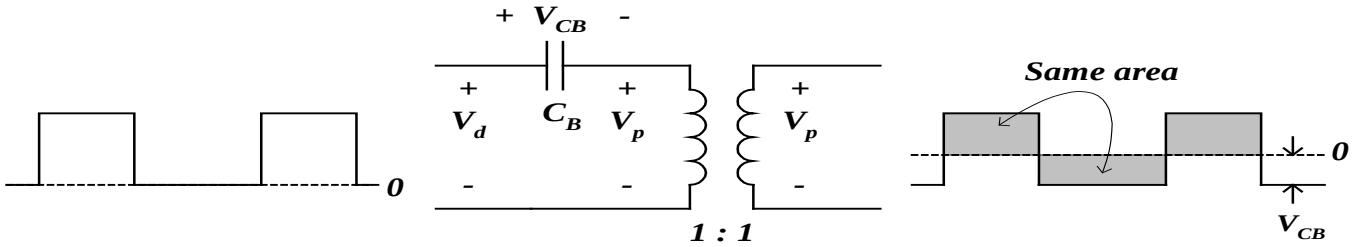
$$\frac{V_O}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D$$

Asymmetrical Half Bridge Converter

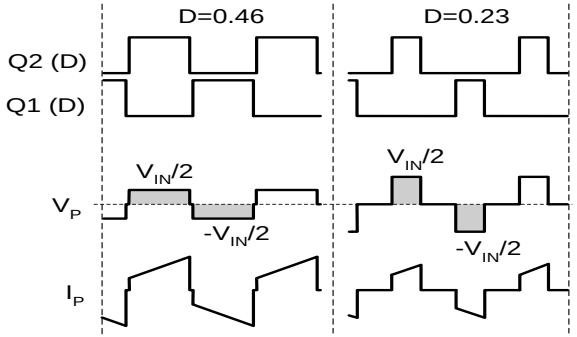




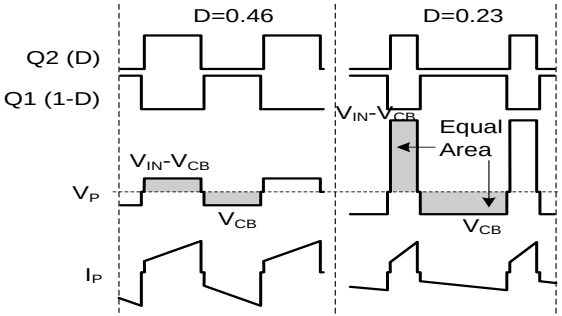
- What if an asymmetric square wave were introduced to the transformer?
  - → Transformer will be saturated
- What if an asymmetric square wave were introduced to the transformer in series with a DC blocking capacitor?
  - → Not saturated due to the voltage of the blocking capacitor, C_B



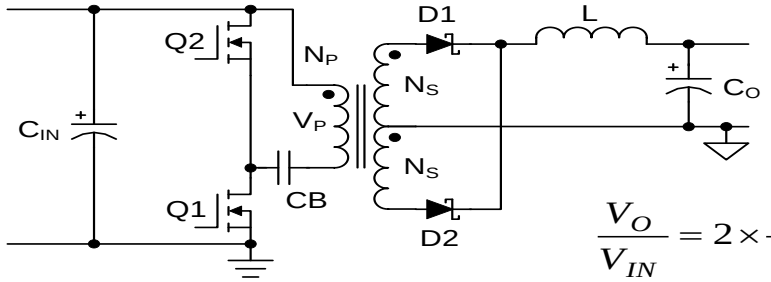
Asymmetrical Half Bridge Converter



(a) Symmetrical HB waveforms



(b) Asymmetrical HB waveforms



$$\frac{V_O}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D \times (1 - D)$$

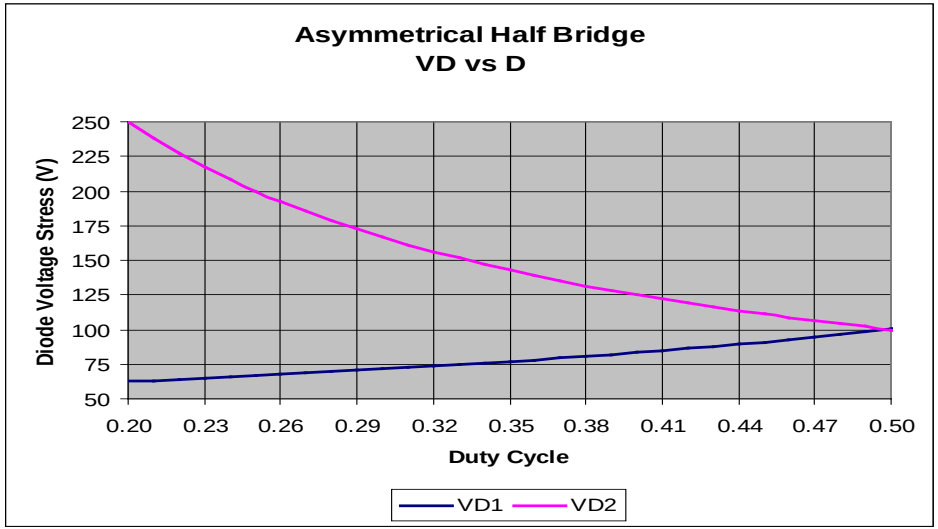
- Asymmetrical Gate Drive
  - Q2 modulated by D
  - Q1 driven by 1-D
  - Fixed dead time between Q1 and Q2
  - Dead time optimized for ZVS and anti cross conduction
  - Fixed frequency ZVS PWM operation
  - Near D=0.5, operation is same as symmetrical HB
- BUT, excessive voltage stress is applied to secondary rectifier at $V_{IN(MAX)}$

Asymmetrical Half Bridge Converter

- Secondary Rectifier Voltage Stress

$$V_{D1} = \frac{V_O}{1-D} \qquad V_{D2} = D \times V_O$$

- Reverse recovery and parasitic ringing
- Wide DD Range requires use of high voltage rectifiers
- Converter operates best at D=0.5



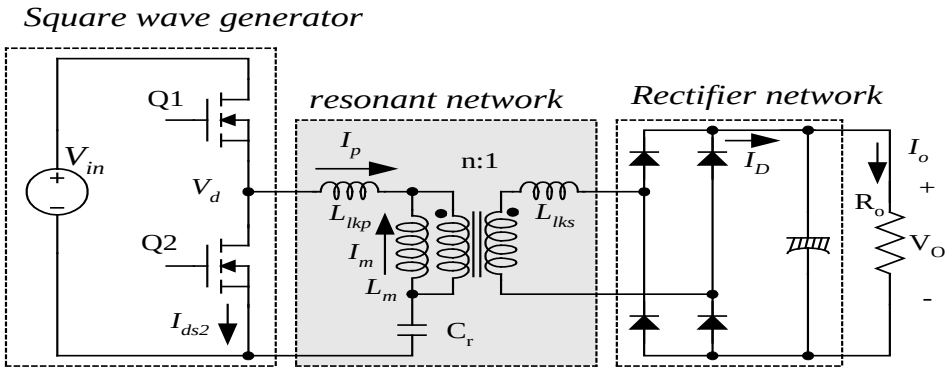
Asymmetrical Half Bridge Converter

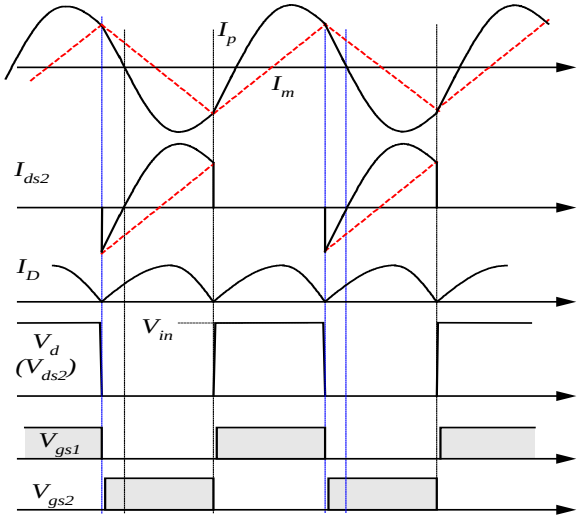
- Advantages
  - Fixed frequency ZVS
  - Constant power transfer (D and 1-D) reduces output ripple
  - Power stage can be controlled using any active clamp PWM controller

- Disadvantages
  - High voltage stress on secondary rectifier
  - Loss of ZVS at some min load current – extending ZVS range is difficult
  - Poor transient response due to blocking capacitor, C_B

LLC Resonant Half Bridge Converter

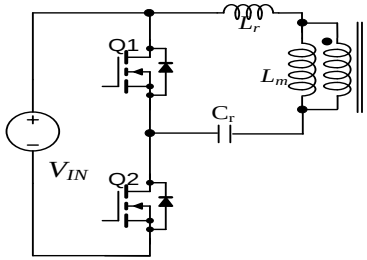
- Square wave generator: produces a square wave voltage, V_d by driving switches, Q1 and Q2 with alternating 50% duty cycle for each switch.
- Resonant network: consists of L_{lkp}, L_{lks}, L_m and C_r. The current lags the voltage applied to the resonant network which allows the MOSFET's to be turned on with zero voltage.
- Rectifier network: produces DC voltage by rectifying AC current



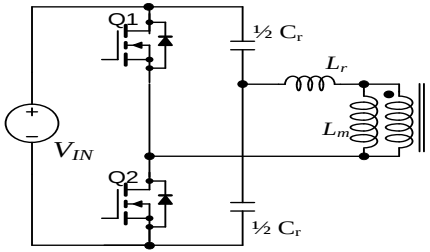


LLC Topology Variations

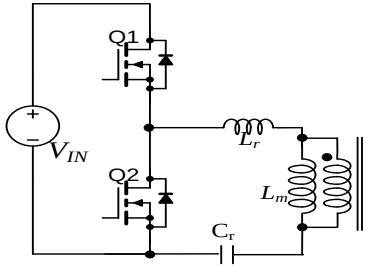
Primary Side Variation



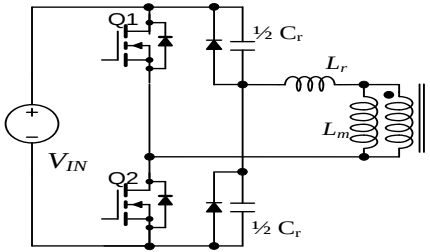
Transformer across the high side MOSFET



Split resonant capacitor

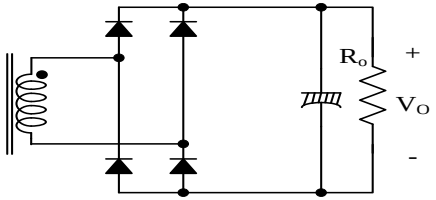


Transformer across the low side MOSFET

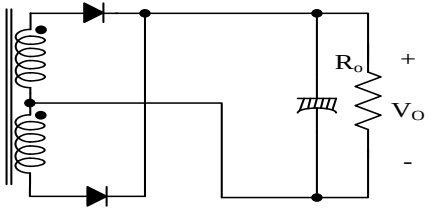


Split resonant capacitor with clamping diode

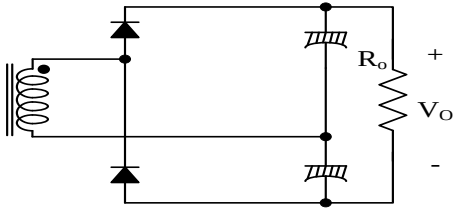
Secondary Side Variation



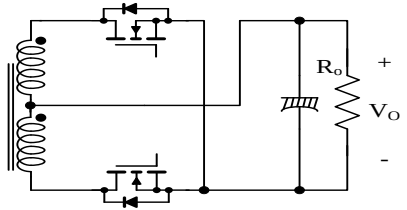
Full bridge rectifier with single winding



2 Rectifier diode with center tab winding



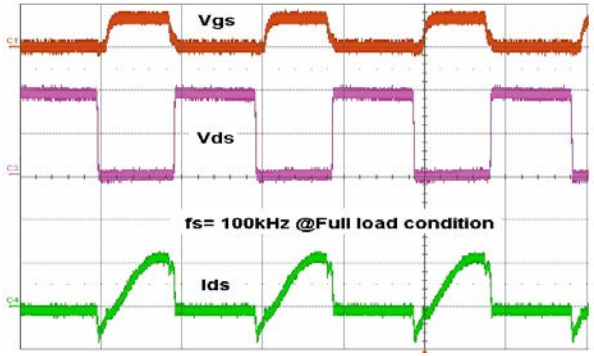
Voltage doubler rectifier with single winding

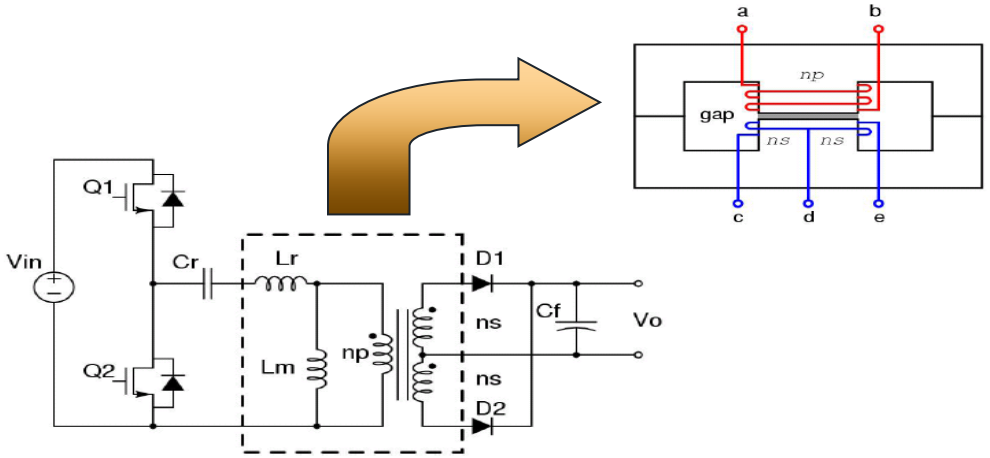


Synchronous rectifier with center tab winding

LLC Resonant Half Bridge Converter

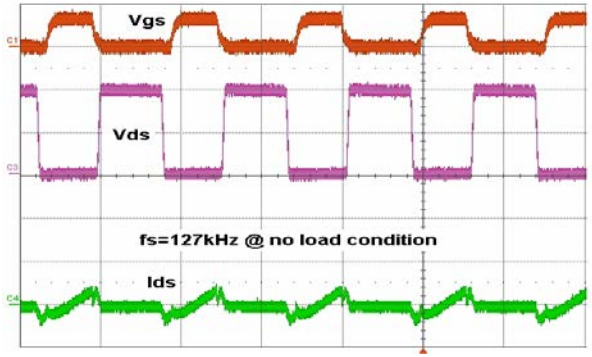
- Advantages of the LLC resonant converter
  - Narrow frequency variation range over wide load range
  - Zero voltage switching even at no load condition
  - Reduced switching loss through ZVS → Improved efficiency and EMI
  - When the two magnetic components are implemented with a single core (use the leakage inductance as the resonant inductor), one component can be saved

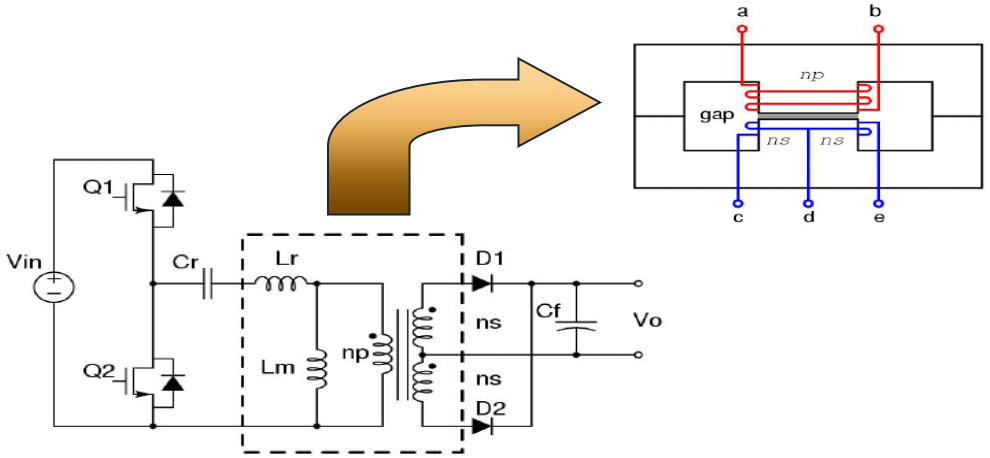




LLC Resonant Half Bridge Converter

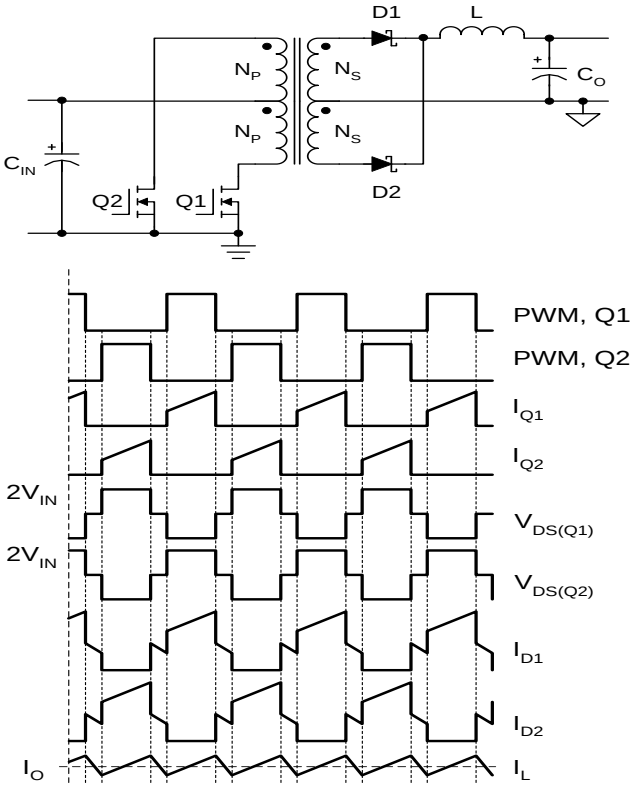
- Disadvantages of the LLC resonant converter
  - Can optimize performance at one operating point, but not with wide range of input voltage and load variations (too wide frequency range)
  - Difficult to regulate the output at no load condition
  - Significant current may circulate through the resonant network, even at the no load condition
  - Quasi-sinusoidal waveforms exhibit higher peak values than equivalent rectangular waveforms
  - High output current ripple





Double Ended (<500W)

Push Pull Converter

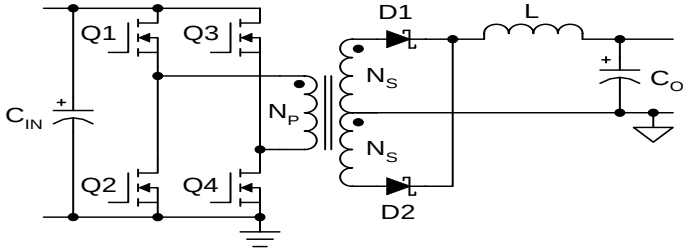


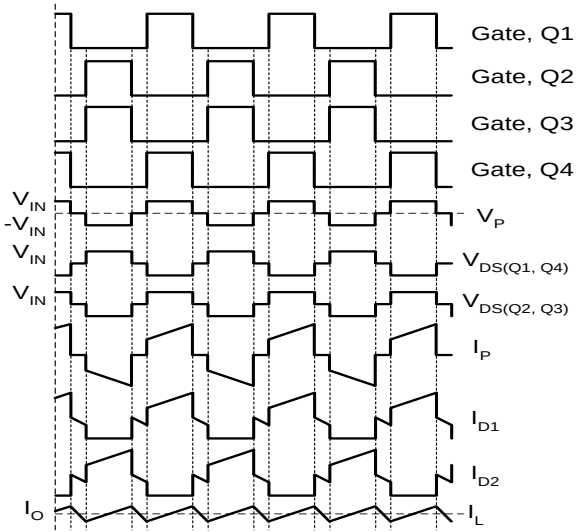
- Advantages
  - Lower primary current compared to HB
  - Best for lower V_{IN}, such as telecom DC/DC of US Line Voltage
  - Simple low-side gate drive
- Disadvantages
  - High voltage ($2xV_{IN}$) on primary MOSFETs
  - Transformer flux walking (VMC only)
  - Center tapped transformer structure
  - Hard switching
- Transfer Function

$$\frac{V_O}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D$$

Double Ended (>500W)

Full Bridge Converter (PWM)



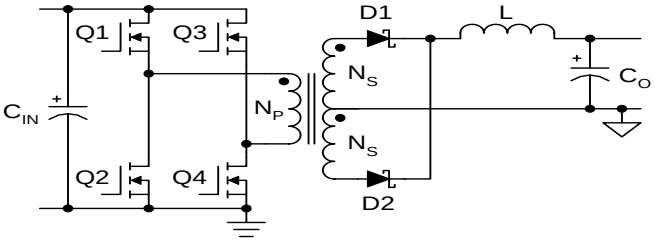


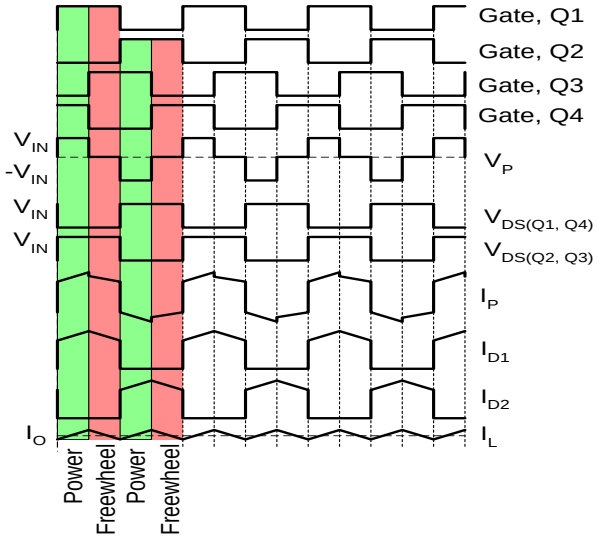
- Advantages
  - MOSFET voltage stress limited to V_{IN}
  - Twice the power compared to half bridge
  - Single winding primary
- Disadvantages
  - Dual, totem pole primary gate drive
  - Hard switching (Non-ZVT)
  - Parasitics degrade circuit performance
  - Circuit complexity
- Transfer Function

$$\frac{V_O}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D$$

Double Ended (>500W)

Phase Shifted Full Bridge Converter

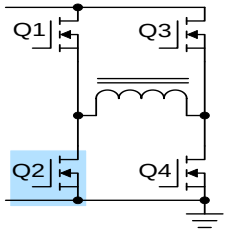




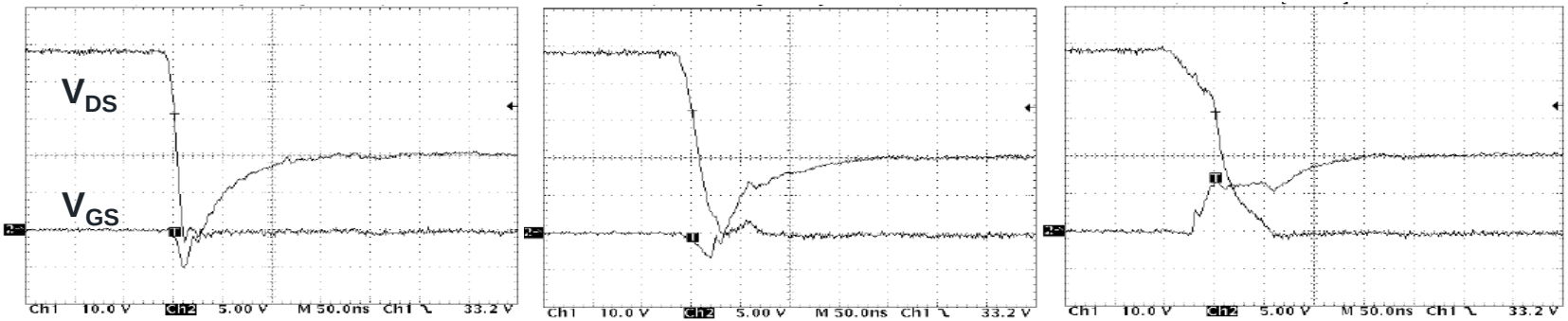
- Advantages
  - High Efficiency ZVS
  - Highest single stage processing power
  - MOSFET voltage stress limited to V_{IN}
  - Twice the power compared to half bridge
  - Full wave rectified secondary
  - Excellent choice for EU line voltage (PFC pre-regulator) with output power >1kW
- Disadvantages
  - Dual, high side primary gate drive
  - Circuit complexity
  - High circulating primary current for ZVS
  - Loss of ZVS at light load current
- Transfer Function $$\frac{V_O}{V_{IN}} = 2 \times \frac{N_S}{N_P} \times D$$

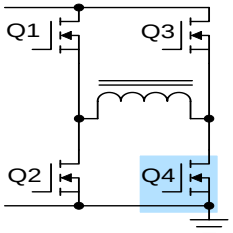
Phase Shifted Full Bridge Converter

ZVS Waveforms

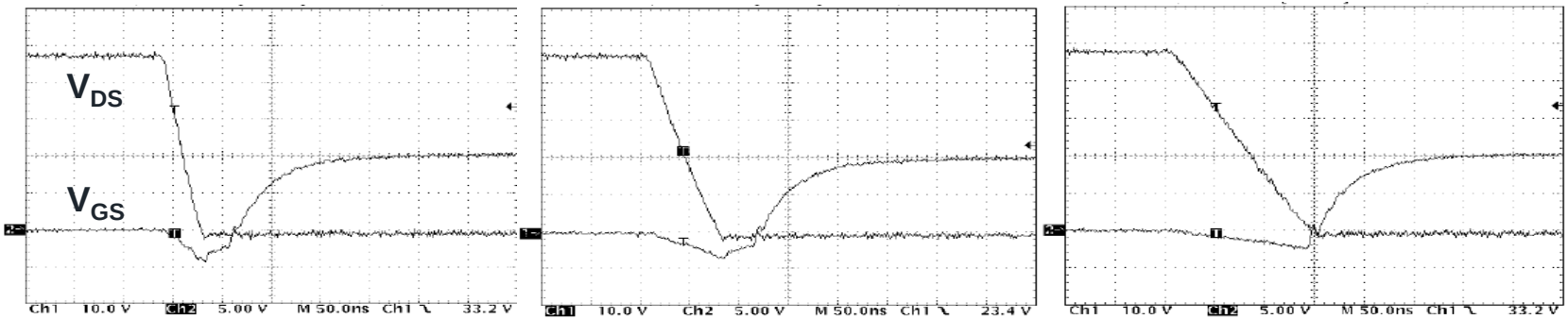


Q2
P→A





Q4
A→P



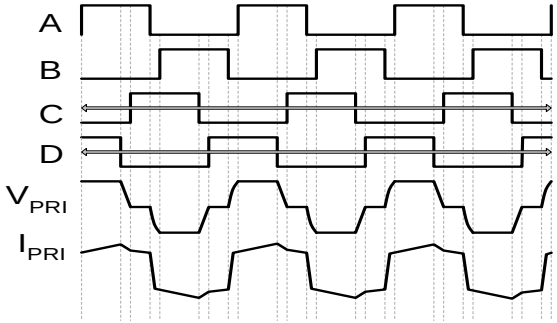
A=Active (Power)
P=Passive (Freewheel)

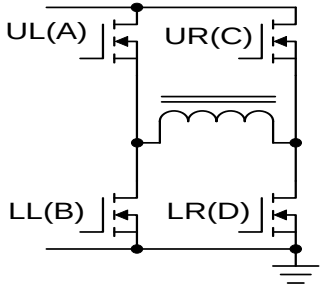
(a) I_O=100%

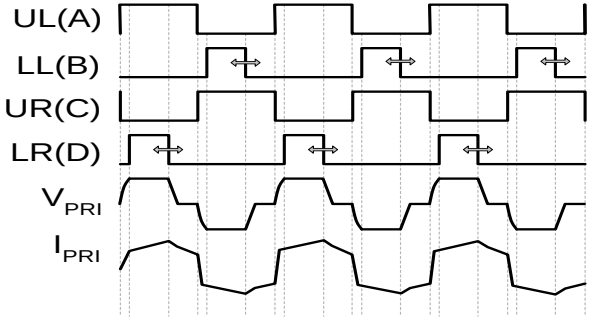
(b) I_O=35%

(c) I_O=0%

Phase Shift Control vs ZVT PWM Control



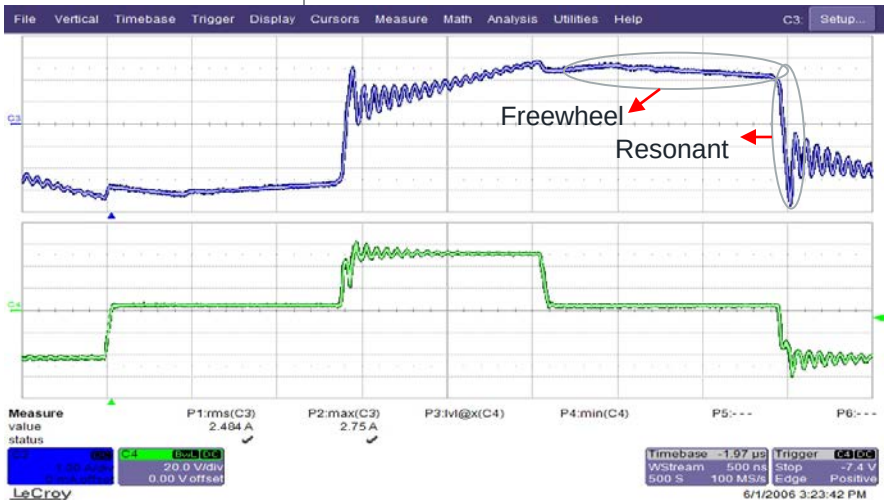


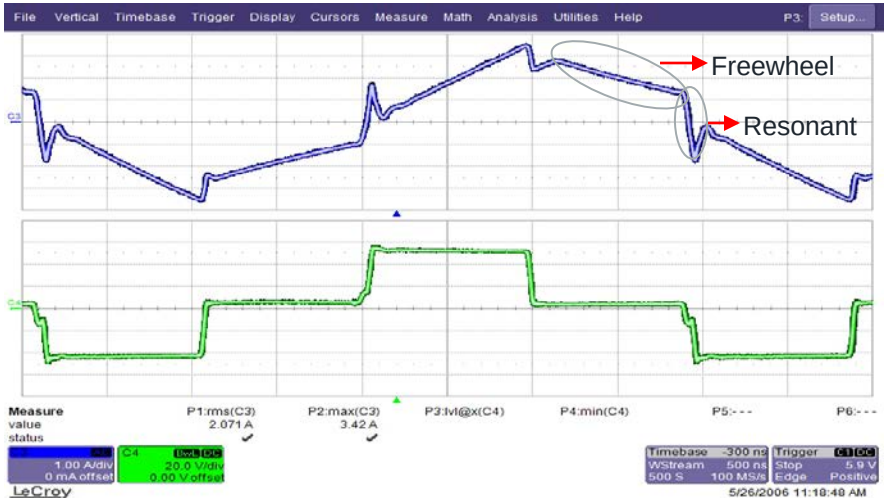


- Phase Shift Control
  - All bridge FETs are fixed at 50% D
  - A and B are synced to clock
  - C and D are phase shift modulated
  - Resonant delay set between AB and CD
- Freewheel period
  - Secondary-side load current freewheels through transformer and is reflected to primary
  - Reflected current aids ZVS
  - Higher conduction losses at higher power

- ZVT PWM Control
  - Upper bridge FETs are fixed at 50% D
  - Lower bridge FETs are trailing edge PWM
  - Resonant delay set on lower FET leading edge
- Freewheel period
  - Both SRs are ON
  - Reduces reflected secondary current since current only flows through both SRs
  - Less available ZVS current

Phase Shift Control vs ZVT PWM Control





- Phase Shift Control
  - Current freewheels through two active high-side FETs for first FW period then through two active low-side FETs for second FW period

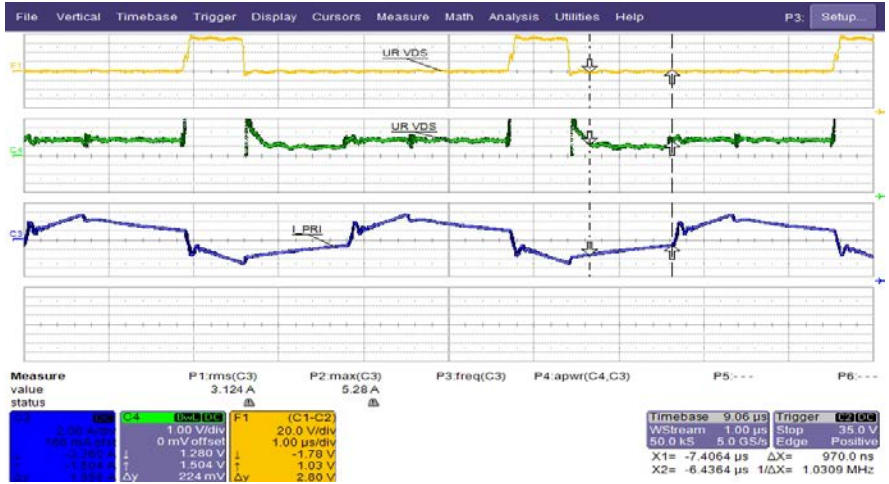
$$P_{DISS} = 2 \times \left(I_{FW}^2 \times R_{DS\_ON} \right)$$

- ZVT PWM Control
  - Current freewheels through one high-side active FET and body-diode of other high-side FET during each FW period

$$P_{DISS} = t_{BD} \times F_{SW} \times V_F \times I_{FW} + \left(I_{FW}^2 \times R_{DS\_ON} \right)$$

ZVT PWM Control

Upper Bridge MOSFET Body-Diode Conduction



- Freewheel (FW) Period
  - For 36V<VIN<72V
  - Body-diode conduction is 970ns at VIN=72V
- Minimize body-diode conduction in upper MOSFETs
  - Pre-regulate input voltage (PFC)
    - ❑ Still have to deal with brown-out and hold-up
  - Operate converter at lowest frequency possible

- Comparison of FW MOSFET Conduction Losses for Telecom DC/DC App

Measured Values

$V_F = 1V$ $F_{SW} = 265kHz$ $I_{OUT} = 10A$

$I_{FW} = 2A$ $R_{DS\_ON} = 25m\Omega$

$t_{BD} = 970ns(25\%)$ $V_{IN} = 72V$

Calculated Body-Diode Conduction Loss in each Upper FET

$$P_{BD} = 970ns \times 265kHz \times 2A \times 1V = 514mW$$

Calculated Channel Conduction Loss in each Upper FET

$$P_{RDS(ON)} = 2A^2 \times 25m\Omega = 100mW$$

Total Conduction Loss for each FW period (ZVT PWM Control)

$$P_{FW1(ZVTPWM)} = 514mW + 100mW = 614mW \quad \text{(UL and UR)}$$

$$P_{FW2(ZVTPWM)} = 514mW + 100mW = 614mW \quad \text{(UL and UR)}$$

Total Conduction Loss for each FW period (PSFB Control)

$$P_{FW1(PSFB)} = 2 \times 100mW = 200mW \quad \text{(A and B)}$$

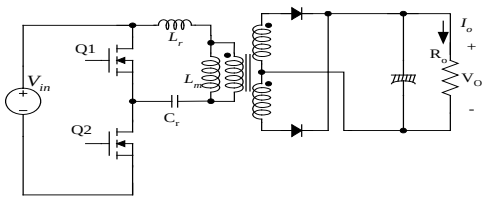
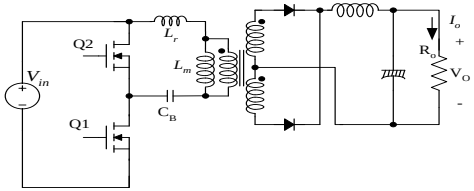
$$P_{FW2(PSFB)} = 2 \times 100mW = 200mW \quad \text{(C and D)}$$

*Assume switching, gate charge, Coss losses are same for each control method

High Power Topology Summary

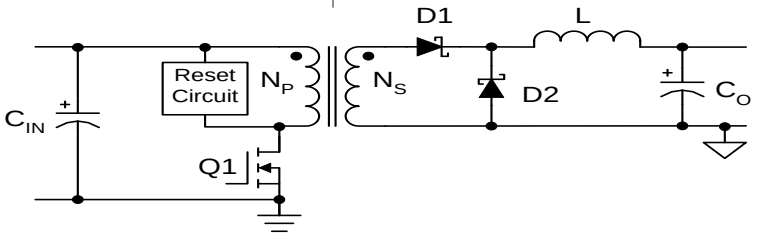
Topology	Transformer	Primary Switches	V_{DS}	"Ideal" Application
CCM Boost	Inductor (non-isolated)	1	V_{OUT}	High power PFC >300W Interleaved PFC >Several kW
BCM Boost	Inductor (non-isolated)	1	V_{OUT}	PFC <300W Interleaved PFC <1kW
Forward	Single-end	1	$2xV_{IN}$	<200W, universal off-line or telecom
Active Clamp	Single-end	2	$V_{IN} \times \frac{1}{1-D}$	<500W, universal off-line or telecom, highest efficiency required
2-Switch Forward	Single-end	2	V_{IN}	<500W, universal off-line, PFC pre-regulator
Half Bridge	Double-end	2	V_{IN}	<500W, EU off-line, Intermediate Bus Converters
Push Pull	Double-end	2	$2xV_{IN}$	<500W, telecom or low V_{IN} (<200V)
Full Bridge	Double-end	4	V_{IN}	>500W, universal off-line
Phase Shifted FB	Double-end	4	V_{IN}	>1kW, universal off-line or telecom, highest efficiency required
Current Doubler	Double-end	NA	NA	Any double-ended topology, low V_{OUT}, high I_{OUT} most benefit

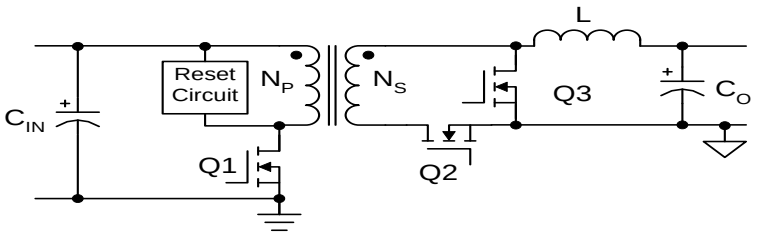
LLC vs AHB Comparison

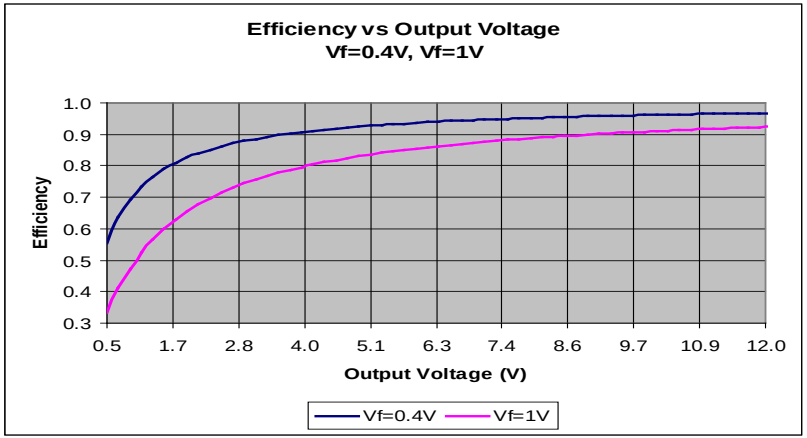
	LLC resonant converter	Asymmetric Half-bridge
		
Control method	**Variable frequency with fixed duty cycle (50%)**	**PWM with fixed frequency**
Practically input voltage range	**V^{max}/V^{min}=1.2~1.4**	**V^{max}/V^{min}=1.2~1.3**
Primary side MOSFET voltage	**☺ Clamped to the input voltage**	**☺ Clamped to the input voltage**
Secondary side rectifier voltage stress	**☺ 2 times the output voltage (for center tapped transformer)**	**☹ Usually about 3 to 6 times the output voltage for powering and freewheeling diodes, respectively (for center tapped transformer)**
Output capacitor current ripple	**☹ Almost twice the output current (peak-to-peak)**	**☺ Several tens % of output current (peak-to-peak)**
ZVS condition	**☺ ZVS is easily achieved from full load to no load condition using the energy in the magnetizing inductance**	**☹ ZVS is difficult to achieve at light load condition** **☺ ZVS at full load condition is relatively easy**
Other features	**☹ No simple power limit capability such as pulse-by-pulse current limit in PWM operation** **☹ Requires tight tolerance of resonant components (L,C)** **☹ Relatively large circulating current**	**☺ Tight tolerance is not required for the resonant components (L,C)**

- Non-Isolated Converter Topologies
- Single Ended Converter Topologies
- Double Ended Converter Topologies
- **Synchronous Rectification**

Synchronous Rectification (SR)





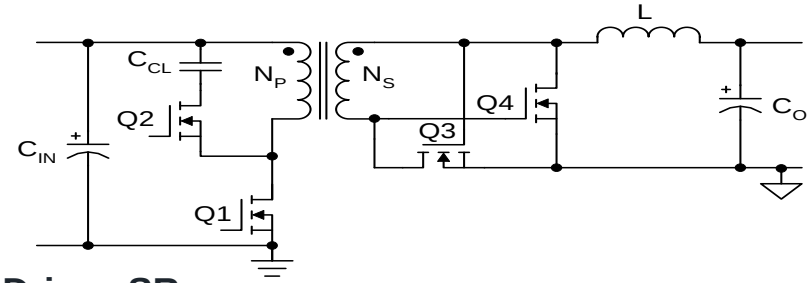


$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + V_F \times I_{OUT}} = \frac{1}{1 + \frac{V_F}{V_{OUT}}}$$

- What is Synchronous Rectification?
  - Replacing secondary side discrete rectifiers (D1, D2) with MOSFETs (Q2, Q3)
- Benefits of SR
  - Parallel MOSFETs
  - Increase efficiency
- Lower output voltage and higher current applications benefit most
- How do we drive them?

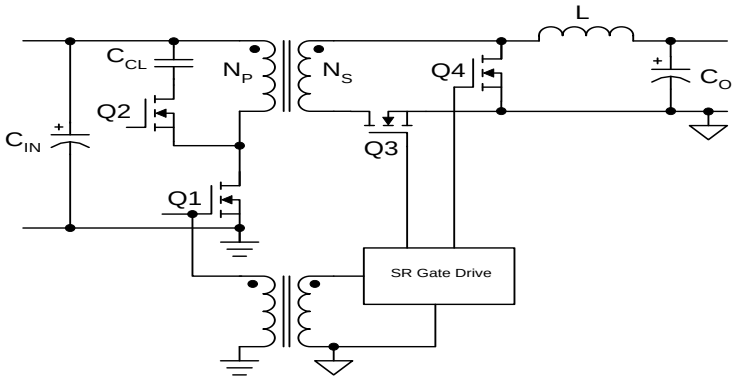
Single Ended Synchronous Rectification

SR Gate Drive Options



Self-Driven SR

- SR gate drive derived from transformer (as shown) or output inductor
- Advantages
  - Simple – no timing issues
  - High efficiency for few components
- Disadvantages
  - SR gate drive not regulated
  - Difficult when V_{IN} > 2:1
  - No control of secondary during start-up
  - Not compatible with all reset techniques

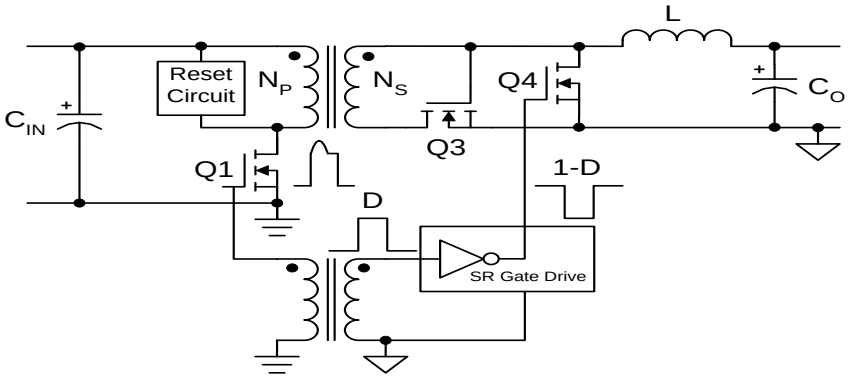


Control-Driven SR

- SR gate drive comes from PWM control signal
- Advantages
  - SR gate drive is regulated
  - Can be used for wide V_{IN} applications
  - Secondary is controlled by primary
- Disadvantages
  - Primary to secondary timing

Single Ended “Hybrid” SR

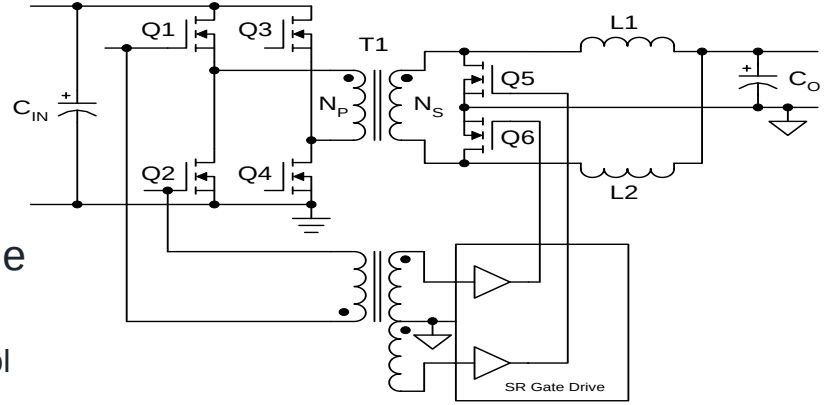
SR Gate Drive Options



- Hybrid-Driven SR
  - Combination of control driven and self driven
  - Forward SR (Q3) self driven by D
  - Free wheeling SR (Q4) driven by PWM inverted (1-D)
- Applications
  - Forward converter operating in DCM
  - RCD, Resonant and Third Winding Reset

Double Ended Synchronous Rectification *(>1kW)*

- SR applications typically greater than 12V output
- Highest efficiency
  - Minimize body-diode conduction
  - Use Secondary sensing for best timing
- SR driver solution is strongly related to control scheme
  - Primary side PWM control
    - ❑ Need signal and timing from pri-to-sec for good SR control
    - ❑ Difficult to adapt over line/load changes
  - Secondary side PWM control
    - ❑ Allows sensing key nodes for timing optimization
    - ❑ Cross boundary with timing to communicate with primary
    - ❑ Direct drive between PWM and SR
    - ❑ Needs startup bias supply



(a) Full Bridge with Current Doubler SR Secondary

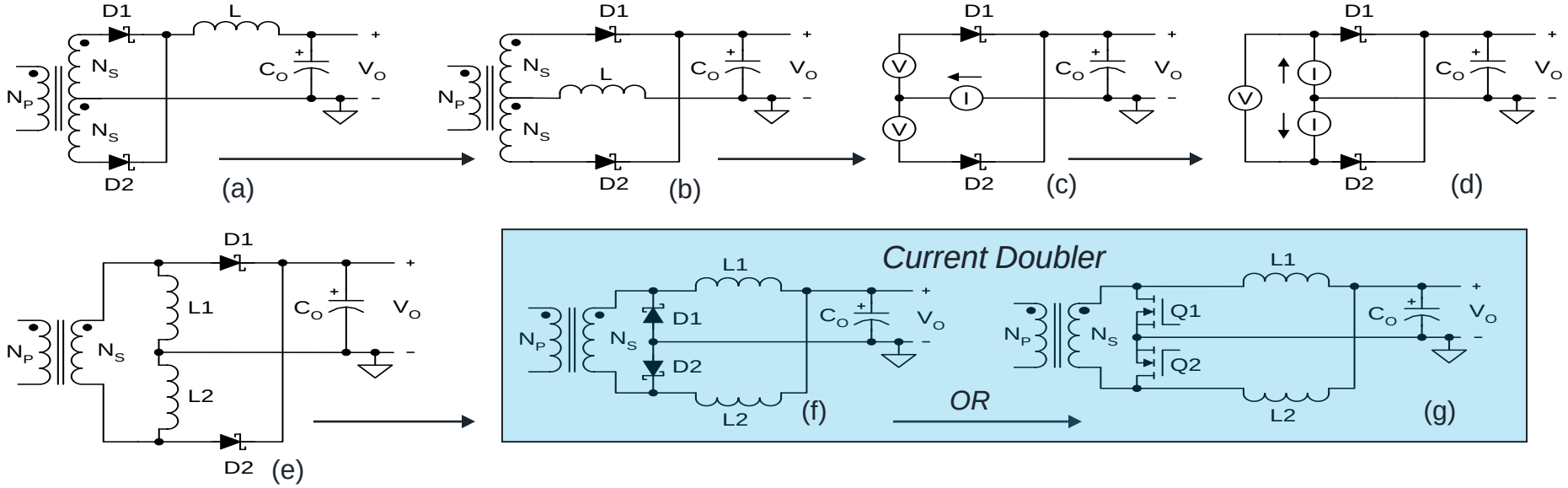
- Double ended control driven SR drive is the more difficult SR problem to solve

Double Ended (All)

Current Doubler Rectifier

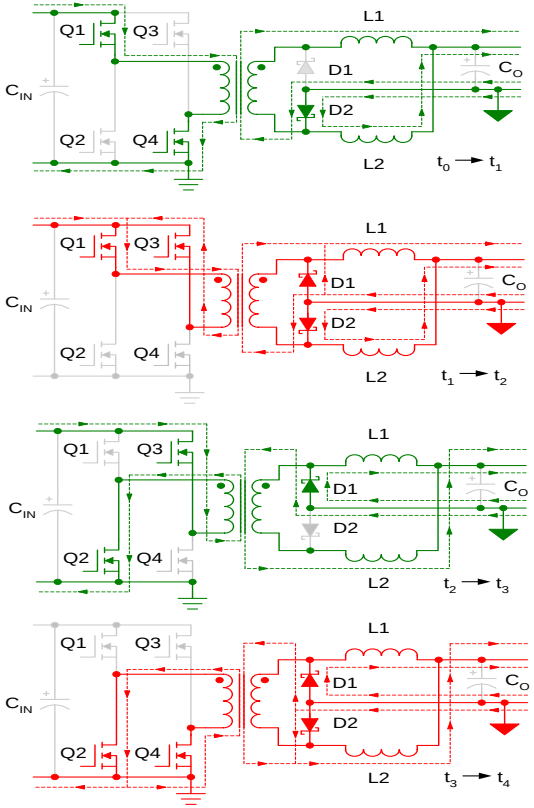
What is it? - *A full wave alternative rectification technique compatible with all double ended converter topologies*

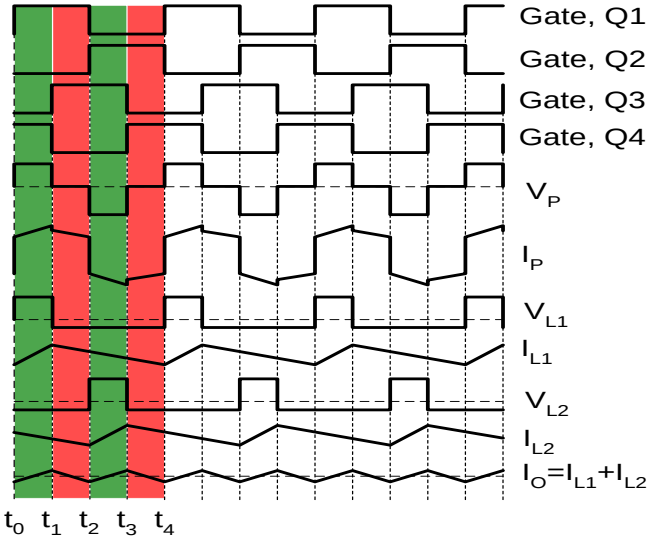
Derivation of Current Doubler



Double Ended (All)

Current Doubler Rectifier Operation





Current Doubler Timing Diagram (PSFB Application)

- Current doubler benefits:
  - Better thermal distribution for higher current outputs
  - Each inductor carries half the load current at half the switching frequency
  - Ripple currents cancel as a function of D
  - Single winding secondary

Summary

- Choosing the “best” topology:
  - Is the output voltage higher or lower than the input voltage range?
  - Are there isolation requirements?
  - Are multiple outputs required?
  - AC input – PFC/THD requirements?
  - Output power?
  - What is the maximum input/output voltage?
  - What is the maximum input/output current?
- Fine tune topology choice by trading off:
  - Efficiency
  - Performance
  - Cost
  - Size
- Q&A?

THANK YOU