



**ON Semiconductor®**

# **Step by Step Design Tutorial of a fixed-frequency adapter < 75 W with very low power consumption**

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# Agenda

- Application and requirements
- Flyback converter basics
- Flyback converter parasitic
- Design step 1: Power stage
- Design step 2: Efficiency optimization
- Design step 3: Control mode and protections
- Design step 4: No Load Input Power
- Design step 5: Magnetics
- Design step 6: EMI
- Demoboard example

# The flyback, a popular structure

- The flyback converter is widely used in consumer products
- ✓ Ease of design, low-cost, well-known structure
- Poor EMI signature, bulky transformer, practical up to 150 W



*DVD player* →

flyback  $\approx$  10 – 35 W



*charger* →

flyback  $\approx$  3 – 5 W



*notebook* →

flyback  $\approx$  40 – 180 W



# EPA 2.0 (External Power Supplies)

EPA ENERGY STAR Version 2.0 EPS Voluntary Specification  
(Effective November 1, 2008)

## *Energy-Efficiency Criteria for Ac-Ac and Ac-Dc External Power Supplies in Active Mode: Standard Models*

Nameplate Output Power ( $P_{no}$ )	Minimum Average Efficiency in Active Mode (expressed as a decimal)
0 to $\leq$ 1 watt	$\geq 0.480 * P_{no} + 0.140$
> 1 to $\leq$ 49 watts	$\geq [0.0626 * \ln(P_{no})] + 0.622$
> 49 watts	$\geq 0.870$

*(was > 0.84 in previous version 1.1)*

## *Energy Consumption Criteria for No-Load*

Nameplate Output Power ( $P_{no}$ )	Maximum Power in No-Load	
	AC-AC EPS	AC-DC EPS
0 to < 50 watts	$\leq 0.5$ watts	$\leq 0.3$ watts
$\geq 50$ to $\leq 250$ watts	$\leq 0.5$ watts	$\leq 0.5$ watts

*(< 0.5 W in 1.1)*

*(< 0.75 W in 1.1)*

# EPS 5.0 (ENERGY STAR® Program Requirements for Computers)

- Defines  $E_{TEC}$  for different types of products as a Typical Energy Consumption
- For the desktop and notebook product categories TEC will be determined by the following formula:

$$E_{TEC} = (8760/1000) * (P_{off} * T_{off} + P_{sleep} * T_{sleep} + P_{idle} * T_{idle})$$

- where all Px are power values in watts, all Tx are Time values in % of year, and the TEC  $E_{TEC}$  is in units of kWh and represents annual energy consumption based on mode weightings
- **The light load efficiency and no load consumption is more important**

$E_{TEC}$  requirement desktops and notebooks

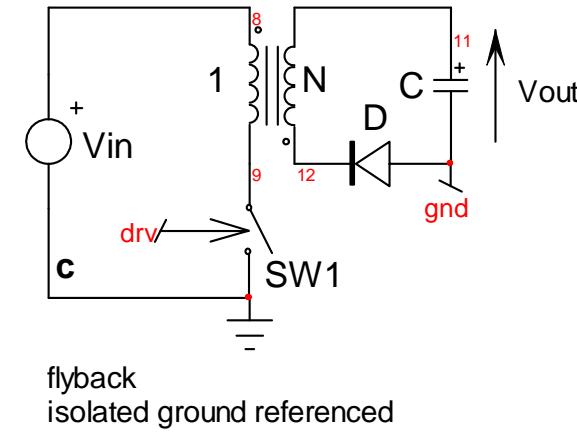
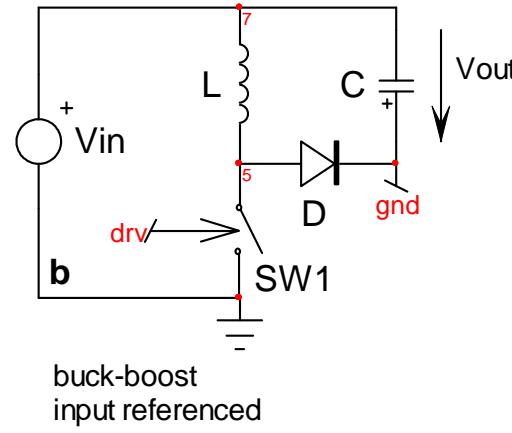
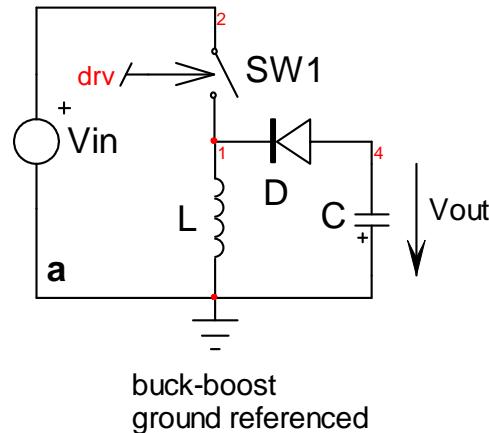
	Desktops and Integrated Computers (kWh)	Notebook Computers (kWh)
TEC (kWh)	<b>Category A:</b> ≤ 148.0 <b>Category B:</b> ≤ 175.0 <b>Category C:</b> ≤ 209.0 <b>Category D:</b> ≤ 234.0	<b>Category A:</b> ≤ 40.0 <b>Category B:</b> ≤ 53.0 <b>Category C:</b> ≤ 88.5

- Effective from July 1, 2009 (except: game consoles from July 1, 2010)

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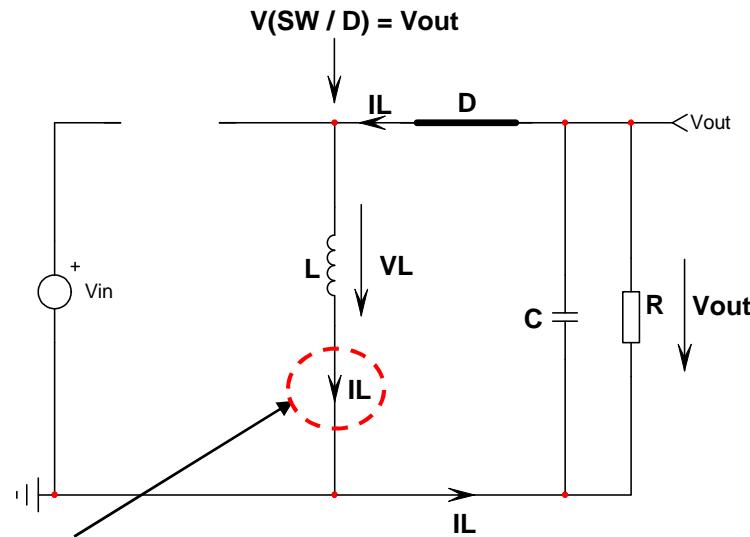
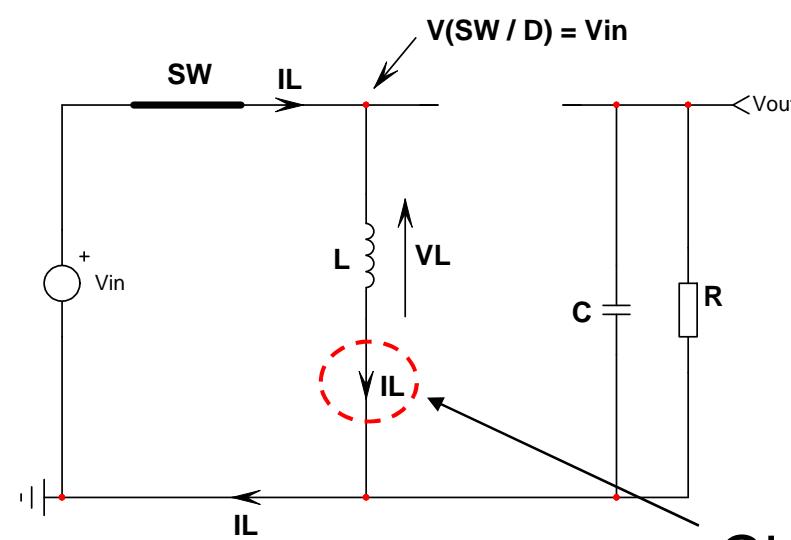
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# An isolated buck-boost



- The flyback converter is an isolated version of the buck-boost cell
- By rotating the switch, we obtain a ground-referenced isolated converter
- Keep this in mind for the small-signal analysis!

# On-time and freewheel



Circulates in the  
same direction

$$I_{peak} = I_{valley} + \frac{V_{in}}{L} t_{on}$$

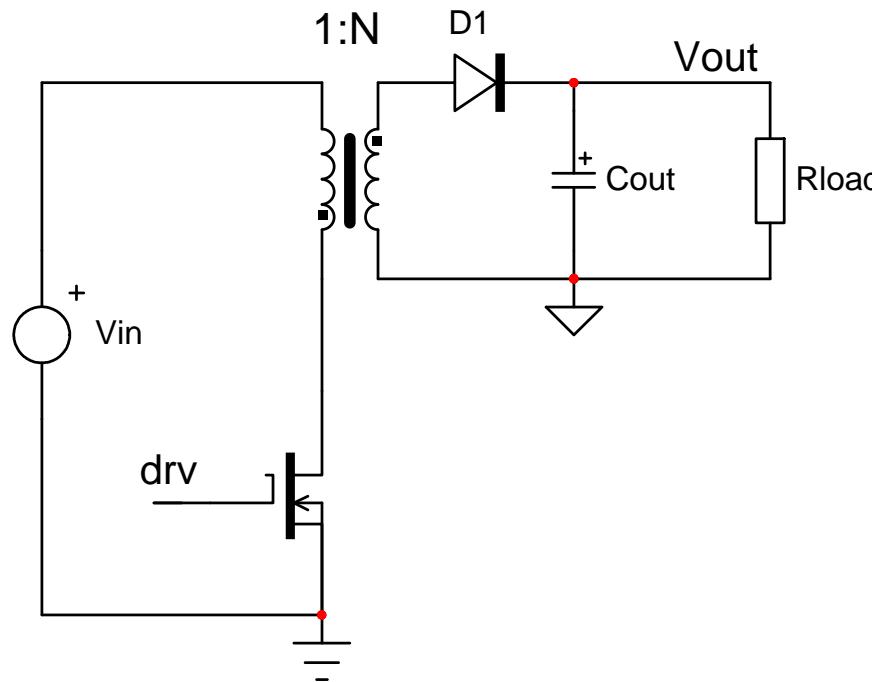
*SW* is closed, *D* is blocked

$$I_{valley} = I_{peak} - \frac{V_{out}}{L} t_{off}$$

*SW* is open, *D* is closed

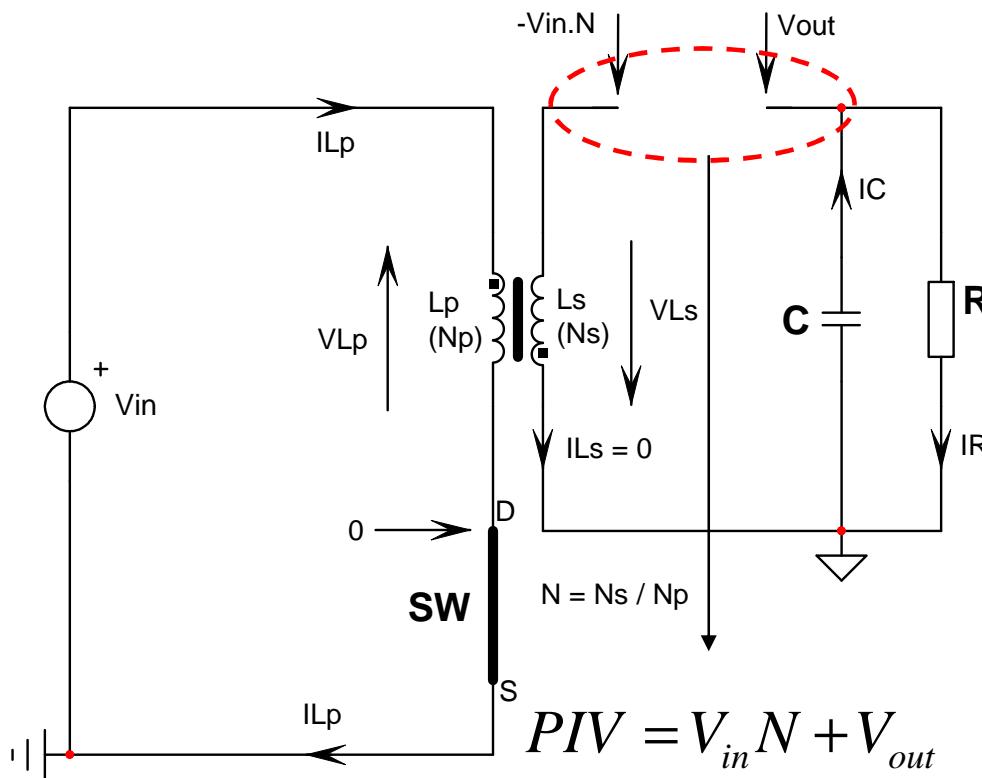
- When the switch closes, current ramps-up in *L*
- At the switch opening, the stored energy is dumped into *C*

# The flyback circuit



- Similar buck-boost equations hold when scaled by the turn ratio  $N$
- The switch is now ground referenced for an easier drive
- We have galvanic isolation between the primary and the secondary

# The turn-on event



$$S_{on} = \frac{V_{in}}{L_p}$$

$$I_{peak} = I_{valley} + \frac{V_{in}}{L_p} t_{on} \quad \text{CCM}$$

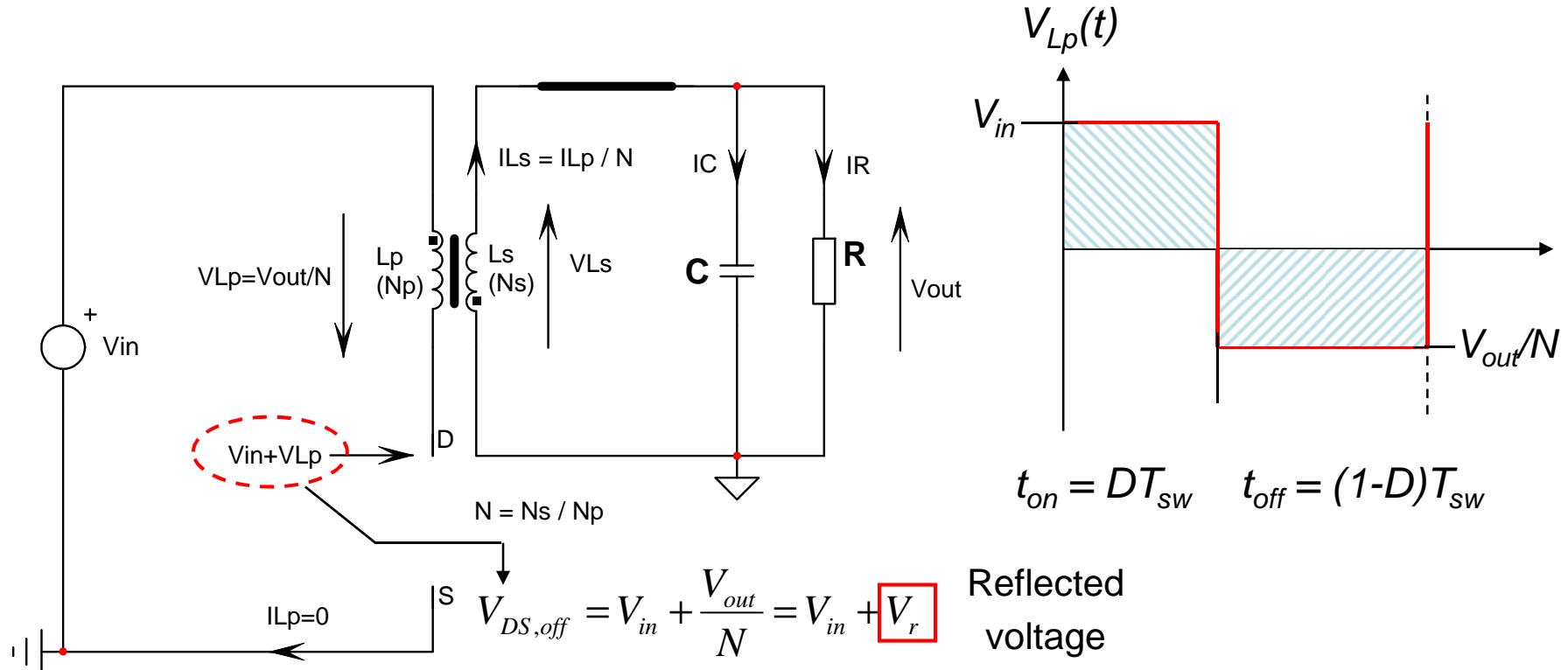
$$I_{peak} = \frac{V_{in}}{L_p} t_{on} \quad \text{DCM}$$

Reverse voltage on the diode

- The controller instructs the power switch to turn on
- The current increases in the inductor in relationship to  $V_{in}$  and  $L_p$
- The output capacitor supplies the load on its own

Simplified, no leakage

# Applying volt-second balance, CCM

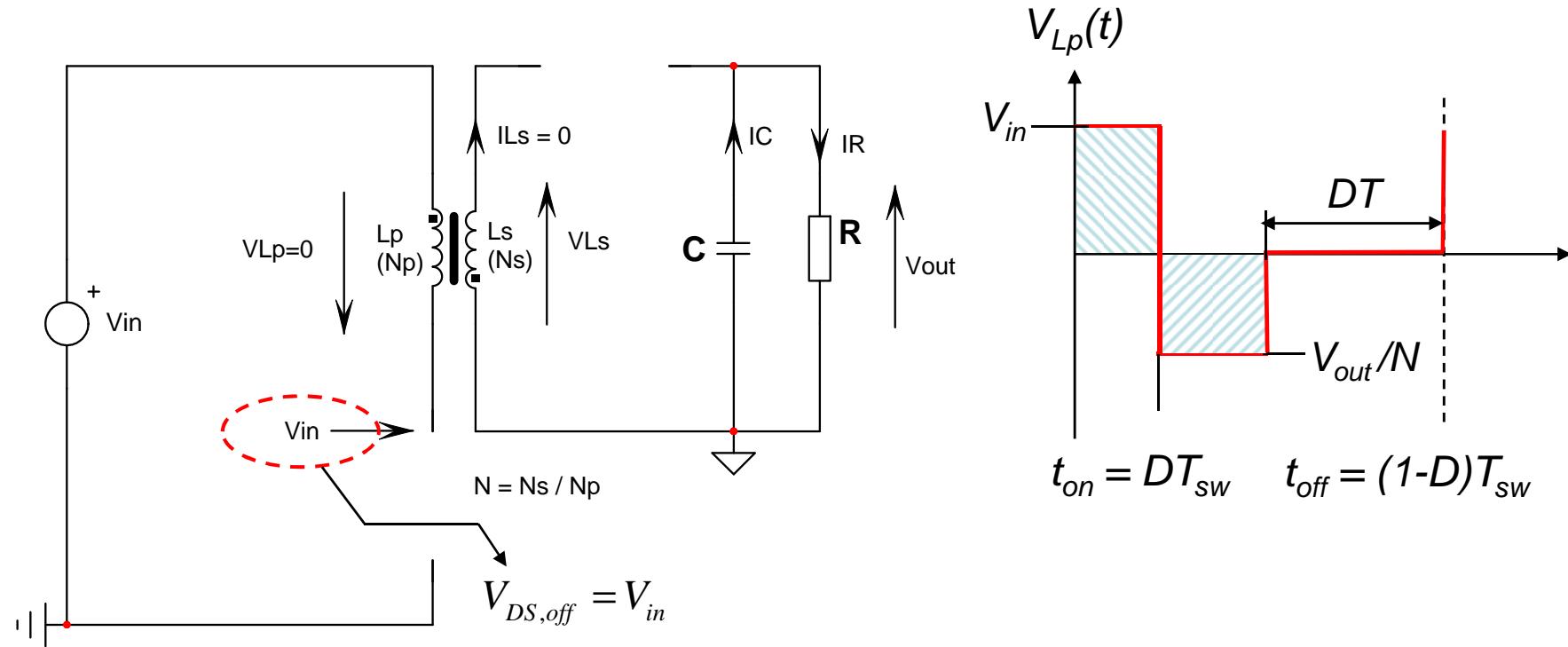


$$\frac{V_{out}}{V_{in}} = \frac{Nt_{on}}{t_{off}} = \frac{NDT_{sw}}{(1-D)T_{sw}} = \frac{ND}{(1-D)}$$

dc transfer function in CCM

Simplified, no leakage

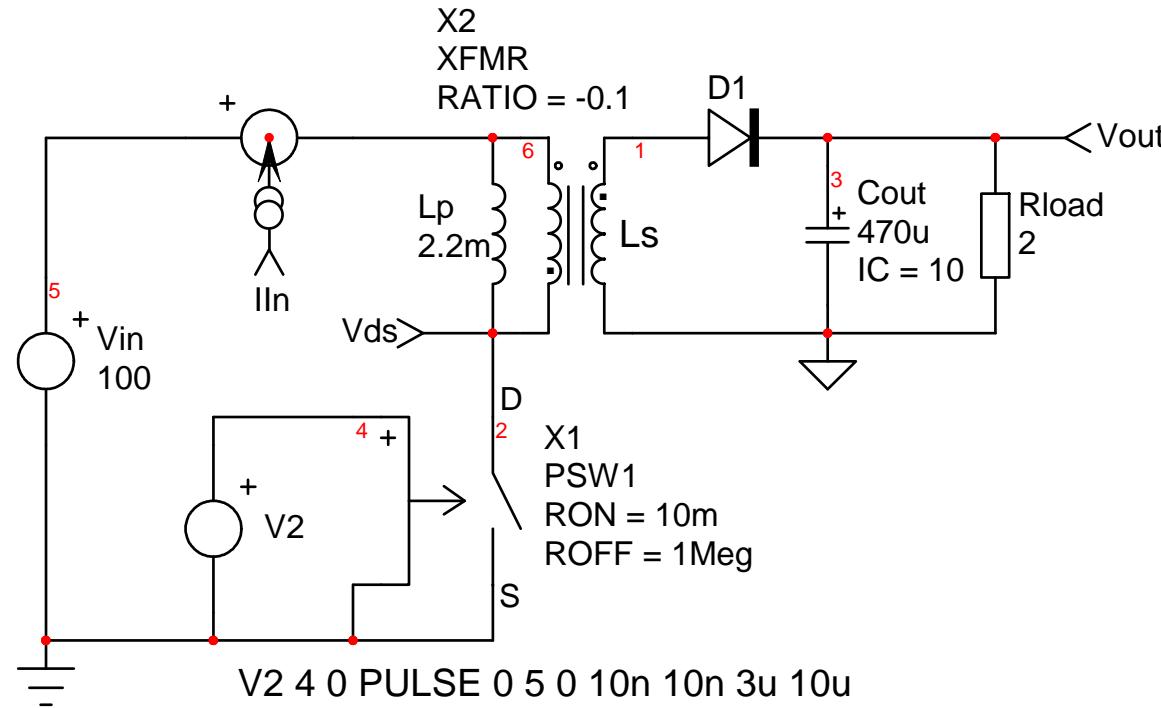
# Applying volt-second balance, DCM



$$\frac{V_{out}}{V_{in}} = D \sqrt{\frac{R_{load}}{2L_p F_{sw}}}$$

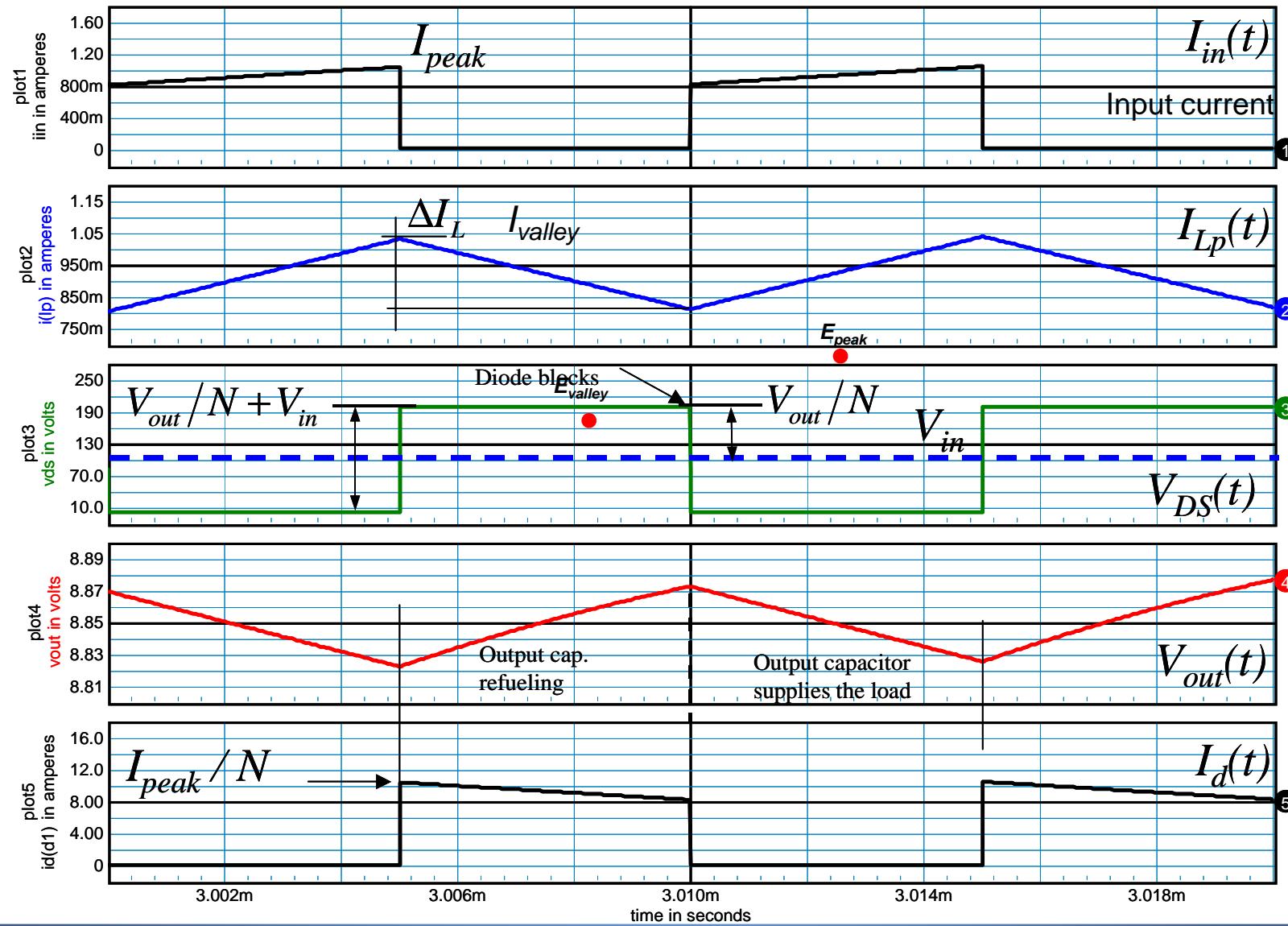
dc transfer function in DCM  
 $N$  no longer plays a role  
 $R_{load}$ ,  $L_p$  and  $F_{sw}$  do

# Flyback, typical waveforms

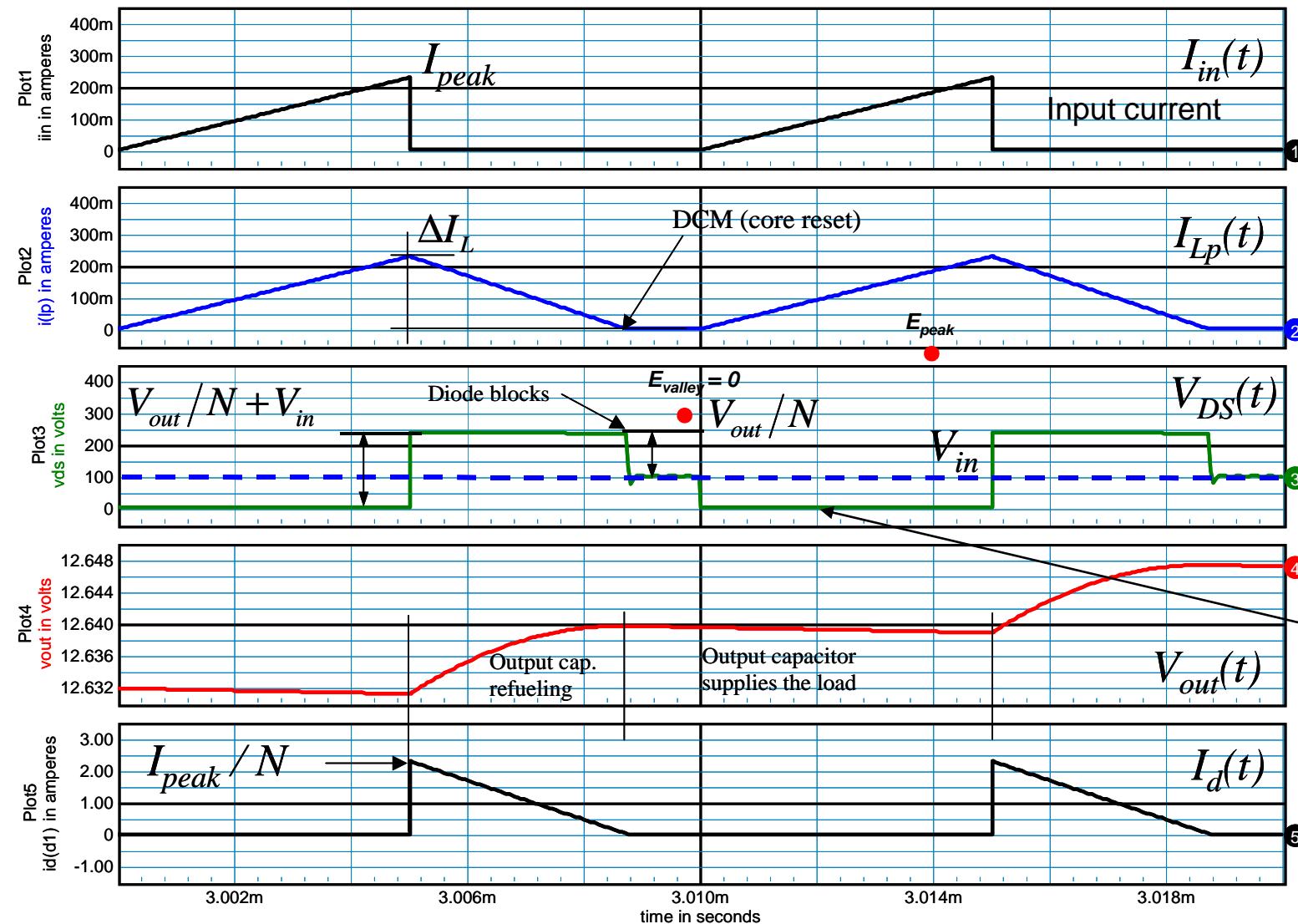


- A simple flyback circuit without parasitic elements
- It runs open-loop for the sake of simplicity
- $V_{out} = 8 V$

# Flyback, typical waveforms, CCM



# Flyback, typical waveforms, DCM



# Energy transfer in CCM and DCM

$$E_{L_p, \text{valley}} = \frac{1}{2} L_p I_{\text{valley}}^2 \quad \text{Initially stored energy}$$

$$E_{L_p, \text{peak}} = \frac{1}{2} L_p I_{\text{peak}}^2 \quad \text{Stored energy at } t_{\text{on}}$$

$$E_{L_p, \text{accu}} = \frac{1}{2} L_p I_{\text{peak}}^2 - \frac{1}{2} L_p I_{\text{valley}}^2 = \frac{1}{2} L_p (I_{\text{peak}}^2 - I_{\text{valley}}^2) \quad \text{Accumulated energy at } T_{\text{sw}}$$

Power (watts) is energy (joules) averaged over time (a switching cycle, seconds)

$$P_{\text{out}} = \frac{1}{2} (I_{\text{peak}}^2 - I_{\text{valley}}^2) L_p F_{\text{sw}} \eta$$

CCM

$$P_{\text{out}} = \frac{1}{2} I_{\text{peak}}^2 L_p F_{\text{sw}} \eta$$

DCM,  $I_{\text{valley}} = 0$

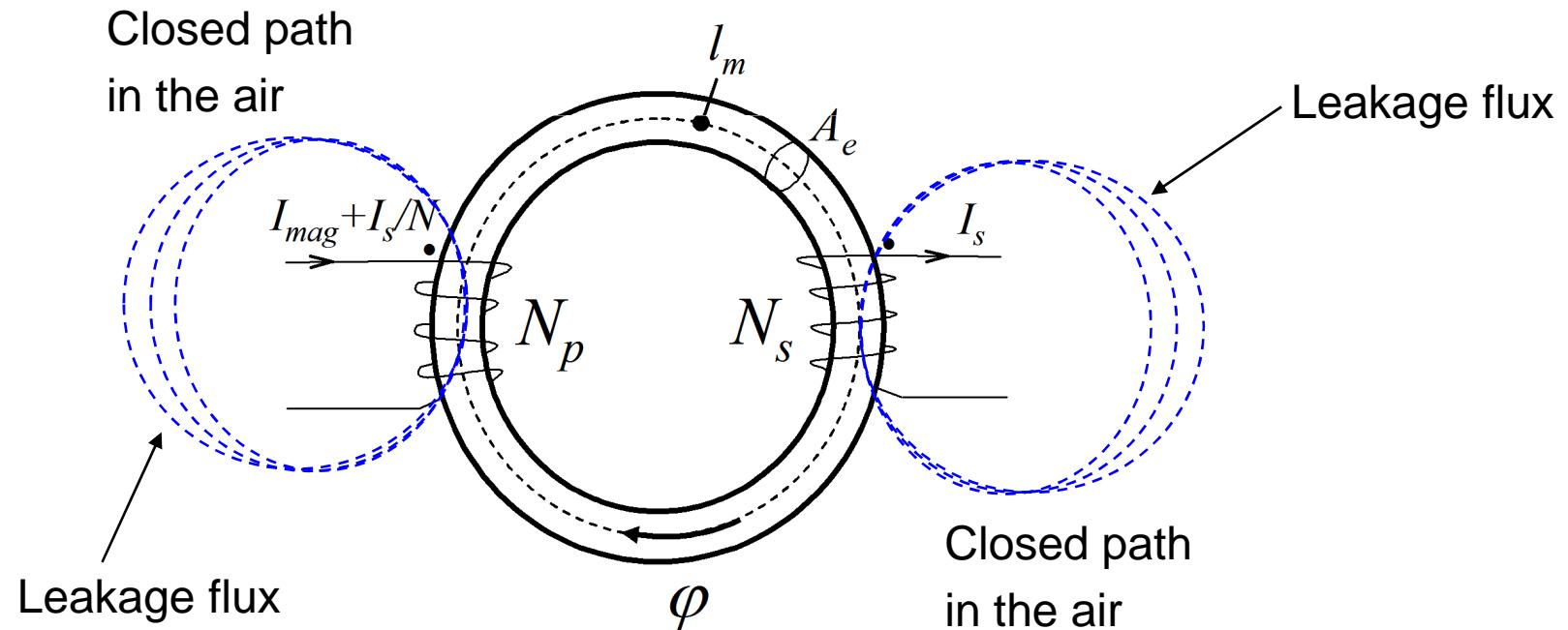
Eta, the efficiency

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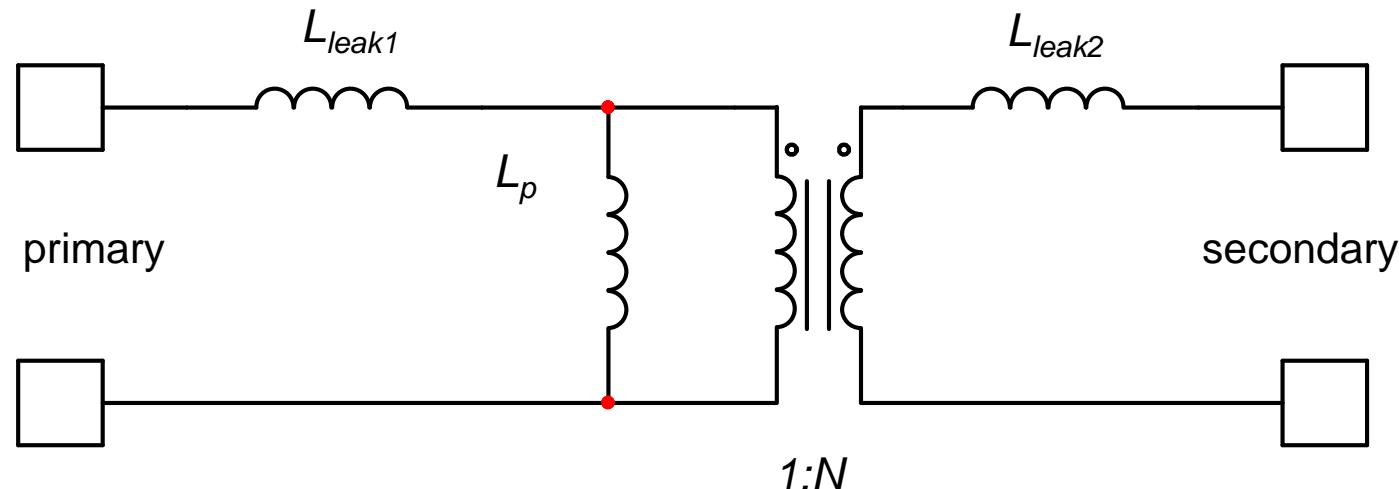
# The leakage inductance

- The coupling in a transformer is not perfect
- Some induction lines couple in the air: leakage flux

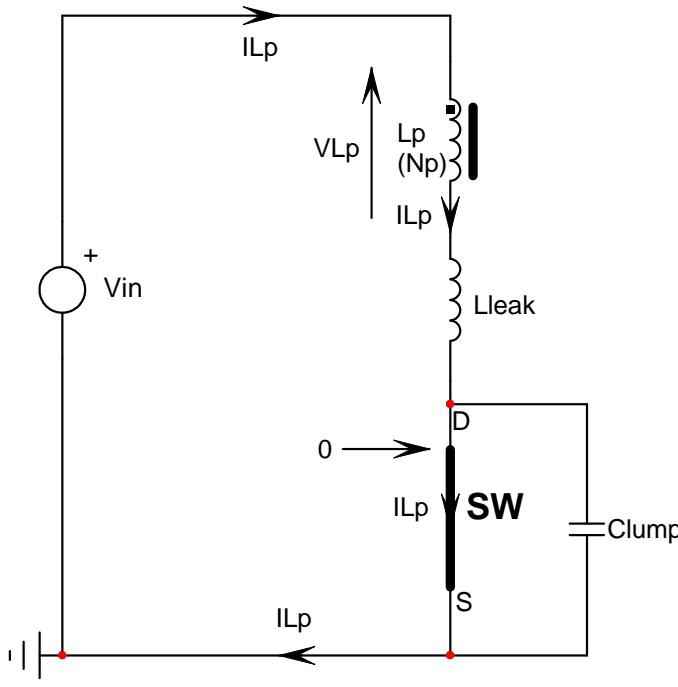


# An equivalent transformer model

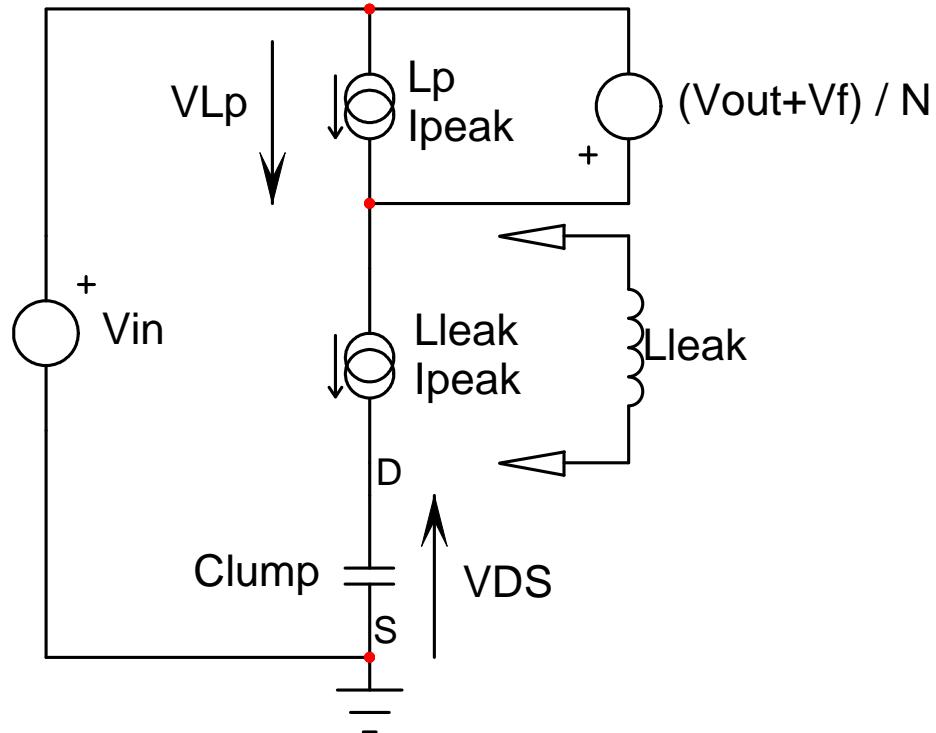
- For a two-winding transformer, the model is simple:
  - ✓ Two leakage inductors
  - ✓ One magnetizing inductor



# The leakage role

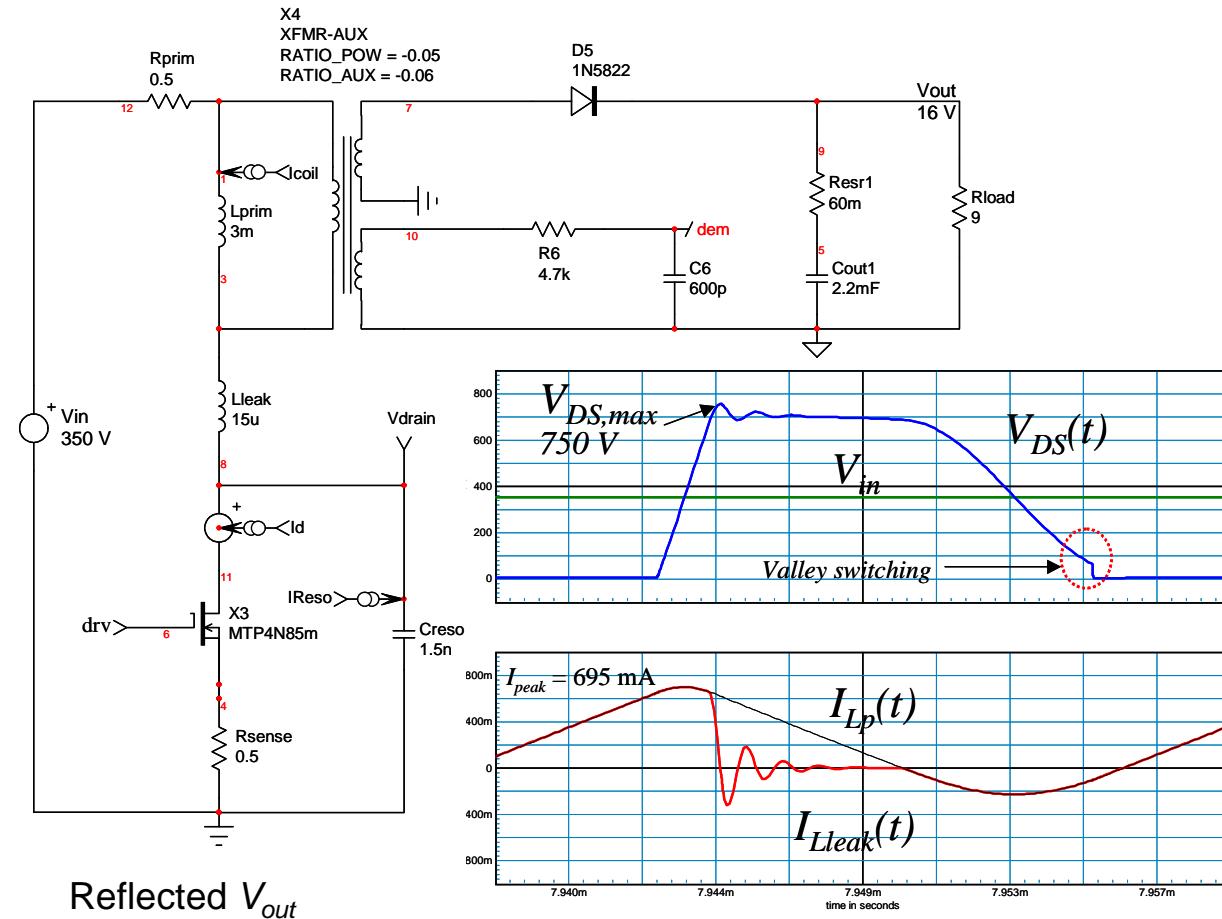


The switch closes:  
Current flows in  $L_{leak}$  and  $L_p$



The switch opens:  
The current charges the lump capacitor

# Drain-source excursion



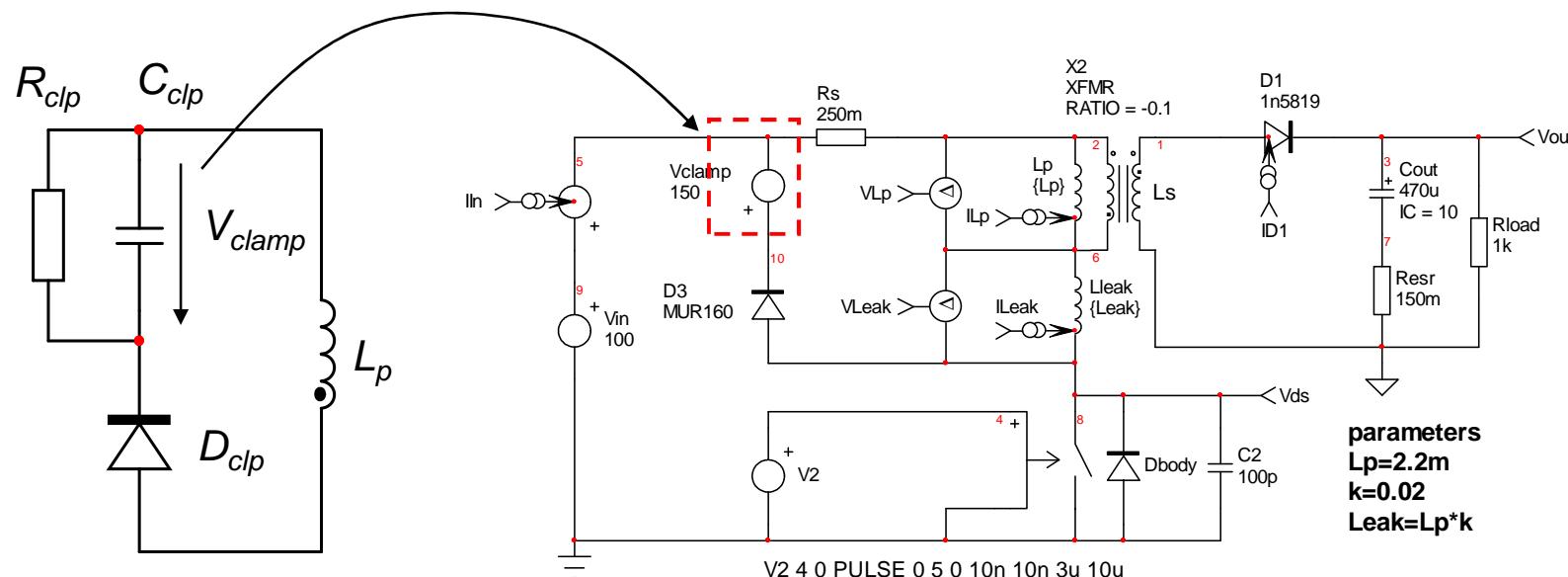
$$V_{DS,max} = V_{in} + \frac{(V_{out} + V_f)}{N} + I_{peak} \sqrt{\frac{L_{leak}}{C_{lump}}}$$

Reflected  $V_{out}$

Characteristic impedance

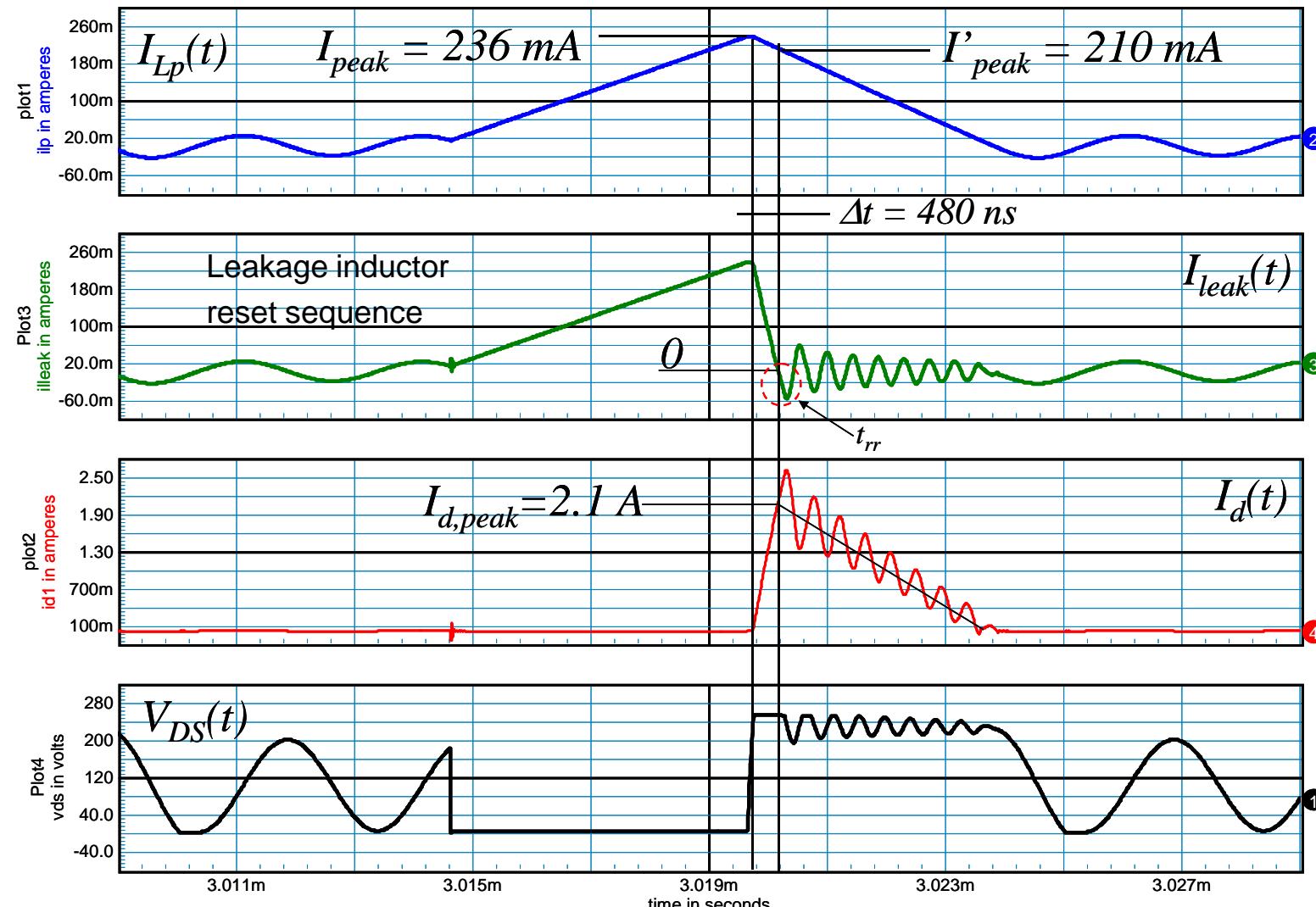
Need to limit the excursion!

# The need of a clamp

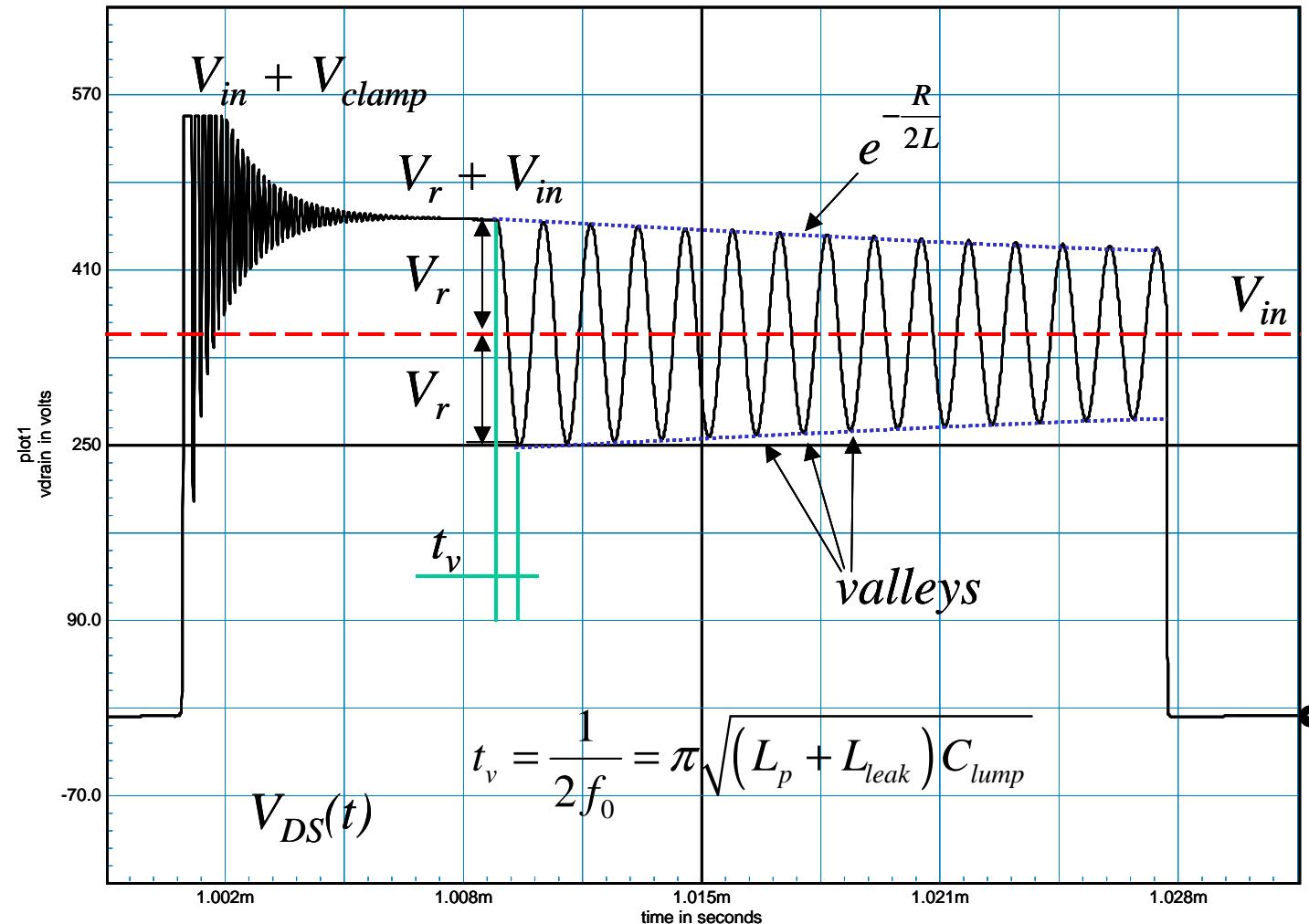


- The clamp is made by a low impedance voltage source
- When the drain reaches  $V_{in} + V_{clamp}$ , the clamp diode conducts

# A reduced secondary-side current



# Ringing and turn-on in the valleys?

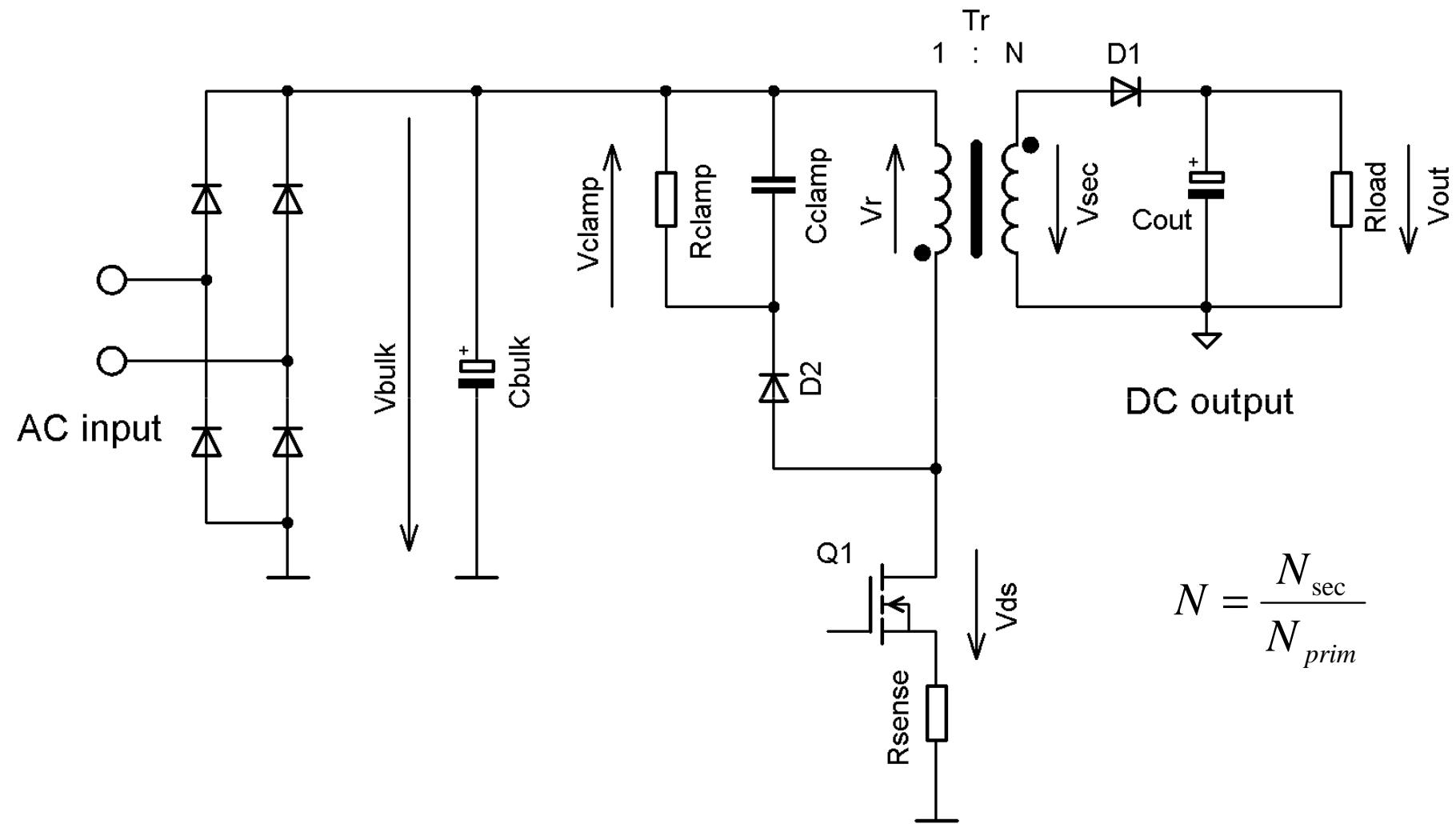


- Wait until the drain voltage is minimum and reduce turn-on losses: valley switching!

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# Power stage: Schematic of flyback converter



$$N = \frac{N_{sec}}{N_{prim}}$$

# Power stage design: Bulk capacitor

- Output power  $P_{out}$

$$P_{out} = V_{out} \cdot I_{out}$$

- Estimation of input power  $P_{in}$

$$P_{in} = \frac{P_{out}}{\eta}$$

Estimate the  $\eta$  based  
on the EPA standard

- Average input current  $I_{in,avg}$

$$I_{in,avg} = \frac{P_{in}}{V_{bulk,min}}$$

- Design the bulk capacitor for the maximum output power and the minimum input line voltage.

# Power stage design: Bulk capacitor

- 1<sup>st</sup> current approach

$$C_{bulk} = \frac{1}{2 \cdot f_{line}} \cdot \frac{I_{in,avg}}{\Delta V_{bulk}} \left[ 1 - \frac{1}{\pi} \cdot \cos^{-1} \left( 1 - \frac{\Delta V_{bulk}}{V_{peak}} \right) \right]$$

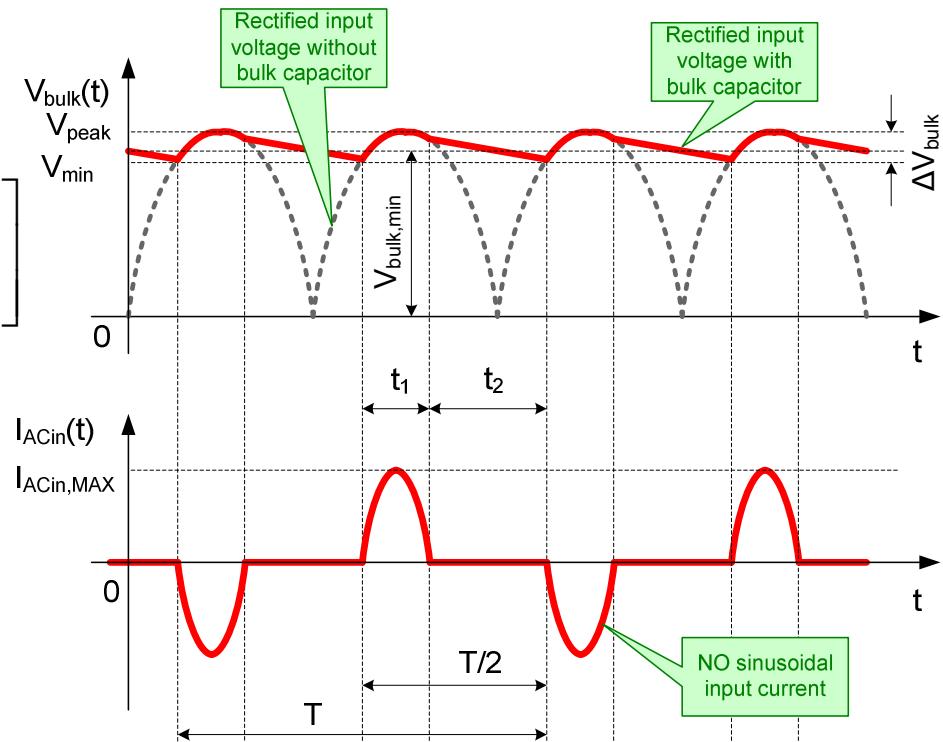
Simple current approach:

$$C_{bulk} = \frac{I_{in,avg} \cdot t_2}{\Delta V_{bulk}}$$

Use  $t_2=7.5$  to  $8.5\text{ms}$  for  $f_{line}=50\text{Hz}$

- 2<sup>nd</sup> power approach

$$C_{bulk} = \frac{2 \cdot P_{in} \cdot t_2}{V_{peak}^2 - V_{min}^2}$$



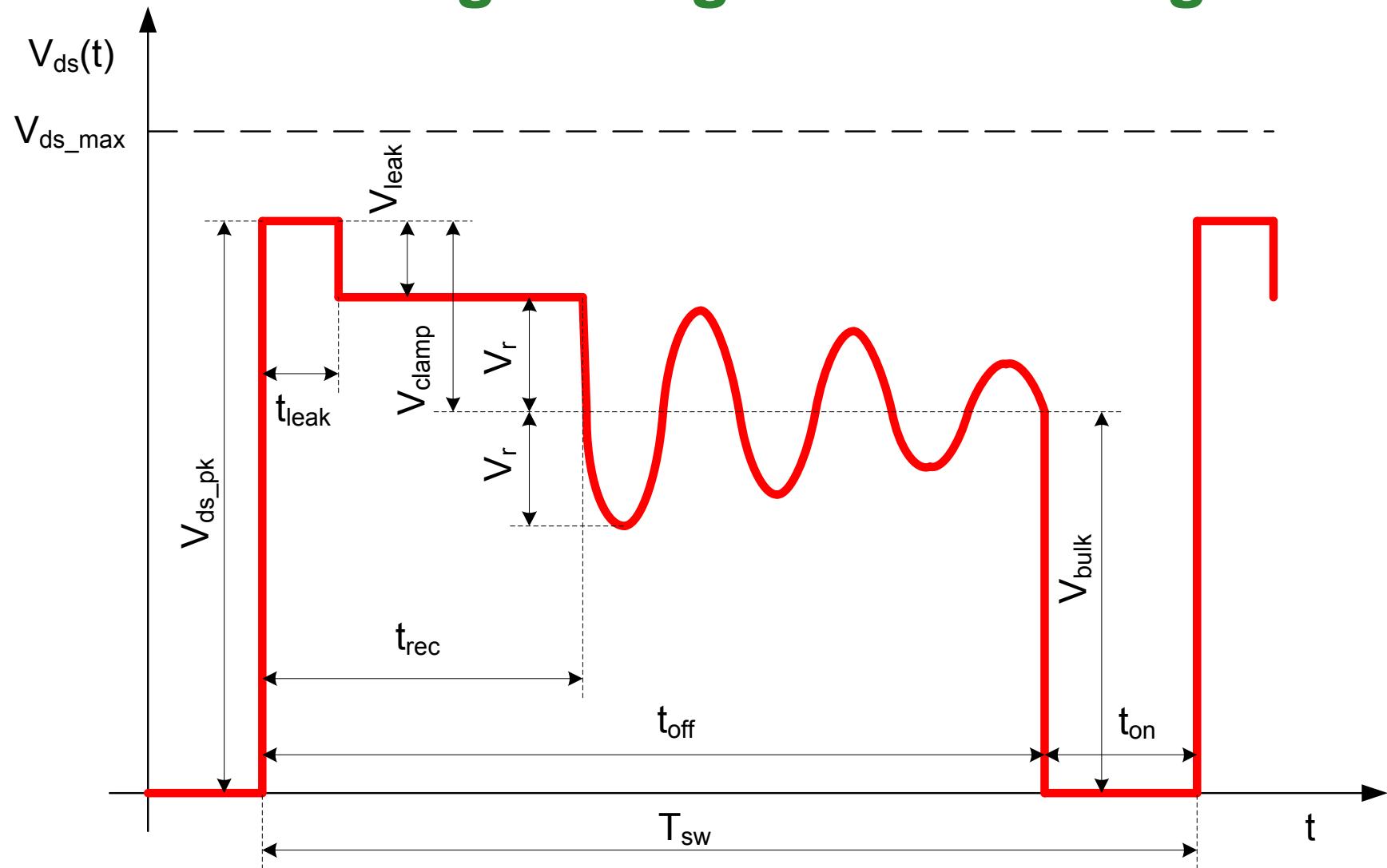
$$T = \frac{1}{f_{line}}$$

## Consideration:

Low volume bulk: large ripple, better PF, lower input RMS current

High volume bulk: low ripple, bad PF, high input RMS current

# Power stage design: Drain voltage



# Power stage design: Transformer ratio

Transformer ratio – consideration of the  $V_{DSS}$  of used Q1

$$N = \frac{k_C \cdot (V_{out} + V_{f,diode})}{0.85 \cdot V_{DS,max} - 20V - V_{bulk,max}}$$
$$k_C = \frac{V_{clamp}}{V_r}$$

*The 20V means margin for clamping diode turning-on overshoot.*

Reflected voltage  $V_r$  at primary from secondary

$$V_r = \frac{V_{out} + V_{f,diode}}{N}$$

$$N = \frac{N_{sec}}{N_{prim}}$$

Maximum duty cycle  $DC_{max}$

In CCM operation:

$$DC_{max} = \frac{V_r}{V_r + V_{bulk,min}}$$

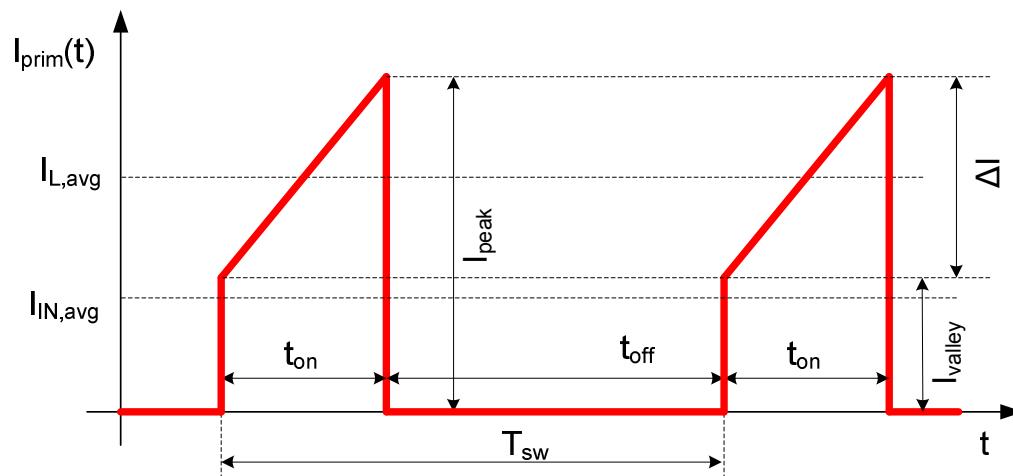
In DCM operation doesn't depend on N:

$$DC_{max} = \frac{V_{out}}{V_{bulk,min}} \cdot \sqrt{\frac{2 \cdot L_{prim} \cdot F_{sw}}{R_{load,min}}}$$

# Power stage design: Current ripple

The average shared transformer current reflected to primary winding  $I_{L,avg}$

$$I_{L,avg} = \frac{I_{in,avg}}{DC_{max}}$$



Choose the relative ripple  $\delta I_r$ : it affects the operation in the CCM or DCM

- For universal AC input design use the  $\delta I_r$  in range 0.5 to 1.0
- For European AC input use the  $\delta I_r$  in range 0.8 to 1.6

$$\delta I_r = \frac{\Delta I}{I_{L,avg}}$$

$$\Delta I = \delta I_r \cdot I_{L,avg}$$

$$\Delta I = I_{peak} - I_{valley}$$

$$I_{peak} = I_{L,avg} \cdot \left( 1 + \frac{\delta I_r}{2} \right)$$

$$I_{valley} = I_{L,avg} \cdot \left( 1 - \frac{\delta I_r}{2} \right)$$

# Power stage design: Primary inductance

Transformer primary winding inductance  $L_{\text{prim}}$

$$L_{\text{prim}} = \frac{V_{\text{bulk,min}} \cdot DC_{\text{max}}}{F_{\text{sw}} \cdot \Delta I}$$

Maximum RMS value of the current flowing through primary winding  $I_{\text{prim,RMS}}$

$$I_{\text{primRMS}} = \sqrt{DC_{\text{max}} \cdot \left( I_{\text{peak}}^2 - I_{\text{peak}} \cdot \Delta I + \frac{\Delta I^2}{3} \right)}$$

Maximum RMS value of the current flowing through secondary winding  $I_{\text{sec,RMS}}$

$$I_{\text{sec,peak}} = \frac{I_{\text{peak}}}{N} \quad \Delta I_{\text{sec}} = \frac{\Delta I}{N}$$

$$I_{\text{secRMS}} = \sqrt{(1 - DC_{\text{max}}) \cdot \left( I_{\text{sec,peak}}^2 - I_{\text{sec,peak}} \cdot \Delta I_{\text{sec}} + \frac{\Delta I_{\text{sec}}^2}{3} \right)}$$

# Power stage design: Q1 selection

Conduction loss at Q1 should be approx. 1% of the Pout

$$R_{DSon} \leq \frac{P_{out}}{100 \cdot I_{prim,RMS}^2}$$

Then the right device is chosen by parameters  $V_{DSmax}$ ,  $I_{peak}$ ,  $t_{on}$ ,  $t_{off}$

Current sensing resistor  $R_{sense}$  selection

$$R_{sense} = \frac{V_{ILIM}}{1.1 \cdot I_{peak}}$$

$$P_{sense} = I_{primRMS}^2 \cdot R_{sense}$$

*The 1.1 factor means 10% margin for  $L_{prim}$  and other parameters spread, to be able to deliver maximum power.*



# Power stage design: Secondary rectification

## D1 selection:

Reverse voltage across D1

$$PIV = V_{bulk,\max} \cdot N + V_{out}$$

The next important parameters for D1 selection are  $I_{sec,peak}$ ,  $I_{out}$  and the fast and soft recovery

## Cout selection:

Minimum  $C_{out}$  value

$$C_{out} \geq \frac{I_{out} \cdot DC_{\max}}{V_{out,ripple} \cdot F_{sw}}$$

The maximum allowed ESR of  $C_{out}$

$$ESR \leq \frac{V_{out,ripple}}{I_{sec,peak}} \quad \text{Dominant part}$$

$$I_{Cout,rms} = \sqrt{I_{sec,rms}^2 - I_{out}^2}$$

It is recommended to use more parallel  $C_{out}$  for lowering the output voltage ripple.

# Power stage design: Clamping network

TVS – losses in the suppressor: better at no load conditions

$$P_{clamp} = E_{clamp} \cdot F_{sw} = \frac{1}{2} \cdot L_{leak} \cdot I_{peak}^2 \cdot F_{sw} \cdot \frac{V_{clamp}}{V_{clamp} - V_r}$$

RCD clamp – 1<sup>st</sup> iteration: better EMI response

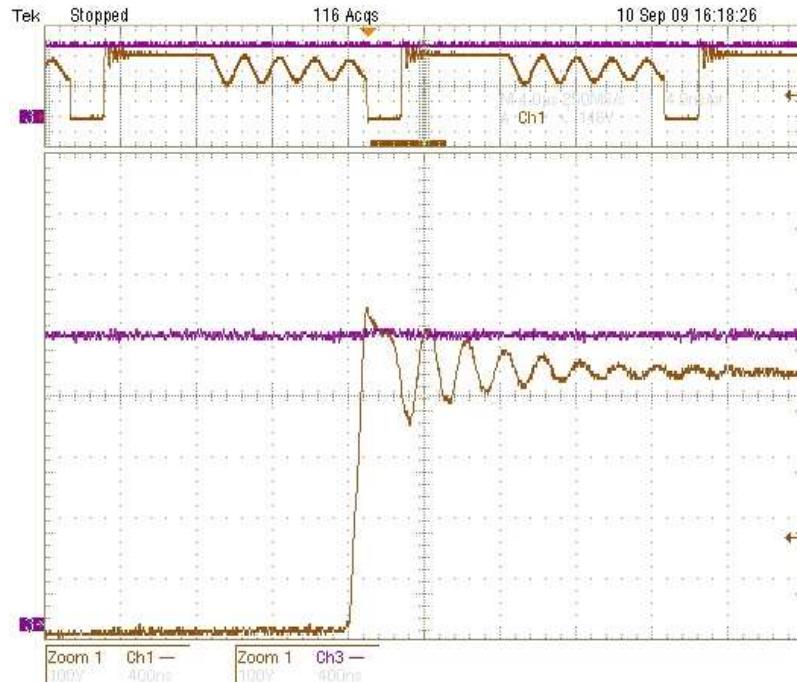
$$R_{clamp} = \frac{2 \cdot V_{leak} \cdot V_{clamp}}{L_{leak} \cdot I_{peak}^2 \cdot F_{sw}}$$

$$P_{clamp} = \frac{V_{clamp}^2}{R_{clamp}}$$

$$C_{clamp} > \frac{V_{clamp}}{V_{ripple} \cdot R_{clamp} \cdot F_{sw}}$$

These values need to be optimized for the no load consumption and losses in slow clamping diode D2

# TVS vs RCD clamp comparison



Drain voltage ringing with TVS as clamp



Drain voltage ringing with RCD as clamp

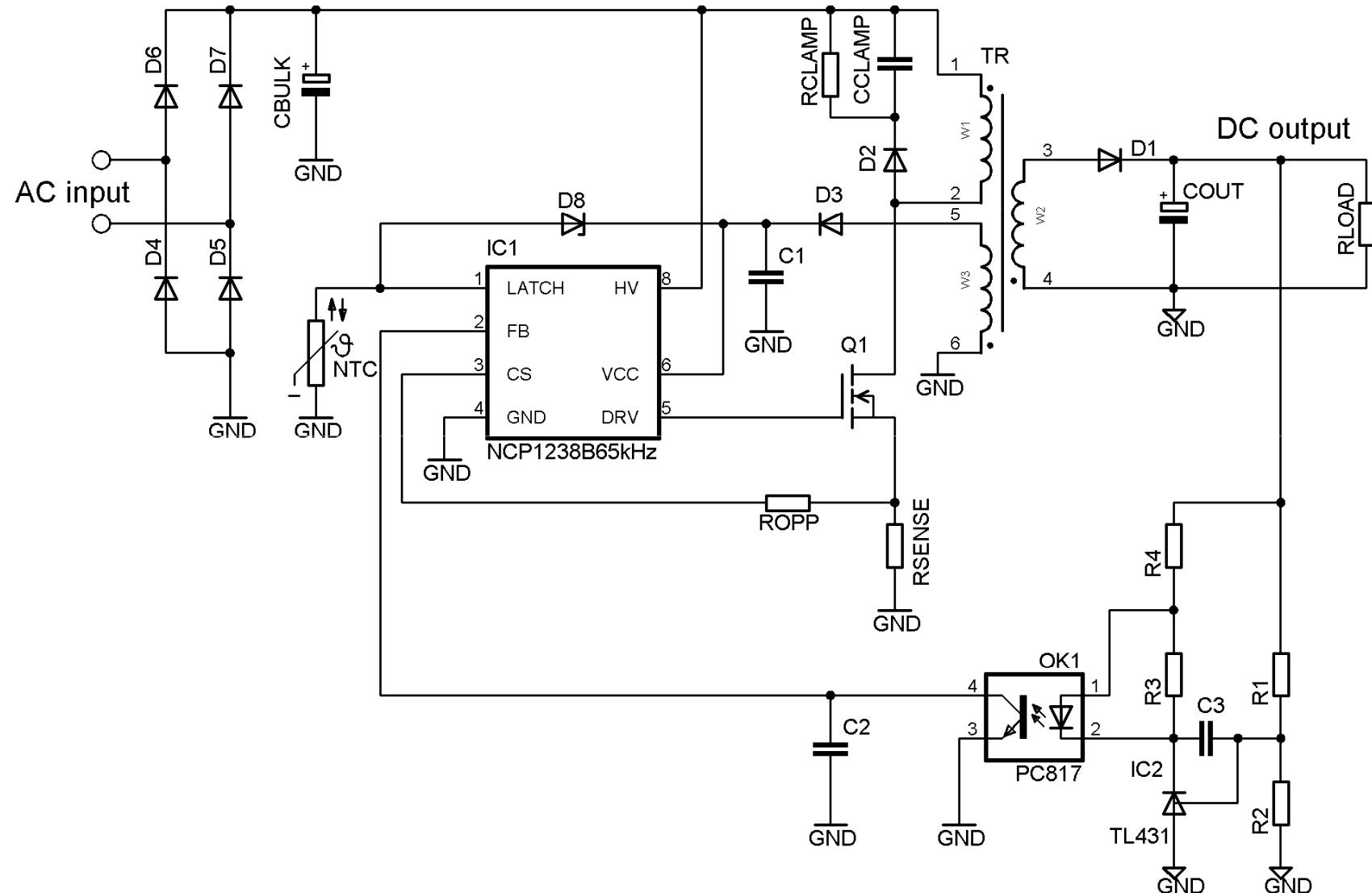
Different  $R_{damp}$  used in clamp

Ch1 – Drain, Ch3 – Clamp node

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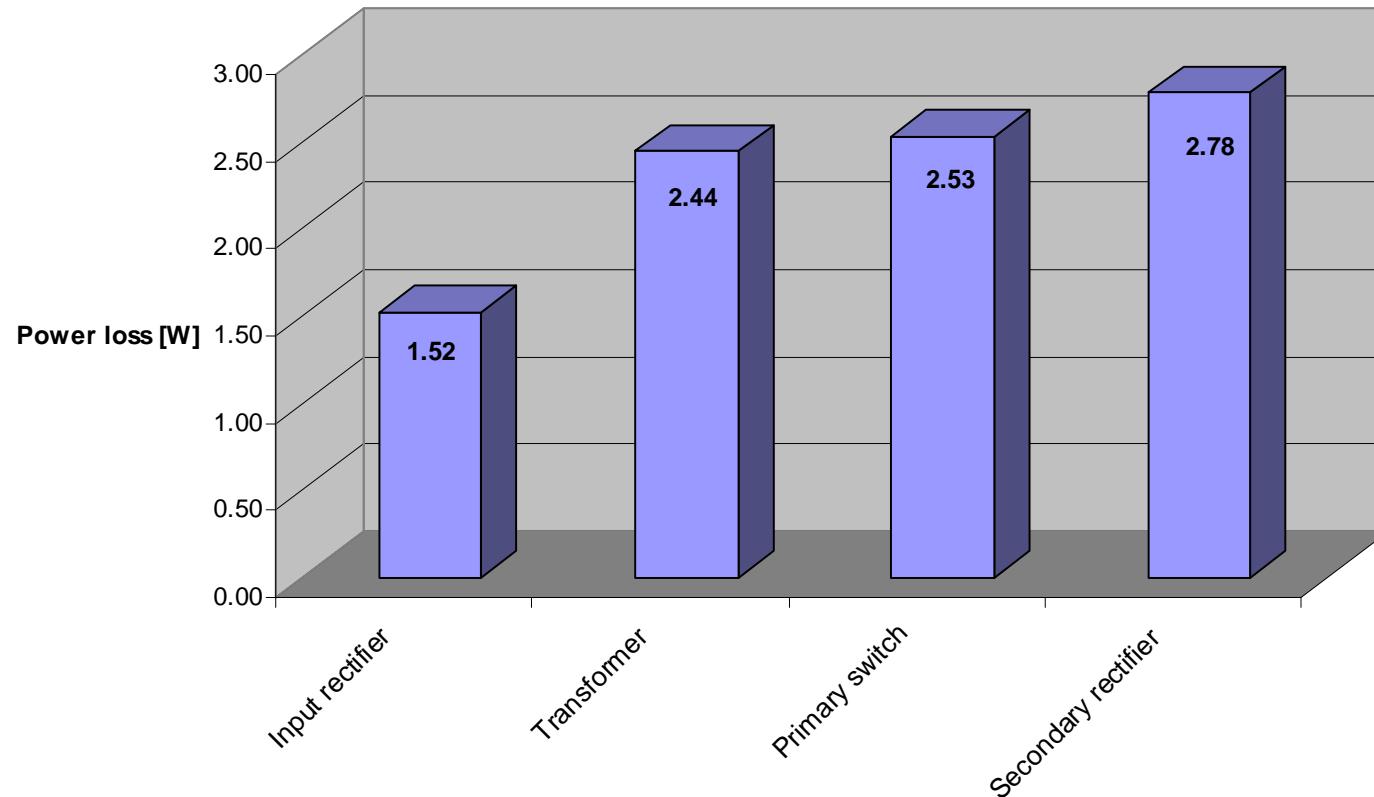
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# Application schematic



# The losses distribution

Losses distribution measured without EMI filters and surge protecting NTC



Input line	Input power	Output power	Total loss power	Efficiency
110 V / 60 Hz	72.5 W	63.62 W	8.88W	87.75%

# Optimization of efficiency

- There was not found excessive contributor of losses in the power stage of the flyback converter
- Losses in all components should be decreased
- Optimization approach:
  - 1) decreasing the losses in power stage by selection of primary switch Q1 and secondary rectifier D1
  - 2) decreasing the losses in power stage by decreasing losses in transformer
  - 3) try to improve the bridge rectifier (not much space)
  - 4) decreasing the conductive losses in EMI filters
  - 5) Do we need surge protecting NTC in case of “low value” bulk capacitor ?

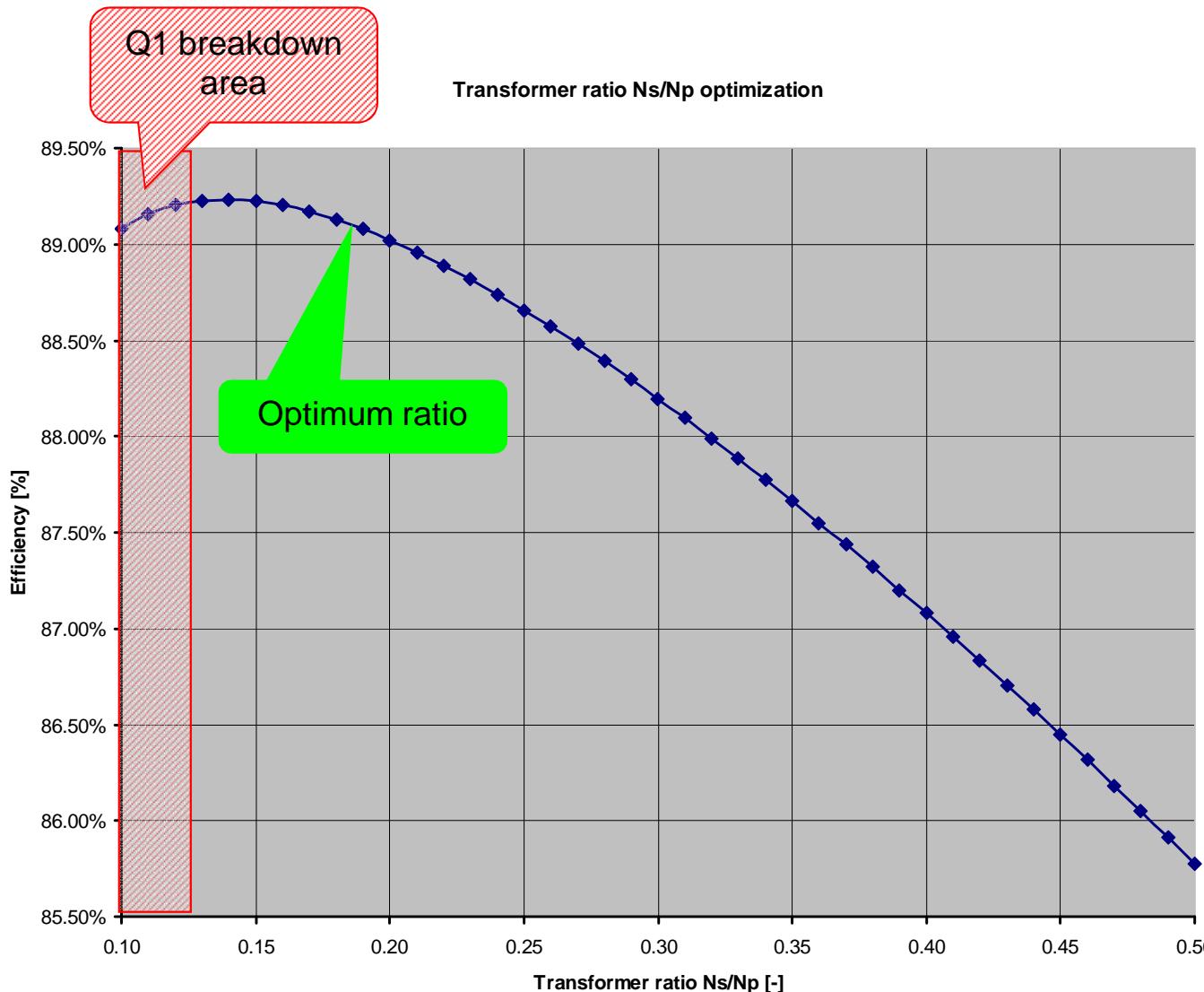
# Influence of EMI filters

- Input EMI filter contributes to the conductive losses mainly at full load and low line condition
- The high inductance 22mH or more is needed to reject the “low” frequency emissions ( below 1 MHz )
- There is needed to use two chamber CM choke or 2 CM mode chokes to reject the high frequency emissions above 10MHz
- Output EMI filter (CM choke) reject the high frequency emissions from the DC cord, only low inductance is needed → low Rdc → low conduction losses
- The most important are losses in the high inductance input common choke from the efficiency optimization point of view

Note from experiments:

There was found an influence of HF ripple at input current to the precision of measurement of input power using wattmeter **YOKOGAWA WT210**. There were measured lower input power with the connected 100uH common choke in comparison without any EMC filter. (at the same conditions) It is better always to use some EMI filter, with small Rdc to reject the error given by the noisy HF currents.

# Transformer optimization result



The optimum ratio is given by the Q1 maximum break down voltage with 15% derating factor

Decreasing the Ns/Np decreases the secondary winding losses and primary RMS current

Decreasing the Ns/Np increases the Q1 switching losses and secondary RMS current

# Improving Efficiency

- Sources of loss:

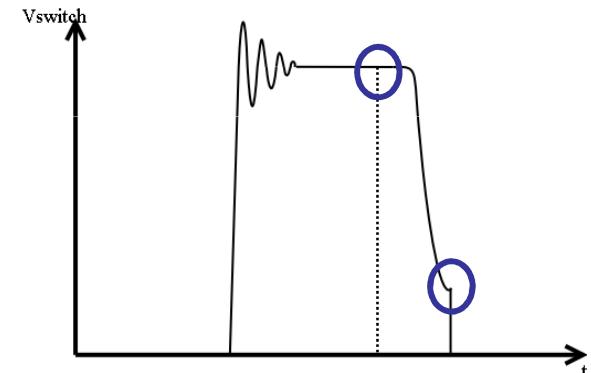
- Switching losses:

$$P_{loss(switching)} = \frac{1}{2} \cdot C_{DRAIN} \cdot V_{DRAIN(turn-off)}^2 \cdot F_{SW}$$

- Losses caused by leakage inductance:

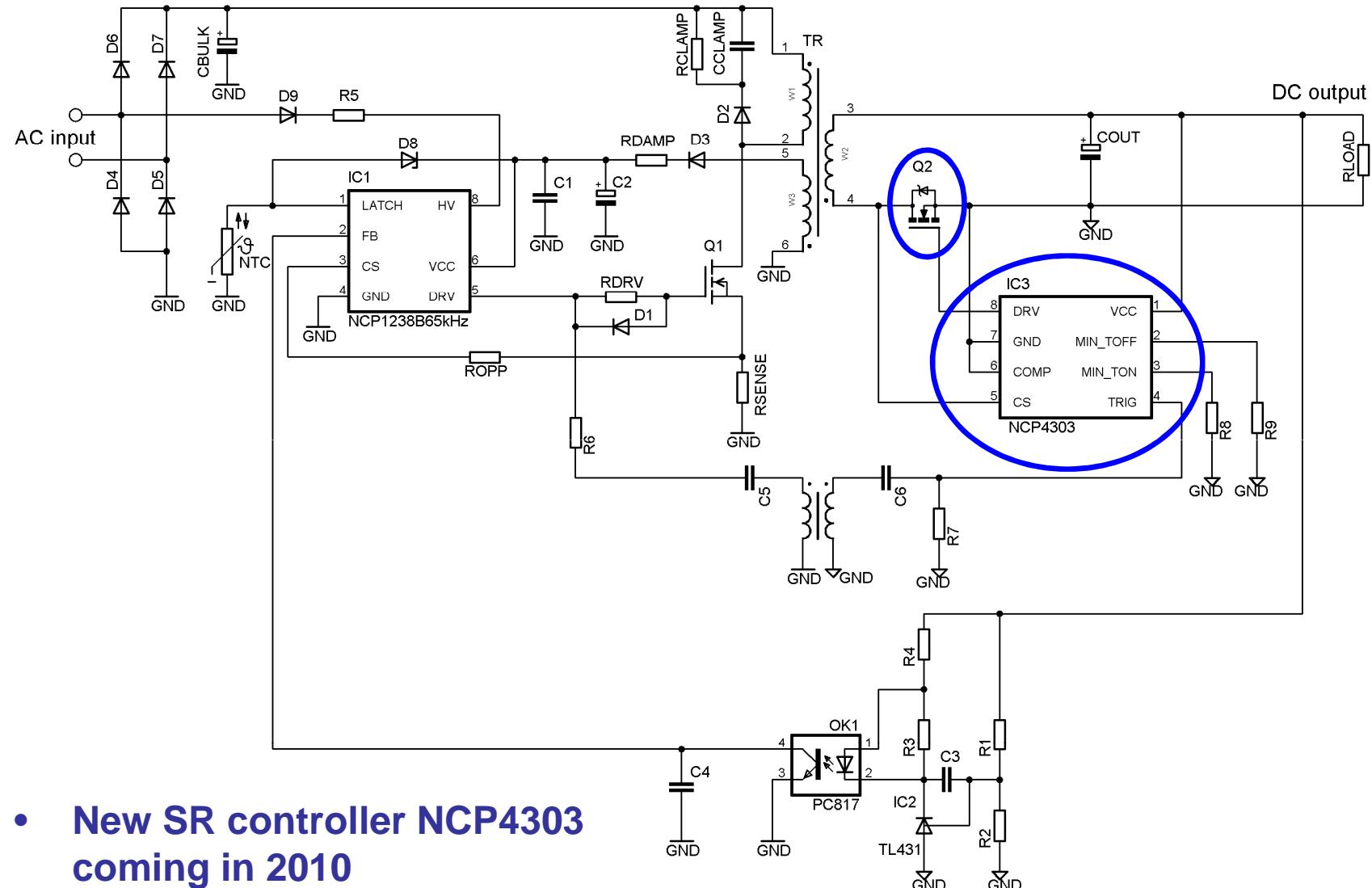
$$P_{loss(leak)} = \frac{1}{2} \cdot L_{leak} \cdot I_{peak}^2 \cdot F_{SW}$$

- Ways to improve efficiency:



- Lower the switching frequency  $F_{SW}$  → frequency foldback at light loads
  - Lower the Drain voltage at turn-off → valley switching

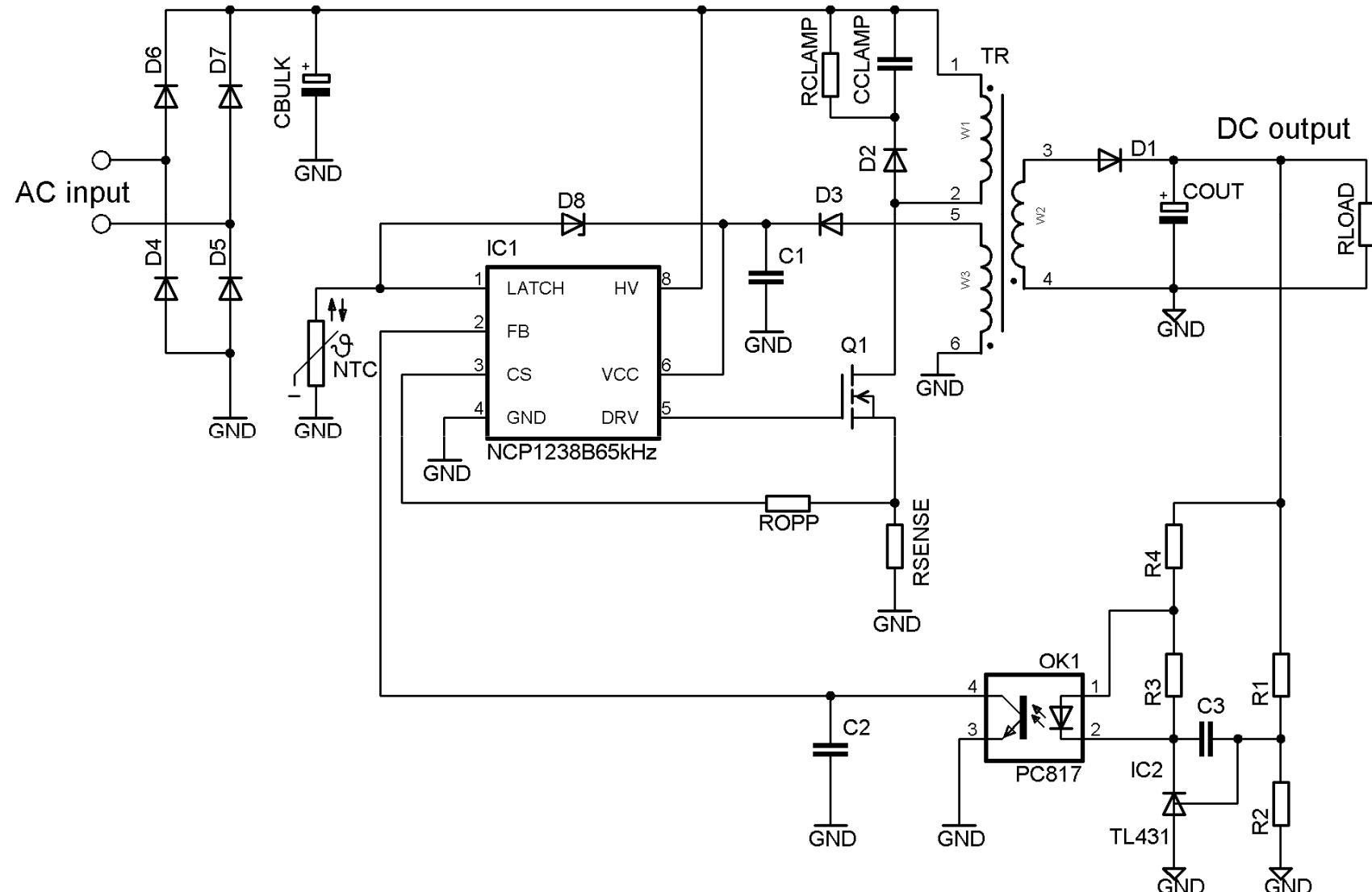
# Synchronous rectification



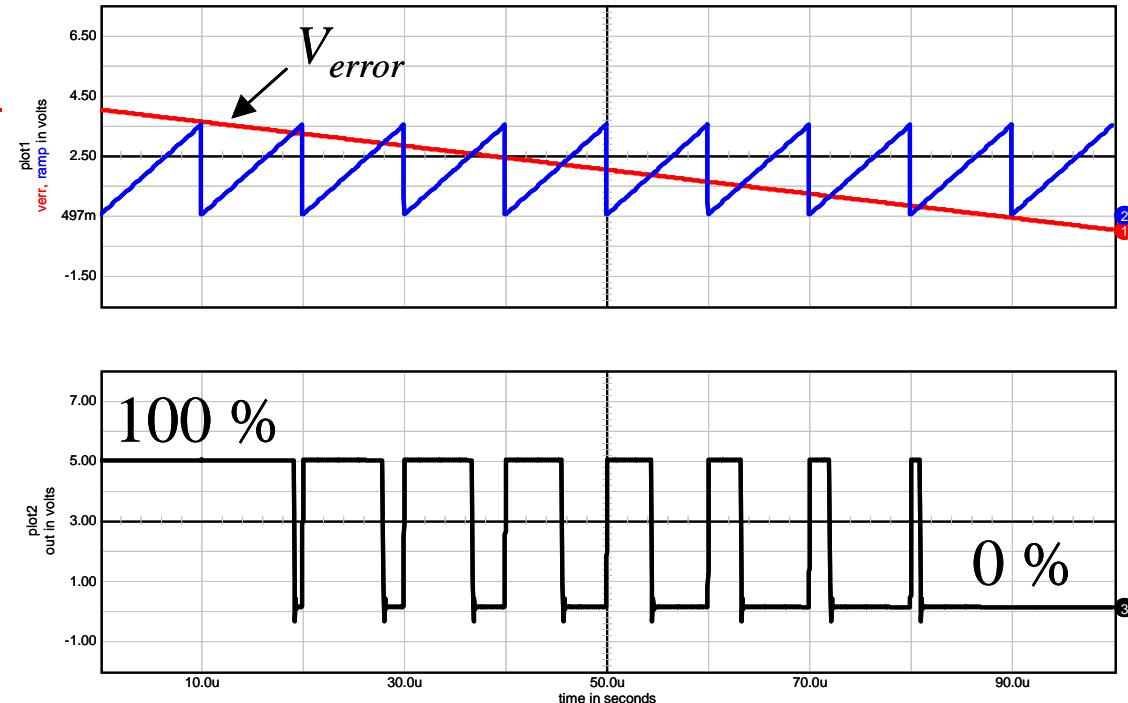
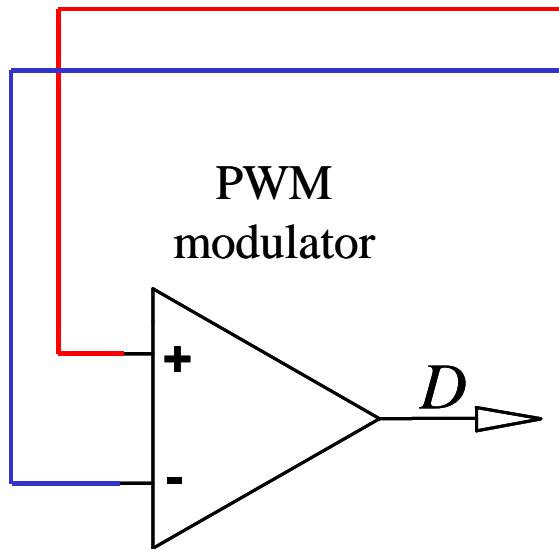
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- Demoboard example

# Application schematic

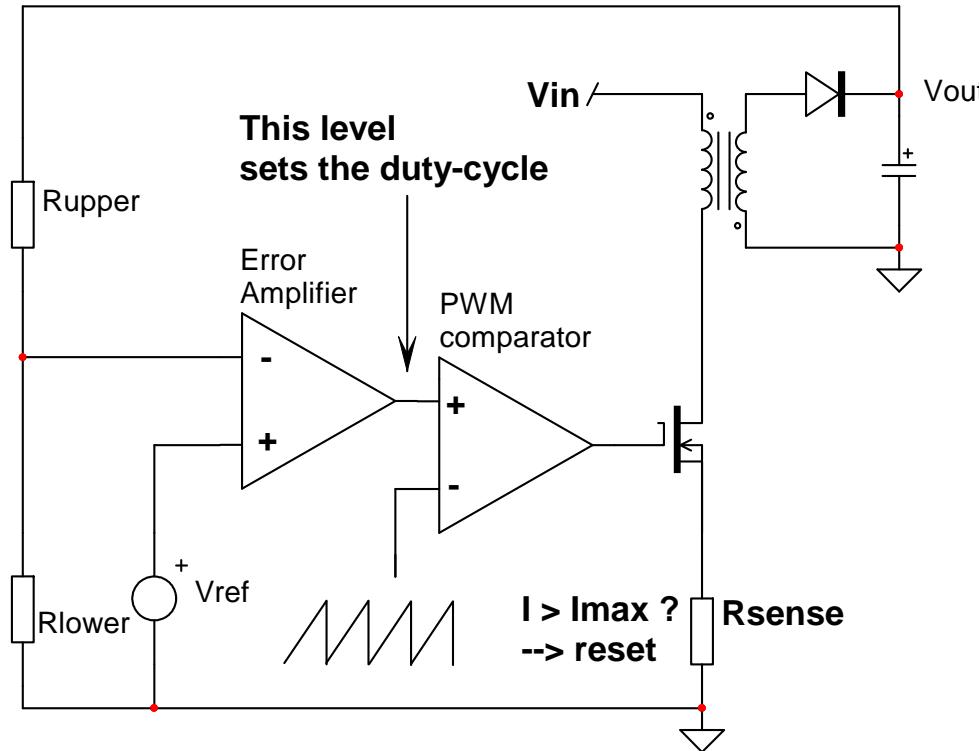


# The voltage-mode PWM generation



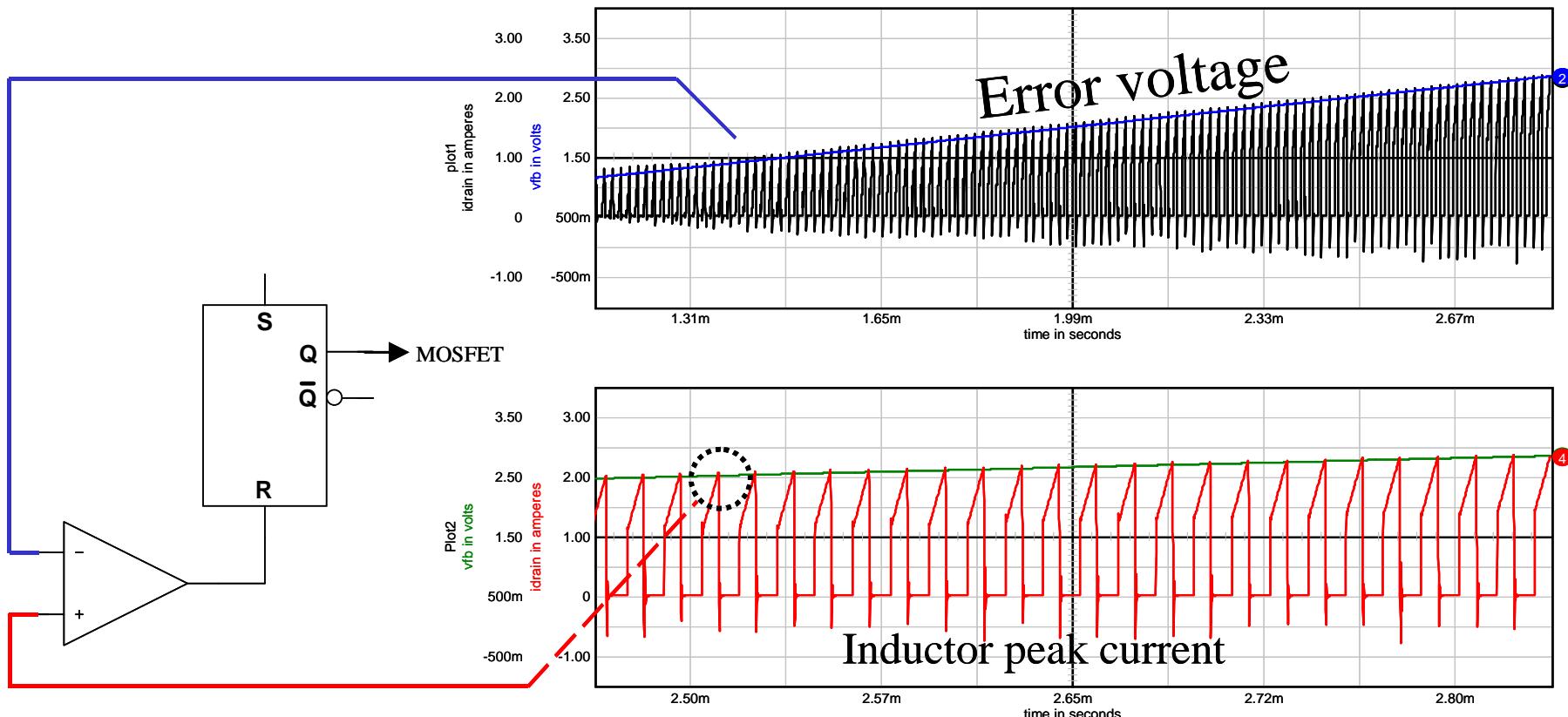
- ❑ In voltage-mode, one compares the error voltage to a fix ramp
- ❑ This is « Pulse Width Modulation » also called « PWM »

# The voltage-mode PWM generation



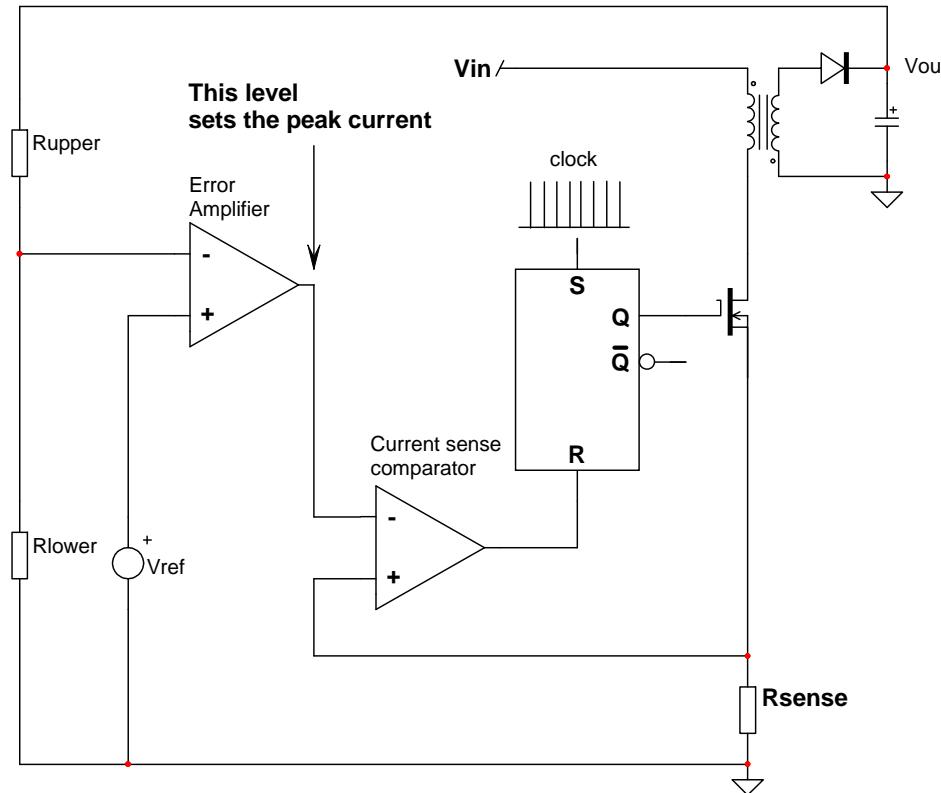
- The inductor current is sensed for safety only

# The current-mode PWM generation



- In current-mode, the error voltage fixes the peak current

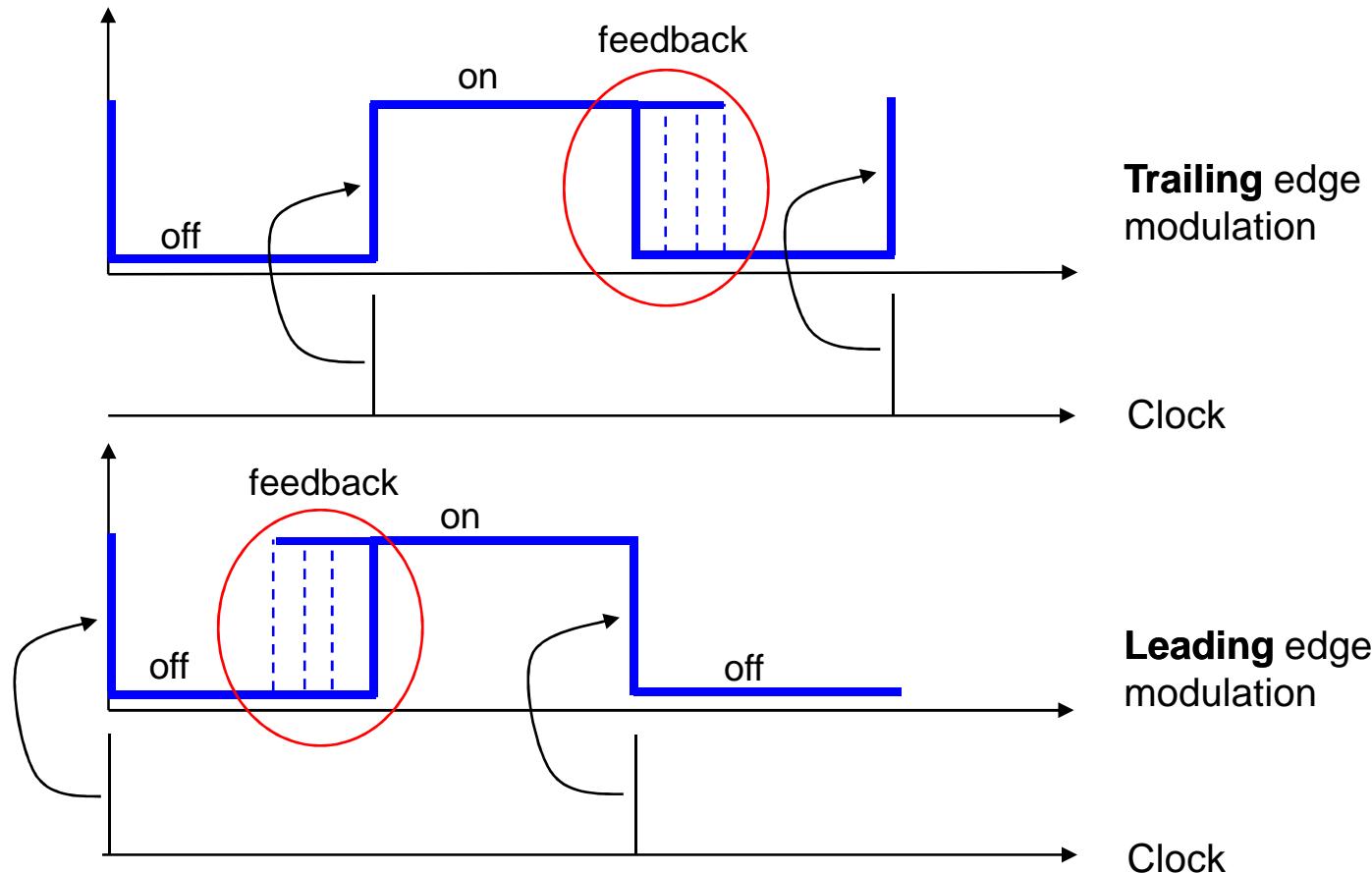
# The current-mode PWM generation



- The sense resistor provides a ***pulse-by-pulse*** current limit

# Same modulation between VM and CM

- Both modulators use trailing edge modulation



# NCP1237/38/87/88 flyback controller

## Value Proposition

The NCP1237/38/87/88 series represents the next generation of fixed frequency PWM controllers. It targets applications where cost-effectiveness, reliability, design flexibility and low standby power are compulsory.

### Unique Features

- High-voltage current source with built-in Brown-out and mains OVP
- Freq. reduction in light load conditions and skip mode
- Adjustable Over Power Protection

### Benefits

- Fewer components and rugged design
- Extremely low no-load standby power
- Simple option to alter the max. peak current set point at high line

### Application Data



	DSS	Dual OCP	Latch	Auto Recovery
NCP1237A	Yes	Yes	Yes	
NCP1237B	Yes	Yes		Yes
NCP1238A	Yes	No	Yes	
NCP1238B	Yes	No		Yes
NCP1287A	HV only	Yes	Yes	
NCP1287B	HV only	Yes		Yes
NCP1288A	HV only	No	Yes	
NCP1288B	HV only	No		Yes

Various options available depending upon end applications needs

### Others Features

- Latch-off input for severe fault conditions, allowing direct connection of NTC
- Timer-based protection: auto-recovery or latched
- Dual OCP option available
- Built-in ramp compensation
- Frequency jittering for a softened EMI signature
- Vcc operation up to 30 V

### Market & Applications

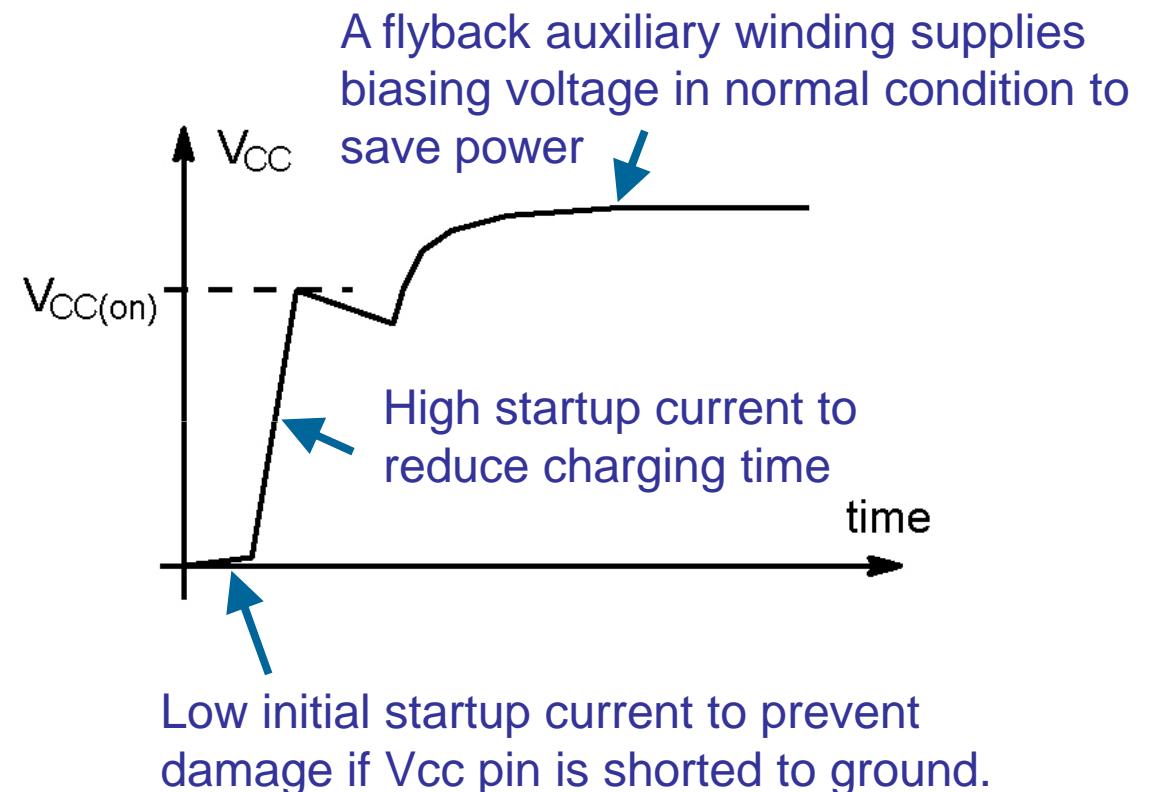
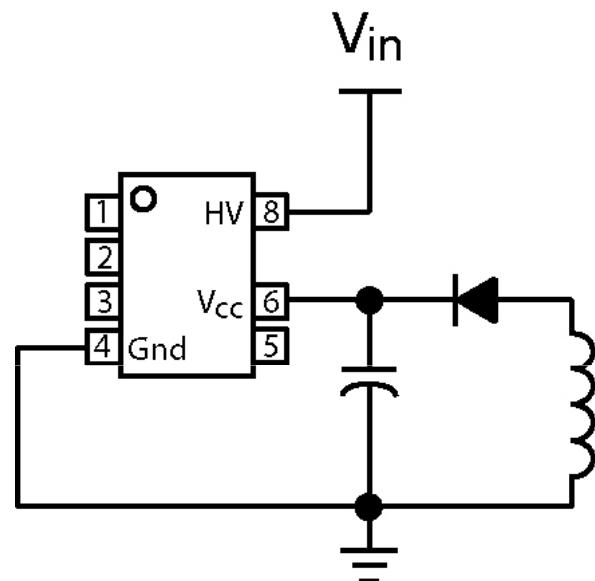
- AC-DC adapters for notebooks, LCD monitor, game console, printers
- CE applications (DVD, STB)

### Ordering & Package Information

- NCP1237/38xDR2G - NCP1287/88xDR2G
- SOIC-7 2500p per reel

Pb O, DW

# NCP1237/38/87/88 – Built-in Startup FET



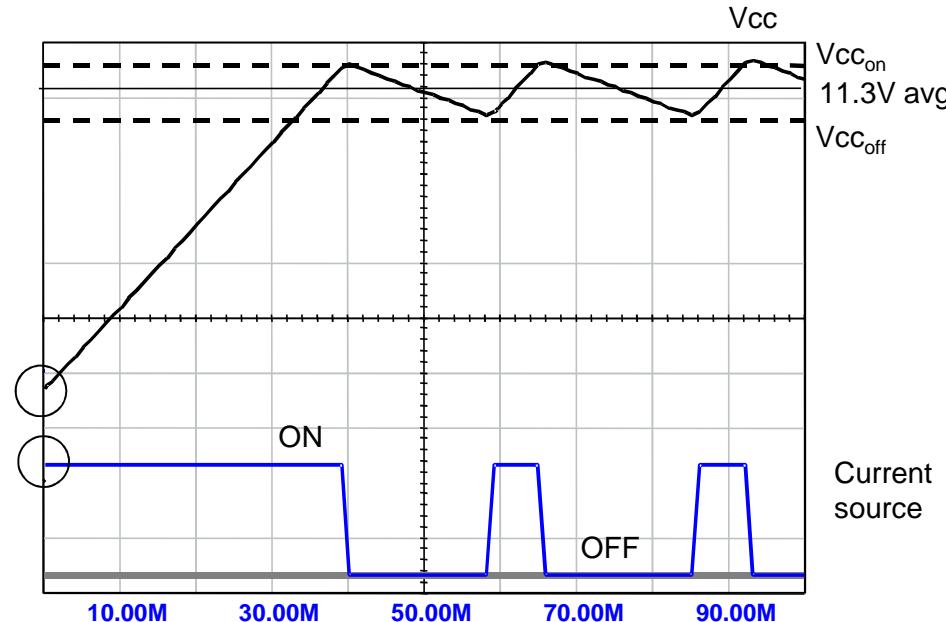
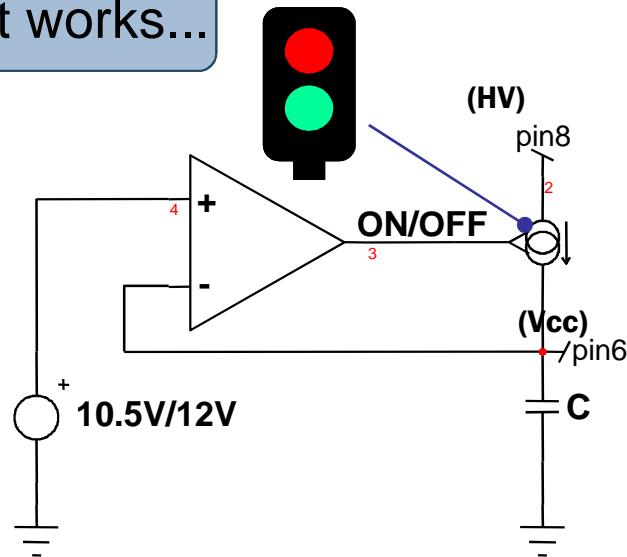
No startup resistor!



Saves PCB area  
& saves power

# NCP1237/38/87/88 – Dynamic Self Supply (optional)

How it works...



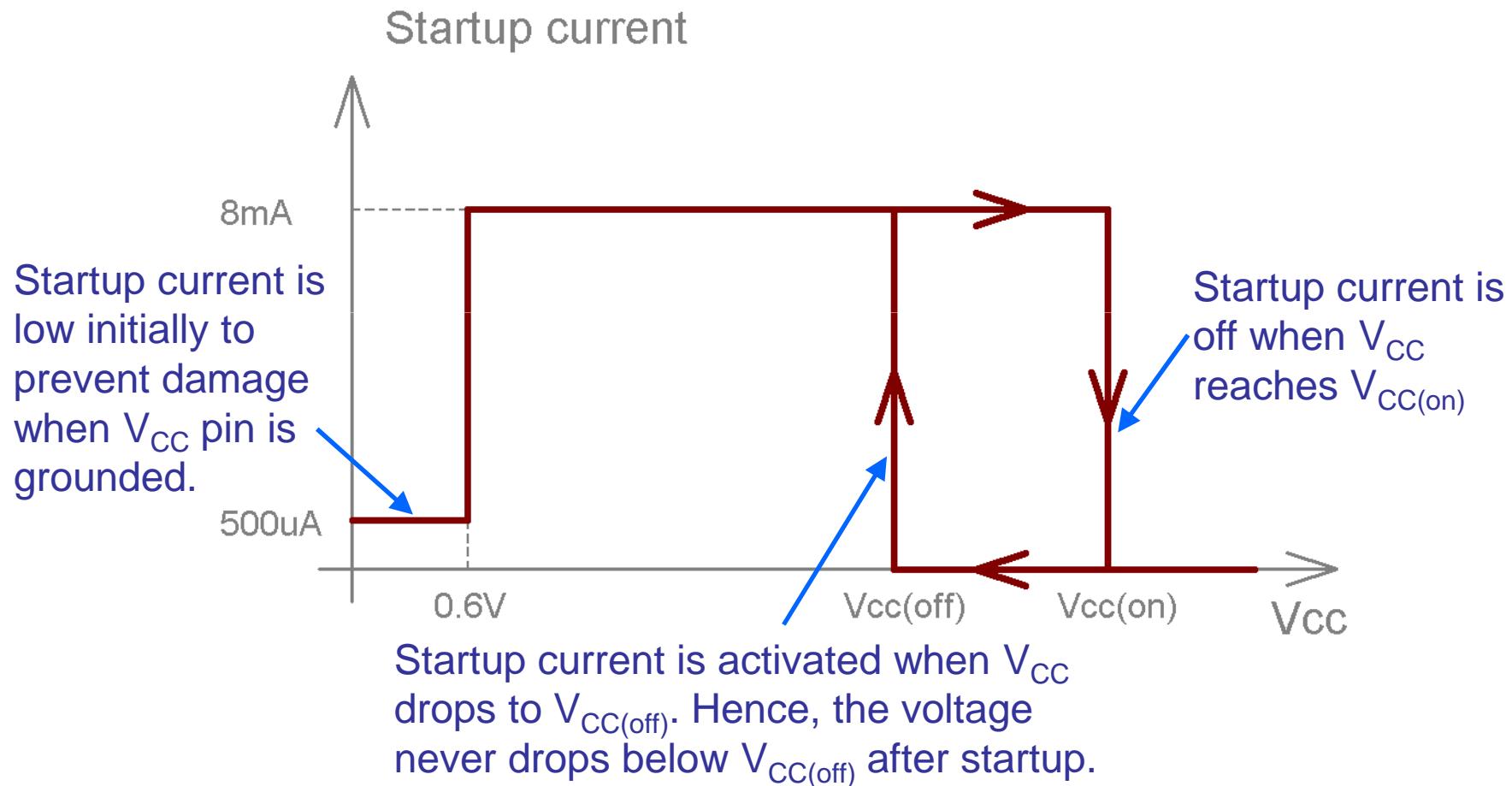
Power ON → Current Source turns ON →  $V_{cc}$  is rising; no output pulses

$V_{cc}$  reaches  $V_{cc(on)}$  → Current Source turns OFF →  $V_{cc}$  is falling; output is pulsing

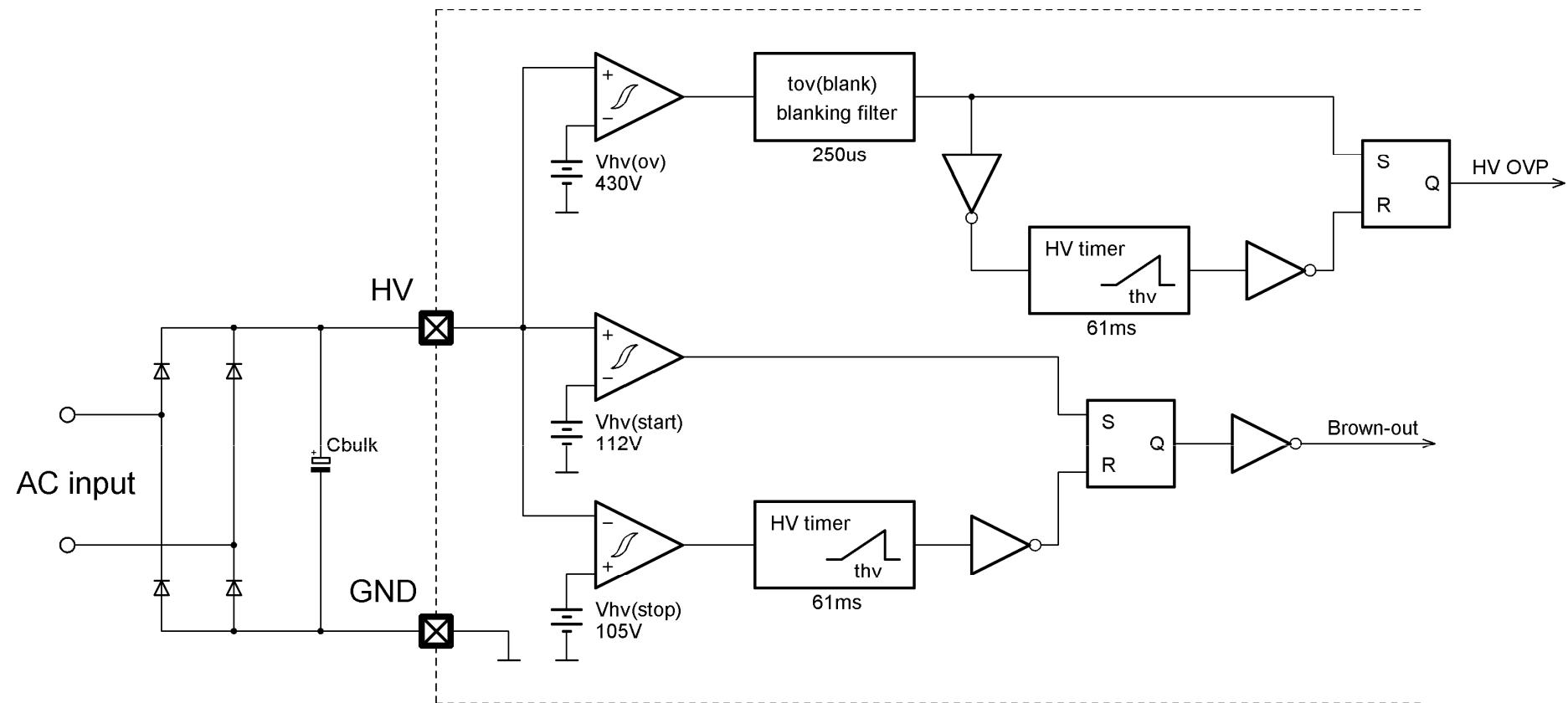
$V_{cc}$  falls to  $V_{cc(off)}$  → Current Source turns ON →  $V_{cc}$  is rising; output is pulsing

Dynamic Self-Supply No need of auxiliary winding!

# NCP1237/38/87/88 – Dual startup current level



# NCP1237/38/87/88 – Brown-out and Mains OVP

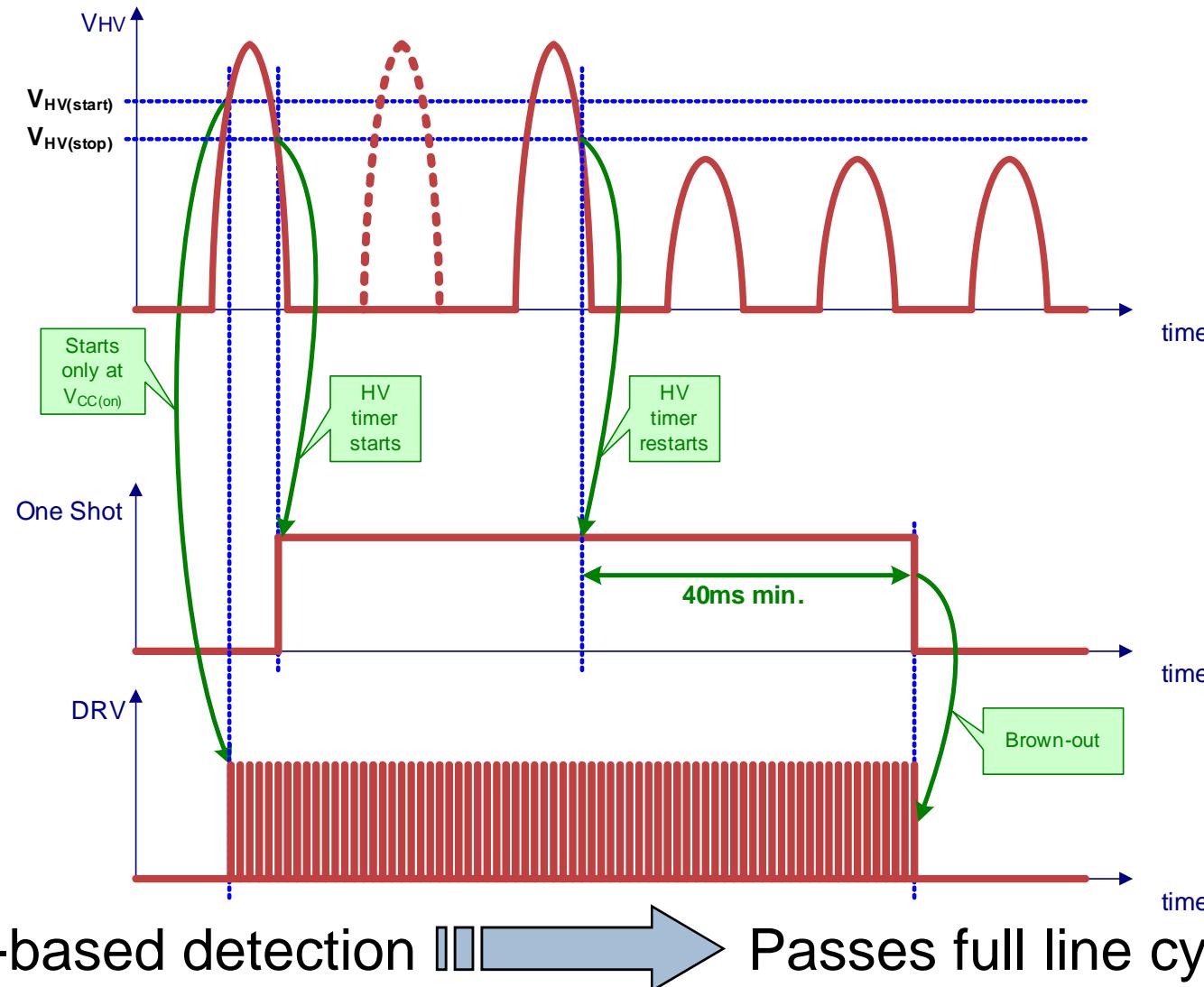


Detection independent of  
Ripple on HV pin



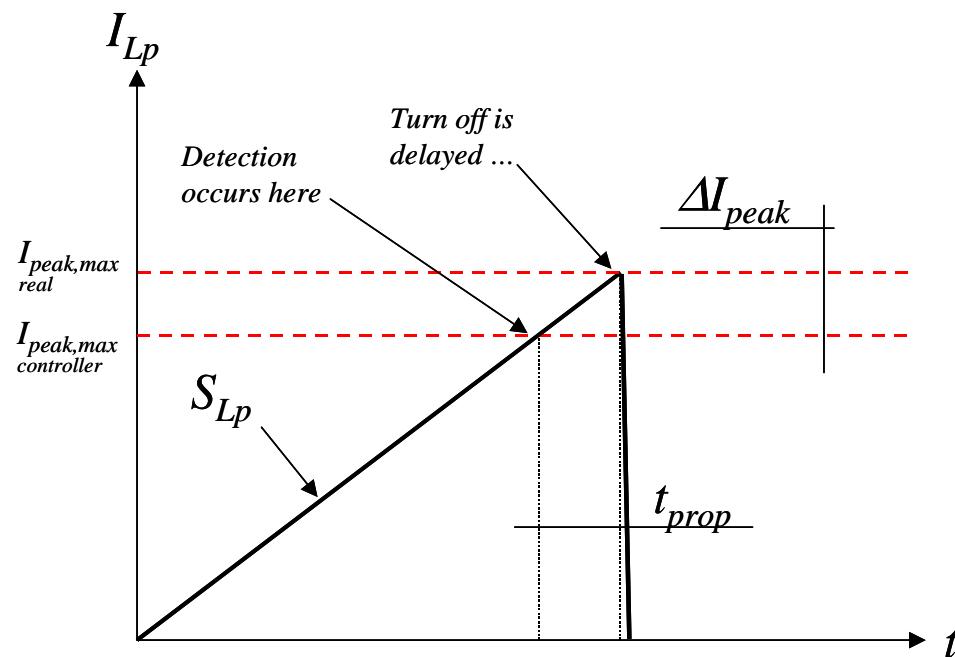
Can be connected to the  
half-wave rectified ac line

# NCP1237/38/87/88 – Brown-out and Mains OVP



Timer-based detection → Passes full line cycle drop-out

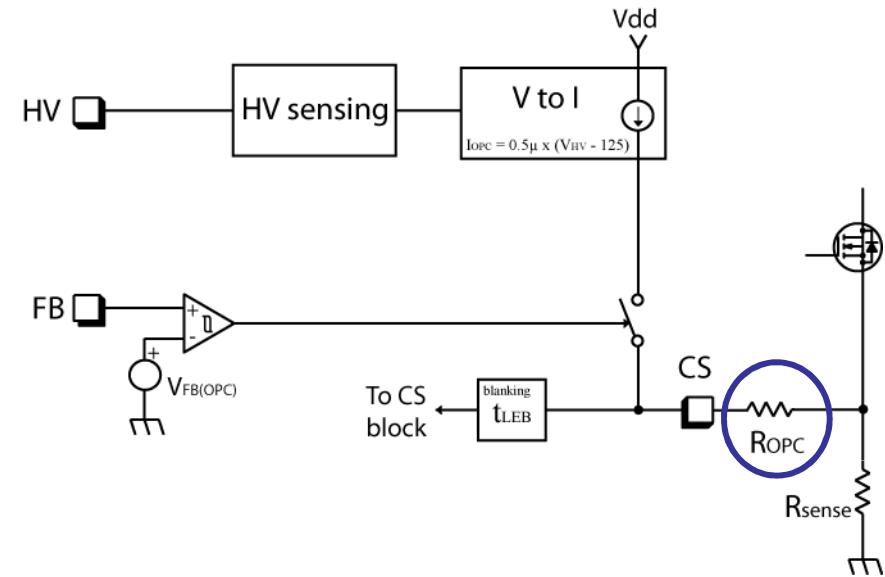
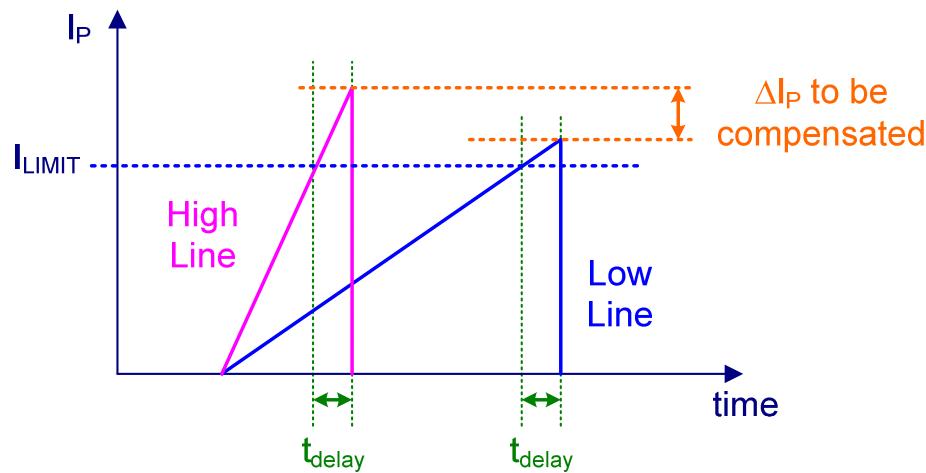
# Current overshoot: do not underestimate it...



$$I_{peak,max} = \frac{V_{sense,max}}{R_{sense}} + \frac{V_{in,max}}{L_p} t_{prop}$$

- ❑ Watch-out for clamp voltage variations, at start-up or in short-circuit
- ❑ The main problem comes from the propagation delay!

# NCP1237/38/87/88 – Over Power Protection

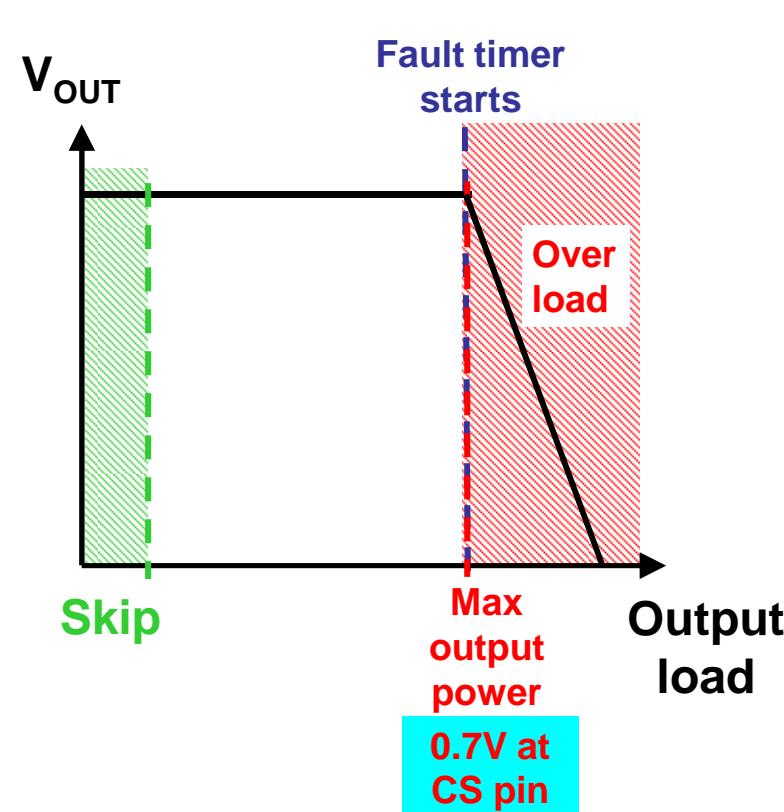


*Need to compensate for the effect of the propagation delay*

*The compensation current creates an offset on the Current Sense signal*

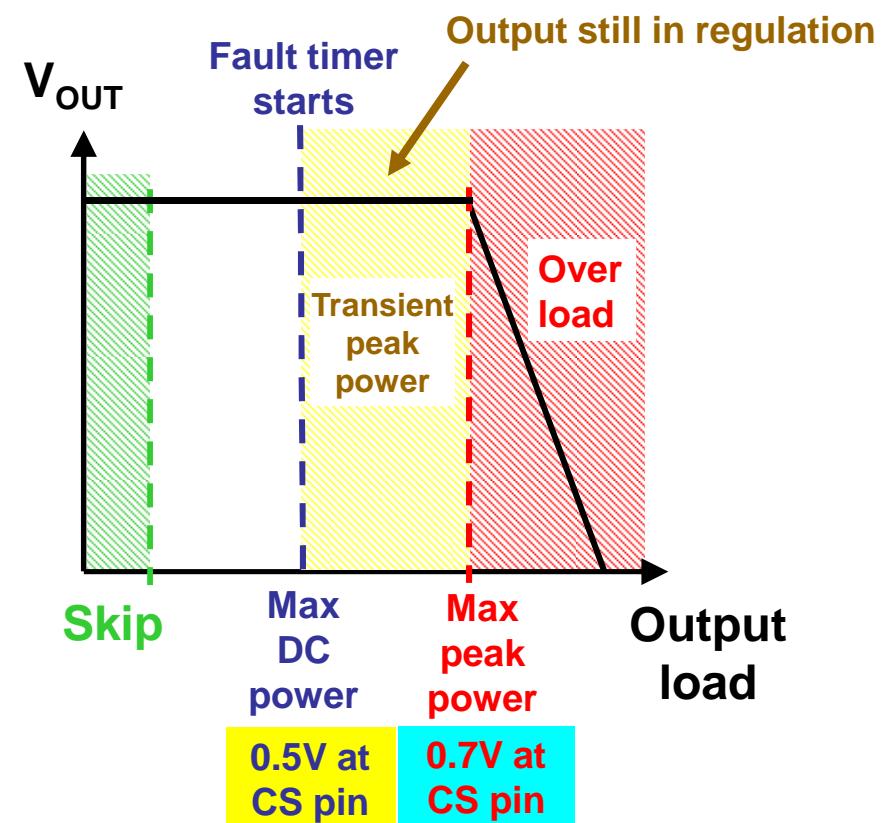
Over Power Protection → Maximum output power clamped

# NCP1237/38/87/88 – Dual OCP threshold



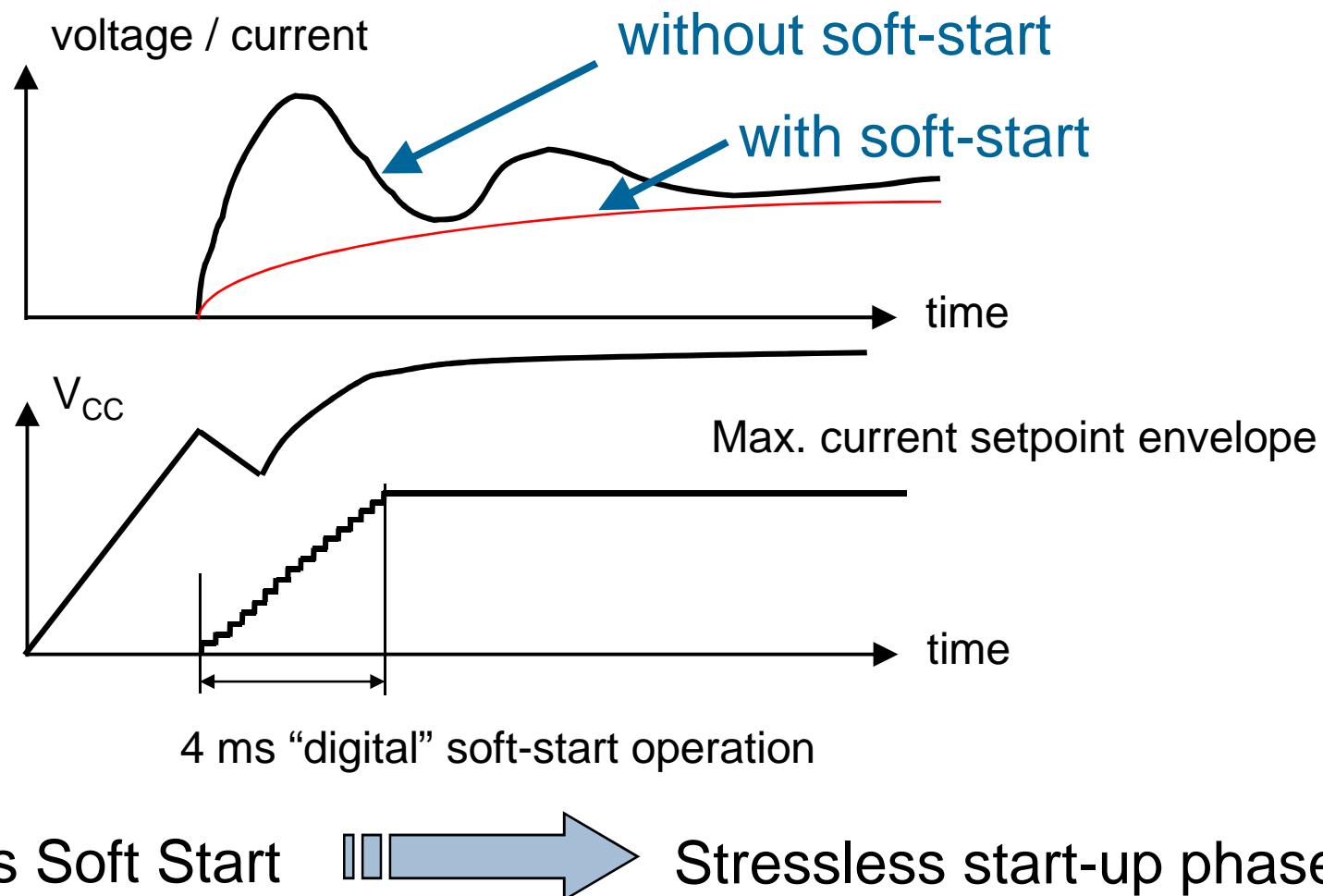
Accommodates large output power transients

These protections use the Up/Down counters, like classical analog integration.

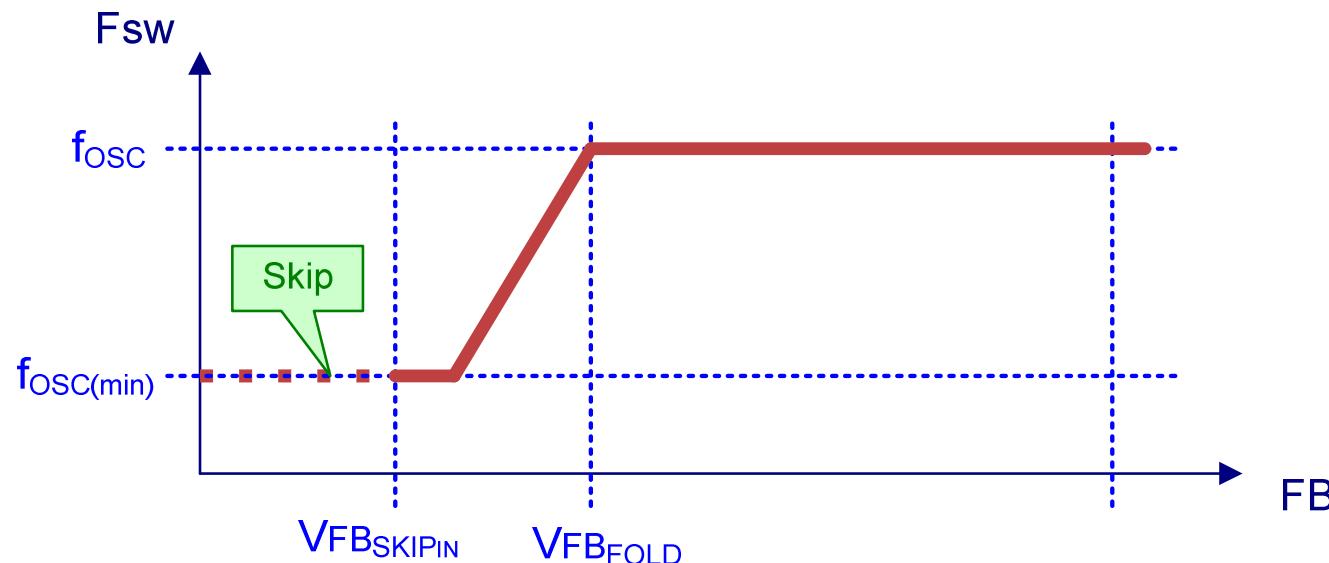


Suitable for printers

# NCP1237/38/87/88 – 4 ms Soft Start



# NCP1237/38/87/88 – Frequency Foldback



Switching frequency lowered at light load



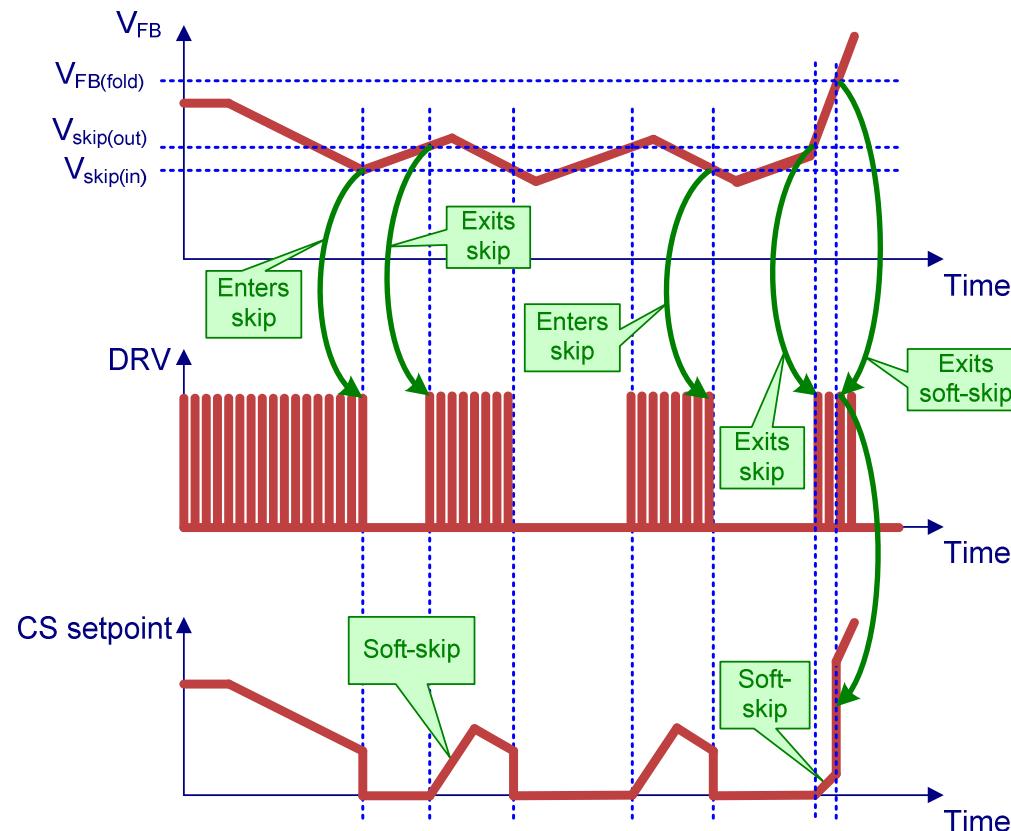
Increased efficiency

Switching frequency clamped at 25 kHz



No audible noise

# NCP1237/38/87/88 – Recover from Standby



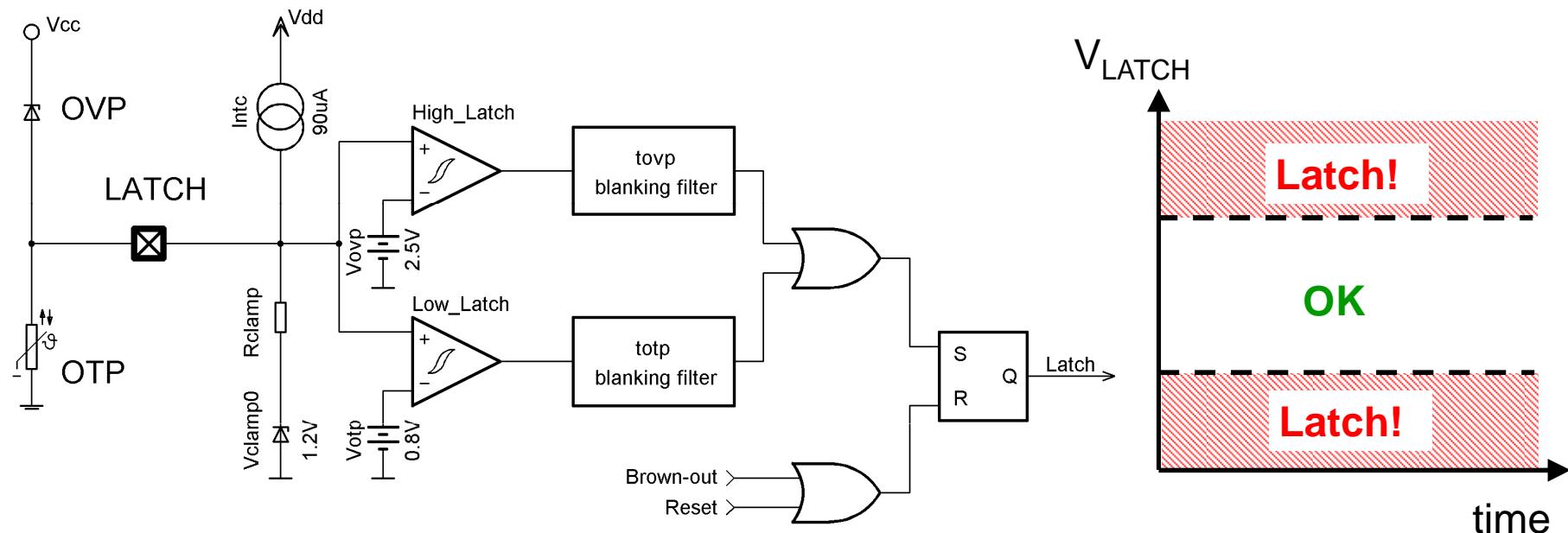
Soft-Skip mode is left as soon as the voltage on the feedback pin reaches the TLD threshold

Transient Load Detect Function (TLD)

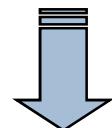


Improved Load Transient response time

# NCP1237/38/87/88 – Latch-off Protection

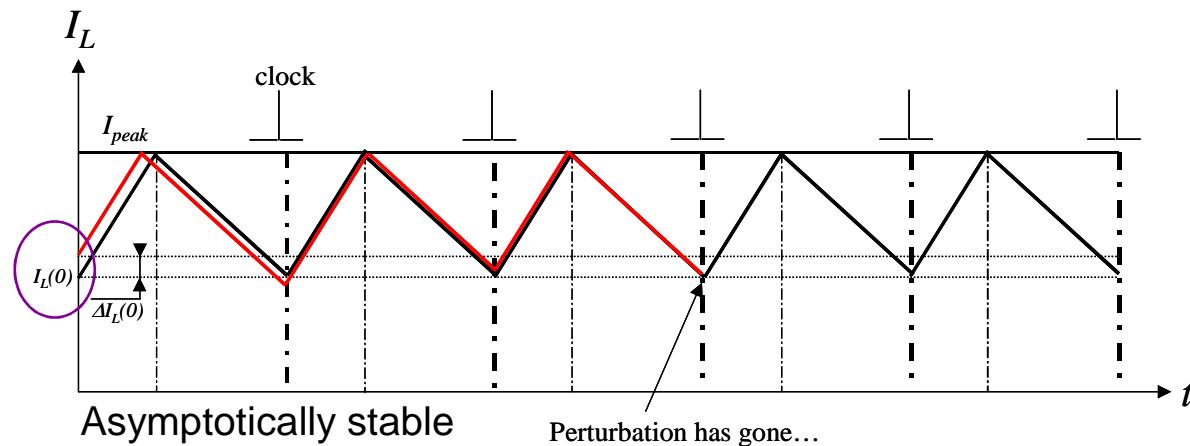


An NTC thermistor can be directly connected to the IC

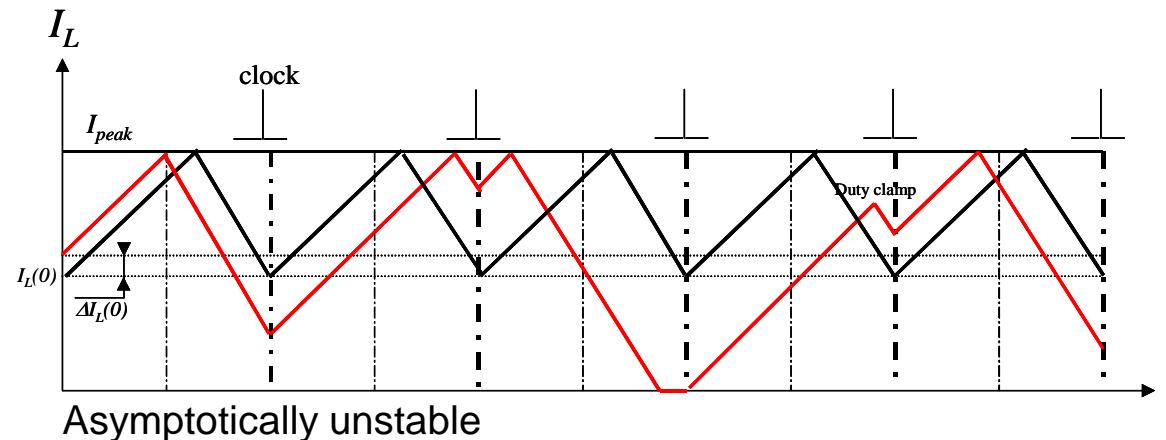


Less external components needed

# CCM operation, current instabilities

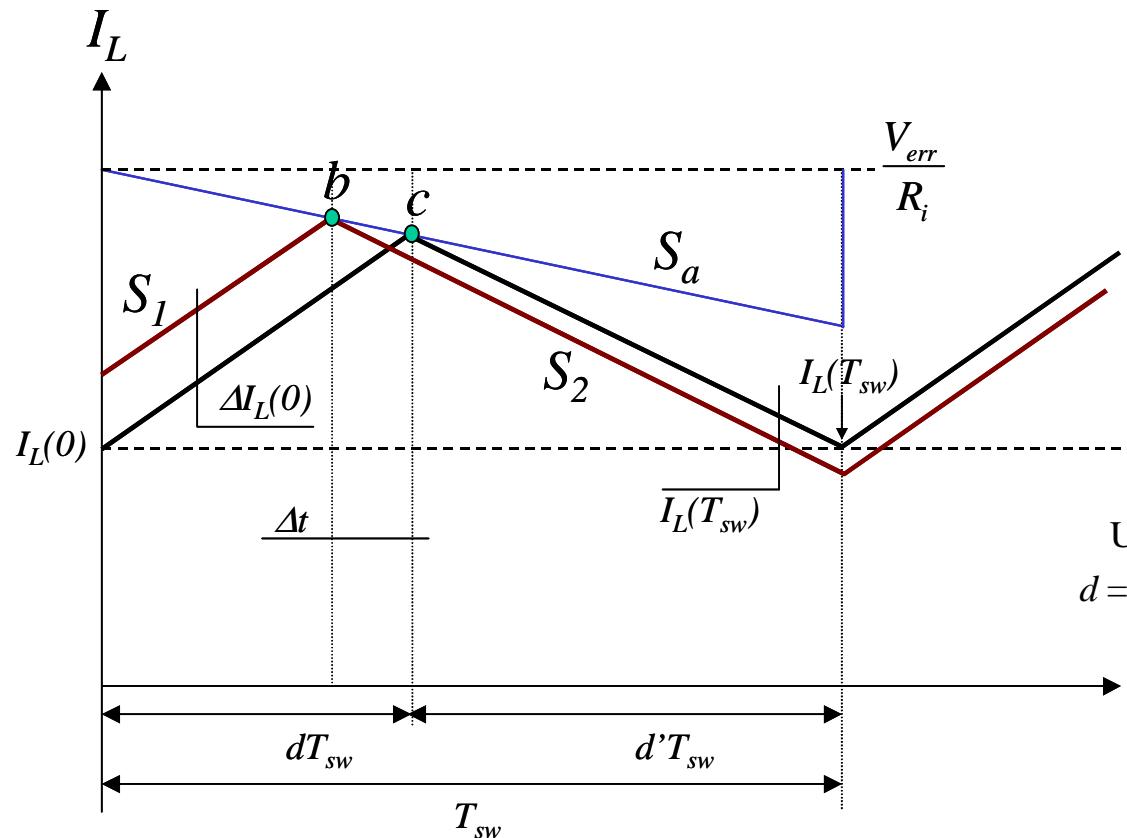


Duty-cycle < 50%



Duty-cycle > 50%

# CCM operation, curing current instabilities



Inject ramp compensation

$$\Delta I_L(nT_{sw}) = \Delta I_L(0) \left[ -\frac{1 - \frac{S_a}{S_2}}{\frac{d'}{d} + \frac{S_a}{S_2}} \right]^n = \Delta I_L(0) (-a)^n$$

Must stay below 1

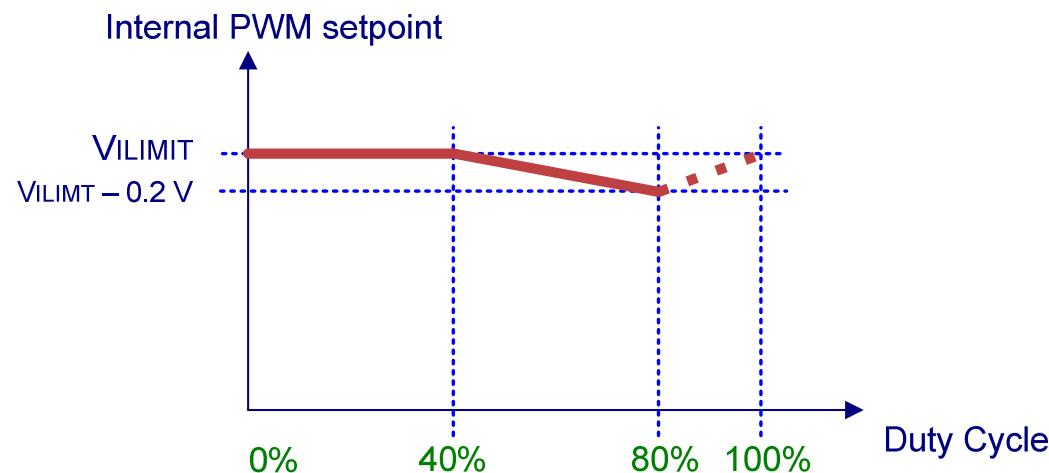
Up to  
 $d = 100\%$

$$\left| 1 - \frac{S_a}{S_2} \right| < 1$$

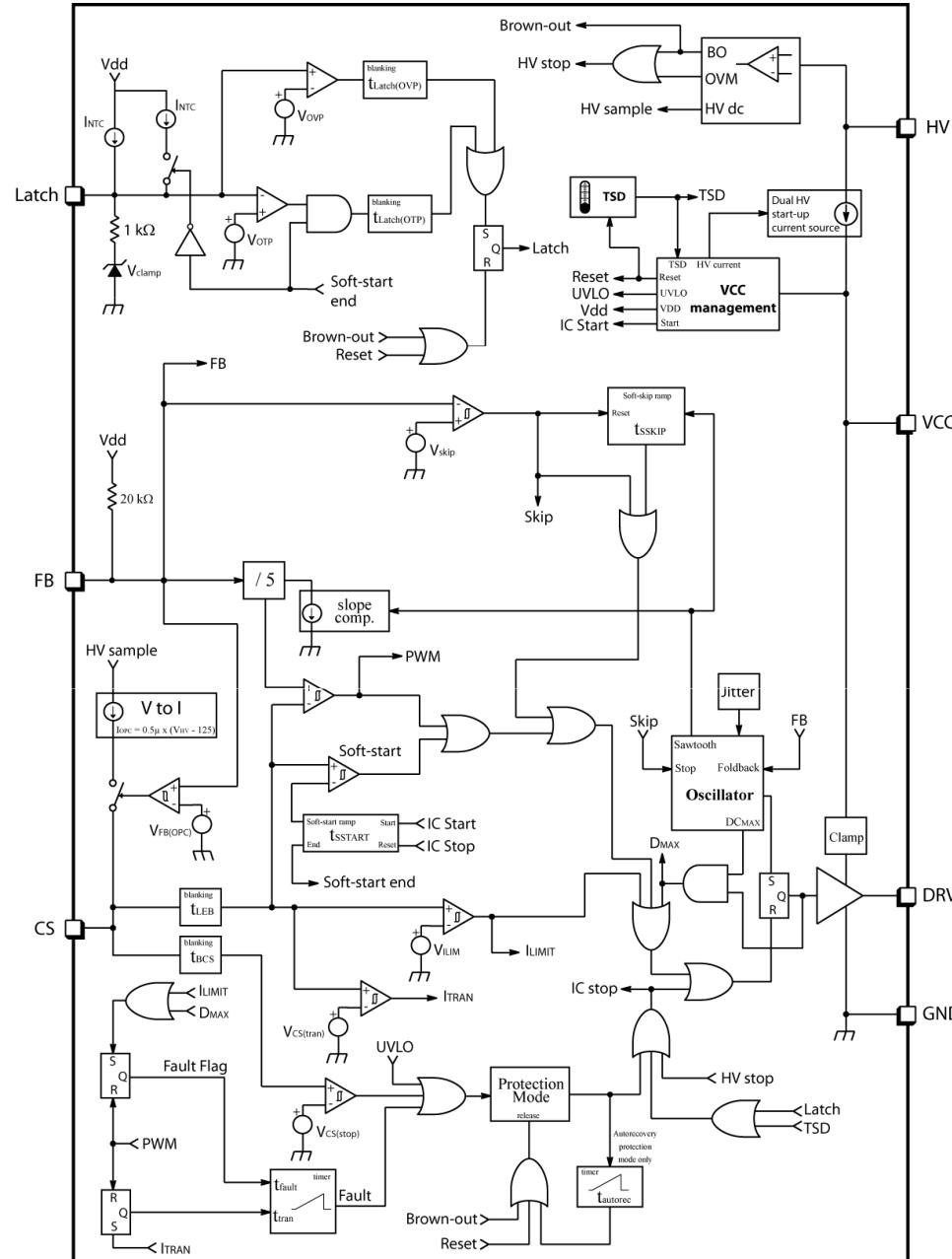
$$S_a > 50\% S_2$$

# NCP1237/38/87/88 – Slope compensation

- There is a built in slope compensation with no external setting
- The internal slope compensation is activated if the duty cycle is higher than 40%
- The amount of slope compensation is 5mV/% observed at CS pin



# Block schematic

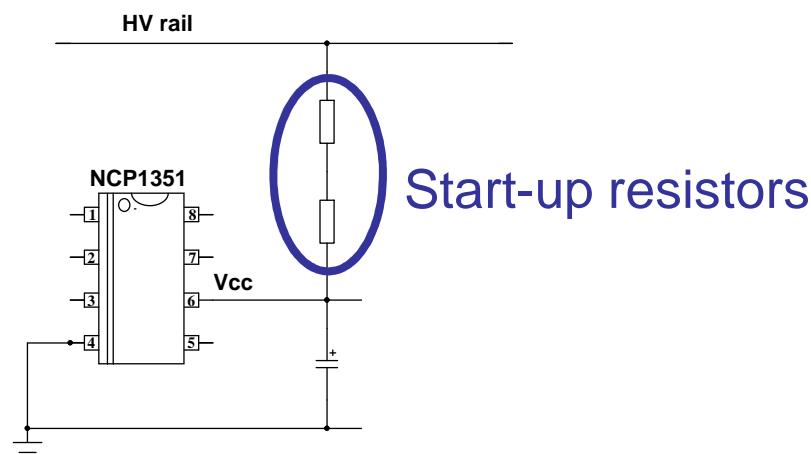


# Agenda

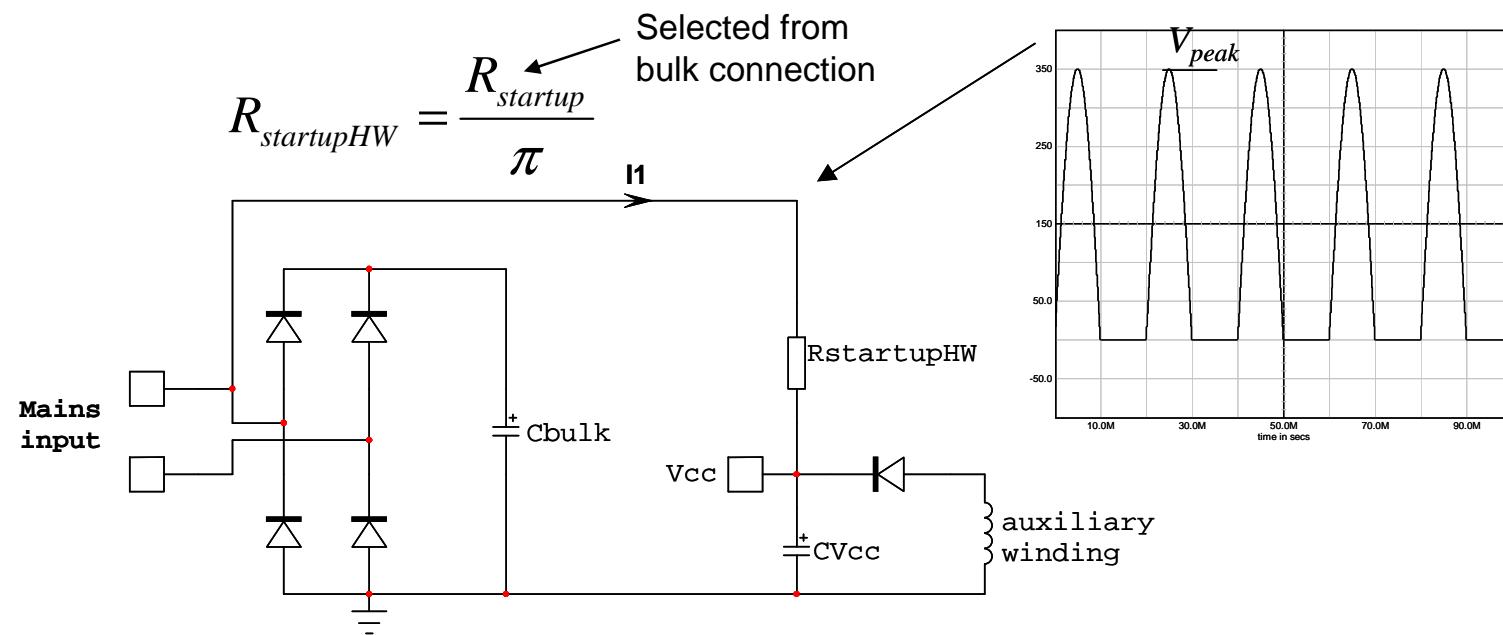
- Application and requirements
- Flyback converter basics
- Flyback converter parasitic
- Design step 1: Power stage
- Design step 2: Efficiency optimization
- Design step 3: Control mode and protections
- Design step 4: No Load Input Power
- Design step 5: Magnetics
- Design step 6: EMI
- Demoboard example

# Reducing No-load Input Power

- Static losses in the start-up circuit:
  - Start-up resistor permanently drawing current from the bulk capacitor
- Ways to lower the start-up circuit losses
  - With external start-up resistor → Extremely low start-up current
  - Integrated start-up current source → Extremely low leakage when off
  - Connect the start-up circuit to the half-wave rectified ac input

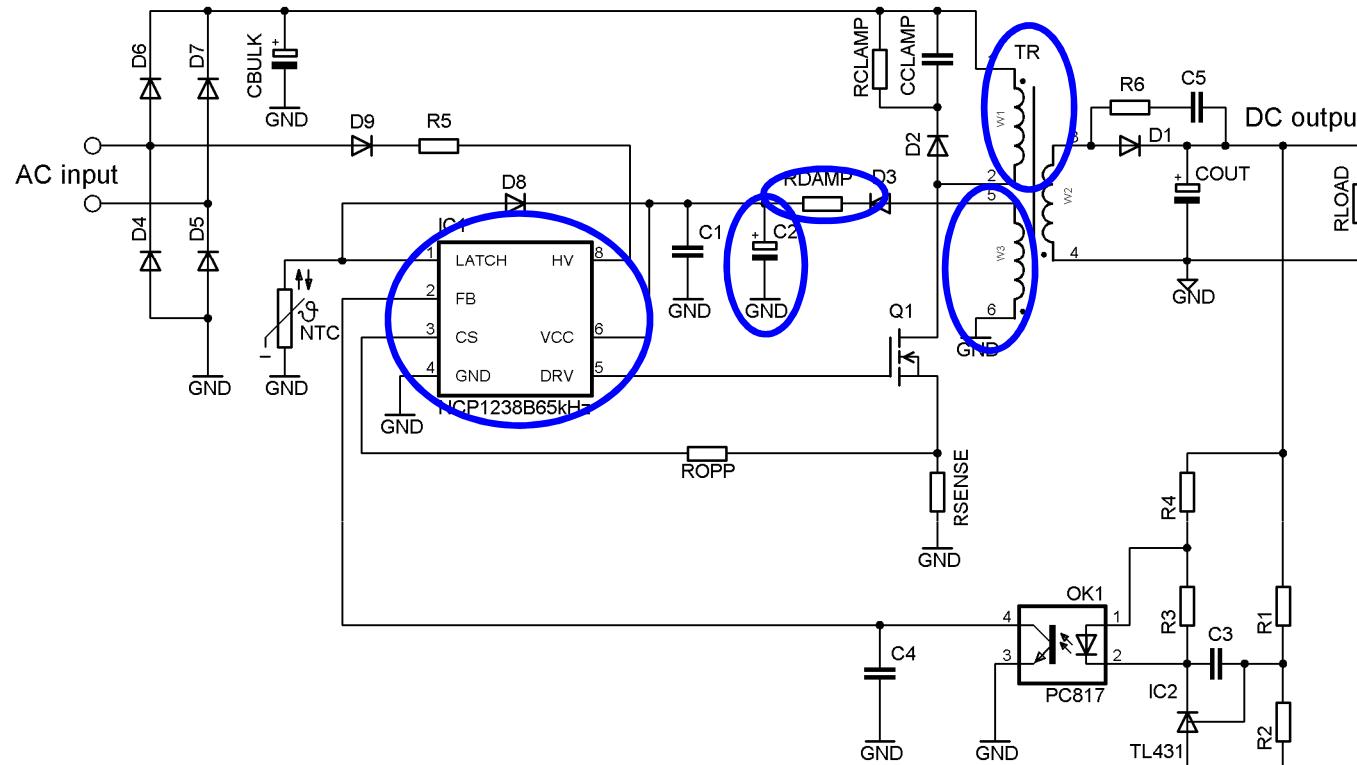


# Reducing No-load Input Power



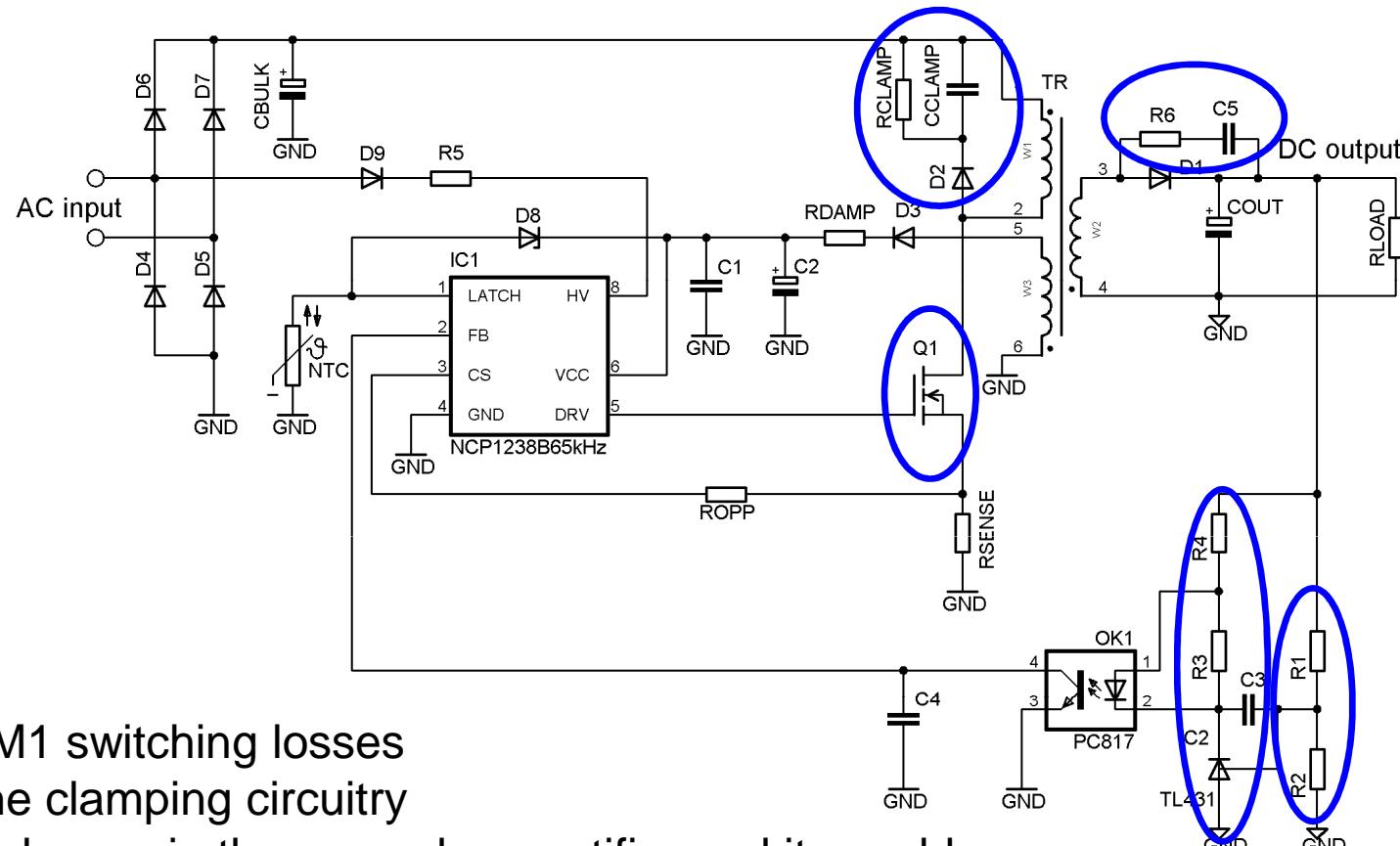
$$P_{R_{startupHW}} = \frac{P_{R_{startup}} \pi}{4} \longrightarrow \text{Brings a 21% reduction in power}$$

# No load input power reducing approach



- Decrease the transformer leakage inductance
- Use the controller IC with the frequency foldback and skip mode features
- Do not allow the DSS operation (Vcc cap increase)
- In case of low Vcc and high aux winding leakage increase the aux number of turns to disable the DSS
- Decrease the value of the Vcc damping resistor (may affect the EMI)

# No load input power reducing approach



- Lower the M1 switching losses
- Optimize the clamping circuitry
- Reduce the losses in the secondary rectifier and its snubber
- Decrease the TL431 biasing
- Decrease the cross current through the feedback resistor divider
- Set a stable operation for all loading currents
- Do not use the output voltage indication LED

# Agenda

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# Area product $A_P$

- There is defined the area product  $A_P$  [ $\text{m}^4$ ]
- Product of effective window area  $W_a$  [ $\text{m}^2$ ] and iron cross section area  $A_c$  [ $\text{m}^2$ ]

$$A_P = W_a \cdot A_c$$

- Allows fast, effective and optimal magnetic design
- Should be published in core datasheet

# Window utilization factor Ku

Ku is a measure of the amount of copper that appears in the window area of transformer. This window utilization factor is affected by:

- 1) Wire insulation
- 2) Wire lay (fill factor)
- 3) Bobbin area
- 4) Insulation required for multilayer windings or between windings

Typical values lay in range 0.35 to 0.48

# The load coefficient K<sub>load</sub>

- Flux density in magnetic should be designed at I<sub>peak</sub> with some margin (5%) to avoid saturation
- Do you really need 100% I<sub>out</sub> for 100% time??

**If not, decrease core size!!**

$$K_{load} = \frac{I_{out,RMS}}{I_{out,RMS,max}}$$

Example:

- Maximum DC output current is 3.5A, but it's only needed for transients
- The long term RMS value is only 1.75A (at least 10 min.)
- Loading coefficient is only 0.5 (not 1) → core size is smaller  
→ losses in core and in copper are smaller

# Flyback transformer core sizing

The core size can be calculated by the  $A_P$  factor in case of these inputs:

1. Converter parameters:  $L_{\text{prim}}$ ,  $I_{\text{peak}}$ ,  $K_{\text{load}}$ ,  $\delta I_r$ ,  $DC_{\max}$
2. Core maximum flux density  $B_{\max}$  considered with the hysteresis and eddy current losses at switching frequency  $F_{\text{sw}}$
3. Winding parameters (utilization factors for primary and secondary windings  $Ku_{\text{prim}}$ ,  $Ku_{\text{sec}}$ ), (current densities in primary and secondary windings  $J_{\text{prim}}$ ,  $J_{\text{sec}}$ )

$$A_P = \frac{L_{\text{prim}} \cdot I_{\text{peak}}^2}{B_{\max}} \cdot K_{\text{load}} \cdot \left( \frac{\sqrt{DC_{\max}}}{J_{\text{prim}} \cdot Ku_{\text{prim}}} + \frac{\sqrt{1 - DC_{\max}}}{J_{\text{sec}} \cdot Ku_{\text{sec}}} \right) \cdot \sqrt{\frac{\delta I_r^2 + 12}{3 \cdot (\delta I_r + 2)^2}}$$

Now the appropriate core can be selected from the vendor products list by the  $A_P$  factor .

# Windings design

- Number of turns of primary winding

$$NT_{prim} = \frac{L_{prim} \cdot I_{peak}}{B_{max} \cdot A_c}$$

- Number of turns of secondary winding

$$NT_{sec} = N \cdot NT_{prim}$$

- Number of turns of auxiliary winding

$$NT_{aux} = \frac{V_{CC} + V_{f,Vcc}}{V_{out} + V_{f,diode}} \cdot NT_{sec}$$

# Air gap length $l_g$

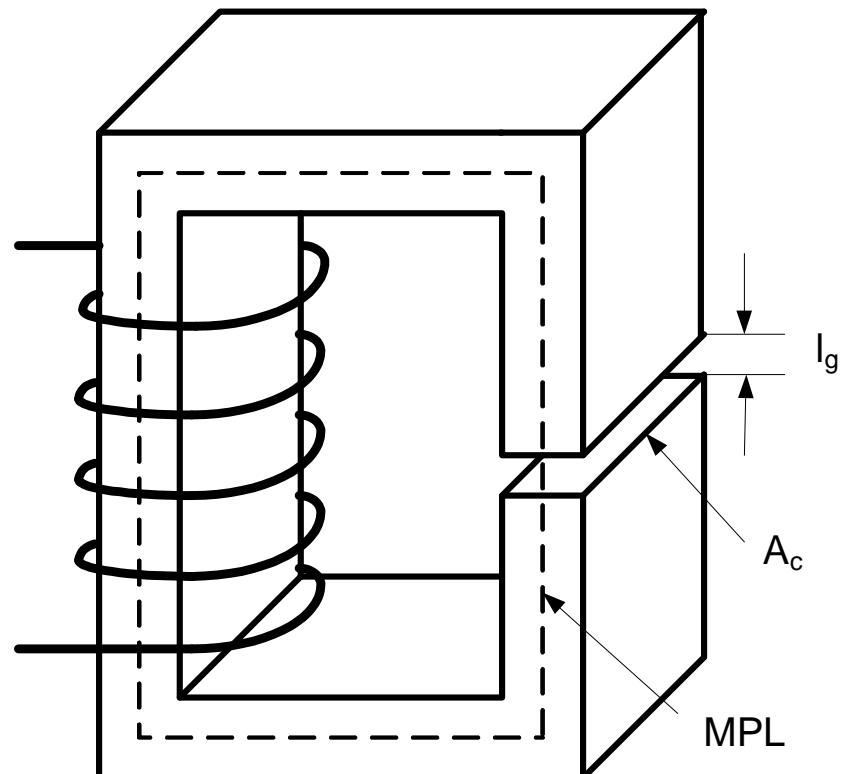
$$l_g = \frac{N \cdot \mu_0 \cdot I_{peak}}{B_{max}} - \frac{MPL}{\mu_r} \quad \text{in case of } l_g \ll MPL$$

MPL – core magnetic path length

$\mu_0$  - permeability of vacuum

$\mu_r$  - permeability of core

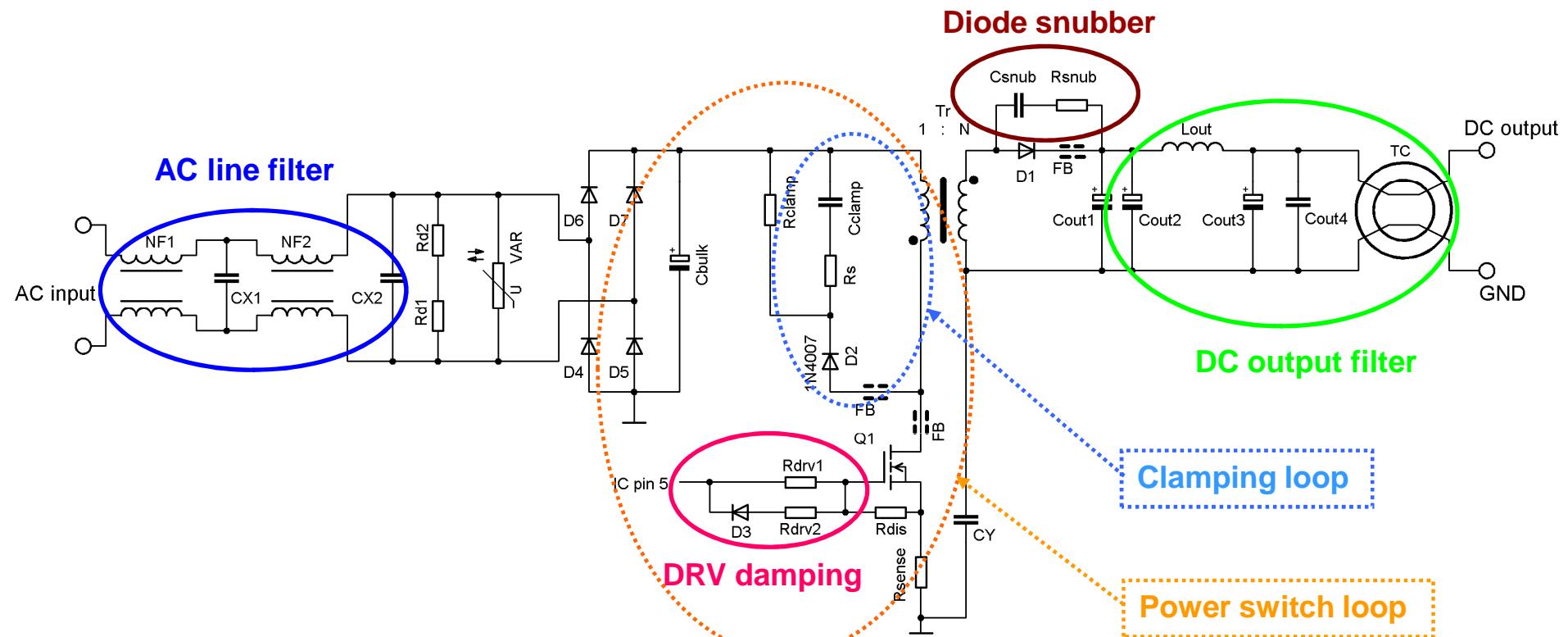
In case an EE, RM or pot core is used, divide the calculated  $l_g$  by factor 2, because your core has 2 air gaps in magnetic path



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# How to improve EMI of my design?



- All switching loops with RF currents should have small area
- Divide input AC filter at two chokes to decrease the parasitic capacitance coupling
- CY – closes the current loop for the RF currents injected via transformer

# Diode snubber design

- Snubber resistance value should be close to the characteristic impedance of ringing circuitry

$$R_{snubber} = \sqrt{\frac{L_{leak,SEC}}{C_d}}$$

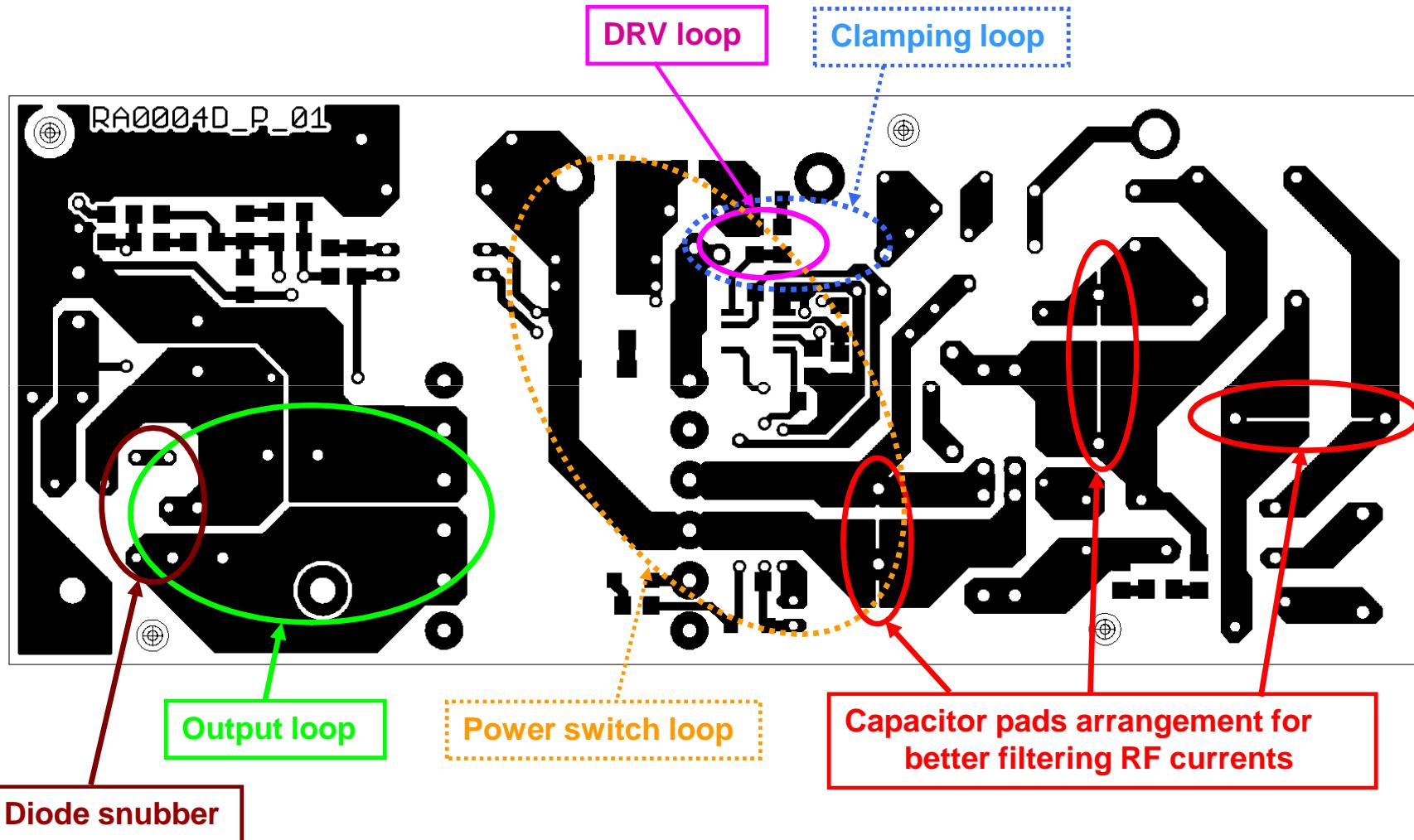
$L_{leak,SEC}$  –the transformer leakage inductance observed from secondary side

$C_d$  – reverse direction diode capacitance

- RC time constant of the snubber should be small compared to the switching period but long compared to the voltage rise time

$$C_{snubber} \approx 3 \div 4 \cdot C_d$$

# PCB Layout tips

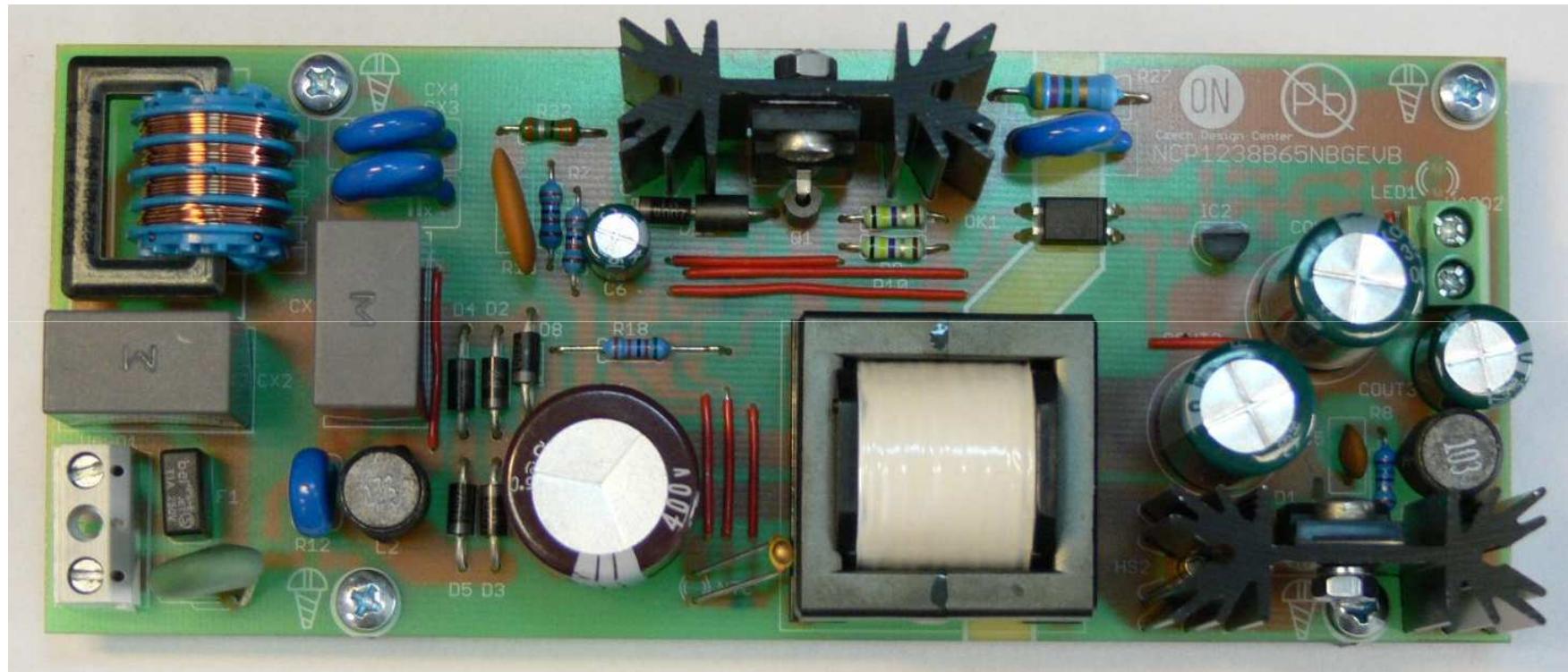


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# Preliminary demonstration board

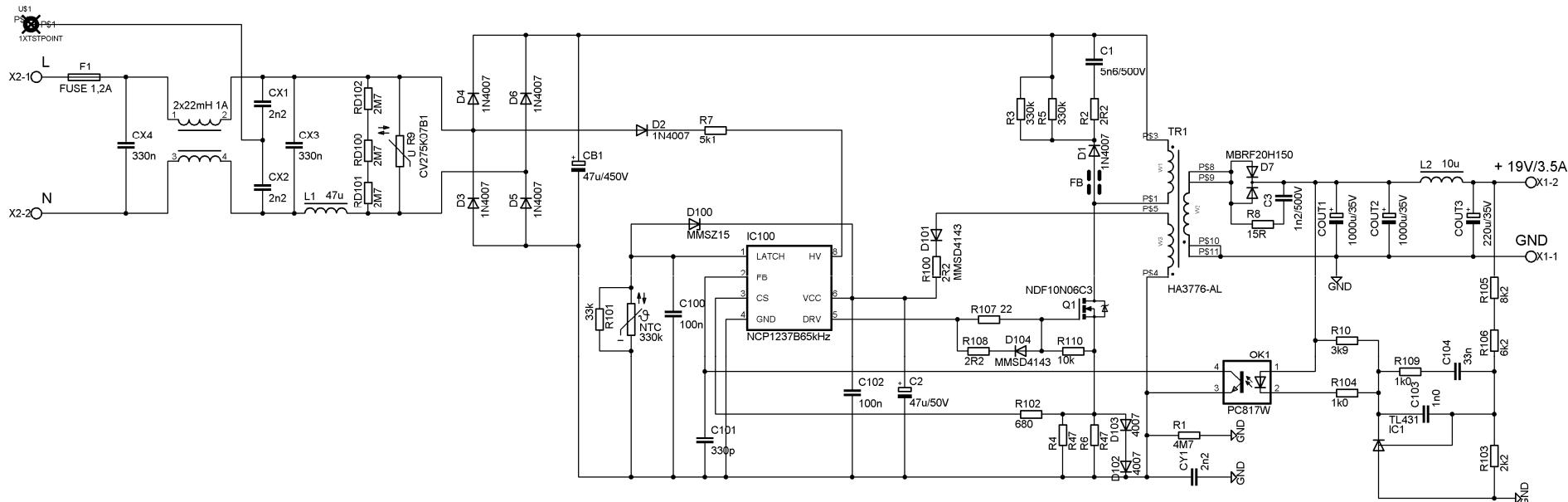
A typical 65 W notebook adapter (19 V output)



(optimized for EPS 2.0)

# Schematic of preliminary demonstration board

A typical 65 W notebook adapter (19 V output)



(optimized for EPS 2.0)

## Demonstration board Efficiency (measured with DC cord)

The DC cord length is 1.05m and copper cross sec. is 0.75mm<sup>2</sup>

$V_{IN}$ % of $P_{OUTnom}$	115 Vac/60Hz	230 Vac/60Hz
100 % (65 W)	87.10 %	87.37 %
75 % (49 W)	87.52 %	87.63 %
50 % (32 W)	87.54 %	87.88 %
25 % (16 W)	87.79 %	85.96 %

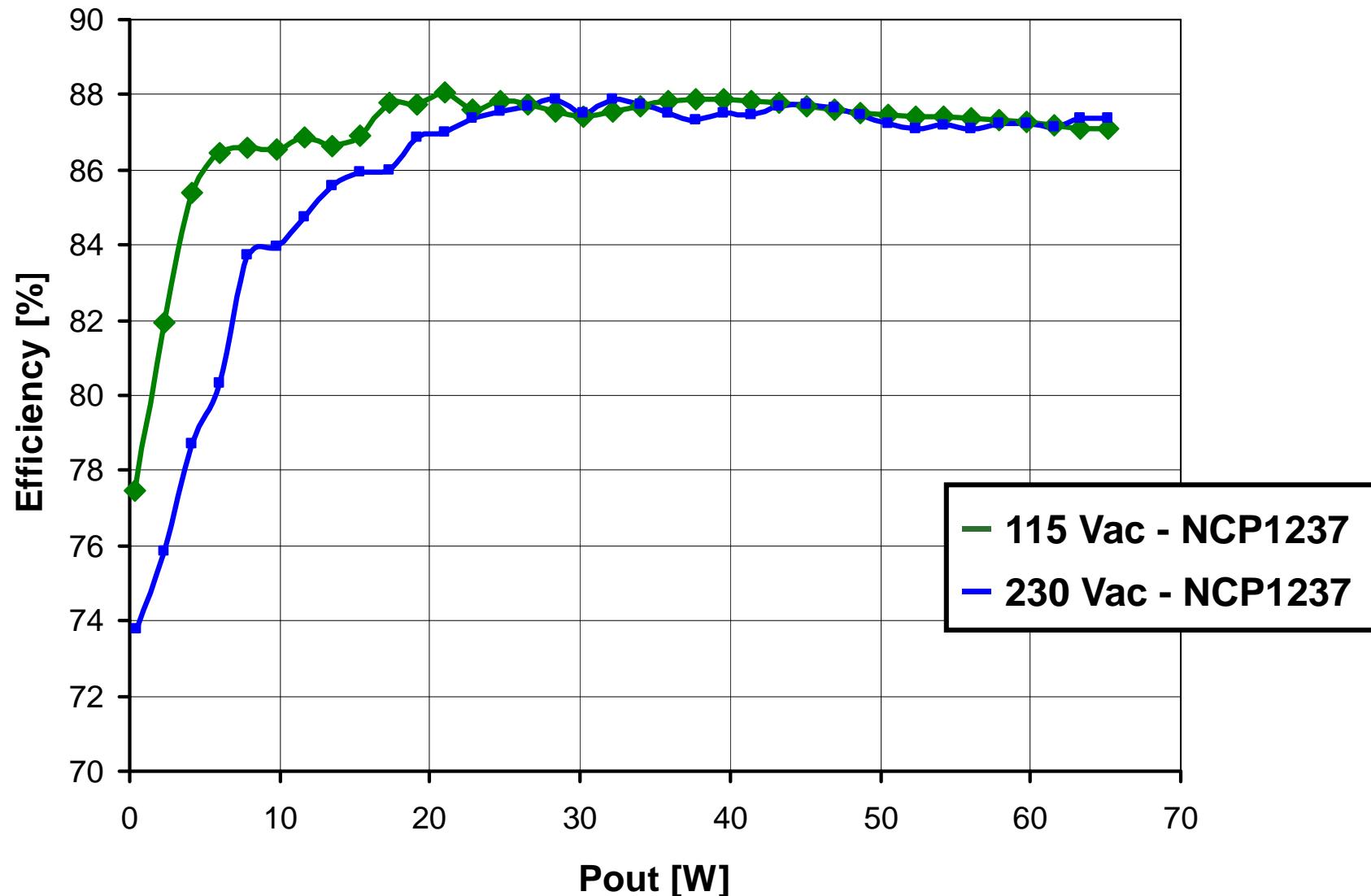
Average at 115Vac is 87.32% and at 230 Vac is 87.21 %

# Demonstration board Standby Power

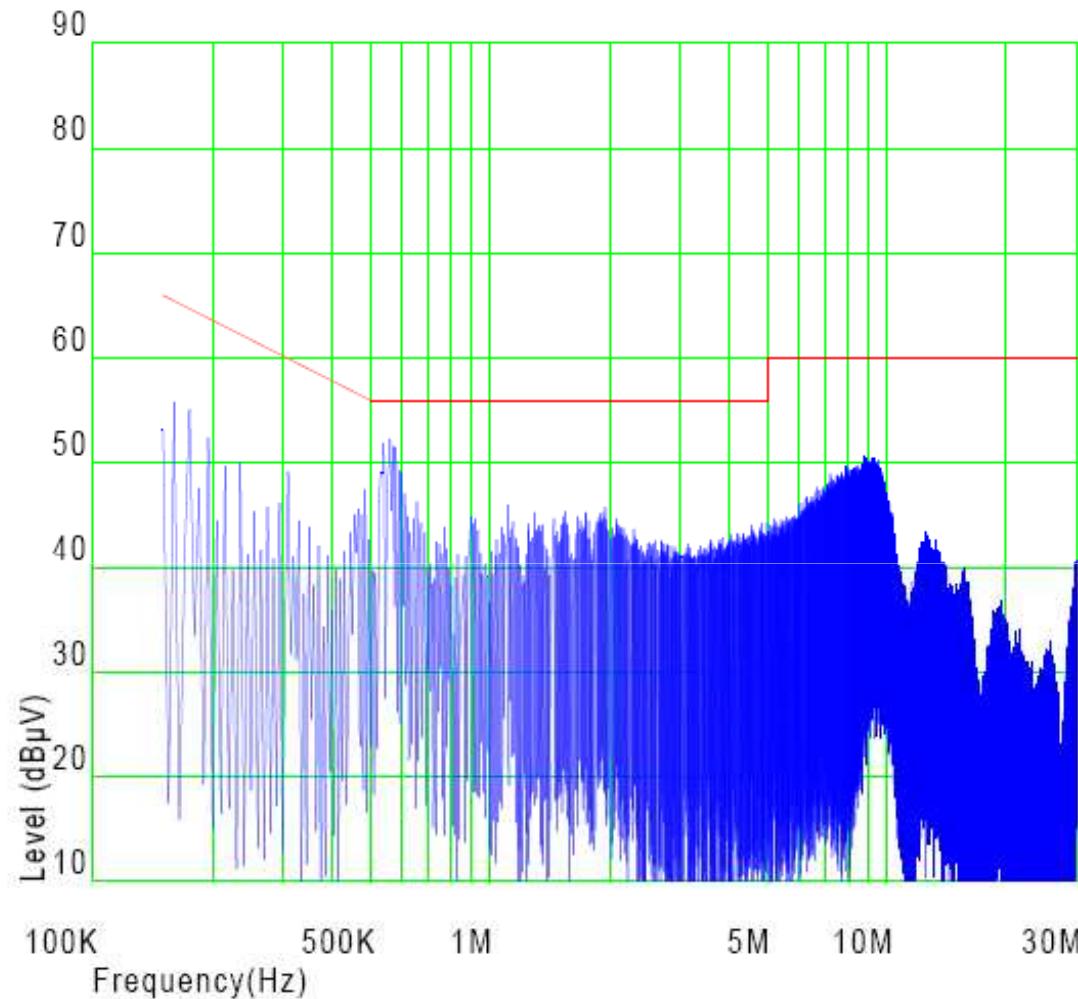
Light load and no load input power with the NCP1237

$P_{OUT}$	$V_{IN}$	115 Vac/60Hz	230 Vac/50Hz
10 % (6.5 W)		86.55 %	83.74 %
5 % (3.3 W)		85.40 %	78.72 %
1 % (0.65 W)		77.49 %	73.77 %
No load		51.1 mW	73.5 mW

# Demonstration board Efficiency

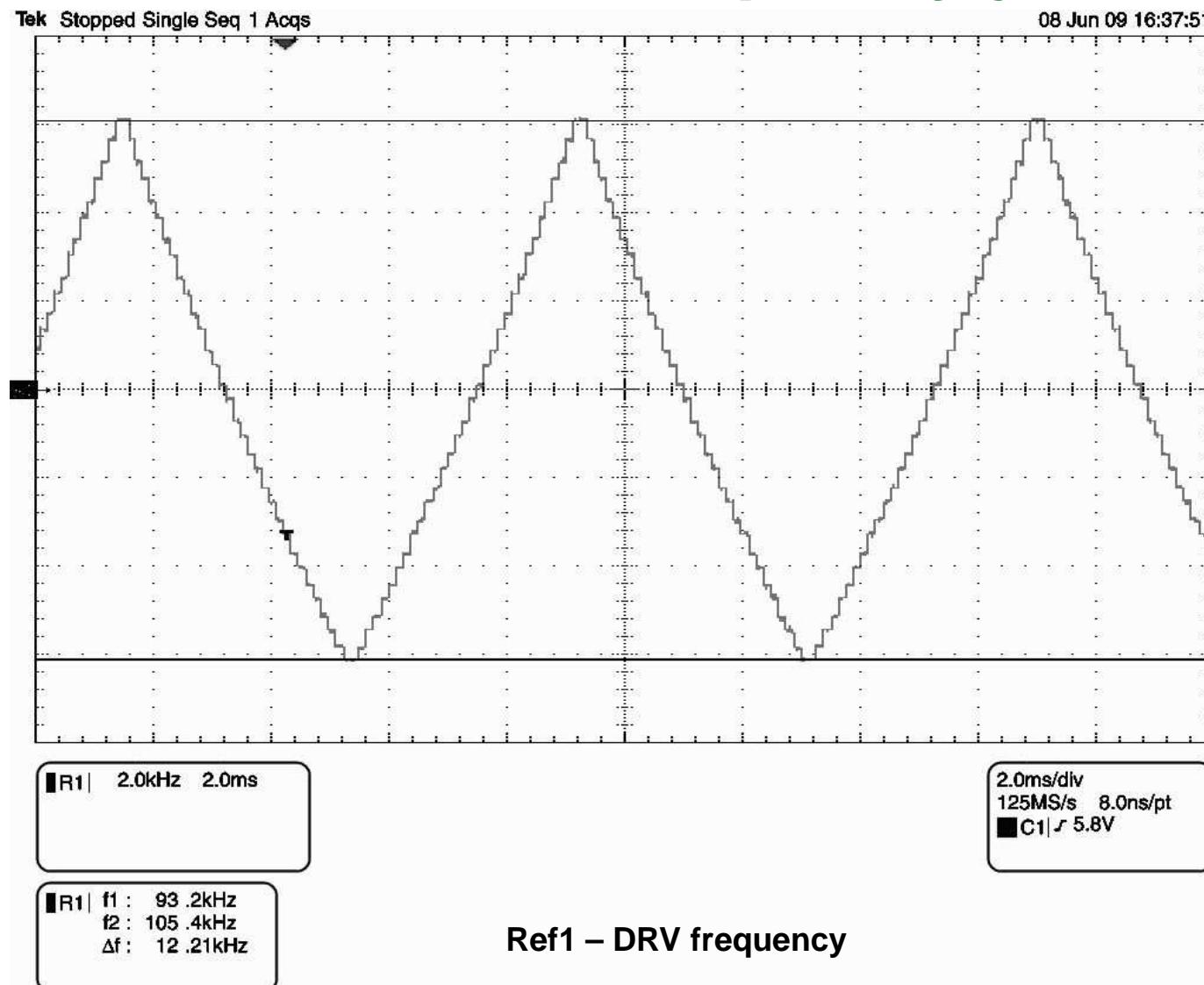


# Demonstration board conducted EMI

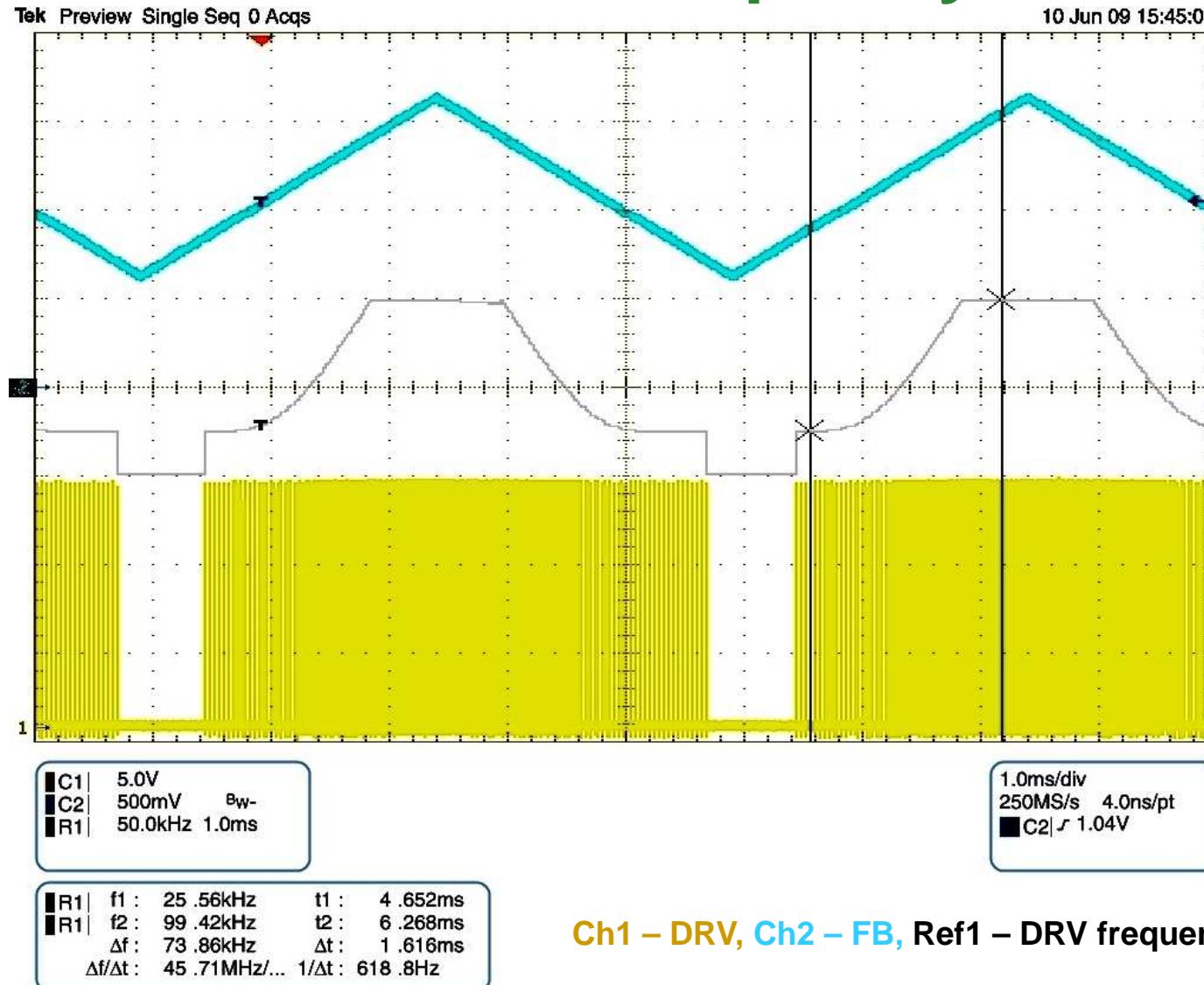


80% of full load (2.72A) at 230V/50Hz NCP1237B65kHz

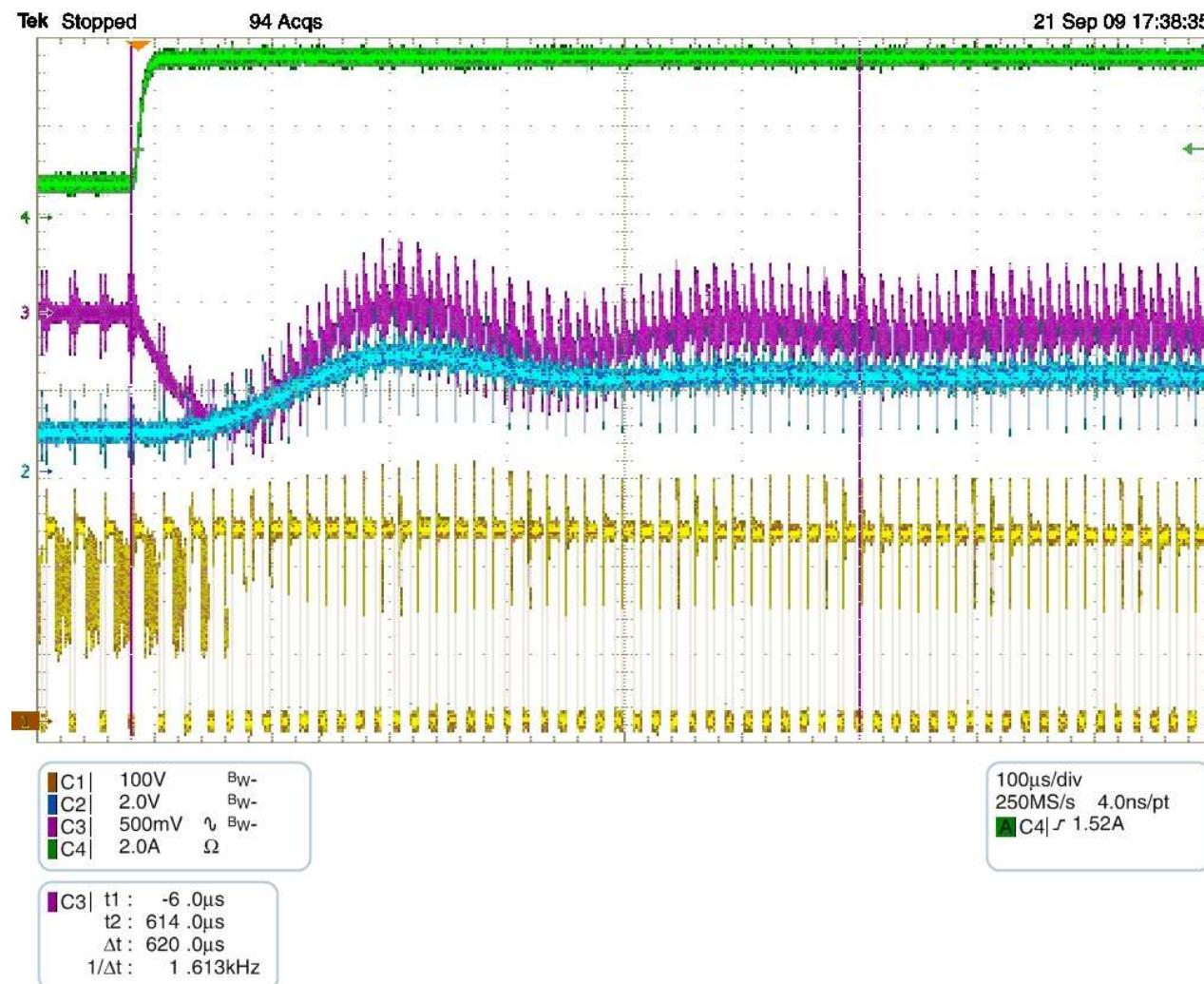
# NCP1237B100kHz frequency jittering



# NCP1237B100kHz frequency foldback

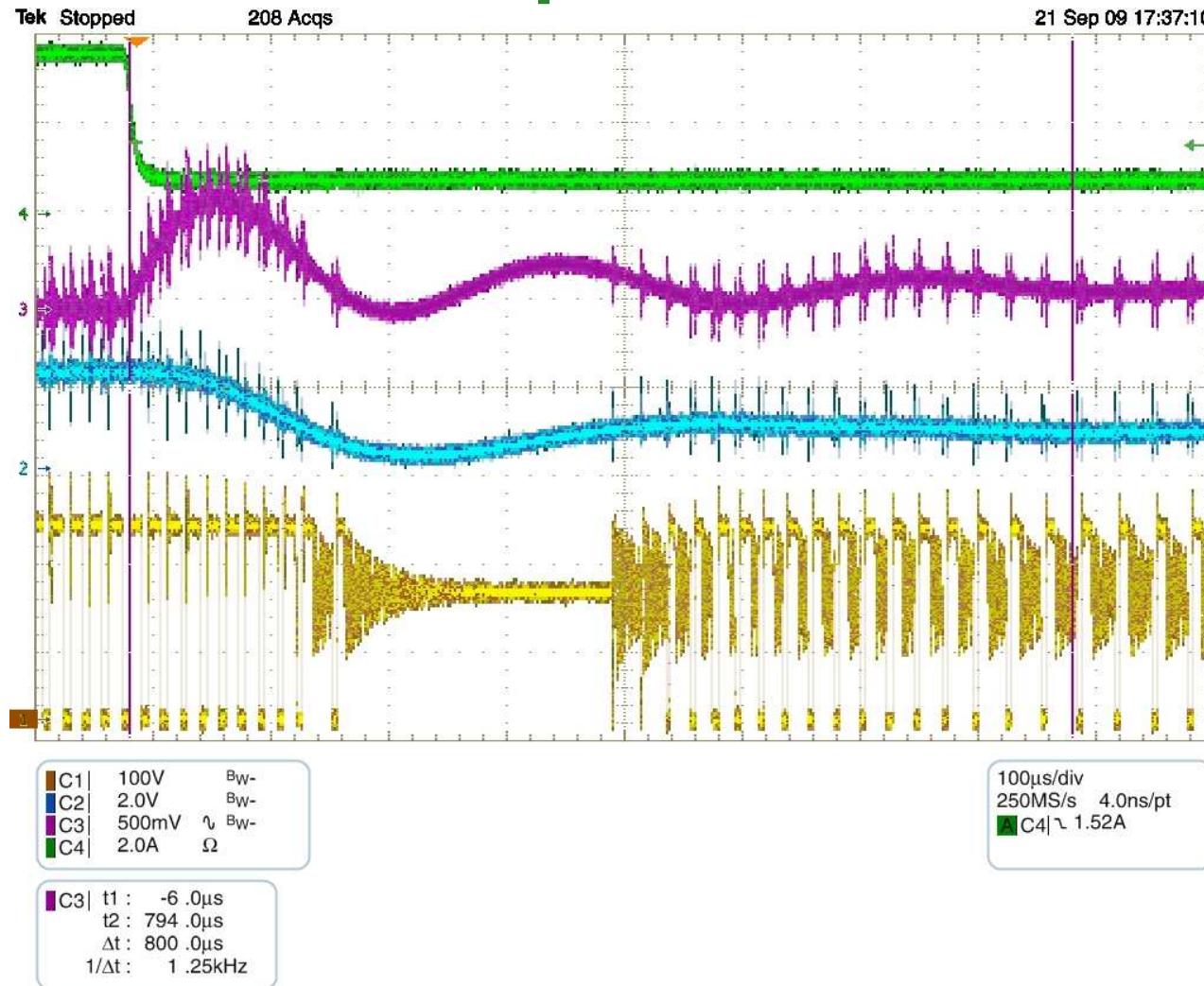


# Load transient response from 20% to 100%



Ch1 – Drain, Ch2 – FB, Ch3 – Vout (AC coupling), Ch4 - Iout

# Load transient response from 100% to 20%



Ch1 – Drain, Ch2 – FB, Ch3 – Vout (AC coupling), Ch4 - Iout

# Conclusion

- Meeting the most recent requirements from ENERGY STAR® or IEC is possible with the classical Flyback converter
- The new controller NCP1237/37/87/88 with frequency foldback and skip-mode at light load makes it possible
- Average efficiencies above 87% are possible
- No-load input power below 300 mW is possible
- No-load input power below 100 mW is achievable, although the controller alone cannot ensure this. The whole power supply must be designed to reduce power waste.

# References

Tutorial and Application notes:

[http://www.onsemi.com/pub\\_link/Collateral/TND376-D.PDF](http://www.onsemi.com/pub_link/Collateral/TND376-D.PDF)

[http://www.onsemi.com/pub\\_link/Collateral/AND8461-D.PDF](http://www.onsemi.com/pub_link/Collateral/AND8461-D.PDF)

[http://www.onsemi.com/pub\\_link/Collateral/DN06074.PDF](http://www.onsemi.com/pub_link/Collateral/DN06074.PDF)

Feedback loop design spreadsheet:

[http://www.onsemi.com/pub/Collateral/FLYBACK\\_DWS.XLS.ZIP](http://www.onsemi.com/pub/Collateral/FLYBACK_DWS.XLS.ZIP)



**ON Semiconductor®**

**Thank You! Any Questions?**

# Backup



# Over power compensation

The overpower compensation affects the primary peak current, by the following formula:

$$I_{PEAK} = \frac{V_{CS\text{int}}}{R_{sense}} + V_{bulk} \cdot \left( \frac{t_{PROP}}{L_P} - g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}} \right) + V_{off} \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}}$$

Then the overpower compensation resistor can be calculated:

$$R_{OPP} = \frac{t_{PROP} \cdot R_{sense}}{L_P \cdot g_{OPP}}$$

The over power compensating resistor affects only the  $I_{peak}$  value, but in CCM the output power is given by the following formula, where  $I_{valley}$  plays a role:

$$P_{out} = \frac{1}{2} \cdot \eta \cdot L_{prim} \cdot F_{sw} \cdot \left( I_{peak}^2 - I_{valley}^2 \right)$$

## 2<sup>nd</sup> level over current protection

The overpower compensation affects the 2<sup>nd</sup> level over current protection by the addition of bulk voltage feed forward.

$$I_{TRAN} = \frac{V_{CStran}}{R_{sense}} - (V_{bulk} - V_{off}) \cdot g_{OPP} \cdot \frac{R_{OPP}}{R_{sense}}$$

The 2<sup>nd</sup> level over current protection can be used for reducing the transformer size to ½ and keeping the peak power capability.

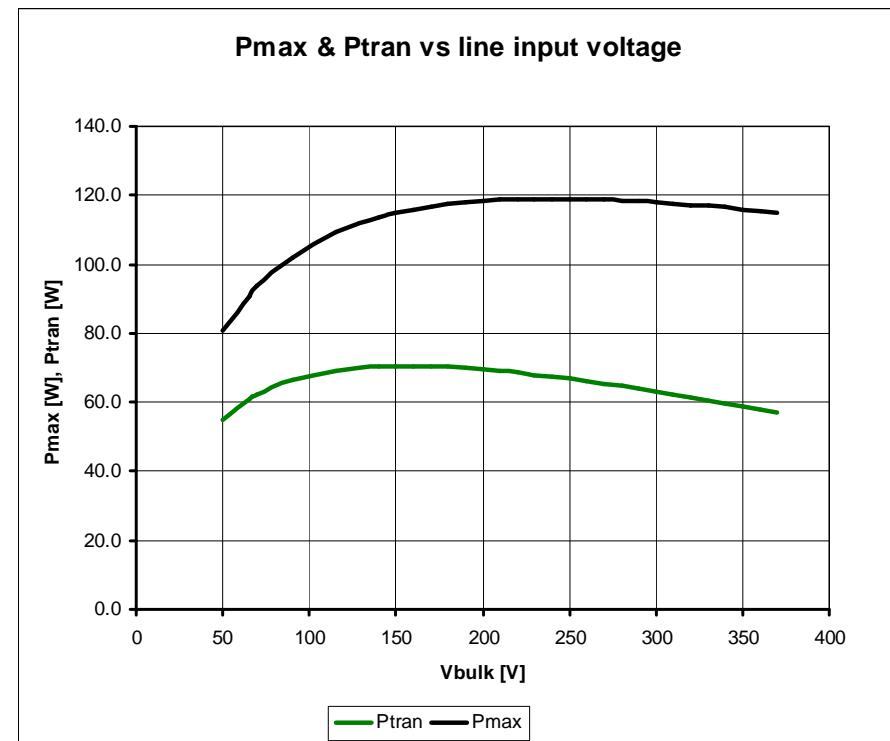
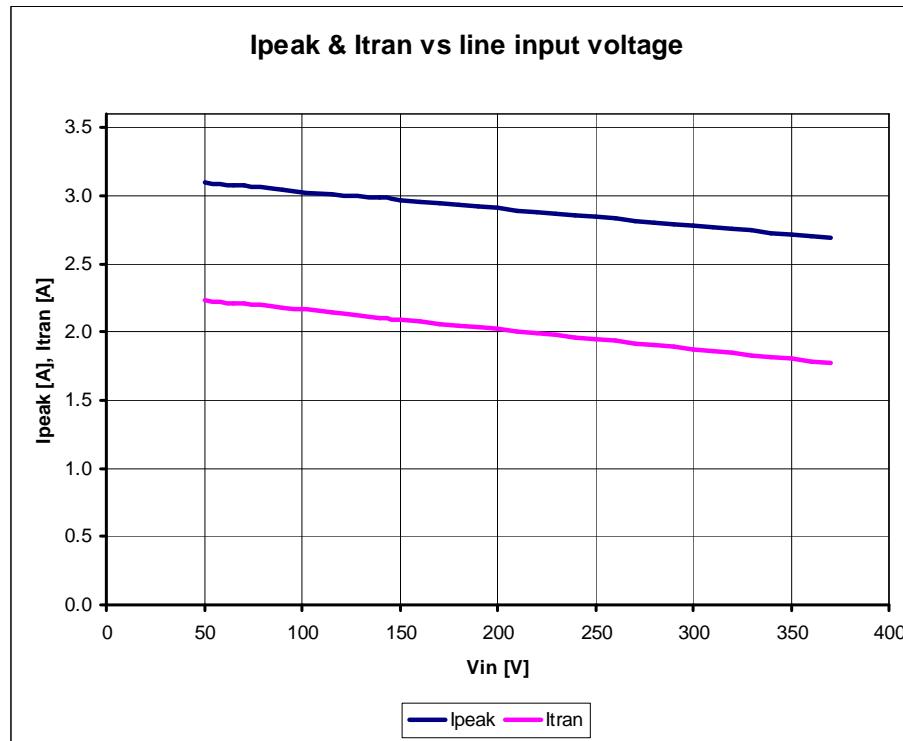
# Spread sheet design of OPC

OPC design spread sheet was created and the user can choose the right  $R_{OPP}$  and it's effect to  $I_{peak}$ ,  $I_{tran}$ ,  $P_{out}$  and  $P_{tran}$ :

Inputs:

Output voltage	Vout [V]	19
Primary turns	N1 [-]	100
Secondary turns	N2 [-]	25
Ramp Comp at CS	RaCo [mV/%]	5
Maximum int set point	Vilimit [V]	0.7
Sensing resistor	Rsense [Ohm]	0.235
Propagation delay	tprop [ns]	100
Primary inductance	Lp [uH]	560
Vin to lopp ratio	gopp [uS]	0.5
Over power comp resistor	Ropp [Ohm]	680
Switching frequency	Fsw [kHz]	65
2nd level overcurrent prot	Vcstran [V]	0.5

# Spread sheet design of OPC



Keeping constant  $I_{peak}$  in CCM mode tends to  $I_{valley}$  decreasing with increasing the  $V_{in}$ . That's why the maximum output deliverable power  $P_{out}$  increases with increasing  $V_{in}$ . **Choose the right compensation.**