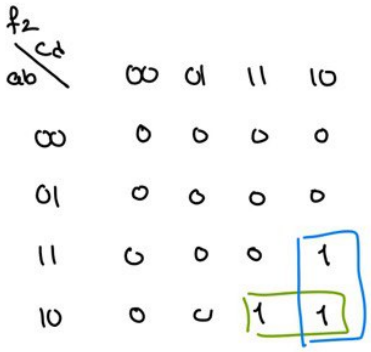
With_ SSI

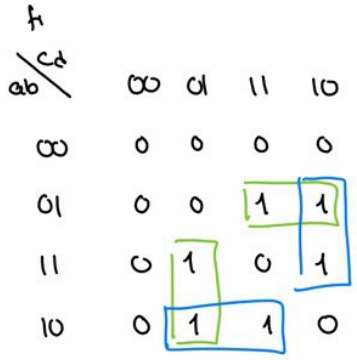
- First i obtain the f0, f1, f2 and f3 with the basic gates with the help of karnaugh maps

a	b	c	d	f_3	f_2	f_1	f_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1



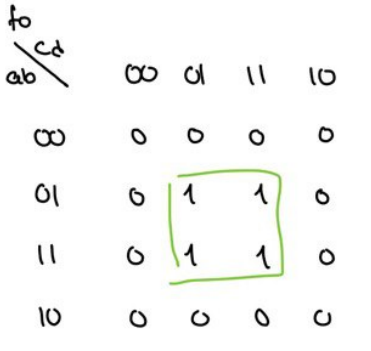
$f_2 = ab'c + acd'$

$= ac(\bar{b} + \bar{d})$



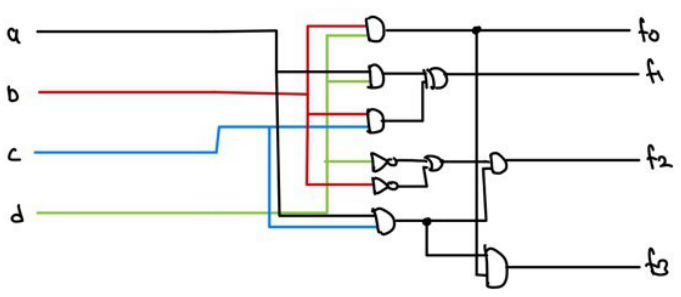
$f_1 = ac'd + ab'd + a'bc + bcd'$

$= ad \oplus bc$



$f_0 = bd$

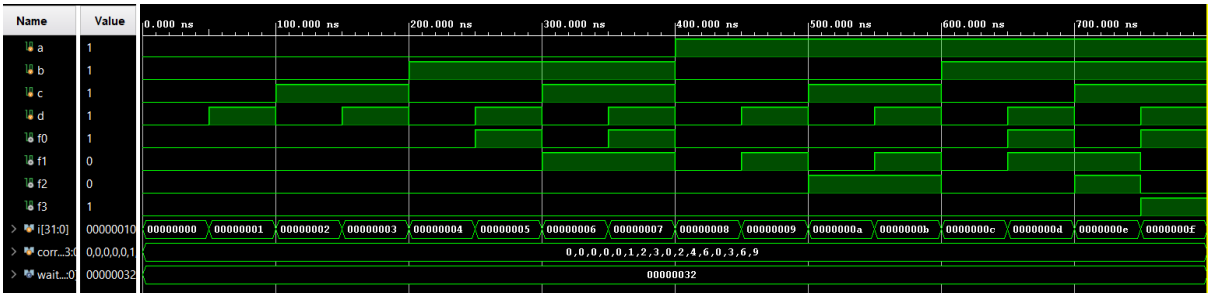
$f_3 = abcd$



- then I wrote my code with gates that i did in the SSı library with the help of circuit i made in the first step

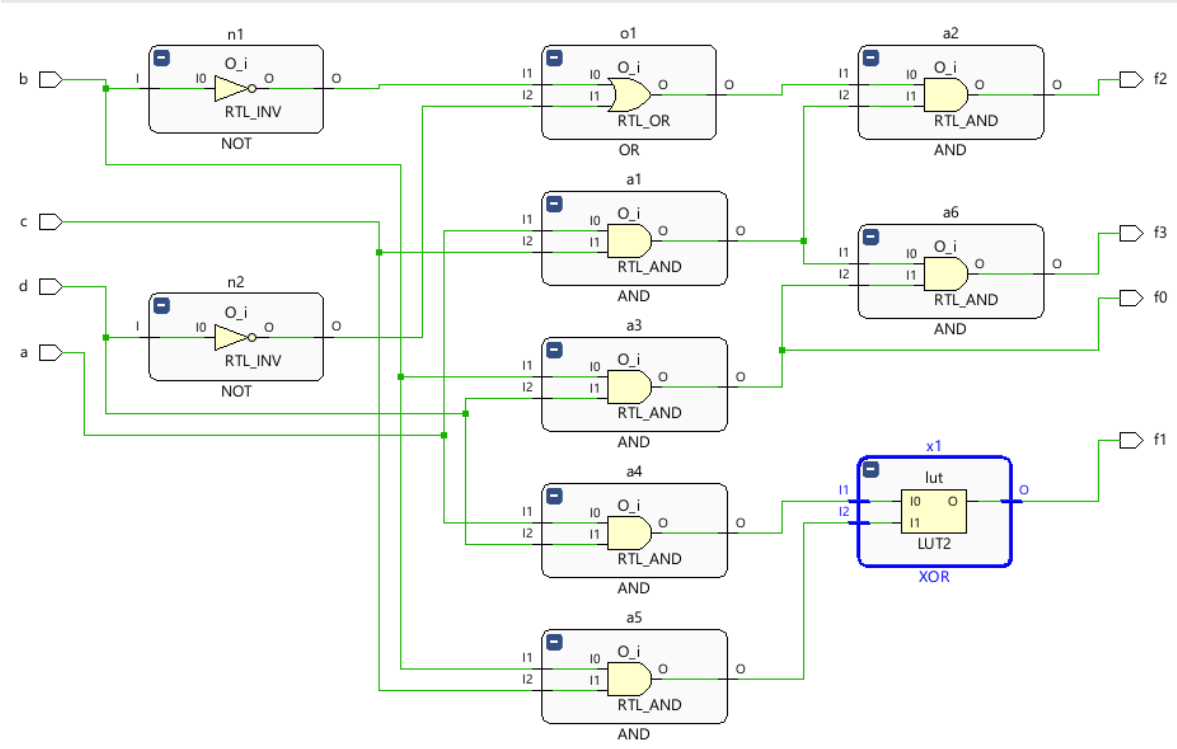
```
module with_SSI(
input a,b,c,d,
output f3,f2,f1,f0
    );
    wire [5:0] fort;

    AND a1(a, c, fort[0]);
    NOT n1(b, fort[1]);
    NOT n2(d, fort[2]);
    OR o1(fort[1], fort[2], fort[3]);
    AND a2(fort[3], fort[0], f2);
    AND a3(b, d, f0);
    AND a6(fort[0], f0, f3);
    AND a4(a, d, fort[4]);
    AND a5(b, c, fort[5]);
    XOR x1(fort[4], fort[5], f1);

endmodule
```

- my Simulation results are true.

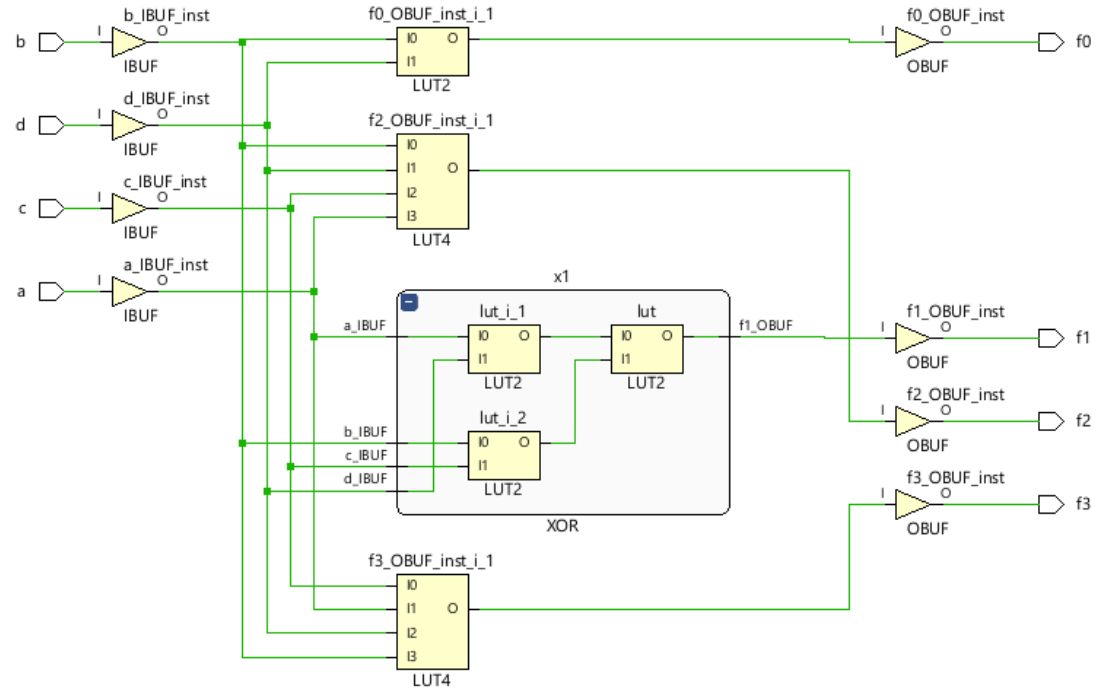


```
# run 1000ns
{a,b,c,d}=0000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0001 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0010 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0011 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0101 => {f3,f2,f1,f0} = 0001 -- TRUE
{a,b,c,d}=0110 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=0111 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1001 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=1010 => {f3,f2,f1,f0} = 0100 -- TRUE
{a,b,c,d}=1011 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1101 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1110 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1111 => {f3,f2,f1,f0} = 1001 -- TRUE
```

- RTl schematic



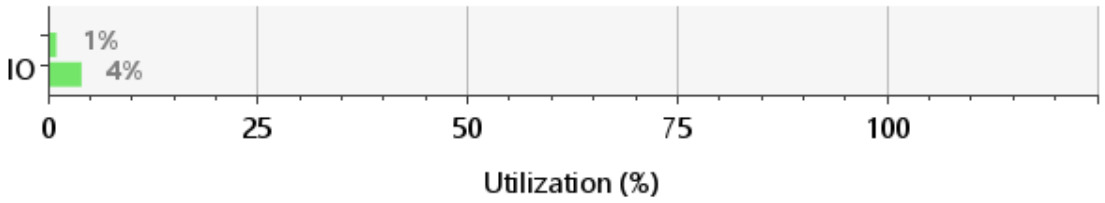
- Technology schematic



- Timing and utilization reports my maximum combinational delay is 9.601 and 5 lut is used in this design

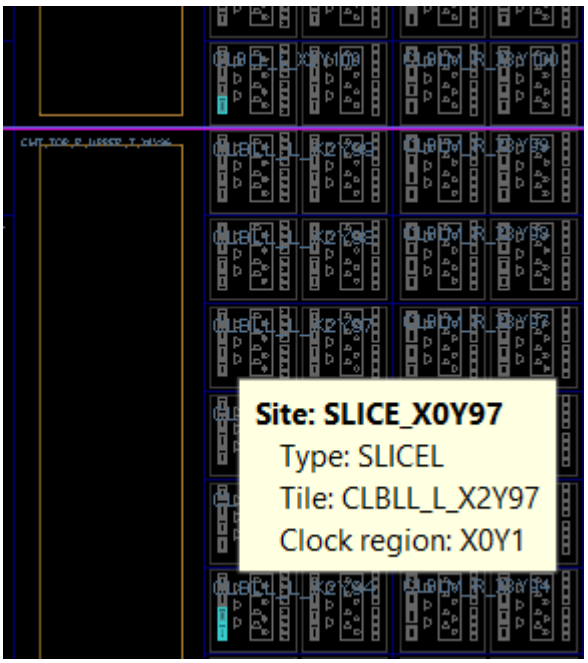
From Port	To Port	Max Delay 1	Max Process Corner	Min Delay	Min Process Corner
a	f2	9.601	SLOW	2.992	FAST
a	f1	9.524	SLOW	2.950	FAST
d	f2	9.489	SLOW	2.910	FAST
b	f1	9.402	SLOW	2.851	FAST
c	f1	9.199	SLOW	2.728	FAST
a	f3	9.111	SLOW	2.809	FAST
c	f2	9.088	SLOW	2.729	FAST
d	f3	8.999	SLOW	2.723	FAST
d	f1	8.933	SLOW	2.700	FAST
b	f0	8.922	SLOW	2.688	FAST
b	f2	8.891	SLOW	2.728	FAST
c	f3	8.596	SLOW	2.544	FAST
b	f3	8.433	SLOW	2.539	FAST
d	f0	8.092	SLOW	2.382	FAST

Resource	Utilization	Available	Utilization %
LUT	5	63400	0.01
IO	8	210	3.81



- and the used luts:

```
set cell_list [get_cells -hierarchical -filter { PRIMITIVE_TYPE =~ LUT.*.* }]
f0_OBUF_inst_i_1 f2_OBUF_inst_i_1 f3_OBUF_inst_i_1 x1/lut x1/lut_i_1 x1/lut_i_2
```



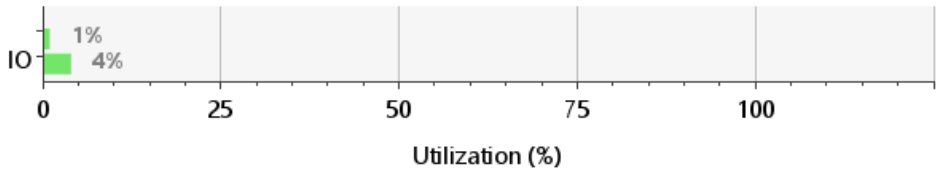
- After I add the constraint my maximum combinational delay reduced to 9.041 but not met the 9ns and number of luts used in design decreased to 4

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-0.042 ns	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	-0.042 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	1	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	4	Total Number of Endpoints:	4	Total Number of Endpoints:	NA

Timing constraints are not met.

From Port	To Port	Max Delay	Max Process Corner
a	f2	9.041	SLOW
b	f0	8.948	SLOW
a	f1	8.883	SLOW
d	f0	8.837	SLOW
b	f1	8.829	SLOW
b	f2	8.805	SLOW
c	f1	8.482	SLOW
c	f2	8.401	SLOW
d	f1	8.287	SLOW
d	f2	8.286	SLOW
a	f3	8.260	SLOW
c	f3	8.163	SLOW
d	f3	8.150	SLOW
b	f3	7.693	SLOW

Resource	Utilization	Available	Utilization %
LUT	4	63400	0.01
IO	8	210	3.81



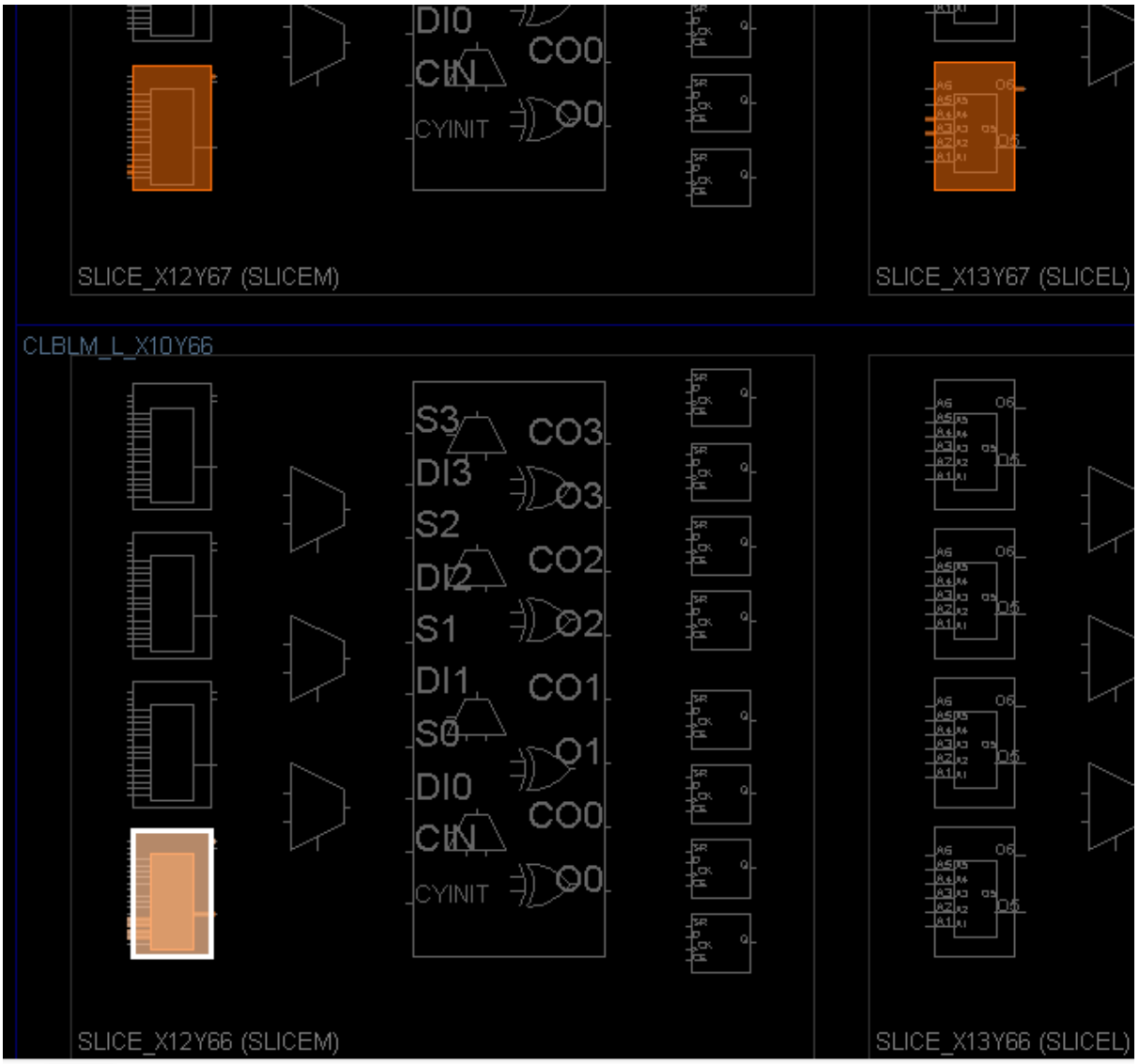
- And the used luts:

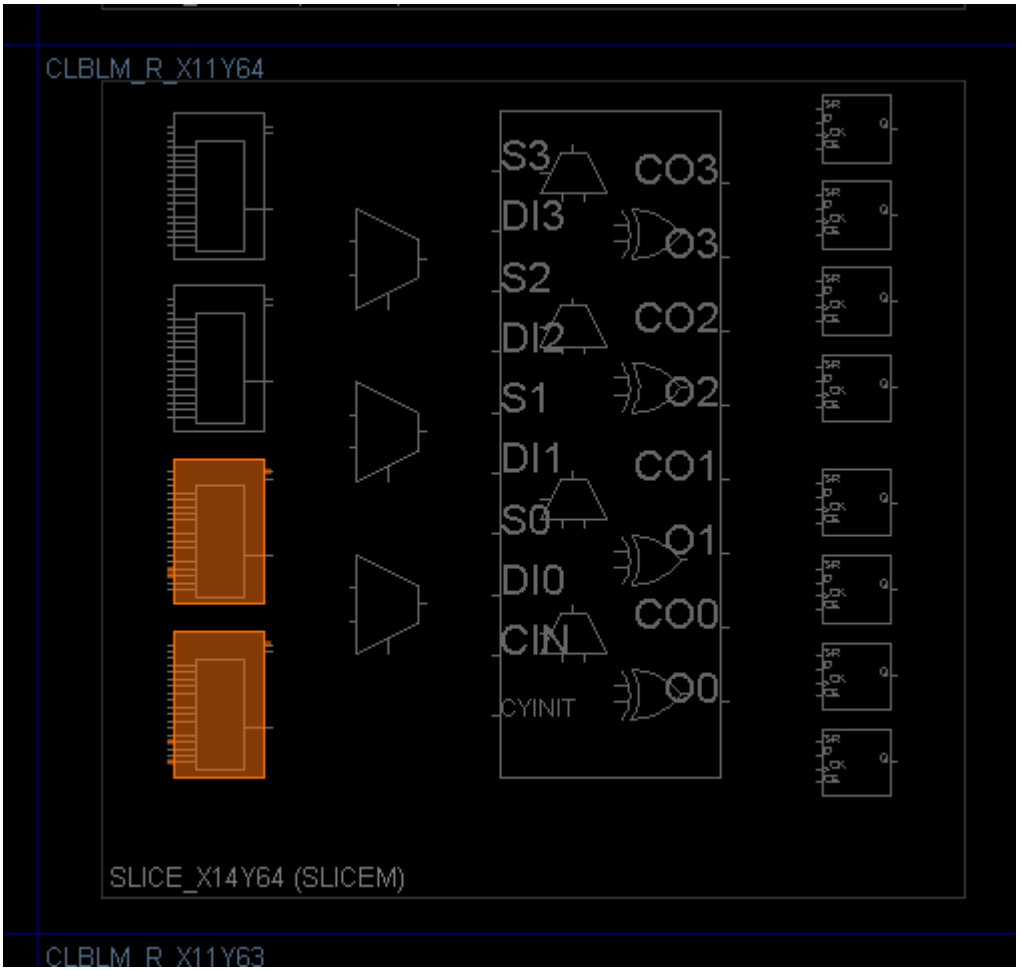
```
set cell_list [get_cells -hierarchical -filter { PRIMITIVE_TYPE =~ LUT.*.* }]
f0_OBUF_inst_i_1 f2_OBUF_inst_i_1 f3_OBUF_inst_i_1 x1/lut_comp x1/lut_i_2
```

- I added the LOC and choose slices with them and comment out the timing constraint

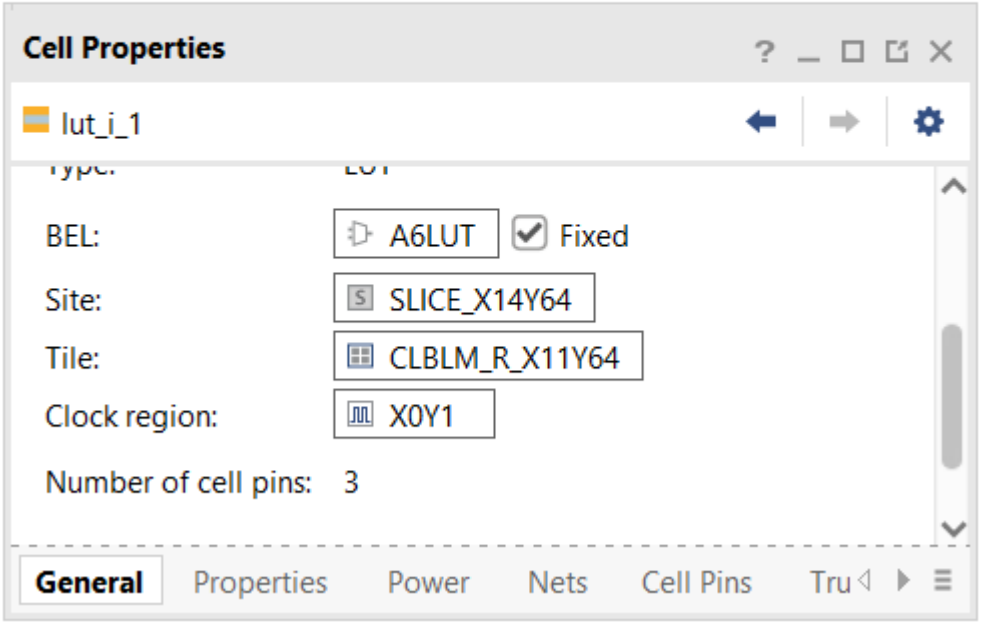
```
set_property LOC SLICE_X12Y67 [get_cells f0_OBUF_inst_i_1]
set_property LOC SLICE_X12Y66 [get_cells f2_OBUF_inst_i_1]
set_property LOC SLICE_X13Y67 [get_cells x1/lut]
set_property LOC SLICE_X14Y64 [get_cells x1/lut_i_1]
set_property LOC SLICE_X14Y64 [get_cells x1/lut_i_2]
```

- After choosing the slices the written slices in the constraint file can be seen in the device as used luts.




CLBLM_R_X11Y64
S3
DI3
S2
DI2
S1
DI1
S0
DI0
CIN
CYINIT
CO3
O3
CO2
O2
CO1
O1
CO0
O0
SLICE_X14Y64 (SLICEM)
CLBLM_R_X11Y63

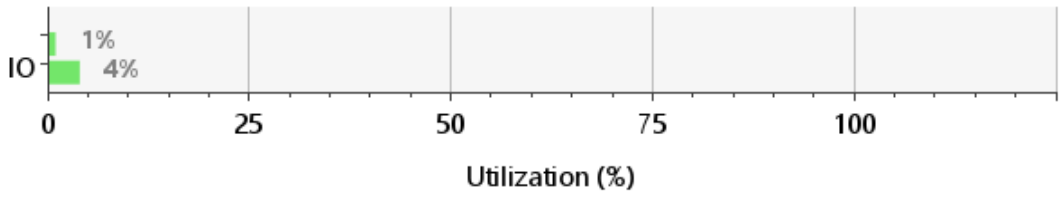

lut (LUT2)
lut_i_1 (LUT2)
lut_i_2 (LUT2)


Cell Properties
lut_i_1
BEL:
A6LUT
Fixed
Site:
SLICE_X14Y64
Tile:
CLBLM_R_X11Y64
Clock region:
X0Y1
Number of cell pins:
3
General
Properties
Power
Nets
Cell Pins

- With this particular slices the maximum combinational delay is increased because the path is longer now but used lut number is same. The reason causing an increase is that used luts are more far from the inputs and between themselves.

From Port	To Port	Max Delay 1	Max Process Corner	Min Delay	Min Process Corner
d	f1	12.051	SLOW	4.056	FAST
b	f1	11.478	SLOW	3.804	FAST
c	f1	11.474	SLOW	3.807	FAST
d	f2	11.322	SLOW	3.796	FAST
a	f1	11.072	SLOW	3.605	FAST
d	f3	11.038	SLOW	3.704	FAST
d	f0	10.990	SLOW	3.655	FAST
c	f2	10.964	SLOW	3.665	FAST
b	f2	10.687	SLOW	3.554	FAST
b	f0	10.683	SLOW	3.516	FAST
c	f3	10.682	SLOW	3.572	FAST
b	f3	10.407	SLOW	3.464	FAST
a	f2	10.051	SLOW	3.270	FAST
a	f3	9.737	SLOW	3.182	FAST

Resource	Utilization	Available	Utilization %
LUT	5	63400	0.01
IO	8	210	3.81



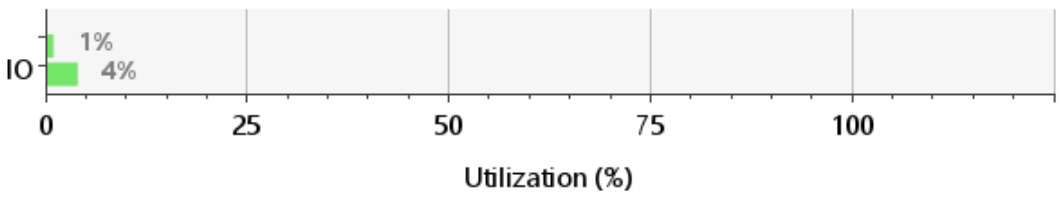
- Then I add the timing constraint and maximum combinational delay is reduced but it did not met again. Maximum combinational delay is 10.738 ns

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-1.739 ns	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	-6.356 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	4	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	4	Total Number of Endpoints:	4	Total Number of Endpoints:	NA

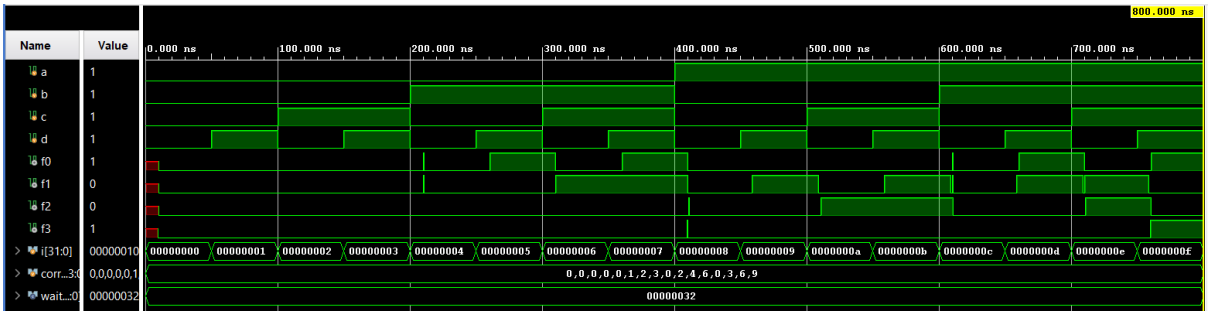
Timing constraints are not met.

From Port	To Port	Max Delay	Max Process Corner
c	f1	10.738	SLOW
b	f2	10.643	SLOW
d	f0	10.629	SLOW
b	f1	10.561	SLOW
c	f2	10.550	SLOW
d	f2	10.541	SLOW
b	f3	10.341	SLOW
c	f3	10.245	SLOW
b	f0	10.227	SLOW
d	f3	10.205	SLOW
a	f2	10.111	SLOW
a	f3	9.807	SLOW
a	f1	9.426	SLOW
d	f1	9.246	SLOW

Resource	Utilization	Available	Utilization %
LUT	5	63400	0.01
IO	8	210	3.81



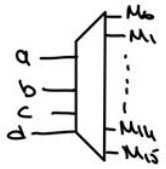
- The waveform of the circuit. we can see the delay at the beginning and in the parts that changes immediately at first waveform.



- The designs that used time constraints combinational delays are less than the others and the design that has not specific loc is have less combinational delay than the other

With_Decoder

- First i did the decoder representation with all possible minterms then express the f0, f1, f2, f3 with these minterms.



$m_0 = a'b'c'd'$ $m_6 = a'bcd'$ $m_{12} = abc'd'$

$m_1 = a'b'c'd$ $m_7 = a'bcd$ $m_{13} = abc'd$

$m_2 = a'b'cd'$ $m_8 = ab'c'd'$ $m_{14} = abcd'$

$m_3 = a'b'cd$ $m_9 = ab'c'd$ $m_{15} = abcd$

$m_4 = a'bc'd'$ $m_{10} = ab'cd'$

$m_5 = a'bcd$ $m_{11} = ab'cd$

$f_0 = bd = x1x1 = m_5 + m_7 + m_{13} + m_{15}$

$f_1 = ac'd + ab'd + a'bc + bcd' = 1x01 + 10x1 + 011x + x110 = m_{13} + m_9 + m_{11} + m_7 + m_6 + m_{14}$

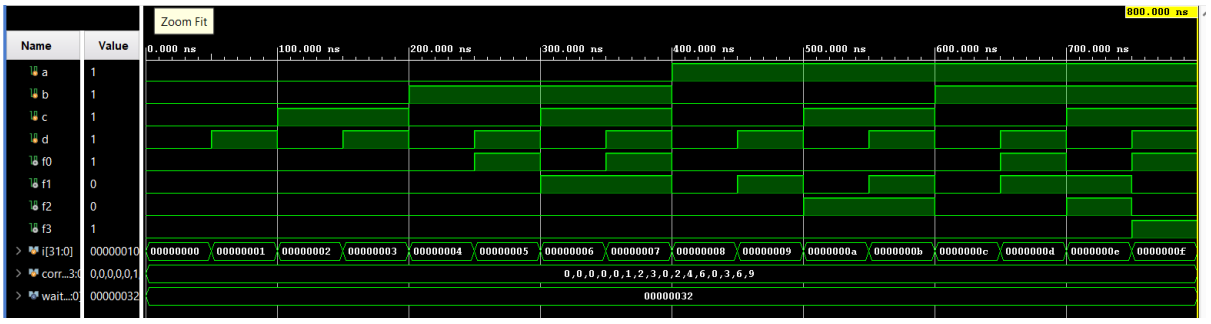
$f_2 = ab'c + acd' = 101x + 1x10 = m_{11} + m_{10} + m_{14}$

$f_3 = abcd = m_{15}$

- then i wrote my code with the help of previous step

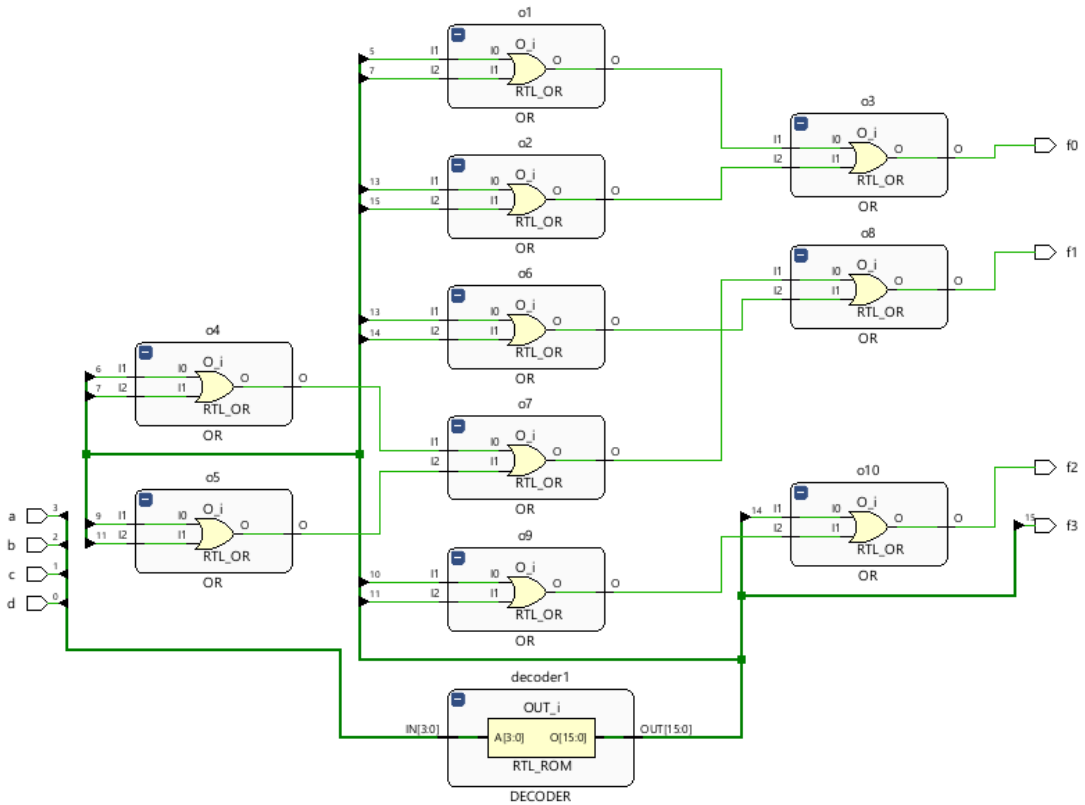
```
module with_decoder(
input a,b,c,d,
output f3,f2,f1,f0
);
wire [15:0] m;
wire fort0,fort1,fort2,fort3,fort4,fort5,fort6,fort7;

DECODER decoder1(.IN({a,b,c,d}), .OUT(m));

assign f3=m[15];

OR o1(m[5], m[7], fort0);
OR o2(m[13], m[15], fort1);
OR o3(fort0, fort1, f0);
OR o4(m[6], m[7], fort3);
OR o5(m[9], m[11], fort4);
OR o6(m[13], m[14], fort5);
OR o7(fort3, fort4, fort6);
OR o8(fort6, fort5, f1);
OR o9(m[10], m[11], fort7);
OR o10(m[14], fort7, f2);

endmodule
```

- my simulation results are true

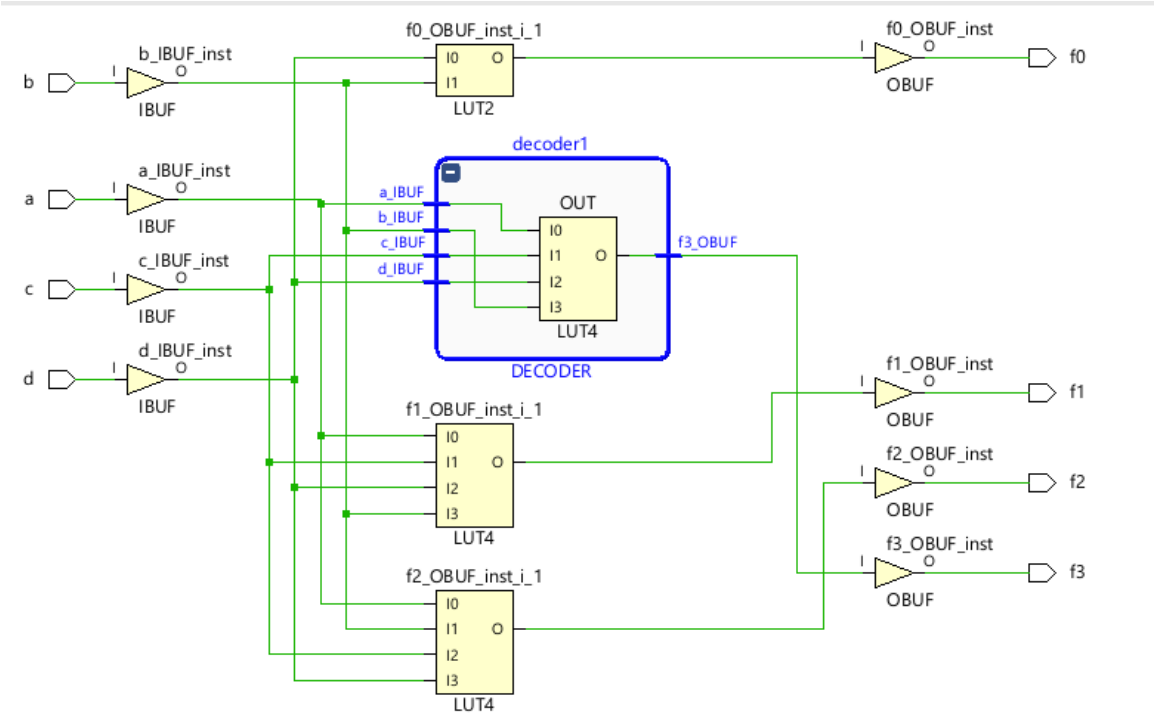


```
# run 1000ns
{a,b,c,d}=0000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0001 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0010 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0011 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0101 => {f3,f2,f1,f0} = 0001 -- TRUE
{a,b,c,d}=0110 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=0111 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1001 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=1010 => {f3,f2,f1,f0} = 0100 -- TRUE
{a,b,c,d}=1011 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1101 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1110 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1111 => {f3,f2,f1,f0} = 1001 -- TRUE
```

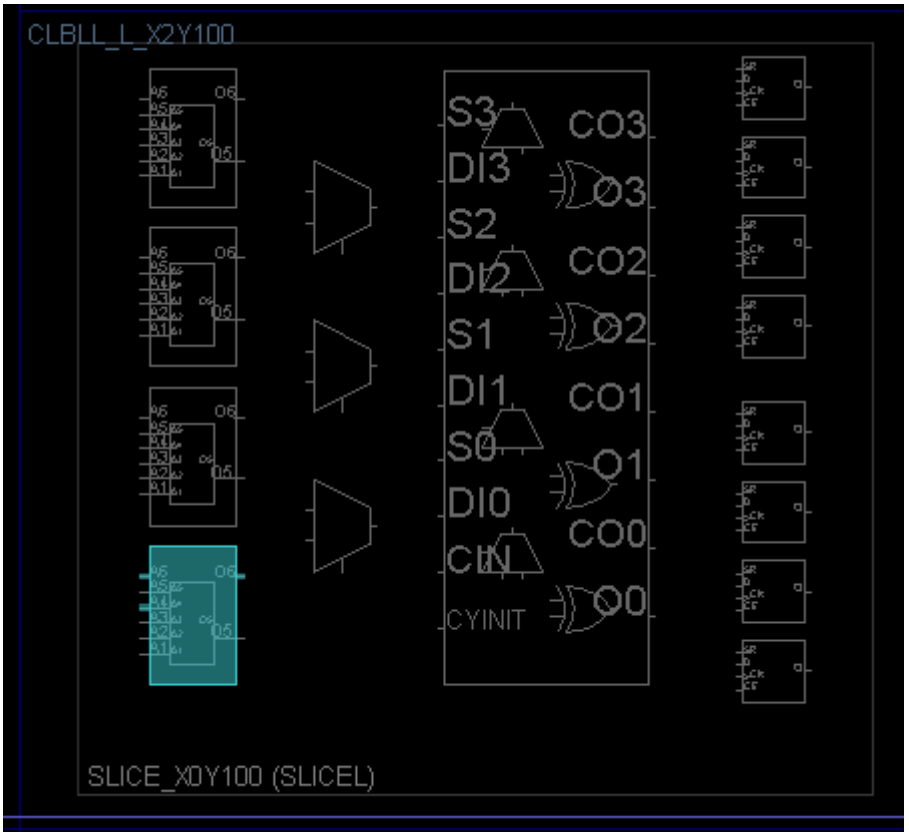
- RTL schematic

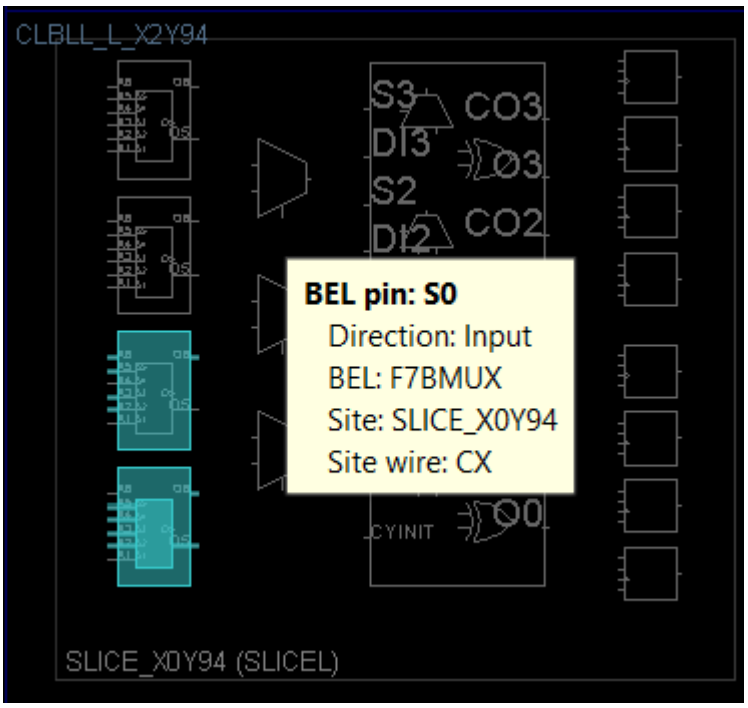


Technology schematic



The luts are in slice X0Y100 and X0Y94

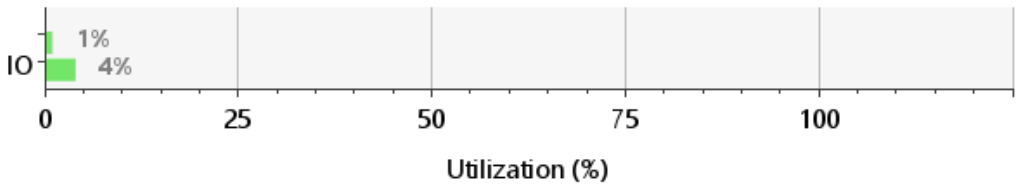




- **Timing and utilization reports. maximum combinational delay is9.497, 3 lut is used that can see in the device previous step**

From Port	To Port	Max Delay 1	Max Process Corner	Min Delay	Min Process Corner
a	f2	9.497	SLOW	2.979	FAST
a	f1	9.422	SLOW	2.895	FAST
a	f3	9.261	SLOW	2.866	FAST
b	f0	8.922	SLOW	2.688	FAST
b	f2	8.898	SLOW	2.732	FAST
b	f1	8.821	SLOW	2.645	FAST
d	f2	8.665	SLOW	2.649	FAST
b	f3	8.652	SLOW	2.603	FAST
c	f2	8.619	SLOW	2.591	FAST
d	f1	8.556	SLOW	2.569	FAST
c	f1	8.543	SLOW	2.508	FAST
d	f3	8.431	SLOW	2.533	FAST
c	f3	8.285	SLOW	2.445	FAST
d	f0	8.091	SLOW	2.381	FAST

Resource	Utilization	Available	Utilization %
LUT	3	63400	0.00
IO	8	210	3.81



- **After I add the timing constraint the constraint not met but the maximum combinational delay reduced to 8.826 ns**

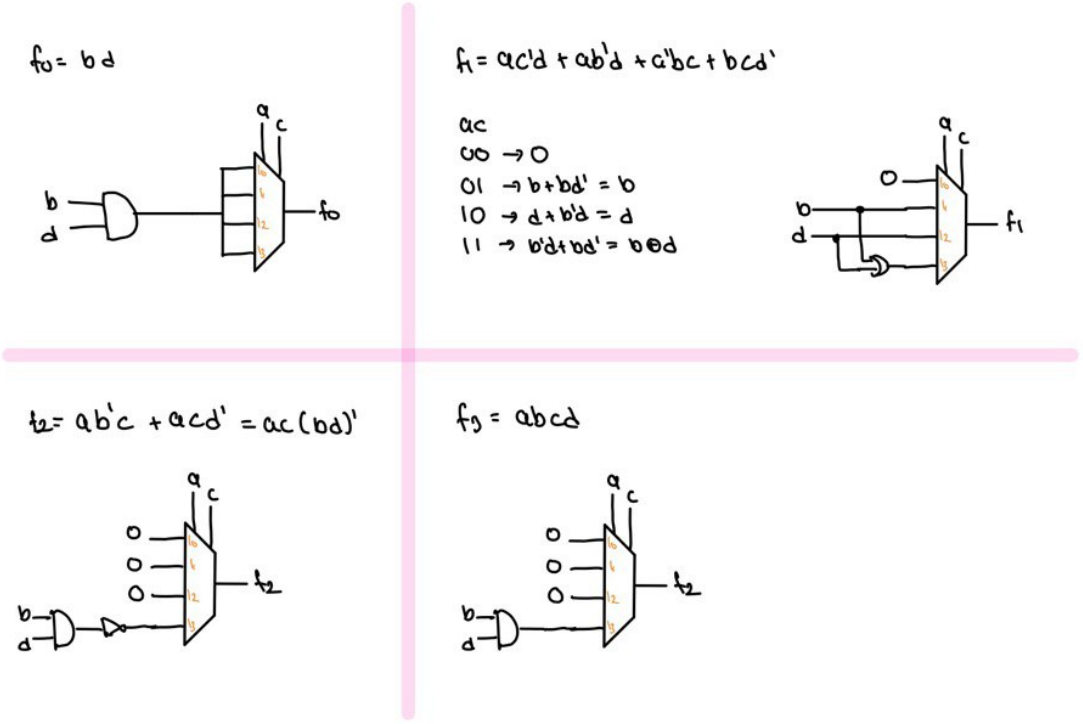
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-2.826 ns	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	-9.709 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	4	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	4	Total Number of Endpoints:	4	Total Number of Endpoints:	NA

Timing constraints are not met.

From Port	To Port	Max Delay 1	Max Process Corner
a	f2	8.826	SLOW
c	f2	8.688	SLOW
d	f2	8.577	SLOW
b	f2	8.551	SLOW
a	f1	8.399	SLOW
b	f0	8.307	SLOW
d	f1	8.237	SLOW
d	f0	8.178	SLOW
d	f3	8.177	SLOW
b	f1	8.132	SLOW
c	f3	8.088	SLOW
c	f1	8.059	SLOW
b	f3	7.988	SLOW
a	f3	7.929	SLOW

With_mux

- First I obtain f0, f1, f2, f3 with the mux that has a and c as a select and b and d as an input.



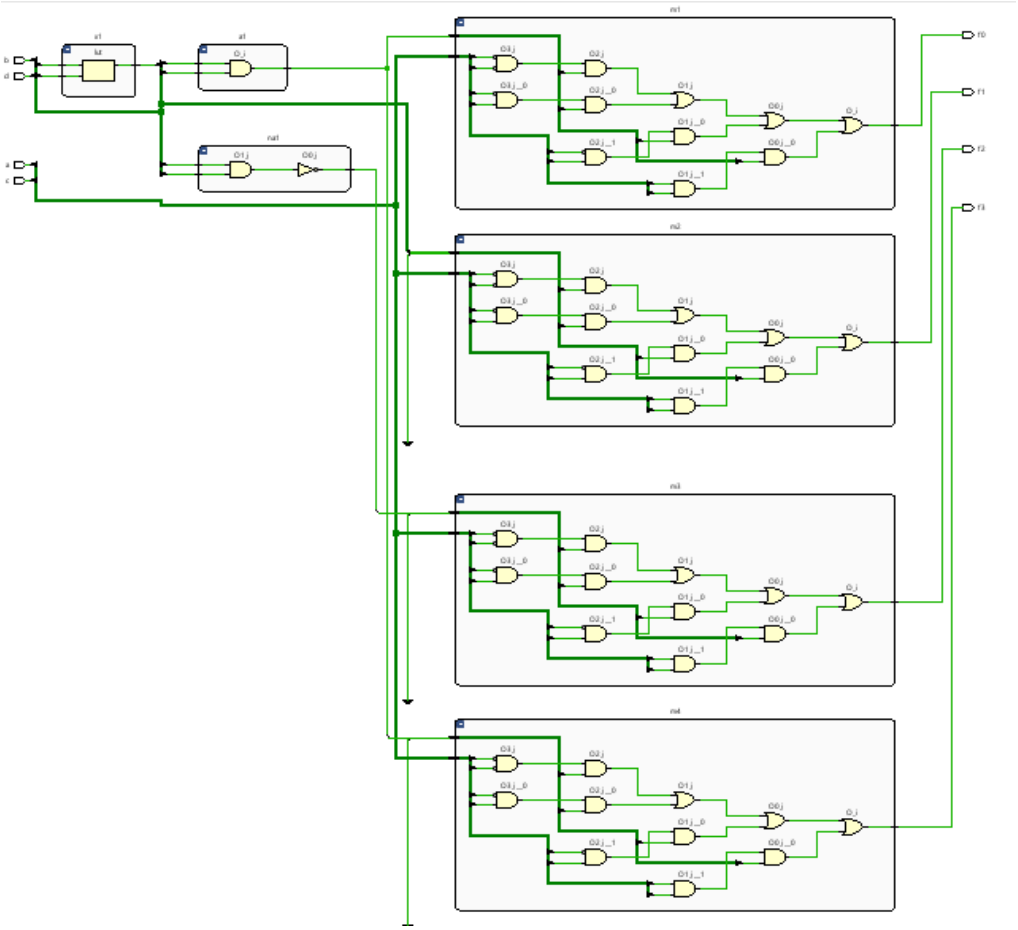
- Then with the help of the first step I wrote the code with the MUX in from the exp2 library.

```
module with_MUX(
input a,b,c,d,
output f3,f2,f1,f0
);

wire fort1,fort2,fort3;
AND a1(b, d, fort1);
XOR x1(b, d, fort2);
NAND na1(b, d, fort3);
MUX m1(.D({fort1,fort1,fort1,fort1}), .S({a,c}), .O(f0));
MUX m2(.D({fort2,d,b,1'b0}), .S({a,c}), .O(f1));
MUX m3(.D({fort3,1'b0,1'b0,1'b0}), .S({a,c}), .O(f2));
MUX m4(.D({fort1,1'b0,1'b0,1'b0}), .S({a,c}), .O(f3));
endmodule
```

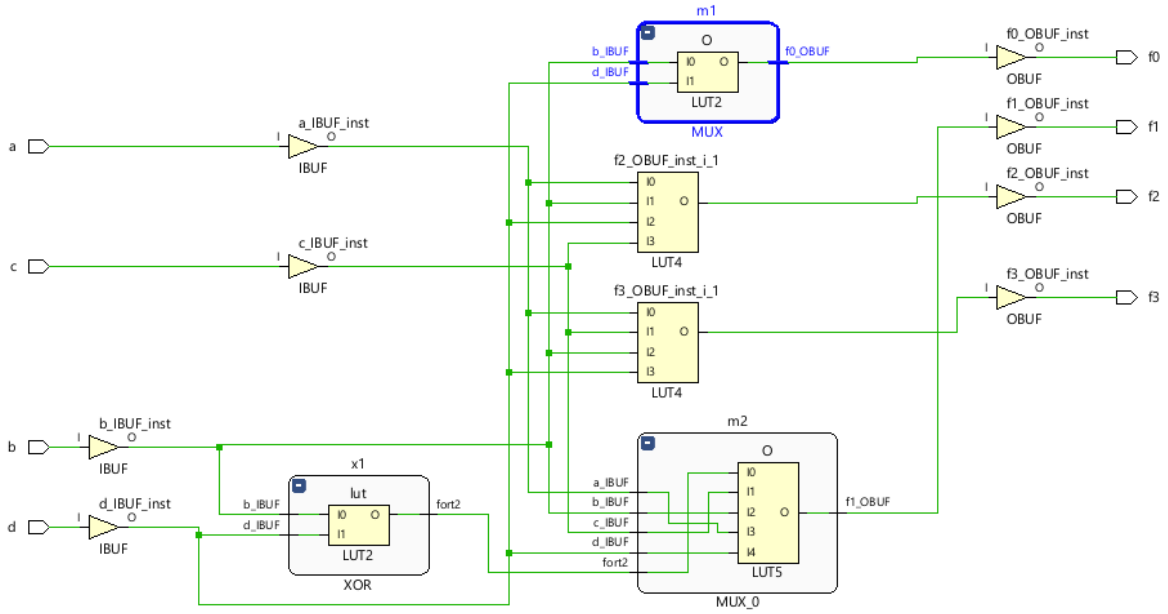
- My simulation result is as expected and same with the others

```
{a,b,c,d}=0000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0001 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0010 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0011 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0101 => {f3,f2,f1,f0} = 0001 -- TRUE
{a,b,c,d}=0110 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=0111 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1001 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=1010 => {f3,f2,f1,f0} = 0100 -- TRUE
{a,b,c,d}=1011 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1101 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1110 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1111 => {f3,f2,f1,f0} = 1001 -- TRUE
```

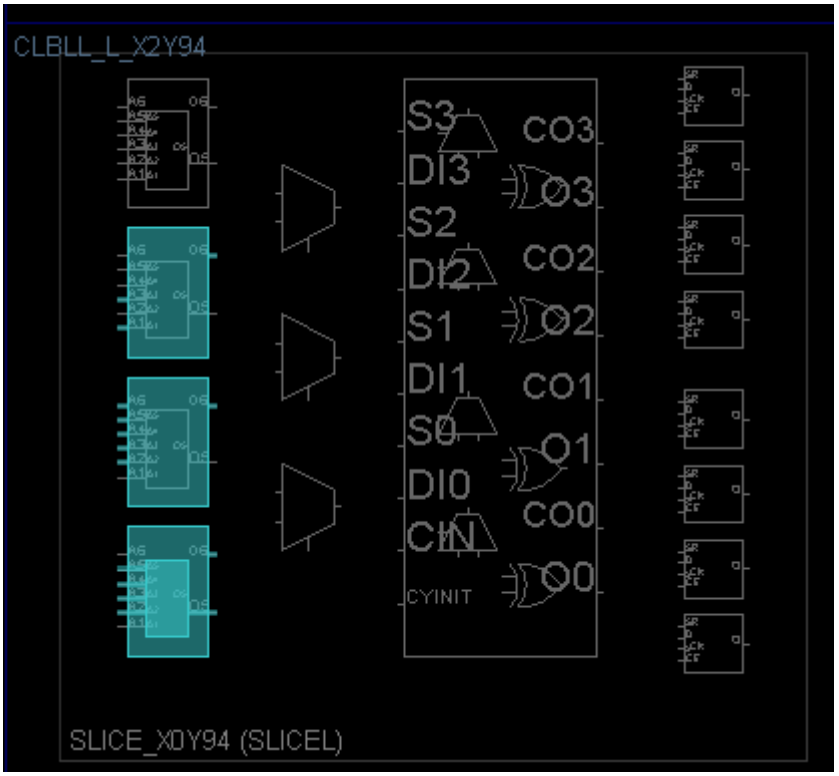
- RTL schematic

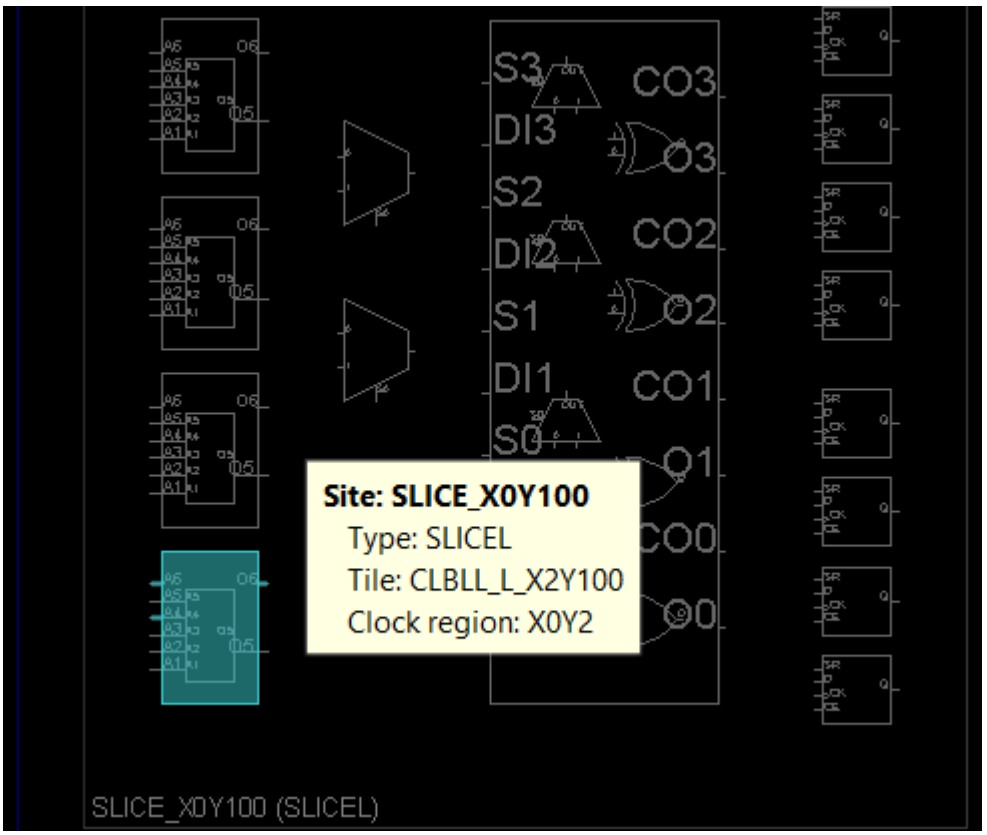


- Technology schematic



- The used luts are in the slice X0Y94 and slice X0Y100 different from with_decoder

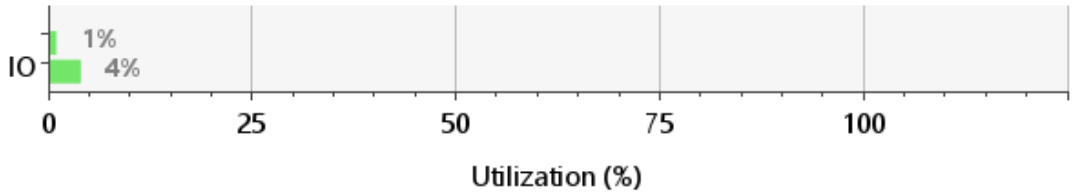




- Timing and Utilization report. Maximum combinational delay is 9.745 and 4 lut is used as we can see in the device in previous step

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f1	9.047	SLOW	2.783	FAST
a	f2	9.754	SLOW	3.044	FAST
a	f3	9.262	SLOW	2.859	FAST
b	f0	8.922	SLOW	2.688	FAST
b	f1	8.901	SLOW	2.530	FAST
b	f2	9.162	SLOW	2.804	FAST
b	f3	8.672	SLOW	2.621	FAST
c	f1	8.006	SLOW	2.359	FAST
c	f2	8.677	SLOW	2.627	FAST
c	f3	8.219	SLOW	2.438	FAST
d	f0	8.092	SLOW	2.382	FAST
d	f1	8.933	SLOW	2.646	FAST
d	f2	9.500	SLOW	2.922	FAST
d	f3	9.010	SLOW	2.735	FAST

Resource	Utilization	Available	Utilization %
LUT	4	63400	0.01
IO	8	210	3.81



- After I add the timing constraint the constraints are not met but maximum delay reduced to 8.853 and the used luts increased to 5 from 4.

Setup

Worst Negative Slack (WNS):	-2.853 ns
Total Negative Slack (TNS):	-10.460 ns
Number of Failing Endpoints:	4
Total Number of Endpoints:	4

Hold

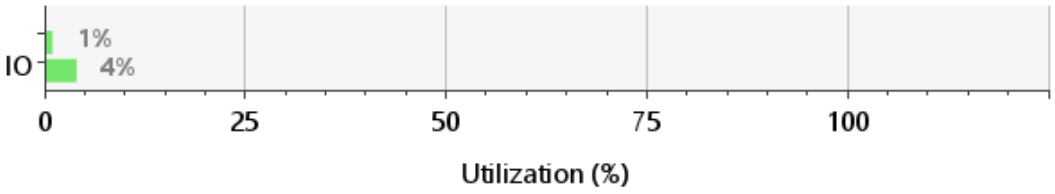
Worst Hold Slack (WHS):	inf
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4

Pulse Width

Worst Pulse Width Slack (WPWS):	NA
Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA

Timing constraints are not met.

Resource	Utilization	Available	Utilization %
LUT	5	63400	0.01
IO	8	210	3.81



From Port	To Port	Max Delay	Max Process Corner
a	f1	8.592	SLOW
a	f2	8.827	SLOW
a	f3	8.167	SLOW
b	f0	8.430	SLOW
b	f1	8.522	SLOW
b	f2	8.547	SLOW
b	f3	8.158	SLOW
c	f1	8.145	SLOW
c	f2	8.853	SLOW
c	f3	7.931	SLOW
d	f0	8.560	SLOW
d	f1	8.638	SLOW
d	f2	8.721	SLOW
d	f3	8.409	SLOW

Miscellaneous Questions

- Behavioral Simulation, an early design stage, verifies high-level functionality using VHDL or Verilog. Post-Synthesis Functional Simulation, post-synthesis, ensures functionality at a lower level, checking the synthesized netlist without detailed timing. Post-Implementation Functional Simulation, after place-and-route, considers physical placement with a focus on functional correctness and basic timing. Post-Implementation Timing Simulation, at a low level, includes detailed timing verification, ensuring the design meets specific timing requirements.
- This design performs a multiplication on ab and cd.
- The second design is easier to code because we have all the minterms..
- The first design has 9.041 ns combinational delay with constraint. The second one has maximum 8.826ns combinational delay and the third one has 8.853ns combinational delay.
- The best in terms of timing is the design with mux. The used lut number is 4, 3, 4 respectively. So the best one in terms of utilization is the decoder one.