INAx181 双向低侧和高侧电压输出电流感应放大器

1 特性

- 共模范围 (V_{CM})：–0.2V 至 +26V
- 高带宽：350kHz（A1 器件）
- 偏移电压：
  - ±150µV（最大值），V_{CM} = 0V
  - ±500µV（最大值），V_{CM} = 12V
- 输出压摆率：2V/µs
- 双向电流感应功能
- 精度：
  - ±1% 增益误差（最大值）
  - 1µV/°C 温漂（最大值）
- 增益选项：
  - 20V/V（A1 器件）
  - 50V/V（A2 器件）
  - 100V/V（A3 器件）
  - 200V/V（A4 器件）
- 瞬态电流：最大为 260µA (INA181)

2 应用

- 电机控制
- 电池监控
- 电源管理
- 照明控制
- 过流检测
- 光伏逆变器

3 说明

INA181、INA2181 和 INA4181 (INAx181) 电流检测放大器专为经成本优化的 解决方案而设计。这些器件是一系列双向电流检测放大器（也称为电流分流监控器），可在独立于电源电压的 –0.2V 至 +26V 范围内的共模电压中感测电流检测电阻器上的压降。INAx181 系列集成有一个匹配的电阻器增益网络，具有四个固定增益器件选项：20V/V、50V/V、100V/V 或 200V/V。该匹配增益电阻器网络可最大限度地减小增益误差并降低温漂。

这些器件由 2.7V 至 5.5V 单电源供电。单通道 INA181 消耗的最大电源电流为 260µA；而双通道 INA2181 消耗的最大电源电流为 500µA，四通道 INA4181 消耗的最大电源电流为 900µA。

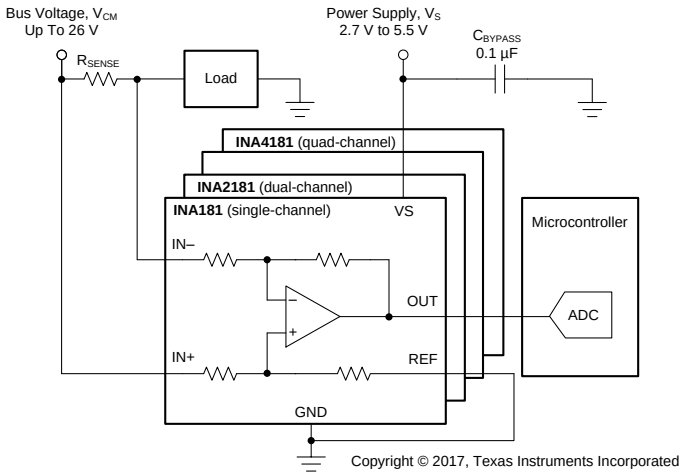
INA181 可提供 6 引脚 SOT-23 封装。INA2181 可提供 10 引脚 VSSOP 封装。INA4181 可提供 20 引脚 TSSOP 封装。所有器件选项的额定扩展工作温度范围均为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA181	SOT-23 (6)	2.90mm × 1.60mm
INA2181	VSSOP (10)	3.00mm × 3.00mm
INA4181	TSSOP (20)	6.50mm × 4.40mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。

典型应用电路



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4 修订历史记录

Changes from Revision E (July 2018) to Revision F — **Page**

- 已添加 new paragraph regarding phase reversal to end of *Input Differential Overload* section ... 21
- 已更改 Figure 57 to fix pin number typos ... 33
- 已更改 Figure 58 to fix pin number typos ... 34

Changes from Revision D (March 2018) to Revision E — **Page**

- 已更改 将 INAx180 实例更改为 INAx181（拼写错误） ... 1

Changes from Revision C (December 2017) to Revision D — **Page**

- 已更改 将 INA4181 器件从预览更改为生产数据（有效） ... 1
- 已添加 new Figure 25 for INA4181 ... 12
- 已添加 new Figure 28 for INA4181 ... 12
- 已添加 "other" to first sentence after Figure 49 to clarify channel connection in *Summing Multiple Currents* section ... 27

Changes from Revision B (November 2017) to Revision C — **Page**

- 已更改 将 INA2181 器件从预览更改为生产数据（有效） ... 1
- 已添加 "Both Inputs" to Figure 21 title ... 11
- 已添加 new Figure 24 for INA2181 ... 11
- 已添加 new Figure 25 placeholder for INA4181 ... 12
- 已添加 new Figure 27 for INA2181 ... 12
- 已添加 new Figure 28 placeholder for INA4181 ... 12
- 已更改 Figure 29 and added "(A3 Devices)" to end of title ... 12
- 已添加 new Figure 38 for INA2181 ... 14
- 已更改 "less than 150 μV" to "within ±150 μV" regarding offset voltage in *Precise Low-Side Current Sensing* section ... 19

- 已添加 text regarding RC filter and reference to application report to note at the bottom of Figure 45 23
- 已删除 V_S from Equation 3 24
- 已添加 equation and curve for f_{-3dB} to Figure 48..... 25
- 已添加 new content to *Summing Multiple Currents* section and moved to *Application Information* section..... 27
- 已添加 new content to *Detecting Leakage Currents* section and moved to *Application Information* section..... 28
- 已添加 new bullet to *Layout Guidelines* section 33

Changes from Revision A (August 2017) to Revision B **Page**

- 已添加 在产品说明书中添加了 INA4181 预览器件和相关内容 1
- 已更改 design parameter name in Table 3 from "Accuracy" to "Current sensing error" for clarity 30
- 已更改 "RMS" to "RSS" in reference to equation 7 31

Changes from Original (April 2017) to Revision A **Page**

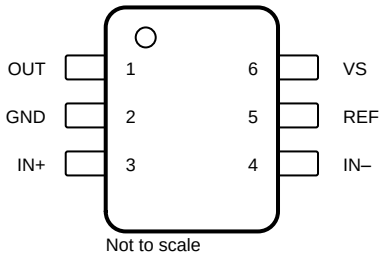
- 已添加 在产品说明书中添加了 INA2181 预览器件和相关内容 1

5 Device Comparison Table

PRODUCT	NUMBER OF CHANNELS	GAIN (V/V)
INA181A1	1	20
INA181A2	1	50
INA181A3	1	100
INA181A4	1	200
INA2181A1	2	20
INA2181A2	2	50
INA2181A3	2	100
INA2181A4	2	200
INA4181A1	4	20
INA4181A2	4	50
INA4181A3	4	100
INA4181A4	4	200

6 Pin Configuration and Functions

INA181: DBV Package
6-Pin SOT-23
Top View



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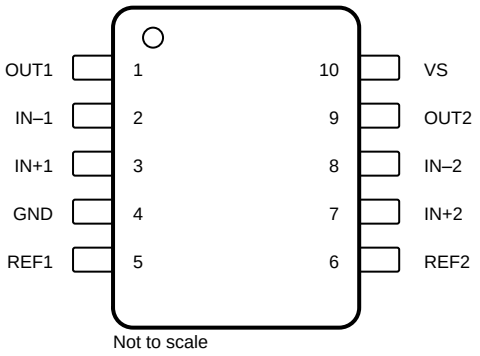
Pin Functions: INA181 (Single Channel)

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	Analog	Ground
IN–	4	Analog input	Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	3	Analog input	Current-sense amplifier positive input. For high-side applications, connect to bus-voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
OUT	1	Analog output	Output voltage
REF	5	Analog input	Reference input
VS	6	Analog	Power supply, 2.7 V to 5.5 V

INA2181: DGS Package
10-Pin VSSOP
Top View



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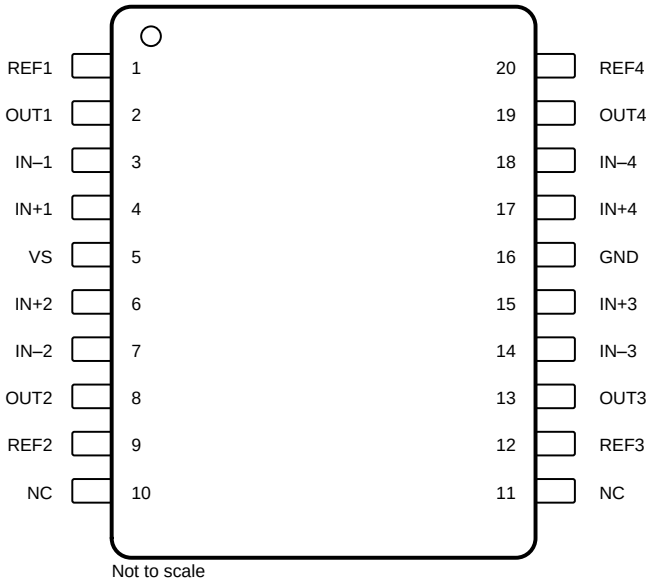
INA4181: PW Package
20-Pin TSSOP
Top View



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Pin Functions: INA2181 (Dual Channel) and INA4181 (Quad Channel)

PIN			TYPE	DESCRIPTION
NAME	INA2181	INA4181		
GND	4	16	Analog	Ground
IN–1	2	3	Analog input	Current-sense amplifier negative input for channel 1. For high-side applications, connect to load side of channel-1 sense resistor. For low-side applications, connect to ground side of channel-1 sense resistor.
IN+1	3	4	Analog input	Current-sense amplifier positive input for channel 1. For high-side applications, connect to bus-voltage side of channel-1 sense resistor. For low-side applications, connect to load side of channel-1 sense resistor.
IN–2	8	7	Analog input	Current-sense amplifier negative input for channel 2. For high-side applications, connect to load side of channel-2 sense resistor. For low-side applications, connect to ground side of channel-2 sense resistor.
IN+2	7	6	Analog input	Current-sense amplifier positive input for channel 2. For high-side applications, connect to bus-voltage side of channel-2 sense resistor. For low-side applications, connect to load side of channel-2 sense resistor.
IN–3	—	14	Analog input	Current-sense amplifier negative input for channel 3. For high-side applications, connect to load side of channel-3 sense resistor. For low-side applications, connect to ground side of channel-3 sense resistor.
IN+3	—	15	Analog input	Current-sense amplifier positive input for channel 3. For high-side applications, connect to bus-voltage side of channel-3 sense resistor. For low-side applications, connect to load side of channel-3 sense resistor.
IN–4	—	18	Analog input	Current-sense amplifier negative input for channel 4. For high-side applications, connect to load side of channel-4 sense resistor. For low-side applications, connect to ground side of channel-4 sense resistor.
IN+4	—	17	Analog input	Current-sense amplifier positive input for channel 4. For high-side applications, connect to bus-voltage side of channel-4 sense resistor. For low-side applications, connect to load side of channel-4 sense resistor.
NC	—	10, 11	—	NC denotes no internal connection. These pins can be left floating or connected to any voltage between V_S and ground.
OUT1	1	2	Analog output	Channel 1 output voltage
OUT2	9	8	Analog output	Channel 2 output voltage
OUT3	—	13	Analog output	Channel 3 output voltage
OUT4	—	19	Analog output	Channel 4 output voltage

Pin Functions: INA2181 (Dual Channel) and INA4181 (Quad Channel) (continued)

PIN			TYPE	DESCRIPTION
NAME	INA2181	INA4181		
REF1	5	1	Analog input	Channel 1 reference voltage, 0 to V_S
REF2	6	9	Analog input	Channel 2 reference voltage, 0 to V_S
REF3	—	12	Analog input	Channel 3 reference voltage, 0 to V_S
REF4	—	20	Analog input	Channel 4 reference voltage, 0 to V_S
VS	10	5	Analog	Power supply pin, 2.7 V to 5.5 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs, IN+, IN–(2)	Differential (V_{IN+}) – ($V_{IN–}$)	–26	26	V
	Common-mode(3)	GND – 0.3	26	
Input voltage range	at REF pin	GND – 0.3	V_S + 0.3	V
Output voltage		GND – 0.3	V_S + 0.3	V
Maximum output current, I_{OUT}			8	mA
Operating free-air temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5 mA.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage (IN+ and IN–)	–0.2	12	26	V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		INA181 DBV (SOT-23) 6 PINS	INA2181 DGS (VSSOP) 10 PINS	INA4181 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	198.7	177.3	97.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.9	68.7	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.3	98.4	48.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.3	12.6	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.0	96.9	47.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, V_{IN+} = 12 V, and V_{SENSE} = V_{IN+} – $V_{IN–}$ (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
CMRR	Common-mode rejection ratio, RTI (1)	V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV, T_A = –40°C to +125°C		84	100		dB
V_{OS}	Offset voltage, RTI	V_{SENSE} = 0 mV			±100	±500	µV
		V_{SENSE} = 0 mV, V_{IN+} = 0 V			±25	±150	µV
dV_{OS}/dT	Offset drift, RTI	V_{SENSE} = 0 mV, T_A = –40°C to +125°C			0.2	1	µV/°C
PSRR	Power-supply rejection ratio, RTI	V_S = 2.7 V to 5.5 V, V_{IN+} = 12 V, V_{SENSE} = 0 mV			±8	±40	µV/V
I_{IB}	Input bias current	V_{SENSE} = 0 mV, V_{IN+} = 0 V			-6		µA
		V_{SENSE} = 0 mV			75		µA
I_{IO}	Input offset current	V_{SENSE} = 0 mV			±0.05		µA
OUTPUT							
G	Gain	A1 devices			20		V/V
		A2 devices			50		V/V
		A3 devices			100		V/V
		A4 devices			200		V/V
E_G	Gain error	V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40°C to +125°C			±0.1%	±1%	
	Gain error vs temperature	T_A = –40°C to +125°C			1.5	20	ppm/°C
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V			±0.01%		
	Maximum capacitive load	No sustained oscillation			1		nF
VOLTAGE OUTPUT (2)							
V_{SP}	Swing to V_S power-supply rail (3)	R_L = 10 kΩ to GND, T_A = –40°C to +125°C			(V_S) – 0.02	(V_S) – 0.03	V
V_{SN}	Swing to GND (3)	R_L = 10 kΩ to GND, T_A = –40°C to +125°C			(V_{GND}) + 0.0005	(V_{GND}) + 0.005	V
FREQUENCY RESPONSE							
BW	Bandwidth	A1 devices, C_{LOAD} = 10 pF			350		kHz
		A2 devices, C_{LOAD} = 10 pF			210		kHz
		A3 devices, C_{LOAD} = 10 pF			150		kHz
		A4 devices, C_{LOAD} = 10 pF			105		kHz
SR	Slew rate				2		V/µs
NOISE, RTI (1)							
	Voltage noise density				40		nV/√Hz
POWER SUPPLY							
I_Q	Quiescent current	INA181	V_{SENSE} = 0 mV		195	260	µA
			V_{SENSE} = 0 mV, T_A = –40°C to +125°C			300	µA
		INA2181	V_{SENSE} = 0 mV		356	500	µA
			V_{SENSE} = 0 mV, T_A = –40°C to +125°C			520	µA
		INA4181	V_{SENSE} = 0 mV		690	900	µA
			V_{SENSE} = 0 mV, T_A = –40°C to +125°C			1000	µA

(1) RTI = referred-to-input.
(2) See 图 19.
(3) Swing specifications are tested with an overdriven input condition.

7.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

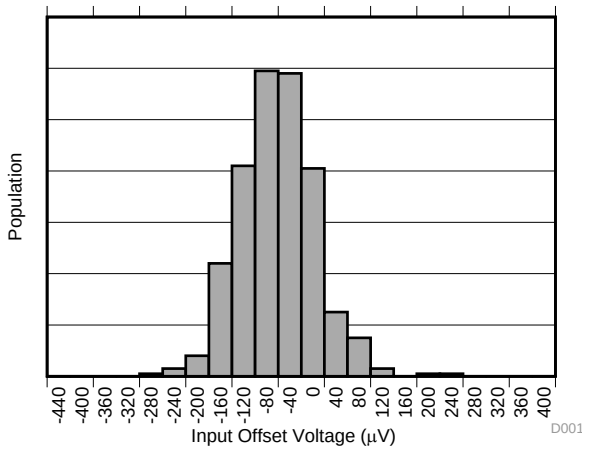


图 1. Input Offset Voltage Production Distribution A1

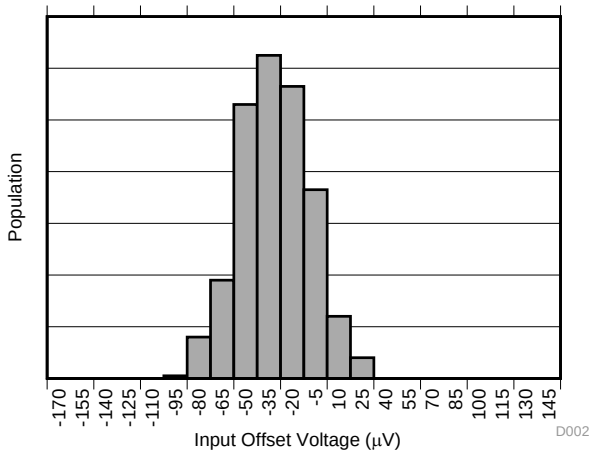


图 2. Input Offset Voltage Production Distribution A2

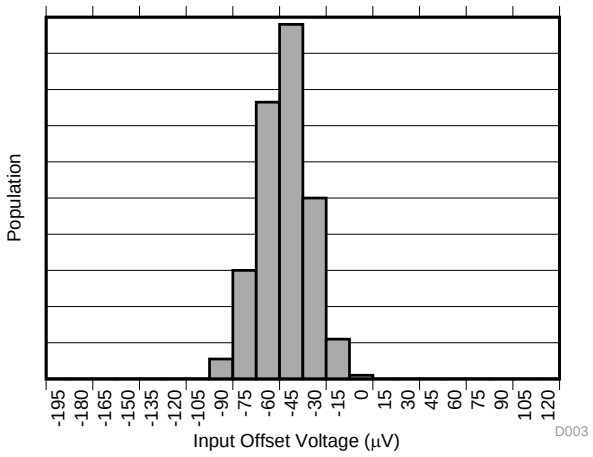


图 3. Input Offset Voltage Production Distribution A3

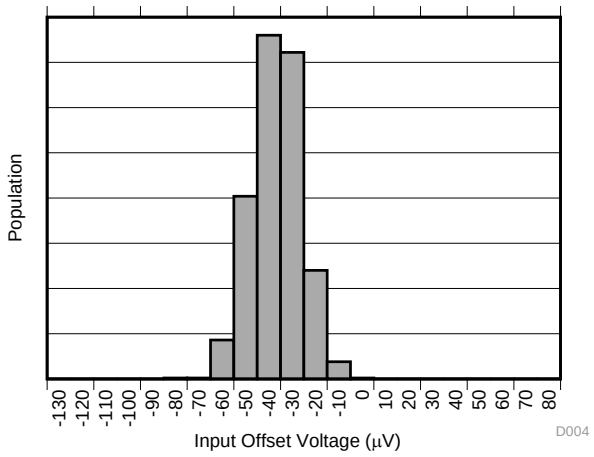


图 4. Input Offset Voltage Production Distribution A4

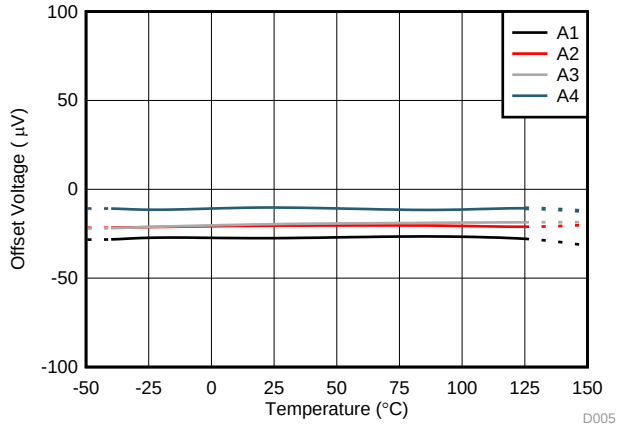


图 5. Offset Voltage vs Temperature

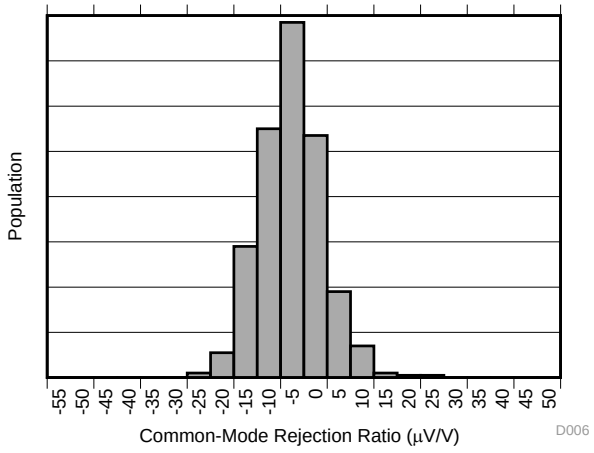


图 6. Common-Mode Rejection Production Distribution A1

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

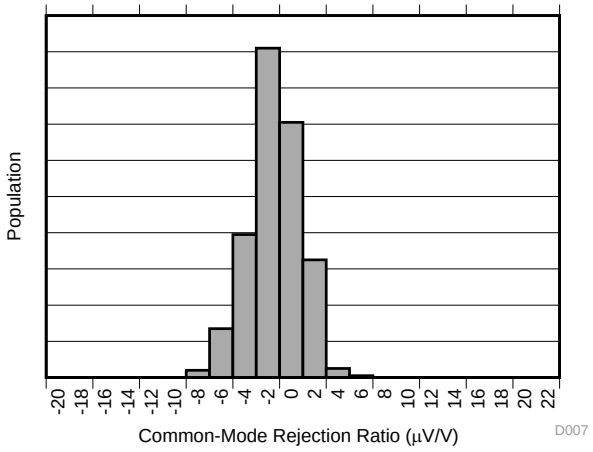


图 7. Common-Mode Rejection Production Distribution A2

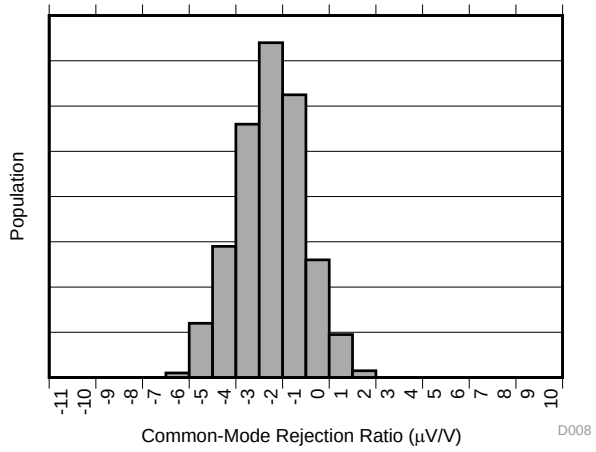


图 8. Common-Mode Rejection Production Distribution A3

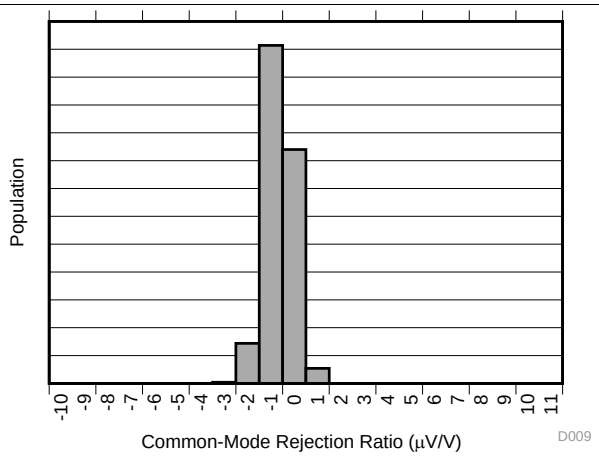


图 9. Common-Mode Rejection Production Distribution A4

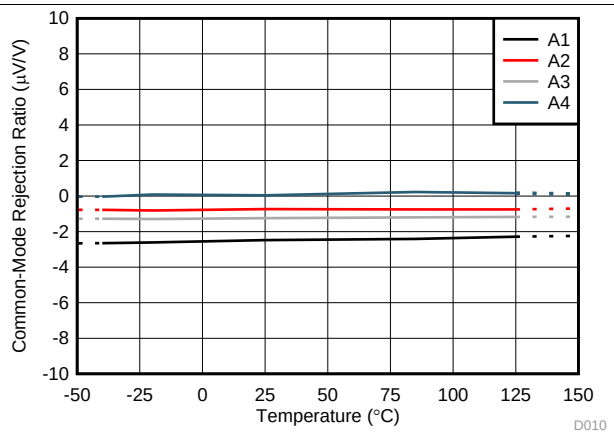


图 10. Common-Mode Rejection Ratio vs Temperature

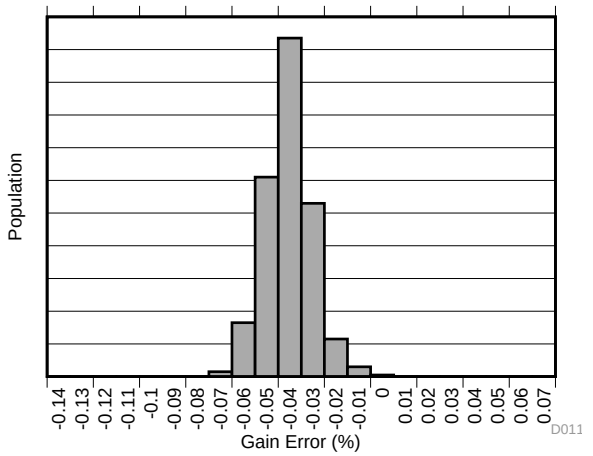


图 11. Gain Error Production Distribution A1

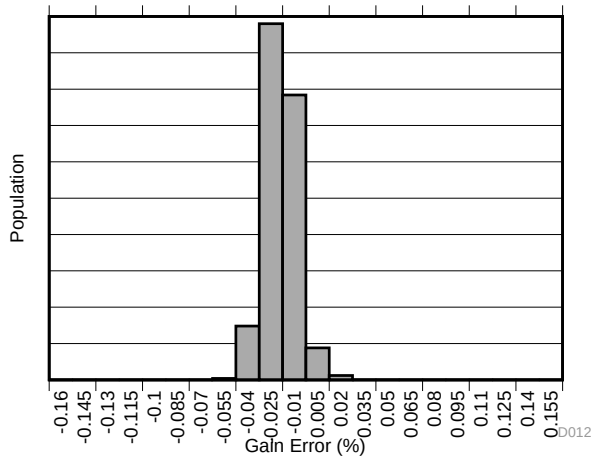


图 12. Gain Error Production Distribution A2

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

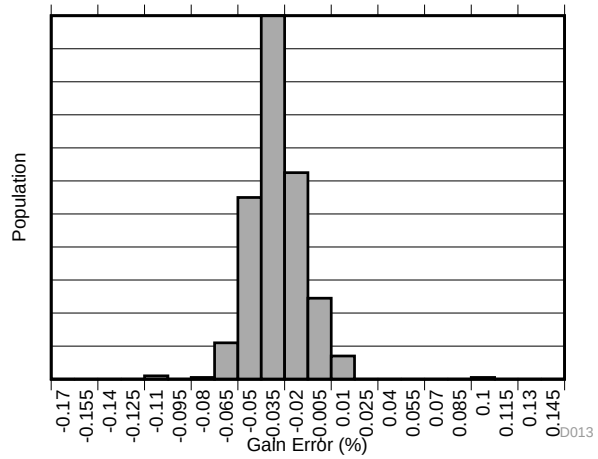


图 13. Gain Error Production Distribution A3

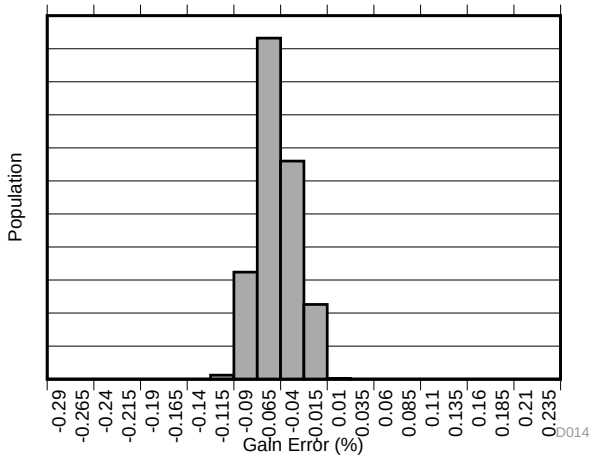


图 14. Gain Error Production Distribution A4

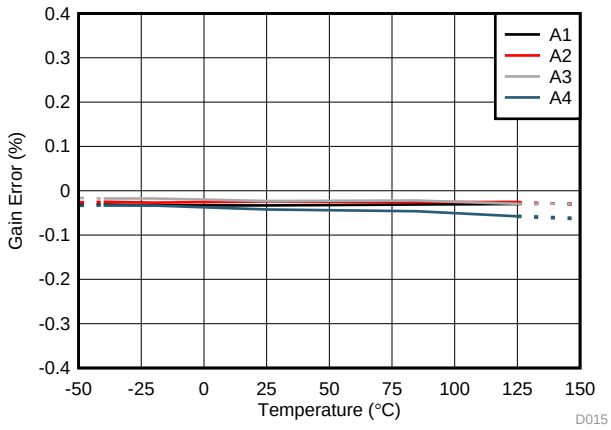


图 15. Gain Error vs Temperature

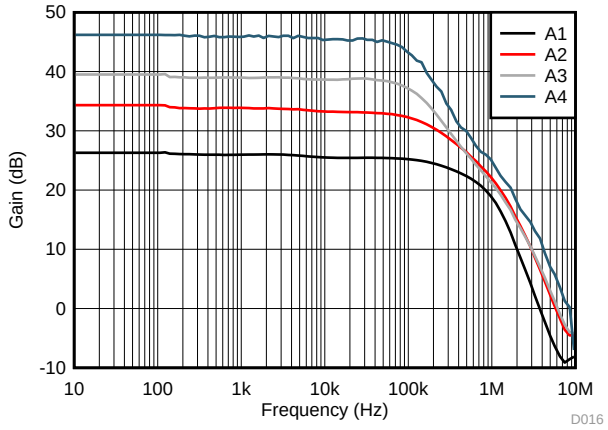


图 16. Gain vs Frequency

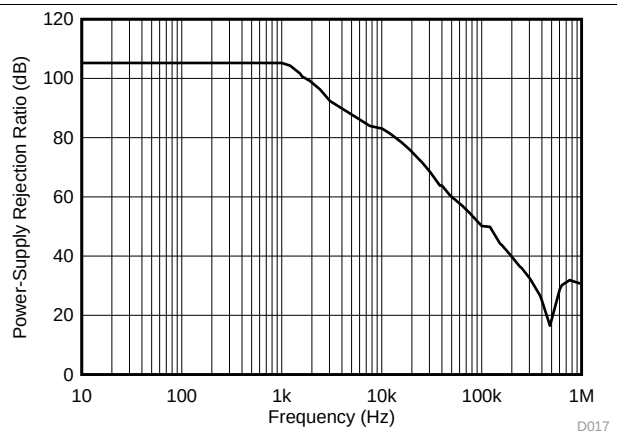


图 17. Power-Supply Rejection Ratio vs Frequency

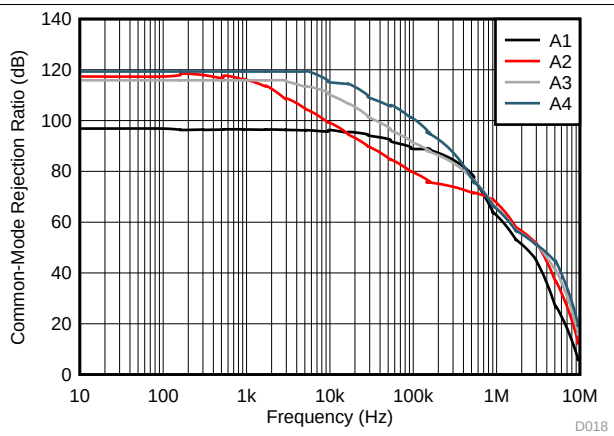


图 18. Common-Mode Rejection Ratio vs Frequency

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

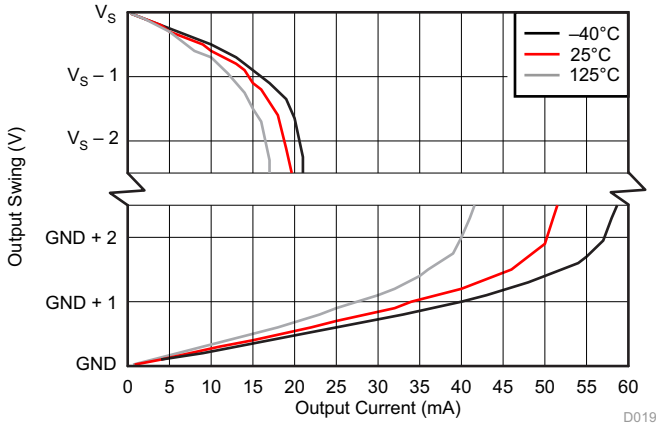


图 19. Output Voltage Swing vs Output Current

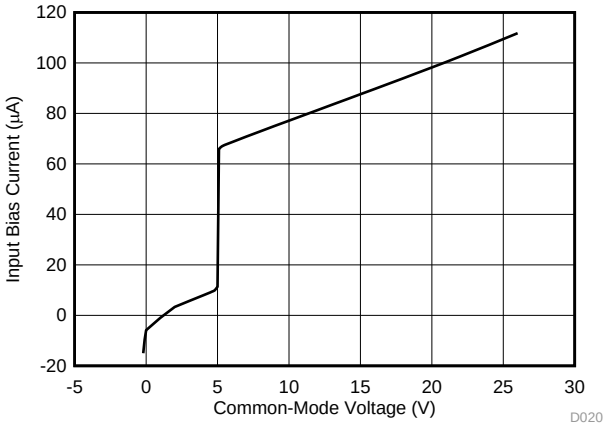


图 20. Input Bias Current vs Common-Mode Voltage

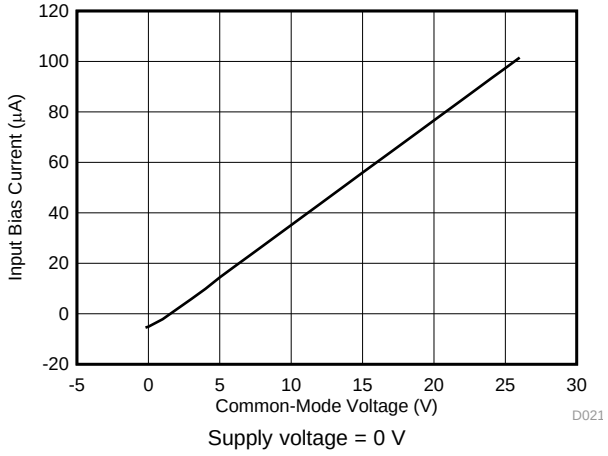


图 21. Input Bias Current vs Common-Mode Voltage (Both Inputs, Shutdown)

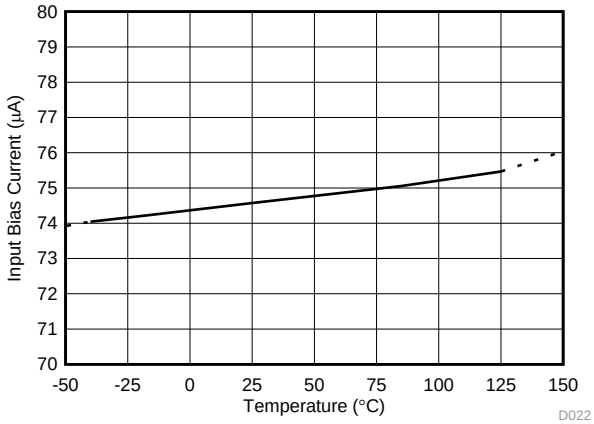


图 22. Input Bias Current vs Temperature

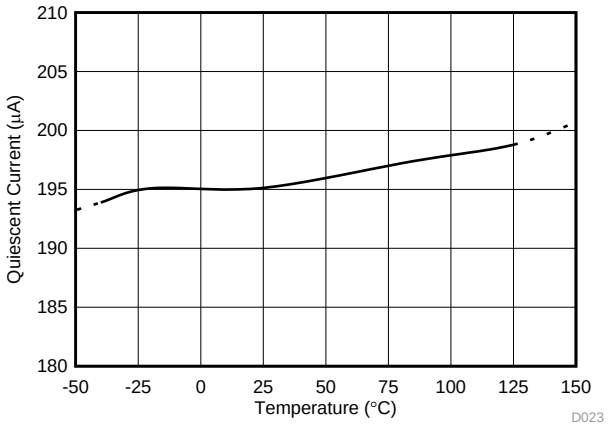


图 23. Quiescent Current vs Temperature (INA181)

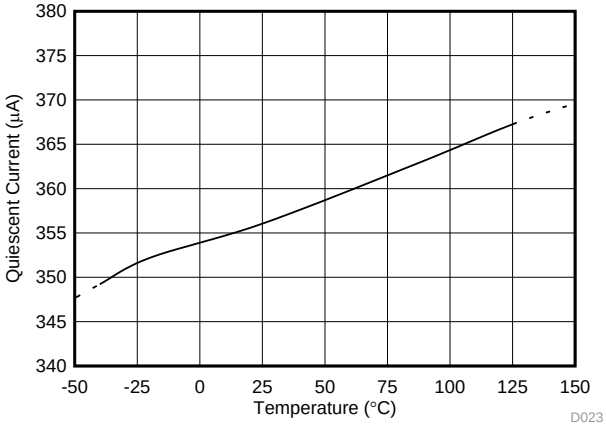


图 24. Quiescent Current vs Temperature (INA2181)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

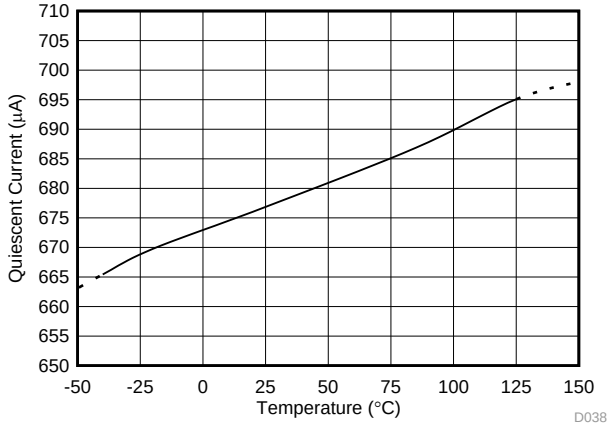


图 25. Quiescent Current vs Temperature (INA4181)

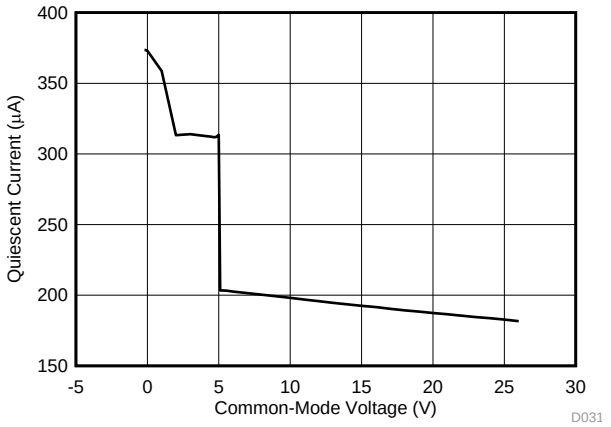


图 26. I_Q vs Common-Mode Voltage (INA181)

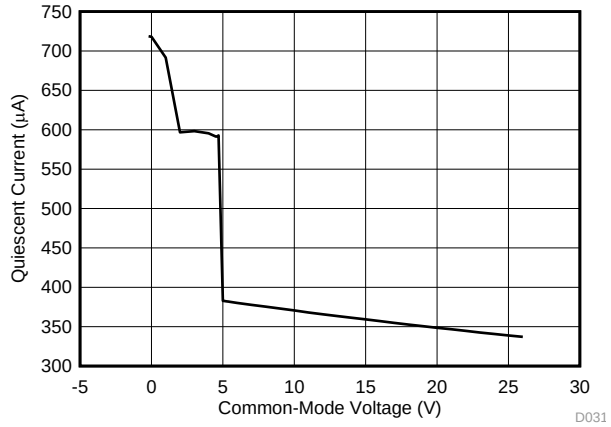


图 27. I_Q vs Common-Mode Voltage (INA2181)

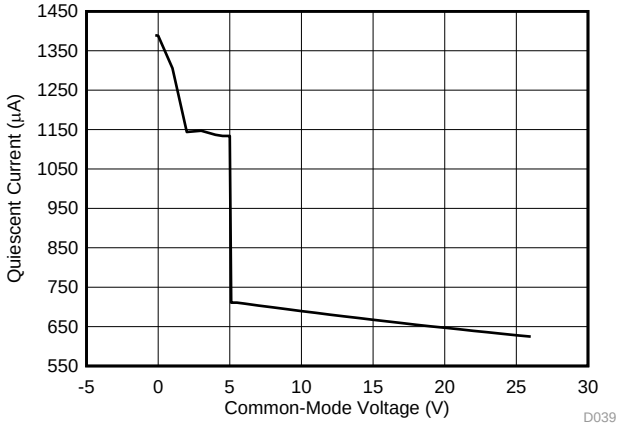


图 28. I_Q vs Common-Mode Voltage (INA4181)

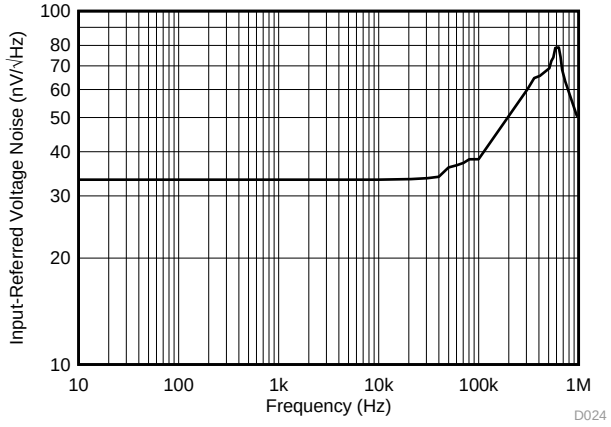


图 29. Input-Referred Voltage Noise vs Frequency (A3 Devices)

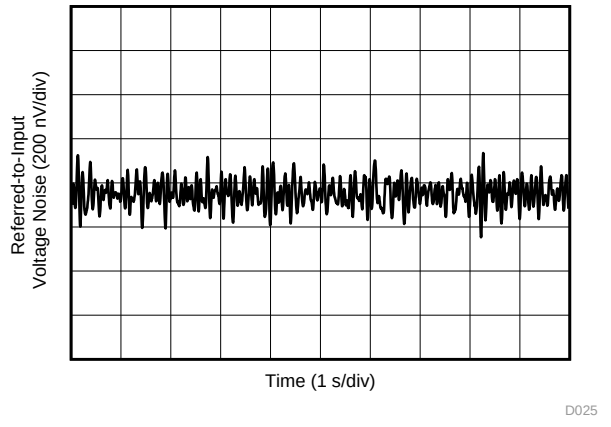
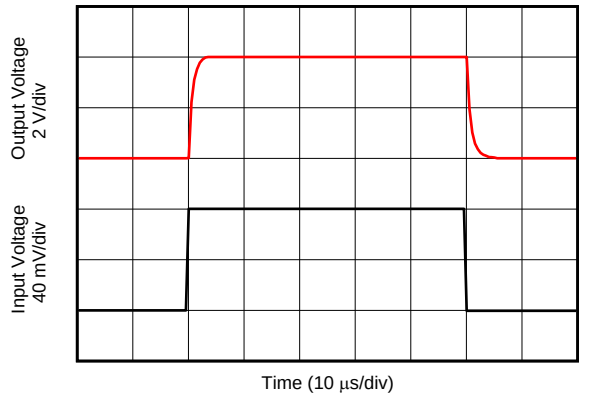


图 30. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)



80-mV_{PP} input step

图 31. Step Response

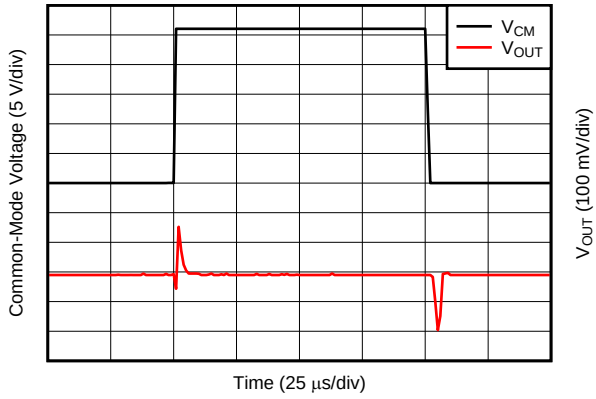


图 32. Common-Mode Voltage Transient Response

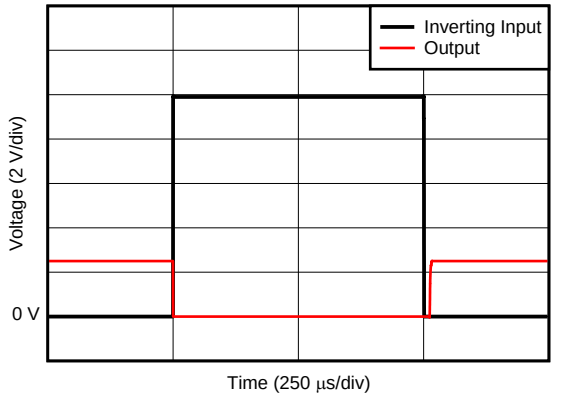


图 33. Inverting Differential Input Overload

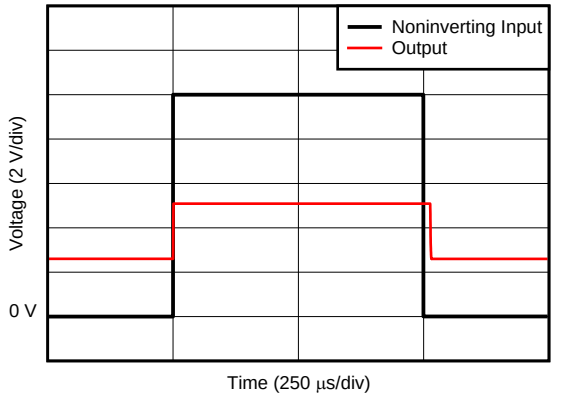


图 34. Noninverting Differential Input Overload

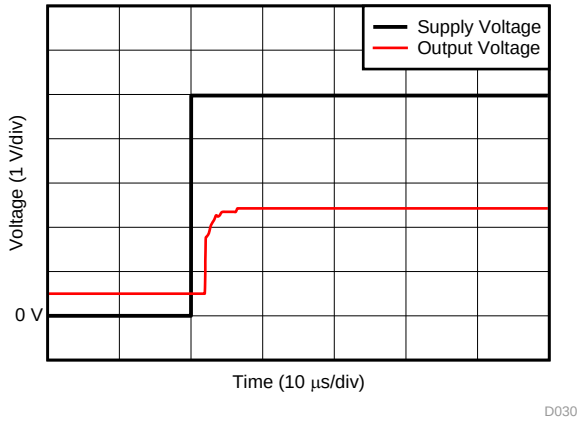


图 35. Start-Up Response

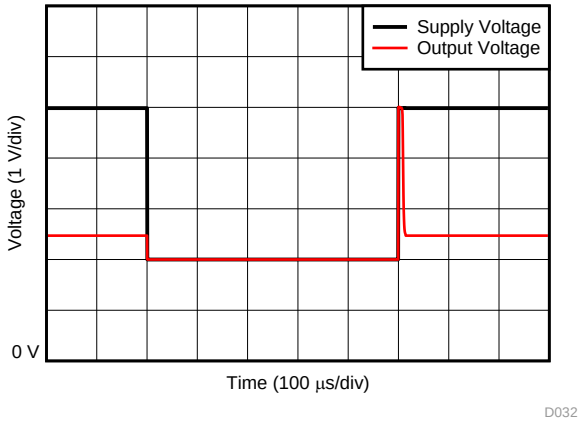


图 36. Brownout Recovery

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, V_{REF} = V_S / 2, and V_{IN+} = 12 V (unless otherwise noted)

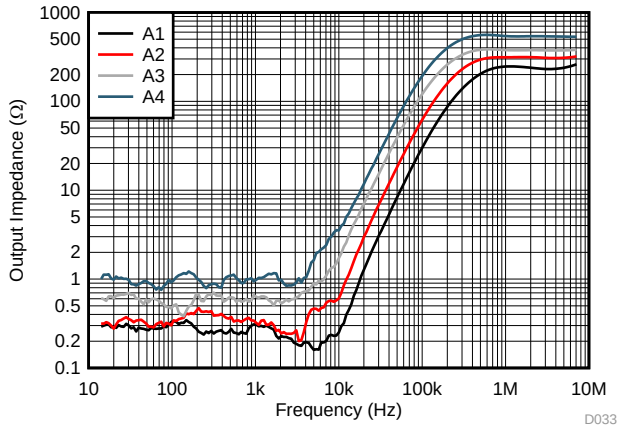


图 37. Output Impedance vs Frequency

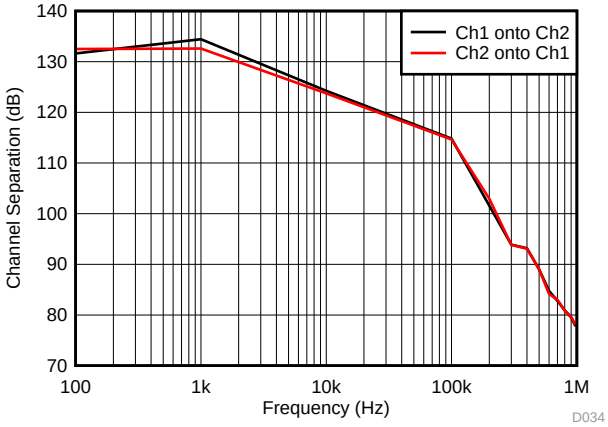


图 38. Channel Separation vs Frequency (INA2181)

8 Detailed Description

8.1 Overview

The INA181, INA2181, and INA4181 (INAx181) are 26-V common-mode, current-sensing amplifiers used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V, and the devices can be powered from supply voltages as low as 2.7 V.

8.2 Functional Block Diagrams

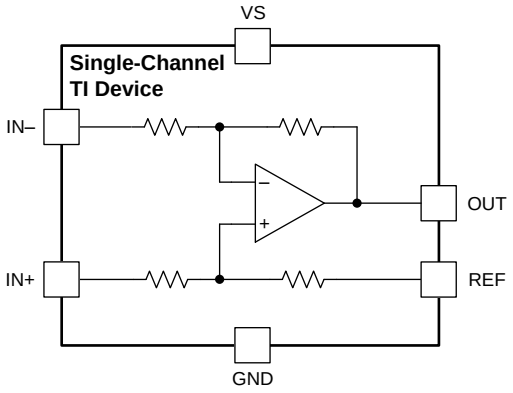


图 39. INA181 Functional Block Diagram

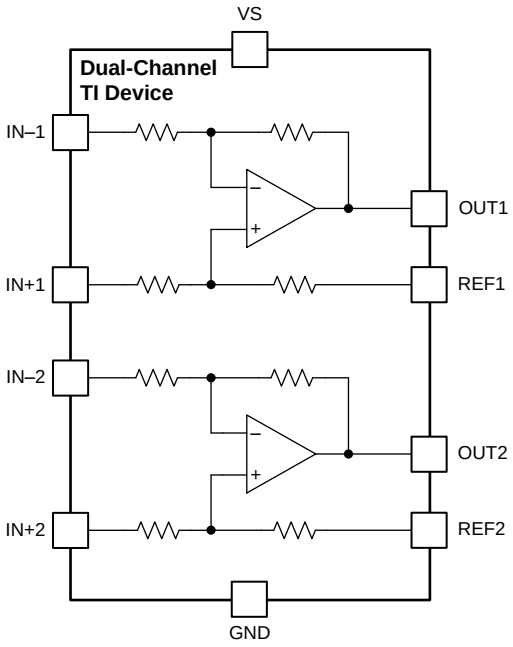


图 40. INA2181 Functional Block Diagram

Functional Block Diagrams (接下页)

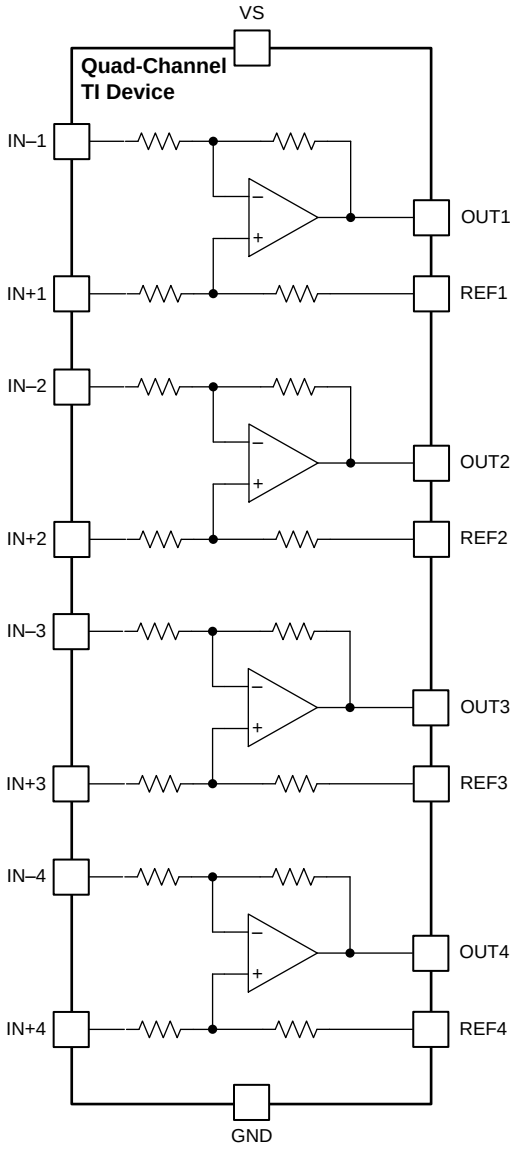


图 41. INA4181 Functional Block Diagram

8.3 Feature Description

8.3.1 High Bandwidth and Slew Rate

The INAx181 support small-signal bandwidths as high as 350 kHz, and large-signal slew rates of 2 V/µs. The ability to detect rapid changes in the sensed current, as well as the ability to quickly slew the output, make the INAx181 a good choice for applications that require a quick response to input current changes. One application that requires high bandwidth and slew rate is low-side motor control, where the ability to follow rapid changing current in the motor allows for more accurate control over a wider operating range. Another application that requires higher bandwidth and slew rates is system fault detection, where the INAx181 are used with an external comparator and a reference to quickly detect when the sensed current is out of range.

8.3.2 Bidirectional Current Monitoring

The INA181 senses current flow through a sense resistor in both directions. The bidirectional current-sensing capability is achieved by applying a voltage at the REF pin to offset the output voltage. A positive differential voltage sensed at the inputs results in an output voltage that is greater than the applied reference voltage; likewise, a negative differential voltage at the inputs results in output voltage that is less than the applied reference voltage. The output voltage of the current-sense amplifier is shown in 公式 1.

$$V_{OUT} = \left(I_{LOAD} \times R_{SENSE} \times GAIN\right) + V_{REF} \quad (1)$$

where

- I_{LOAD} is the load current to be monitored.
- R_{SENSE} is the current-sense resistor.
- GAIN is the gain option of the selected device.
- V_{REF} is the voltage applied to the REF pin.

8.3.3 Wide Input Common-Mode Voltage Range

The INAx181 support input common-mode voltages from –0.2 V to +26 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S) as long as V_S stays within the operational range of 2.7 V to 5.5 V. The ability to operate with common-mode voltages greater or less than V_S allow the INAx181 to be used in high-side, as well as low-side, current-sensing applications, as shown in 图 42.

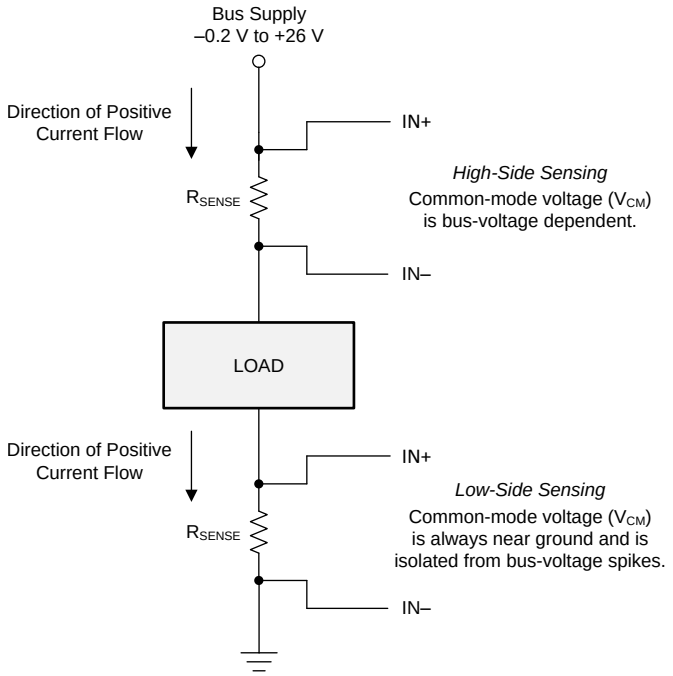


图 42. High-Side and Low-Side Sensing Connections

Feature Description (接下页)

8.3.4 Precise Low-Side Current Sensing

When used in low-side current sensing applications the offset voltage of the INAx181 is within ±150 µV. The low offset performance of the INAx181 has several benefits. First, the low offset allows these devices to be used in applications that must measure current over a wide dynamic range. In this case, the low offset improves the accuracy when the sensed currents are on the low end of the measurement range. Another advantage of low offset is the ability to sense lower voltage drop across the sense resistor accurately, thus allowing a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current sense circuit, and help improve the power efficiency of the end application.

The gain error of the INAx181 is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this voltage becomes the dominant source of error in the current sense measurement.

8.3.5 Rail-to-Rail Output Swing

The INAx181 allow linear current sensing operation with the output close to the supply rail and GND. The maximum specified output swing to the positive rail is 30 mV, and the maximum specified output swing to GND is only 5 mV. In order to compare the output swing of the INAx181 to an equivalent operational amplifier (op amp), the inputs are overdriven to approximate the open-loop condition specified in op amp data sheets. The current-sense amplifier is a closed-loop system; therefore, the output swing to GND can be limited by the product of the offset voltage and amplifier gain during unidirectional operation (V_{REF} = 0 V).

For devices that have positive offset voltages, the swing to GND is limited by the larger of either the offset voltage multiplied by the gain or the swing to GND specified in the *Electrical Characteristics* table.

For example, in an application where the INA181A4 (gain = 200 V/V) is used for low-side current sensing and the device has an offset of 40 µV, the product of the device offset and gain results in a value of 8 mV, greater than the specified negative swing value. Therefore, the swing to GND for this example is 8 mV. If the same device has an offset of –40 µV, then the calculated zero differential signal is –8 mV. In this case, the offset helps overdrive the swing in the negative direction, and swing performance is consistent with the value specified in the *Electrical Characteristics* table.

The offset voltage is a function of the common-mode voltage as determined by the CMRR specification; therefore, the offset voltage increases when higher common-mode voltages are present. The increase in offset voltage limits how low the output voltage can go during a zero-current condition when operating at higher common-mode voltages with V_{REF} = 0 V . The typical limitation of the zero-current output voltage vs common-mode voltage for each gain option is shown in 图 43.

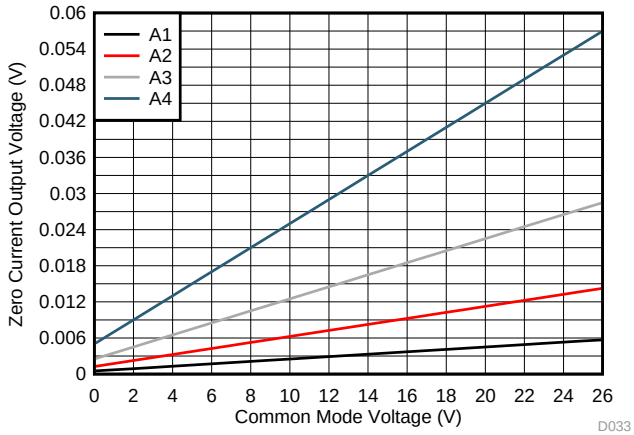


图 43. Zero-Current Output Voltage vs Common-Mode Voltage

8.4 Device Functional Modes

8.4.1 Normal Mode

The INAx181 are in normal operation when the following conditions are met:

- The power supply voltage (V_S) is between 2.7 V and 5.5 V.
- The common-mode voltage (V_{CM}) is within the specified range of –0.2 V to +26 V.
- The maximum differential input signal times gain plus V_{REF} is less than V_S minus the output voltage swing to V_S.
- The minimum differential input signal times gain plus V_{REF} is greater than the swing to GND (see the *Rail-to-Rail Output Swing* section).

During normal operation, these devices produce an output voltage that is the *gained-up* representation of the difference voltage from IN+ to IN– plus the reference voltage at V_{REF}.

8.4.2 Unidirectional Mode

These devices can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in 图 44. When the current flows from the bus supply to the load, the input signal across IN+ to IN– increases, and causes the output voltage at the OUT pin to increase.

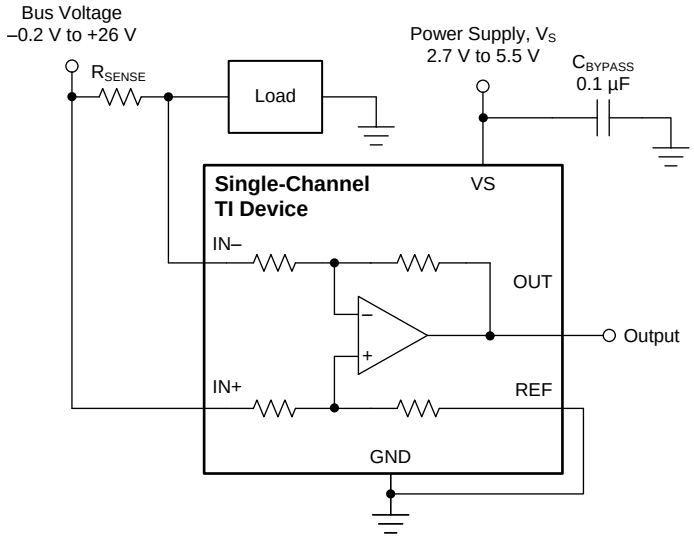


图 44. Unidirectional Application

The linear range of the output stage is limited by how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, buffer the reference voltage connected to the REF pin.

A less-frequently used output biasing method is to connect the REF pin to the power-supply voltage, V_S. This method results in the output voltage saturating at 200 mV less than the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed V_S.

Device Functional Modes (接下页)

8.4.3 Bidirectional Mode

The INAx181 are bidirectional, current-sense amplifiers capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flowing through the resistor can change directions.

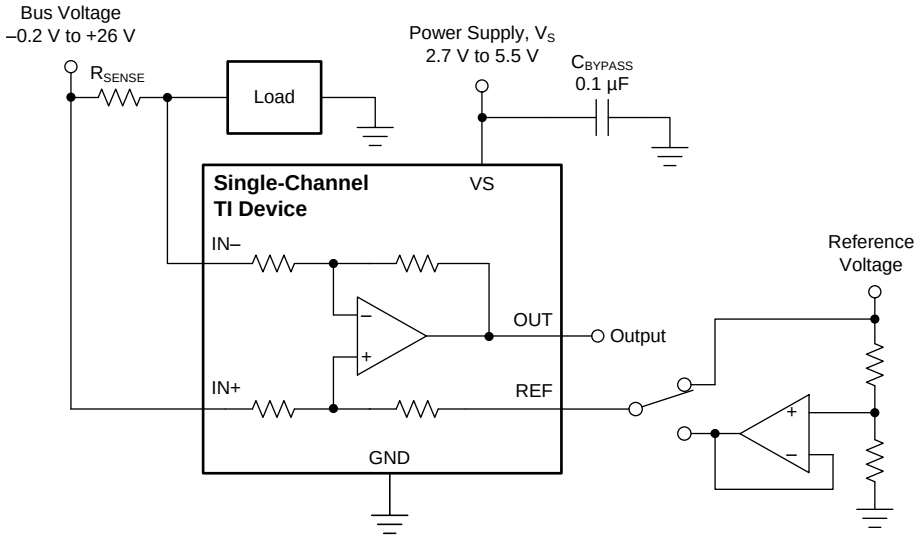


图 45. Bidirectional Application

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in 图 45. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above V_{REF} for positive differential signals (relative to the IN– pin) and responds by decreasing below V_{REF} for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V_S. For bidirectional applications, V_{REF} is typically set at mid-scale for equal signal range in both current directions. In some cases, however, V_{REF} is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

8.4.4 Input Differential Overload

If the differential input voltage ($V_{IN+} – V_{IN–}$) times gain exceeds the voltage swing specification, the INAx181 drive the output as close as possible to the positive supply or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INAx181 returns to the expected value approximately 20 µs after the fault condition is removed.

When the INAx181 output is driven to either the supply rail or ground, increasing the differential input voltage does not damage the device as long as the absolute maximum ratings are not violated. Following these guidelines, the INAx181 output maintains polarity, and does not suffer from phase reversal.

Device Functional Modes (接下页)

8.4.5 Shutdown Mode

Although the INAx181 do not have a shutdown pin, the low power consumption of these devices allows the output of a logic gate or transistor switch to power the INAx181. This gate or switch turns on and off the INAx181 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INAx181 in shutdown mode, as shown in 图 46.

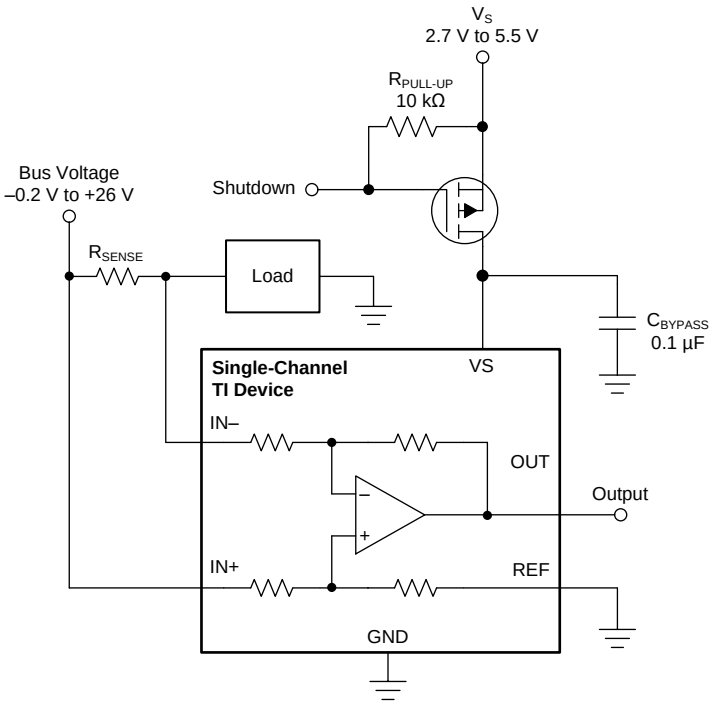


图 46. Basic Circuit to Shut Down the INA181 With a Grounded Reference

There is typically more than 500 kΩ of impedance (from the combination of 500-kΩ feedback and input gain set resistors) from each input of the INAx181 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the voltage at the connection. For example, if the REF pin is grounded, the calculation of the effect of the 500 kΩ impedance from the shunt to ground is straightforward. However, if the reference is powered while the INAx181 is in shutdown mode, instead of assuming 500 kΩ to ground, assume 500 kΩ to the reference voltage.

Regarding the 500-kΩ path to the output pin, the output stage of a disabled INAx181 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage present across a 500-kΩ resistor.

As a final note, as long as the shunt common-mode voltage is greater than V_S when the device is powered up, there is an additional and well-matched 55-µA typical current that flows in each of the inputs. If less than V_S, the common-mode input currents are negligible, and the only current effects are the result of the 500-kΩ resistors.

9 Application and Implementation

注

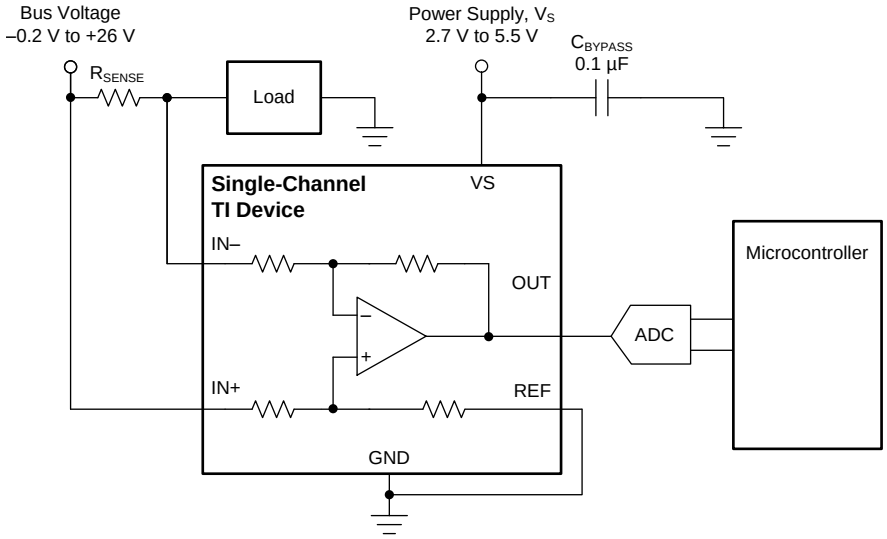
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INAx181 amplify the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed in previous sections.

9.1.1 Basic Connections

图 47 shows the basic connections of the INA181. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.



NOTE: To help eliminate ground offset errors between the device and the analog-to-digital converter (ADC), connect the REF pin to the ADC reference input and then to ground. For best performance, use an RC filter between the output of the INAx181 and the ADC. See *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT* for more details.

图 47. Basic Connections for the INA181

A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

Application Information (接下页)

9.1.2 R_{SENSE} and Device Gain Selection

The accuracy of the INAx181 is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application. The INAx181 have typical input bias currents of 75 µA for each input when operated at a 12-V common-mode voltage input. When large current-sense resistors are used, these bias currents cause increased offset error and reduced common-mode rejection. Therefore, using current-sense resistors larger than a few ohms is generally not recommended for applications that require current-monitoring accuracy. A second common restriction on the value of the current-sense resistor is the maximum allowable power dissipation that is budgeted for the resistor. 公式 2 gives the maximum value for the current sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2}$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current that will flow through R_{SENSE}. (2)

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, V_S, and device swing to rail limitations. In order to make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. 公式 3 provides the maximum values of R_{SENSE} and GAIN to keep the device from hitting the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} - V_{REF}$$

where:

- I_{MAX} is the maximum current that will flow through R_{SENSE}.
- GAIN is the gain of the current sense-amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.
- V_{REF} is the externally applied voltage on the REF pin. (3)

To avoid positive output swing limitations when selecting the value of R_{SENSE}, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device in order to avoid positive swing limitations.

The negative swing limitation places a limit on how small of a sense resistor can be used in a given application. 公式 4 provides the limit on the minimum size of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} - V_{REF}$$

where:

- I_{MIN} is the minimum current that will flow through R_{SENSE}.
- GAIN is the gain of the current sense amplifier.
- V_{SN} is the negative output swing of the device (see Rail-to-Rail Output Swing).
- V_{REF} is the externally applied voltage on the REF pin. (4)

In addition to adjusting the offset and gain, the voltage applied to the REF pin can be slightly increased to avoid negative swing limitations.

Application Information (接下页)

9.1.3 Signal Filtering

Provided that the INAx181 output is connected to a high impedance input, the best location to filter is at the device output using a simple RC network from OUT to GND. Filtering at the output attenuates high-frequency disturbances in the common-mode voltage, differential input signal, and INAx181 power-supply voltage. If filtering at the output is not possible, or filtering of only the differential input signal is required, it is possible to apply a filter at the input pins of the device. 图 48 provides an example of how a filter can be used on the input pins of the device.

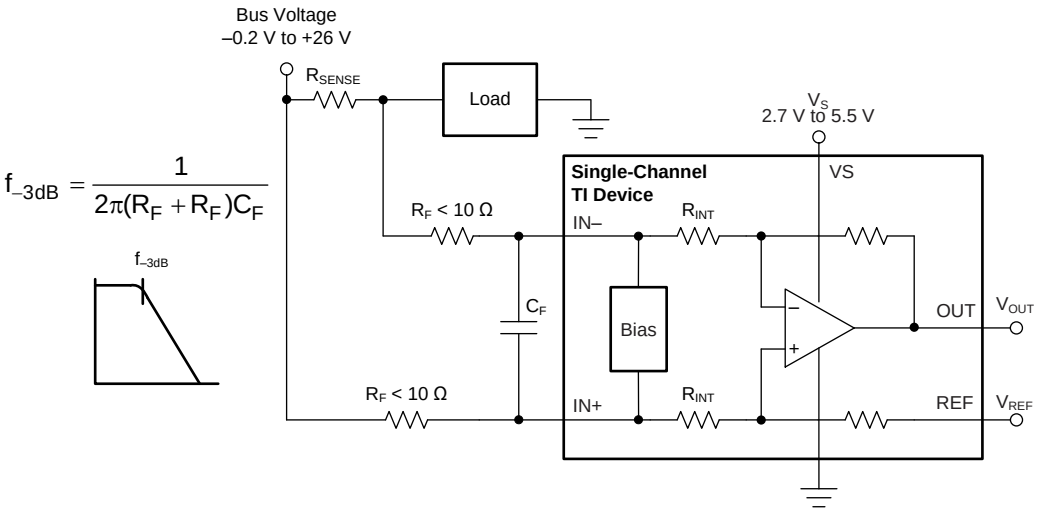


图 48. Filter at Input Pins

The addition of external series resistance creates an additional error in the measurement; therefore, the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in 图 48 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using 公式 6, where the gain error factor is calculated using 公式 5.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance (R_F) value as well as internal input resistor R_{INT}, as shown in 图 48. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. Calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given using 公式 5:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{(1250 \times R_F) + (1250 \times R_{INT}) + (R_F \times R_{INT})} \quad (5)$$

where:

- R_{INT} is the internal input resistor.
- R_F is the external series resistance.

Application Information (接下页)

With the adjustment factor from 公式 5, including the device internal input resistance, this factor varies with each gain version, as shown in 表 1. Each individual device gain error factor is shown in 表 2.

表 1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INAx181A1	20	25
INAx181A2	50	10
INAx181A3	100	5
INAx181A4	200	2.5

表 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INAx181A1	$\frac{25000}{(21 \times R_F) + 25000}$
INAx181A2	$\frac{10000}{(9 \times R_F) + 10000}$
INAx181A3	$\frac{1000}{R_F + 1000}$
INAx181A4	$\frac{2500}{(3 \times R_F) + 2500}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on 公式 6:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (6)$$

For example, using an INA181A2 and the corresponding gain error equation from 表 2, a series resistance of 10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using 公式 6, resulting in an additional gain error of approximately 0.89% solely because of the external 10-Ω series resistors.

9.1.4 Summing Multiple Currents

The outputs of the INA2181 are easily summed by connecting the output of one channel to the reference input of a second channel. The circuit configuration shown in 图 49 is an easy way to achieve current summing. To correctly sum multiple output currents the values for the current sense resistor R_{SENSE} must be the same for all channels.

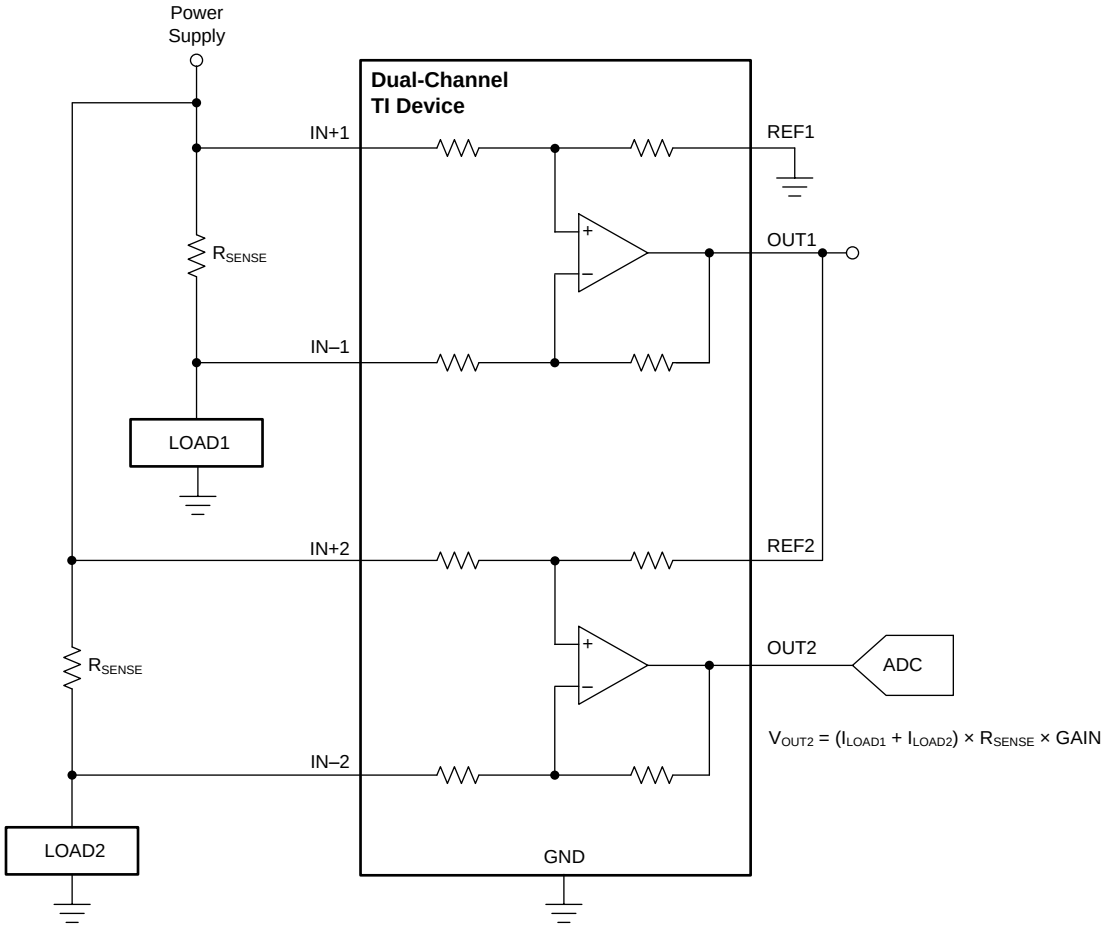
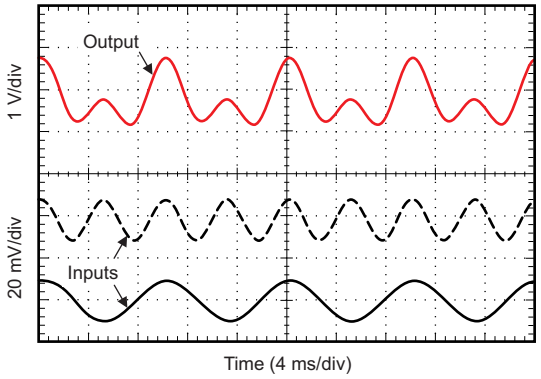


图 49. Summing Multiple Currents

Connect the output of one channel of the INA2181 to the reference input of the other channel. Use the reference input of the first circuit to set the reference of the final summed output operating point. The currents sensed at each circuit in the chain are summed at the output of the last device in the chain.

An example output response of a summing configuration is shown in 图 50. The reference pin of the first circuit is connected to ground, and sine waves at different frequencies are applied to the two circuits to produce a summed output as shown. The sine wave voltage input for the first circuit is offset so that the whole wave is above GND.



V_{REF} = 0 V

图 50. Current Summing Application Output Response (A2 Devices)

9.1.5 Detecting Leakage Currents

Occasionally, the need arises to confirm that the current going into a load is identical to the current coming out of a load; usually, as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing, except that the two amplifiers have the inputs connected opposite of each other. To correctly detect leakage currents, the values for the current sense resistor R_{SENSE} must be the same for all channels. Also an external reference voltage must be provided to the REF1 input to allow bidirectional leakage current detection.

If the current into a load is equal to the current out of the load, then the voltage at OUT2 is the same as the applied voltage to REF1. To enable accurate differences between the two currents, a reference voltage must be applied. The reference voltage prevents the output of the device from being driven to ground, and also enables detection if the current into the load is either greater than or less than the current coming out of the load.

For current differencing, the dual-channel INA2181 must have the inputs connected opposite to each other, as shown in 图 51. The reference input of the first channel sets the output quiescent level for all the devices in the string. Connect the output of the first channel to the reference input of the second channel. The reference input of the first channel sets the reference at the output. This circuit example is identical to the current summing example, except that the two shunt inputs are reversed in polarity. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. This current differencing circuit is useful in detecting when current in to and out of a load do not match.

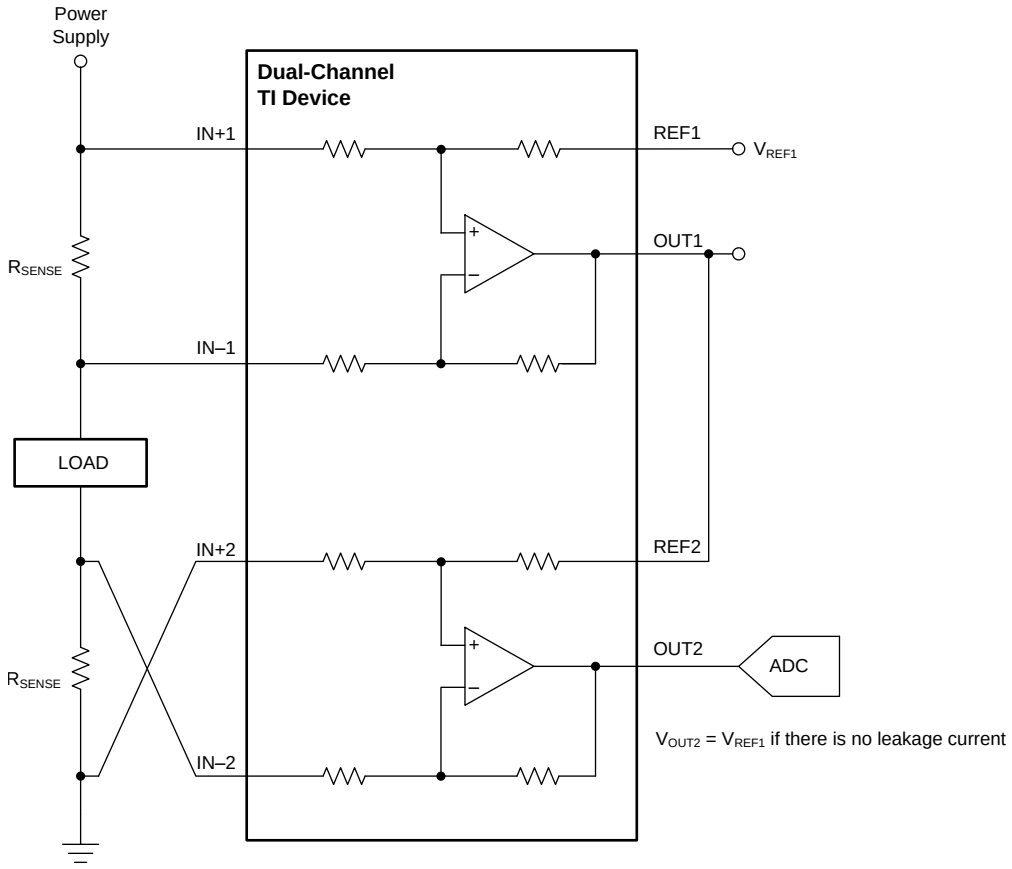
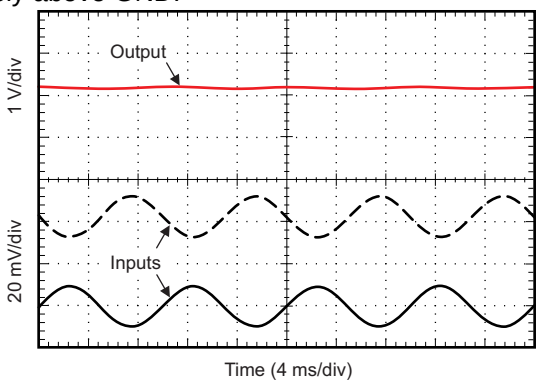


图 51. Detecting Leakage Currents

An example output response of a difference configuration is shown in 图 52. The reference pin of the first channel is connected to a reference voltage of 2.048 V. The inputs to each circuit is a 100-Hz sine wave, 180° out-of-phase with each other, resulting in a zero output as shown. The sine wave input to the first circuit is offset so that the input wave is completely above GND.



V_{REF} = 2.048 V

图 52. Current Differencing Application Output Response (A2 Devices)

9.2 Typical Application

One application for the INAx181 is to monitor bidirectional currents. Bidirectional currents are present in systems that have to monitor currents in both directions; common examples are monitoring the charging and discharging of batteries and bidirectional current monitoring in motor control. The device configuration for bidirectional current monitoring is shown in 图 53. Applying stable REF pin voltage closer to the middle of device supply voltage allows both positive- and negative-current monitoring, as shown in this configuration. Configure the INAx181 to monitor unidirectional currents by grounding the REF pin.

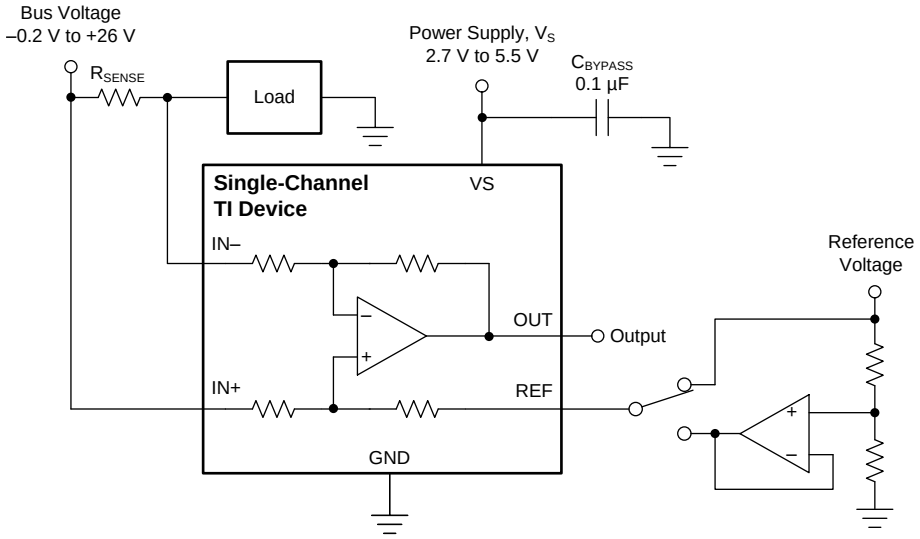


图 53. Measuring Bidirectional Current

9.2.1 Design Requirements

The design requirements for the circuit shown in 图 53, are listed in 表 3

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage, V_S	5 V
Bus supply rail, V_{CM}	12 V
R_{SENSE} power loss	< 450 mW
Maximum sense current, I_{MAX}	±20 A
Current sensing error	Less than 3.5% at maximum current, T_J = 25°C
Small-signal bandwidth	> 100 kHz

9.2.2 Detailed Design Procedure

The maximum value of the current sense resistor is calculated based on the maximum power loss requirement. By applying 公式 2, the maximum value of the current-sense resistor is calculated to be 1.125 mΩ. This is the maximum value for sense resistor R_{SENSE}; therefore, select R_{SENSE} to be 1 mΩ because it is the closest standard resistor value that meets the power-loss requirement.

The next step is to select the appropriate gain and reduce R_{SENSE}, if needed, to keep the output signal swing within the V_S range. The design requirements call for bidirectional current monitoring; therefore, a voltage between 0 and V_S must be applied to the REF pin. The bidirectional currents monitored are symmetric around 0 (that is, ±20 A); therefore, the ideal voltage to apply to V_{REF} is V_S / 2 or 2.5 V. If the positive current is greater than the negative current, using a lower voltage on V_{REF} has the benefit of maximizing the output swing for the given range of expected currents. Using 公式 3, and given that I_{MAX} = 20 A , R_{SENSE} = 1 mΩ, and V_{REF} = 2.5 V,

the maximum current-sense gain calculated to avoid the positive swing-to-rail limitations on the output is 122.5. Likewise, using 公式 4 for the negative-swing limitation results in a maximum gain of 124.75. Selecting the gain-of-100 device maximizes the output range while staying within the output swing range. If the maximum calculated gains are slightly less than 100, the value of the current-sense resistor can be reduced to keep the output from hitting the output-swing limitations.

To calculate the accuracy at peak current, the two factors that must be determined are the gain error and the offset error. The gain error of the INAx181 is specified to be a maximum of 1%. The error due to the offset is constant, and is specified to be 500 µV (maximum) for the conditions where V_{CM} = 12 V and V_S = 5 V. Using 公式 7, the percentage error contribution of the offset voltage is calculated to be 2.5%, with total offset error = 500 µV, R_{SENSE} = 1 mΩ, and I_{SENSE} = 20 A.

$$\text{Total Offset Error (\%)} = \frac{\text{Total Offset Error (V)}}{I_{SENSE} \times R_{SENSE}} \times 100\% \tag{7}$$

One method of calculating the total error is to add the gain error to the percentage contribution of the offset error. However, in this case, the gain error and the offset error do not have an influence or correlation to each other. A more statistically accurate method of calculating the total error is to use the RSS sum of the errors, as shown in 公式 8:

$$\text{Total Error (\%)} = \sqrt{\text{Total Gain Error (\%)}^2 + \text{Total Offset Error (\%)}^2} \tag{8}$$

After applying 公式 8, the total current sense error at maximum current is calculated to be 2.7%, and that is less than the design example requirement of 3.5%.

The INA181A3 (gain = 100) also has a bandwidth of 150 kHz that meets the small-signal bandwidth requirement of 100 kHz. If higher bandwidth is required, lower-gain devices can be used at the expense of either reduced output voltage range or an increased value of R_{SENSE}.

9.2.3 Application Curve

An example output response of a bidirectional configuration is shown in 图 54. With the REF pin connected to a reference voltage (2.5 V in this case), the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals, and falls below the reference voltage for negative differential input signals.

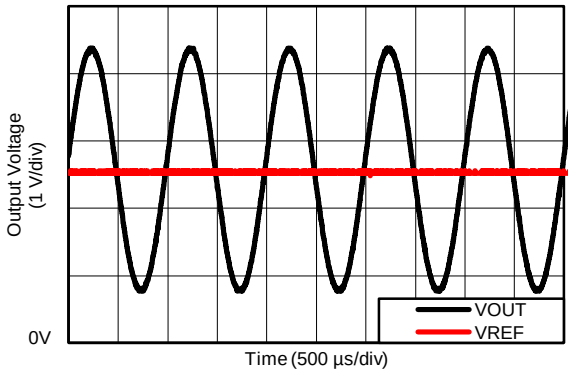


图 54. Bidirectional Application Output Response

10 Power Supply Recommendations

The input circuitry of the INAx181 accurately measures beyond the power-supply voltage, V_S. For example, V_S can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the VS pin. The INAx181 also withstand the full differential input signal range up to 26 V at the IN+ and IN– input pins, regardless of whether or not the device has power applied at the VS pin.

10.1 Common-Mode Transients Greater Than 26 V

With a small amount of additional circuitry, the INAx181 can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode; see 图 55. Keep these resistors as small as possible; most often, around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Signal Filtering* section. This circuit limits only short-term transients; therefore, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

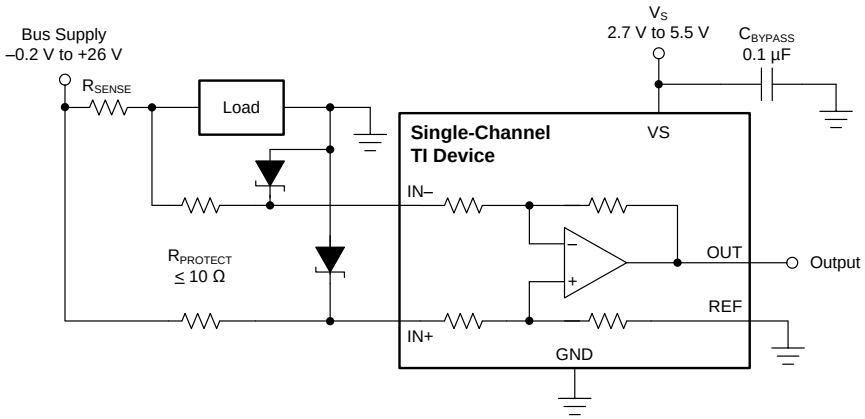


图 55. Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in 图 56. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in 图 55 and 图 56, the total board area required by the INAx181 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

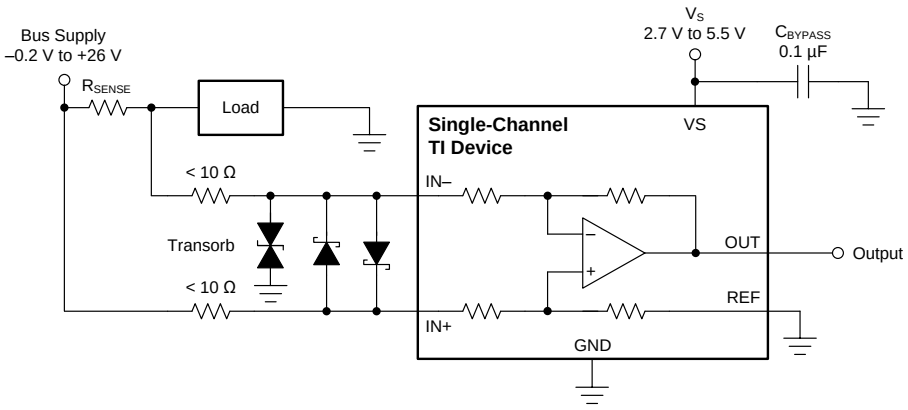


图 56. Transient Protection Using a Single Transzorb and Input Clamps

Common-Mode Transients Greater Than 26 V (接下页)

For more information, see *Current Shunt Monitor With Transient Robustness Reference Design*.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current sense resistor to the device, keep the trace lengths as close as possible in order to minimize any impedance mismatch..

11.2 Layout Example

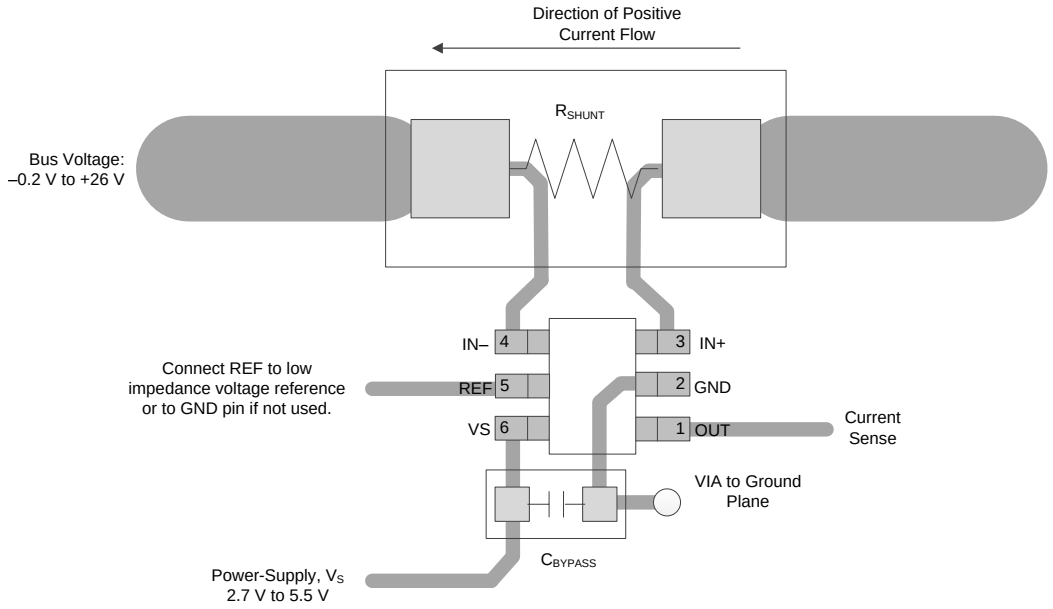


图 57. Single-Channel Recommended Layout

Layout Example (接下页)

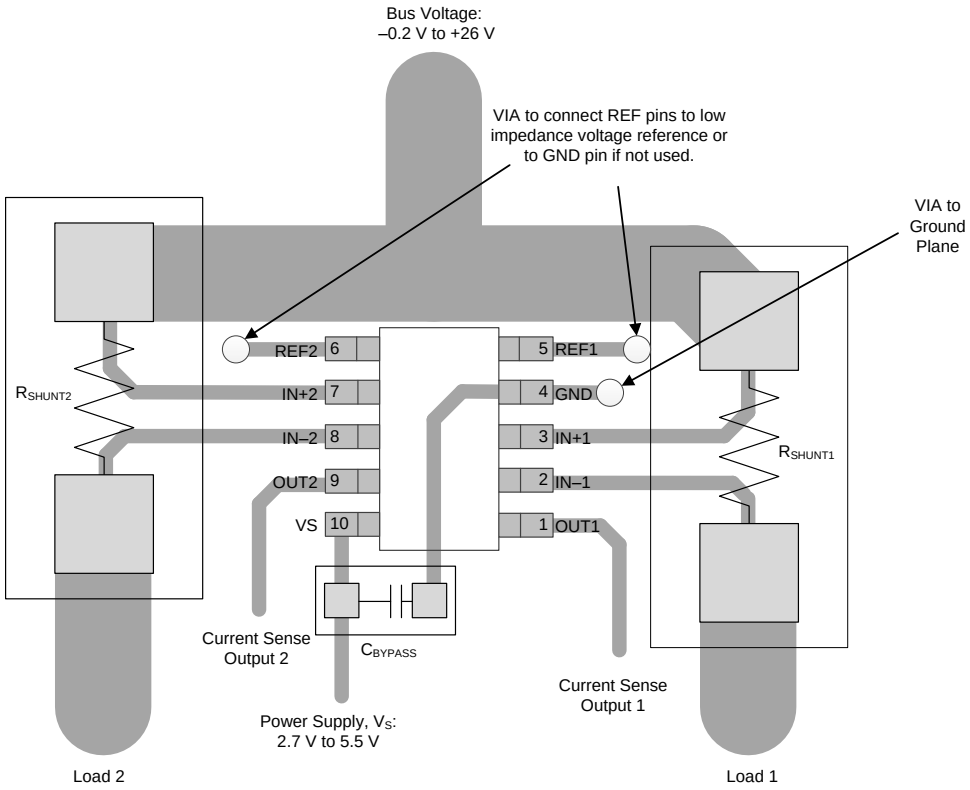


图 58. Dual-Channel Recommended Layout

Layout Example (接下页)

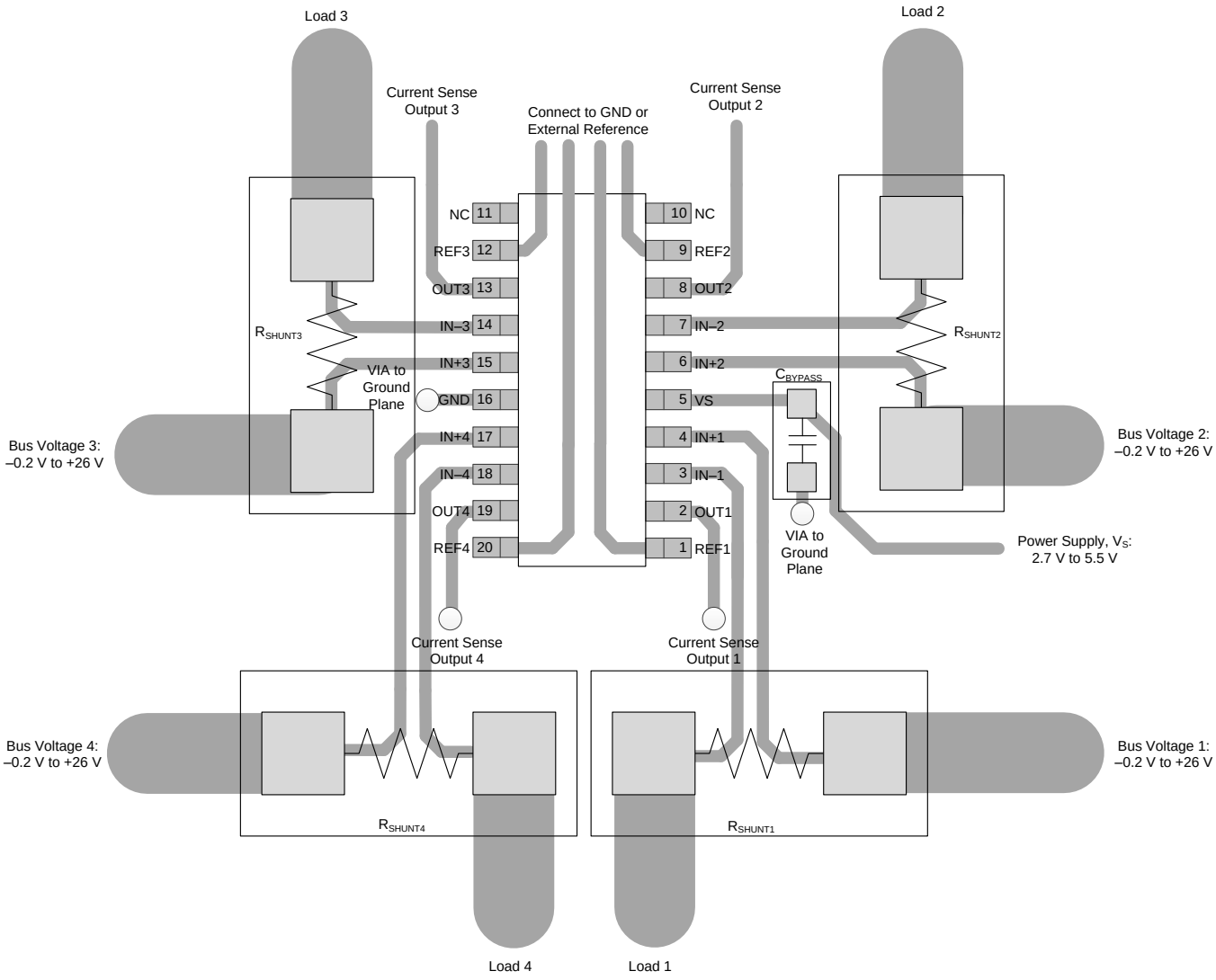


图 59. Quad-Channel Recommended Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

《具有瞬态稳定性的电流分流监控器参考设计》

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《INA180-181EVM 用户指南》*
- 德州仪器 (TI)，*《INA2180-2181EVM 用户指南》*
- 德州仪器 (TI)，*《INA4180-4181EVM 用户指南》*

12.3 相关链接

表 4 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具与软件，以及立即订购快速访问。

表 4. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
INA181	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
INA2181	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
INA4181	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA181A1IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	18JD	Samples
INA181A1IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	18JD	Samples
INA181A2IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AED	Samples
INA181A2IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AED	Samples
INA181A3IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AFD	Samples
INA181A3IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AFD	Samples
INA181A4IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AGD	Samples
INA181A4IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1AGD	Samples
INA2181A1IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CW6	Samples
INA2181A1IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1CW6	Samples
INA2181A1IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25IY	Samples
INA2181A1IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25IY	Samples
INA2181A2IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1DR6	Samples
INA2181A2IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1DR6	Samples
INA2181A2IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25JY	Samples
INA2181A2IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25JY	Samples
INA2181A3IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1DS6	Samples
INA2181A3IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1DS6	Samples
INA2181A3IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25KY	Samples
INA2181A3IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25KY	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA2181A4IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DT6	Samples
INA2181A4IDGST	ACTIVE	VSSOP	DGS	10	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1DT6	Samples
INA2181A4IDSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25LY	Samples
INA2181A4IDSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	25LY	Samples
INA4181A1IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A1	Samples
INA4181A2IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A2	Samples
INA4181A3IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A3	Samples
INA4181A4IPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4181A4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA181, INA2181, INA4181 :

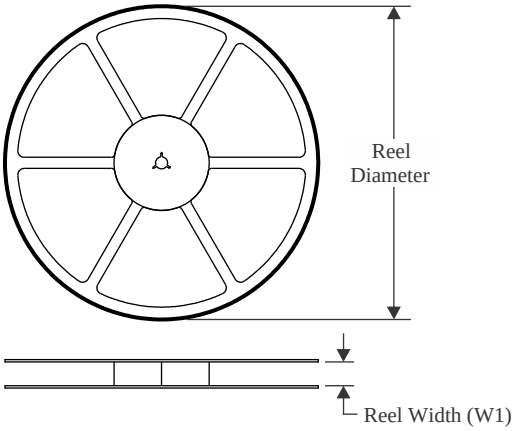
- Automotive : INA181-Q1, INA2181-Q1, INA4181-Q1

NOTE: Qualified Version Definitions:

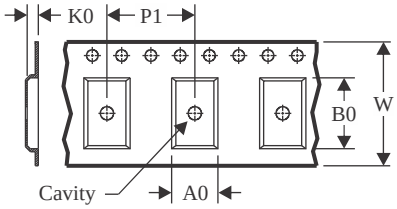
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

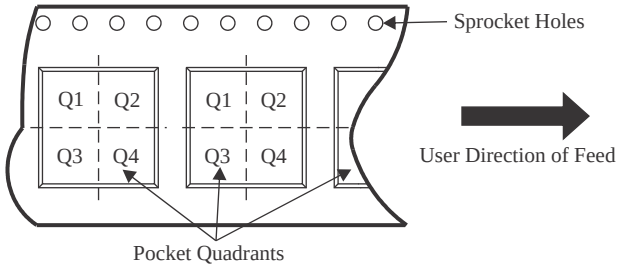


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

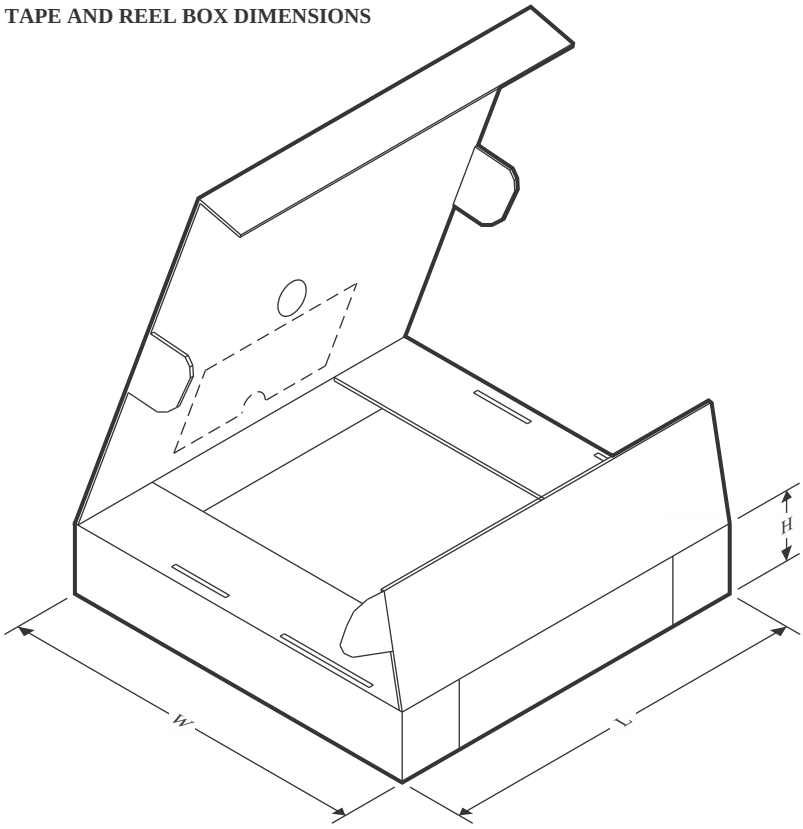


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA181A1IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A1IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A2IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A2IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A3IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A3IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A4IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA181A4IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
INA2181A1IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A1IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A1IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A1IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A2IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A2IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A2IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A2IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2181A3IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A3IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A3IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A3IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A3IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A3IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A4IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A4IDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2181A4IDSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA2181A4IDSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
INA4181A1IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A2IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A3IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
INA4181A4IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA181A1IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A1IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA181A2IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A2IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA181A3IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A3IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA181A4IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
INA181A4IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
INA2181A1IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A1IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A1IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A1IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA2181A2IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A2IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A2IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A2IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA2181A3IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A3IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0

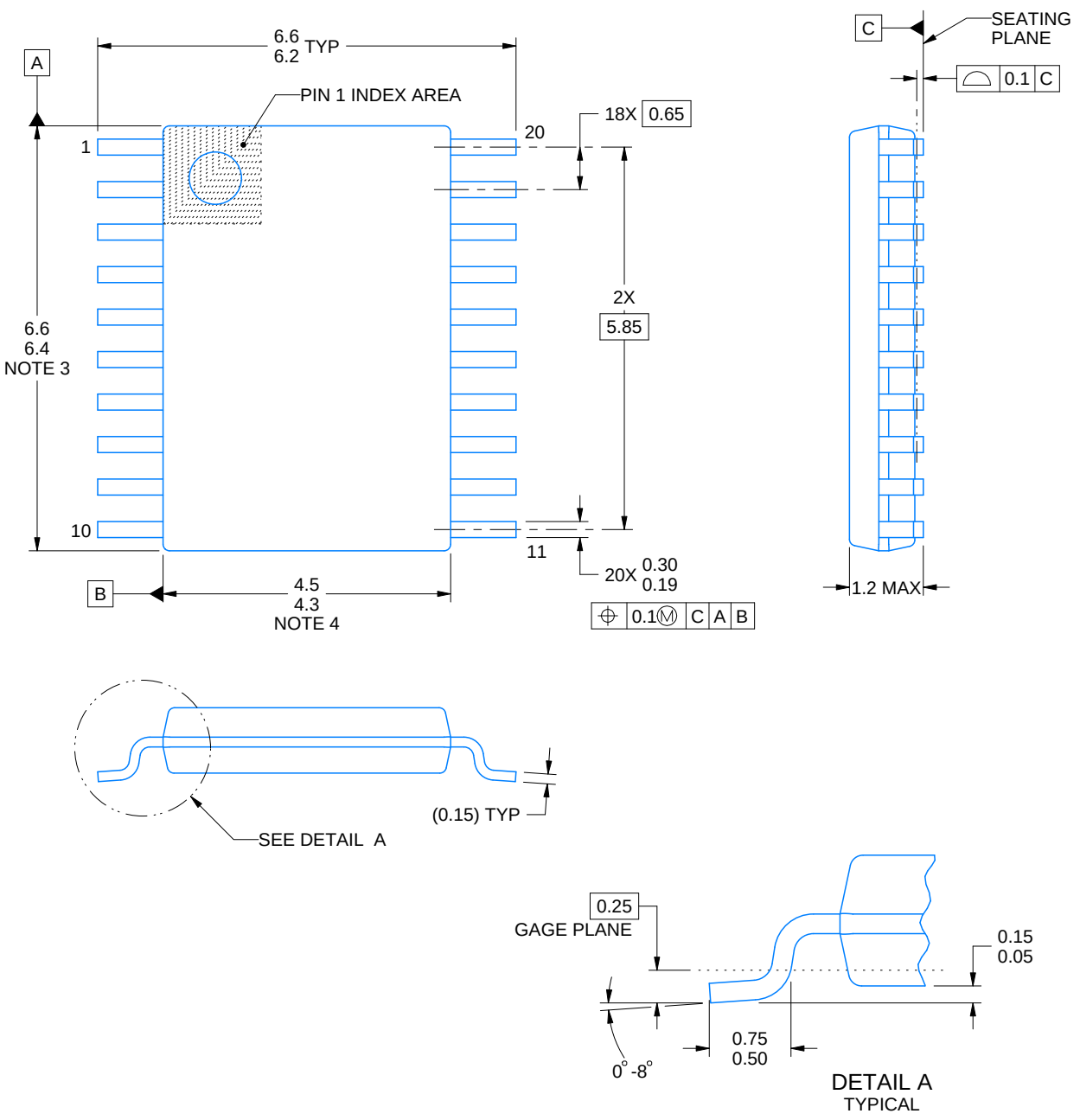
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2181A3IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A3IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A3IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A3IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA2181A4IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
INA2181A4IDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
INA2181A4IDSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
INA2181A4IDSQT	WSON	DSQ	10	250	210.0	185.0	35.0
INA4181A1IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
INA4181A2IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
INA4181A3IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
INA4181A4IPWR	TSSOP	PW	20	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0020A

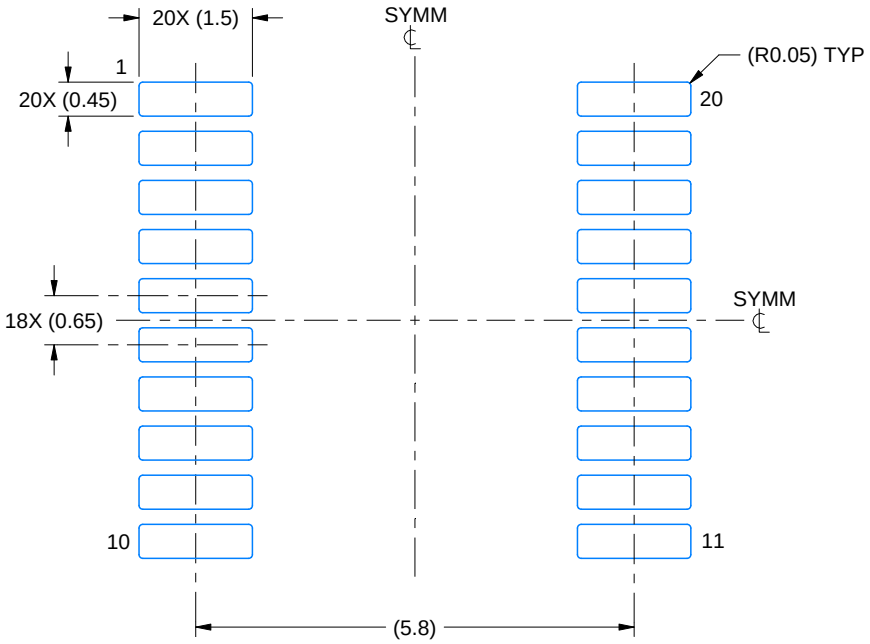
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



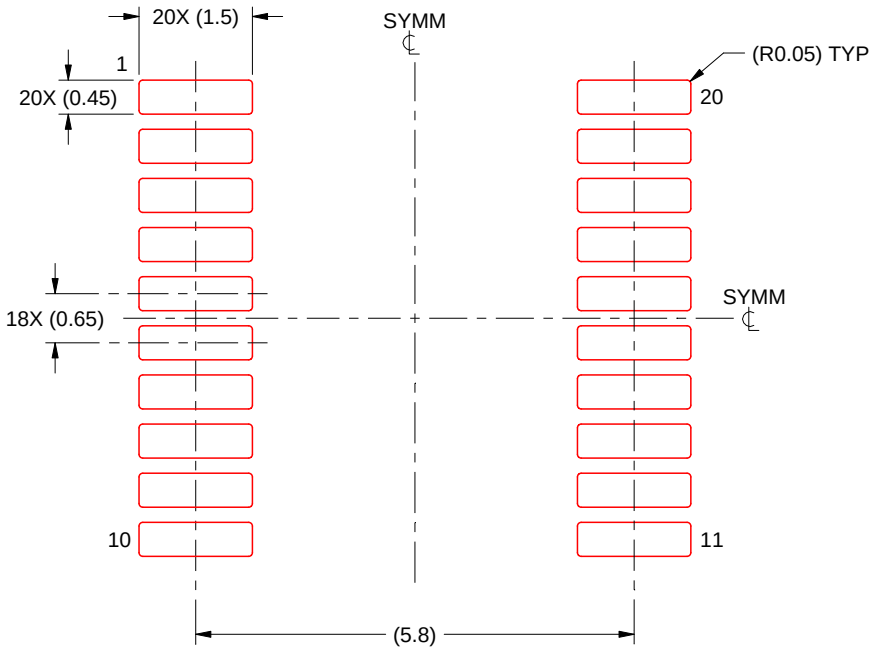
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



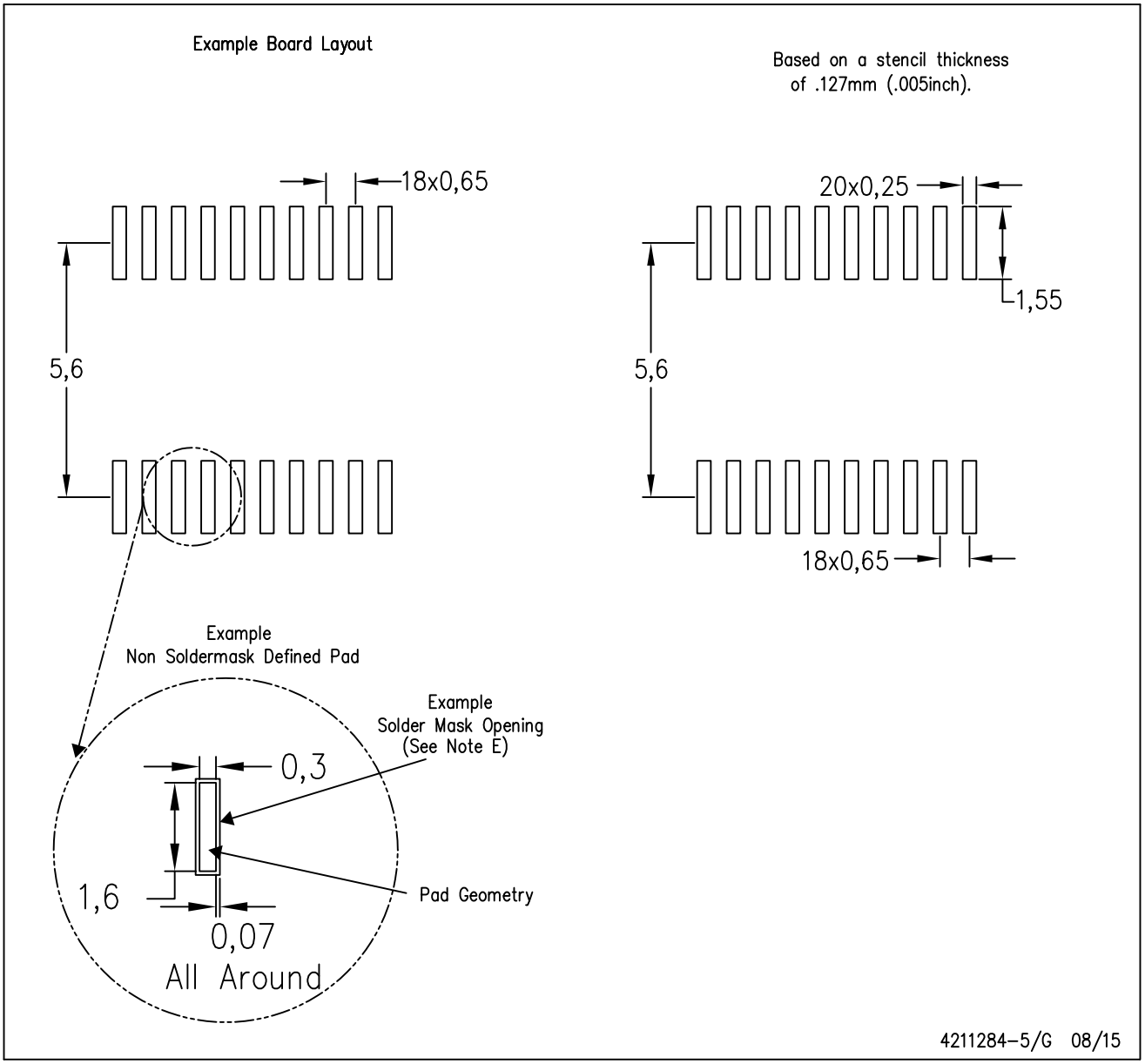
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



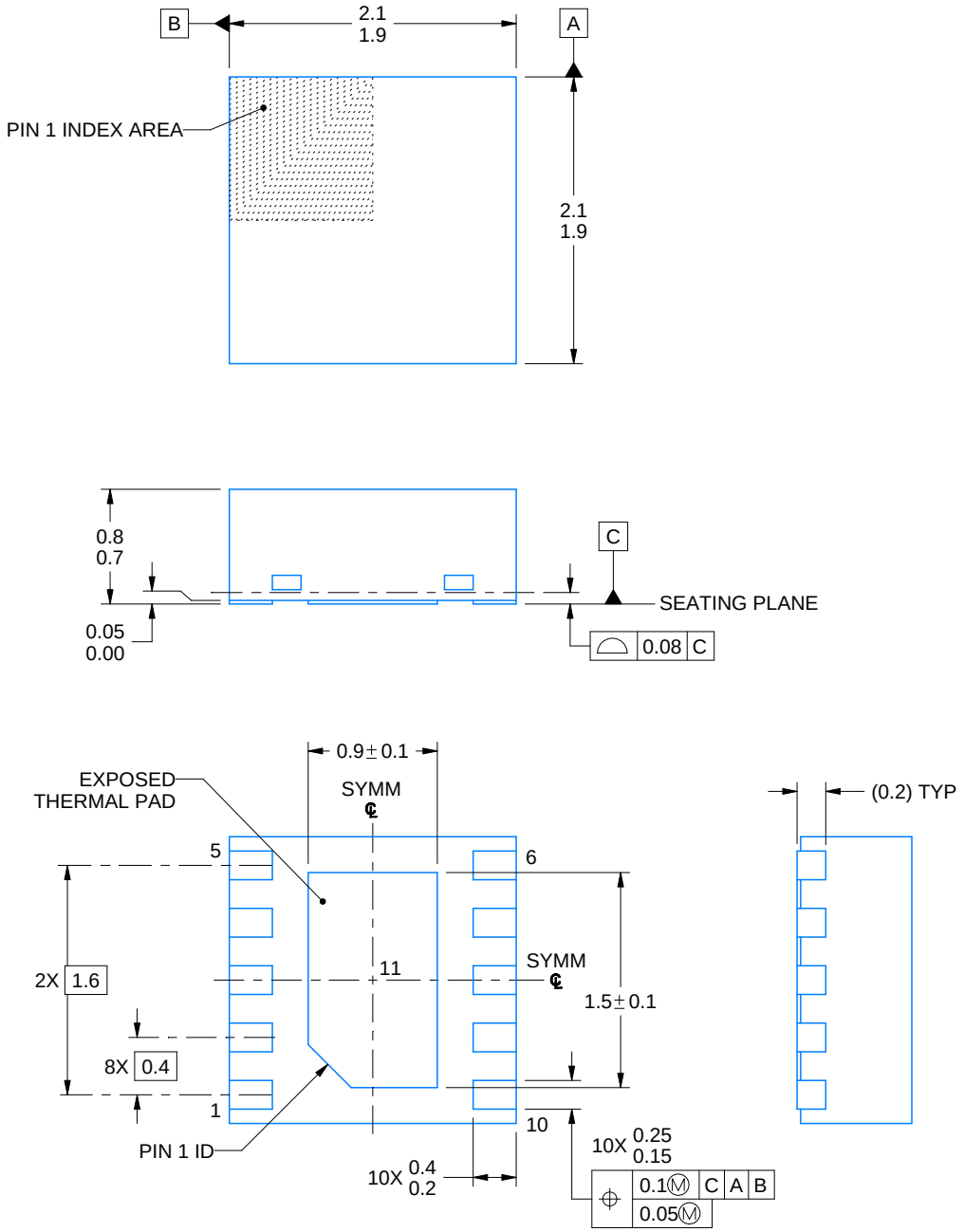
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218906/A 04/2019

NOTES:

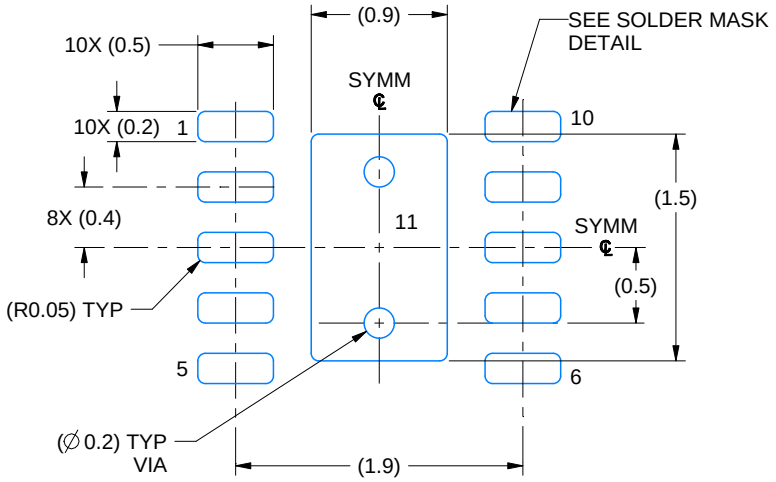
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

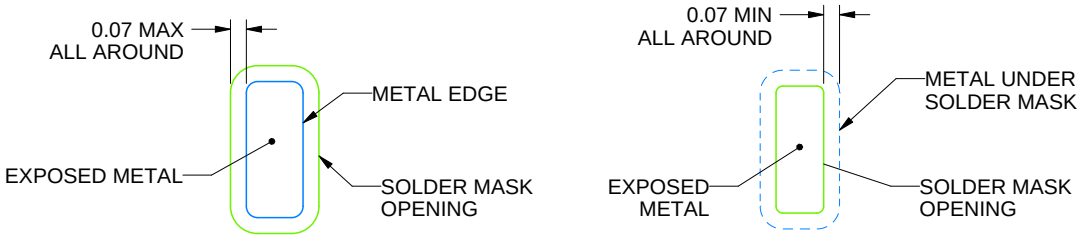
DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

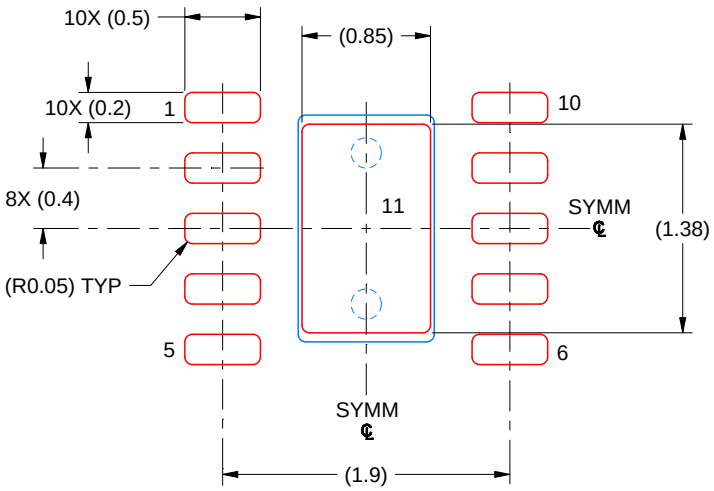
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218906/A 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 11
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218906/A 04/2019

NOTES: (continued)

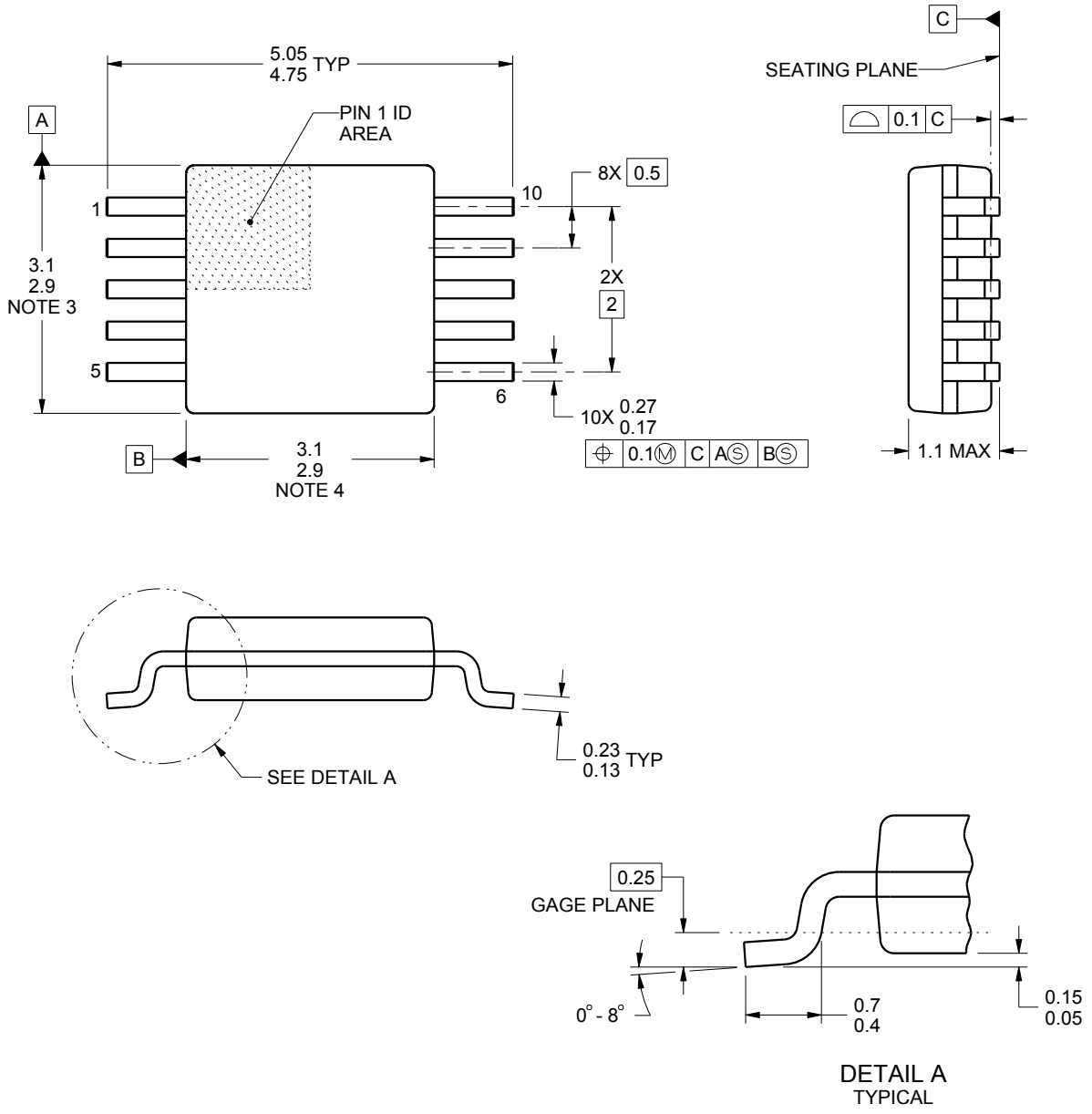
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGS0010A

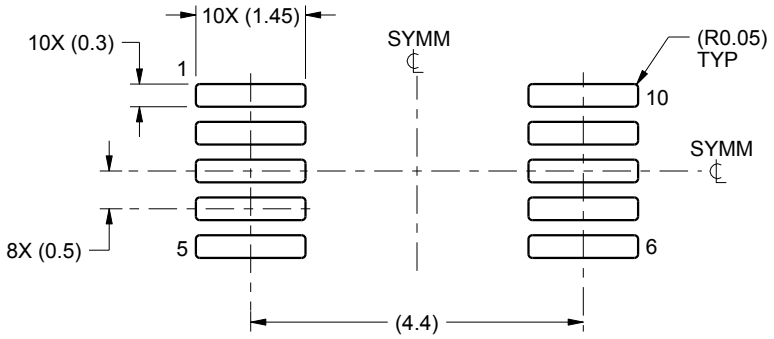
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

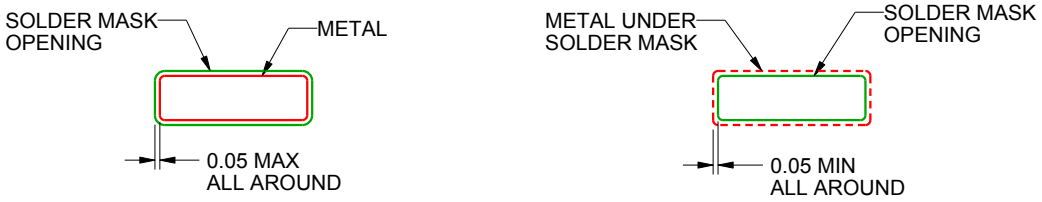


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

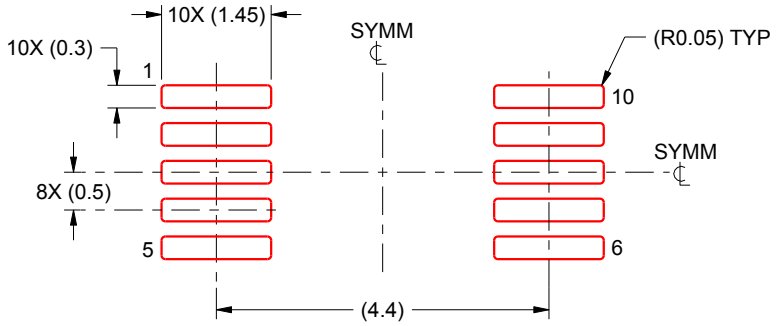


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

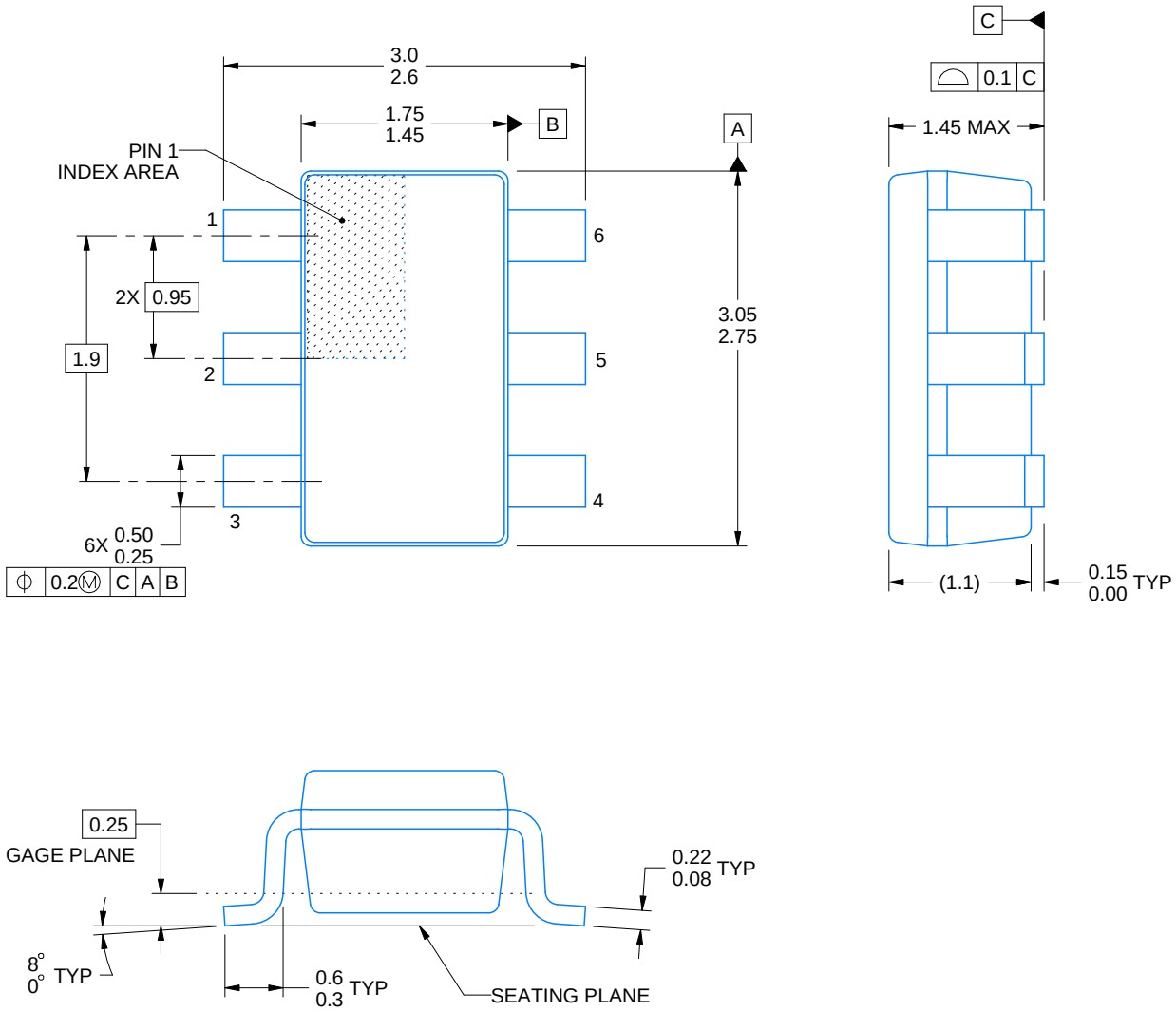
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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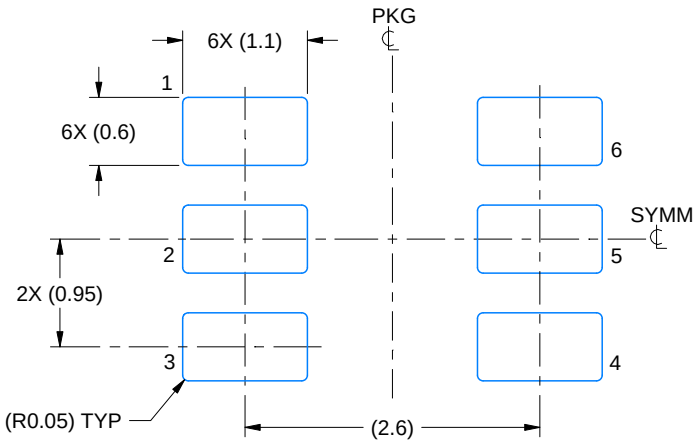
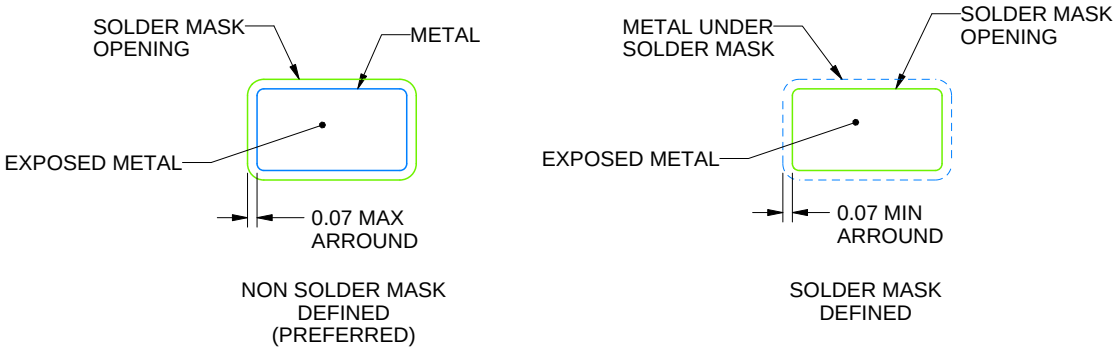
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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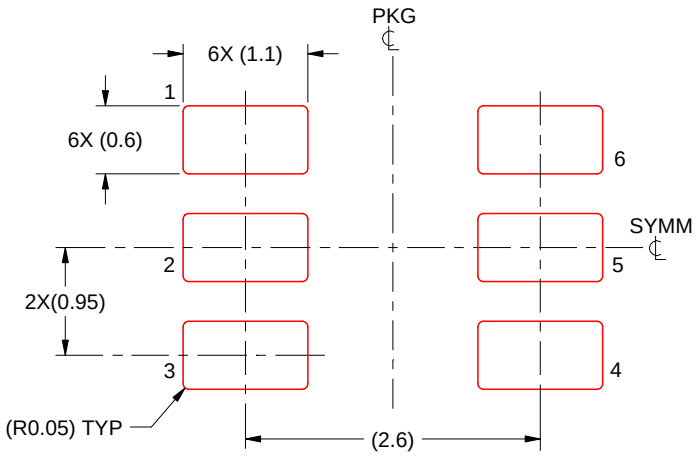
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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