HW 8, Newton-Rapshon method

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We will now use Newton-Rapshon method to find ϕ approximately with the Poisson equation.

$$\frac{d}{dx}\left(\epsilon\frac{d}{dx}\,\phi(x)\right) = \;qN_{acc} + qn_i\exp\left(\frac{q\phi_i}{kT}\right) - qn_i\exp\left(-\frac{q\phi_i}{kT}\right)$$

i-th entry of the residue vector :

$$r_i = \frac{\epsilon}{\Delta x}(\phi_{i+1} - 2\phi_i + \phi_{i-1}) - \Delta xqN_{acc} - \Delta xqn_i\exp\left(\frac{q\phi_i}{kT}\right) + \Delta xqn_i\exp\left(-\frac{q\phi_i}{kT}\right)$$

The Jacobian matrix is :

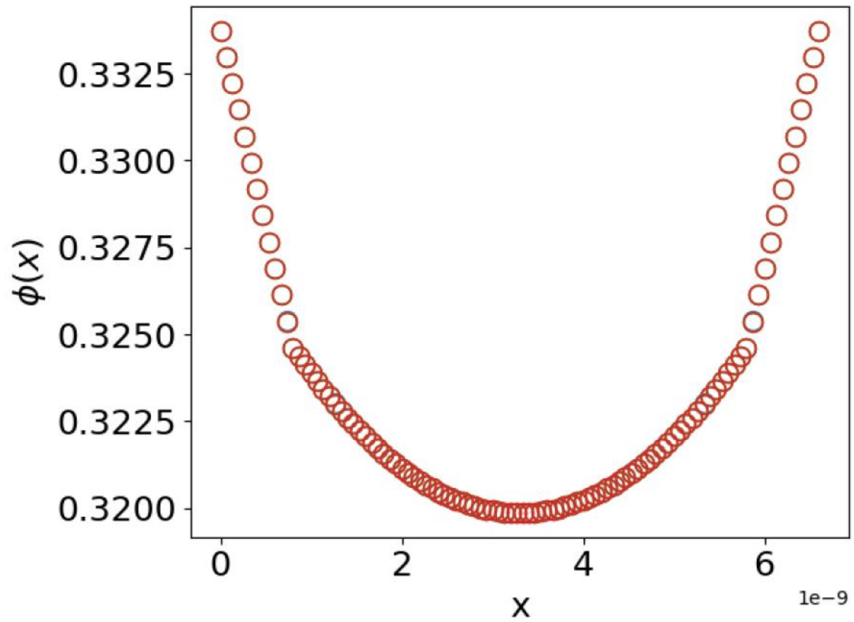
$$J_{i,i+1} = \frac{\epsilon_{si}}{\Delta \mathrm{x}},\qquad J_{i,i} = -\frac{2\epsilon_{si}}{\Delta x} - \frac{\Delta xqn_iq}{kT}\exp\left(\frac{q\phi_i}{kT}\right) - \frac{\Delta xqn_iq}{kT}\exp\left(-\frac{q\phi_i}{kT}\right),\qquad J_{i,i-1} = \frac{\epsilon_{si}}{\Delta x}$$

Now we can earn $\delta\phi$ to estimate ϕ.

$$J\delta\phi = -\mathrm{r}, \delta\phi = -J^{-1}r \;\rightarrow\; \phi^1 = \phi^0 + \delta\phi$$

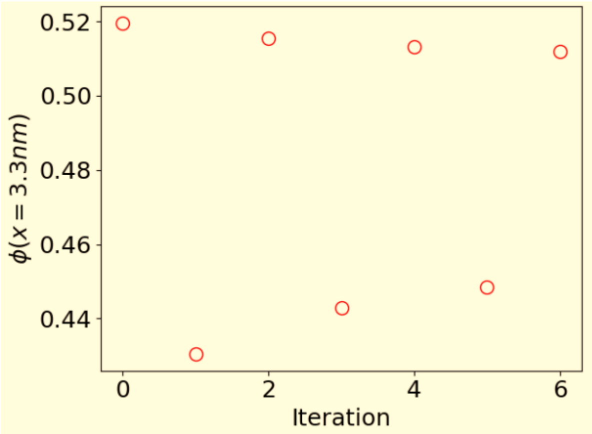
Here is the result of ϕ where the gate voltage is 0.

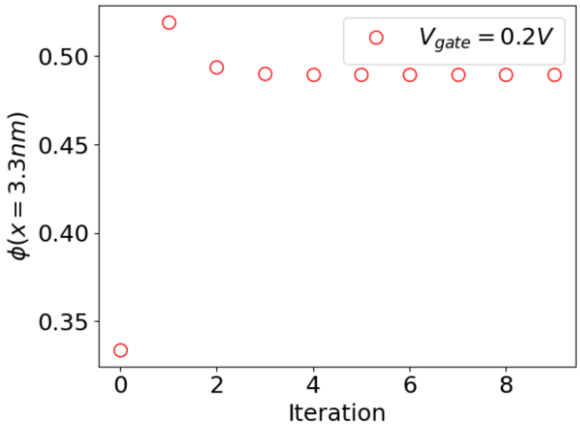
1.$\boldsymbol{\phi(x)}$ $\boldsymbol{for\ V_{gate} = 0}$



$\phi(x)$ looks same with previous results. However, we found that some gate voltage values makes weird behaviors of $\phi(x = 3.3nm)$ with depletion approximation. (hw 6)

2.$\boldsymbol{\phi(x = 3.3nm), V_{gate} = 0.2V}$

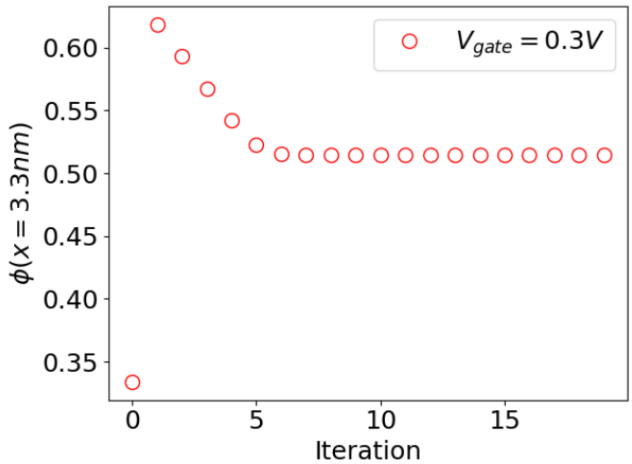




Left yellow figure shows $\phi(x = 3.3nm)$ with depletion approximation (hw6). It makes two converged values by the iteration number (odd or even).

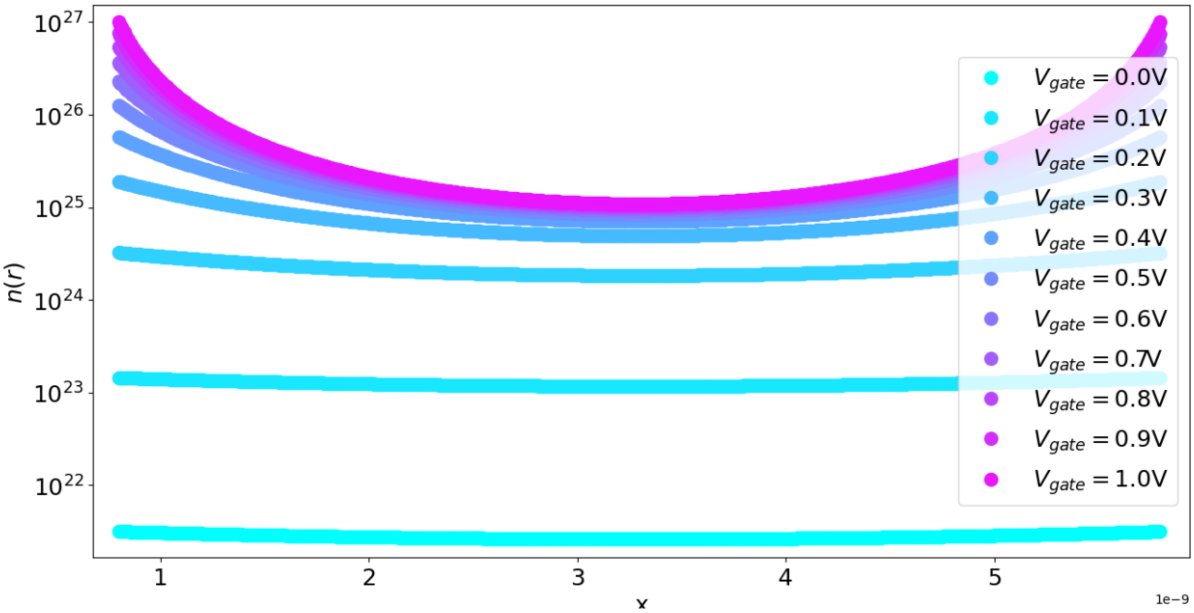
Right figure shows that Newton-Rapshon method does not show weird behavior.

3.$\boldsymbol{\phi(x = 3.3nm), V_{gate} = 0.3V}$



$\phi(x = 3.3nm)$ converged well with $V_{gate} = 0.3V$. $\phi(x = 3.3nm)$ diverged at $V_{gate} \geq 0.3V$ with depletion approximation (hw6).

4.$n(r), V_{gate} = 0.1V\ to\ 1V$



Self-consistent iterations are finished when $\left|\phi^{(n+1)}(x = 3.3nm) - \phi^{(n)}(x = 3.3nm)\right| < 10^{-5}$. The reason to choose $x = 3.3nm$ is that ϕ largely fluctuates by iterations. We find that high gate voltage makes high electric densities in the silicon layer.