Computational Microelectronics
Lecture 10 Some Selected Papers

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IEDM Papers

My personal view

- I don’t know the pre-history of TCAD.
  - My career as a graduate student starts in 2001.
- I have little idea about the process simulation.
- Some trendy topics are not included (or less emphasized):
  - 2D materials
  - “New” memory devices
  - Ferroelectric

Bonani, 1995

- A novel implementation of noise analysis in general-purpose PDE-based semiconductor device simulators

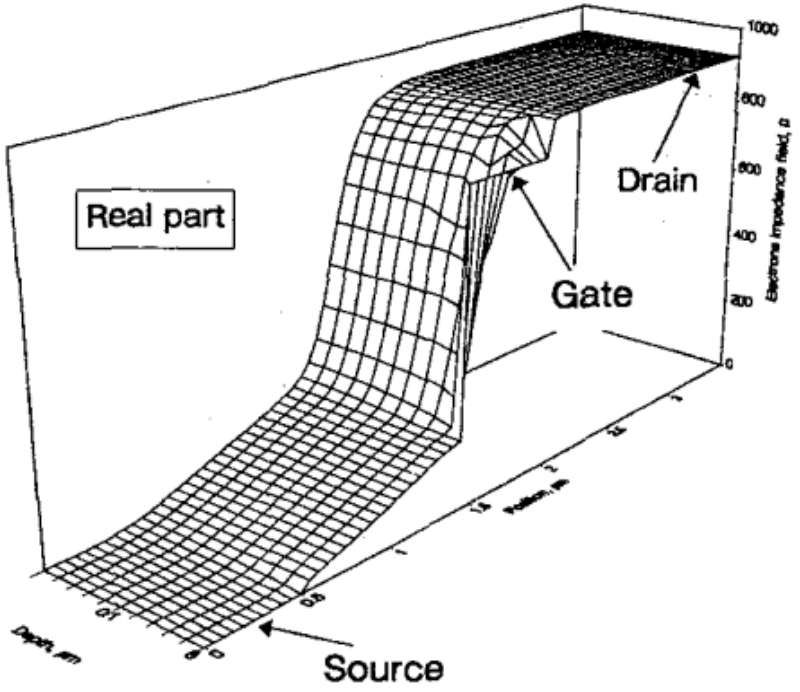


Figure 11: Real part of the drain electrons impedance field for the 2D Si MESFET. The bias point is in saturation, $f = 1$ GHz.

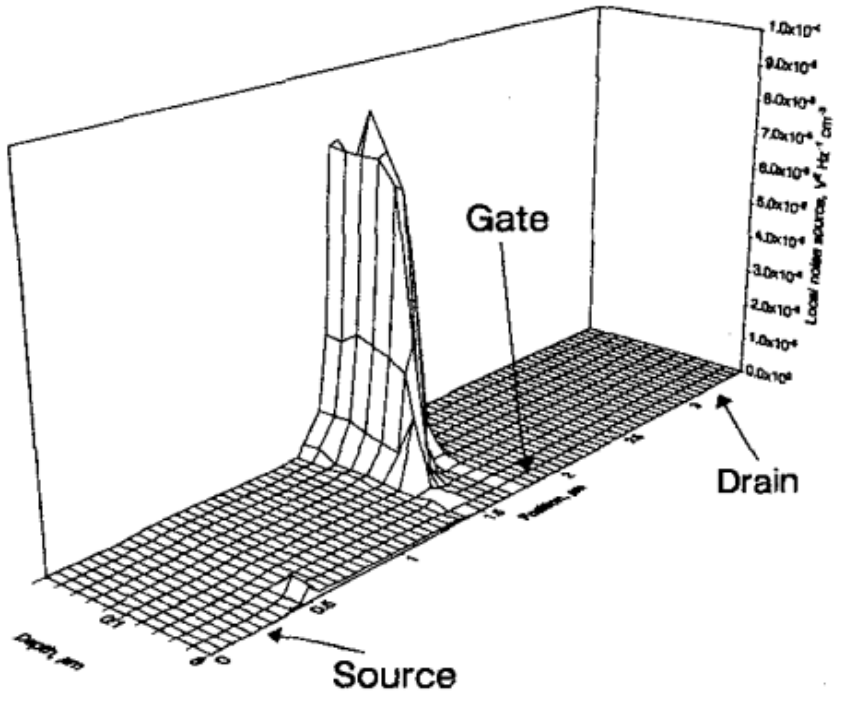


Figure 13: Distributed local noise source for the drain noise spectrum of the 2D Si MESFET. The bias point is in saturation, $f = 1$ GHz.

Asenov, 1999

- Quantum mechanical enhancement of the random dopant induced threshold voltage fluctuations and lowering in sub 0.1 micron MOSFETs

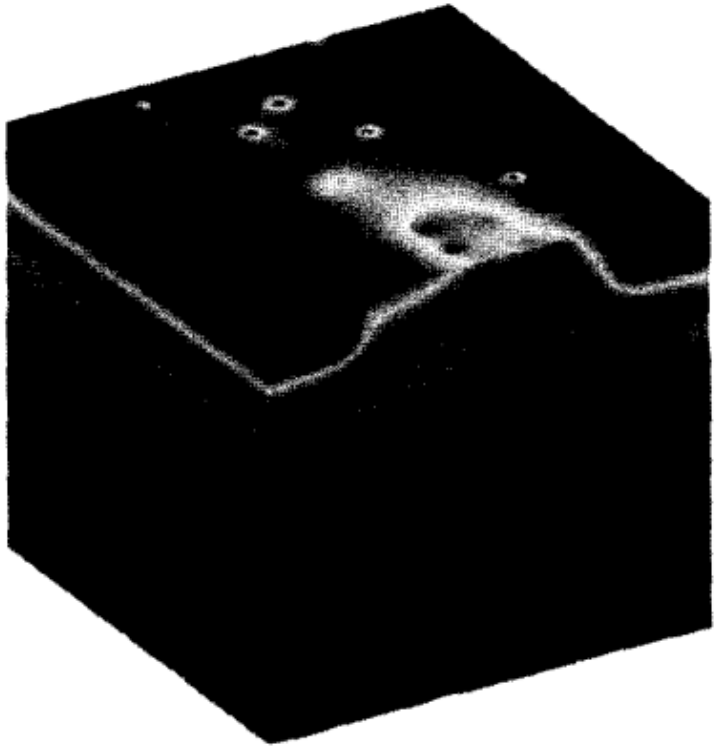


Fig. 2: Potential distribution at threshold voltage obtained from the 'atomistic' DG simulation of a 30×50 nm MOSFET with design parameters given in Fig. 1.

Jungemann, 2001

- Hierarchical 2D RF noise simulation of Si and SiGe devices by Langevin-type DD and HD models based on MC generated noise parameters

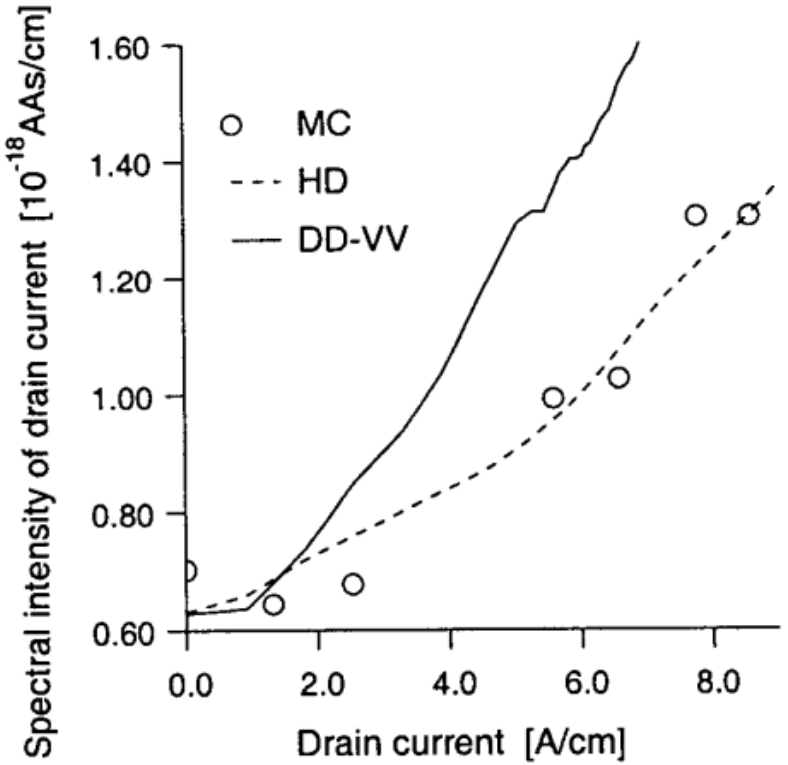


Fig. 4: Low-frequency spectral intensity of the drain current fluctuations $S_{I_D I_D}$ for a 40nm-NMOSFET by DD-VV, HD, and MC device simulation for room temperature in strong inversion

Luisier, 2010

- Phonon-limited mobility and injection velocity in n- and p-doped ultrascaled nanowire field-effect transistors with different crystal orientations

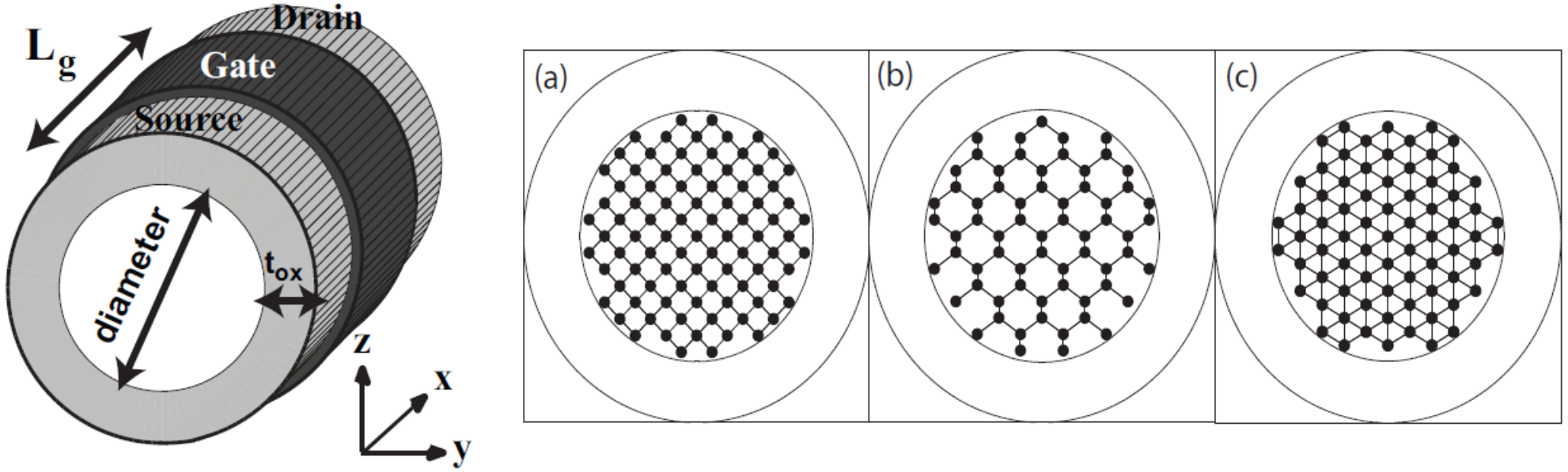
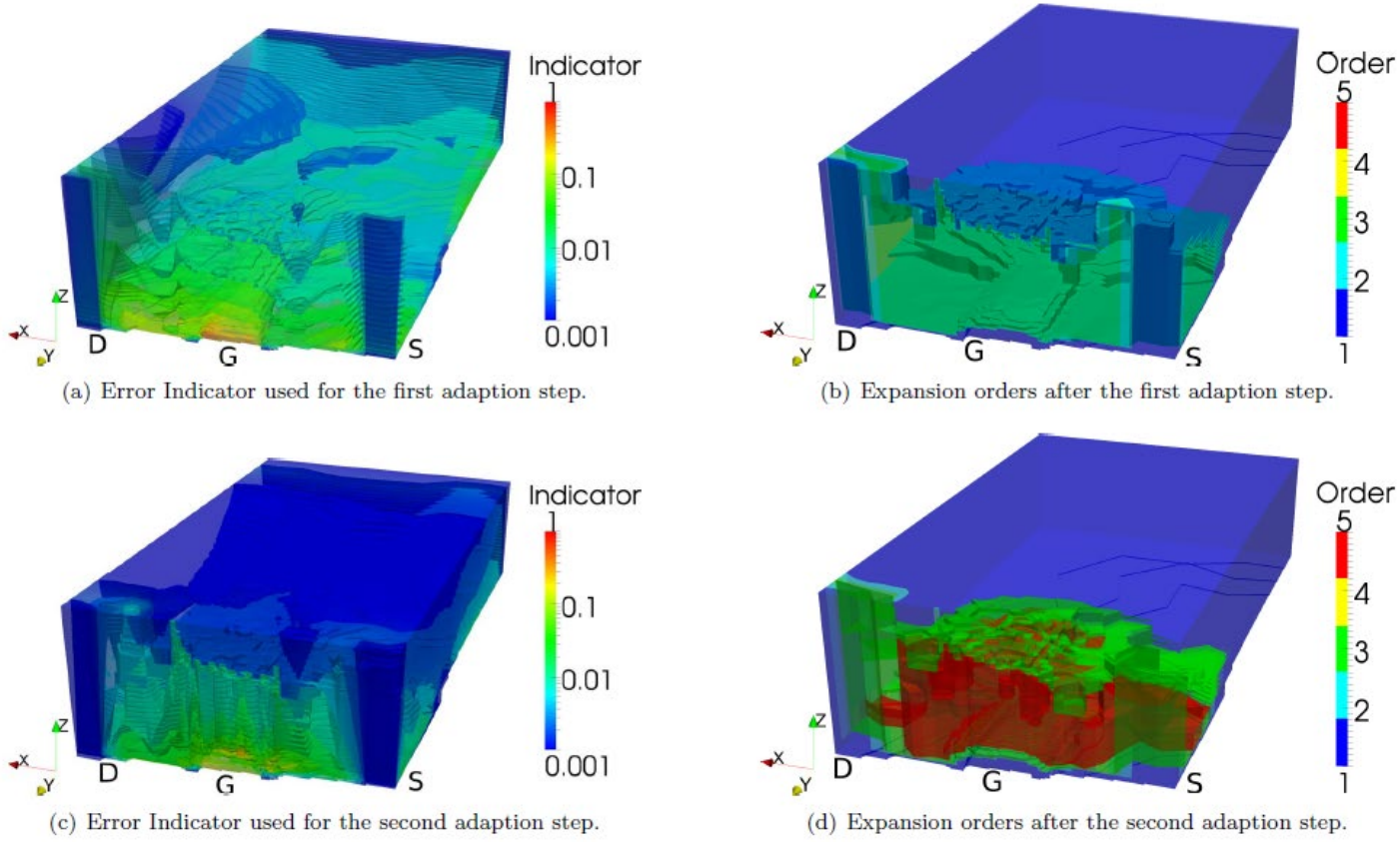


Fig. 1. Schematic view of the Si gate-all-around circular nanowire (NW) field-effect transistors (FETs) considered in this work. The diameter d is equal to 3nm, the source and drain extensions both measure 10nm, the gate length L_g is set to 15nm to calculate injection velocities and varies from 15nm to 30nm to determine the low-field mobility using the dR/dL method [13]. The equivalent oxide thickness (EOT) of all the transistors is 1nm. The transport direction x is aligned with the (a) [100], (b) [110], and (c) [111] crystal axis. The doping of the source and drain extensions amounts to N_D=1e20 cm^{-3} donors for the n-doped devices and N_A=1e20 cm^{-3} acceptors for the p-doped devices. The supply voltage V_{DD} is chosen to be 0.6 V. Note that the OFF-current of the different transistors is not aligned, but they all have the same dimensions and material parameters.

Rupp, 2011

- On the feasibility of spherical harmonics expansions of the Boltzmann transport equation for three-dimensional device geometries



(a) Error Indicator used for the first adaption step.

(b) Expansion orders after the first adaption step.

(c) Error Indicator used for the second adaption step.

(d) Expansion orders after the second adaption step.

Figure 2: Based on the error indicator the expansion orders are locally increased. The bulk is kept at a fixed first order, since the contribution to transport is negligible. The z-axis denotes total energy.

Jin, 2014

- Performance evaluation of InGaAs, Si, and Ge nFinFETs based on coupled 3D drift-diffusion/multisubband Boltzmann transport equations solver

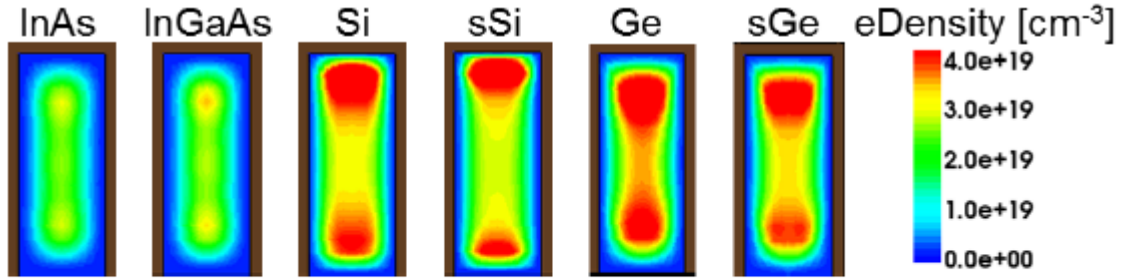


Fig. 2. Electron density profiles at the 2D cross-section of the channel center when $V_G = 0.6$ V and $V_D = 0$ V. The quantum confinement is more pronounced at the InAs and InGaAs channels due to small effective mass.

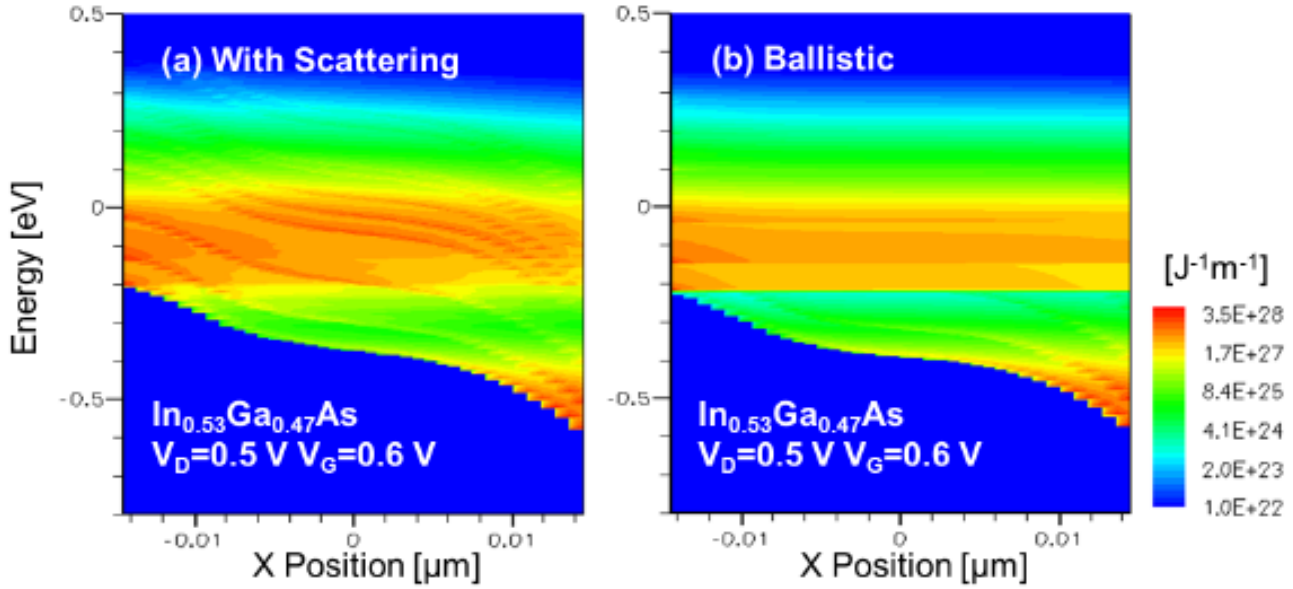


Fig. 6. Energy resolved electron density inside the $In_{0.53}Ga_{0.47}As$ channel (a) with and (b) without scattering. In the ballistic simulation, small amount of artificial inelastic phonon scattering needs to be added to avoid numerical instability.

Szabo, 2014

- Ab-initio simulations of MoS_2 transistors: from mobility calculation to device performance evaluation

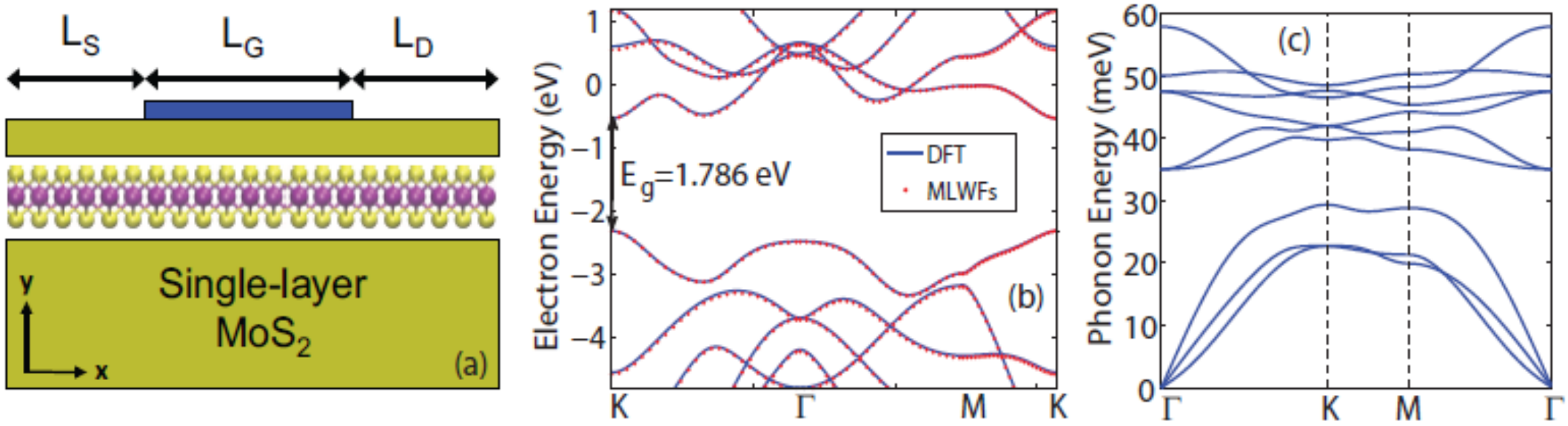


Fig. 1. (a) Schematic view of the n-type single-gate MoS_2 field-effect transistor (FET) considered in this work. The source and drain extensions measure L_s=L_d=15 nm each and are doped with a donor concentration N_D=6e13 cm^{-2}. The gate is L_g=10.7 nm long and is separated from the channel by a t_{ox}=3 nm thick HfO_2 layer with ϵ_R=20 (EOT=0.58 nm). The single-layer MoS_2 is deposited on a SiO_2 substrate. All the simulations are done at room temperature. (b) MoS_2 electron bandstructure calculated with VASP [7] and with the maximally-localized Wannier functions used in quantum transport. (c) MoS_2 phonon bandstructure calculated with VASP. The DFT phonon energies and modes are imported into our quantum transport solver to model electron-phonon scattering.

Chen, 2017

- NeuroSim+: An integrated device-to-algorithm framework for benchmarking synaptic devices and array architectures

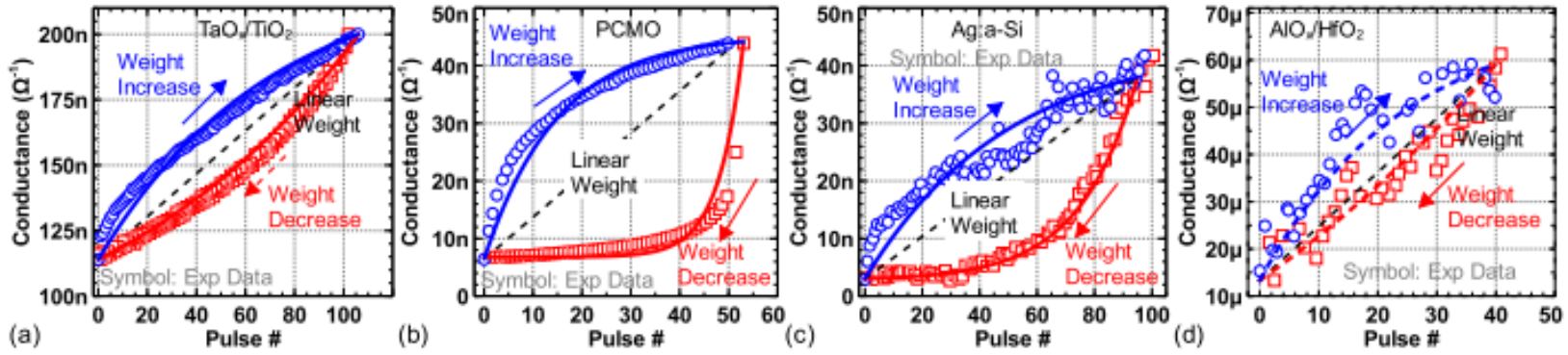


Fig. 1 Weight update curve of the reported (a) TaO_x/TiO_2 [10], (b) PCMO [11], (c) Ag:a-Si [12] and (d) AlO_x/HfO_2 [13] type analog eNVMs.

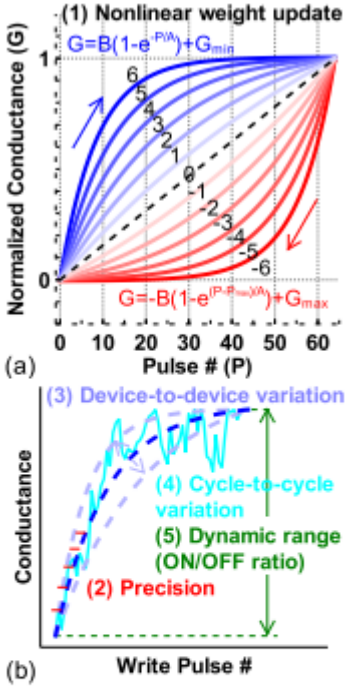


Fig. 2 Summary of non-ideal analog eNVM device properties modeled in this work. Exponential functions are used to model the nonlinear weight update behaviors, where the nonlinearity is labeled from -6 to 6. Device-to-device and cycle-to-cycle variations are the variation in the nonlinearity baseline and conductance change, respectively.

Shin, 2017

- First-principles based quantum transport simulations of nanoscale field effect transistors

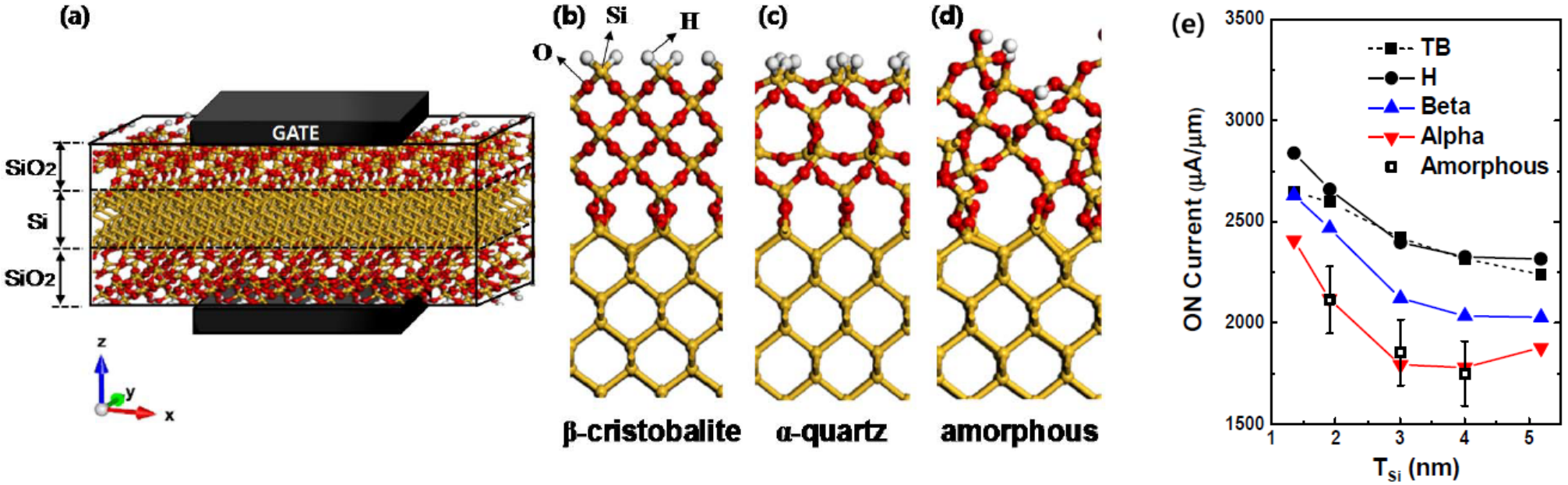


Figure 5. (a) Si UTB FETs with atomistically modeled SiO_2 dielectrics. (b)-(d) display the atomic models for β-cristobalite, α-quartz, and amorphous SiO_2, respectively. (e) The ON current levels by the SiO_2 model types are shown as a function of Si thickness T_{si}. The OFF current criteria was 0.1 μA/μm. Long channel length compared to channel thickness was assumed to avoid the short channel effects. The Si [001] direction is oriented along the z-axis and transport takes place along the Si [110] direction. The results from H-passivated devices and TB calculations are also shown for comparison.

Myung, 2021

- Restructuring TCAD system: Teaching traditional TCAD new tricks

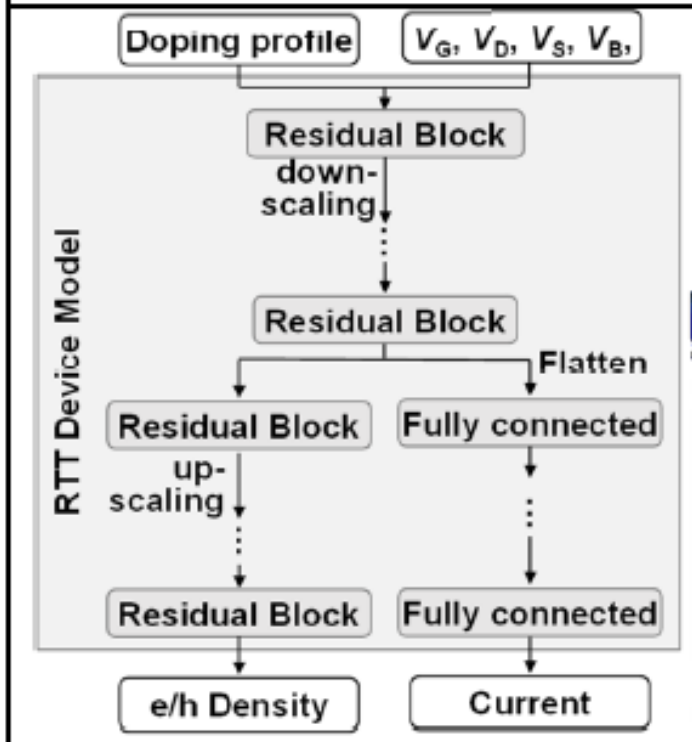


Fig. 5. Illustration of RTT device model, which can predict both electron/hole density and the current.

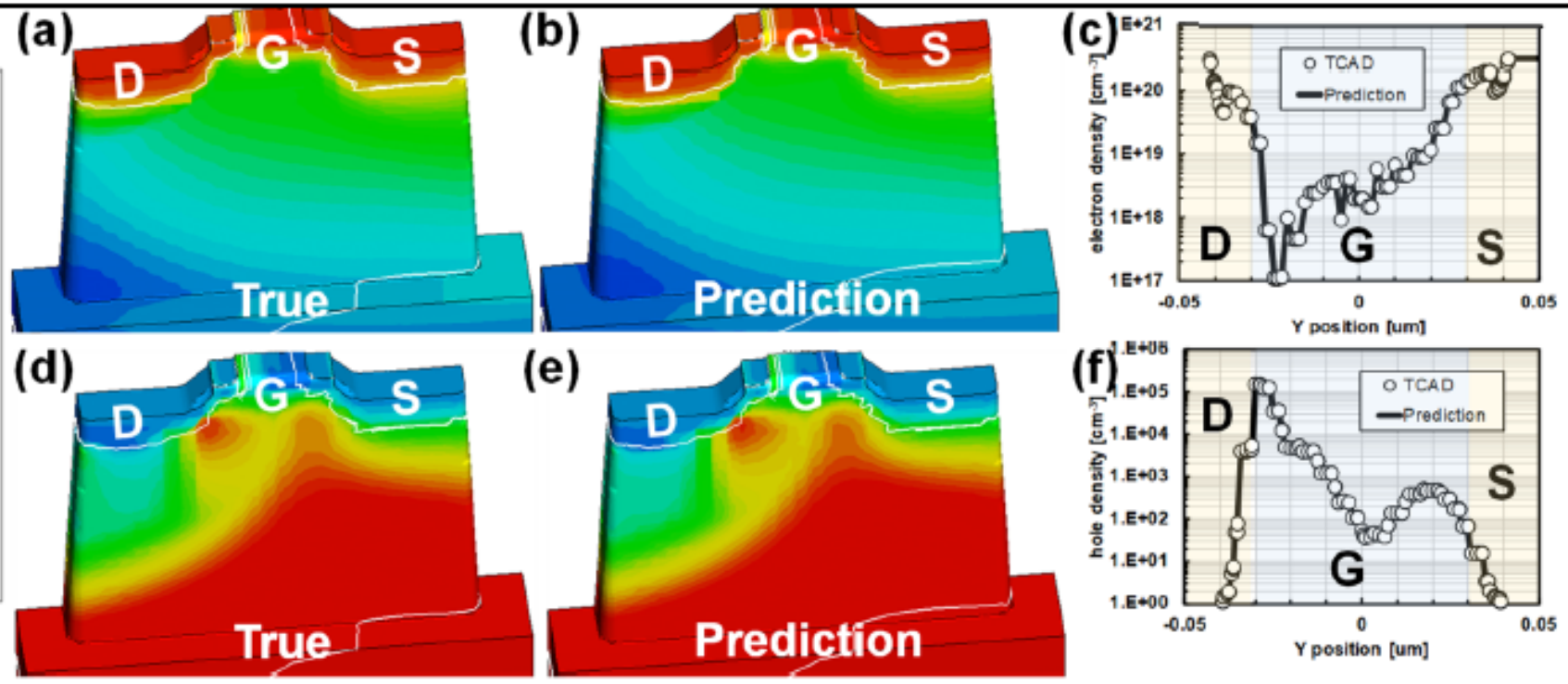


Fig. 6. Electron density of (a) TCAD (b) RTT device model at V_D=V_G=V_{DD}. (c) 1-D electron density in the horizontal direction below the gate. Hole density of (d) TCAD (e) RTT device model at V_D=V_G=V_{DD}. (f) 1-D hole density in the horizontal direction below the gate.

Rzepa, 2022

- Performance and variability-aware SRAM design for gate-all-around nanosheets and benchmark with FinFETs at 3nm technology node

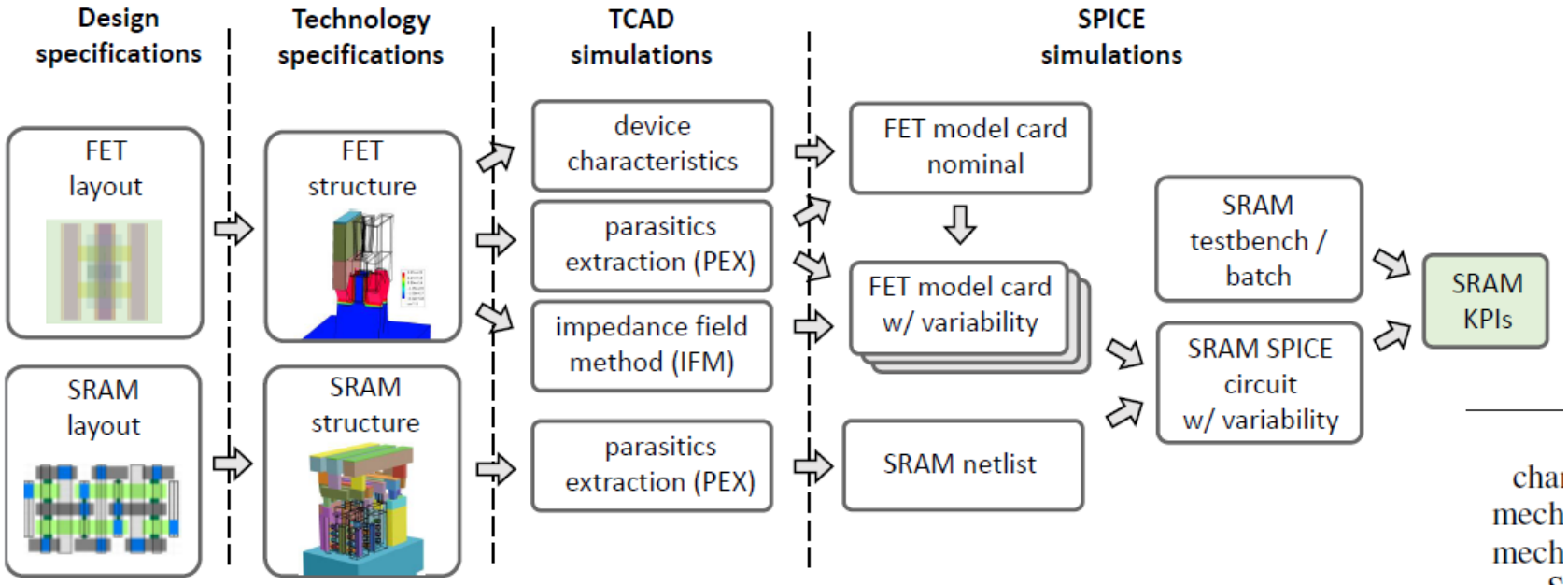


Fig. 1: Simulation flow combining TCAD with SPICE simulations allowing for variability-aware design and technology assessment [7]. Both single FET and full SRAM structures are generated, but the latter is only used for fast PEX to obtain the full SRAM netlist. On the contrary, FETs are extensively characterized with TCAD to extract accurate BSIM-CMG model cards including variability. Combining the SRAM netlist with the FET model cards enables fast SPICE simulations.

Concluding remarks

- Design-Technology Co-Optimization (DTCO)
- Process research using the density-functional theory (DFT)
- Simulation capability

Thank you!