# Computational Microelectronics L2

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# Binary adder

# Addition of binary numbers

- We can recognize that
  - Addition of two 1-bit binary numbers is the core operation.
  - There are only *four* possible cases.

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 10$$

Carry

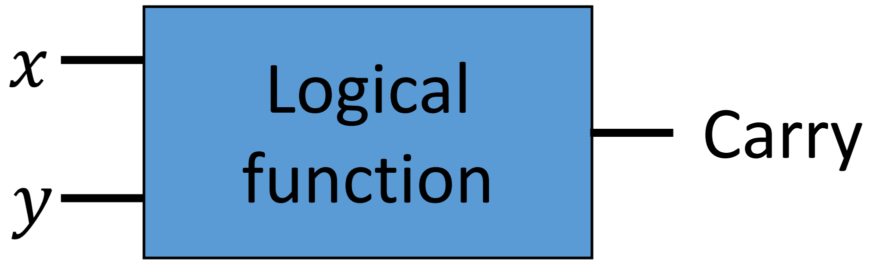
# Inclusion of carry-bit

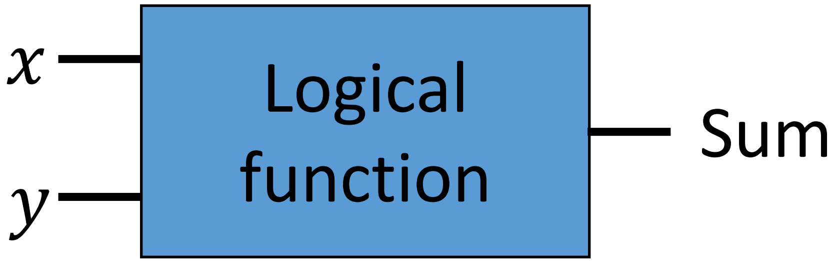
- We introduce a separate bit for representing the carry.
  - Carry-bit & sum-bit

Carry

$$0 + 0 = 0\ 0$$
$$0 + 1 = 0\ 1$$
$$1 + 0 = 0\ 1$$
$$1 + 1 = 1\ 0$$

Sum



# Truth tables

- Relation between $x$, $y$, and the output
  - Sum-bit
    $x$ XOR $y$

| $\boldsymbol{x}$ | $\boldsymbol{y}$ | **sum** |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

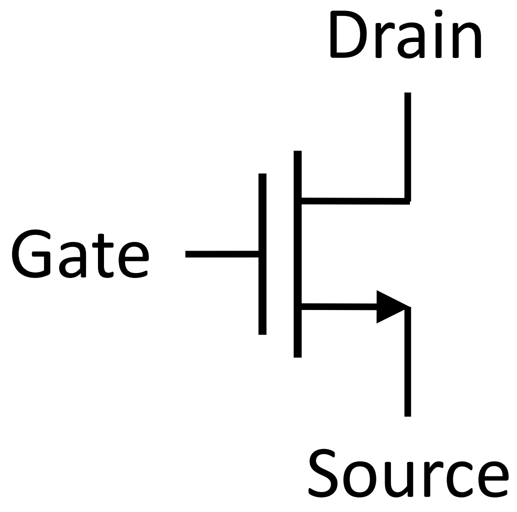
  - Carry-bit
    $x$ AND $y$

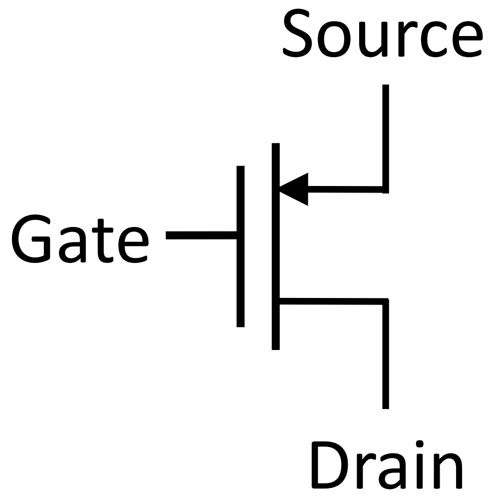
| $\boldsymbol{x}$ | $\boldsymbol{y}$ | **carry** |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

# Compact MOSFET model

# MOSFET

- Basic unit of microelectronics
  - Controlled by the gate voltage
  - NMOSFET and PMOSFET



# Level 1 model (NMOSFET)

- A simple model (Shichman-Hodges)
  - Its basic current model is:
  - Cutoff region, $V_{gs} < V_t$

$$I_d = 0$$

  - Linear region, $V_{ds} < V_{gs} - V_t$

$$I_d = KP \frac{W_{eff}}{L_{eff}} (1 + LAMBDA \times V_{ds}) \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

  - Saturation region, $V_{ds} > V_{gs} - V_t$

$$I_d = \frac{KP}{2} \frac{W_{eff}}{L_{eff}} (1 + LAMBDA \times V_{ds}) \left( V_{gs} - V_t \right)^2$$

  - (Red-colored quantities are the SPICE model parameters.)

# Level 1 model (NMOSFET)

- A simple model (Shichman-Hodges)
  - Threshold voltage:
  - For nonnegative $V_{sb}$,

$$V_t = VTO + GAMMA\left(\sqrt{PHI + V_{sb}} - \sqrt{PHI}\right)$$

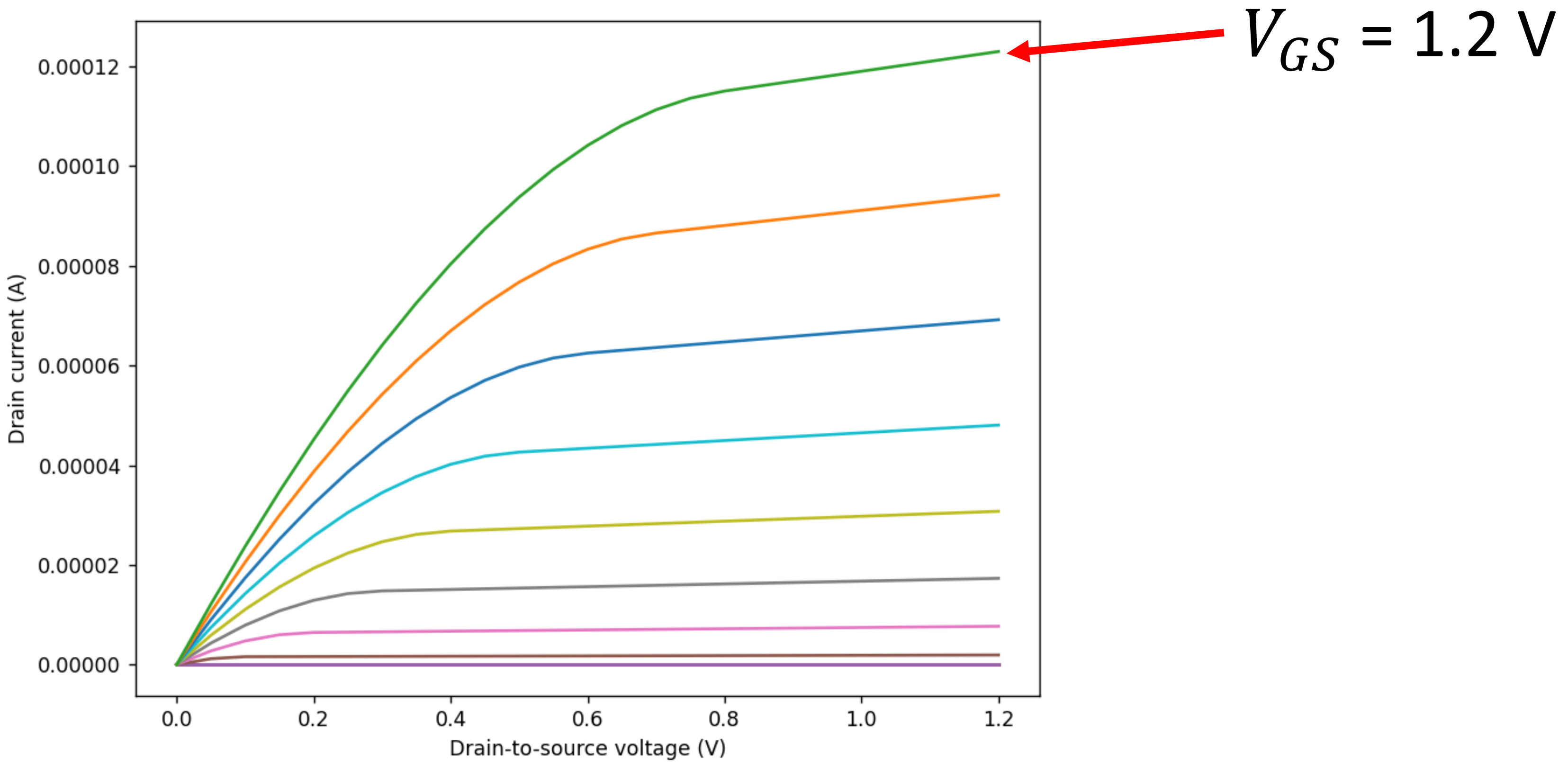
  - $VTO$ is the “zero-bias” threshold voltage.
  - $GAMMA$ is the body effect coefficient.
  - $PHI$ is the surface potential.

# NMOSFET example

- Consider the following parameters:

  `KP=155e-6 LAMBDA=0.2 VTO=0.4 PHI=0.93 GAMMA=0.6`

  – $W_{eff}/L_{eff} = 2$

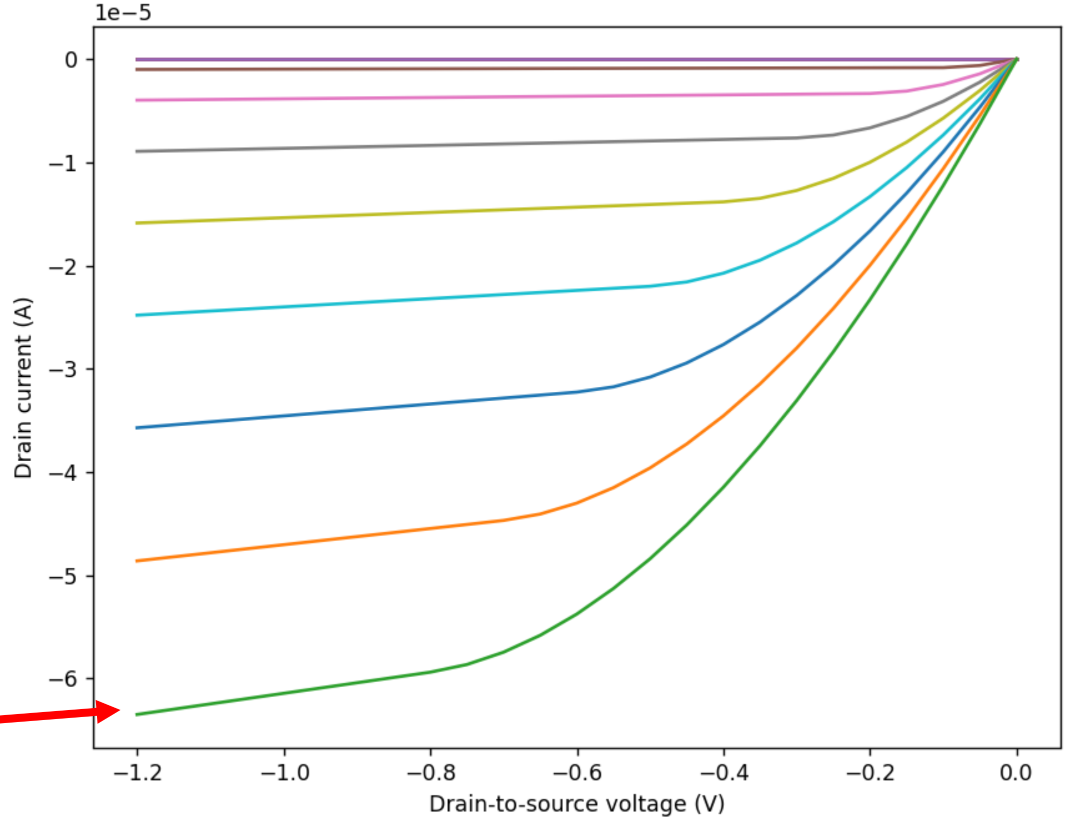


# PMOSFET example

- Consider the following parameters:

  `KP=80e-6 LAMBDA=0.2 VTO=-0.4 PHI=0.93 GAMMA=0.6`

  $-W_{eff}/L_{eff} = 2$

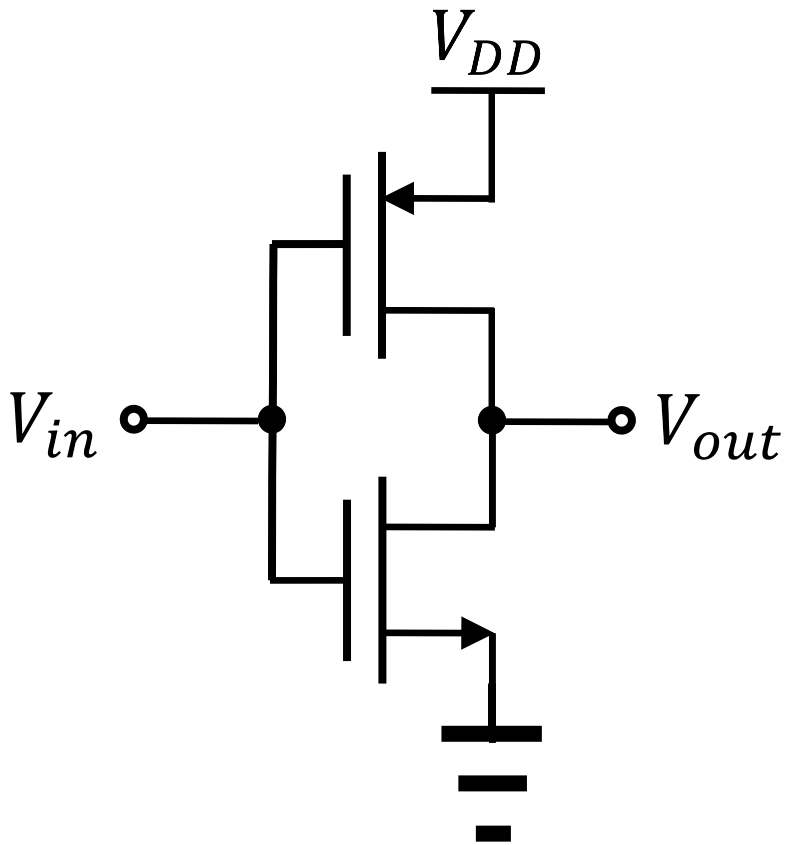



$V_{GS}$ = -1.2 V

# CMOS inverter

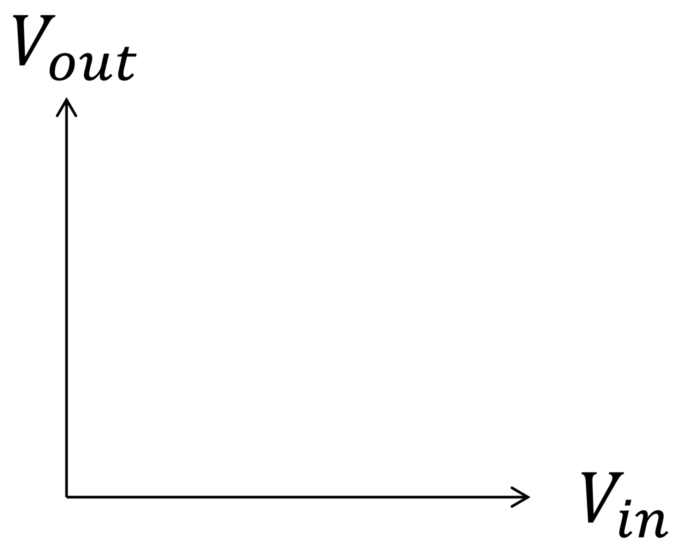
# The simplest logic gate

- When $V_{in}$ = 0,
  - NMOS OFF
  - PMOS ON
  - $V_{out}$ is "pulled up."
  - $V_{out}$ = $V_{DD}$
- When $V_{in}$ = $V_{DD}$,
  - NMOS ON
  - PMOS OFF
  - $V_{out}$ is "pulled down."
  - $V_{out}$ = 0



# Assume that $V_{in}$ is given.

- The goal is to calculate $V_{out}$.
  - $V_{out}(V_{in})$ is called the voltage transfer curve.




  - What is the condition for a point on the VTC?

$$I_{Dn} + I_{Dp} = 0$$

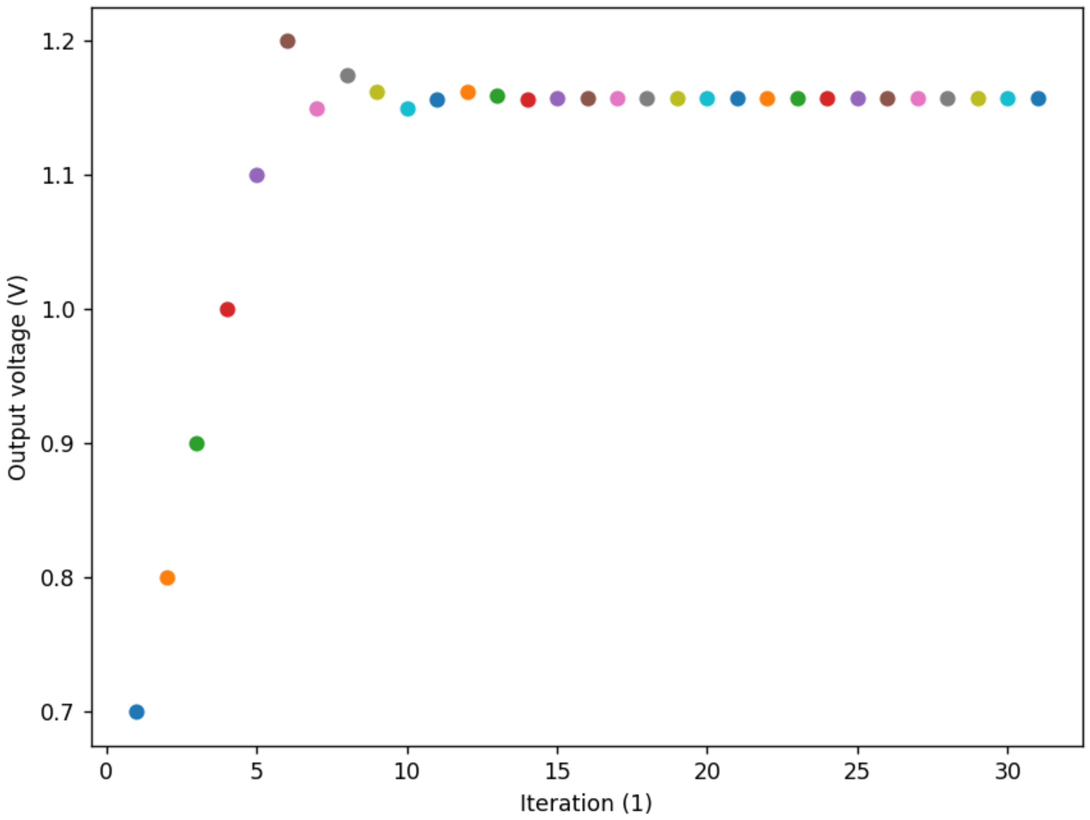
  - Assume that $V_{DD}$ = 1.2 V.
  - For example, at $V_{in}$ = 0.5 V and $V_{out}$ = 0.7 V, we have $I_{Dn}$ = 1.77 μA and $I_{Dp}$ = -7.92 μA. Certainly, it is not on the VTC.

# One possible way (Trial-and-error)

- In order to increase $I_{Dn}$, we can try a higher $V_{out}$, for example 0.8 V.
  - Still, the currents are much different.
  - 0.9 V. No.
  - 1.0 V. No.
  - 1.1 V. No.
  - 1.2 V. Well, now, $I_{Dn}$ = 1.92 µA and $I_{Dp}$ = 0 A. We must increase $\left|I_{Dp}\right|$.
  - 1.15 V. $I_{Dn}$ = 1.91 µA and $I_{Dp}$ = -2.22 µA. We must increase $I_{Dn}$.
  - 1.175 V. $I_{Dn}$ = 1.91 µA and $I_{Dp}$ = -1.16 µA. We must increase $\left|I_{Dp}\right|$.
  - 1.1625 V. $I_{Dn}$ = 1.91 µA and $I_{Dp}$ = -1.70 µA. We are getting closer…

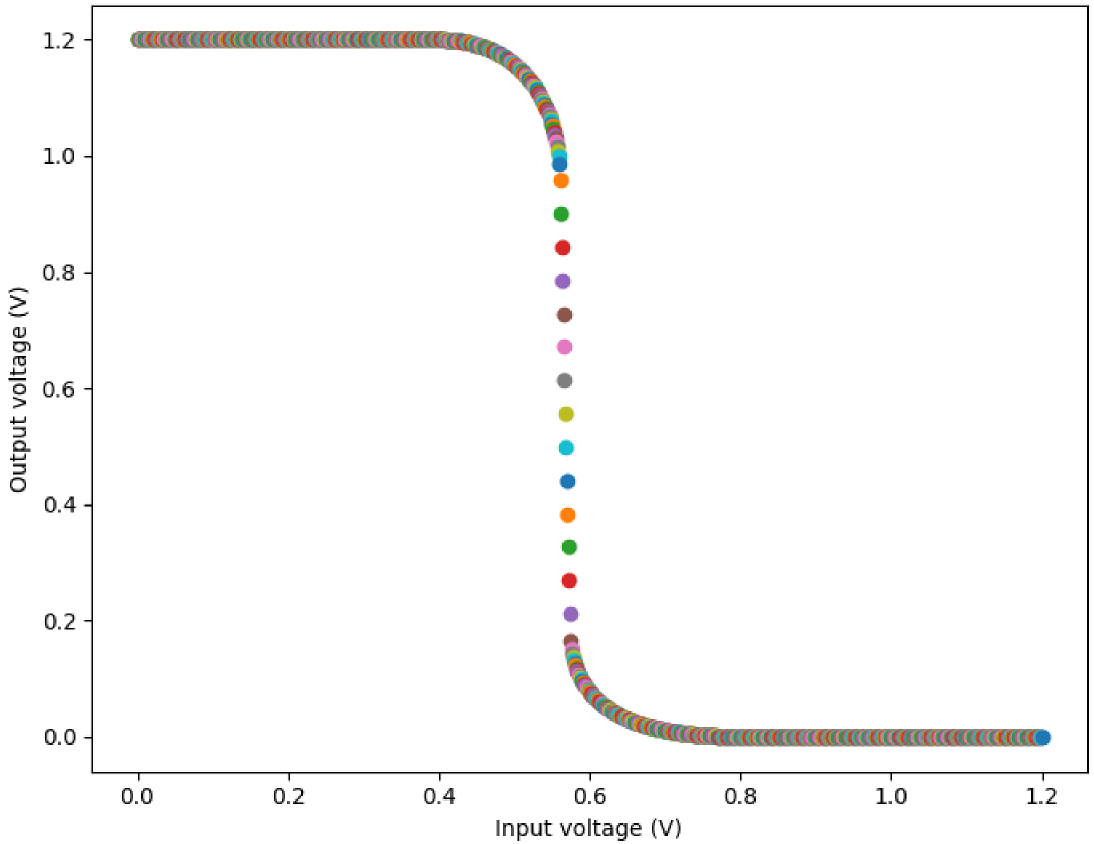
# Number of iterations

- When we have a voltage change smaller than 1 µV, the calculation stops.
  - Start at $\frac{V_{DD}}{2}$.
  - Initial step is 0.1 V.
  - When the sign of difference changes, the step is reduced with a factor of 0.5. Otherwise, keep the step.
  - 31 iterations at $V_{in}$ = 0.5 V



# Homework#2

- Due: AM08:00, September 19 (Two weeks later)
- Problem#1
  - Draw the voltage transfer curve.



# Thank you for your attention!