Special Topics on Basic EECS I
VLSI Devices
Lecture 19 - Memory

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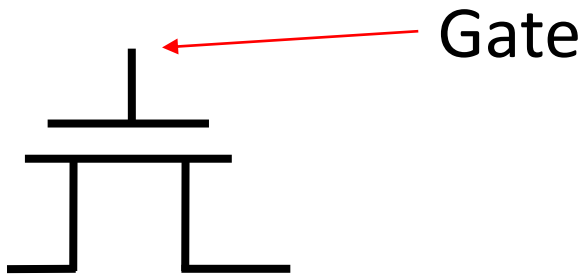
L19 is for memory devices.

- L18 was for the MOS capacitor.
- Due to my business trip (International Memory Workshop),
  - L19 was recorded.

- L20 (May 20) will consider the MOS capacitor, again.

Note that

- To understand this lecture, we must first understand the operation of MOS transistors.
  - However, we are still considering the MOS capacitor… ☹
  - Treat the MOS transistor as a switch controlled by the gate voltage.
  - Its threshold voltage is V_t.

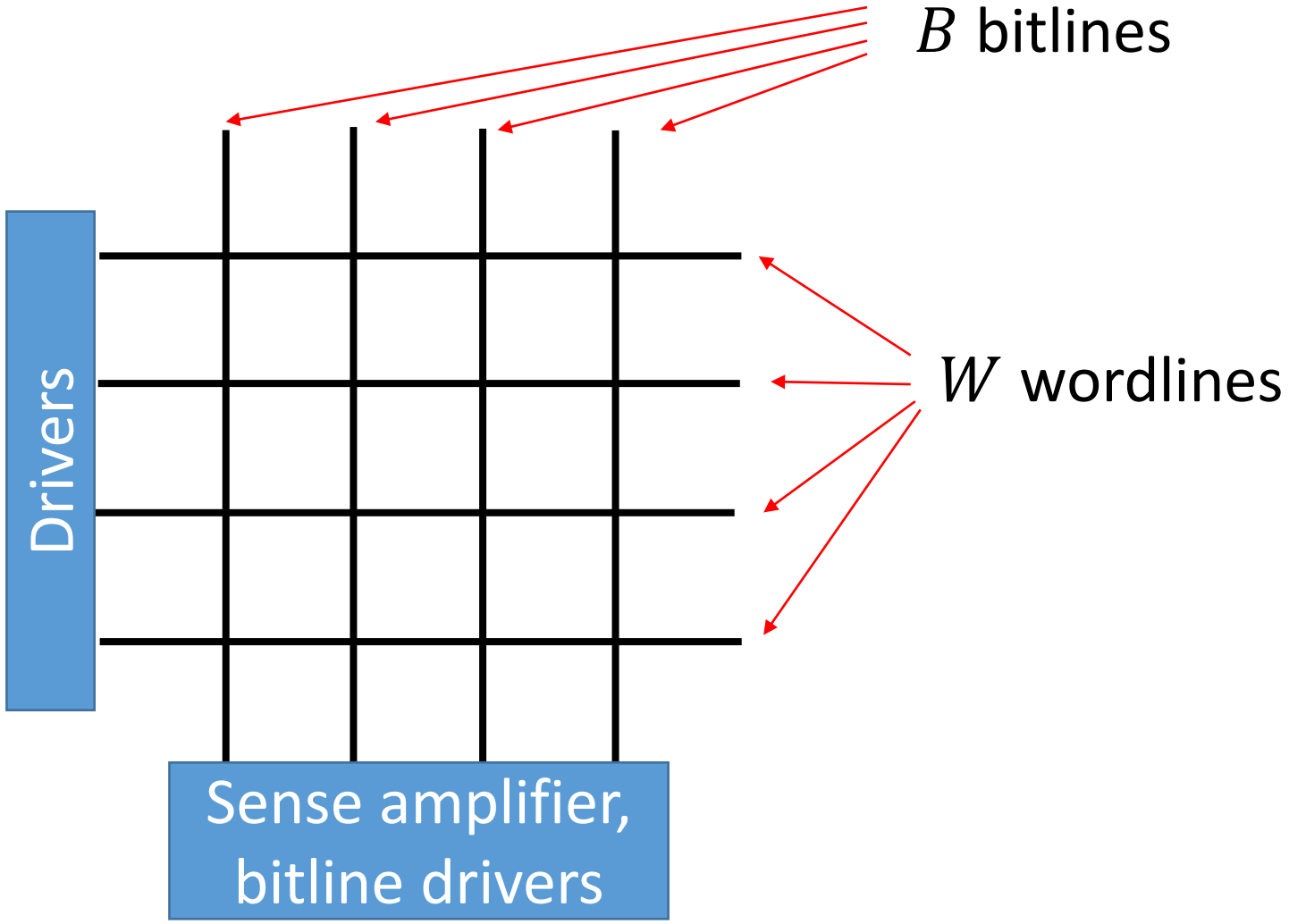


Memory devices

- Three representative memory devices
  - SRAM
  - **DRAM**
  - NAND
- There are also “new” memory devices.
  - FeRAM
  - PCRAM
  - STT-MRAM
  - ReRAM

Array of memory cells

- $W \times B$ bits

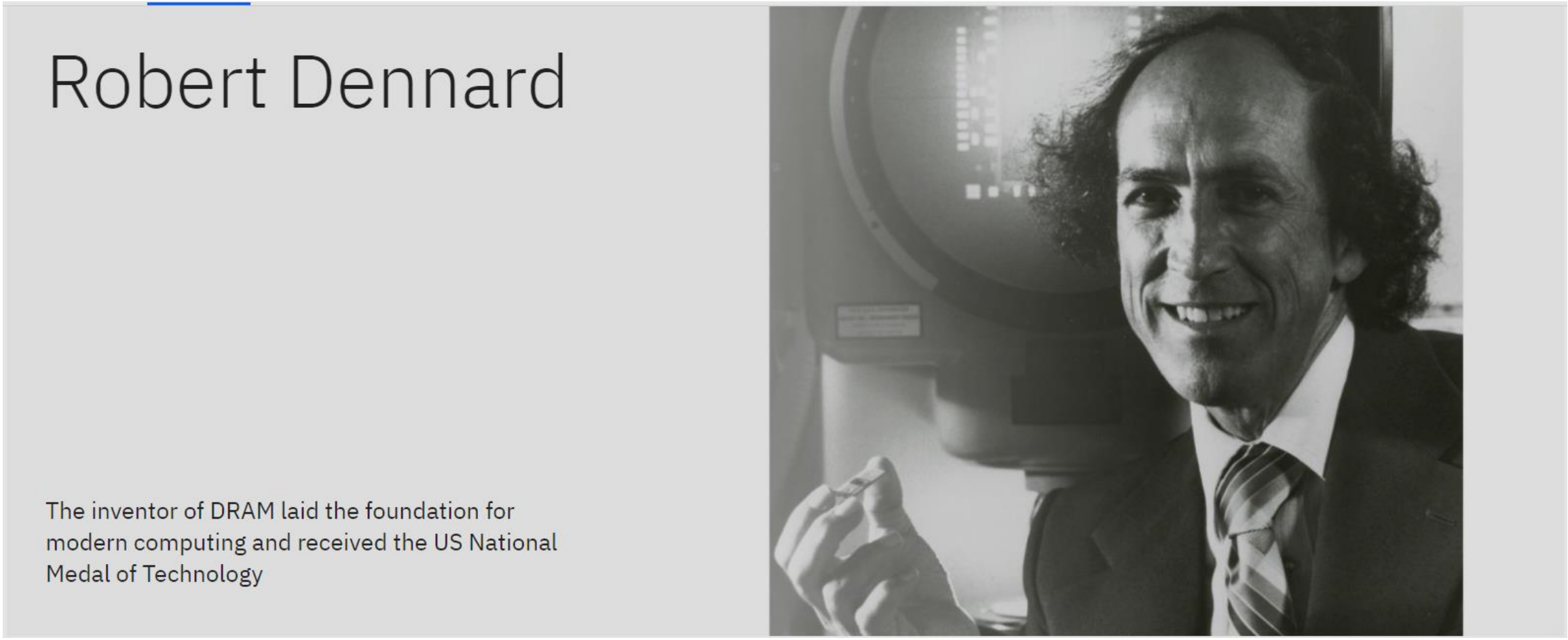


SRAM (Static Random-Access Memory)

- For the SRAM device, watch my previous lecture.
  - Title: **[DIC2023] L25_20231205**
  - Starting point: 35:05

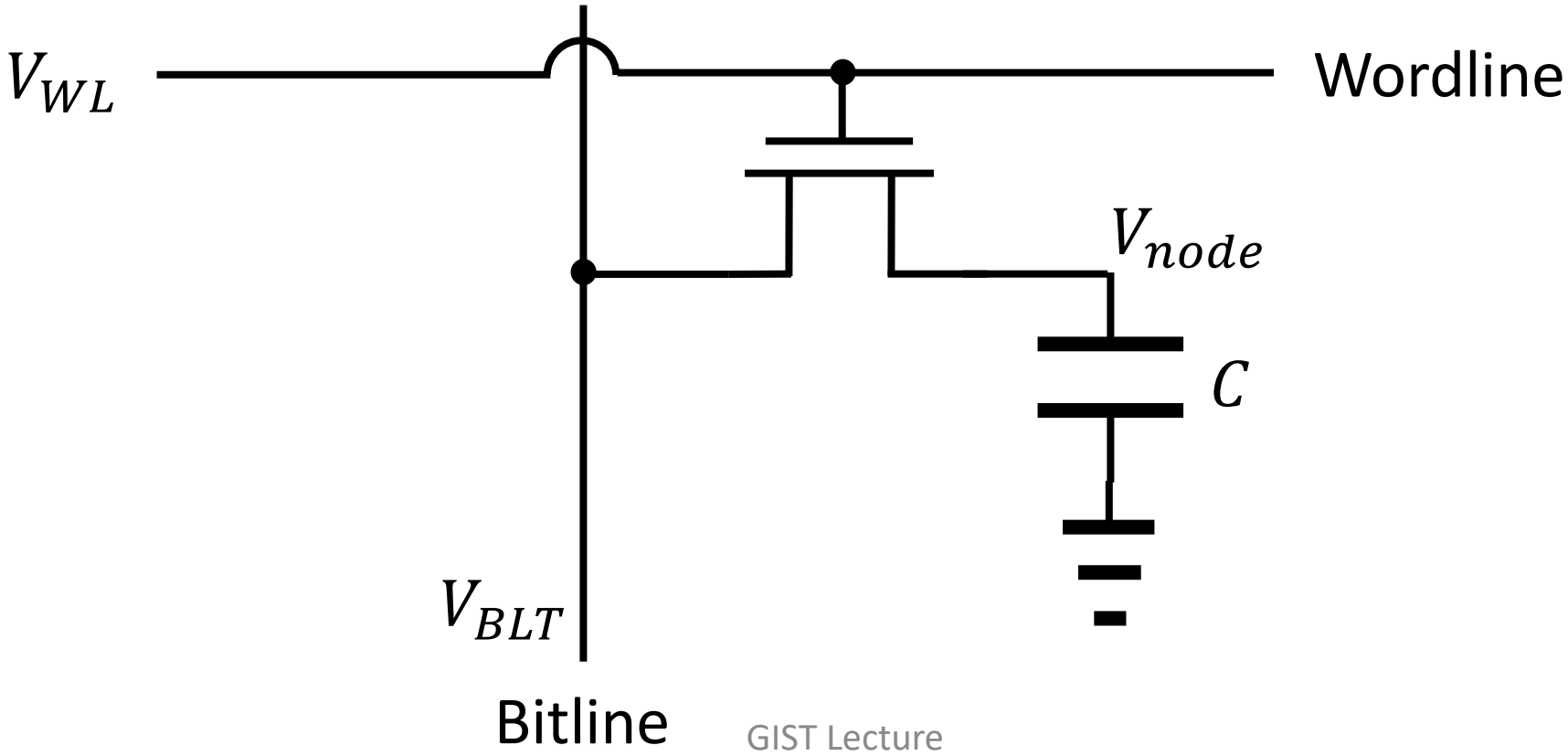
DRAM (Dynamic Random-Access Memory)

- Robert Dennard, the inventor of DRAM, passed away on April 23, 2024.



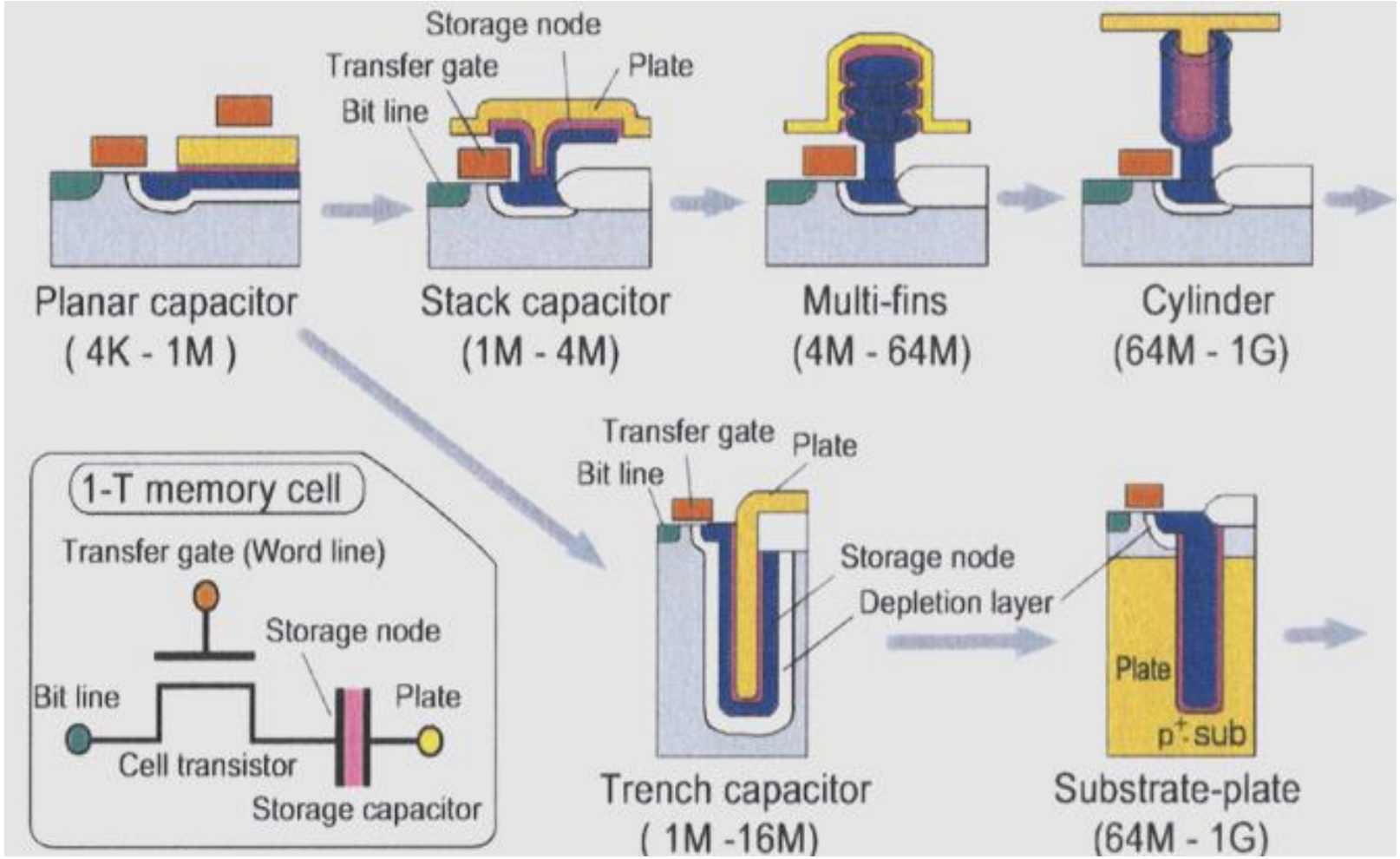
1T1C

- It is considerably smaller in silicon area than a CMOS SRAM cell.
  - The cell is in state “1” when there is charge in the capacitor.



Capacitor

- Its capacitance is ~ 10 fF nowadays.



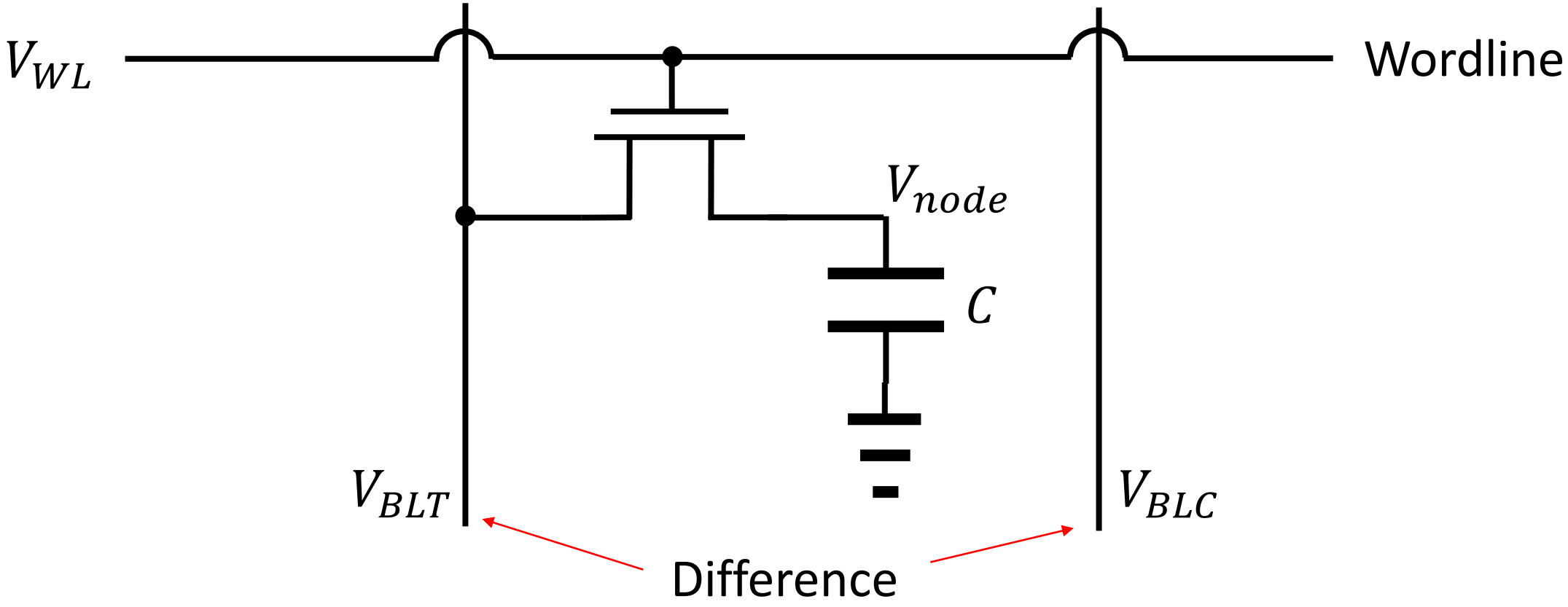
Major advancement in DRAM cell innovation
(H. Sunami, ICSICT 2008)

WRITE operation

- It is straightforward to write a “0” to a DRAM cell.
  - V_{WL} is V_{dd}. V_{BLT} is 0 V.
  - Then, V_{node} is 0 V.
- In writing a “1,”
  - V_{WL} is boosted to be higher than $V_{dd} + V_t$. V_{BLT} is V_{dd}.
  - Then, V_{node} can reach V_{dd}.
- After the storage node is fully charged or discharged,
  - The wordline is brought back to its standby voltage. (The transistor is turned off.)

READ operation

- A cross-coupled CMOS sense amplifier
  - BLT and BLC are precharged to $V_{dd}/2$.



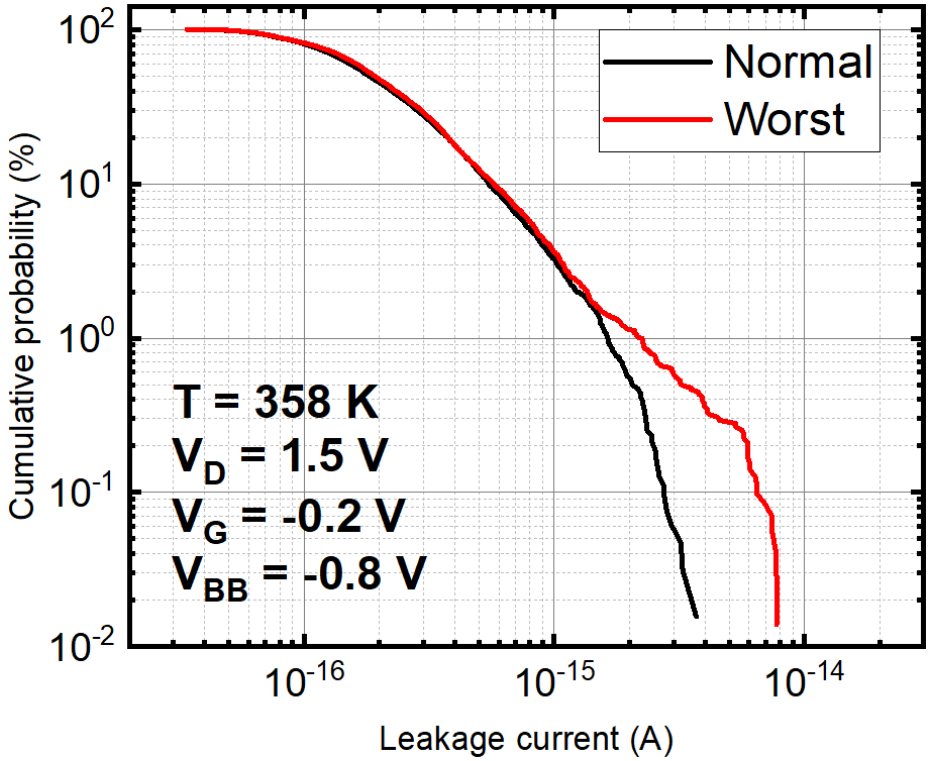
Sense amplifier

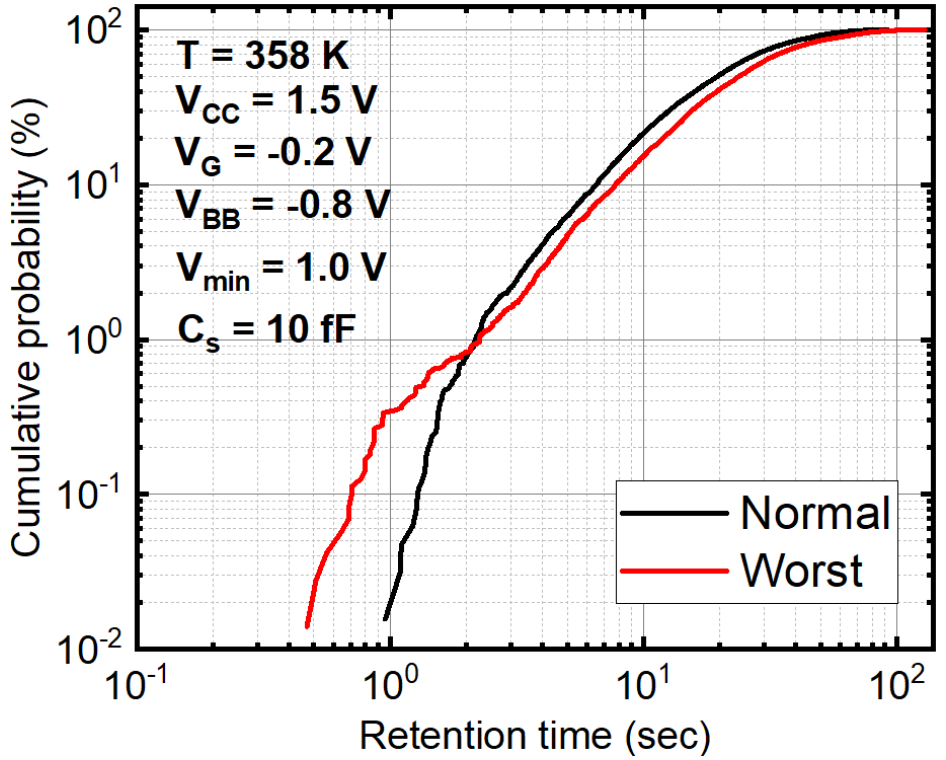
- The same boost of the wordline to $V_{WL} > V_{dd} + V_t$ is applied.
  - If a "0" bis it stored in the cell, V_{BLT} is discharged to below $V_{dd}/2$.
  - If a "1" bit is stored in the cell, V_{BLT} is charged to above $V_{dd}/2$.
- After a differential signal is developed between BLT and BLC,
  - The sense amplifiers is activated.
  - It restores V_{node}. (Refresh)
- Read signal, V_s

$$V_s(C_{cell} + C_{bitline}) = \left(V_{node} - \frac{V_{dd}}{2}\right) C_{cell}$$ Taur, Eq. (9.11)

Leakage current

- The charge stored in the capacitor leaks away over time.
  - Periodic read and refresh are necessary.
  - Retention time: Time interval between data refreshes
  - A typical worst-case data retention time is about 100 ms.





Thank you!