Special Topics on Basic EECS I
VLSI Devices
Lecture 18

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Switching from OFF to ON

- It takes some time before the diode is turned on and reaches the steady state.
  - Charging up the depletion-layer capacitor
  - Filling up the p- and n-regions with excess minority carriers
- Similarly, when a diode is switched from the ON state to the OFF state, it takes some time before the diode is turned off.

Excessive minority carriers

- (The lightly doped side is often referred to as the *base* of the diode. The other one is called the *emitter*.)
  - Total excess minority-carrier charge per unit area

$$Q_B = -q \int_0^W (n_p - n_{p0}) dx$$ Taur, Eq. (2.144)

  - For a wide-base diode,

$$Q_B = J_n(x=0)\tau_n$$ Taur, Eq. (2.145)

  - For a narrow-base diode,

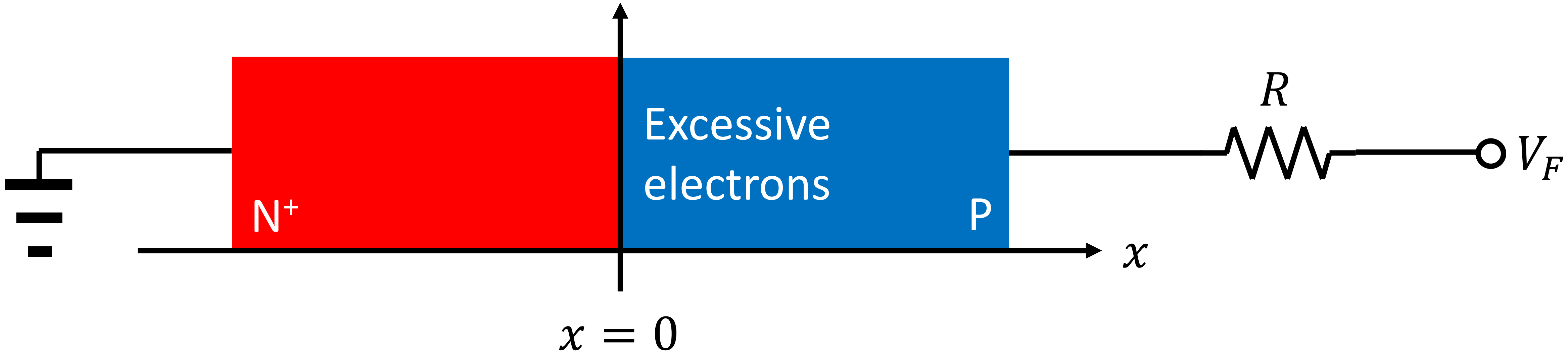
$$Q_B = J_n(x=0)t_B$$ Taur, Eq. (2.146)

Base-transit time, $\frac{W^2}{2D_n}$

Discharging time of a forward-biased diode

- External voltage changes from V_F to V_R at $t = 0$. Assume that $|V_F|$ and $|V_F|$ are sufficiently higher than 1.0 V.
  - At $t < 0$,

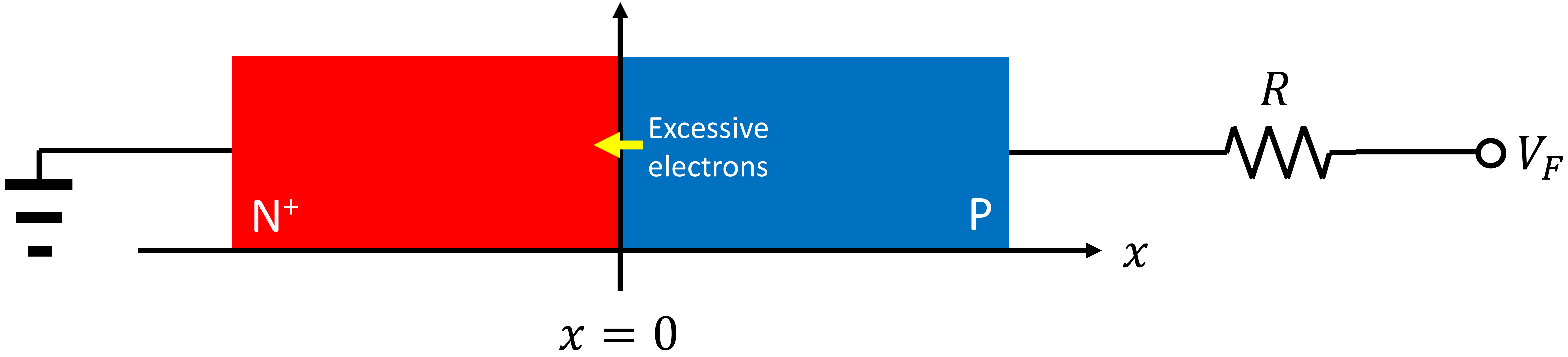
$$I \approx \frac{V_F}{R}$$



Reverse voltage of V_R

- Electrons at the edge of the depletion region are swept away by the electric field in the depletion region towards the n$^+$ emitter at a saturated velocity.
  - The reverse current is limited by the external resistor,

$$I \approx \frac{V_R}{R}$$ (Note that it is a negative number.)

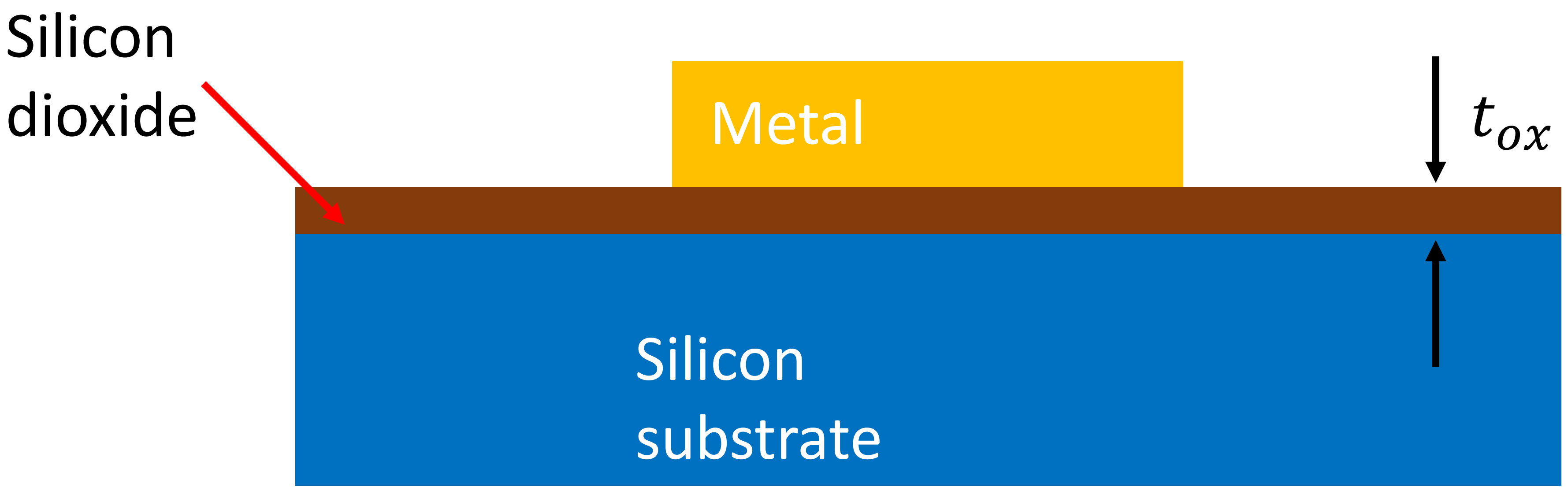


Later,

- The reverse current is limited by the diffusion of electrons instead of by the external resistor.
  - Finally, when all the excess electrons removed, the pn diode is completely off.

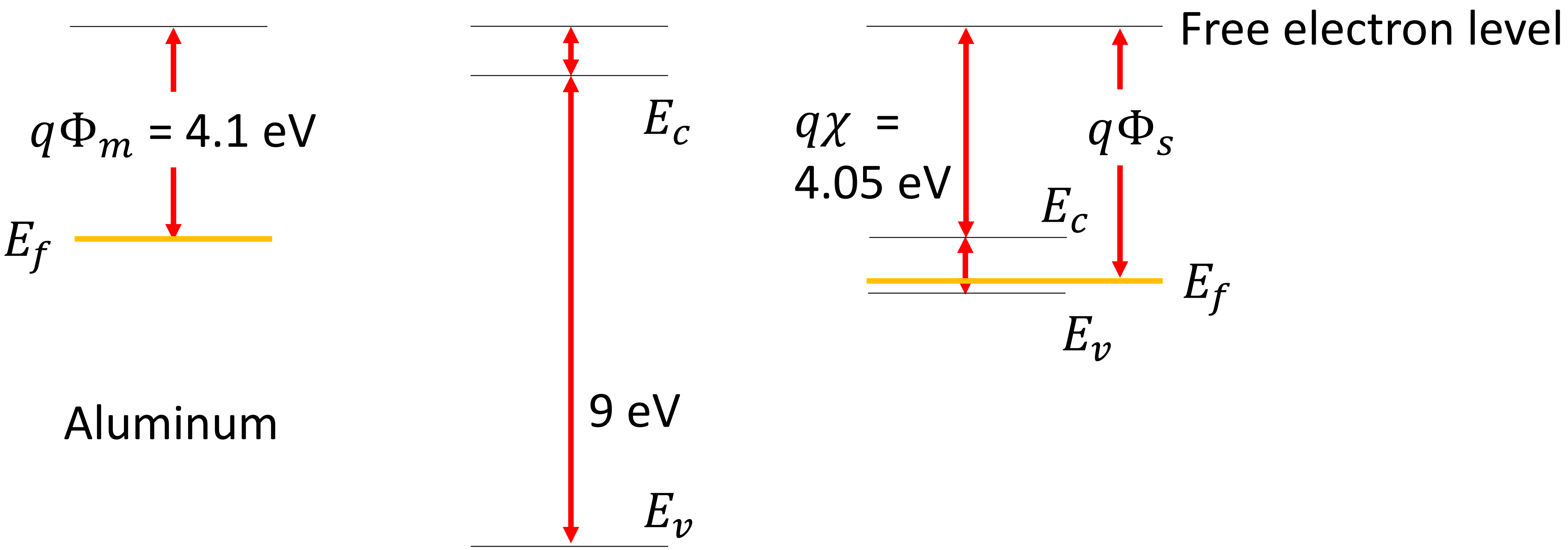
MOS capacitors

- Basis of CMOS technology



Energy band diagram

- Three components
  - Metal, silicon dioxide, and p-type silicon

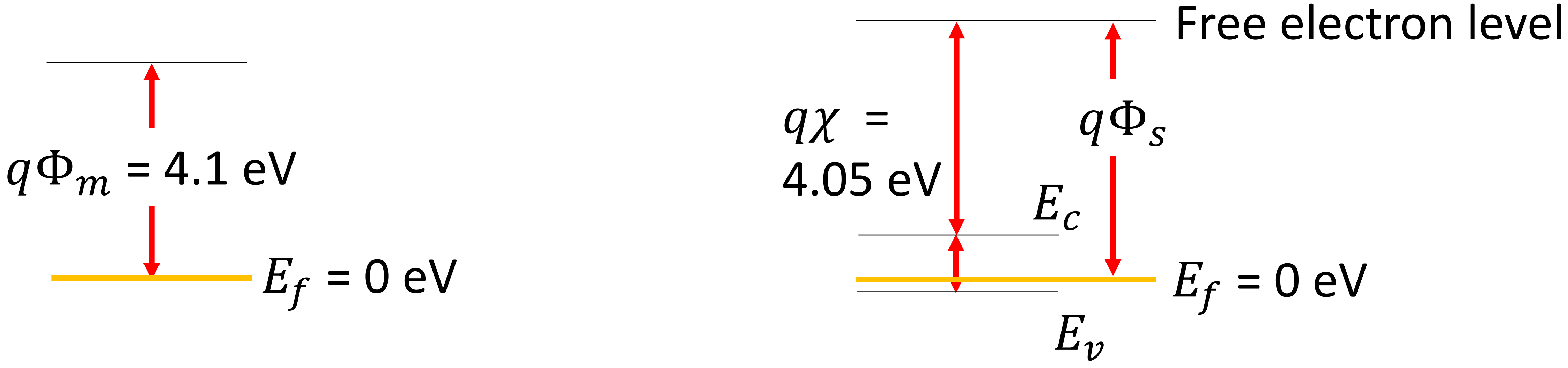


Consider $V_g = V_{sub}$ = 0 V.

- Rule: Align the Fermi level.
  - The energy difference is

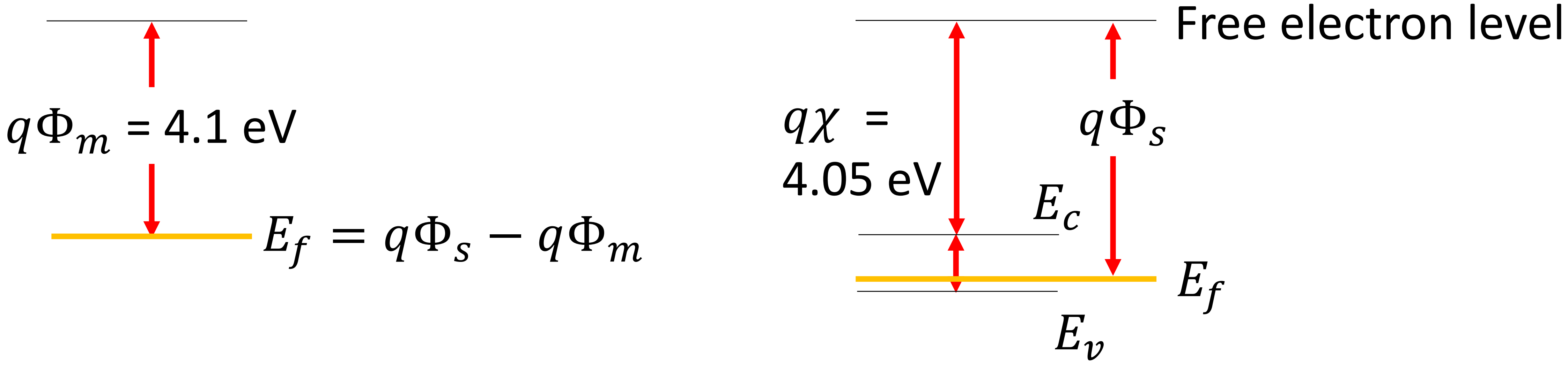
$$q\Phi_s - q\Phi_m$$

  - It means that a non-zero electric field is applied in the oxide layer.



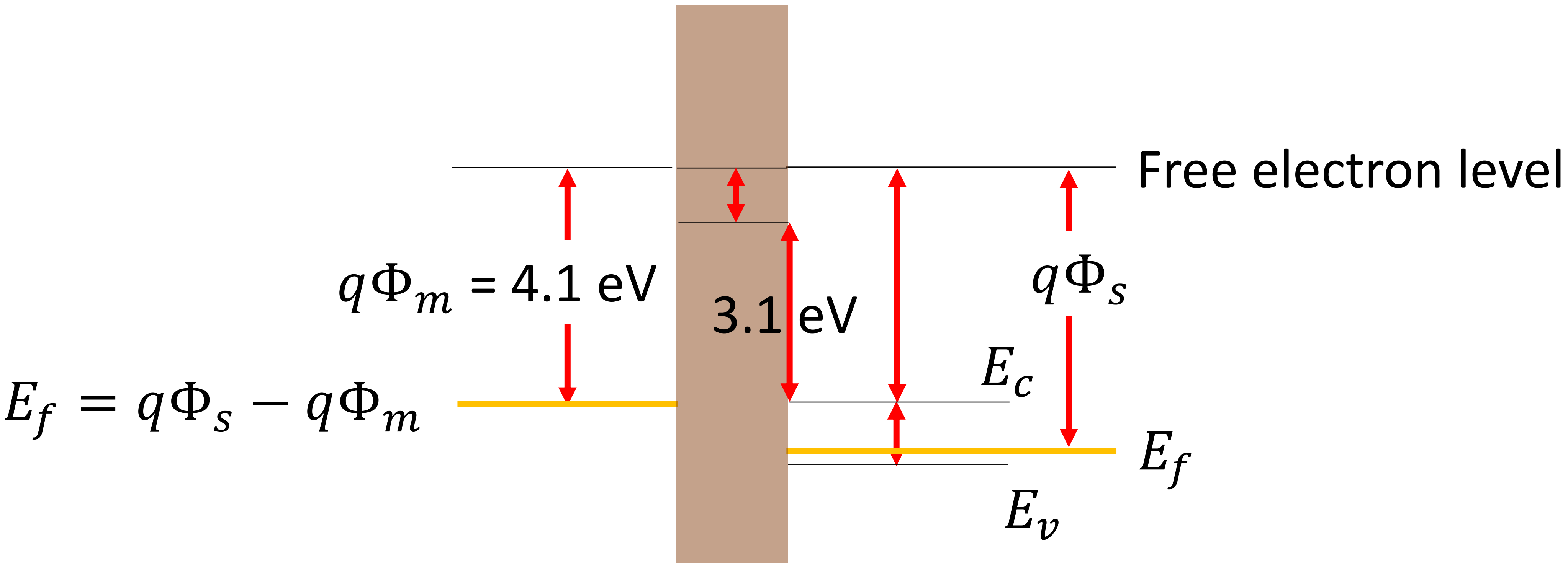
When $V_g = \Phi_m - \Phi_s < 0$,

- The energy band at gate moves upward.
  - There is no energy difference.
  - It means that the energy band becomes flat.
  - This gate voltage is called the flatband voltage, V_{fb}.



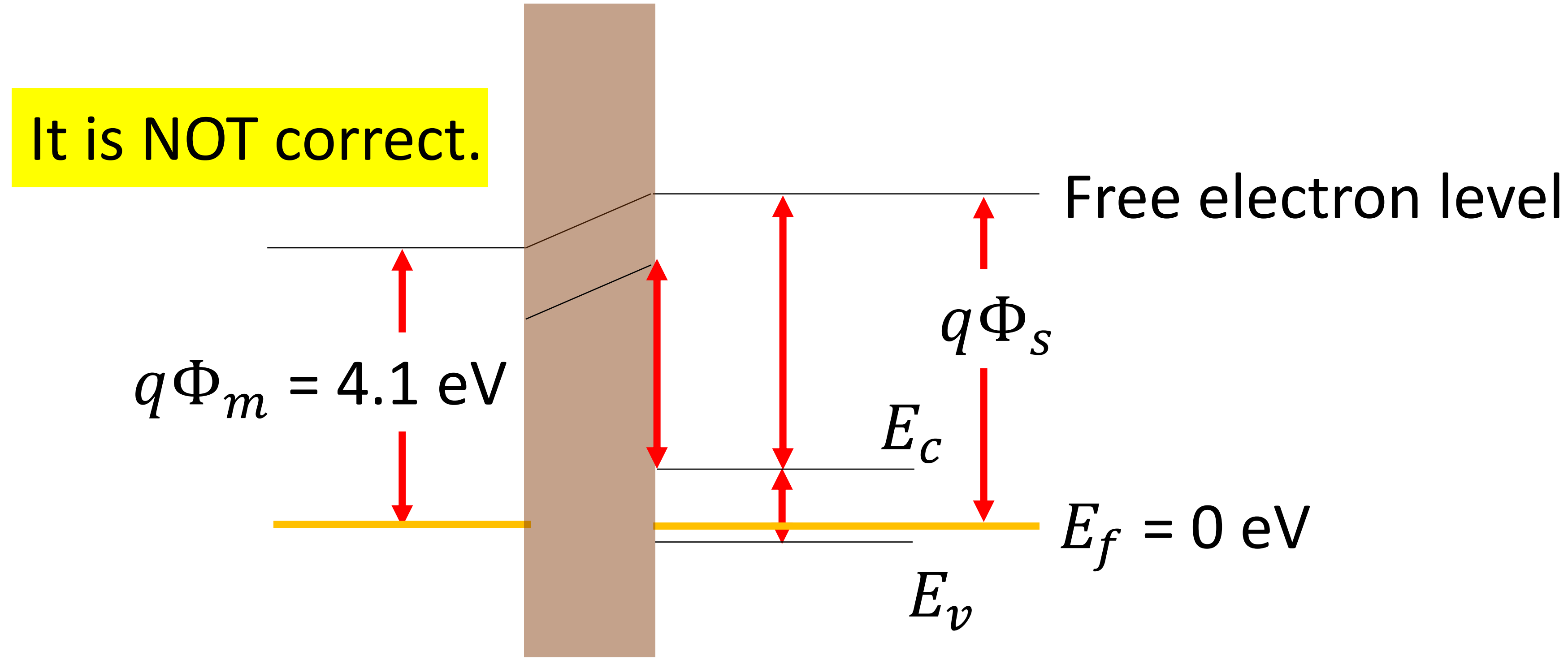
Draw the energy band diagram at $V_g = V_{fb}$.

- Since the energy band is flat, it is not difficult.
  - The electron energy barrier is 3.1 eV between the conduction bnads of silicon and silicon dioxide.



Consider V_g = V_{sub} = 0 V, again.

- Non-zero electric field is found.
  - However, the energy difference, $q\Phi_s - q\Phi_m$, cannot be solely applied to the oxide layer. *Why?*

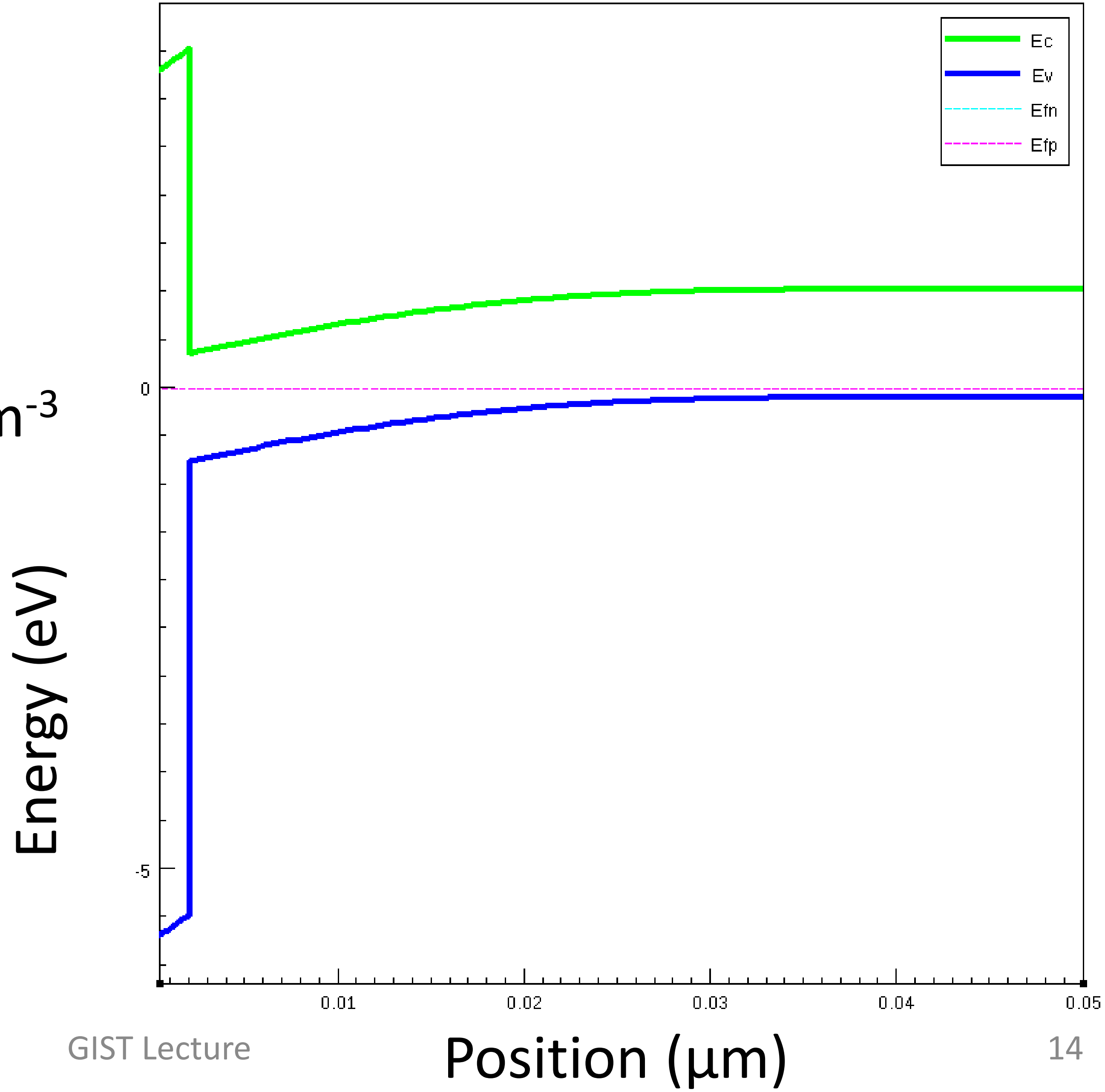


Surface potential, ϕ_s

- A downward bending of bands in the p-type silicon near the surface
  - It is important to note that
    $$V_g - V_{fb} = \phi_s + V_{ox} \qquad \text{Taur, Eq. (2.172)}$$
  - At the silicon-oxide interface,
    $$\epsilon_{ox}|\mathbf{E}_{ox}| = \epsilon_{si}|\mathbf{E}_{si}| \qquad \text{Taur, Eq. (2.173)}$$
  - Since $\epsilon_{ox} = 3.9\epsilon_0$ and $\epsilon_{si} = 11.7\epsilon_0$,
    $$|\mathbf{E}_{ox}| \approx 3|\mathbf{E}_{si}|$$

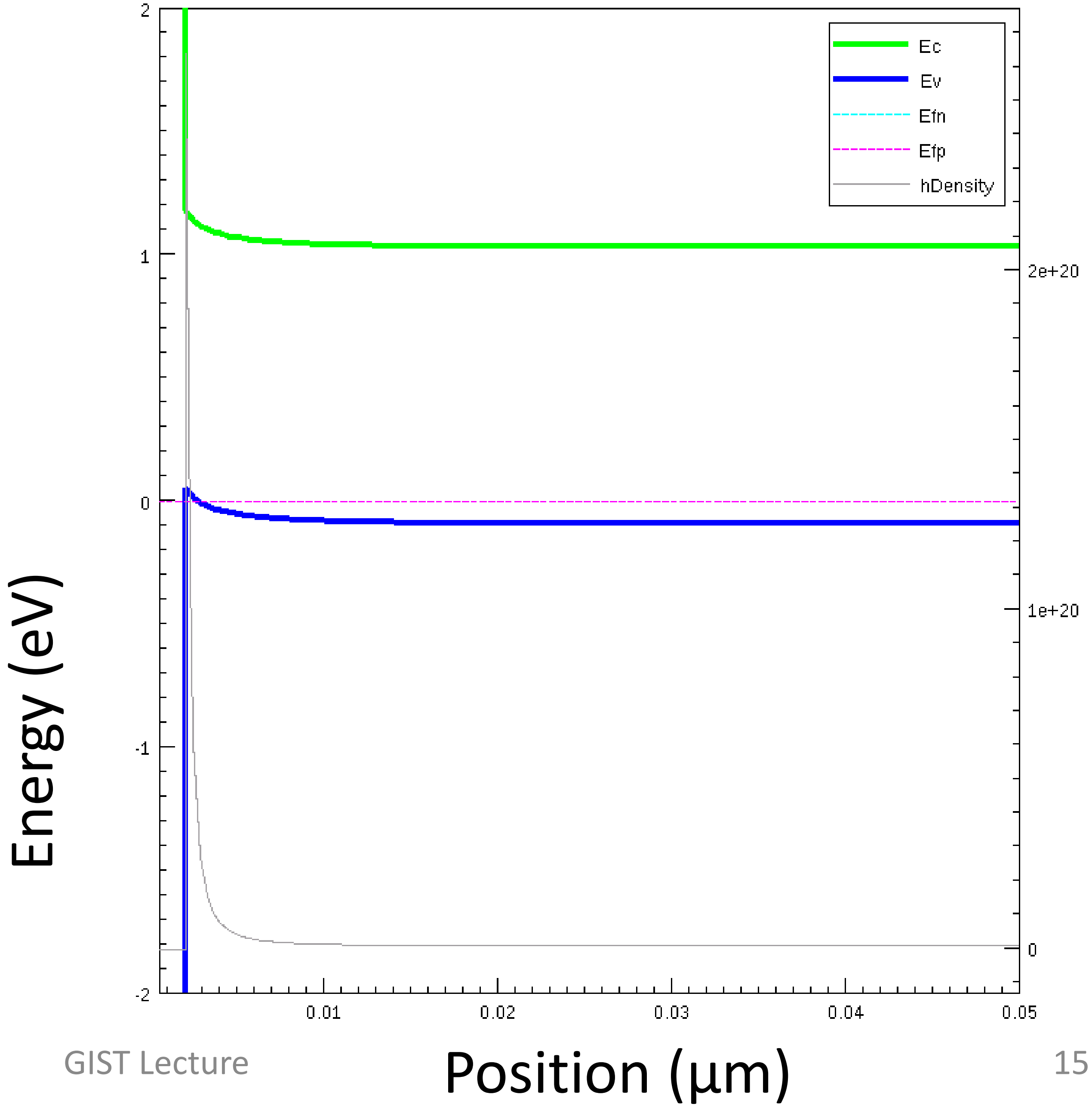
TCAD simulation

- Model parameter
  - Workfunction of 4.17 eV
  - Oxide thickness of 20 Å
  - P-type doping of 1×10^{18} cm^{-3}



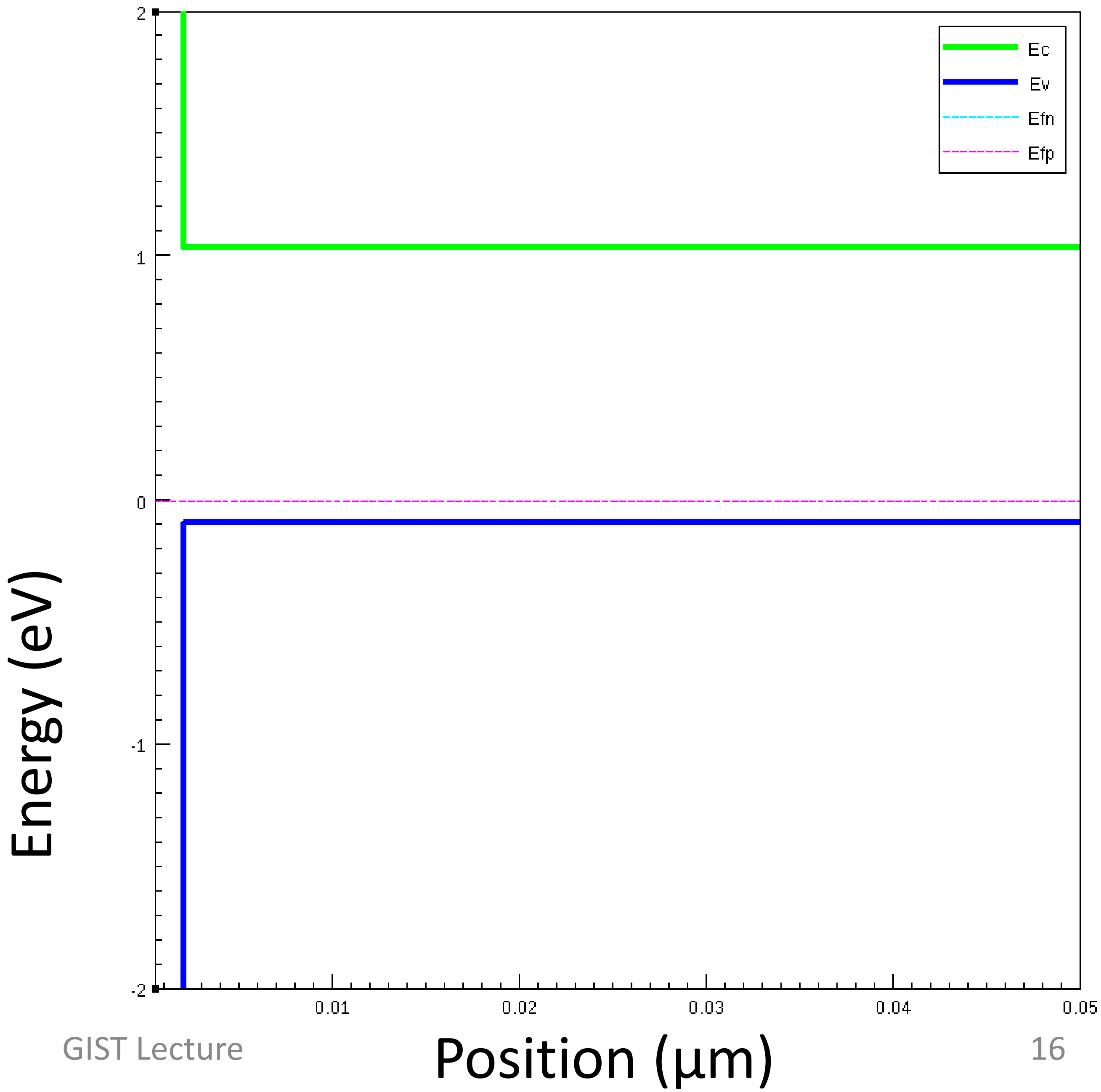
Case1

- V_g = -2.0 V
  - Accumulation
- Hole density



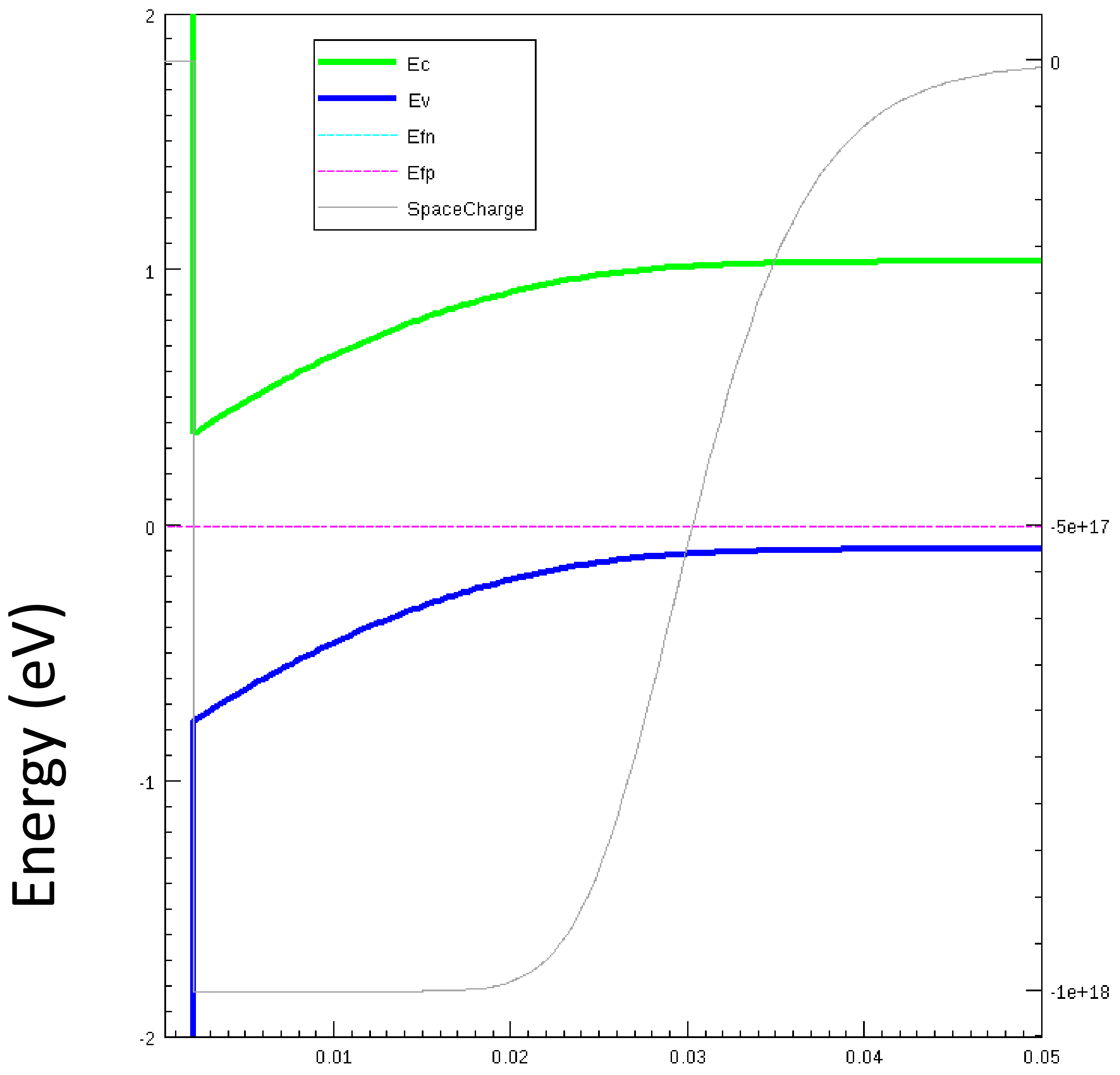
Case2

- V_g = -0.94 V
  - Flatband condition



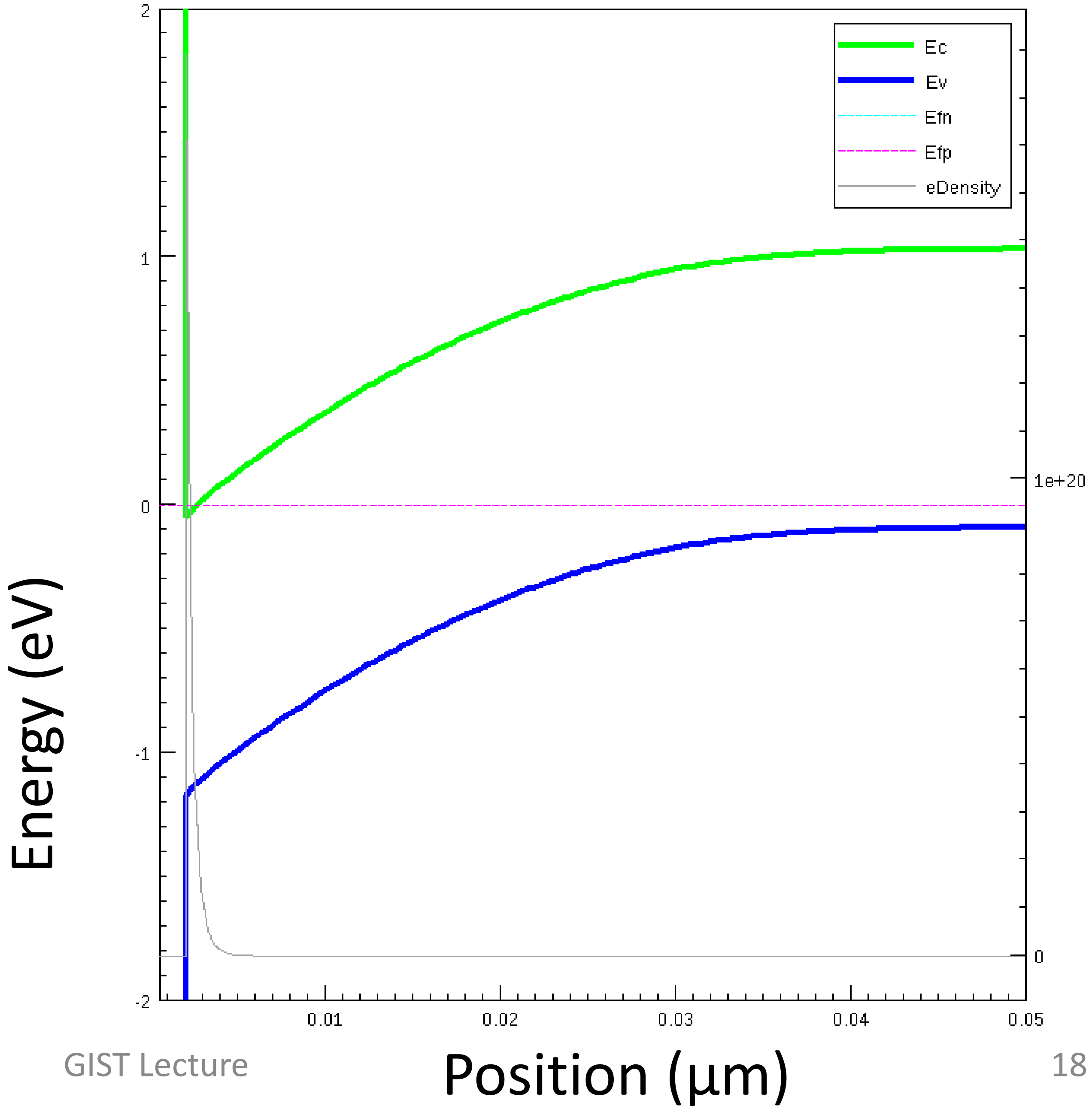
Case3

- V_g = 0.0 V
  - Depletion
- Space charge



Case4

- V_g = 1.0 V
  - Inversion
- Electron density



Thank you!