Digital I.C Assignment

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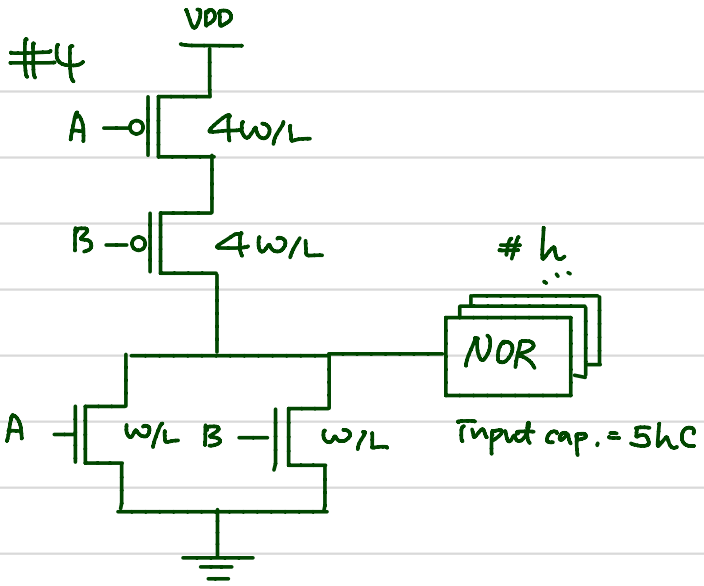
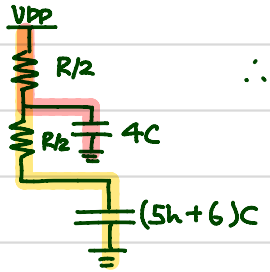
#4

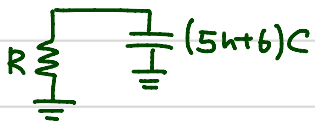


① rising delay



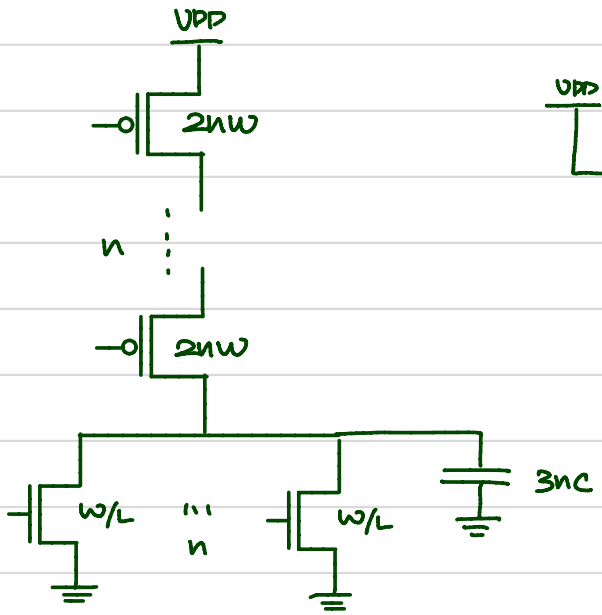
$\therefore t_{pd} = [4C \cdot R/2] + (5h+6)C \cdot R = (8+5h)RC$

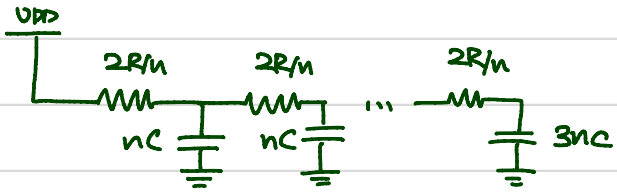
② falling delay



$t_{pd} = (5h+6)RC$

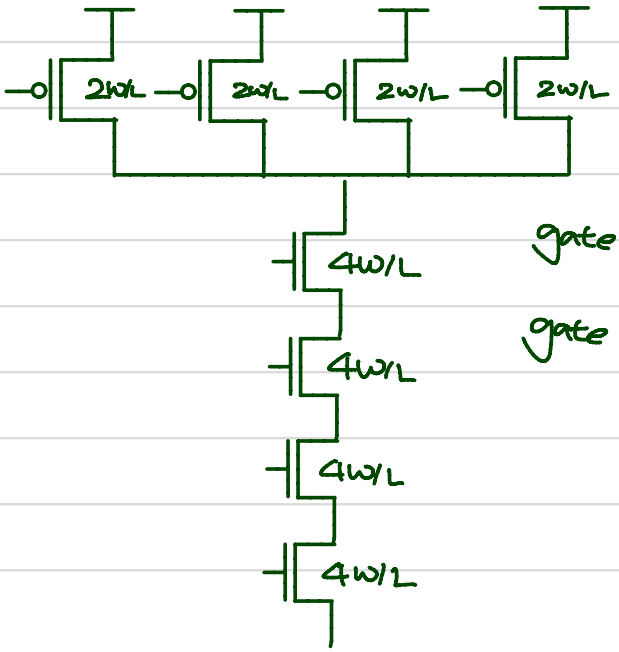
#4.4 n Input NOR gate.





$\frac{2R}{n} \cdot nC + 2 \cdot \frac{2R}{n} \cdot nC + \cdots (n-1) \cdot \frac{2R}{n} \cdot nC + \frac{2R}{n} \cdot n \cdot 3nC = (n^2+2n)RC$

#4.9



gate capacitance = 2C+4C = 6C

gate cap. of standard Inverter = 2C+C = 3C

$\therefore$ logical effort = 6C/3C = 2

4.10

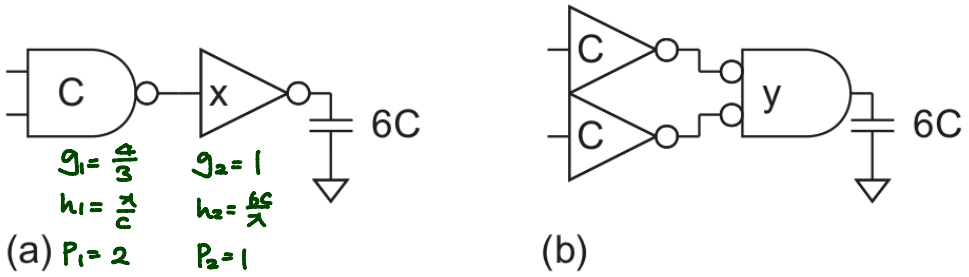
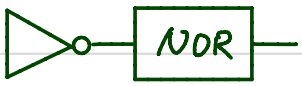


FIGURE 4.39 2-input AND gate

a) $g_1h_1 = g_2h_2 = (g_1g_2h_1h_2)^{1/2} = \frac{4}{3} \cdot 1 \cdot \frac{x}{c} \cdot \frac{6c}{x} = (8)^{1/2} = 2\sqrt{2}$

$\therefore$ Delay $= g_1h_1 + P_1 + g_2h_2 + P_2 = 2\sqrt{2} + 2 + 2\sqrt{2} + 1 = 3 + 4\sqrt{2} = 8.6$

b)



$g_1 = 1$ $\quad g_2 = 5/3$

$h_1 = y/c$ $\quad h_2 = 6c/y$

$P_1 = 1$ $\quad P_2 = 2$

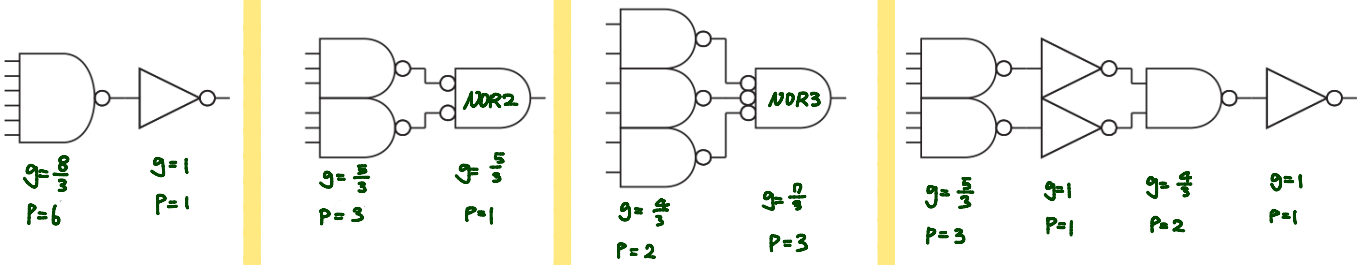
$g_1h_1 = g_2h_2 = (g_1h_1 \cdot g_2h_2)^{1/2} = 10^{1/2}$

delay $= g_1h_1 + P_1 + g_2h_2 + P_2$

$= 2\sqrt{10} + 3 = 3.16 \times 2 + 3 = 9.32$

$\therefore$ delay (a) < delay (b)

4.11



H=1	$2\left(\frac{8}{3} \cdot 1\right)^{1/2} + 7 = 10.3$	$2\left(\frac{5}{3} \cdot \frac{5}{3}\right)^{1/2} + 4 = 8.3$	$2\left(\frac{4}{3} \cdot \frac{10}{3}\right)^{1/2} + 5 = 8.5$	$4\left(\frac{5}{3} \cdot \frac{4}{3}\right)^{1/4} + 7 = 11.8$
H=5	$2\left(\frac{8}{3} \cdot 5\right)^{1/2} + 7 = 14.3$	$2\left(\frac{5}{3}\frac{5}{3} \cdot 5\right)^{1/2} + 4 = 12.5$	$2\left(\frac{4}{3} \cdot \frac{10}{3} \cdot 5\right)^{1/2} + 5 = 12.9$	$4\left(\frac{5}{3} \cdot \frac{4}{3} \cdot 5\right)^{1/4} + 7 = 14.3$
H=20	$2\left(\frac{8}{3} \cdot 20\right)^{1/2} + 7 = 21.6$	$2\left(\frac{5}{3}\frac{5}{3} \cdot 20\right)^{1/2} + 4 = 19.9$	$2 \cdot \left(\frac{4}{3} \cdot \frac{10}{3} \cdot 20\right)^{1/2} + 4 = 20.8$	$4\left(\frac{5}{3} \cdot \frac{4}{3} \cdot 20\right)^{1/4} + 7 = 17.3$

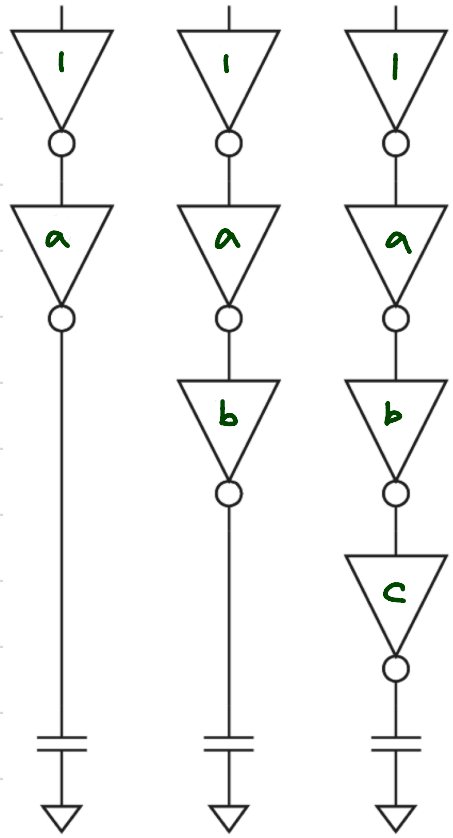
#5.1 $P = \alpha C V^2 f = 0.1\ (450 \times 10^{-12},\ n_0) \cdot 0.9^2 \cdot 450 \times 10^6 = 1.08\,W$

#5.4 10 cycle 동안 2번의 0→VDD transition

∴ 0.2

#5.5 Switch의 개수가 가장 적은 2 Stage 가 가장 적은 energy를 소모

#5.6



- 2stage

  $d = a + 500/a + 2$

  $E = 1 + a$

- 3stage

  $d = a + b/a + 500/b + 3$

  $E = 1 + a + b$

  $a = 5 \quad b = 32.09 \quad E = 38.09$

- 4stage

  $d = a + b/a + c/b + 500/c + 4$

  $E = 1 + a + b + c$

  $a = 2.15 \quad b = 6.23 \quad c = 31.43 \quad E = 39.81$