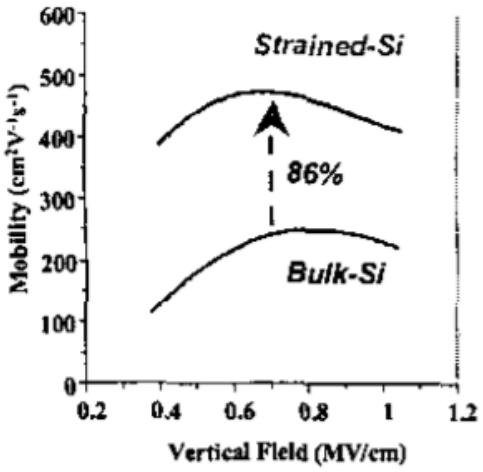
Digital Integrated Circuits HW#4

20175138 임경록

1. Introduction:

Compared to bulk-Si CMOS, 70nm strained-Si CMOS process fabricated on SiGe virtual substrates leads to an improvement in mobility and drive current.

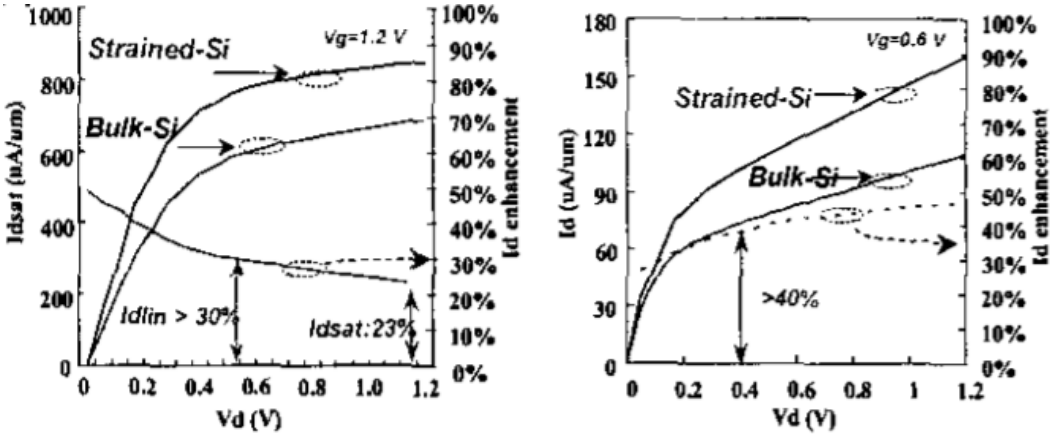
2. Long Channel Devices (strained-Si in 10μm)



[Figure 1] Comparing Mobility value

CMOS devices which has 16×10^{-10}m nitride oxide is fabricated by SiGe. Therefore, the arsenic diffusion is enhanced, so the mobility of CMOS would be enhanced, too. In this graph, the electron mobility of strained-Si increases by 86% compared to bulk Si devices.

3. Short Channel NMOS Devices (W = 0.3 μm, L_{poly} ~ 70 nm)

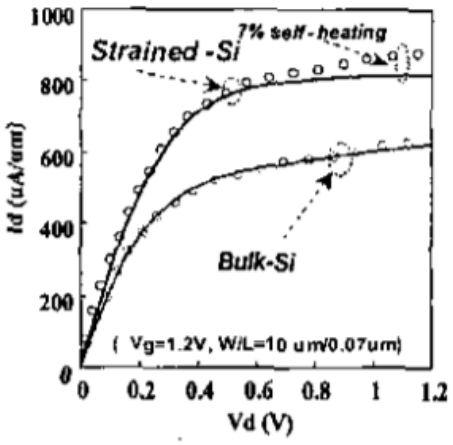


[Figure 2, 3] IV characteristic at $V_g = 1.2V$(left) and at $V_g = 0.6V$(right)

There are three lines in each graphs, Strained-Si current, Bulk-Si current, and drive current enhancement ($=\frac{I_{d,sat}(Strained-Si)- I_{d,sat}(Bulk-Si)}{I_{d,sat}(Bulk-Si)} \times 100(\%)$). In Figure 2, drive current has more than 30% when the drain voltage is lower than 0.6V (linear region). At the saturation region, the drain current enhancement is almost 23%. In Figure 3, the current of Strained-Si and Bulk-Si have a similar tendency as in Figure 2. However, the current value is less than Figure 2 value, because current is proportional to $V_{gs} - V_{th}$ value.

This larger linear current enhancement due to the higher low-field mobility implies a better driving capability during the switching cycle.

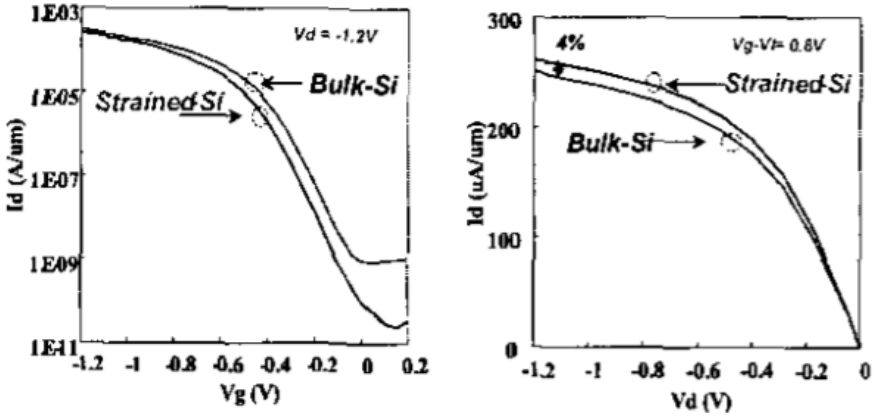
4. Short Channel NMOS Devices (W = 10 μm, L_{poly} ~ 70 nm at 25°C)



[Figure 4] $I_D - V_{DS}$ measurement

DC measurement is indicated as line and pulsed measurement is indicated as circle. During 100ns pulsed measurement, the strained-Si NMOS $I_{dn,sat}$ increases 7% due to reduced self-heating.

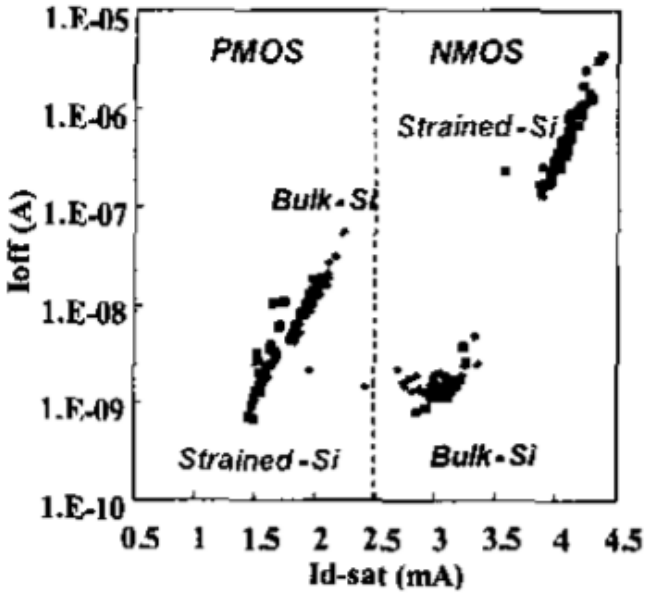
5. Short Channel PMOS Devices (W = 0.3 μm, L_{poly} ~ 75 nm)



[Figure 5, 6] $I_d - V_g$ characteristics (left), $I_d - V_d$ characteristics (right)

In Figure 5, since the hole mobility enhancement of strained-Si on SiGe is small, the PMOS drive current is comparable to that of bulk-Si. In Figure 6, the strained-Si PMOS 4% larger than the bulk-Si PMOS in the saturation region.

6. Current Characteristics of the Inverter NMOS and PMOS Component Devices (L_{poly} ~ 70 nm)



[Figure 7] Current characteristics of the inverter

$I_{dn,sat}$ is 30% higher and $I_{dp,sat}$ is 20% lower for strained-Si compared to bulk-Si.

7. Reference

J. R. Hwang *et al.*, "Performance of 70 nm strained-silicon CMOS devices," *2003 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.03CH37407)*, Kyoto, Japan, 2003, pp. 103-104.

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