DIC L23: Interconnect (1)

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GIST Lecture on December 3, 2019

5.3. Static power (6)

- Example 5.4
  - 50M logic transistors (Average width: 12λ)
    - 5 % low-V_T + 95 % high-V_T
  - 950M memory transistors (Average width: 4λ)
    - 100 % high-V_T
  - 1.0 V 65 nm process (λ is 25 nm.)
  - Subthreshold leakage is 100 nA/μm (low-V_T) or 10 nA/μm (high-V_T).
  - Gate leakage is 5 nA/μm. (Neglect the junction leakage.)
  - Estimate the static power consumption. (Assume that half the transistors contribute leakage currents.)

5.3. Static power (7)

- Power gating
  - Turn off the power supply to the sleeping blocks.
  - “A total of 1.5m of total width per core of ultra-low-leakage PMOS transistors are used with the gate terminal adaptively switched to the highest available chip voltage to further reduce leakage.”

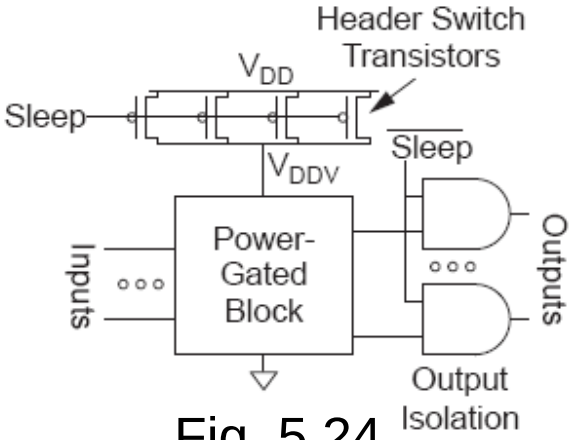
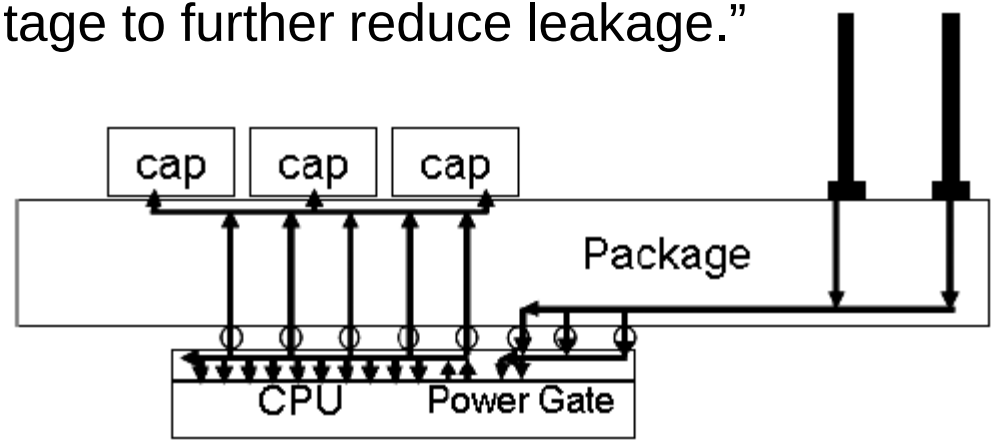


Fig. 5.24



(Kumar et al., ISSCC, 2009)

6.1. Introduction (1)

- Wire geometry
  - Pitch = $w + s$
  - Aspect ratio (AR) = $\frac{t}{w}$
  - Older processes had AR << 1.
  - Modern processes have AR ≈ 2.

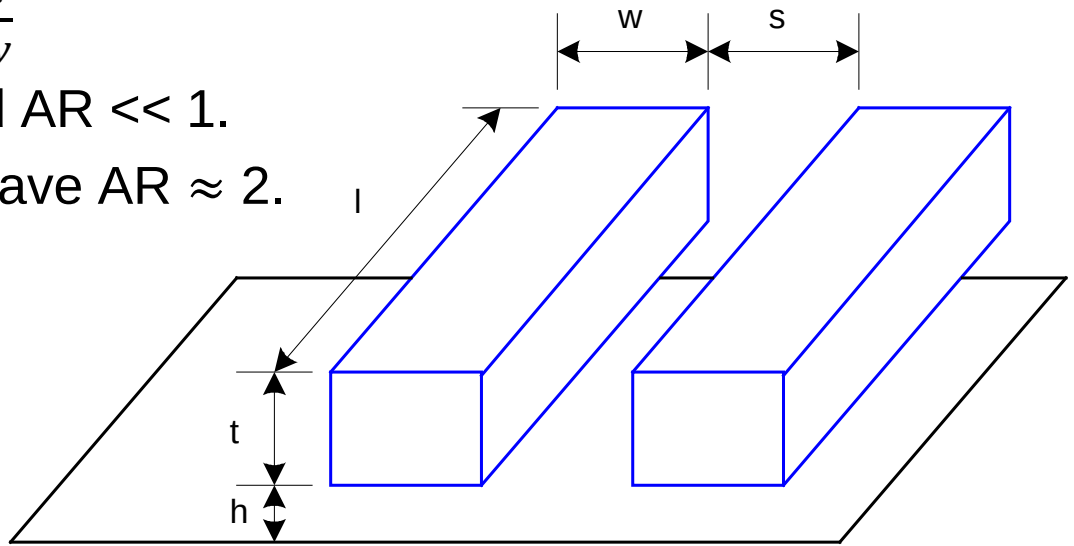


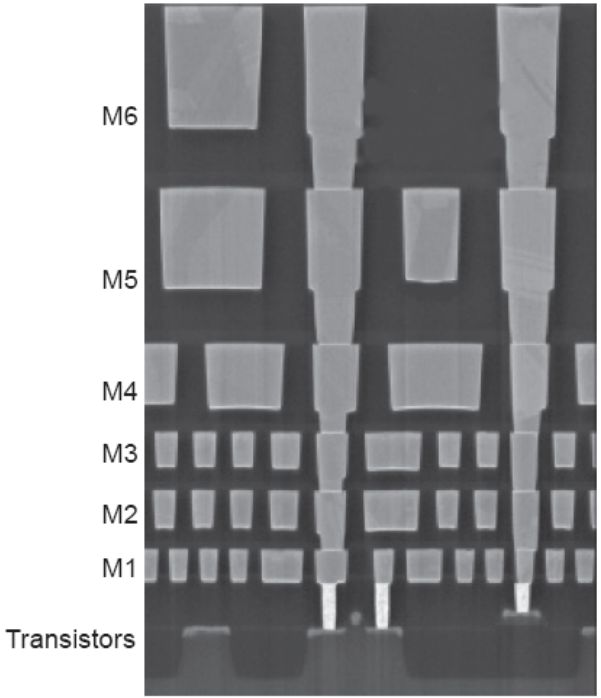
Fig. 6.1

6.1. Introduction (2)

- Example: Intel metal stacks

Layer	Dielectric Material	Pitch (nm)	Thick (nm)	Aspect Ratio
Metal 1	Low k	160	144	1.8
Metal 2	Low k	160	144	1.8
Metal 3	Low k	160	144	1.8
Metal 4	Low k	240	216	1.8
Metal 5	Low k	280	252	1.8
Metal 6	Low k	360	324	1.8
Metal 7	Low k	560	504	1.8
Metal 8	SiO_2	810	720	1.8
Metal 9	Polymer	30.5μm	7μm	0.4

(Equivalent to Table 6.1)



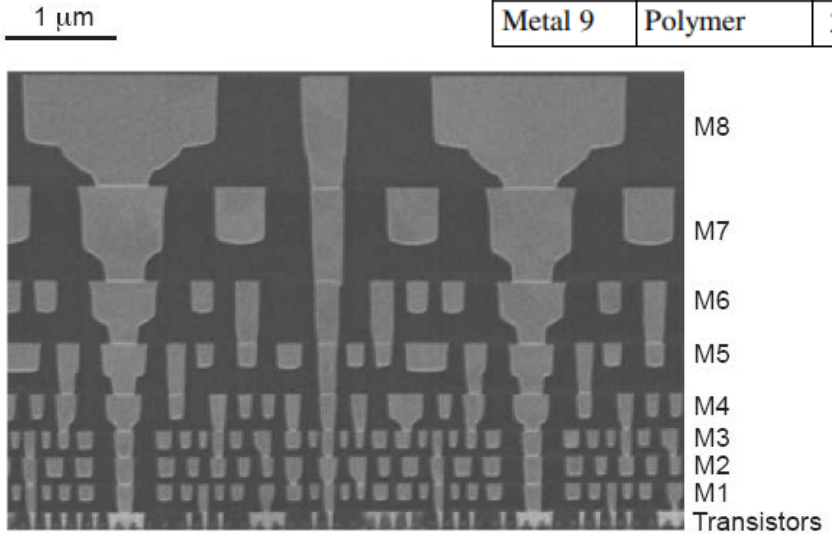


Fig. 6.2

6.2. Interconnect modeling (1)

- Lumped element models
  - A wire is a distributed circuit with a resistance and capacitance per unit length.

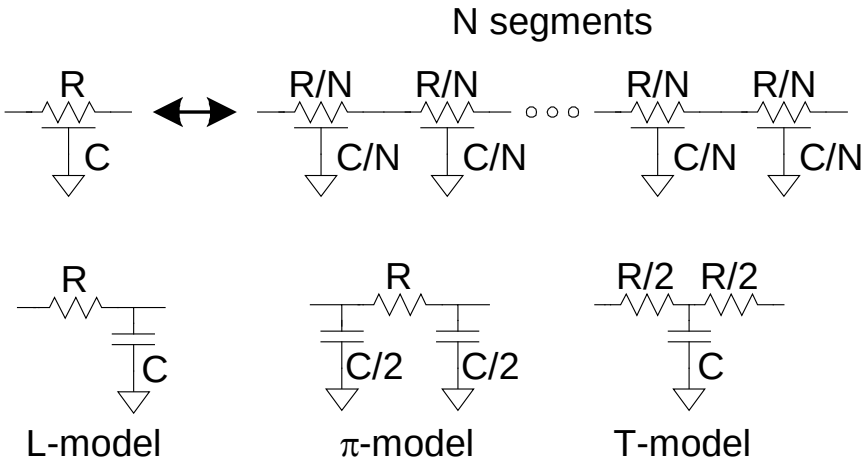


Fig. 6.5

6.2. Interconnect modeling (2)

- Wire resistance
  - Resistance

$$R = \frac{\rho}{t}\frac{l}{w} \qquad \text{Eq. (6.1)}$$

  - With the sheet resistance

$$R = R_{\square}\frac{l}{w} \qquad \text{Eq. (6.2)}$$

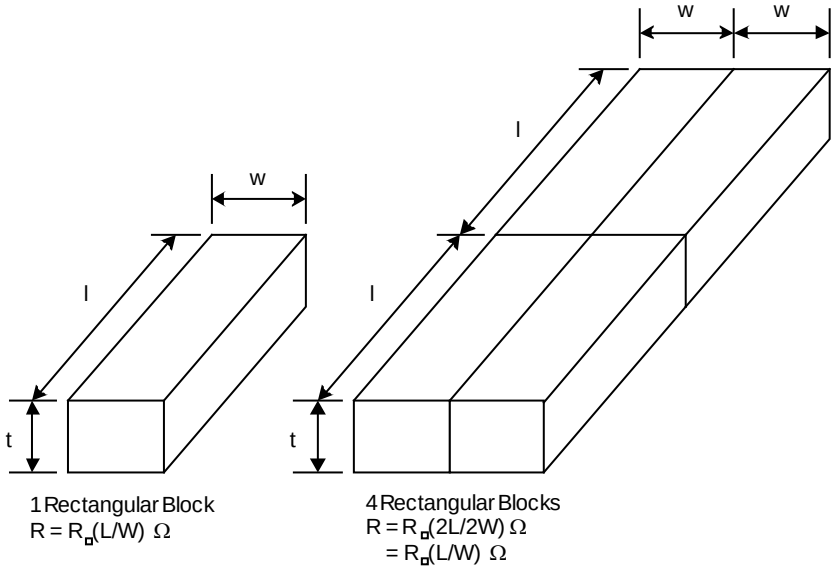


Fig. 6.6

6.2. Interconnect modeling (3)

- Wire resistance
  - Resistance

$$R = \frac{\rho}{t}\frac{l}{w}$$

  - With the sheet resistance

$$R = R_{\square}\frac{l}{w}$$

- Example 6.1
  - Sheet resistance of $0.1\ \Omega/_{\square}$
  - 0.125 μm wide and 1 mm long

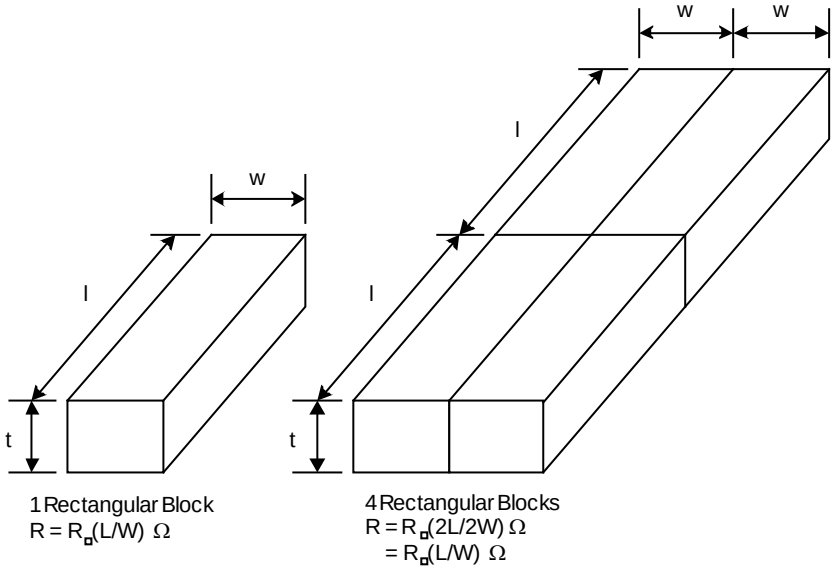


Fig. 6.6

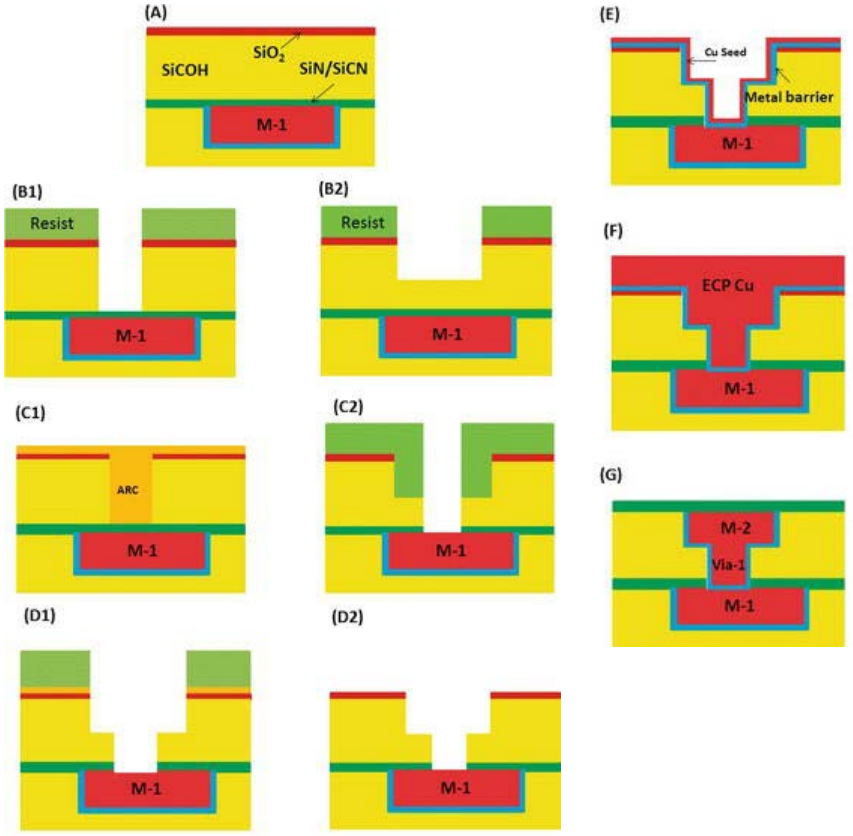
6.2. Interconnet modeling (4)

- Al versus Cu
  - Dual damascene process

Metal	Bulk resistivity (μΩ • cm)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Titanium (Ti)	43.0

Table 6.2

(Cheng et al., “Copper metal for semiconductor interconnects”)



6.2. Interconnect modeling (5)

- Wire capacitance

$$C_{total} = C_{top} + C_{bot} + 2C_{adj} \qquad \text{Eq. (6.9)}$$

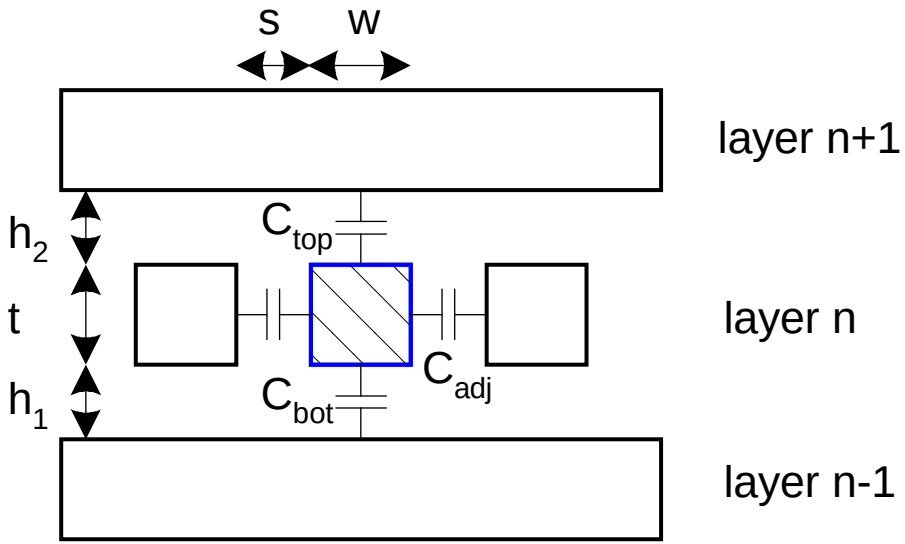


Fig. 6.11