DIC L16: Delay (4)

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4.3. RC delay model (4)

- Example 4.2

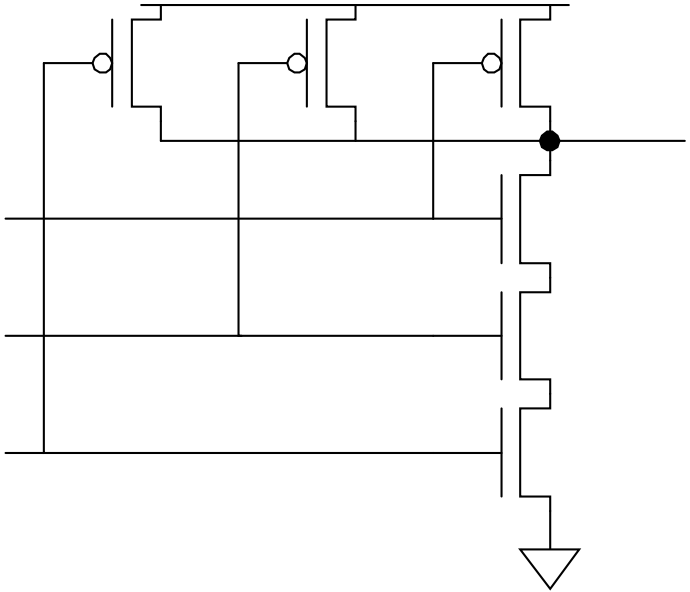


Fig. 4.7(b)

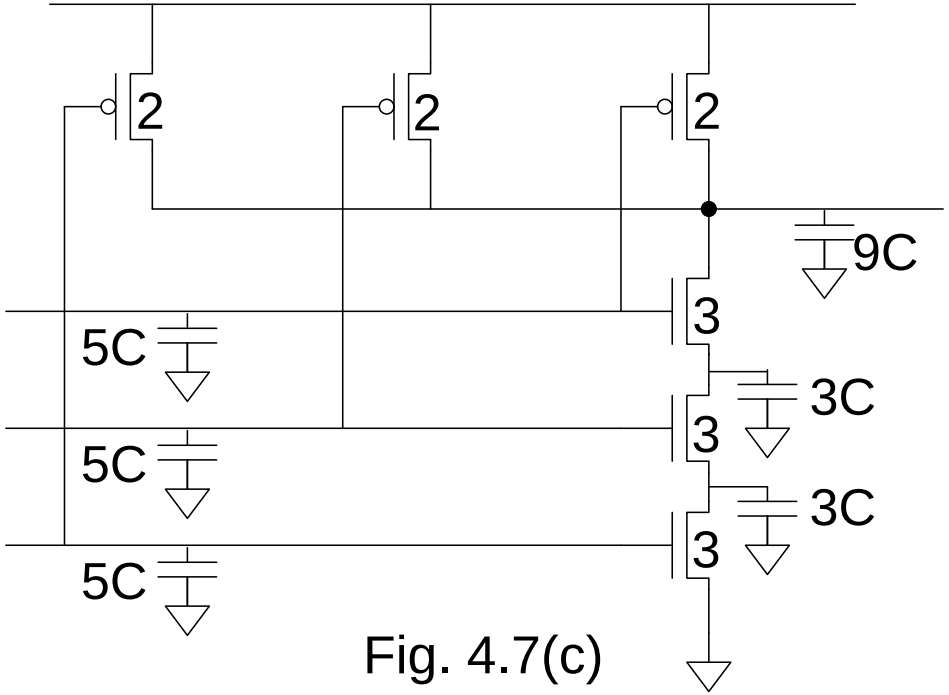


Fig. 4.7(c)

4.3. RC delay model (5)

- First-order RC circuit
  - Its output voltage follows

$$V_{out}(t) = V_{DD} \exp\left(-\frac{t}{RC}\right) \qquad \text{Eq. (4.7)}$$

  - Then, the propagation delay becomes

$$t_{pd} = RC \ln 2 \qquad \text{Eq. (4.8)}$$

- Second-order RC circuit

$$V_{out}(t) = V_{DD} \frac{\tau_1 e^{-t/\tau_1} - \tau_2 e^{-t/\tau_2}}{\tau_1 - \tau_2} \qquad \text{Eq. (4.11)}$$

- How about general RC tree circuits?

4.3. RC delay model (6)

- Example 4.4
  - Estimate for a “unit” inverter (PMOS width:NMOS width=2:1 & minimum length) driving *m* identical “unit” inverters.
  - Effective R (same for NMOS and PMOS)
  - Capacitance is (3+3*m*)C.

$$t_{pd} = (3 + 3m)RC$$

- Example 4.5
  - When the driver is *w* times unit size,

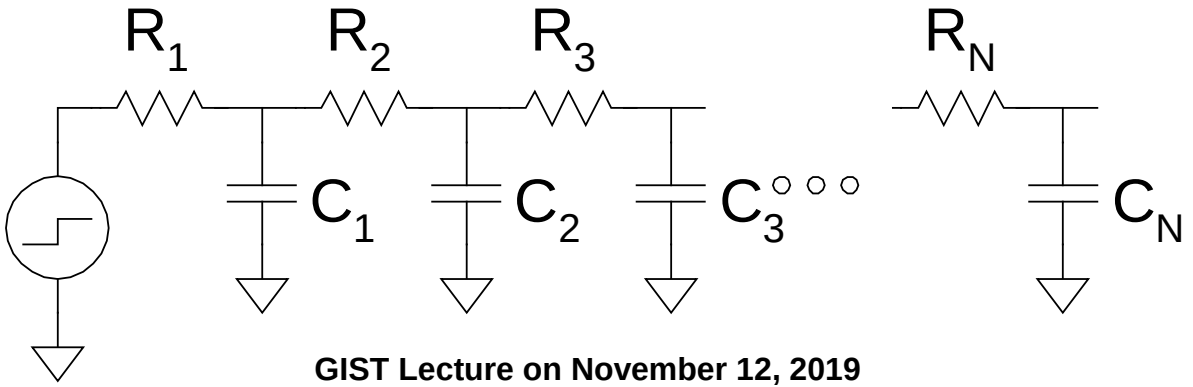
$$t_{pd} = \left(3 + 3\frac{m}{w}\right)RC$$

4.3. RC delay model (7)

- Example 4.4
  - A simple single time constant approximation

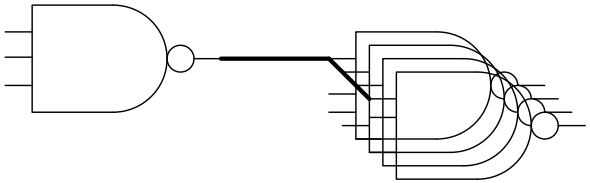
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i \qquad \text{Eq. (4.14)}$$

$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$

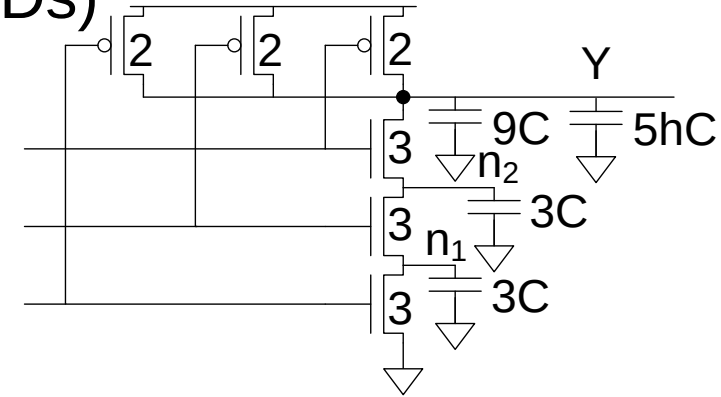


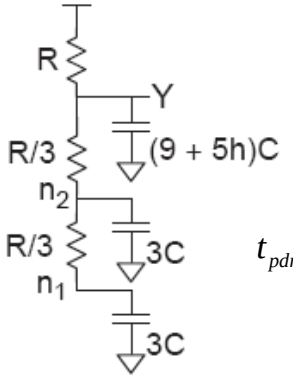
4.3. RC delay model (8)

- Example 4.7 (*h* identical NANDs)

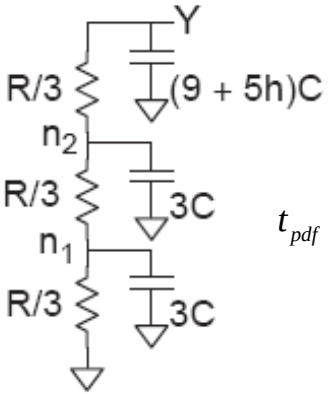


h copies





$$t_{pdr} = (9+5h)RC$$



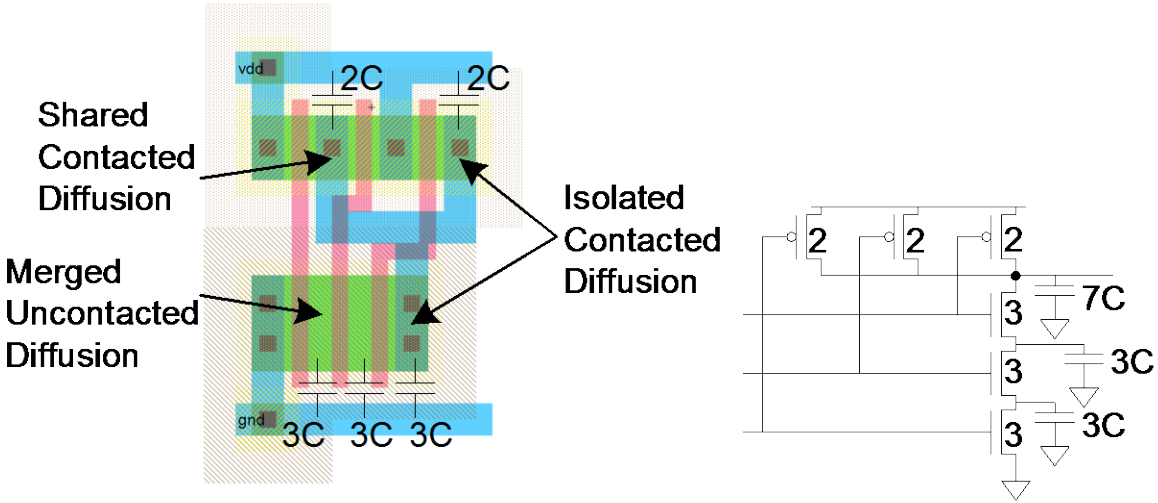
$$t_{pdf} = (3C)\left(\tfrac{R}{3}\right) + (3C)\left(\tfrac{R}{3}+\tfrac{R}{3}\right) + \left[(9+5h)C\right]\left(\tfrac{R}{3}+\tfrac{R}{3}+\tfrac{R}{3}\right)$$
$$= (12+5h)RC$$

4.3. RC delay model (9)

- Delay components
  - Parasitic delay
    - 9 or 12 RC
    - Independent on load
  - Effort delay
    - 5*h* RC
    - Proportional to load capacitance

4.3. RC delay model (9)

- Layout dependence of capacitance
  - Good layout minimizes the diffusion area.



4.4. Linear delay model (1)

- Delay in a logic gate
  - Express delays in process-independent unit

$$d = \frac{t_{pd}}{\tau} = \frac{t_{pd}}{3RC} \qquad \text{Eq. (4.15)}$$

  - Delay has two components:

$$d = f + p \qquad \text{Eq. (4.20)}$$

  - Effort delay

$$f = gh \qquad \text{Eq. (4.21)}$$

  - Logical effort, g
    - $g \equiv 1$ for inverter

4.4. Linear delay model (2)

- Delay in a logic gate (continued)
  - Electrical effort

$$h = \frac{C_{out}}{C_{in}} \qquad \text{Eq. (4.22)}$$

    - Ratio of output to input capacitance
  - Parasitic delay, p
    - Represents delay of gate driving no load
    - Set by internal parasitic capacitance

4.4. Linear delay model (3)

- Normalized delay versus fanout