GIST EECS

HW#5

Digital Integrated Circuit 2019 Fall

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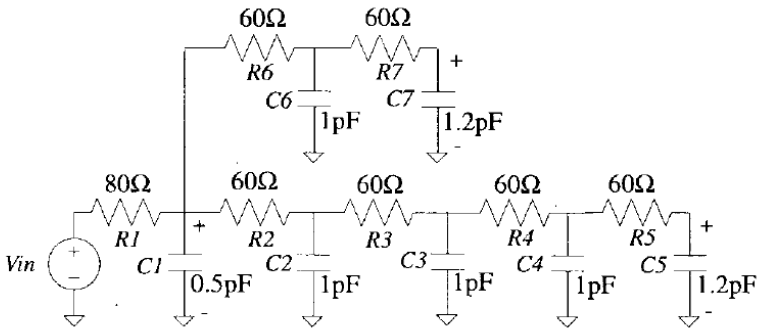
- Research Paper Title : The Elmore Delay as a Bound for RC Trees with Generalized Input Signals
- Writers & Researcher : Rohini Gupta, Bogdan Tutuianu, Lawrence T.Pileggi
- Published Journal : IEEE Transactions on Computer Computer-Aided Design of Integrated Circuits and Systems, Vol 16, No1, January 1997

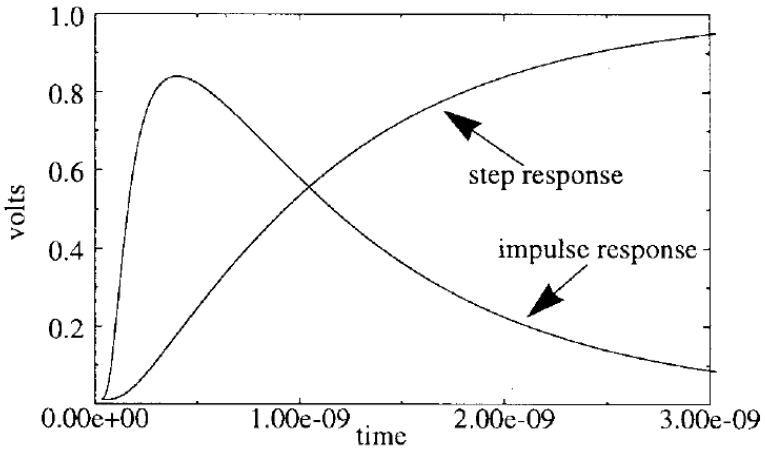
RC trees is commonly used to model digital logic gates and their associated interconnect paths at various stage of the design process. This paper proves that Elmore delay value possesses an absolute upper bound on the 50% delay of an RC tree. This is proved according to few steps. First, they prove that RC tree impulse response distributions are guaranteed to be unimodal and positively skewed. Second, they show that the mean of such a distribution will always exceed the median by using the classical theory of distribution functions. In addition, they specify a lower bound on the 50% delay by calculating the mean and the variance of the impulse response.

Fig.1 is common simple RC tree with resistor (R) and capacitor (C). Two different responses – unit step and unit impulse response – at 'C5' from this tree can be seen in Fig.2. Elmore delay is a metric for RC tree delay which is easily and efficiently calculated with following equation. *i* represents output node, N represents number of node in the tree, and *k* indicates certain node. Table I indicates various delay factors on different node in RC tree.

$$T_{D_i} = \sum_{k=1}^{N} R_{ki} C_k$$



<Fig. 1. Simple RC tree>

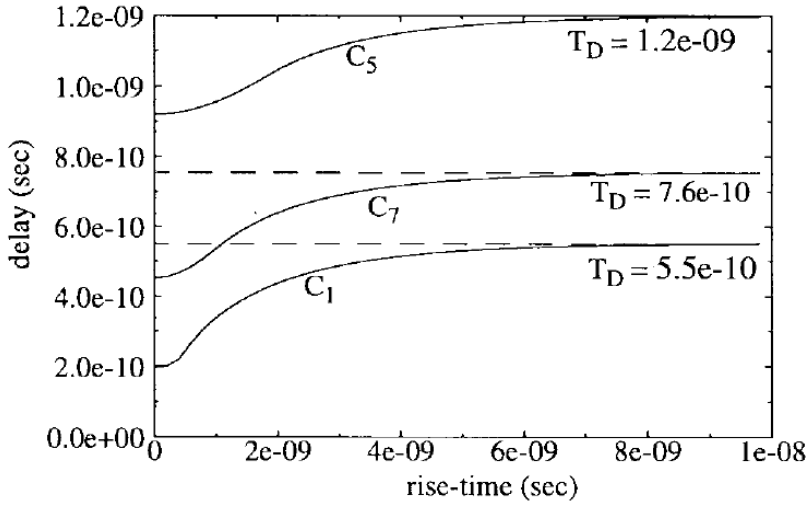


<Fig.2. The unit step and the unit impulse response (scaled by 1e+09) for the voltage across C5 in Fig.1>

TABLE I
DELAY BOUNDS FOR CIRCUIT IN FIG. 1

(1)	(2)	(3)	(4)	(5)	(6)	(7)
Node	**Actual delay**	**Elmore delay, T_D**	**Lower bound, $T_D - \sigma$**	**Single pole approx. $T_D \cdot \ln(2)$**	**PRH upper bound, t_{max}**	**PRH lower bound, t_{min}**
C1	0.196 ns	0.55 ns	0 ns	0.383 ns	0.55 ns	0 ns
C5	0.919 ns	1.2 ns	0.2 ns	0.83 ns	1.32 ns	0.51 ns
C7	0.45 ns	0.75 ns	0 ns	0.524 ns	1.02 ns	0.054 ns

In this research paper, the author asserts that there is a certain upper bound for Elmore delay. It is proven with Laplace transfer function and the fact that Mean is always bigger or equal to Median, and the Median is always equal or bigger than Mode. According to Fig.3, delays on different output node in RC tree has different maximum limitation on delay. The delay approaches to a certain delay time constant called "TD." This is proved with Laplace transform in the beginning, which indicates that the dominant pole (time constant) implies dominant time constant approximation. This results an exponential voltage curve. In addition to the dominant time constant, the author uses an equation "Mode≤ Median ≤ Mean", which is proved via classical theory of distribution. When the mean on the dominant time constant calculated, it automatically implies that mode and median of delay time constant will have an upper bound of mean value as delay limitation.

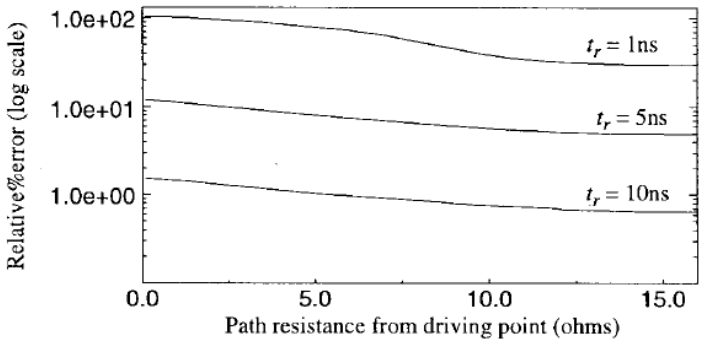


<Fig.3. Delay curves show that as the rise time of the input signal increases, the delay approaches Td>

In the end, the author concludes the assertion with delays and relative error at three different nodes in RC tree as in Fig.4.

TABLE II
DELAYS AND RELATIVE ERROR AT NODES A, B, C ALONG A SIGNAL PATH

Node	Elmore delay	Rise-time = 1ns		Rise-time = 5ns		Rise-time =10ns	
		Delay	% Error	Delay	% Error	Delay	% Error
A	0.02 ns	0.01 ns	104%	18.0 ps	11.9%	19.0 ps	1.54%
B	1.13 ns	0.72 ns	54.7%	1.06 ns	6.5%	1.116 ns	0.86%
C	1.56 ns	1.2 ns	29.6%	1.48 ns	4.8%	1.547 ns	0.64%



<Fig.4 Relative error (Delay-TD)/Delay as function of path resistance from driving point (i.e., distance from driving point).