DIC L19: Delay (7)
DIC L20: Power (1)

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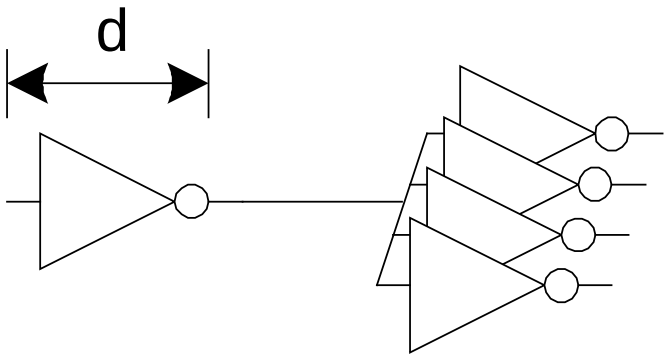
4.4. Linear delay model (7)

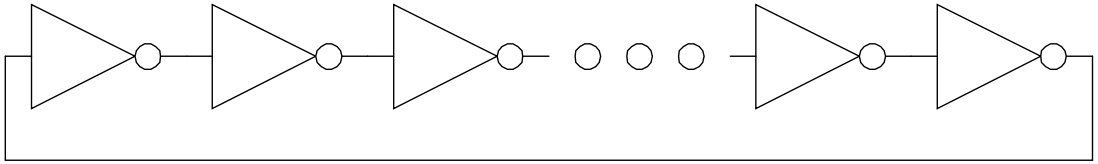
- Example 4.10



  - Logical Effort: g = 1
  - Electrical Effort: h = 4
  - Parasitic Delay: p = 1
  - Stage Delay: d = 5
  - When $\tau = 3RC = 3$ ps, the total delay is 15 ps.

4.4. Linear delay model (8)

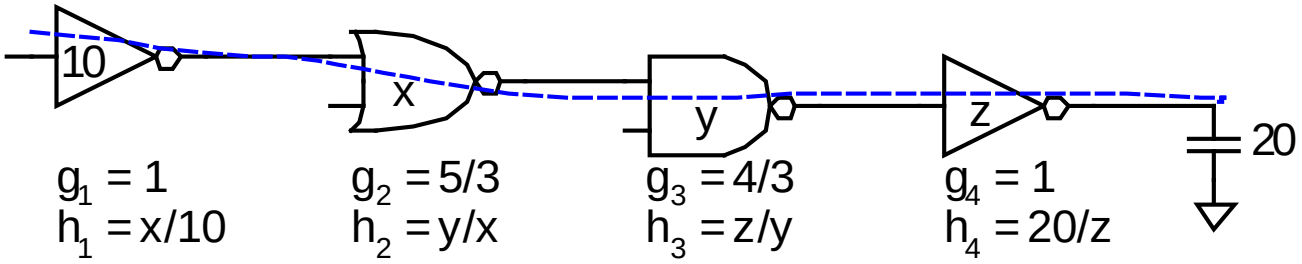
- Example 4.11



  - Logical Effort: g = 1
  - Electrical Effort: h = 1
  - Parasitic Delay: p = 1
  - Stage Delay: d = 2
  - Frequency: $f_{osc} = 1/(2*N*d) = 1/4N$

4.5. Logical effort of paths (1)

- Multistage logic networks
  - Logical effort is independent of size.
  - Electrical effort depends on sizes.



  - Some metrics for the path as a whole?

4.5. Logical effort of paths (2)

- Multistage logic networks
  - Logical effort is independent of size.
  - Electrical effort depends on sizes.
- Path logical effort $$G = \prod g_i$$ Eq. (4.32)
- Path electrical effort $$H = \frac{C_{out-path}}{C_{in-path}}$$ Eq. (4.33)
- Path effort $$F = \prod f_i = \prod g_i h_i$$ Eq. (4.34)

4.5. Logical effort of paths (3)

- With the branching effort, B,

$$F = GBH$$ Eq. (4.37)

- Path effort delay $D_F = \sum f_i$
- Path parastic delay $P = \sum p_i$ Eq. (4.38)
- Path delay $D = \sum d_i = D_F + P$

4.5. Logical effort of paths (4)

- Paths that branch

  G = 1

  H = 90 / 5 = 18

  GH = 18

  h_1 = (15 +15) / 5 = 6

  h_2 = 90 / 15 = 6

  F = $g_1g_2h_1h_2$ = 36 = 2GH

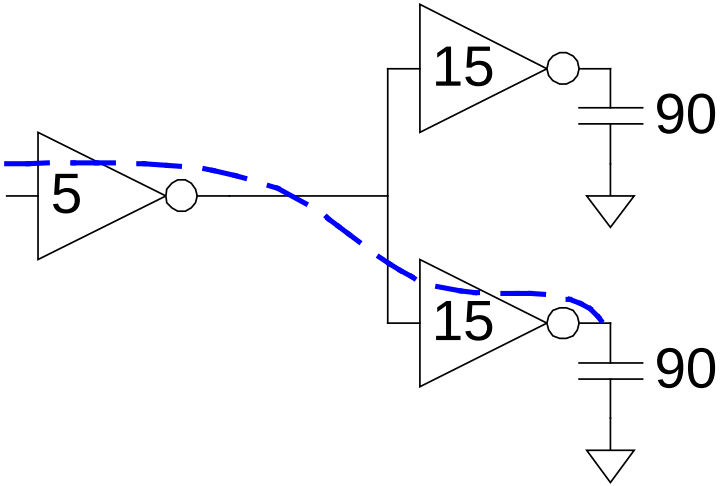


Fig. 4.30

- It's not difficult to evaluate F.
  - Even without specific sizes, we can do it!
  - It means that F is fixed.

4.5. Logical effort of paths (5)

- Important observation
  - We want to make D_F (a sum of f_i's) small.
  - But, F (a product of f_i's) is fixed.
- Assume N stages.
- Inequality of arithmetic and geometric means

$$f_1 + f_2 + \cdots + f_N \geq N \sqrt[N]{f_1 f_2 \cdots f_N}$$

  - The equality holds if and only if $f_1 = f_2 = \cdots = f_N$.
  - Therefore, the minimum value of D_F is given by

$$D_F = N \sqrt[N]{F}$$

4.5. Logical effort of paths (6)

- The minimum delay

$$D = NF^{1/N} + P \qquad \text{Eq. (4.40)}$$

  - This is a key result of logical effort.
  - It shows that:
    - The minimum delay of the path can be estimated knowing only the number of stages (N), path effort ($F = GBH$), and parasitic delays (P) without the need to assign transistor sizes.
- When the stage effort is given as $\hat{f} = F^{1/N}$,
  - The transistor size can be determined to satisfy $\hat{f} = gh = g\frac{C_{out}}{C_{in}}$.
  - Working backward!

4.5. Logical effort of paths (7)

- Example 4.13

$$G = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} = \frac{100}{27}$$

$$B = 3 \times 2 = 6$$

$$H = \frac{45}{8}$$

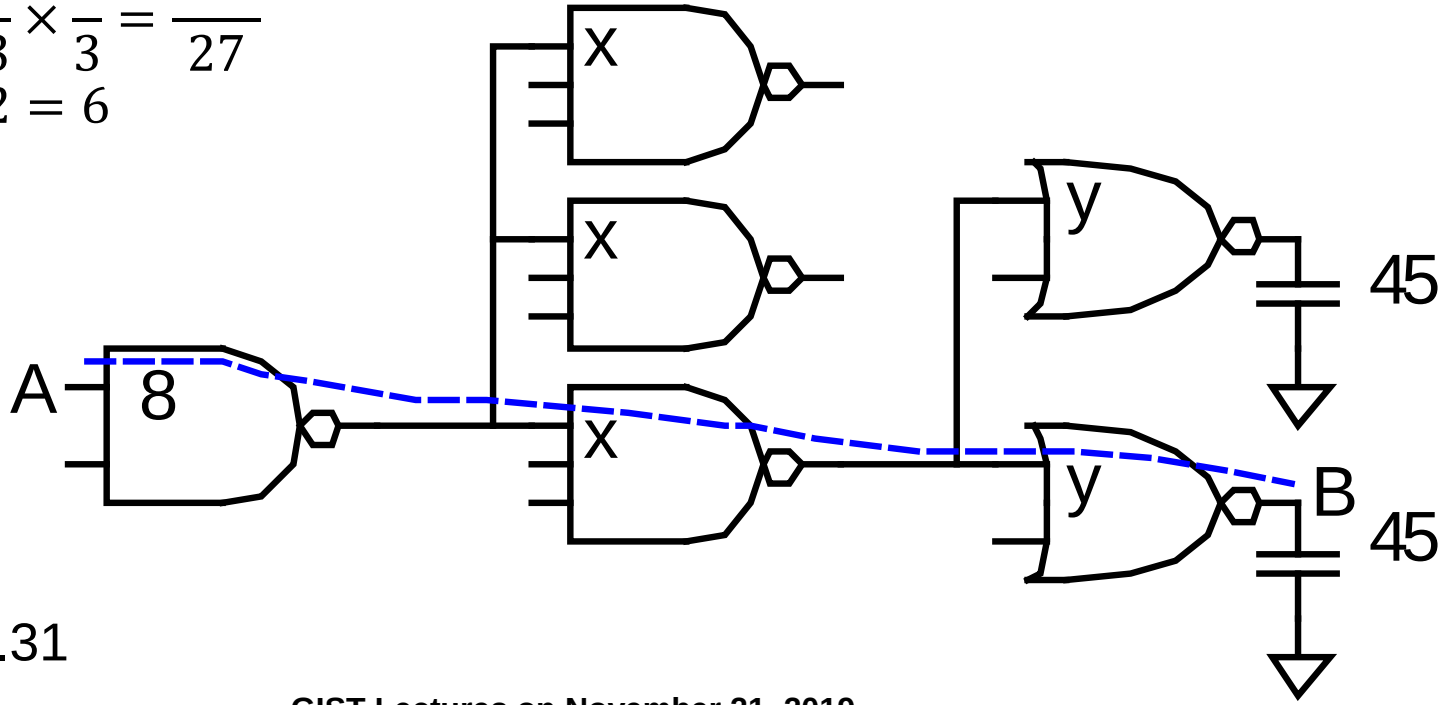


Fig. 4.31

4.5. Logical effort of paths (8)

- Example 4.14

$$D = N(64)^{1/N} + N$$

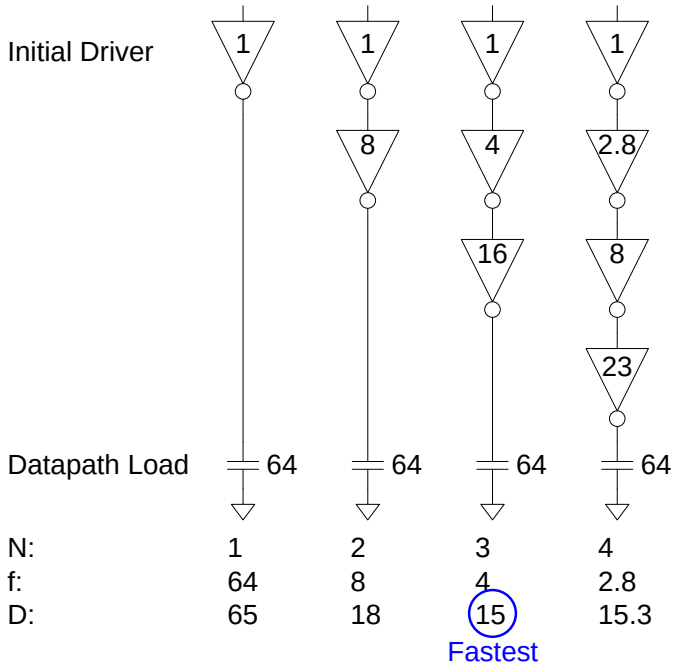


Fig. 4.33

5.1. Introduction (1)

- Definitions
  - Instanteneous power

$$P(t) = I(t)V(t) \qquad \text{Eq. (5.1)}$$

  - Energy

$$E = \int_0^T P(t)dt \qquad \text{Eq. (5.2)}$$

  - Average power

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt \qquad \text{Eq. (5.3)}$$

5.1. Introduction (2)

- Charging a capacitor
  - Energy stored in the capacitor

$$\int_0^\infty I(t)V_{out}(t)dt = \frac{1}{2}C_L V_{DD}^2$$

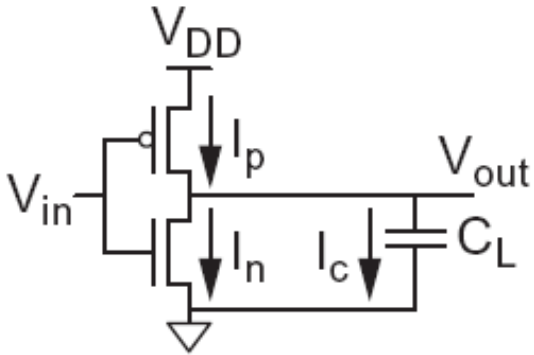


Fig. 5.4

  - The energy delivered from the power supply

$$\int_0^\infty I(t)V_{DD}dt = C_L V_{DD}^2$$

  - Half of the energy from V_{DD} is dissipated in the PMOS transistor as heat.

5.1. Introduction (3)

- Switching waveforms

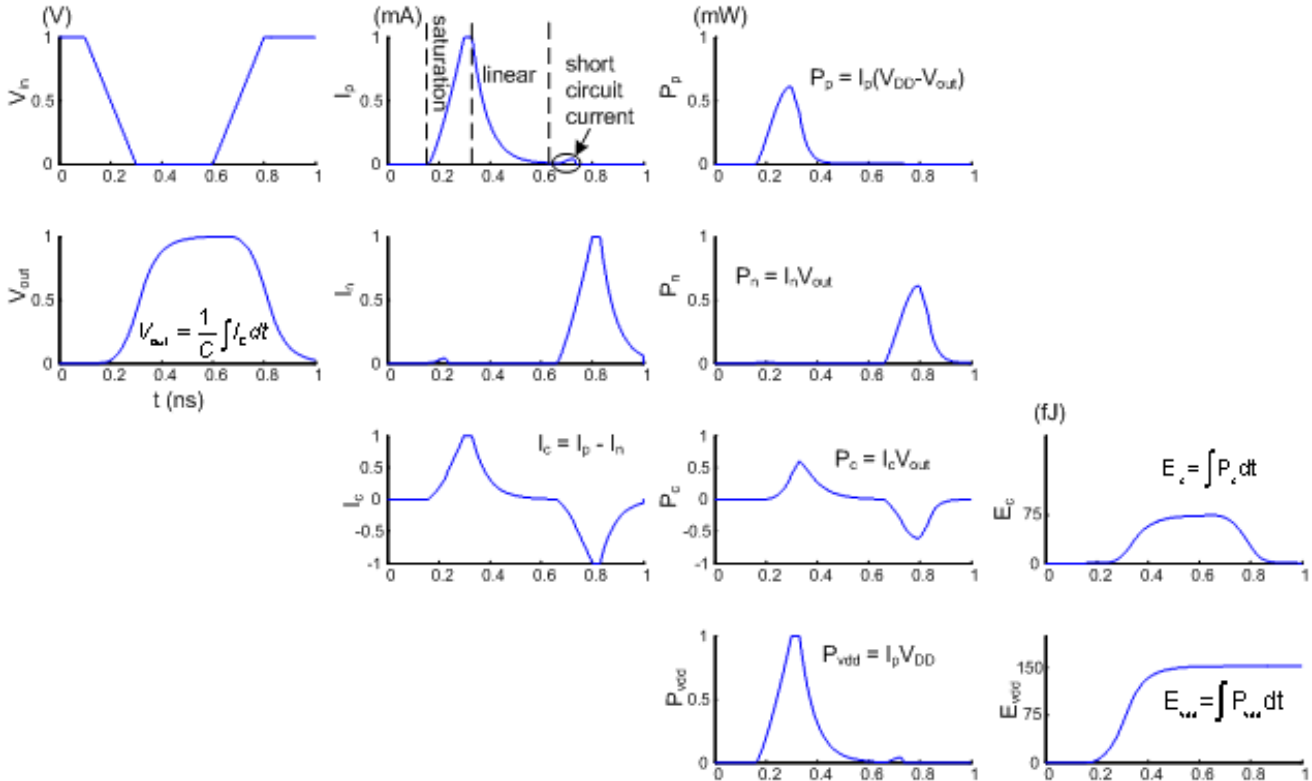


Fig. 5.5

5.1. Introduction (4)

- Average power dissipation
  - When a gate is

$$P_{switching} = \frac{CV_{DD}^2}{T} = CV_{DD}^2 f_{sw}$$

- Most gates do not switch every clock cycle.
  - Let $f_{sw} = \alpha f$, where α is the activity factor.
  - Then, the dynamic power is written as

$$P_{switching} = \alpha CV_{DD}^2 f$$