GIST EECS

HW#4 – CMOS TECH.

[EC4202-01] Digital Integrated Circuit

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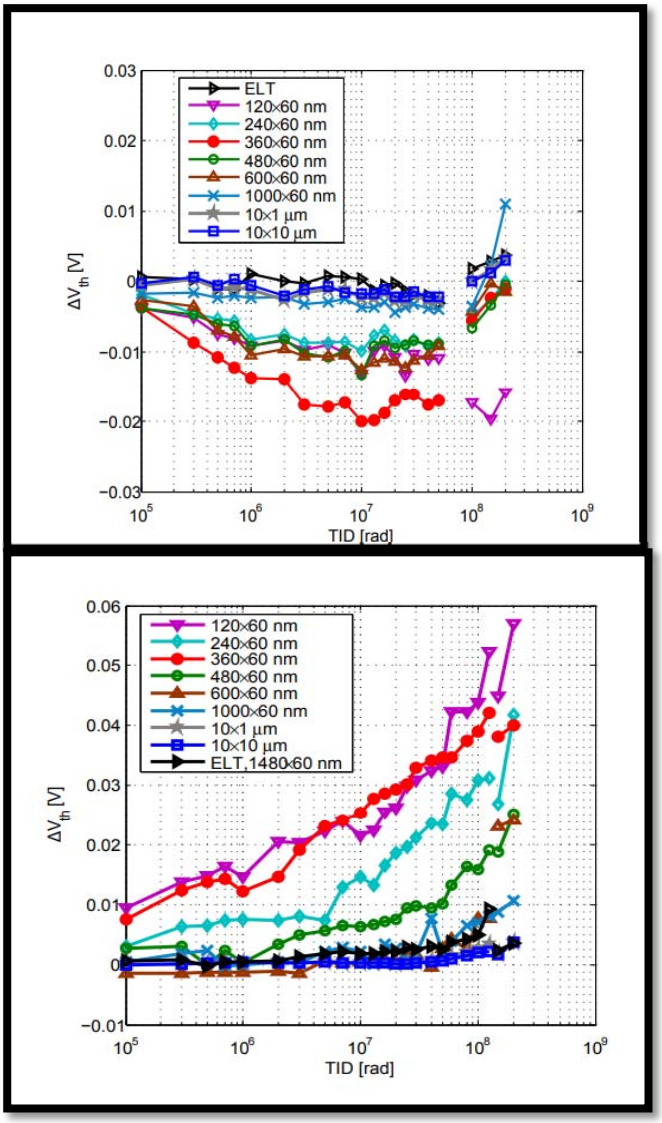
- **CMOS Technology** : CMOS 65nm
- **Date of publish** : Jan. 18. 2012
- Journal of Instrumentation, SISSA, "Characterization of a commercial 65nm CMOS technology for SLHC applications"
- **Reference Source** : https://iopscience.iop.org/article/10.1088/1748-0221/7/01/P01015/pdf

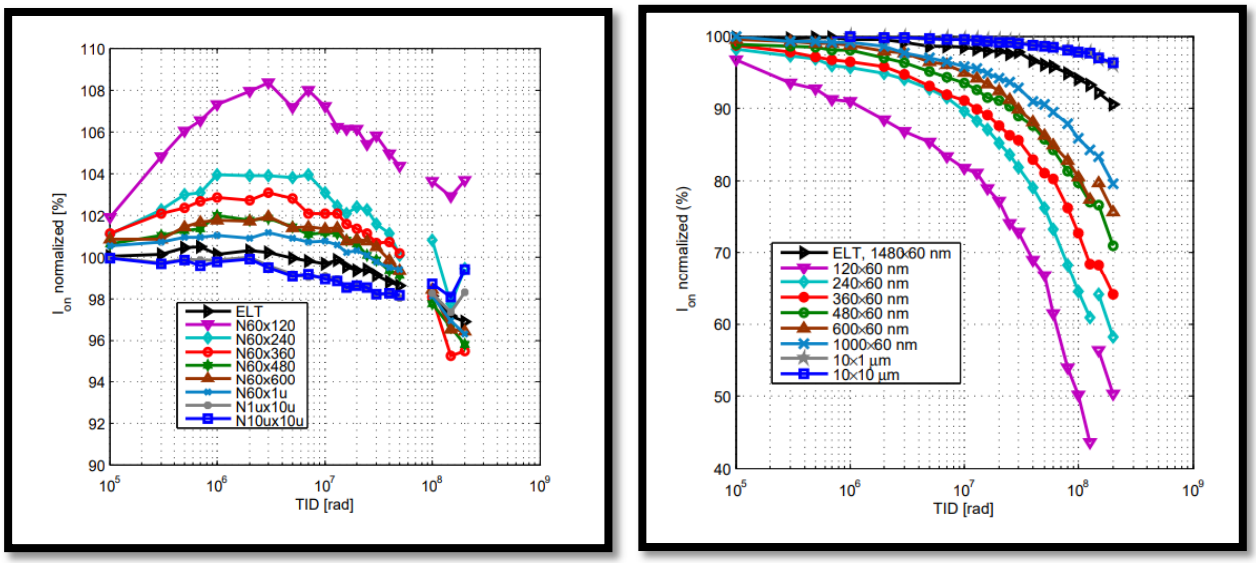
(1) Threshold Voltage variation (NMOS) for different NMOS and PMOS size



➔ The variation of threshold voltage value is inversely proportional to MOSFET size. This is due to mismatch effect. The following equation is used for calculating one standard variation value against current variation. As size gets bigger, the variation value gets lower.

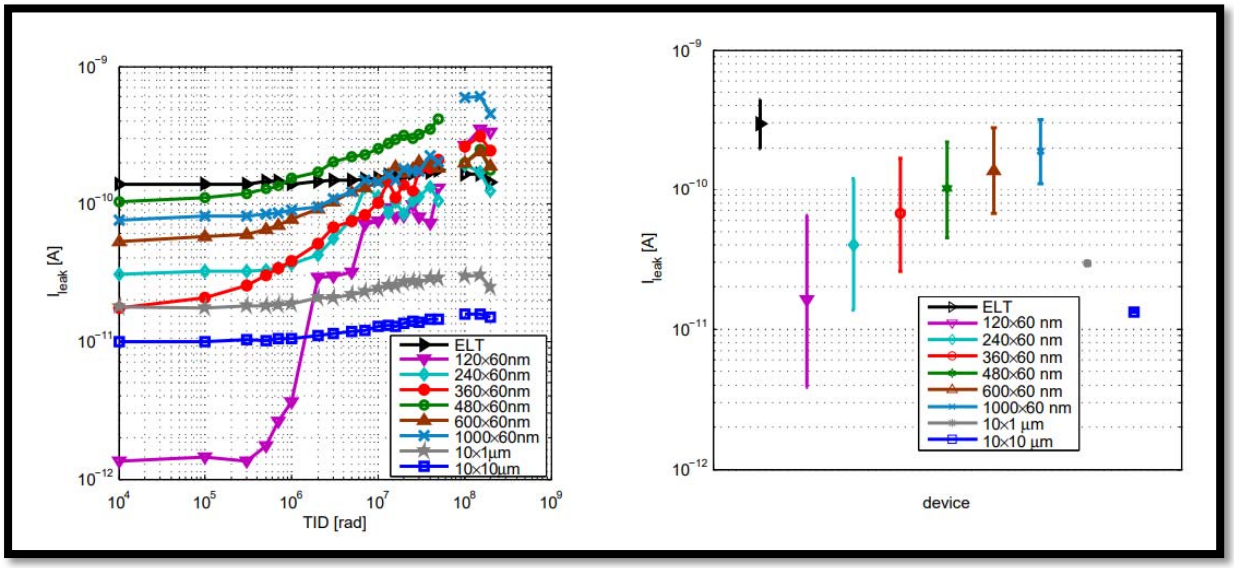
$$\sigma(I) = \frac{2A_{VTH}}{\sqrt{WL}(V_{GS} - V_{TH})}$$

(2) Maximum drive current (Vgs=Vds=1.2V) measured for NMOS and PMOS core devices, normalized to pre-rad



➔ When MOSFET size shrinks,
the maximum drive current varies non-linearly. However, it becomes more linearly degraded when size gets bigger. This is another result due to mismatch effect.

(3) Leakage current and its one sigma standard variation measured with Monte Carlo Simulation for NMOS core devices



➔ The magnitude and the spread of error for leakage current gets bigger as size of MOSFET gets smaller.

(4) Maximum transconductance variation for PMOS core and I/O devices, normalized to pre-rad

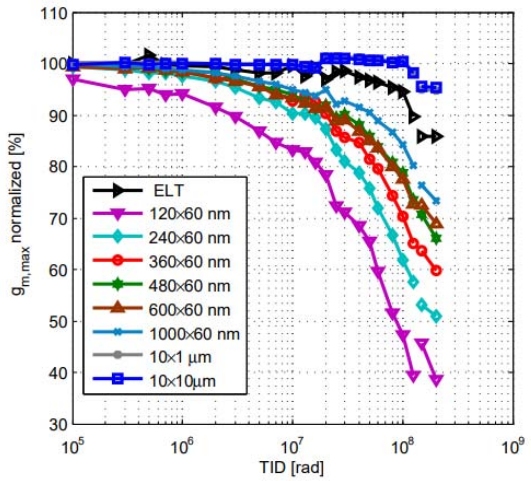


Figure 13. Maximum g_m (strong inversion) for PMOS core devices, normalized to pre-rad.

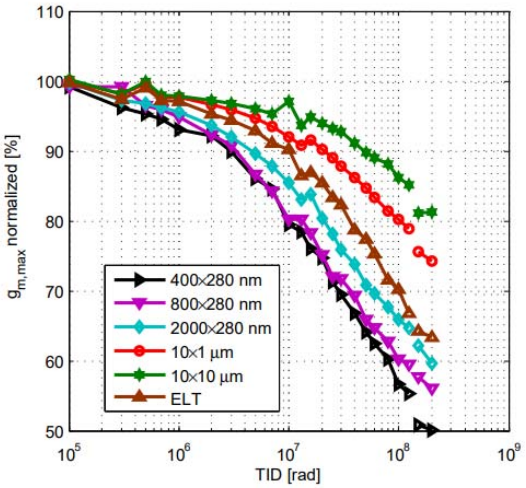


Figure 14. Maximum g_m (strong inversion) for PMOS I/O devices, normalized to pre-rad.

➔ The transcondutance of PMOS devices tend to keep its value when the size of MOSFET is bigger.