DIC L14: Delay (2)

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4.1. Introduction (1)

- Transient response
  - DC analysis: V_{out} if V_{in} is a constant
  - Transisent analysis: $V_{out}(t)$ if $V_{in}(t)$ changes
  - A set of differential equations should be solved.
    - Consider a vector of state variables, $\mathbf{x}$.
    - In many cases,

$$\frac{d}{dt}(\mathbf{C}\,\mathbf{x}) + G(\mathbf{x}) = \mathbf{b}$$

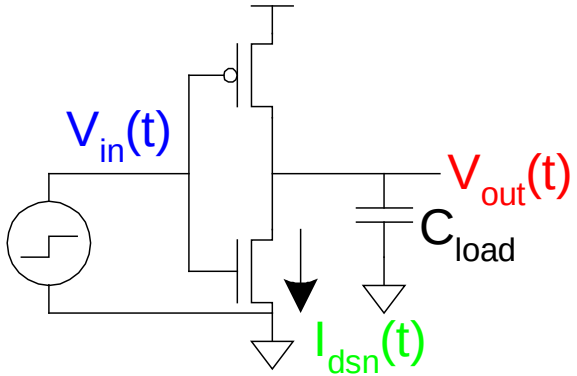
  - Input is usually considered to be a step or ramp.
    - From 0 to V_{DD} or vice versa

4.1. Introduction (2)

$$V_{in}(t) =$$

$$V_{out}(t < t_0) =$$

$$\frac{dV_{out}(t)}{dt} =$$



$$I_{dsn}(t) = \begin{cases} & t \le t_0 \\ V_{out} > V_{DD} - V_t & \\ V_{out} < V_{DD} - V_t & \end{cases}$$

4.1. Introduction (3)

- Definitions
  - **t_{pdr}**: *rising propagation delay*
    - From input to rising output crossing $V_{DD}/2$
  - **t_{pdf}**: *falling propagation delay*
    - From input to falling output crossing $V_{DD}/2$
  - **t_{pd}**: *average propagation delay*, $t_{pd} = (t_{pdr} + t_{pdf})/2$
  - **t_r**: *rise time*
    - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
  - **t_f**: *fall time*
    - From output crossing 0.8 V_{DD} to 0.2 V_{DD}

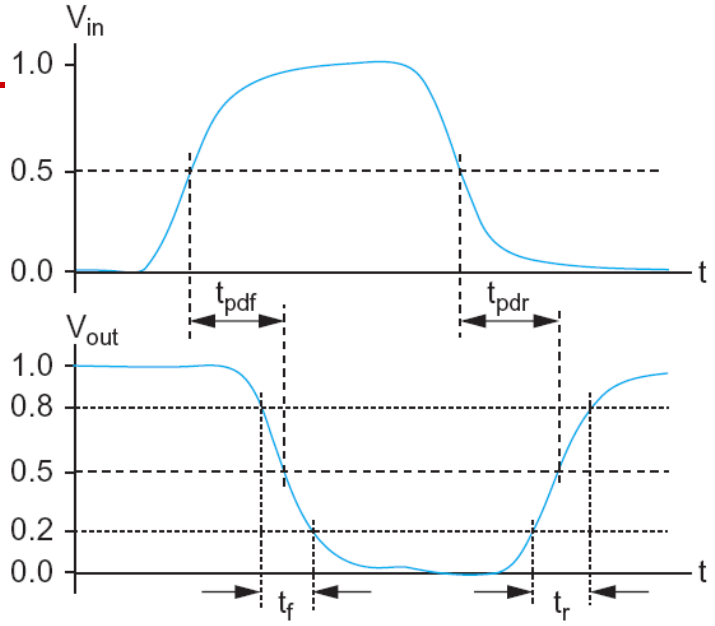
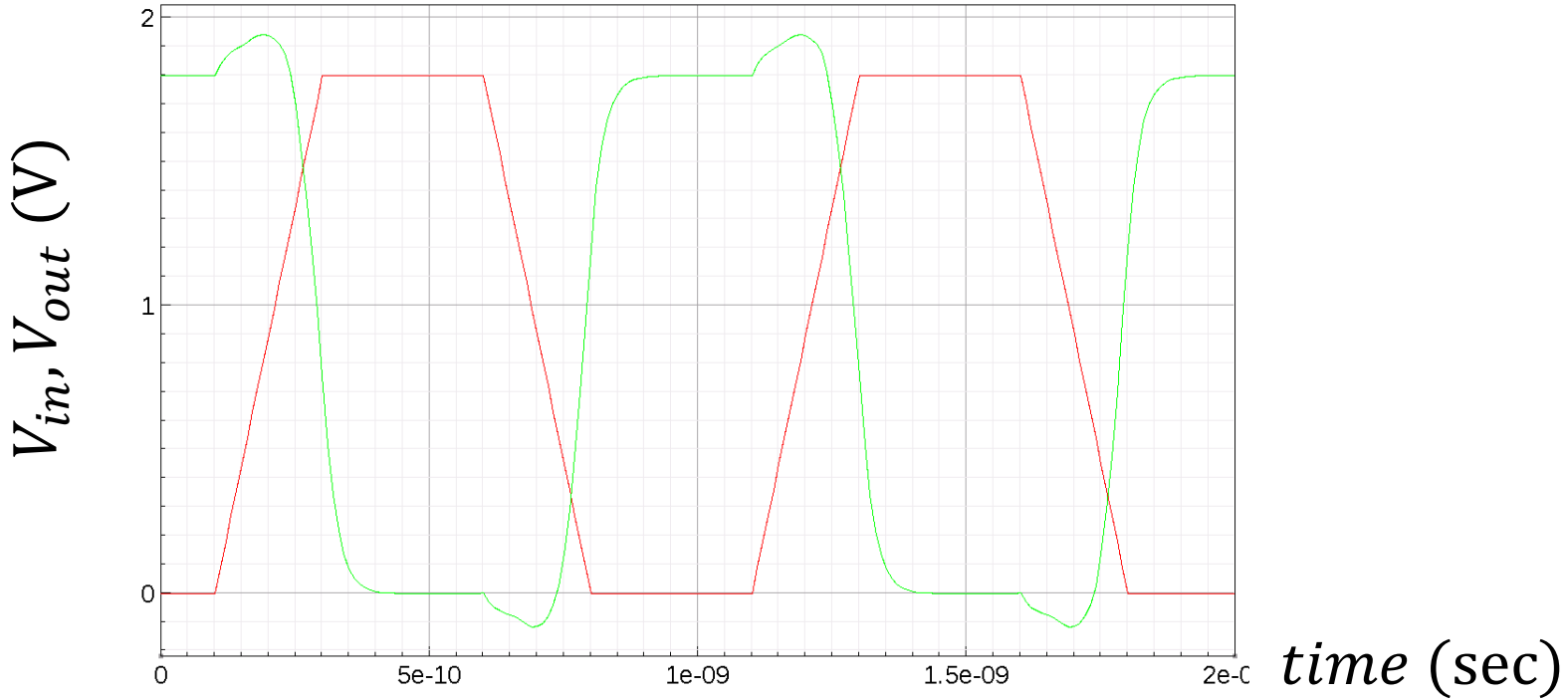


Fig. 4.1

4.1. Introduction (4)

- Inverter example



4.3. RC delay model (1)

- Easily estimate the delay
- RC delay models approximate the nonlinear transistor IV and CV characteristics with an average resistance and capacitance over the switching range of the gate.
  - Total capacitance on output node: C
  - Effective resistance: R
  - Propagation delay ~ RC
- Characterize transistors by finding their effective R values.
  - Not accurate, however good enough to predict RC delay

4.3. RC delay model (2)

- Equivalent RC circuits
  - Unit NMOS (for example, $4\lambda/2\lambda$) is defined to have effective resistance R. An NMOS, whose width is k times unit width, has resistance R/k.
  - Let us assume that unit PMOS has effective resistance 2R.

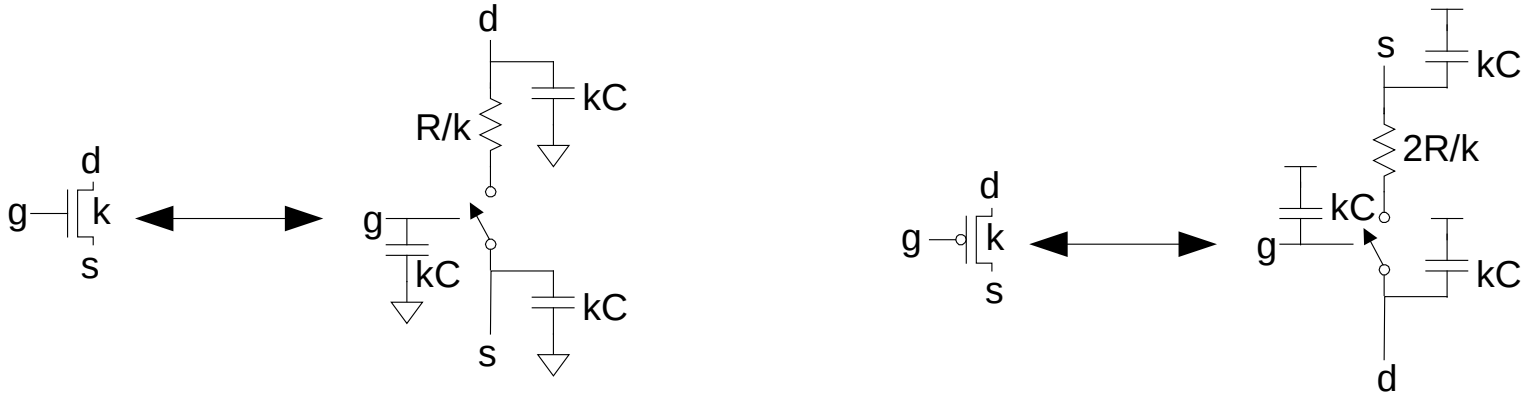


Fig. 4.5