DIC L17: Delay (5)

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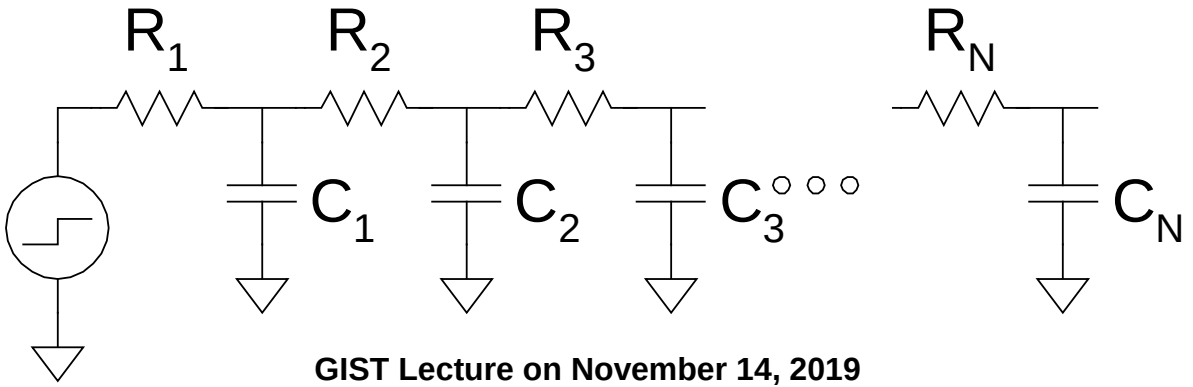
4.3. RC delay model (7)

- Example 4.4
  - A simple single time constant approximation

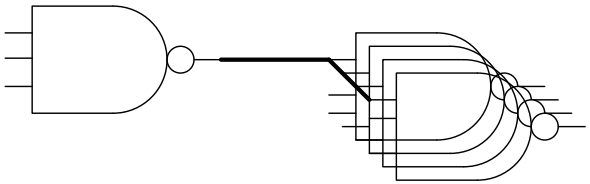
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i \qquad \text{Eq. (4.14)}$$

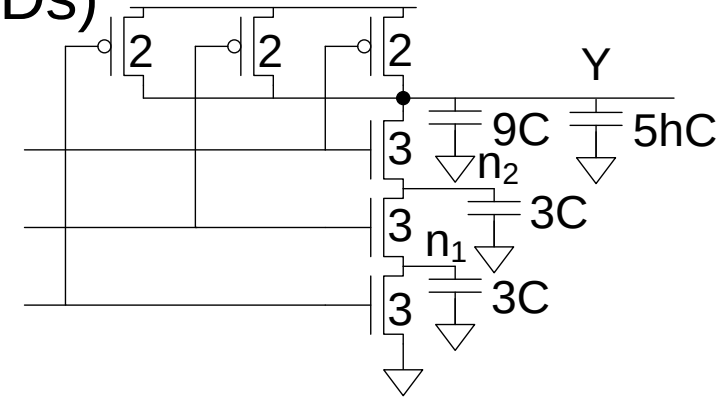
$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$

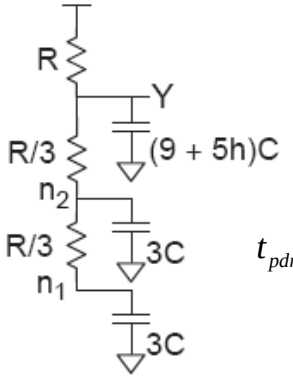


4.3. RC delay model (8)

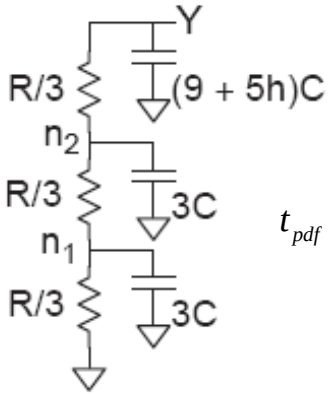
- Example 4.7 (*h* identical NANDs)







$$t_{pdr} = (9+5h)RC$$



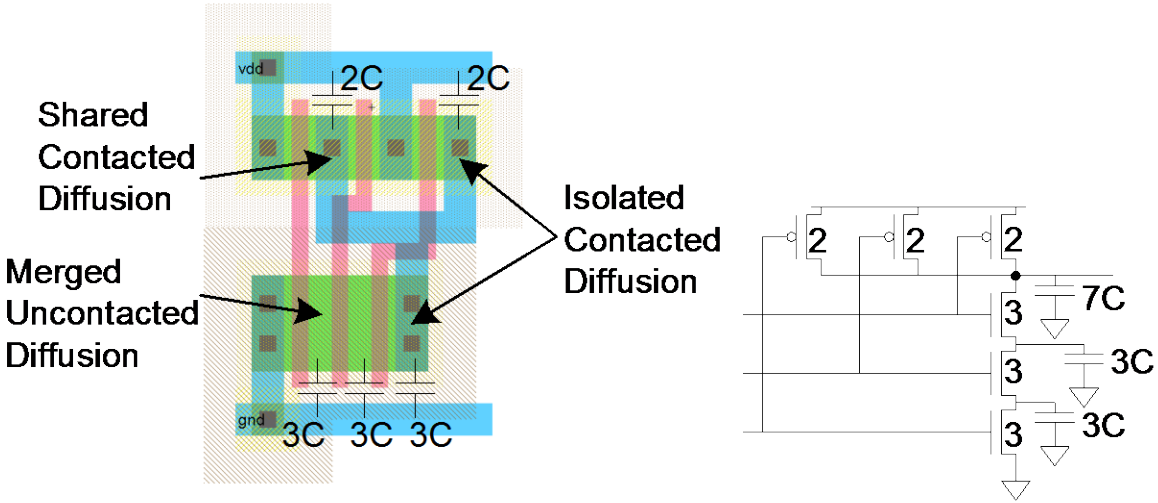
$$t_{pdf} = (3C)\left(\tfrac{R}{3}\right) + (3C)\left(\tfrac{R}{3}+\tfrac{R}{3}\right) + \left[(9+5h)C\right]\left(\tfrac{R}{3}+\tfrac{R}{3}+\tfrac{R}{3}\right)$$
$$= (12+5h)RC$$

4.3. RC delay model (9)

- Delay components
  - Parasitic delay
    - 9 or 12 RC
    - Independent on load
  - Effort delay
    - 5*h* RC
    - Proportional to load capacitance

4.3. RC delay model (9)

- Layout dependence of capacitance
  - Good layout minimizes the diffusion area.



4.4. Linear delay model (1)

- Delay in a logic gate
  - Express delays in process-independent unit

$$d = \frac{t_{pd}}{\tau} = \frac{t_{pd}}{3RC} \quad \text{Eq. (4.15)}$$

  - Delay has two components:

$$d = f + p \quad \text{Eq. (4.20)}$$

  - Effort delay

$$f = gh \quad \text{Eq. (4.21)}$$

  - Logical effort, g
    - $g \equiv 1$ for inverter

4.4. Linear delay model (2)

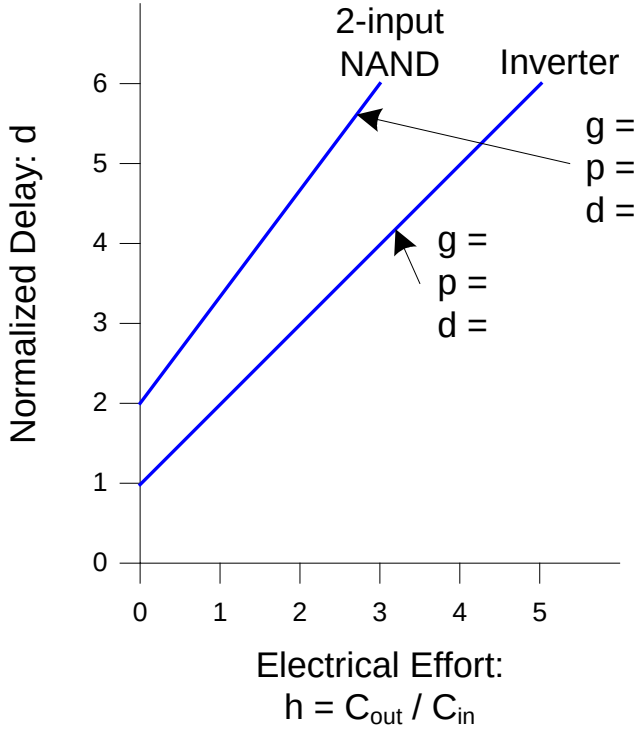
- Delay in a logic gate (continued)
  - Electrical effort

$$h = \frac{C_{out}}{C_{in}} \qquad \text{Eq. (4.22)}$$

    - Ratio of output to input capacitance
  - Parasitic delay, p
    - Represents delay of gate driving no load
    - Set by internal parasitic capacitance

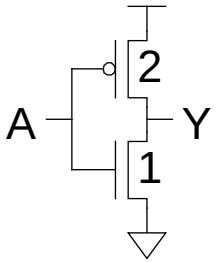
4.4. Linear delay model (3)

- Normalized delay versus fanout

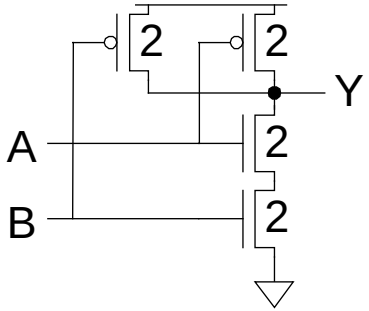


4.4. Linear delay model (4)

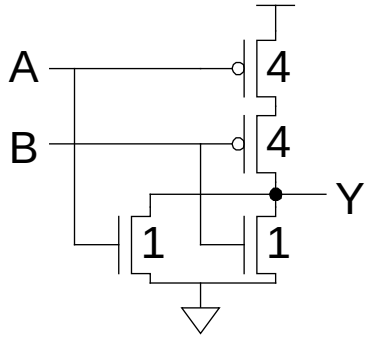
- Computing logical effort
  - *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delevering the same output current.*



C_{in} = 3
g = 3/3



C_{in} = 4
g = 4/3



C_{in} = 5
g = 5/3

4.4. Linear delay model (5)

- Logical effort of common gates

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		4/3	5/3	6/3	(n+2)/3
NOR		5/3	7/3	9/3	(2n+1)/3
Tristate / mux	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

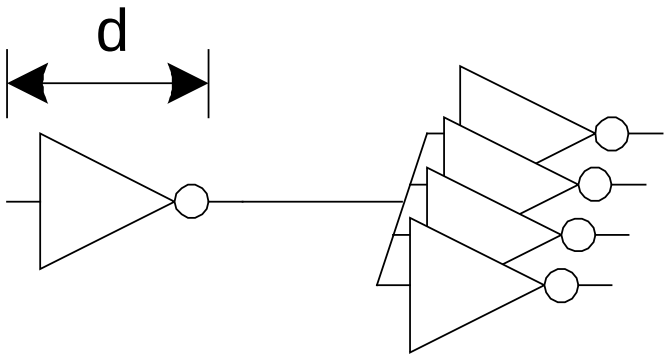
4.4. Linear delay model (6)

- Parasitic delay of common gates

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n
Tristate / mux	2	4	6	8	2n
XOR, XNOR		4	6	8	

4.4. Linear delay model (7)

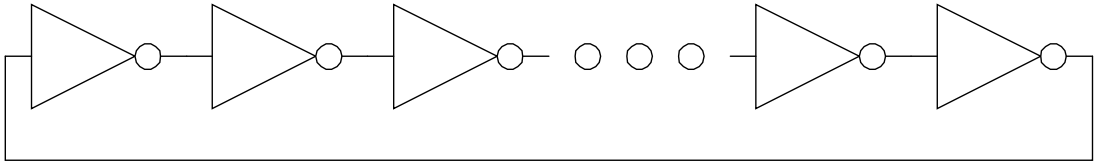
- Example 4.10



  - Logical Effort: g = 1
  - Electrical Effort: h = 4
  - Parasitic Delay: p = 1
  - Stage Delay: d = 5
  - When $\tau = 3RC = 3$ ps, the total delay is 15 ps.

4.4. Linear delay model (8)

- Example 4.11



  - Logical Effort: g = 1
  - Electrical Effort: h = 1
  - Parasitic Delay: p = 1
  - Stage Delay: d = 2
  - Frequency: $f_{osc} = 1/(2*N*d) = 1/4N$