Austriamicrosystems 350nm CMOS process

(1) Geometrical parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
field oxide thickness	TFOX	260	290	320	nm	1
gate oxide thickness	TGOX	7.1	7.6	8.1	nm	2
poly1 thickness	TPOLY1	264	282	300	nm	1
metal1-poly oxide thickness (field region)	TILDFOX	395	645	895	nm	1
metal2-metal1 oxide thickness	TIMD1	620	1000	1380	nm	1
metal3-metal2 oxide thickness	TIMD2	620	1000	1380	nm	1
metal1 thickness	TMET1	565	665	765	nm	3
metal2 thickness	TMET2	540	640	740	nm	3
metal3 thickness (top metal)	TMET3T	775	925	1075	nm	3
passivation thickness 1	TPROT1	800	900	1000	nm	1
passivation thickness 2	TPROT2	800	1000	1200	nm	1
INFORMATION PARAMETERS						
metal1-poly oxide thickness (active region)	TILDDIFF	1140	1290	1440	nm	1
n+ junction depth	XJN		0.2		µm	4
p+ junction depth	XJP		0.2		µm	4
n-well junction depth	XJNW		2.0		µm	4
wafer substrate resistivity (non epi)	RSWAF	14	19	24	Ω cm	5
wafer thickness	TWAF	710		740	µm	5

(2) 3.3V NMOS parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage long channel 10x10	VTO10X10N	0.36	0.46	0.56	V	6
threshold voltage short channel 10x0.35	VTO10X035N	0.40	0.50	0.60	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_N3	0.49	0.59	0.69	V	6
threshold voltage poly on field 0.6µm	VTFPN	15	> 20		V	9
effective channel length 0.35µm	LEFF035N	0.30	0.38	0.46	µm	10
effective channel width 0.4µm	WEFF04N	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAN	0.48	0.58	0.68	$V^{½}$	12
gain factor	KPN	150	170	190	$µA/V^2$	7
drain-source breakdown 0.35µm	BVDS035N	7	> 8		V	14
saturation current 0.35µm	IDS035N	450	540	630	µA/µm	15
substrate current 0.35µm	ISUB035N		1.5	3	µA/µm	16
subthreshold leakage current 0.35µm	SLEAK035N		0.5	2	pA/µm	17
gate oxide breakdown	BVGOXN	7	> 8		V	18
INFORMATION PARAMETERS						
active channel length 0.35µm	LACT035N		0.29		µm	26
threshold voltage narrow channel 0.4x10	VTO04X10N		0.46		V	6
threshold voltage small channel 0.4x0.35	VTO04X035N		0.48		V	6
threshold voltage temperature coefficient	TCVTON		-1.1		mV/K	13
effective substrate doping	NSUBN		212		$10^{15}/cm^3$	12
effective mobility	UON		370		cm^2/Vs	8
mobility exponent	BEXN		-1.8		-	13

(3) 3.3V PMOS parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage long channel 10x10	VTO10X10P	-0.58	-0.68	-0.78	V	6
threshold voltage short channel 10x0.35	VTO10X035P	-0.55	-0.65	-0.75	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_P3	-0.62	-0.72	-0.82	V	6
threshold voltage poly on field 0.6µm	VTFPP	-15	< -20		V	9
effective channel length 0.35µm	LEFF035P	0.42	0.50	0.58	µm	10
effective channel width 0.4µm	WEFF04P	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAP	-0.32	-0.40	-0.48	$V^{½}$	12
gain factor	KPP	48	58	68	$µA/V^2$	7
drain-source breakdown 0.35µm	BVDS035P	-7	< -8		V	14
saturation current 0.35µm	IDS035P	-180	-240	-300	µA/µm	15
subthreshold leakage current 0.35µm	SLEAK035P		-0.5	-2	pA/µm	17
gate oxide breakdown	BVGOXP	-7	< -8		V	18
INFORMATION PARAMETERS						
active channel length 0.35µm	LACT035P		0.31		µm	26
threshold voltage narrow channel 0.4x10	VTO04X10P		-0.90		V	6
threshold voltage small channel 0.4x0.35	VTO04X035P		-0.68		V	6
threshold voltage temperature coefficient	TCVTOP		1.8		mV/K	13
effective substrate doping	NSUBP		101		$10^{15}/cm^3$	12
effective mobility	UOP		126		cm^2/Vs	8
mobility exponent	BEXP		-1.30		-	13

(4) I/V Characteristics

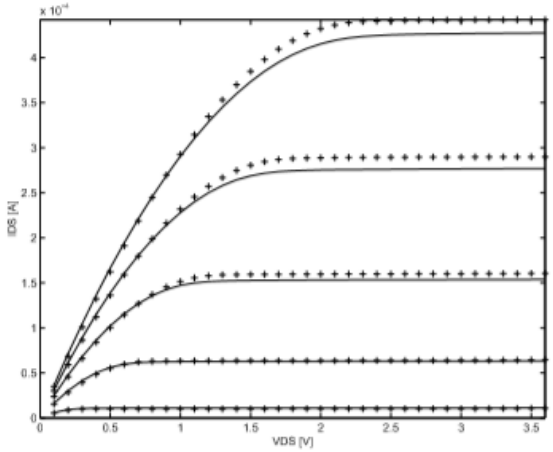

Fig.5.1 NMOS output characteristic of a typical wafer. W/L = 10/10,
VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V,
+ = measured, — = BSIM3v3 model

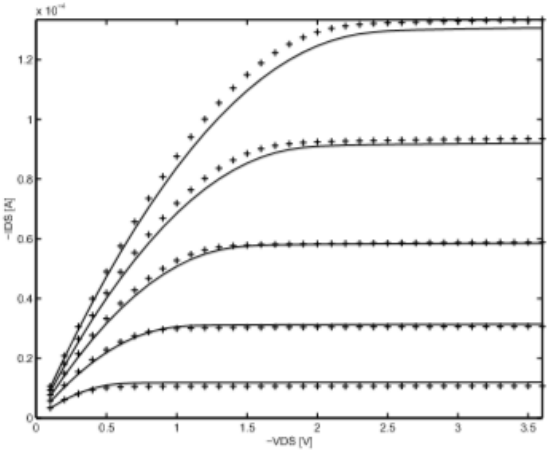

Fig. 5.2 PMOS output characteristic of a typical wafer. W/L = 10/10,
VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V,
+ = measured, — = BSIM3v3 model

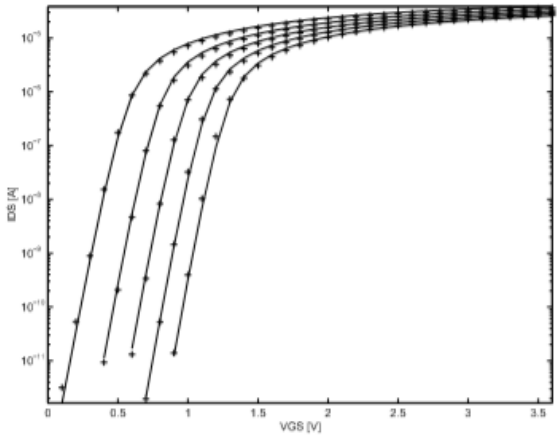

Fig. 5.3 NMOS transfer characteristic of a typical wafer. W/L = 10/10,
VBS =0,-0.9,-1.8,-2.7,-3.6 V, VDS = 0.1 V
+ = measured, — = BSIM3v3 model

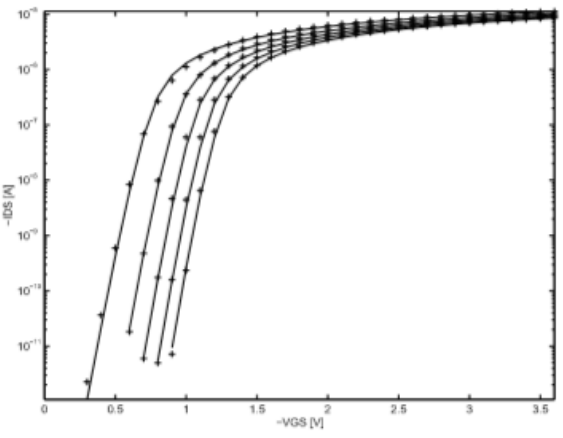

Fig. 5.4 PMOS transfer characteristic of a typical wafer. W/L = 10/10,
VBS =0,0.9,1.8,2.7,3.6 V, VDS = -0.1 V
+ = measured, — = BSIM3v3 model

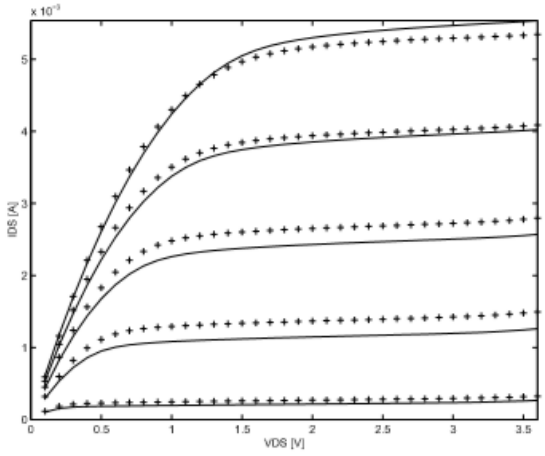

Fig. 5.5 NMOS output characteristic of a typical wafer. W/L = 10/0.35, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

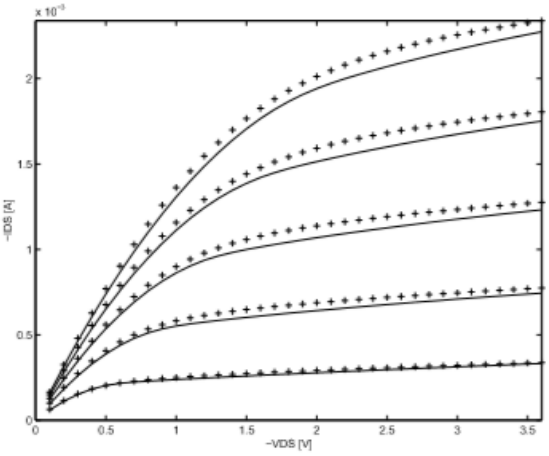

Fig. 5.6 PMOS output characteristic of a typical wafer. W/L = 10/0.35, VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model

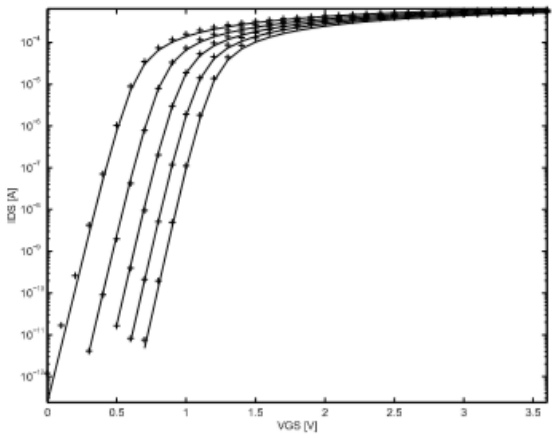

Fig. 5.7 NMOS transfer characteristic of a typical wafer. W/L = 10/0.35, VBS =0,-0.9,-1.8,-2.7,-3.6 V, VDS = 0.1 V + = measured, — = BSIM3v3 model

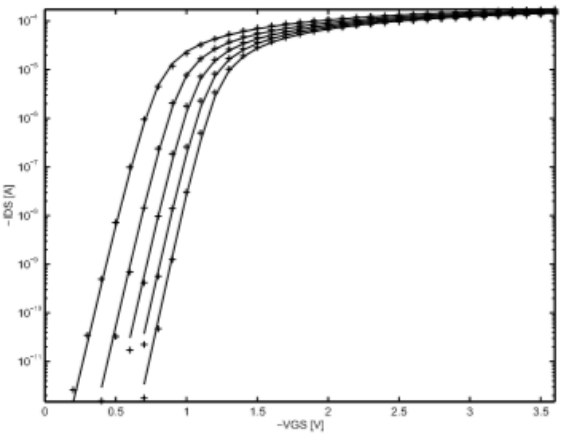

Fig. 5.8 PMOS transfer characteristic of a typical wafer. W/L = 10/0.35, VBS =0,0.9,1.8,2.7,3.6 V, VDS = -0.1 V + = measured, — = BSIM3v3 model