HW6: Digital Integrated Circuit

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Exercise 4.1)

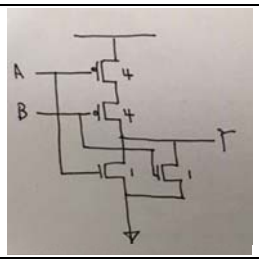

Figure 1. A 2-input NOR gate with the transistor widths, which a given problem described.

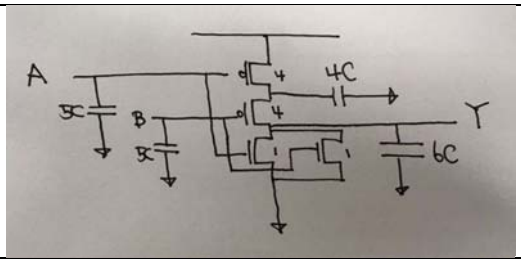

Figure 2. The capacitance-considered circuit diagram of the given NOR gate with the width.

A 2-input NOR gate, which has effective rise and fall resistances equal to a unit inverter is drawn in figure 1. The pull-up network of the 2-input NOR gate has two PMOS connected in series. Assuming the width of the two PMOS is p, the rise resistance should be $4R/p$ with appropriately defined R. Similarly, the pull-down network of the NOR gate has two NMOS connected in parallel, and the fall resistance (the worst case) should be R/n with width of the two NMOS, n. Then, we obtain the width ratio between the PMOS and the NMOS as $p/n = 4$, because effective rise and fall resistances is same in the unit inverter.

The rising and falling delay can be estimated by Elmore delay using figure 2, which describes the capacitance-considered circuit of the given NOR gate. Thus, the delay is calculated as

$$T_{rise} = (6 + 5h)RC + \frac{R}{2} \times 4C = (8 + 5h)RC$$

$$T_{fall} = (6 + 5h)RC$$

Exercise 4.4)

A n-input NOR gate induces that ratio between its PMOS and NMOS widths is determined as $2n$ by similar argument to exercise 4.1, and then the capacitance of an output node is $2nC + nC = 3nC$. For estimating a rising delay, effective resistance and capacitance between the each PMOS in pull-up network are calculated as R/n and $2nC$ by the determined PMOS width. Then, the rising delay is

$$T_{rise} = 3nRC + \sum_{k=1}^{n-1} \left(k \times \frac{R}{n} \times 2nC \right) = [3n + n(n-1)]RC = (n^2 + 2n)RC$$

The worst case falling delay, which is that n NMOS are connected in parallel, can be calculated with similar process as $T = 3nRC$. Finally, we can determine that the rising delay is the worst (the longest) Elmore parasitic delay.

Exercise 4.9)

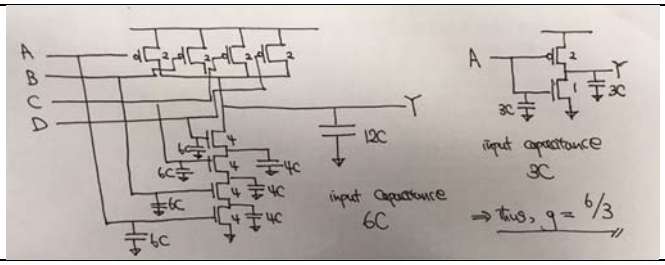

Figure 3. A capacitance-considered 4-input NAND gate with width information

Exercise 4.10)

TABLE 1

	Target	Figure (a)	Figure (b)
H	6	-	
B	1		
P	3		
G		4/3	5/3
$F = GBH$		8	10
$f = F^{1/2}$		2.8284	3.1623
$D = 2f + P$		**8.6568**	9.3246
$\boldsymbol{x = 6CG / f}$		**2.8369**	**3.1623**

As shown in table 1, simple calculation results show that a circuit in figure (a) will be better (faster) than figure (b) since the design of figure (a) has smaller delay (*D*).

Exercise 4.11)

TABLE 2

Target	Figure (a)	Figure (b)	Figure (c)	Figure (d)
B	1 (no branching)			
P	7	5	5	7
G	8/3	25/9	28/9	20/9
N	2	2	2	4
$D_{H=1} = N\,(GBH)^{1/N} + P$	10.265	**8.333**	8.527	11.883
$D_{H=5}$	14.302	**12.453**	12.888	14.302
$D_{H=20}$	21.605	19.907	20.776	**17.327**

As shown in table 2, $H = 1, 5$ induces that a design in figure (b) is the best, and $H = 20$ induces that a design in figure (d) is the best (fastest) logic circuit.

Exercise 5.1)

$$P = \alpha f C V^2 = 0.1 \times 450\ \text{MHz} \times (450\ \text{pF/mm}^2 \times 70\ \text{mm}^2) \times (0.9\ \text{V})^2 = 1.148\ \text{W}$$

Exercise 5.4)

A 1 GHz signal induces that period during its one cycle is 1 ns. Thus, using a figure in this exercise, the signal changes its state 4 times in 10 cycles, so that the activity factor is half of 4/10, $\boldsymbol{\alpha = 0.2}$, because if signal switches its states only 1 time in 1 cycle, its activity factor is 1.

Exercise 5.5)

Example 4.14

A control unit generates a signal from a unit-sized inverter. The signal must drive unit-sized loads in each bitslice of a 64-bit datapath. The designer can add inverters to buffer the signal to drive the large load. Assuming polarity of the signal does not matter, what is the best number of inverters to add and what delay can be achieved?

SOLUTION: Figure 4.33 shows the cases of adding 0, 1, 2, or 3 inverters. The path electrical effort is $H = 64$. The path logical effort is $G = 1$, independent of the number of inverters. Thus, the path effort is $F = 64$. The inverter sizes are chosen to achieve equal stage effort. The total delay is $D = N\sqrt[N]{64} + N$.

The 3-stage design is fastest and far superior to a single stage. If an even number of inversions were required, the two- or four-stage designs are promising. The four-stage design is slightly faster, but the two-stage design requires significantly less area and power.

TABLE 3

Stages	Delay constraint	Energy function	x	y	E_{min}
2	$x + 64/x + 2 = 20$	$E = 1 + x$	**4.877**	-	**5.877**
3	$x + y/x + 64/y + 3 = 20$	$E = 1 + x + y$	1.466	5.401	7.867

In this table, 1, x, and y are the size of the inverter in this design problem. Thus, two-stage buffer design has the lowest energy, whose size of corresponding inverters are determined as 1, 4.877.

Exercise 5.6)

TABLE 4

Stages	Delay constraint	Energy function	x	y	z	E_{min}
2	$x + 500/x + 2 = 30$	$E = 1 + x$	*	-	-	*
3	$x + y/x + 500/y + 3 = 30$	$E = 1 + x + y$	**4.997**	**32.091**	-	**38.087**
4	$x + y/x + z/y + 500/z + 4 = 30$	$E = 1 + x + y + z$	2.151	6.228	31.433	40.812

In order to solve this problem, each size of inverter in our design are defined as 1, x, y, and z. Since the two-stage case has no solution for its delay constraint, x cannot be determined. Moreover, in this case, three-stage buffer design has the lowest energy, whose size of corresponding inverters are calculated as 1, 4.997, 32.091.