DIC L22: Power (3)

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

GIST Lecture on November 28, 2019

5.2. Dynamic power (7)

- Capacitance
  - Gate capacitance (“Gate” is not a contact in this context.)
    - Fewer stages of logic
    - Small gate sizes
  - Wire capacitance
    - Good floorplanning to keep communicating blocks close to each other
    - Drive long wires with invertes of buffers rather than complex gates

5.2. Dynamic power (8)

- Voltage/Frequency
  - Run each block at the lowest possible voltage and frequency that meets performance requirements
  - Voltage domains
    - Provide separate supplies to different blocks
    - Level converters required when crossing from low to high V_{DD} domains

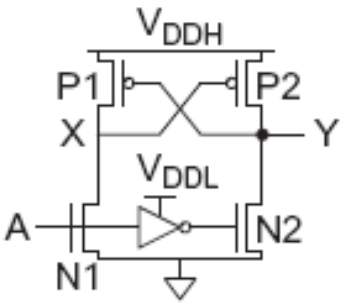
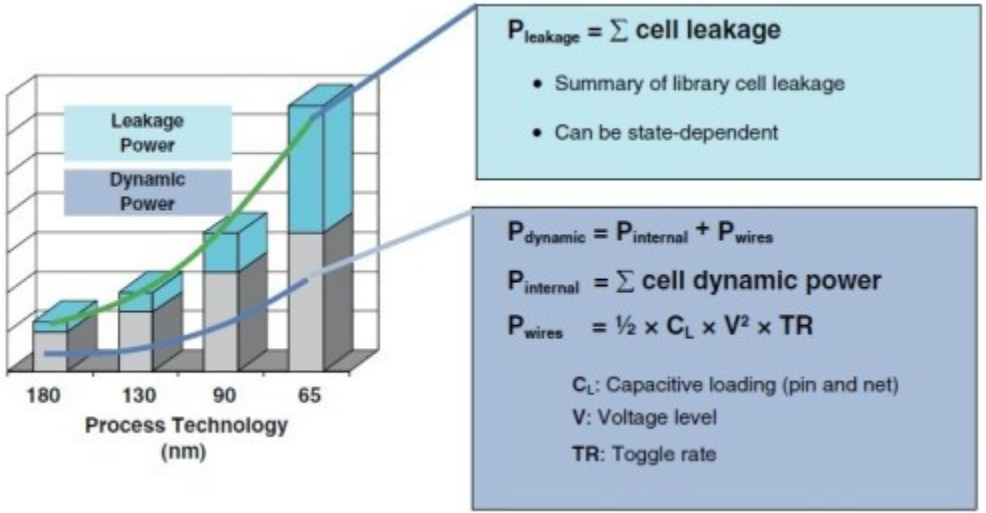


Fig. 5.15

5.3. Static power (1)

- Static power is consumed even when a chip is not switching.

$$P_{static} = \left(I_{sub} + I_{gate} + I_{junct} + I_{contention}\right)V_{DD}$$



(Semiconductor Engineering)

5.3. Static power (2)

- Subthreshold leakage

$$I_{sub} = I_{off} 10^{\frac{V_{gs}+\eta(V_{ds}-V_{DD})-k_\gamma V_{sb}}{S}}$$

Transistor Type	High Speed Logic		Low Power Logic		High Voltage	
Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)	0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)	90	90	90	108	min. 180	min. 450
Lgate (nm)	30	34	34	40	min. 80	min. 280
N/PMOS Idsat/Ioff (mA/um)	1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V 30 pA/um	0.35 / 0.33 @ 0.75 V 15 pA/um	0.92 / 0.8 @ 1.8 V 10 pA/um	1.0 / 0.85 @ 3.3 V 10 pA/um

(Intel's 2012 IEDM abstract)

5.3. Static power (3)

- Stack effect

$$I_{sub} = I_{off} 10^{\frac{V_{gs}+\eta(V_{ds}-V_{DD})-k_\gamma V_{sb}}{S}}$$

  - Series OFF transistors have less leakage
  - $V_x > 0$, so N2 has negative V_{gs}

$$I_{sub} = \underbrace{I_{off} 10^{\frac{\eta(V_x - V_{DD})}{S}}}_{N1} = \underbrace{I_{off} 10^{\frac{-V_x+\eta((V_{DD}-V_x)-V_{DD})-k_\gamma V_x}{S}}}_{N2}$$

$$V_x = \frac{\eta V_{DD}}{1+2\eta+k_\gamma}$$

$$I_{sub} = I_{off} 10^{\frac{-\eta V_{DD}\left(\frac{1+\eta+k_\gamma}{1+2\eta+k_\gamma}\right)}{S}} \approx I_{off} 10^{\frac{-\eta V_{DD}}{S}}$$

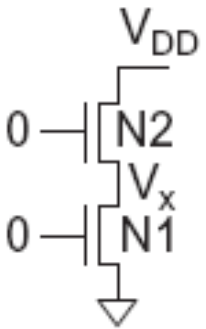
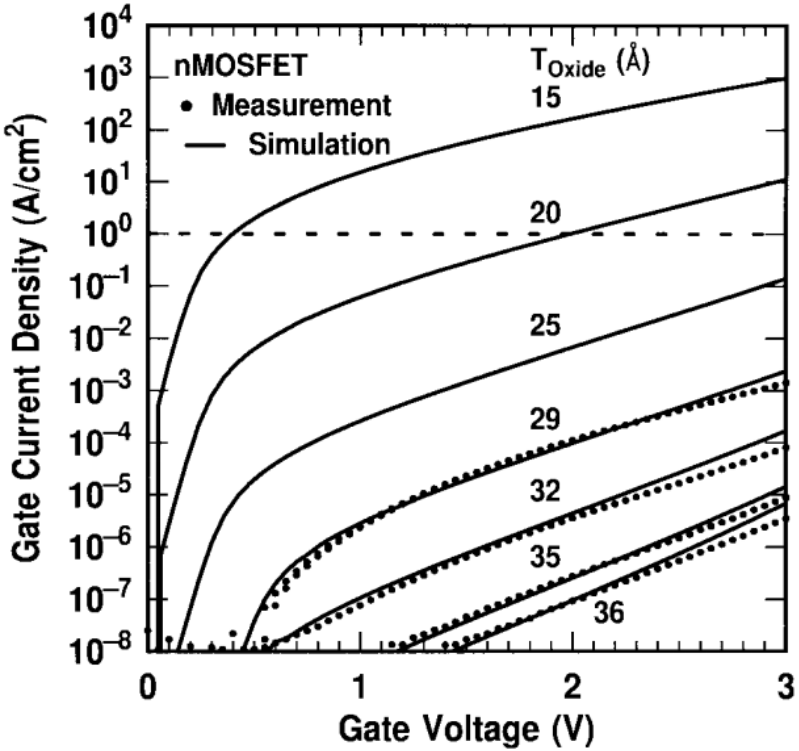


Fig. 5.20

5.3. Static power (3)

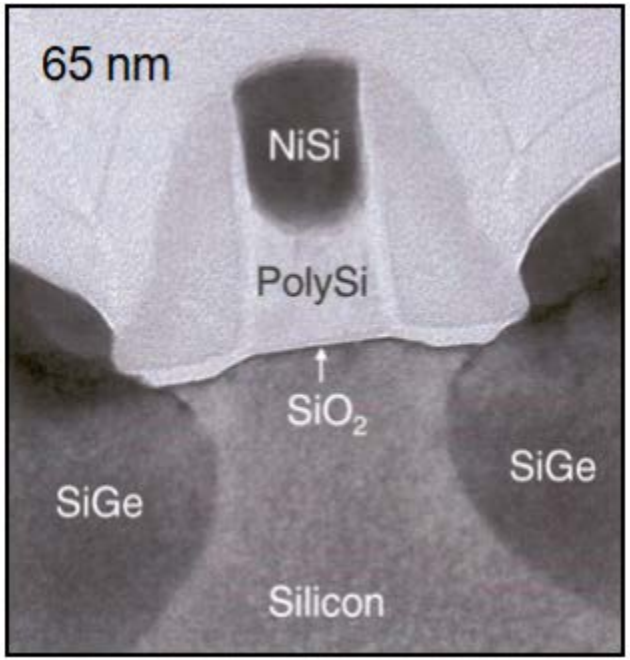
- Gate leakage
  - Various physical mechanisms
  - It is an extremely strong function of the dielectric thickness.
  - It also depends on the voltage across the gate.



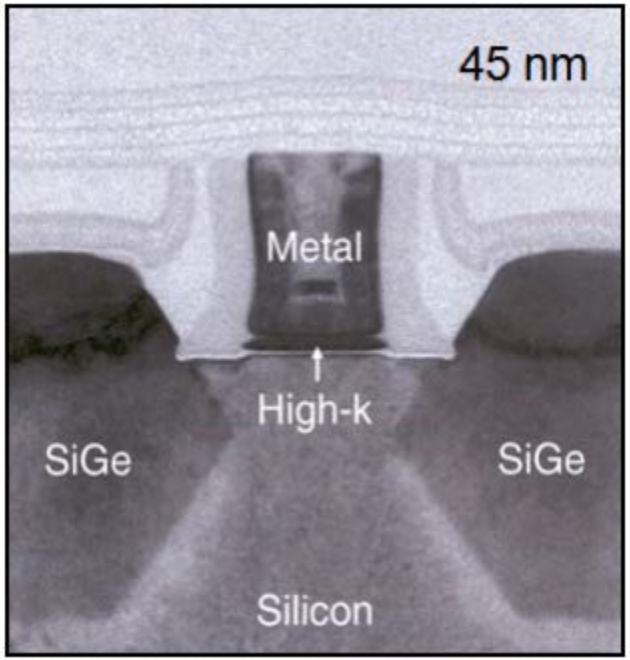
Measured Ig-Vg characteristics (Ho et al., EDL, vol. 18, pp. 209-211)

5.3. Static power (4)

- High-k metal gate



65nm

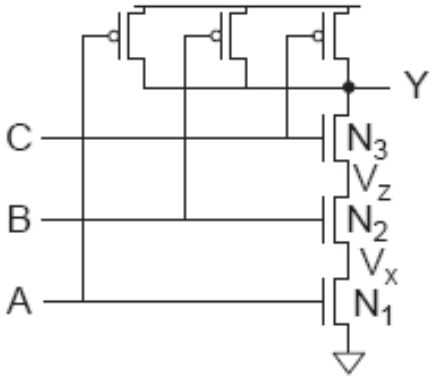


45nm high-k metal gate transistor

5.3. Static power (5)

- NAND3 leakage example

Input State (ABC)	I_{sub}	I_{gate}	I_{total}	V_x	V_z
000	0.4	0	0.4	stack effect	stack effect
001	0.7	0	0.7	stack effect	$V_{DD} - V_t$
010	0.7	1.3	2.0	intermediate	intermediate
011	3.8	0	3.8	$V_{DD} - V_t$	$V_{DD} - V_t$
100	0.7	6.3	7.0	0	stack effect
101	3.8	6.3	10.1	0	$V_{DD} - V_t$
110	5.6	12.6	18.2	0	0
111	28	18.9	46.9	0	0



5.3. Static power (6)

- Example 5.4
  - 50M logic transistors (Average width: 12λ)
    - 5 % low-V_T + 95 % high-V_T
  - 950M memory transistors (Average width: 4λ)
    - 100 % high-V_T
  - 1.0 V 65 nm process (λ is 25 nm.)
  - Subthreshold leakage is 100 nA/μm (low-V_T) or 10 nA/μm (high-V_T).
  - Gate leakage is 5 nA/μm. (Neglect the junction leakage.)
  - Estimate the static power consumption. (Assume that half the transistors contribute leakage currents.)

5.3. Static power (7)

- Power gating
  - Turn off the power supply to the sleeping blocks.
  - “A total of 1.5m of total width per core of ultra-low-leakage PMOS transistors are used with the gate terminal adaptively switched to the highest available chip voltage to further reduce leakage.”

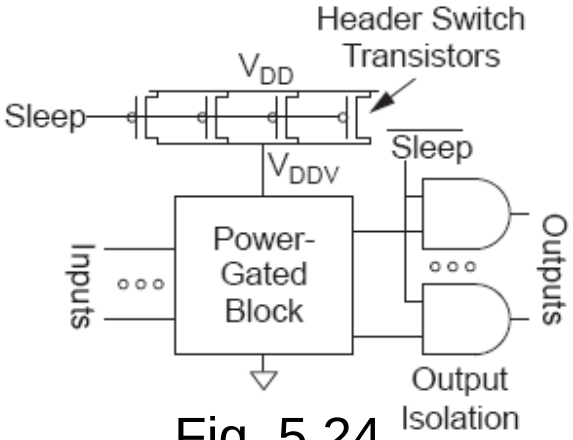
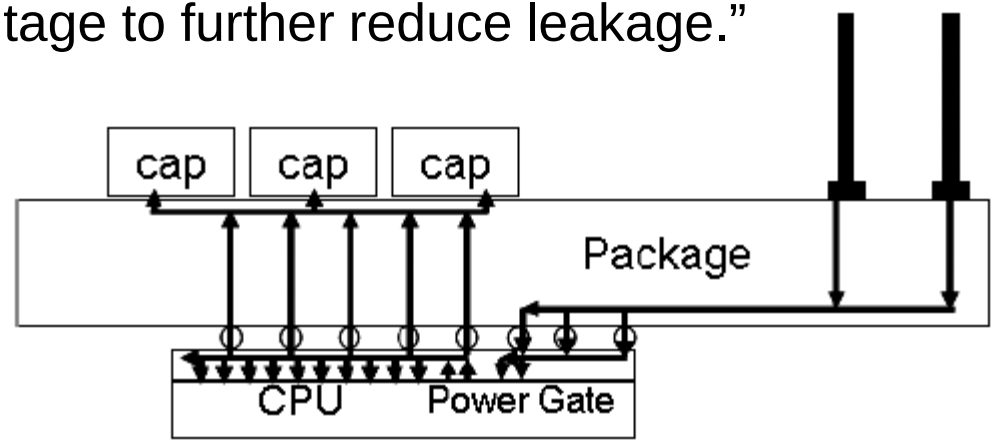


Fig. 5.24



(Kumar et al., ISSCC, 2009)

Homework#6 (The last)

- Solve the exercise problems of the textbook.
  - Exercise 4.1, Exercise 4.4, Exercise 4.9, Exercise 4.10, Exercise 4.11 (Five problems from Ch. 4)
  - Exercise 5.1, Exercise 5.4, Exercise 5.5, Exercise 5.6, (Four problems from Ch. 5)

- Due: December 3, 2019 (Before the lecture starts)
  - Upload your Homework to our GitHub repository.