DIC L11: Inverter (1)

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

GIST Lecture on October 22, 2019

2.4. Nonideal IV (12)

- Threshold voltage (Body effect)
  - It is given by

$$V_t = \frac{\sqrt{2\epsilon_{si} q N_A}}{C_{ox}} \sqrt{\phi_s + V_{sb}} + V_{FB} + \phi_s$$

Positive for negative V_b

γ, Eq. (2.37)

$\phi_s = 2v_T \log \frac{N_A}{n_i}$, Eq. (2.36)

  - Written as

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

2.4. Nonideal IV (13)

- Leakage
  - Subthreshold slope
  - DIBL
    - Drain-induced barrier lowering
  - GIDL
    - Gate-induced drain leakage

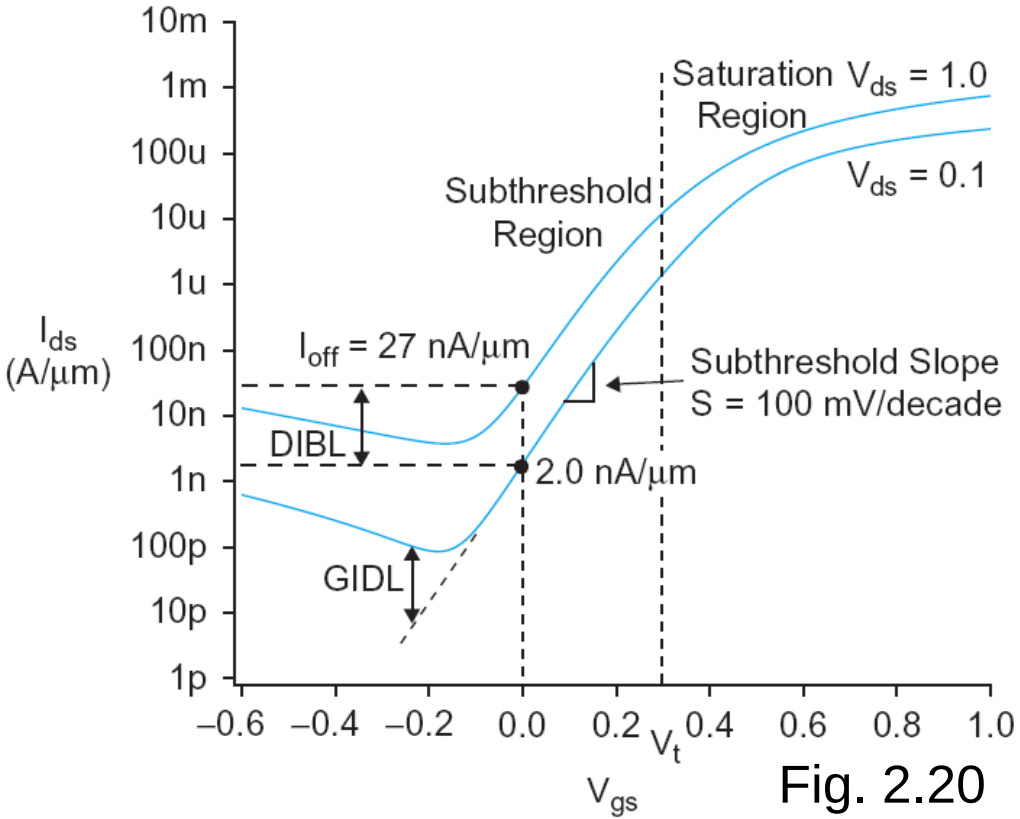


Fig. 2.20

2.5. DC transfer (1)

- A CMOS inverter
  - The transistor is a switch with an infinite off-resistance and a finite on-resistance.

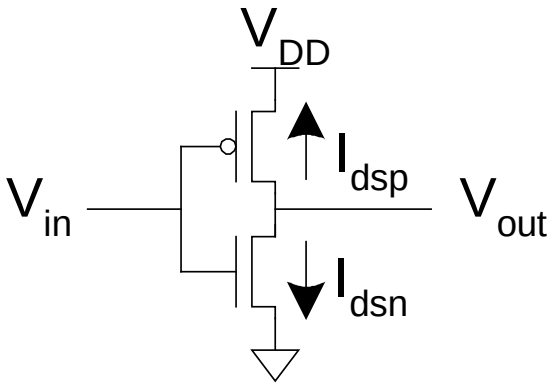
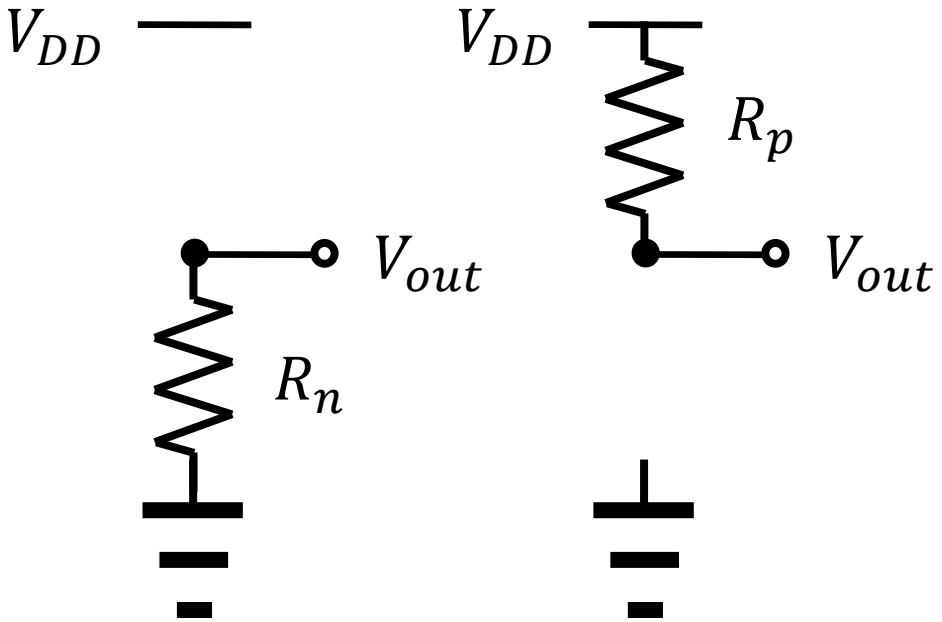


Fig. 2.26

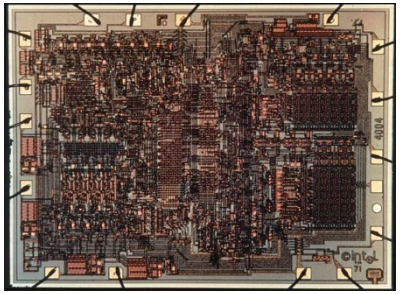


2.5. DC transfer (2)

- Important properties (Taken from Rabaey's book)
  - The HIGH and LOW output levels equal V_{DD} and GND, respectively.
  - The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size. (Ratioless)
  - A well-designed CMOS inverter has a low output impedance.
  - The input resistance of the CMOS inverter is extremely high.
  - The absence of current flow between V_{DD} and GND means that the gate does not consume any static power.

2.5. DC transfer (3)

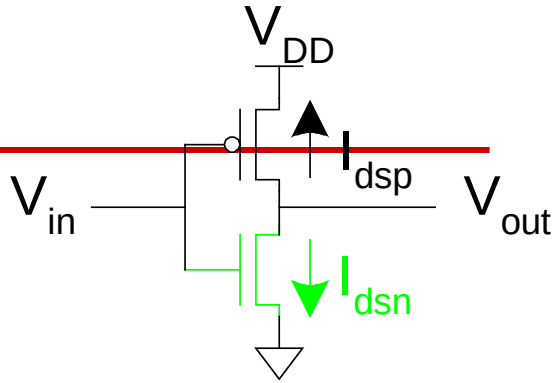
- Intel 4004
  - In 1971, the first microprocessor was released.
  - It has about 2300 transistors.
  - It was designed by Federico Faggin.
  - Masatoshi Shima helped him.
- It was implemented in a pure NMOS tech.



(4004)
Die size: 12 mm^2
Min. feature size: 10 micron
Max. clock speed: 740 kHz

Federico Faggin (Wikipedia)

2.5. DC transfer (4)

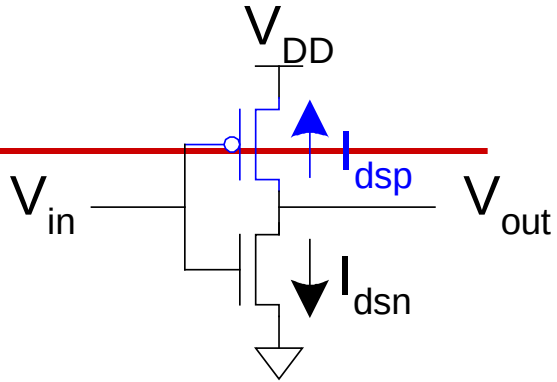


- NMOS
  - It is turned on at HIGH input voltages

Cutoff	Linear	Saturated
$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

Table 2.2

2.5. DC transfer (5)



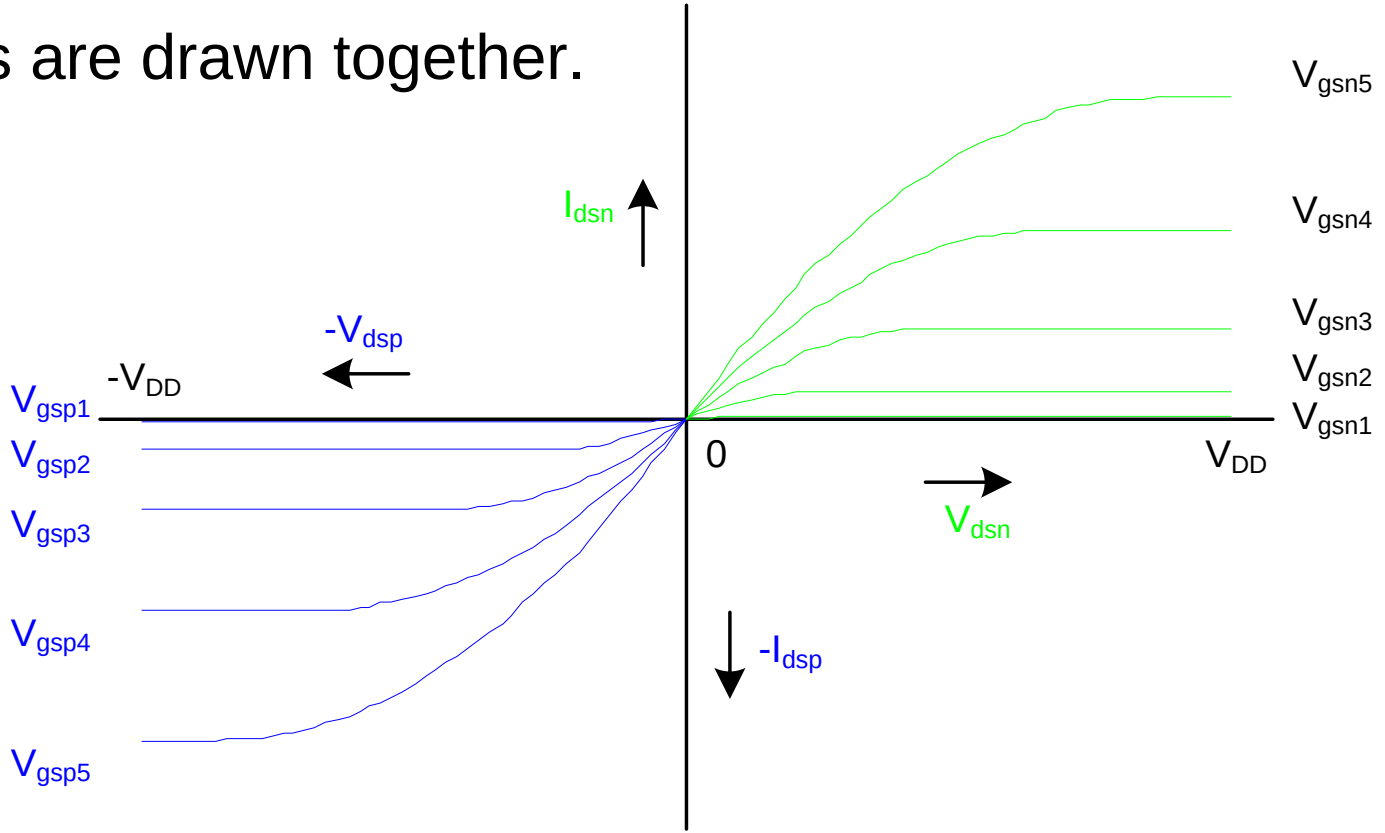
- PMOS
  - It is turned on at LOW gate voltages.

Cutoff	Linear	Saturated
$V_{gsp} > V_{tp}$ $V_{in} > V_{DD} + V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{DD} + V_{tp}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

Table 2.2

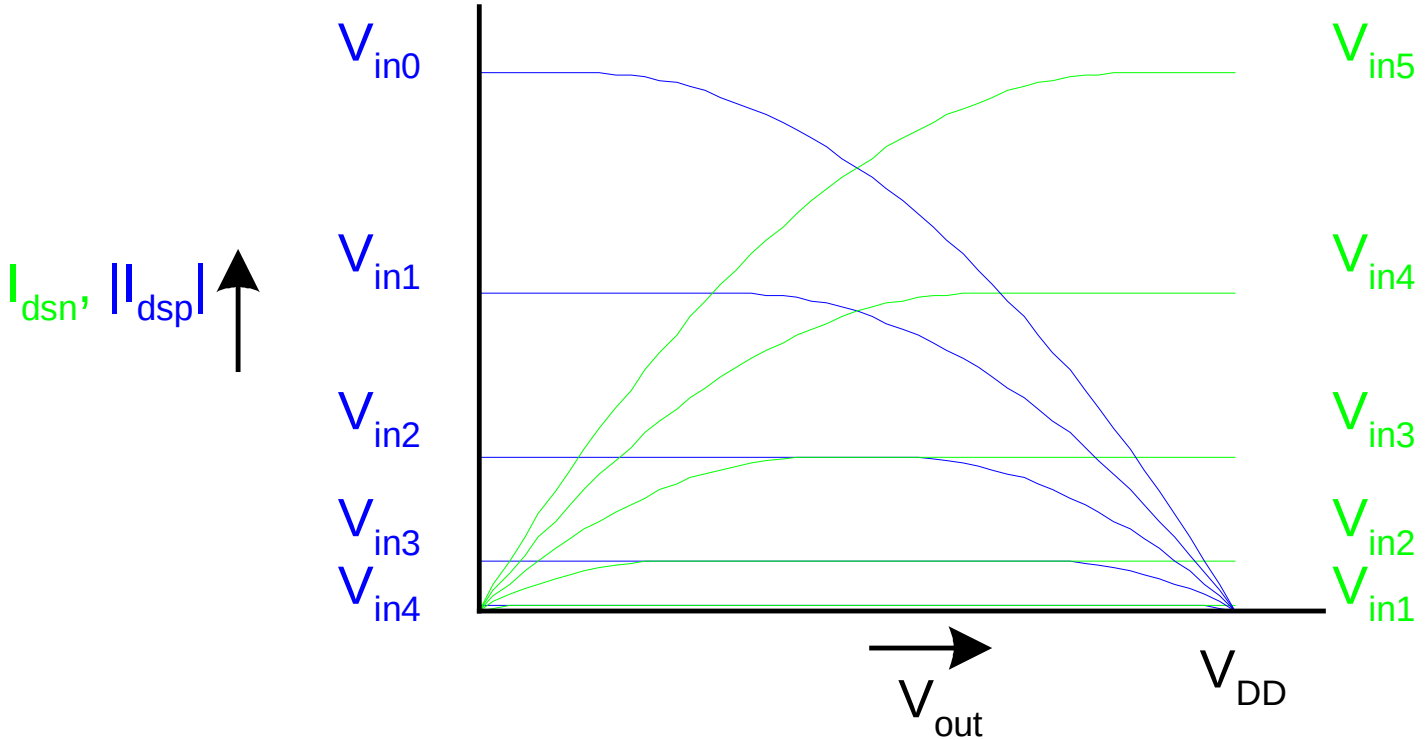
2.5. DC transfer (6)

- Two curves are drawn together.



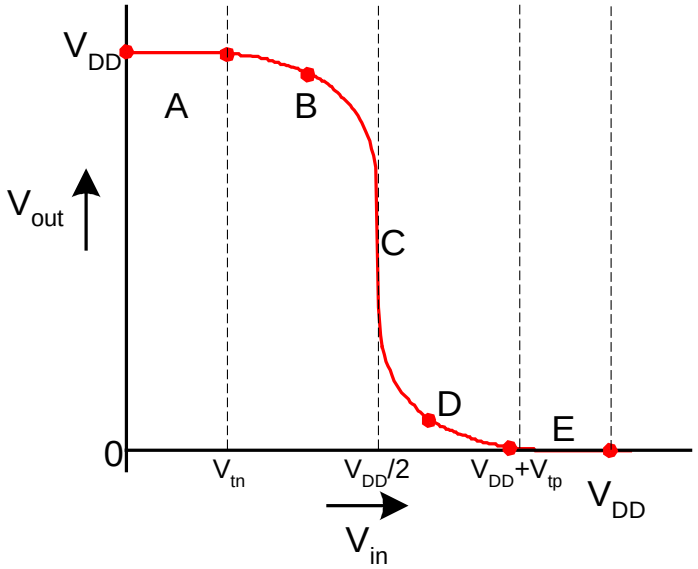
2.5. DC transfer (7)

- Same graph, but in terms of V_{in} and V_{out}



2.5. DC transfer (8)

- Operating regions
  - We have five points. Indentify the operational modes of transistors.



2.5. DC transfer (9)

- Input threshold, V_{inv} (or swithcing threshold)
  - When $V_{in} = V_{out} = V_{inv}$
- Beta ratio
  - Skewed
  - HI-skewed, $\frac{\beta_p}{\beta_n} > 1$
    - Stronger PMOS
  - LO-skewed, $\frac{\beta_p}{\beta_n} < 1$
    - Weaker PMOS