DIC L21: Power (2)

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5.1. Introduction (4)

- Average power dissipation
  - When a gate is

$$P_{switching} = \frac{CV_{DD}^2}{T} = CV_{DD}^2 f_{sw}$$

- Most gates do not switch every clock cycle.
  - Let $f_{sw} = \alpha f$, where α is the activity factor.
  - Then, the dynamic power is written as

$$P_{switching} = \alpha CV_{DD}^2 f$$

5.1. Introduction (5)

- Power dissipation sources

$$P_{total} = P_{dynamic} + P_{static}$$

  - Dynamic power

$$P_{dynamic} = P_{switching} + P_{shortcircuit}$$

  - Static power

$$P_{static} = \left(I_{sub} + I_{gate} + I_{junct} + I_{contention}\right)V_{DD}$$

5.1. Dynamic power (1)

- Example 5.1
  - 50M logic transistors (Average width: 12λ)
    - Activity factor = 0.1
  - 950M memory transistors (Average width: 4λ)
    - Activity factor = 0.02
  - 1.0 V 65 nm process (λ is 25 nm.)
  - C = 1 fF/μm (gate) + 0.8 fF/μm (diffusion)
  - Estimate the switching power when operating at 1 GHz.

5.1. Dynamic power (2)

- Example 5.1
  - 50M logic transistors (Average width: 12λ)
    - Activity factor = 0.1
  - 950M memory transistors (Average width: 4λ)
    - Activity factor = 0.02
  - 1.0 V 65 nm process (λ is 25 nm.)
  - C = 1 fF/μm (gate) + 0.8 fF/μm (diffusion)
  - Estimate the switching power when operating at 1 GHz.

5.1. Dynamic power (3)

- Remember that

$$P_{switching} = \alpha C V_{DD}^2 f$$

  - Try to minimize:
  - Activity factor (α)
  - Capacitance (C)
  - Suply voltage (V_{DD}^2)
  - Frequency (f)

5.1. Dynamic power (3)

- Activity factor estimation
  - Define P_i to be the probability that node i is 1. Also, $\overline{P_i} = 1 - P_i$.
  - Then,

$$\alpha_i = \overline{P_i}\, P_i$$ ← Assumption?

  - Completely random data has $P_i = 0.5$ and $\alpha = 0.25$.
    - (It is the maximum value of $\overline{P_i}\, P_i$.)
  - Data is often not completely random.

5.1. Dynamic power (4)

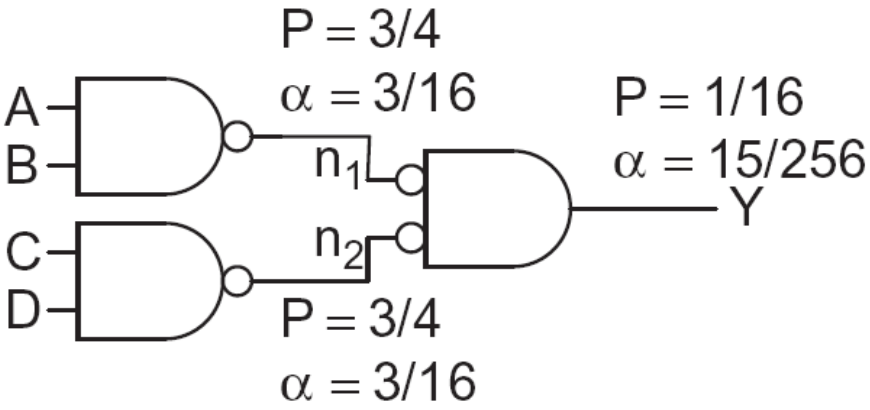
- Switching probability
  - Activity factor of the output is $\overline{P_Y}\ P_Y$.

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \overline{P}_A \overline{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\overline{P}_A \overline{P}_B$
XOR2	$P_A \overline{P}_B + \overline{P}_A P_B$

Table 5.1

5.1. Dynamic power (4)

- Example 5.2
  - A 4-input AND is built out of two levels of gates.
  - Estimate the activity factor at each node if the inputs have $P = 0.5$.



5.1. Dynamic power (6)

- Clock gating
  - The best way to reduce the activity is to turn off the clock to registers in unused blocks.
  - Saves clock activity ($\alpha = 1$)
  - Eliminates all switching activity

  in the block

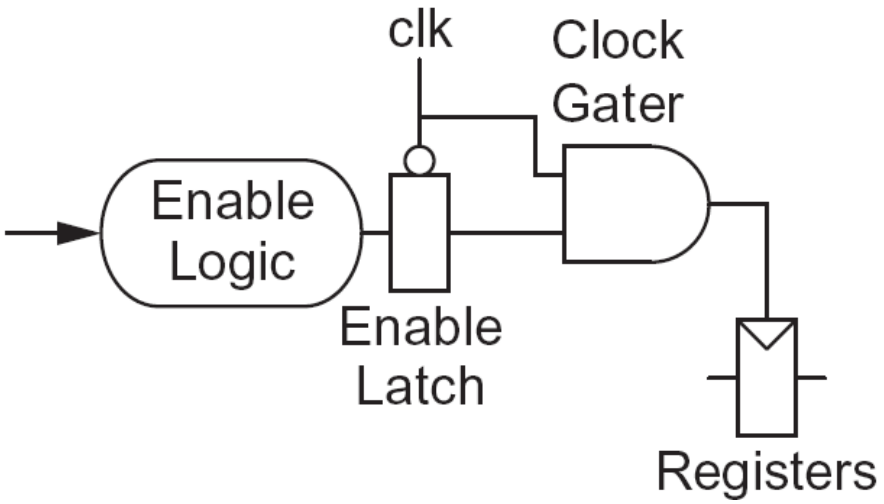


Fig. 5.7

5.1. Dynamic power (6)

- Capacitance
  - Gate capacitance (“Gate” is not a contact in this context.)
    - Fewer stages of logic
    - Small gate sizes
  - Wire capacitance
    - Good floorplanning to keep communicating blocks close to each other
    - Drive long wires with invertes of buffers rather than complex gates