Digital Integrated Circuit HW#6.

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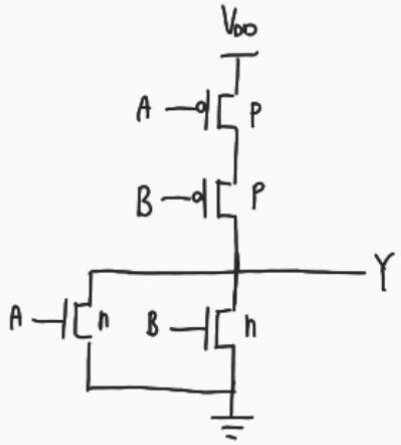
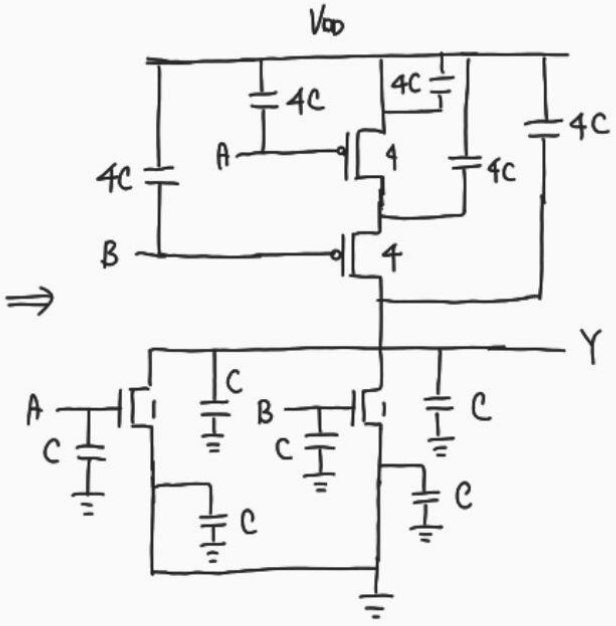
Exercise 4.1



<2-input NOR gate>

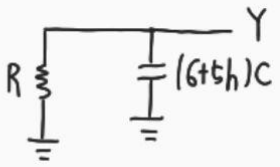
$2 \times \frac{2R}{P} = \frac{R}{n} \Rightarrow P:n = 4:1$



gate capacitance = 5C (at each input)

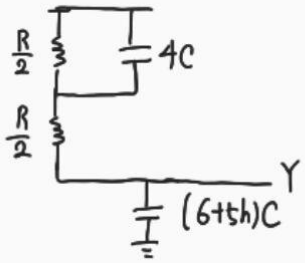
parasitic capacitance = C+C+4C = 6C

Falling propagation delay



$t_{pdf} = R \times (6+th)C = (6+th)RC$

Rising propagation delay

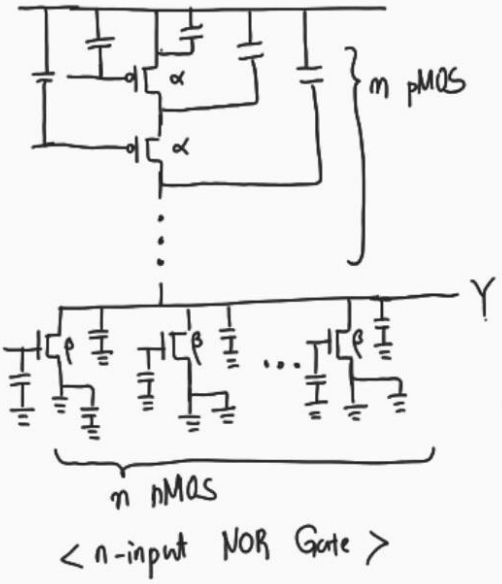


$t_{pdr} = \frac{R}{2} \cdot 4C + \left(\frac{R}{2}+\frac{R}{2}\right) \times (6+th)C = (8+th)RC$

Answer) $t_{pdf} = (6+th)RC$, $t_{pdr} = (8+th)RC$

(2-input NOR Gate is sketched above)

Exercise 4.4.



< n-input NOR Gate >

$\frac{2R}{\alpha} \cdot n = \frac{R}{\beta} = R$

$\alpha = 2n$, $\beta = 1$

parasitic capacitance $= 2nC + n \times C$

$= 3nC$

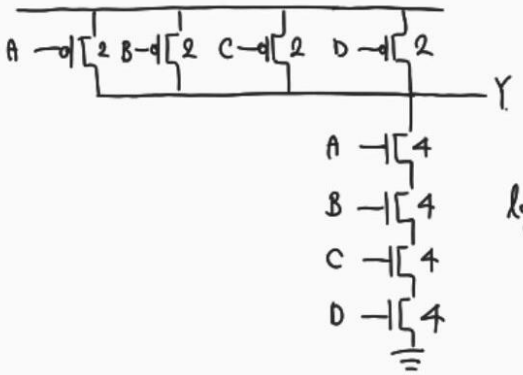
$t_{pd} = \sum_{i=1}^{n-1} \left(\frac{iR}{n}\right)(2nC) + 3nRC$

$= \sum_{i=1}^{n-1} 2iRC + 3nRC$

$= 2RC \cdot \frac{n(n-1)}{2} + 3nRC = (n^2 + 2n)RC$

Answer) $t_{pd} = (n^2+2n)RC$

Exercise 4.9.



gate capacitance $= 2C + 4C = 6C$

logical effort, g

$= \frac{\text{(ratio of the input capacitance)}}{\text{(ratio of the input capacitance of the inverter)}}$

$= \frac{6C}{3C} = \frac{6}{3}$

Exercise 4.10.

(a) would be faster than (b) because NAND gate in (a) has lower logical effort than the NOR gate in (b).

At (a), $G = \frac{4}{3} \cdot 1 = \frac{4}{3}$, $B = 1$, $H = 6$ $\Rightarrow F = \frac{4}{3} \cdot 1 \cdot 6 = 8$

$D = \left((2+1) + 2 \cdot 8^{\frac{1}{2}}\right)\tau = 8.6\tau$, $8^{\frac{1}{2}} = \frac{6c}{x} \Rightarrow \underline{x = 2.12C}$

At (b), $G = 1 \cdot \frac{5}{3} = \frac{5}{3}$, $B = 1$, $H = 6$ $\Rightarrow F = \frac{5}{3} \cdot 1 \cdot 6 = 10$

$D = \left((2+1) + 2 \cdot 10^{\frac{1}{2}}\right)\tau = 9.3\tau$, $10^{\frac{1}{2}} = \frac{5}{3}\frac{6c}{y} = \frac{10c}{y} \Rightarrow \underline{y = 3.16C}$

Answer) path effort in (a) : 8, path effort in (b) : 10.

delay in (a) : 8.6τ, delay in (b) : 9.3τ

$x = 2.12C$, $y = 3.16C$

Exercise 4.11

	N	G	P	D (H=1)	D (H=5)	D (H=20)
(a)	2	$\frac{8}{3} \cdot 1 = \frac{8}{3}$	1+6=7	10.27	14.30	21.61
(b)	2	$\frac{5}{3} \cdot \frac{5}{3} = \frac{25}{9}$	3+2=5	8.33	12.45	19.91
(c)	2	$\frac{4}{3} \cdot \frac{7}{3} = \frac{28}{9}$	2+3=5	8.53	12.89	20.28
(d)	4	$\frac{5}{3} \cdot 1 \cdot \frac{4}{3} \cdot 1 = \frac{20}{9}$	3+1+2+1=7	11.88	14.30	17.33

Answer) At H=1, (b) is the fastest.

At H=5, (b) is the fastest.

At H=20, (d) is the fastest.

Exercise 5.1.

$P = \alpha C V_{DD}^2 f = 0.1 \times 450 \times 10^{-12} \times 70 \times 0.9^2 \times 450 \times 10^6 = 1.148\ W$

Answer) 1.148 W

Exercise 5.4.

clock rate = 1GHz $\Rightarrow$ period = 10^{-9} s

The signal makes 4 transitions in 10 cycles.

$\alpha = \frac{1}{2} \times \frac{4}{10} = 0.2$

Answer) 0.2

Exercise 5.5

A two stage will use the least energy.

stage	delay (=20)	Energy
2	$2 + 64/x + 1$	$1 + x$ $\Rightarrow x = 4.88$, $E = 5.88$

Answer) 2 stage, transistor width = 4.88.

Exercise 5.6

stage	delay (=30)	Energy
2	$2 + x + \frac{600}{x}$	$1 + x$ $\Rightarrow$ x would be imaginary number
3	$3 + \frac{100}{x} + \frac{x}{y} + y$	$1 + x + y$ $\Rightarrow x = 5.00$, $y = 32.09$ $\Rightarrow E = 38.09$

Answer) 3 stage, transistor width = 5.00, 32.09.