DIC L24: Interconnect (2)

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6.1. Introduction (1)

- Wire geometry
  - Pitch = $w + s$
  - Aspect ratio (AR) = $\frac{t}{w}$
  - Older processes had AR << 1.
  - Modern processes have AR ≈ 2.

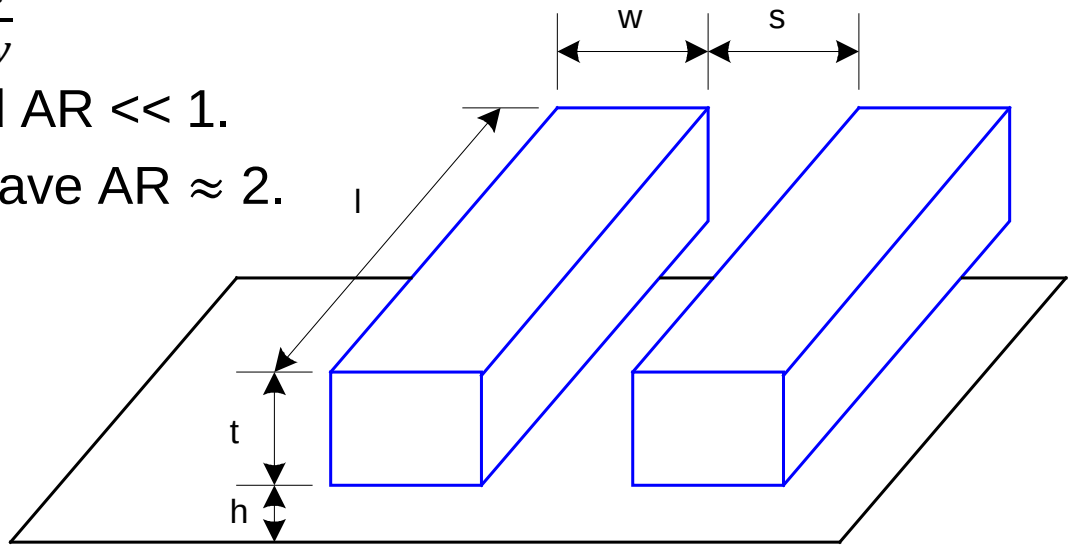


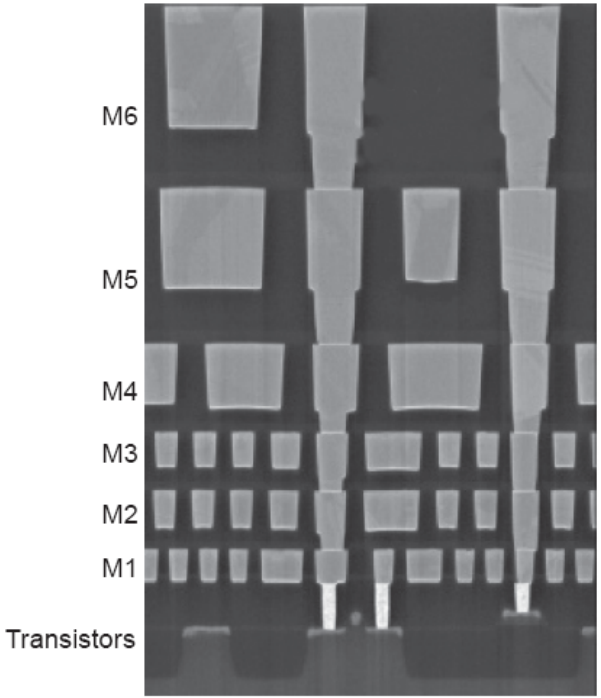
Fig. 6.1

6.1. Introduction (2)

- Example: Intel metal stacks

Layer	Dielectric Material	Pitch (nm)	Thick (nm)	Aspect Ratio
Metal 1	Low k	160	144	1.8
Metal 2	Low k	160	144	1.8
Metal 3	Low k	160	144	1.8
Metal 4	Low k	240	216	1.8
Metal 5	Low k	280	252	1.8
Metal 6	Low k	360	324	1.8
Metal 7	Low k	560	504	1.8
Metal 8	SiO_2	810	720	1.8
Metal 9	Polymer	30.5μm	7μm	0.4

(Equivalent to Table 6.1)



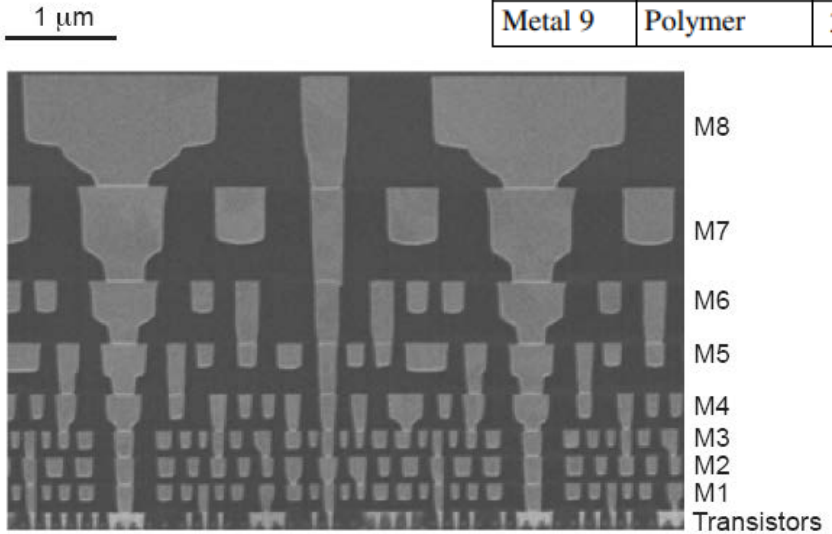


Fig. 6.2

6.2. Interconnect modeling (1)

- Lumped element models
  - A wire is a distributed circuit with a resistance and capacitance per unit length.

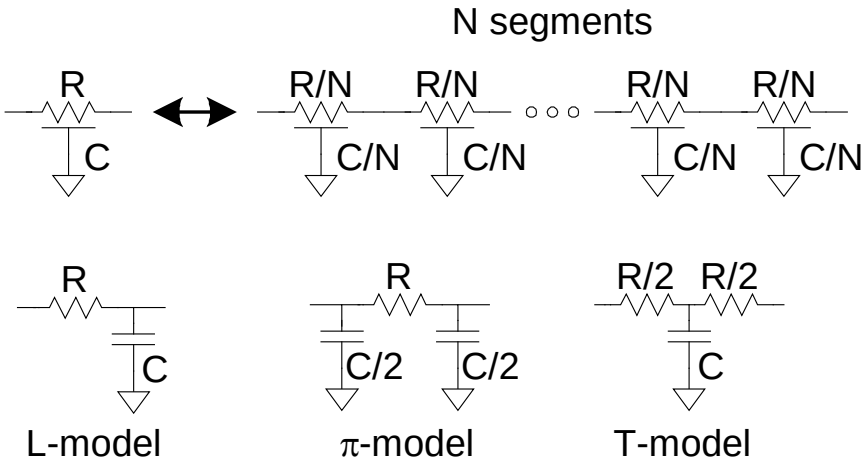


Fig. 6.5

6.2. Interconnect modeling (2)

- Wire resistance
  - Resistance

$$R = \frac{\rho}{t}\frac{l}{w} \qquad \text{Eq. (6.1)}$$

  - With the sheet resistance

$$R = R_{\square}\frac{l}{w} \qquad \text{Eq. (6.2)}$$

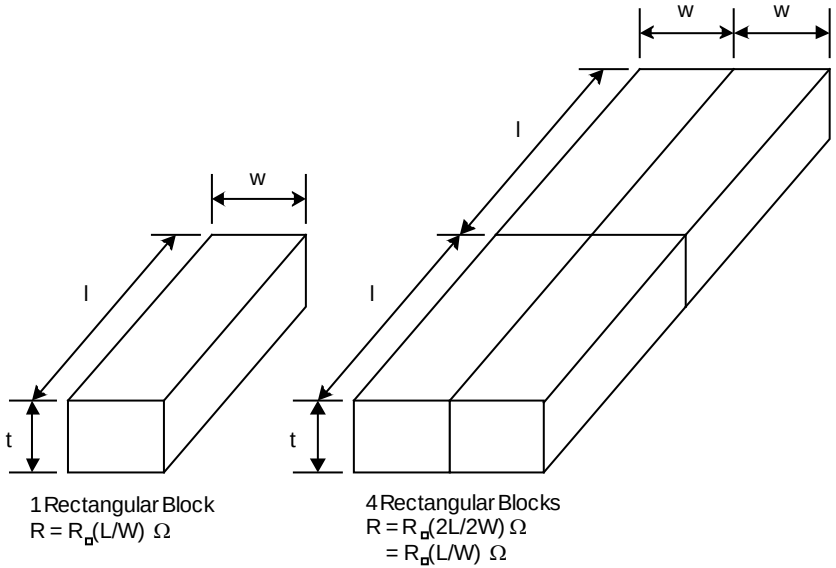


Fig. 6.6

6.2. Interconnect modeling (3)

- Wire resistance
  - Resistance

$$R = \frac{\rho}{t}\frac{l}{w}$$

  - With the sheet resistance

$$R = R_{\square}\frac{l}{w}$$

- Example 6.1
  - Sheet resistance of $0.1\ \Omega/_{\square}$
  - 0.125 μm wide and 1 mm long

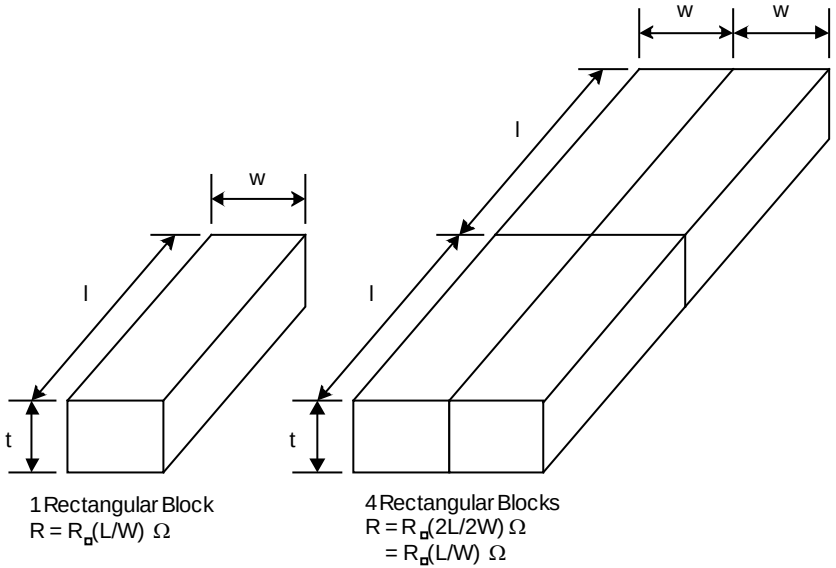


Fig. 6.6

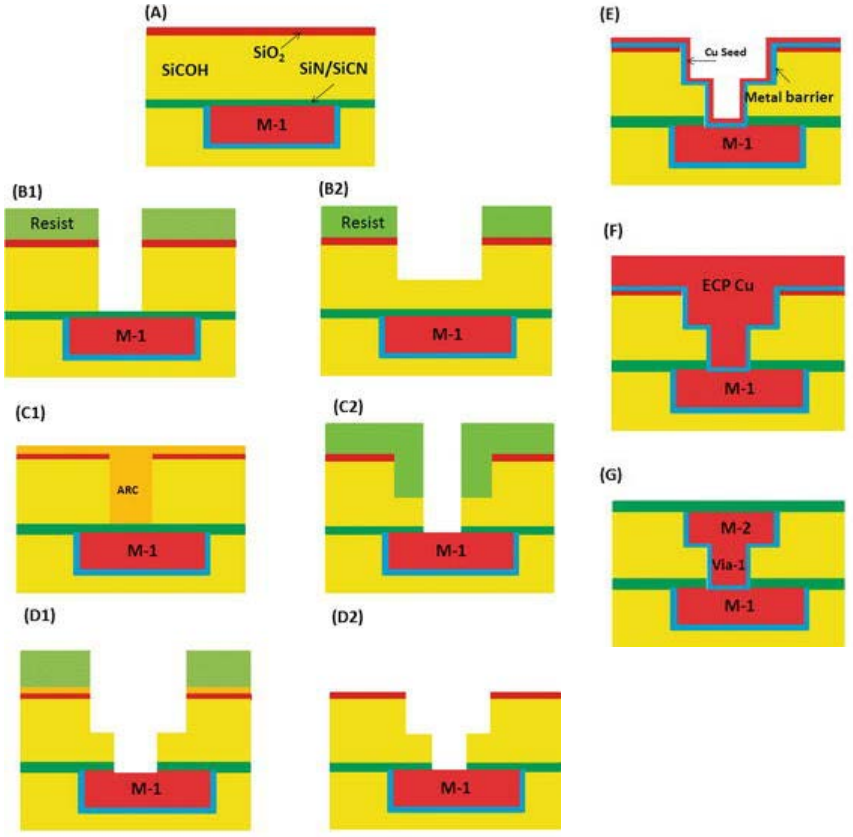
6.2. Interconnet modeling (4)

- Al versus Cu
  - Dual damascene process

Metal	Bulk resistivity (μΩ • cm)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Titanium (Ti)	43.0

Table 6.2

(Cheng et al., “Copper metal for semiconductor interconnects”)



6.2. Interconnect modeling (5)

- Wire capacitance
  - Parallel plate equation, $C = \epsilon_{ox} \frac{A}{d}$

$$C_{total} = C_{top} + C_{bot} + 2C_{adj}$$

$$\approx \epsilon_0 l \left[2k_{vert} \frac{w}{h} + 2k_{horiz} \frac{t}{s} \right] + C_{fringe}$$

Eq. (6.9)

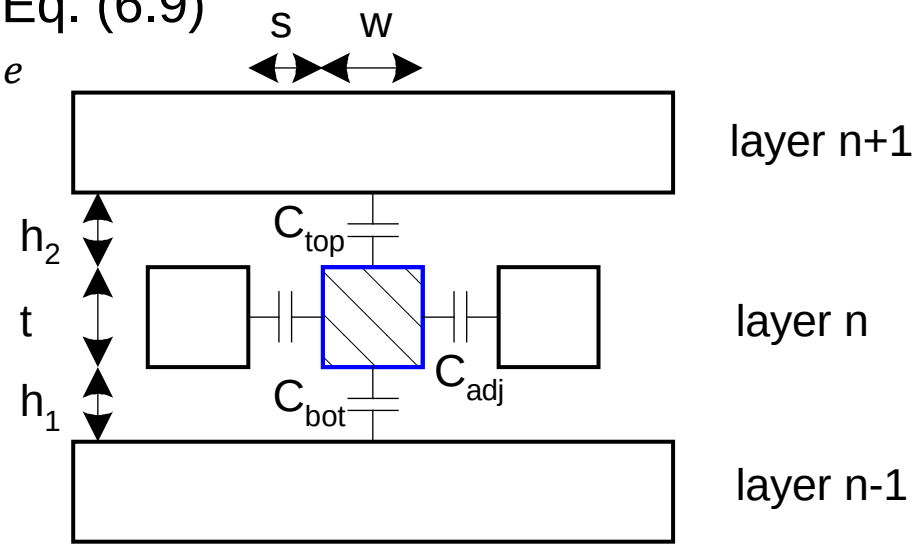


Fig. 6.11

6.2. Interconnect modeling (6)

- M2 capacitance data (180 nm process)
  - Typical dense wires have
  ~ 0.2 fF/μm.

- In practice,
  - The layers above and below the conductor of interest are neither solid planes nor totally empty.

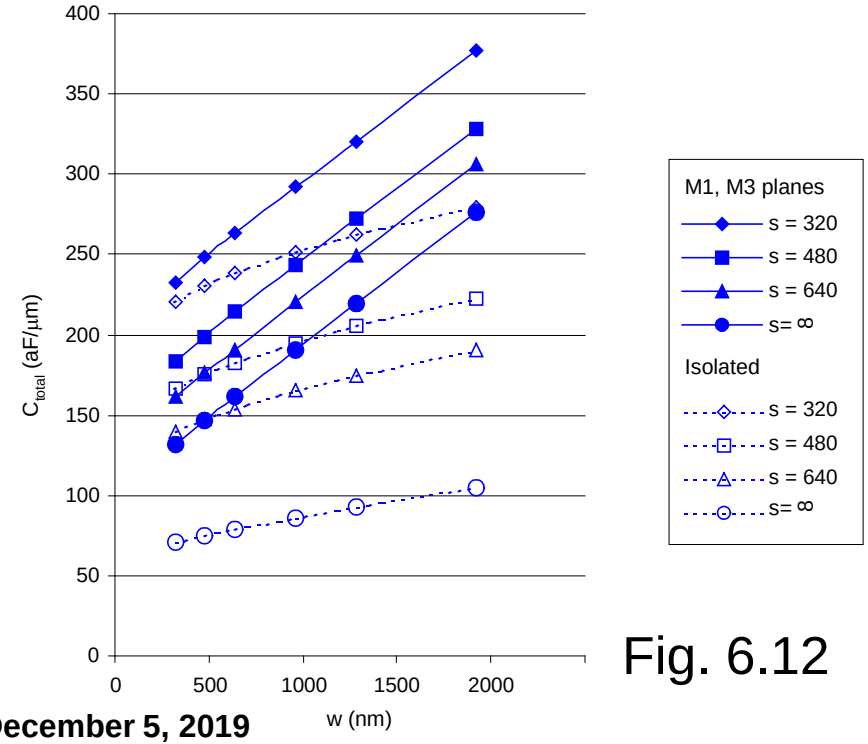


Fig. 6.12

6.3. Interconnect impact (1)

- Example 6.3
  - Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 1 mm wire. (It was considered in Example 6.1.)
  - The wire capacitance is 0.2 fF/μm.
  - The unit-sized NMOSFET has R = 10 $k\Omega$ and C = 0.1 fF.
  - Calculate the Elmore delay.

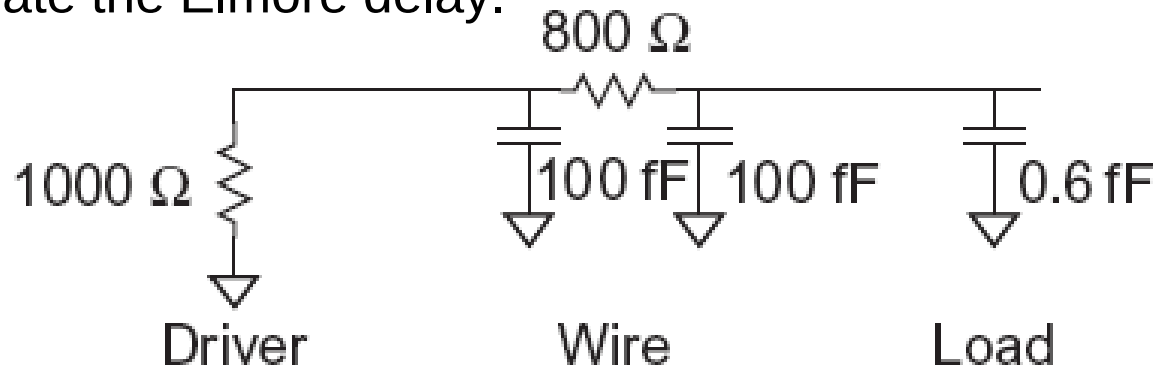


Fig. 6.14

6.3. Interconnect impact (2)

- *Quadratic* dependence of the delay on the length
- Example 6.4
  - The 1 mm-long wire has R = 800 Ω and C = 0.2 pF.
  - When the length is double, both of R and C are doubled.
- N-segement L-model
  - Each segment has r and c. Then, R = N X r and C = N X c.
  - The Elmore delay

$$\sum_{i=1}^{N} irc = rc \sum_{i=1}^{N} i = rc \frac{N(N+1)}{2} \approx \frac{RC}{2}$$

6.3. Interconnect impact (3)

- Long wires have significant capacitance and thus require substantial amounts of energy to switch.
- Example 6.6
  - Estimate the energy per unit length to send a bit of information (one rising and one falling transition) in a CMOS process.
  - Consider the same wire in the previous examples.
  - Assume that V_{DD} is 1 V.
  - E = (0.2 pF/mm)(1.0 V)^2 = 0.2 pJ/bit/mm
    = 0.2 mW/Gbps/mm

6.3. Interconnect impact (4)

- Crosstalk
  - Increased delay on switching wires
  - Noise on non-switching wires
- Crosstalk delay
  - The direction of the switching affects the delay.

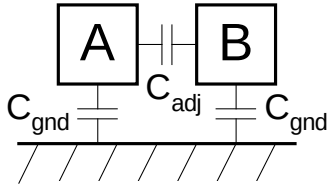


Fig. 6.16

B	**ΔV**	**$C_{eff(A)}$**	**MCF**
Constant	V_{DD}	$C_{gnd} + C_{adj}$	1
Switching with A	0	C_{gnd}	0
Switching opposite A	$2V_{DD}$	$C_{gnd} + 2\ C_{adj}$	2

Table 6.3

6.3. Interconnect impact (5)

- Crosstalk noise
  - In the floating case,

$$\Delta V_{victim} = \frac{C_{adj}}{C_{gnd-v} + C_{adj}} \Delta V_{aggressor}$$

  - Fro the driven victim, the victim noise is reduced.

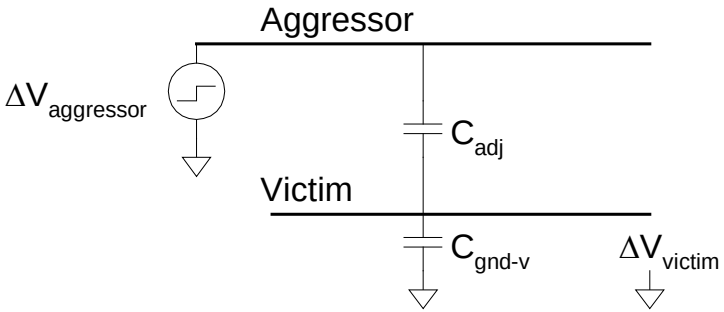


Fig. 6.17

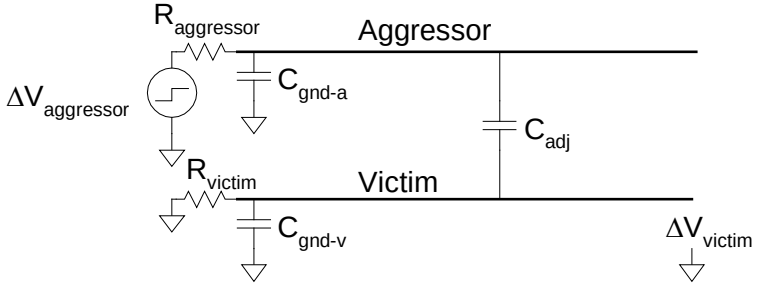


Fig. 6.18

6.3. Interconnect impact (6)

- Simulated with $C_{adj} = C_{victim}$

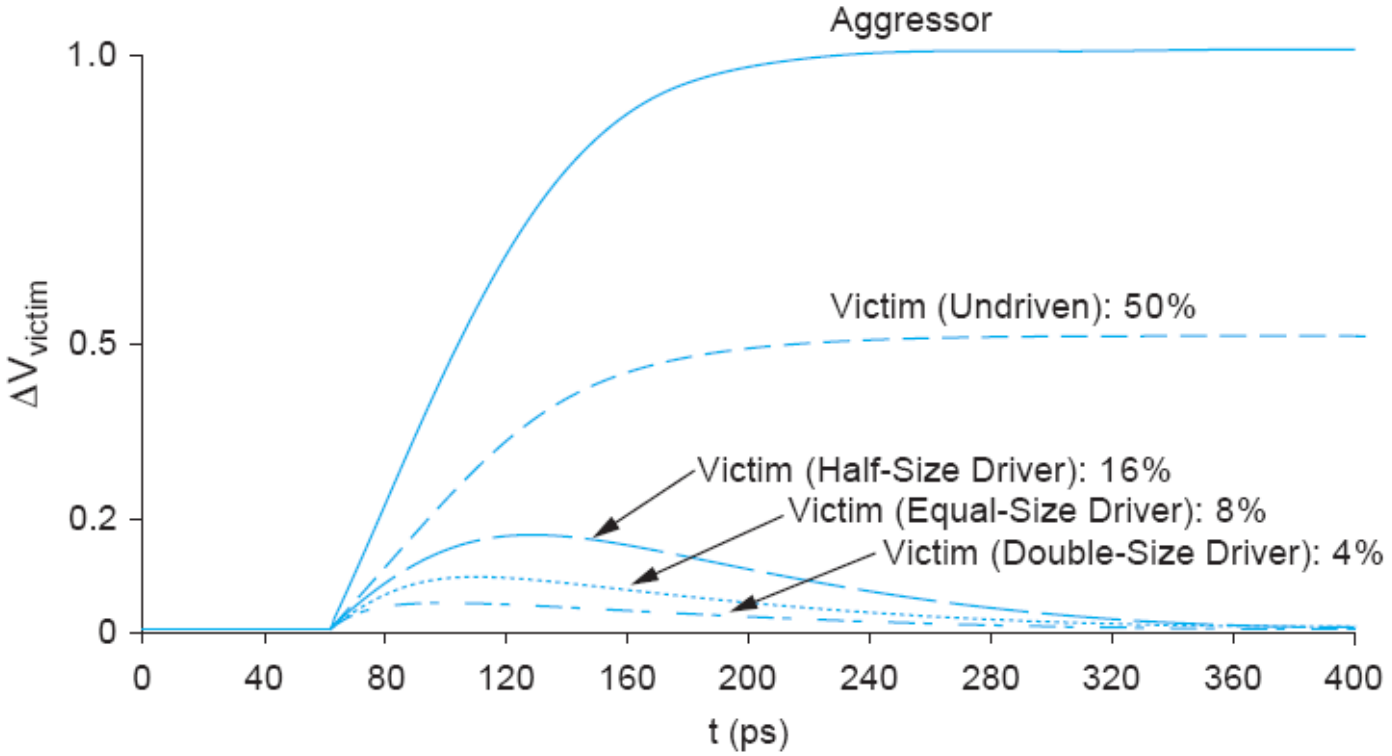


Fig. 6.19