TSMC 0.18um process

Drawn Gate Length (nm)	180
Layers of the metal	6
Layout grid (nm)	5
Vertical pin grid (nm)	560
Horizontal pin grid (nm)	660
Cell power and ground rail width (um)	800

Table. 1 Physical specifications

TSMC offered the world's first 0.18-micron (µm) low power process technology in 1998. Table 1 indicate the physical design specifications of TSMC 180nm process. It has used 1.8V power supply and has 180nm channel length. The minimum layout grid is 5nm and the process supports designs with 6 layers of metal.

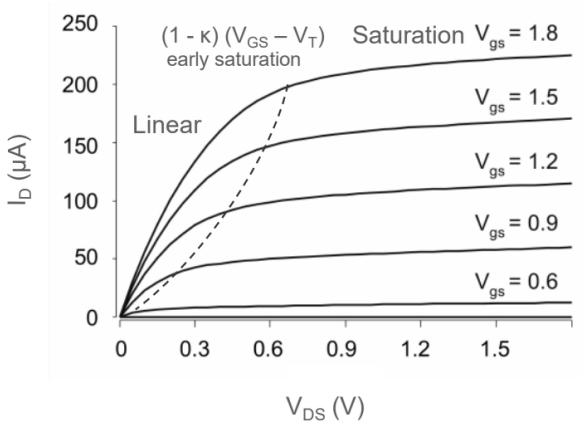

Fig. 1 I_D-V_{DS} characteristic simulation

Fig. 1 is the drain current simulation varied with drain source voltage. The simulation is set with 1.8V VDD and 0.4V threshold voltage and $155\frac{W}{L}$ uA/V^2. The current becomes larger as the gate voltage increases and the current in the saturated area increases since the body effect is applied.

Transistor parasitic	Unit	Value
C_{gP}	fF	2.06
C_{gN}	fF	2.06
C_{sbP}	fF	0.3348
C_{sbN}	fF	0.2016
C_{dbP}	fF	0.3348
C_{dbN}	fF	0.2016
R_{onP}	kΩ	24.111
R_{onN}	kΩ	14.944
V_{thP}	V	0.51
V_{thN}	V	0.53

Table 2. Transistor parasitic value of TSMC 180nm process

Table 2. is the parasitic resistor, capacitance and threshold voltage. Because the value of 180nm is a larger scale compared to the state of the art process, the parasitic capacitance and resistance are relatively high. The propagation delay is proportionate with the parasitic capacitance and turn on resistance. Therefore, it is disadvantage to design a high speed circuit.

Reference

Artisan components, “TSMC 0.18um process 1.8-volt SAGE-X™ Standard Cell Library Data book”

Aileen Davidson, “Introduction to CMOS VLSI design MOS behavior in DSM”