

EC4202-01 Digital IC

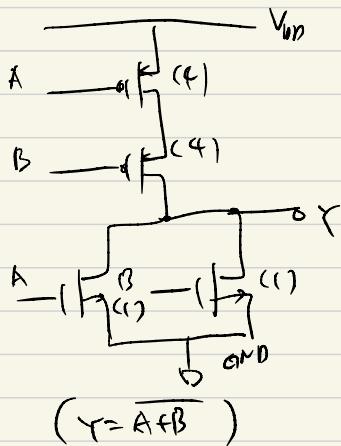
HW#6

Due date : Dec 3rd,2019

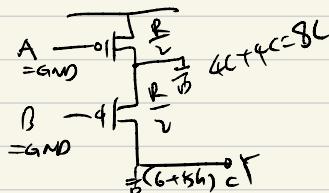
20194044 Park ChangJoo



Ex. 4.1

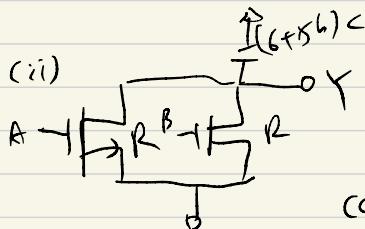


(i) for rising case



$$\begin{aligned} &A \xrightarrow{\text{GND}} \xrightarrow{4C} \xrightarrow{6C} \xrightarrow{5h} \text{GND} \\ &\therefore \text{delay (rise)} = \left(\frac{1}{2}\right)(8C) + \left(\frac{R}{2} + \frac{R}{2}\right)(6+5h)C \\ &= 4RC + R(6+5h)C \\ &= (10+5h)RC \end{aligned}$$

$$\begin{aligned} &\text{(cf) for shared diffusion PMOS case,} \\ &\therefore \text{delay (rise)} = \left(\frac{1}{2}\right)(4C) + (6+5h)RC \\ &= (8+5h)RC \end{aligned}$$



(ii)

$$\begin{aligned} &\therefore \text{delay (fall)} = R \cdot (6+5h)C \\ &= (6+5h)RC \end{aligned}$$

(cf) for both inputs are H25m,

$$\begin{aligned} &\therefore \text{delay (fall)} = \left(\frac{R}{2}/\frac{R}{2}\right)(6+5h)C \\ &= (3+2.5h)RC \end{aligned}$$

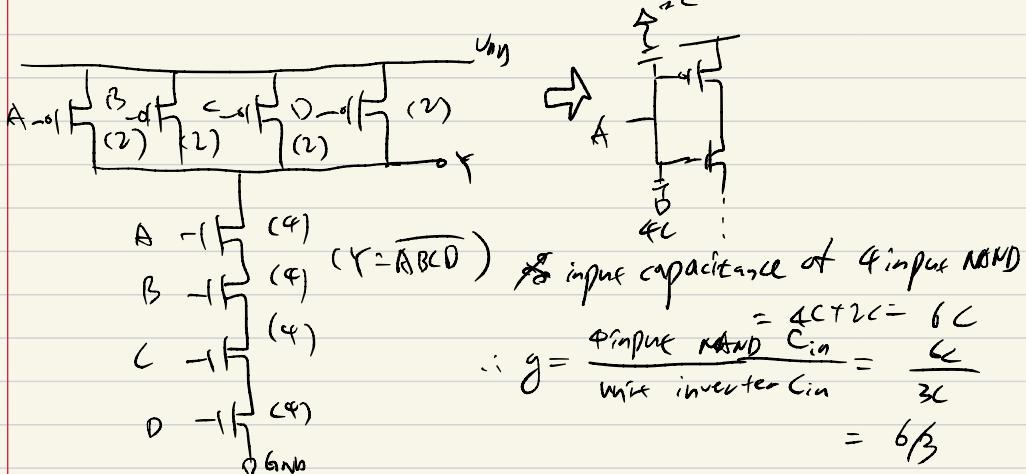
Ex 4.4

$$\begin{cases} C_{\text{concap}} = 3nC \\ C_{\text{intercon}} = 2nC \\ R_{\text{PMOS}} = \frac{R}{n} \end{cases}$$

(n: number of NOR inputs)

$$\begin{aligned} &\therefore t_{pd} = R(3nC) + \sum_{k=1}^{n-1} k \cdot \left(\frac{R}{n}\right) (2nC) \\ &= (n^2 + 2n)RC \end{aligned}$$

Ex 4.9



Ex 4.10

$$(a) \begin{cases} H=6 \\ B=1 \\ P=1+2=3 \\ G=(4/3)(1)=4/3 \end{cases}$$

$$F = GHN = 8$$

$$f = \sqrt{F} \approx 2.8$$

$$\begin{cases} D = nf + p = 2(2.8) + 3 \\ = 8.62 \\ C_{in,r} = (6C) \cdot \frac{1}{f} = 2.14C \end{cases}$$

$$\therefore (C_{in,r}) \cdot f = (C_{out} \cdot g) \quad \therefore D(a) < D(b)$$

$$(b) \begin{cases} H=6 \\ B=1 \\ P=1+2=3 \\ G=(1)(5/3)=\frac{5}{3} \end{cases}$$

$$F = GHN = 10$$

$$f = \sqrt{10} \approx 3.2$$

$$\begin{cases} D = nf + p = 2(3.2) + 3 = 9.42 \\ C_{in,r} = (6C) \cdot \frac{5/3}{f} \approx 3.16C \end{cases}$$

$\therefore \text{"design (a)" is faster than "design (b)"}$

Ex(4.11)

$$D = Nf + P = N(F)^{1/N} + P = N(BN)^{1/N} + P = N(BN)^{1/N} + P$$

$$(B=1)$$

design	G	P	N	$D_{(n=1)}$	$D_{(n=5)}$	$D_{(n=20)}$
(a)	$\frac{(6+2)C}{3L} \cdot 1 = \frac{8}{3}$	$6+1=7$	2	10.3	14.3	21.6
(b)	$\frac{(3+2)C}{3L} \cdot \frac{5}{7} = \frac{25}{9}$	$3+2=5$	2	8.3	12.5	19.9
(c)	$\left(\frac{4}{3}\right)\left(\frac{1}{3}\right) = \frac{28}{9}$	$2+3=5$	2	8.5	12.9	20.8
(d)	$\left(\frac{5}{3}\right)(1)\left(\frac{4}{3}\right)(1) = \frac{20}{9}$	$3+1+2+1=7$	4	11.8	14.3	19.3

{ (b) design is the fastest for "H=1" and "H=5".
 { (d) design is the fastest for "H=20".
 \therefore (d) design has the lowest logical effort
 and more stages to drive the larger path effort)

Ex(5.1)

$$\left\{ \begin{array}{l} \alpha = 0.1 \\ C = 450 \mu F, T_0 = 31.5 \mu F \\ V_{DD} = 0.9V \\ f = 450 \mu Hz \end{array} \right.$$

\therefore Dynamic = $\alpha C V_{DD}^2 f$
 $= (0.1) \times 31.5 \mu F \times (0.9)^2 \times (450 \mu Hz)$
 $\approx 1.15 \text{ W}$

Ex(5.4)

the signal has 4 transitions in 10 clock edges & 15 ns delay.

$$\therefore K = \left(\frac{f}{2}\right) \left(\frac{4}{10}\right) = 0.2$$

Ex(5.5)

A two-stage design consumes the lowest energy because it has the smallest amount of switching hardware.

$$\text{delay: } d = \epsilon f \frac{64}{x} + 2 \quad (\because \text{sizes are "1" and "X"})$$

$$= 202$$

$$x^2 - 18x + 64 \geq 0$$

$$\therefore x = \frac{18t \sqrt{324 - 256}}{2}$$

$$\approx 9 \pm 4.12$$

$$= 13.12, 4.88$$

$\therefore x = 4.88$ (for smallest size)

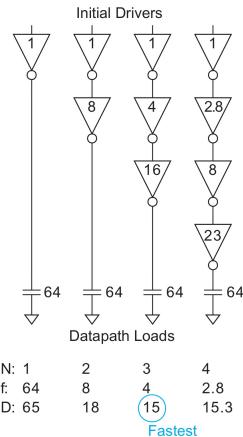


FIGURE 4.33 Comparison of different number of stages of buffers

Ex(5.6)

(i) 2 stage

$$\left\{ \begin{array}{l} d = \epsilon f \frac{500}{x} + 2 = 302 \\ \epsilon = 1 + x \end{array} \right. \Rightarrow x^2 - 28x + 500 = 0$$

$$x = \frac{28t \sqrt{(28)^2 - 500}}{2} \approx 30.85, -2.85$$

\therefore delay constraint cannot be met
($\because x < 0$)

(ii) 3 stage

$$\left\{ \begin{array}{l} d = \epsilon f \frac{4}{x} + \frac{500}{y} + 3 = 302 \\ \epsilon = 1 + xy \end{array} \right. \Rightarrow x^2y + y^2 + 500x - 21xy = 0$$

(for $x = 5$)

$$25y + y^2 + 500 - 105y = 0$$

$$\therefore y = 32.09$$

$$\therefore \epsilon = 38.09$$

(iii) 4 stage

$$\left\{ \begin{array}{l} d = \epsilon f \frac{x}{k} + \frac{500}{z} + 4 = 302 \\ \epsilon = 1 + x + y + z \end{array} \right. \Rightarrow x^2yz + y^2z + xz^2 + 500xy - 26xyz = 0$$

$$\left\{ \begin{array}{l} x = 2.15 \\ y = 6.23 \\ z = 31.43 \end{array} \right. \Rightarrow \epsilon = 40.81$$

\therefore 3-stage consumes the lowest energy (32.09)