# DIC L13: Delay (1)

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

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# 2.5. DC transfer (14)

- Noise margin

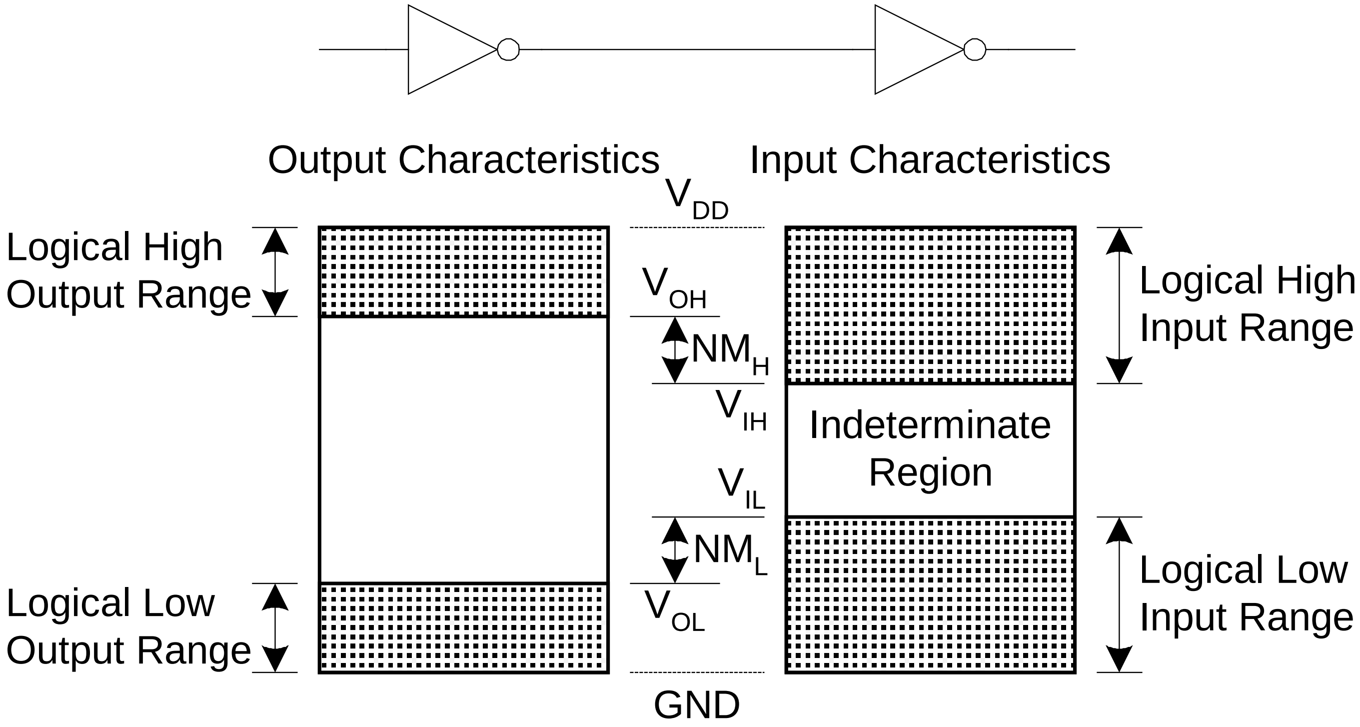



Fig. 2.29

# 2.5. DC transfer (15)

- Unity gain points
  - Two unity gain points
  - $(V_{IL}, V_{OH})$
  - $(V_{IH}, V_{OL})$

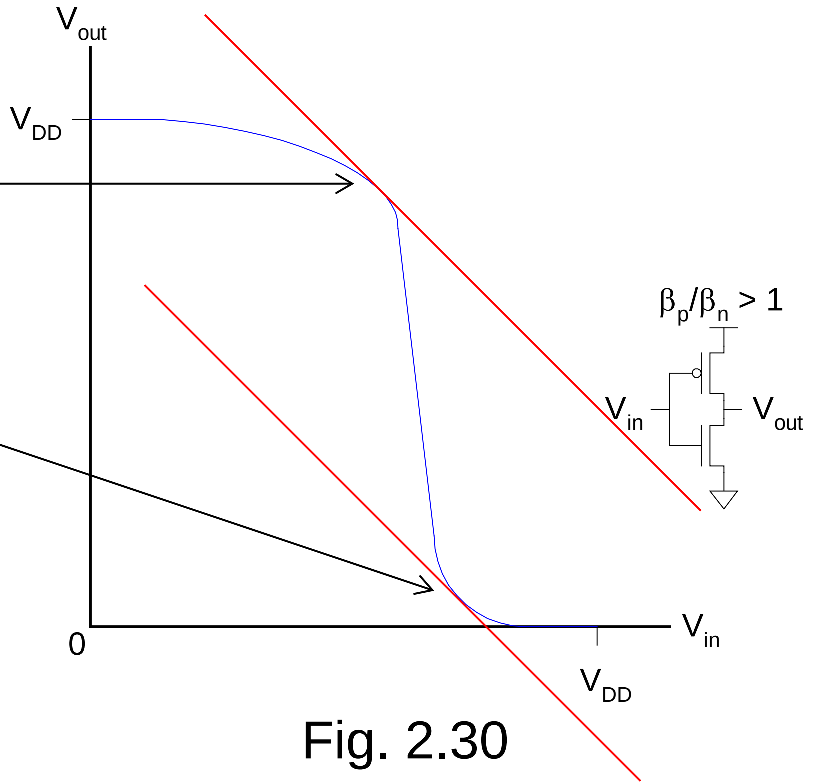



Fig. 2.30

# 2.5. DC transfer (16)

- Calculate $\frac{dV_{out}}{dV_{in}}$ with the channel length modulation
  - Assume the NMOS current.

$$I_{dn} = W_n C_{ox} v_{sat-n}(V_{in} - V_{tn})(1 + \lambda_n V_{out})$$

  - Assume the PMOS current.

$$I_{dp} = -W_p C_{ox} v_{sat-p}\left(V_{in} - V_{DD} - V_{tp}\right)\left(1 + \lambda_p(V_{out} - V_{DD})\right)$$

  - What is the determining factor for $\frac{dV_{out}}{dV_{in}}$?

# 2.5. DC transfer (17)

- Pass transistor

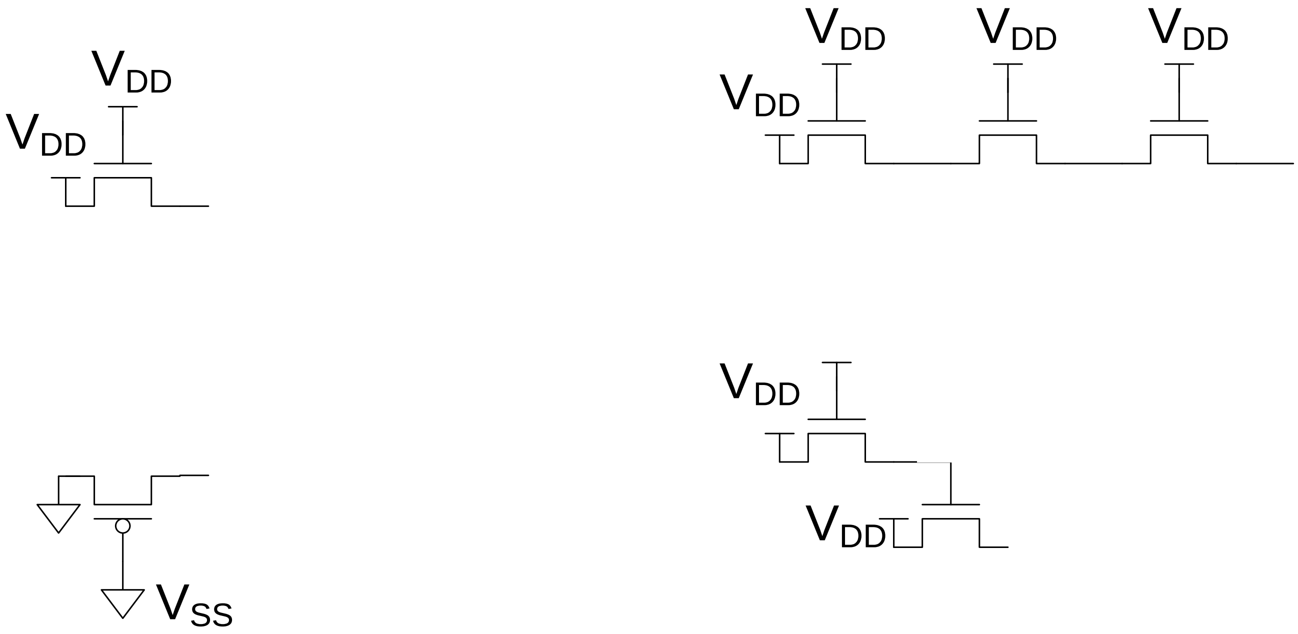



Fig. 2.31

# 4.1. Introduction (1)

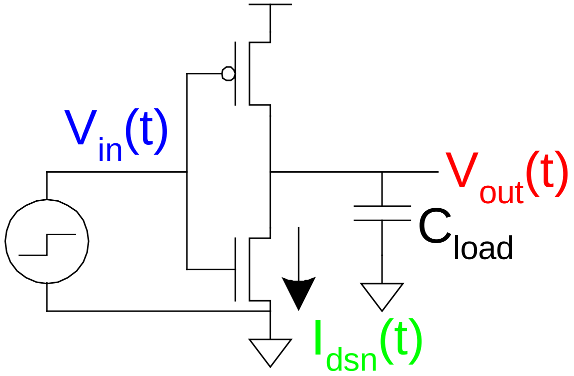
- Transient response
  - DC analysis: $V_{out}$ if $V_{in}$ is a constant
  - Transient analysis: $V_{out}(t)$ if $V_{in}(t)$ changes
  - A set of differential equations should be solved.
  - Input is usually considered to be a step or ramp.
    - From 0 to $V_{DD}$ or vice versa

# 4.1. Introduction (2)

$$V_{in}(t) =$$

$$V_{out}(t < t_0) =$$

$$\frac{dV_{out}(t)}{dt} =$$




$$I_{dsn}(t) = \begin{cases} & t \le t_0 \\ & V_{out} > V_{DD} - V_t \\ & V_{out} < V_{DD} - V_t \end{cases}$$

# 4.1. Introduction (3)

- Definitions
  - **$t_{pdr}$**: *rising propagation delay*
    - From input to rising output crossing $V_{DD}/2$
  - **$t_{pdf}$**: *falling propagation delay*
    - From input to falling output crossing $V_{DD}/2$
  - **$t_{pd}$**: *average propagation delay*, $t_{pd} = (t_{pdr} + t_{pdf})/2$
  - **$t_r$**: *rise time*
    - From output crossing 0.2 $V_{DD}$ to 0.8 $V_{DD}$
  - **$t_f$**: *fall time*
    - From output crossing 0.8 $V_{DD}$ to 0.2 $V_{DD}$

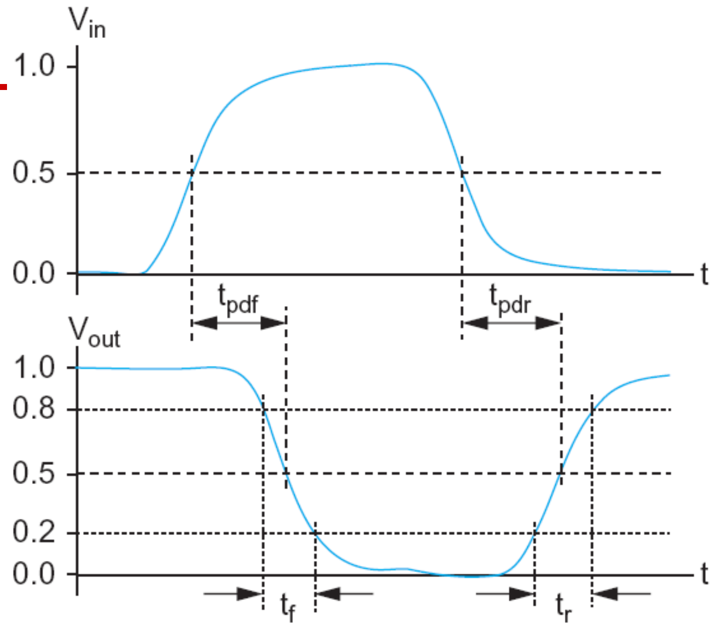



Fig. 4.1