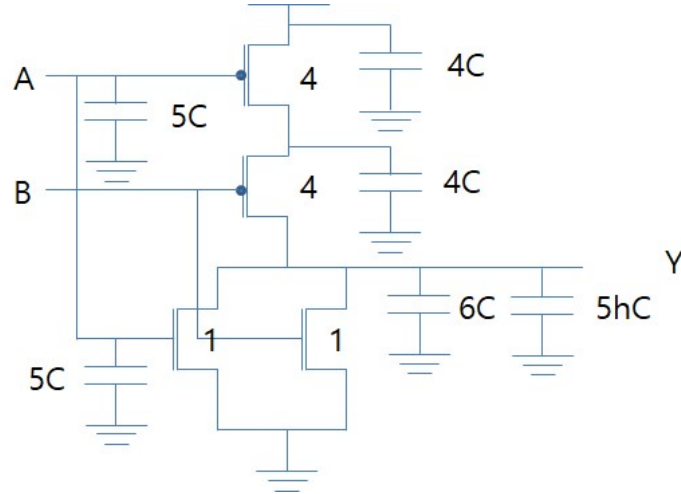


4.1



$$t_{rising} = \frac{R}{2} \times (4C + 4C) + R \times (6C + 5hC) = (10 + 5h)RC$$

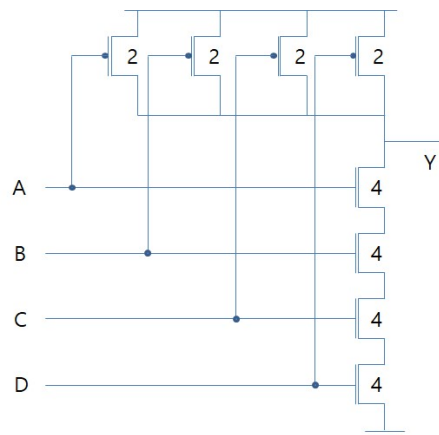
$$t_{falling} = R \times (6C + 5hC) = (6 + 5h)RC$$

4.4

Each of Pull-up network elements (PMOS) has R/n , and Pull-down network elements (NMOS) has R . Also Input node has $2nC$, and output node has $3nC$. Then the propagation delay is

$$t_{pd} = \sum_{i=1}^{n-1} \left(\frac{R}{n} i \right) (2nC) + R(3nC) = (n^2 + 2n)RC$$

4.9



$$g = (2 + 4) / (1 + 2) = 6/3$$

4.10

$$H = 6, P = 3, B = 1$$

(a)

$$F = GBH = 8$$

$$f = \sqrt{F} = 2.83$$

$$D = 2f + P = 8.66$$

(b)

$$F = GBH = 10$$

$$f = \sqrt{F} = 3.16$$

$$D = 2f + P = 9.32$$

Therefore (a) is faster than (b).

4.11

For (a),

$$G = 8/3, P = 7, N = 2$$

$$D_{H=1} = 2(8/3 \times 1)^{\frac{1}{2}} + 7 = 10.3$$

$$D_{H=5} = 2(8/3 \times 5)^{\frac{1}{2}} + 7 = 14.3$$

$$D_{H=20} = 2(8/3 \times 20)^{\frac{1}{2}} + 7 = 21.6$$

For (b),

$$G = 5/3 \times 5/3, P = 5, N = 2$$

$$D_{H=1} = 2(5/3 \times 5/3 \times 1)^{\frac{1}{2}} + 5 = 8.3$$

$$D_{H=5} = 2(5/3 \times 5/3 \times 5)^{\frac{1}{2}} + 5 = 12.5$$

$$D_{H=20} = 2(5/3 \times 5/3 \times 20)^{\frac{1}{2}} + 5 = 19.9$$

For (c),

$$G = 4/3 \times 7/3, P = 5, N = 2$$

$$D_{H=1} = 2(4/3 \times 7/3 \times 1)^{\frac{1}{2}} + 5 = 8.5$$

$$D_{H=5} = 2(4/3 \times 7/3 \times 5)^{\frac{1}{2}} + 5 = 12.9$$

$$D_{H=20} = 2(4/3 \times 7/3 \times 20)^{\frac{1}{2}} + 5 = 20.8$$

For (d),

$$G = 5/3 \times 1 \times 4/3 \times 1, P = 7, N = 4$$

$$D_{H=1} = 4(5/3 \times 1 \times 4/3 \times 1 \times 1)^{\frac{1}{4}} + 5 = 11.8$$

$$D_{H=5} = 4(5/3 \times 1 \times 4/3 \times 1 \times 5)^{\frac{1}{4}} + 5 = 14.3$$

$$D_{H=20} = 4(5/3 \times 1 \times 4/3 \times 1 \times 20)^{\frac{1}{4}} + 5 = 17.3$$

H=1, H=5, (b) is fastest.

H=20, (d) is fastest.

5.1

$$P = 0.1 \times (450 \times 10^{-12} \times 70) \times (0.9)^2 \times 450 \times 10^6 = 1.08 \text{ W}$$

5.4

Since there are 2 rising edges for 10ns, $(2/10) = 0.2$

5.5

Use only two inverter for buffer since we make the least power consumption to spend each inverter.

$$d = x + 64/x + 2 = 20$$

$$\therefore x = 4.88$$

5.6

(2stage)

$$d = x + 500/x + 2 = 20, E = 1 + x$$

There is no answer for x.

(3stage)

$$d = x + y/x + 500/y + 3, E = 1 + x + y$$

$$x = 5, y = 32.09, E = 38.09$$

(4stage)

$$d = x + y/x + z/y + 500/z + 4, E = 1 + x + y + z$$

$$x = 2.15, y = 6.23, z = 31.43, E = 39.81$$

Therefore, 3stage design is best for power efficiency.