DIC L12: Inverter (2)

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2.5. DC transfer (9)

- Input threshold, V_{inv} (or swithcing threshold)
  - When $V_{in} = V_{out} = V_{inv}$
- Beta ratio
  - Skewed
  - HI-skewed, $\frac{\beta_p}{\beta_n} > 1$
    - Stronger PMOS
  - LO-skewed, $\frac{\beta_p}{\beta_n} < 1$
    - Weaker PMOS

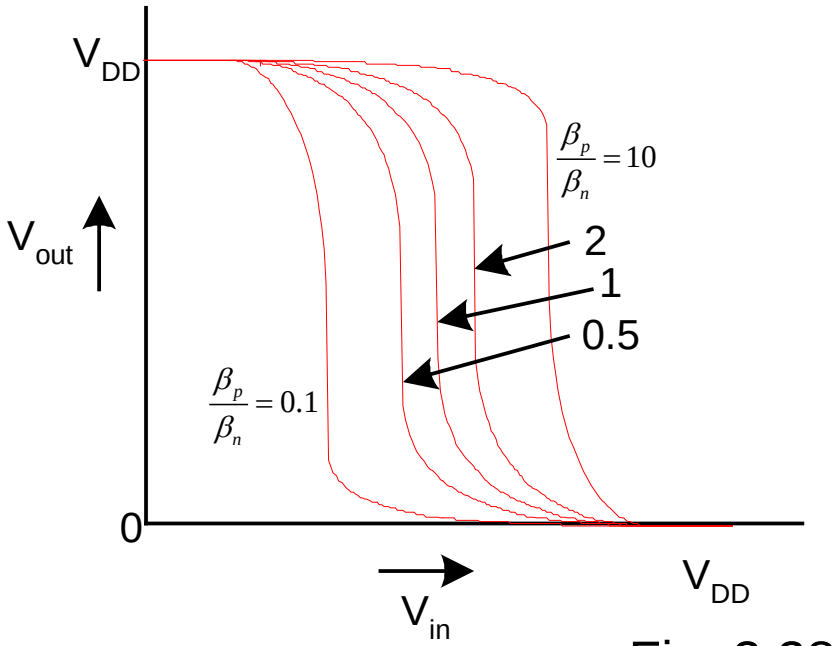


Fig. 2.28

2.5. DC transfer (10)

- Quantitative analysis

$$I_{dn} = \frac{\beta_n}{2}(V_{inv} - V_{tn})^2$$

$$I_{dp} = -\frac{\beta_p}{2}(V_{inv} - V_{DD} - V_{tp})^2$$

  - After manipulation, we have

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}} \qquad \text{Eq. (2.55)}$$

  - For a special case with $r = 1$, $V_{inv} = \frac{V_{DD}+V_{tn}+V_{tp}}{2}$

2.5. DC transfer (11)

- Quantitative analysis with velocity saturation

$$I_{dn} = W_n C_{ox} v_{sat-n}(V_{inv} - V_{tn})$$
$$I_{dp} = -W_p C_{ox} v_{sat-p}(V_{inv} - V_{DD} - V_{tp})$$

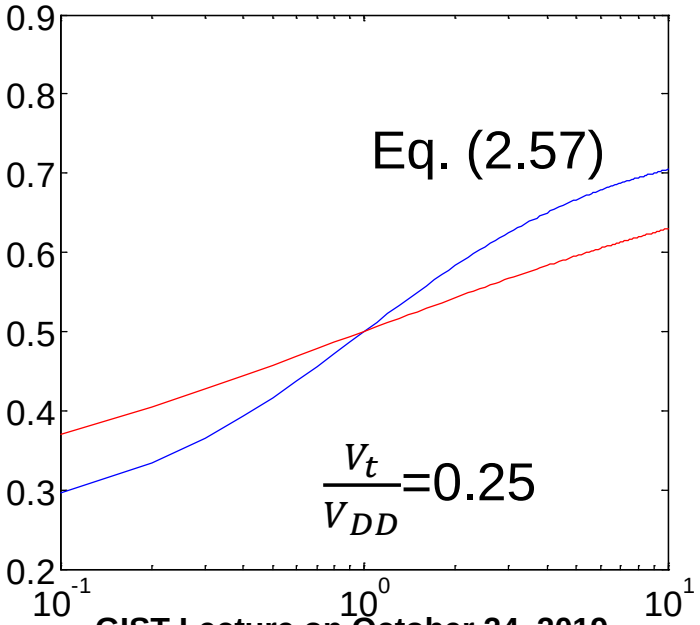
  - After manipulation, we have

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}} \qquad \text{Eq. (2.57)}$$

  - (Here, $r = \frac{W_p v_{sat-p}}{W_n v_{sat-n}}$)
  - For a special case with $r = 1$, $V_{inv} = \frac{V_{DD}+V_{tn}+V_{tp}}{2}$

2.5. DC transfer (12)

- Eq. (2.55) and Eq. (2.57)
  - Let's draw $\frac{V_{inv}}{V_{DD}}$ as a function of r. Assume that $V_t = V_{tn} = -V_{tp}$.



2.5. DC transfer (13)

- Noise margin

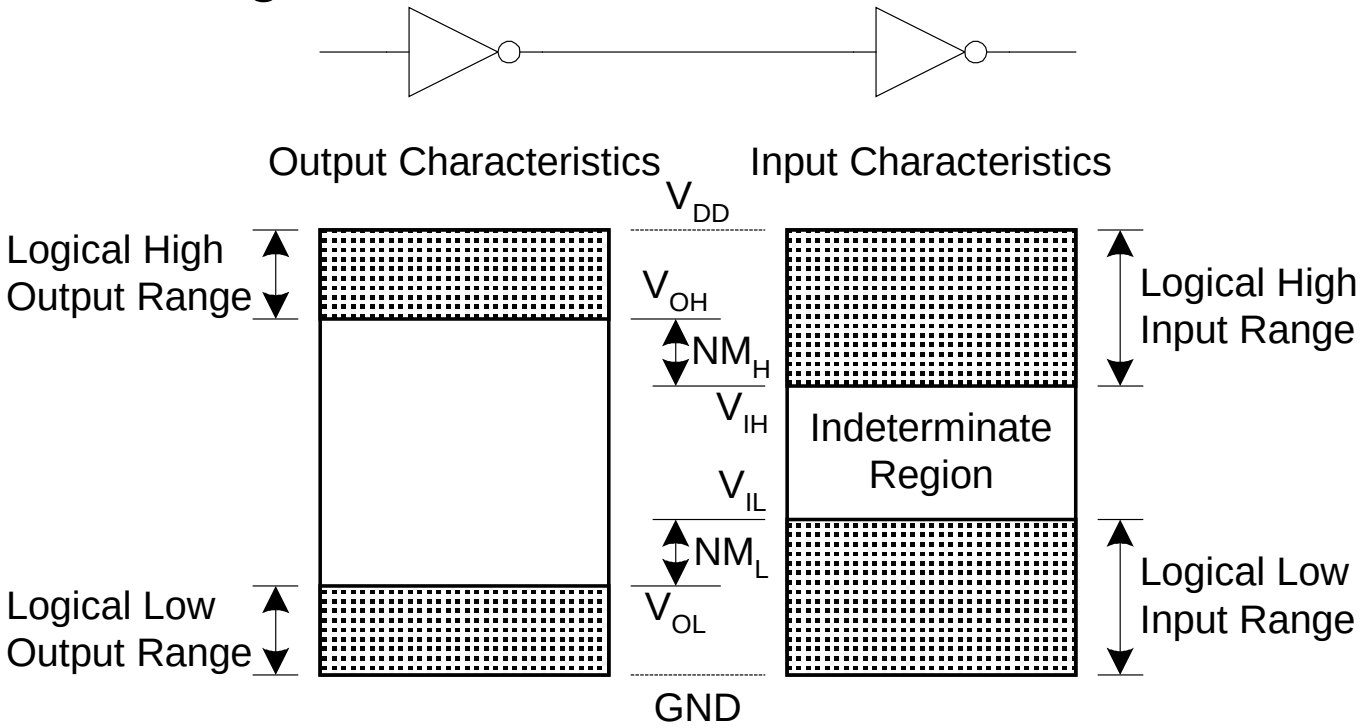


Fig. 2.29

2.5. DC transfer (12)

- Unity gain points
  - Two unity gain points
  - V_{IL}
  - V_{IH}

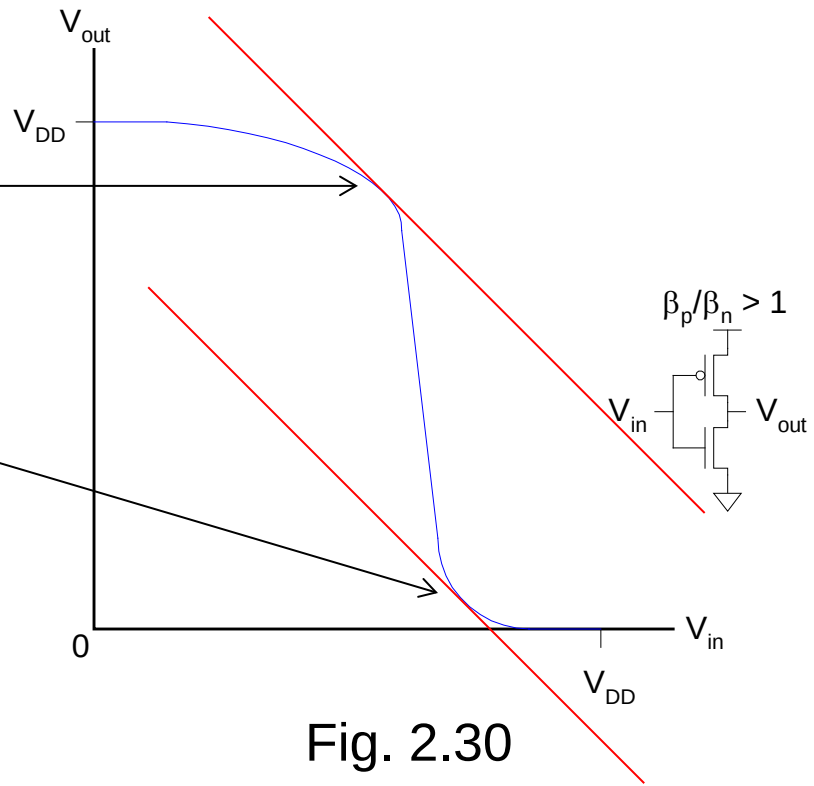


Fig. 2.30

2.5. DC transfer (13)

- Pass transistor

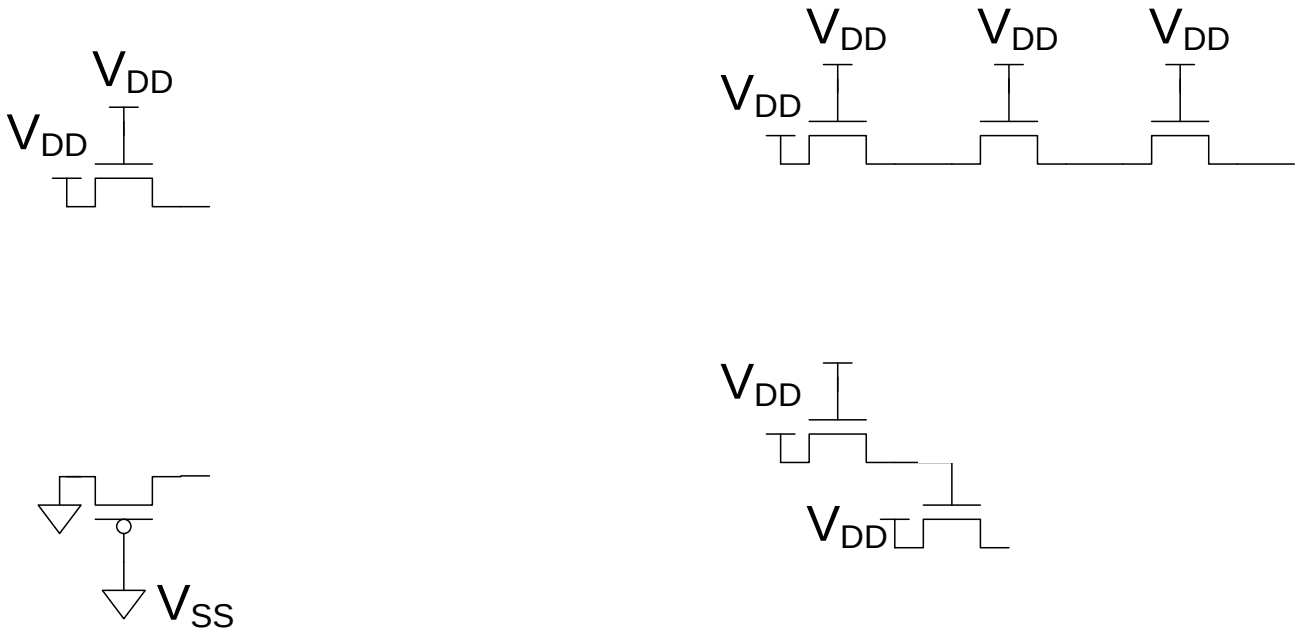


Fig. 2.31