Digital Integrated Circuit
Lecture 14 Delay

Sung-Min Hong (smhong@gist.ac.kr)
Semiconductor Device Simulation Laboratory
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

Review of Previous Lecture

Lecture 13

- Analytic solution of Homework#4
  - The transfer function (to V_2) is given by

$$H(s) = \frac{1}{\tau_1 \tau_2} \frac{1}{\left(s + \frac{1}{\tau_1}\right)\left(s + \frac{1}{\tau_2}\right)}$$

  where $\tau_1 = \frac{3+\sqrt{5}}{2} RC$ and $\tau_2 = \frac{3-\sqrt{5}}{2} RC$.

  - The step response, $V_2(s)$, is written as

$$V_2(s) = \frac{1}{\tau_1 \tau_2} \frac{1}{\left(s + \frac{1}{\tau_1}\right)\left(s + \frac{1}{\tau_2}\right)s}$$

Lecture 13

- Analytic solution of Homework#4
  - It can be re-written as as

$$V_2(s) = -\frac{\tau_1}{\tau_1 - \tau_2}\frac{1}{s + \frac{1}{\tau_1}} + \frac{\tau_2}{\tau_1 - \tau_2}\frac{1}{s + \frac{1}{\tau_2}} + \frac{1}{s}$$

  - By the inverse transform,

$$V_2(t) = -\frac{\tau_1}{\tau_1 - \tau_2}e^{-\frac{t}{\tau_1}} + \frac{\tau_2}{\tau_1 - \tau_2}e^{-\frac{t}{\tau_2}} + u(t)$$

  - In our problem, $V_{in}(t) = 1 - u(t)$. Therefore,

$$V_2(t) = \frac{\tau_1}{\tau_1 - \tau_2}e^{-\frac{t}{\tau_1}} - \frac{\tau_2}{\tau_1 - \tau_2}e^{-\frac{t}{\tau_2}}$$

Lecture 13

- Parasitic delay of a 2-input NAND gate
  - Why $p = 2$?

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n
Tristate / mux	2	4	6	8	2n
XOR, XNOR		4	6	8	

Lecture 13

- Effort delay, f, explained again
  - Consider a logic gate, whose width is k times wider than the unit one.
  - Simply speaking, τ due to the effort is written as

$$\tau = \frac{R}{k}\, C_{out}$$

  - By introducing the electrical effort, $h = \frac{C_{out}}{C_{in}}$,

$$\tau = \frac{R}{k}\, C_{in}\, h$$

  - The input capacitance, C_{in}, is related with the logical effort:

$$C_{in} = 3C\ g\ k$$

  - Then, $\tau = 3RC\ g\ h$.
  - Therefore, $f = g\ h$.

4.5 Logical Effort of Paths

4.5. Logical effort of paths (1)

- Multistage logic networks
  - Logical effort is independent of size.
  - Electrical effort depends on sizes.

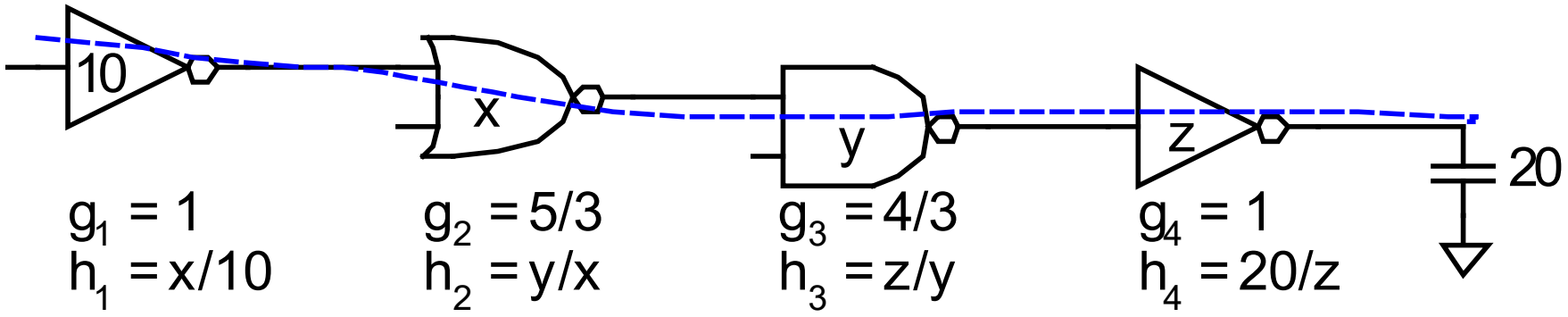


Fig. 4.29

  - What is the total propagation delay?

$$D = \frac{x}{10} + 1 + \frac{5}{3}\frac{y}{x} + 2 + \frac{4}{3}\frac{z}{y} + 2 + \frac{20}{z} + 1$$

4.5. Logical effort of paths (2)

- Minumum propagation delay?
  - Parasitic delay is given as 6.

$$D = 6 + \frac{x}{10} + \frac{5}{3}\frac{y}{x} + \frac{4}{3}\frac{z}{y} + \frac{20}{z}$$

  - Minimize the effort delay.
  - Recall the inequality of arithmetic and geometric means

$$f_1 + f_2 + \cdots + f_N \geq N\sqrt[N]{f_1 f_2 \ldots f_N}$$

The equality holds if and only if $f_1 = f_2 = \cdots = f_N$.

4.5. Logical effort of paths (3)

- Product of effort delays is a constant.
  - In our example,

$$D = 6 + \frac{x}{10} + \frac{5}{3}\frac{y}{x} + \frac{4}{3}\frac{z}{y} + \frac{20}{z} \geq 6 + 4\sqrt[4]{\frac{40}{9}}$$

  - The equality holds when $\frac{x}{10} = \frac{5}{3}\frac{y}{x} = \frac{4}{3}\frac{z}{y} = \frac{20}{z} = \sqrt[4]{\frac{40}{9}} \approx 1.45.$

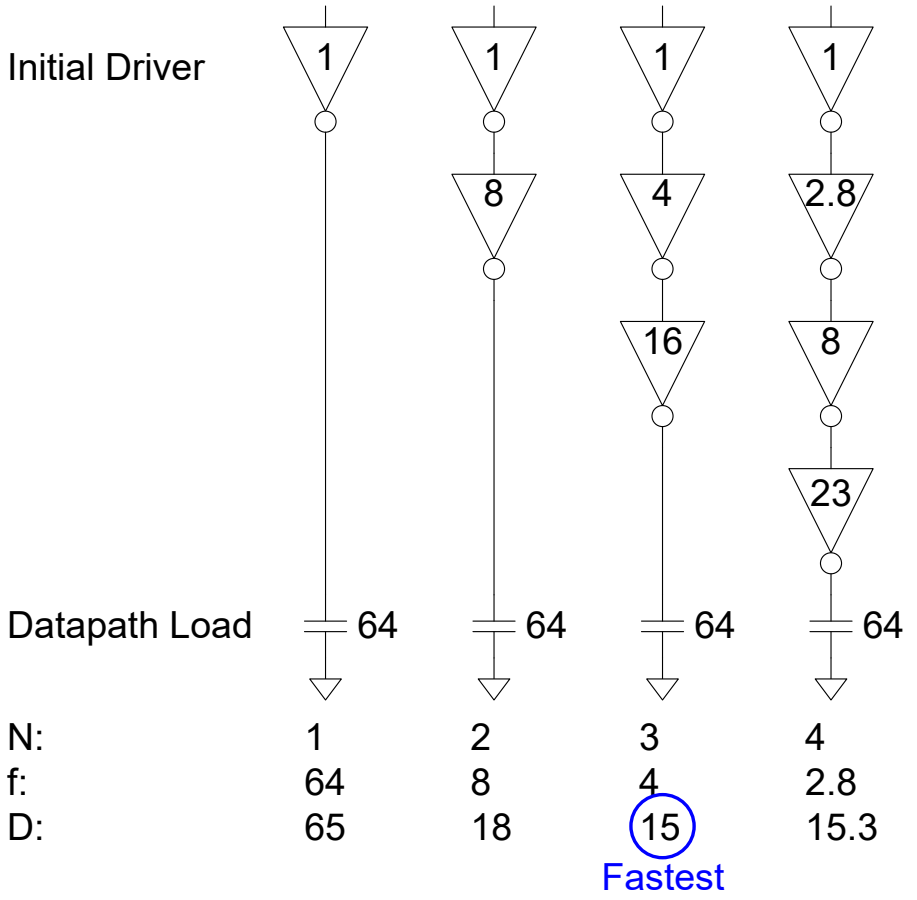
- Minimum possible delay of an N–state path

$$D = N\sqrt[N]{F} + P$$

  - F: Path effort
  - P: Path parasitic delay

4.5. Logical effort of paths (4)

- Exampe 4.14
  - Determine the number of stages.
  - $N = 1: D = 1 + 64$
  - $N = 2: D = 2 + 2\sqrt{64}$
  - $N = 3: D = 3 + 3\sqrt[3]{64}$



Thank you!