Digital Integrated Circuit
Lecture 12 Delay

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Review of Previous Lecture

Lecture 11

- RC model
  - Effective resistance, R
  - Gate capacitance and diffusion capacitances, C
  - Scaling
  - There appears a chain of R and C.

4.3 RC Delay Model

4.3. RC delay model (6)

- Example 4.4
  - Estimate t_{pd} for a “unit” inverter (PMOS width:NMOS width=2:1 & minimum length) driving identical “unit” inverters.
  - Effective resistance is R. (Same for NMOS and PMOS)
  - Capacitance is $(3 + 3m)C$.

$$t_{pd} = (3 + 3m)RC$$

4.3. RC delay model (7)

- Example 4.5
  - The driver is w times unit size.
  - The effective resistance is $\frac{R}{w}$ and the diffusion capacitance is wC.
  - Estimate t_{pd}.

$$t_{pd} = \left(3 + 3\frac{m}{w}\right) RC$$

  - With a fanout of $h = \frac{m}{w}$,

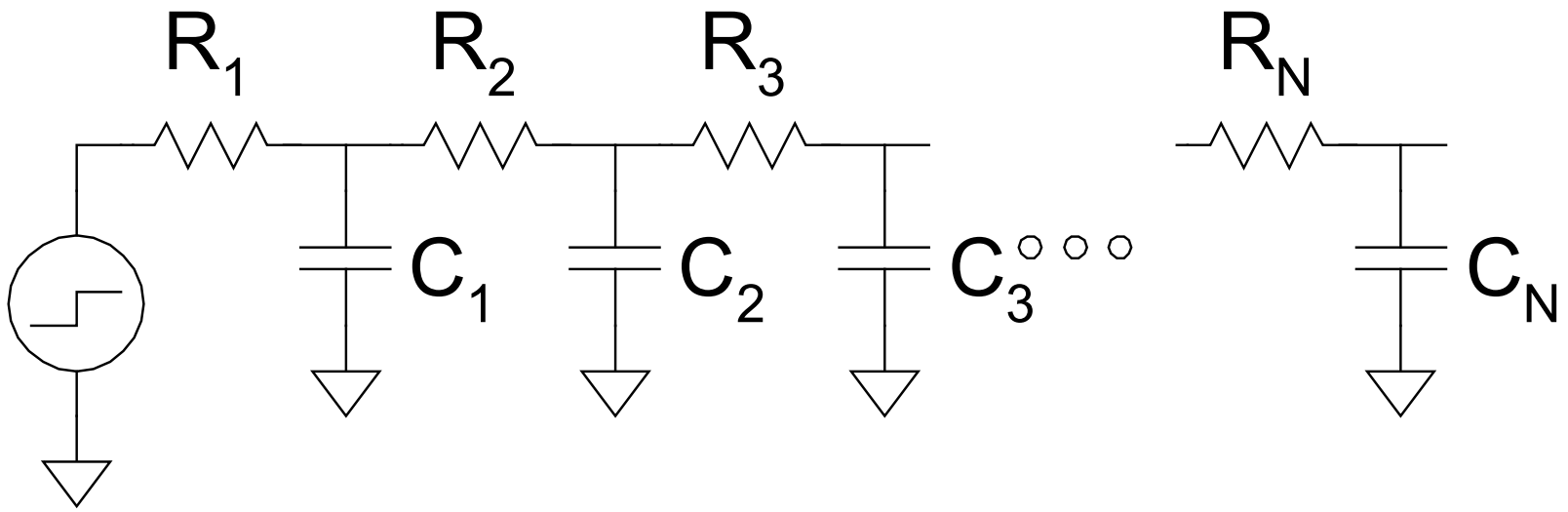
$$t_{pd} = (3 + 3h)RC$$

4.3. RC delay model (8)

- A chain of R and C
  - A simple single time constant approximation

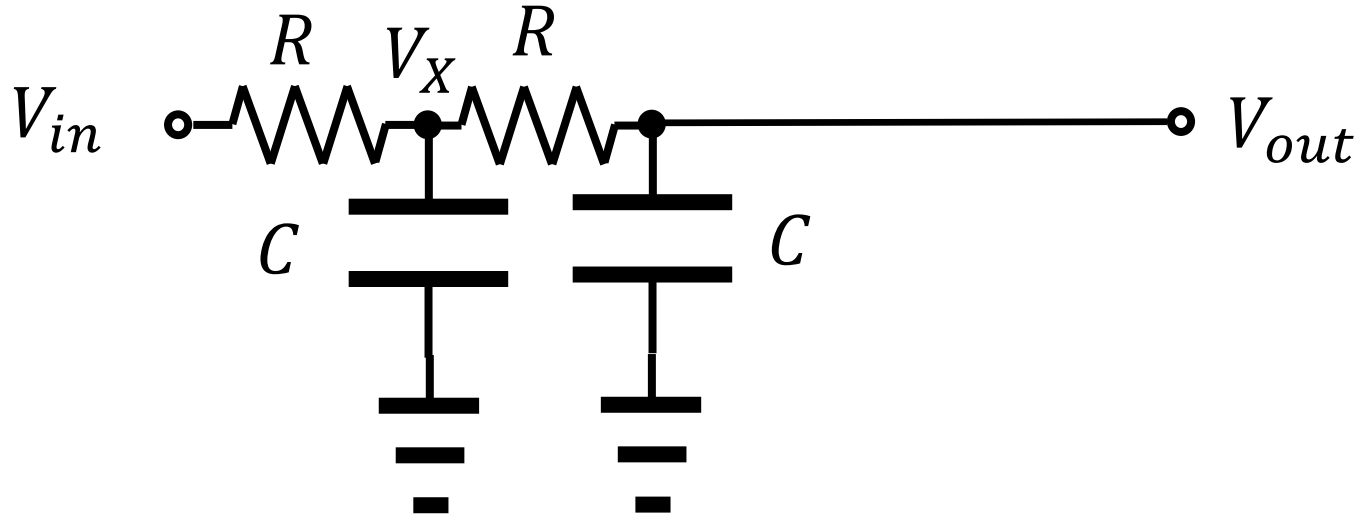
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$



Homework#4

- Due: AM08:00, October 17
- Problem#1
  - Consider a chain of two RC components. Assume that two resistors are the same and two capacitors are the same. At t=0, V_{in} suddenly changes from 1 V to 0 V.
  - Draw the exact response of V_{out} and an approximated one with a single time constant.

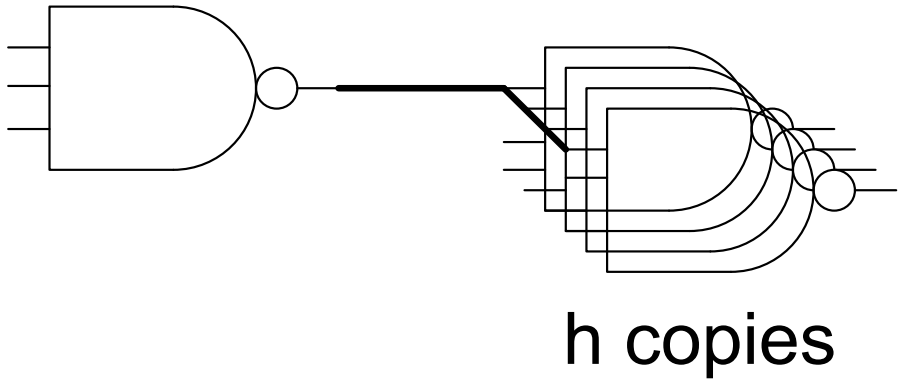


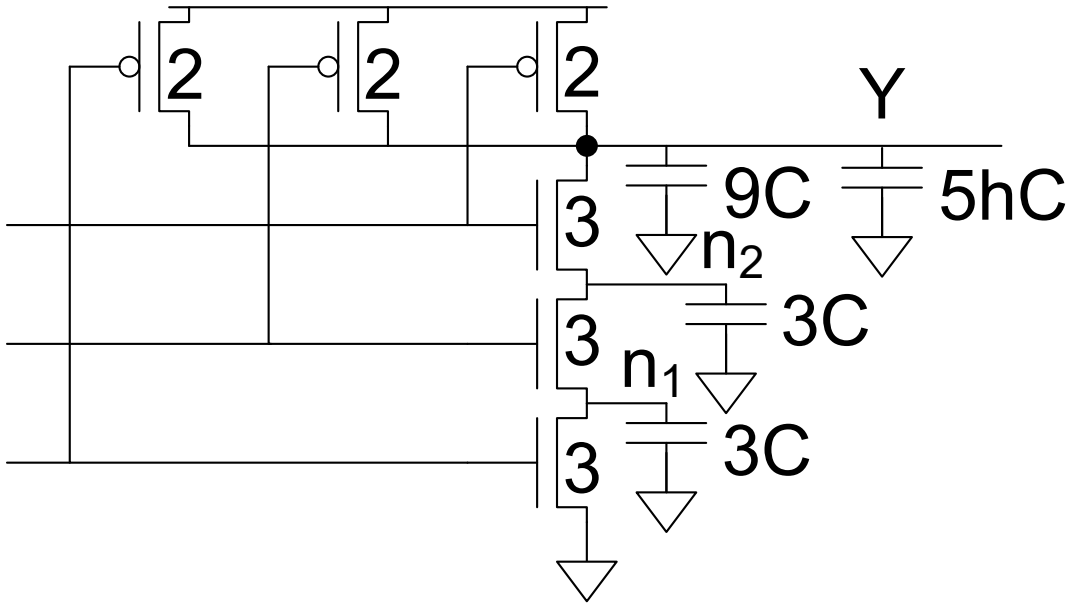
Homework#4

- Problem#2
  - Draw the exact response of V_X and an approximated one with a single time constant.

4.3. RC delay model (9)

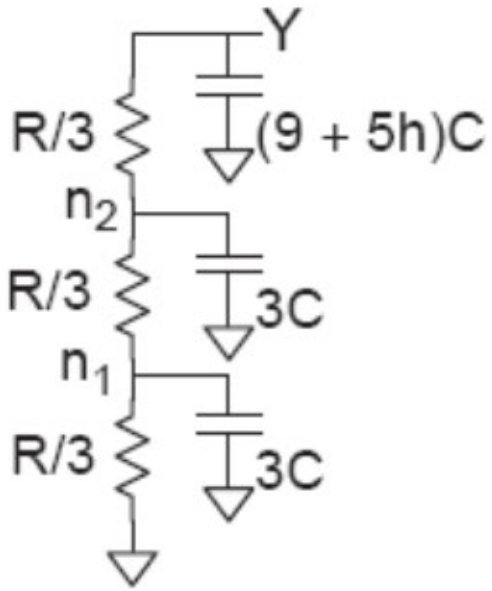
- Example 4.7 (h identical NANDs)
  - We studied it in Example 4.2.





4.3. RC delay model (10)

- For the falling transition
  - Estimate t_{pdf}.
- For the rising transition (in the worst case)
  - Estimate t_{pdr}.



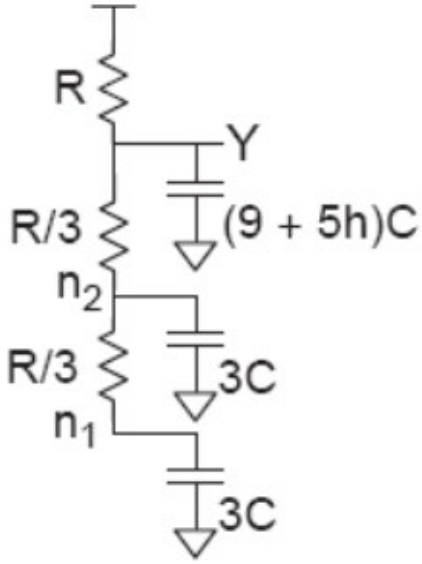


Fig. 4.15

4.3. RC delay model (11)

- Delay components
  - *Parastic delay*: Time for a gate to drive its own internal diffusion capacitance
  - *Effort delay*: It depends on the ratio of external load capacitance to input capacitance.
  - The normalized delay, $d = \frac{t_{pd}}{3RC}$, can be written as

$$d = parastic\ delay + effort\ delay$$

4.3. RC delay model (12)

- Layout dependence of capacitance
  - A good layout minimizes the diffusion area.

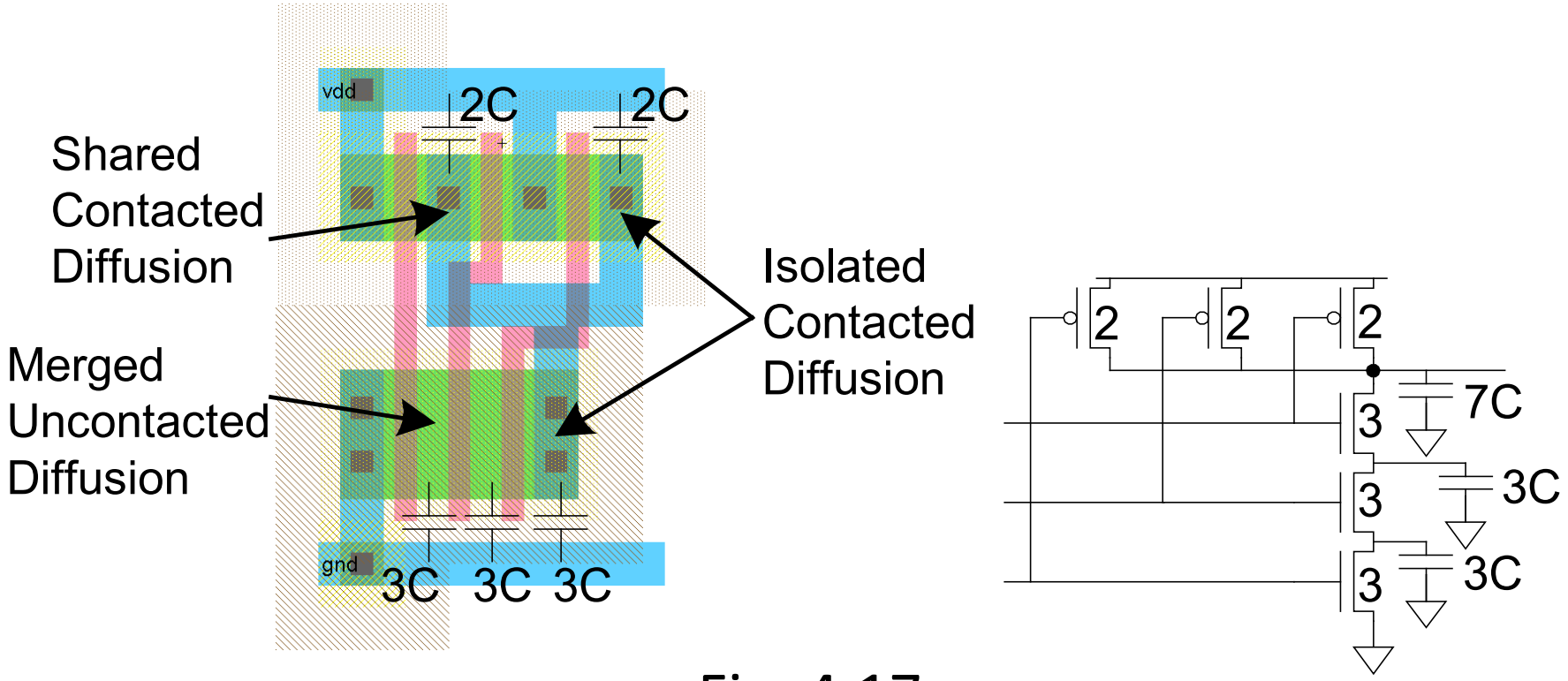


Fig. 4.17

4.4 Linear Delay Model

4.4. Linear delay model (1)

- Delay in a logic gate
  - Normalized delay

$$d = \frac{t_{pd}}{3RC}$$

  - Delay has two components:

$$d = f + p = gh + p$$

  - Effort delay:

$$f = gh$$

(g is the logical effort.)

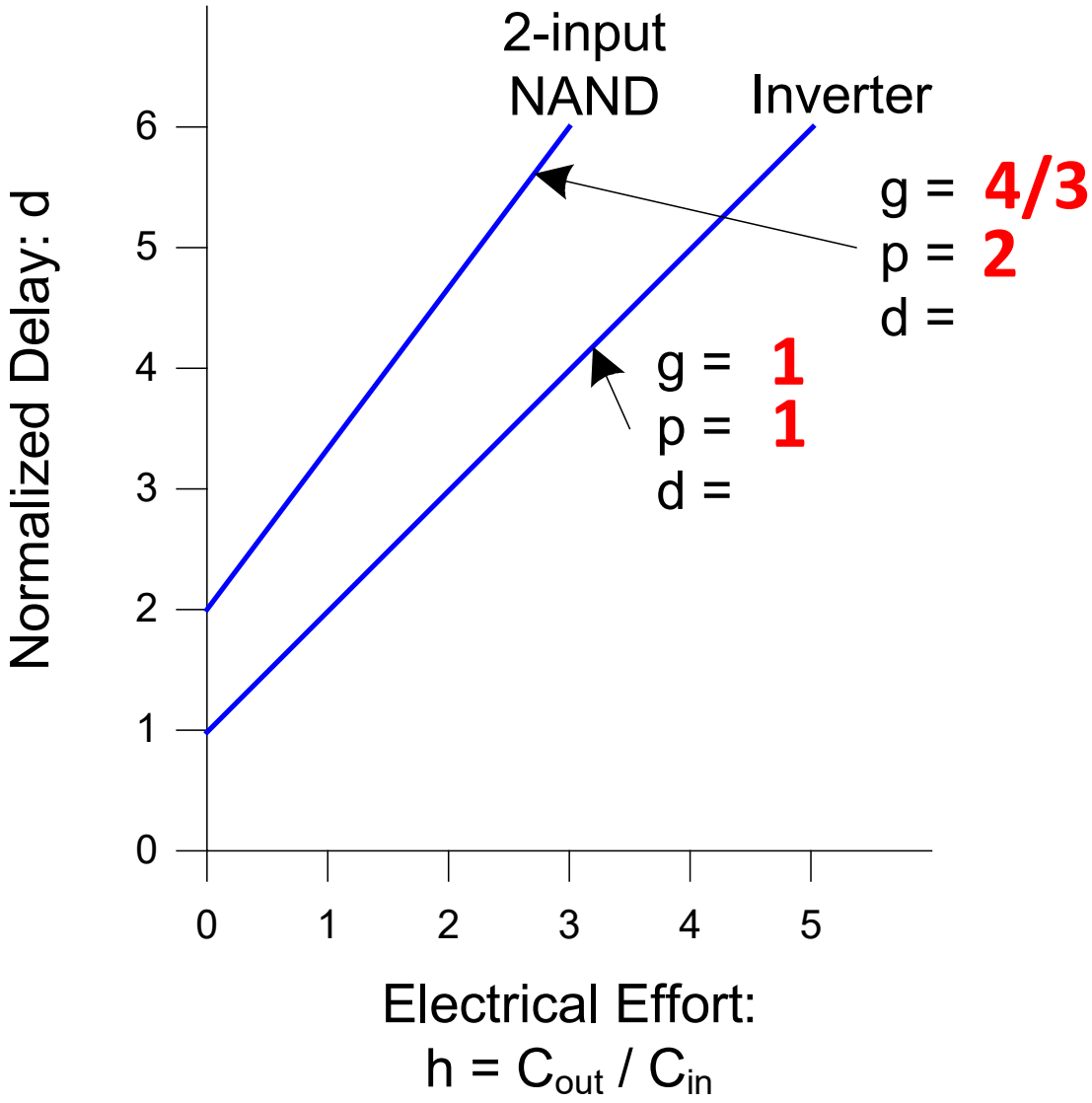
4.4. Linear delay model (2)

- Delay in a logic gate
  - Fanout (or electrical effort)

$$h = \frac{C_{out}}{C_{in}}$$

(Ratio of output to input capacitance)

  - Parasitic delay, p, represents delay of gate driving no load.
  - p is set by internal parasitic capacitance.



Thank you!