Digital Integrated Circuit
Lecture 17 Power

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Review of Previous Lecture

Lecture 16

- Dynamic power
  - It is dominated by the switching power consumption,

$$P_{switching} = \alpha C V_{DD}^2 f$$

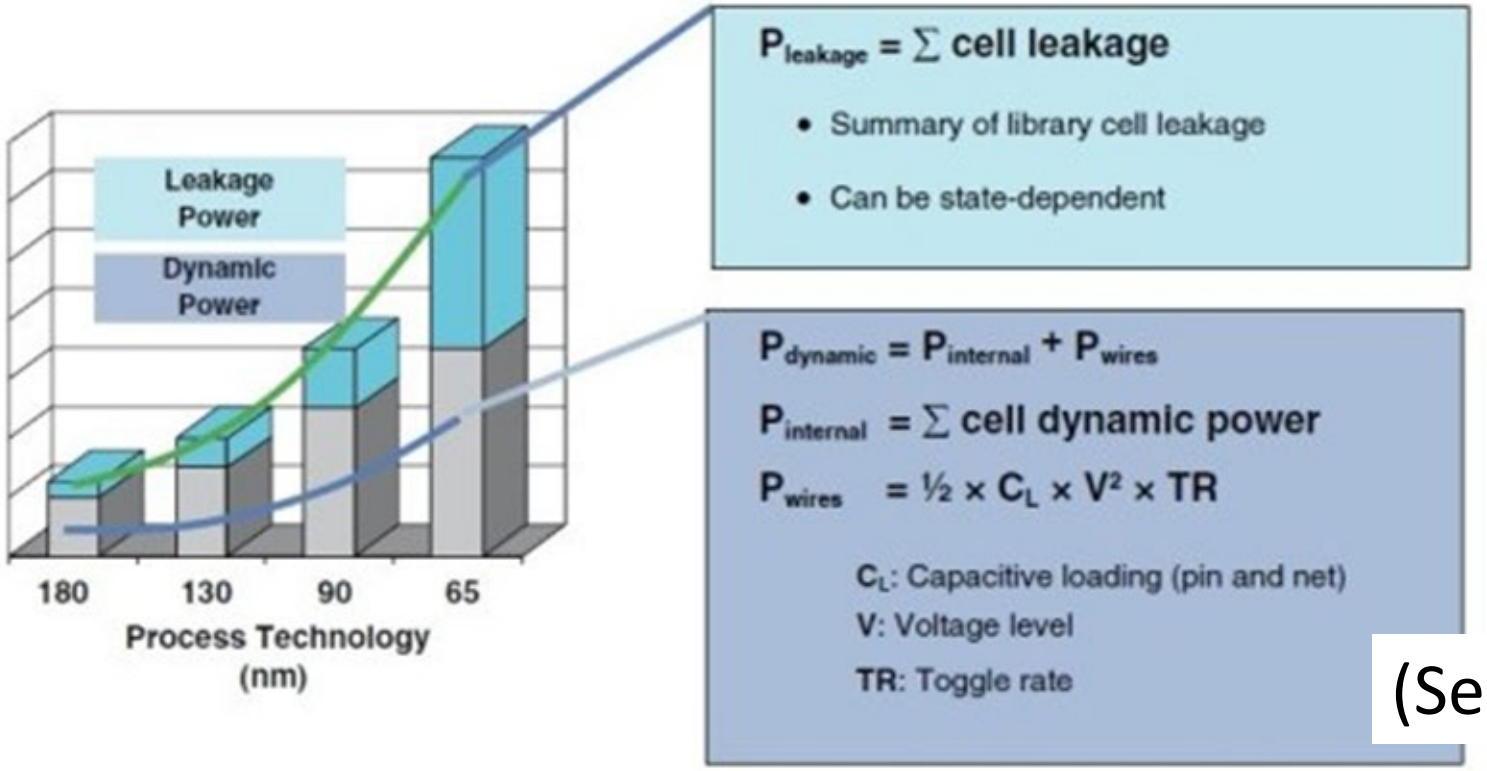
  - Various ways to reduce the switching power

5.3 Static Power

5.3. Static power (1)

- Static power is consumed even when a chip is not switching.

$$P_{static} = \left(I_{sub} + I_{gate} + I_{junct} + I_{contention}\right)V_{DD}$$



(Semiconductor Engineering)

5.3. Static power (2)

- Estimate the static power consumption.
  - 1.0 V 65 nm process (λ is 25 nm.)
  - 50M logic transistors (Average width: 12λ), 95 % of high-V_t, 5 % of low-V_t
  - 950M memory transistors (Average width: 4λ), all high-V_t
  - Total width of low-V_t transistors is 0.75 X 10^6 μm.
  - Total width of high-V_t transistors is 109.25 X 10^6 μm.
  - Subthreshold leakage currents: 100 nA/μm for low-V_t, 10 nA/μm for high-V_t
  - Gate leakage current: 5 nA/μm
  - The answer is 859 mW.

5.3. Static power (3)

- Subthreshold leakage (for V_{ds} > 50 mV)

$$I_{sub} = I_{off} 10^{\frac{V_{gs}+\eta(V_{ds}-V_{DD})-k_\gamma V_{sb}}{S}}$$

Transistor Type	High Speed Logic		Low Power Logic		High Voltage	
Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)	0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)	90	90	90	108	min. 180	min. 450
Lgate (nm)	30	34	34	40	min. 80	min. 280
N/PMOS Idsat/Ioff (mA/um)	1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V 30 pA/um	0.35 / 0.33 @ 0.75 V 15 pA/um	0.92 / 0.8 @ 1.8 V 10 pA/um	1.0 / 0.85 @ 3.3 V 10 pA/um

(Intel's 2012 IEDM abstract)

5.3. Static power (4)

- Stack effect

$$I_{sub} = I_{off} 10^{\frac{V_{gs}+\eta(V_{ds}-V_{DD})-k_\gamma V_{sb}}{S}}$$

  - N1 current

$$I_{sub} = I_{off} 10^{\frac{\eta(V_x-V_{DD})}{S}}$$

  - N2 current

$$I_{sub} = I_{off} 10^{\frac{-V_x+\eta(V_{DD}-V_x-V_{DD})-k_\gamma V_x}{S}}$$

  - Then, with $V_x = \frac{\eta}{1+2\eta+k_\gamma} V_{DD}$,

$$I_{sub} = I_{off} 10^{\frac{-\eta V_{DD}}{S}\left(\frac{1+\eta+k_\gamma}{1+2\eta+k_\gamma}\right)}$$

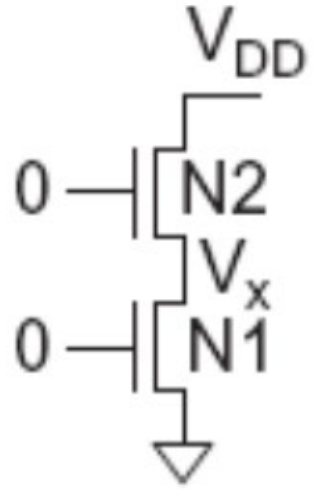
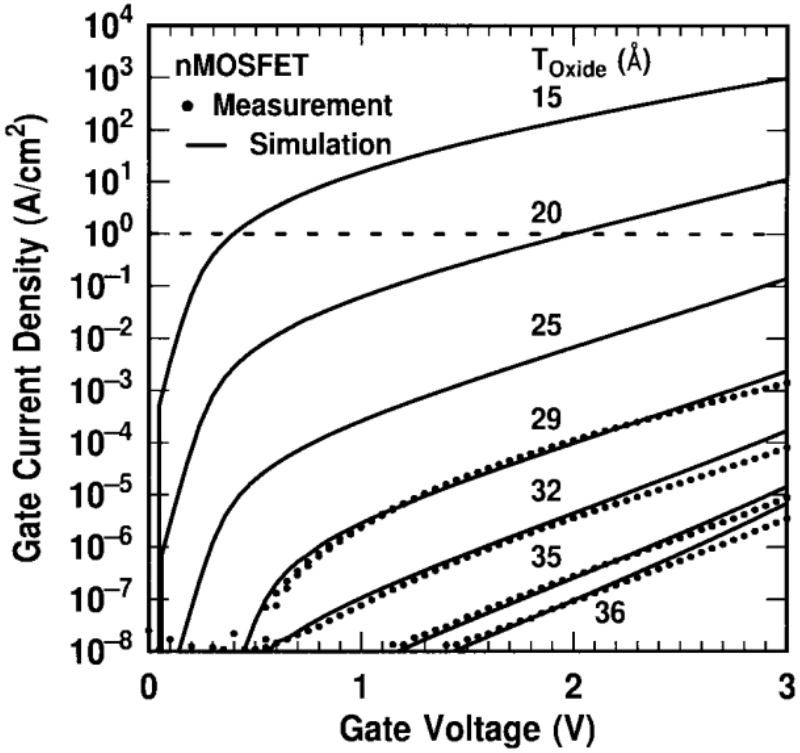


Fig. 5.20

5.3. Static power (5)

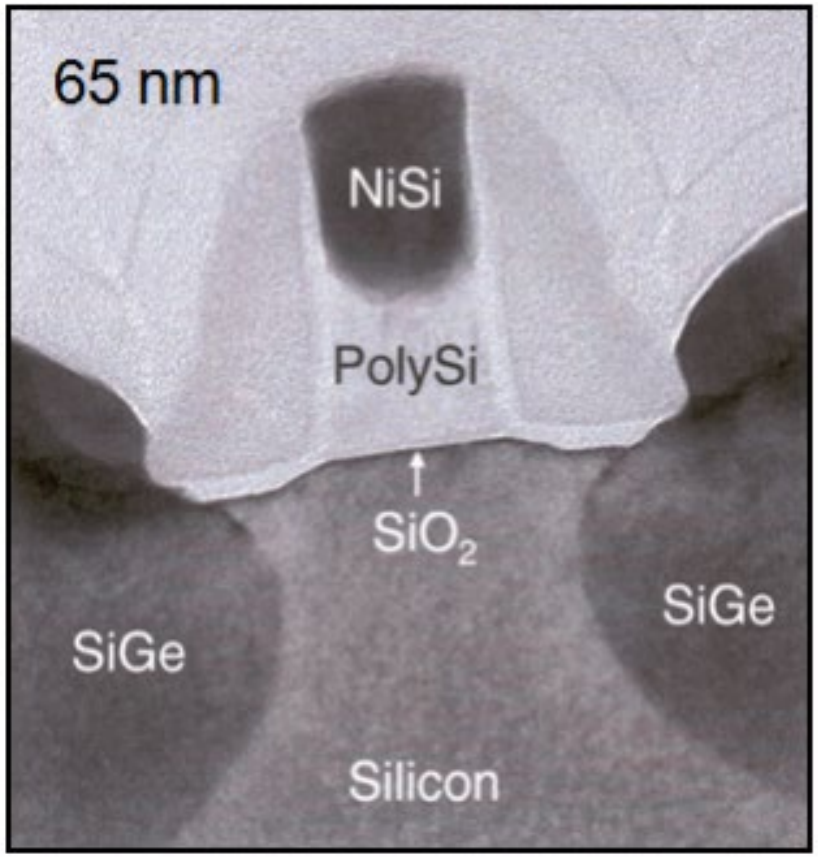
- Gate leakage
  - Various physical mechanisms
  - It is an extremely strong function of the dielectric thickness.
  - It also depends on the voltage across the gate.

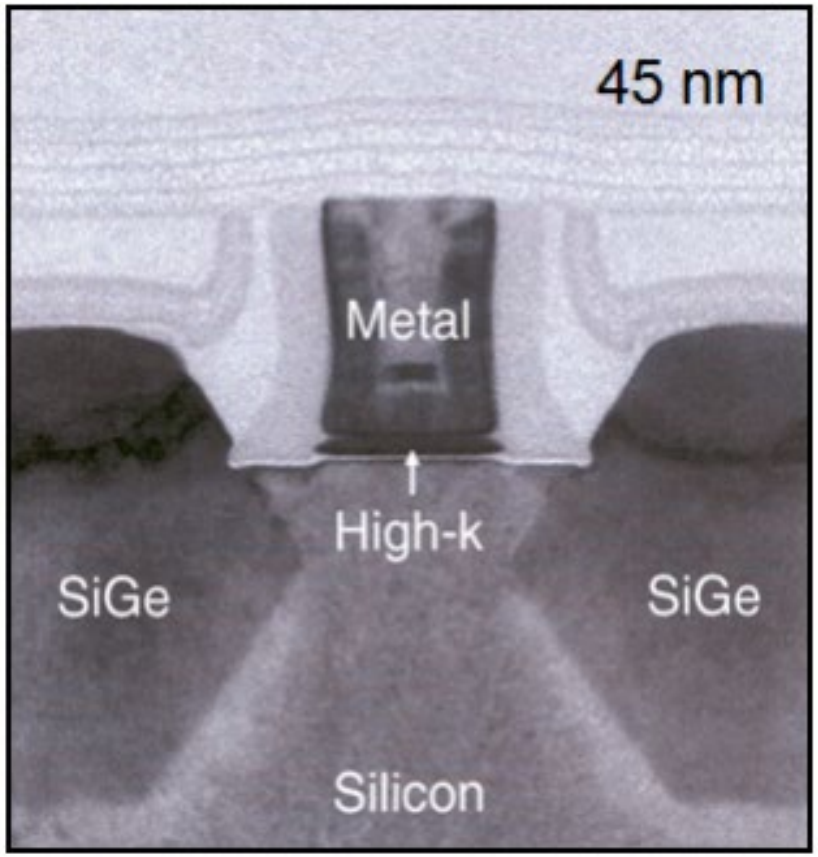


Measured Ig-Vg characteristics
(Ho et al., EDL, vol. 18, pp. 209-211)

5.3. Static power (6)

- High-k metal gate
  - Compare two technologies.





(Intel)

5.3. Static power (7)

- NAND3 leakage example (Leakage current in nA)

Input State (ABC)	I_{sub}	I_{gate}	I_{total}	V_x	V_z
000	0.4	0	0.4	stack effect	stack effect
001	0.7	0	0.7	stack effect	$V_{DD} - V_t$
010	0.7	1.3	2.0	intermediate	intermediate
011	3.8	0	3.8	$V_{DD} - V_t$	$V_{DD} - V_t$
100	0.7	6.3	7.0	0	stack effect
101	3.8	6.3	10.1	0	$V_{DD} - V_t$
110	5.6	12.6	18.2	0	0
111	28	18.9	46.9	0	0

Table 5.2

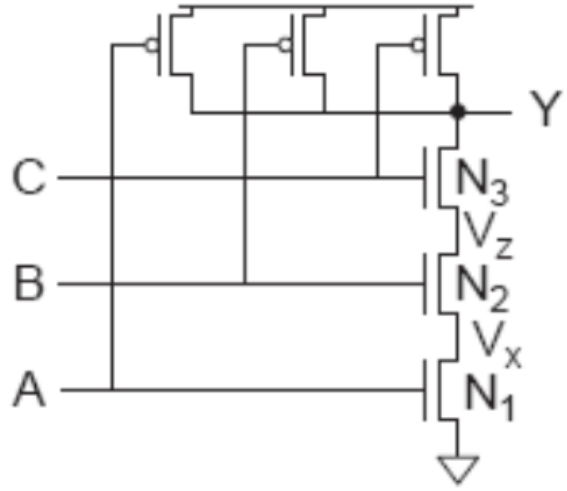


Fig. 5.23

5.3. Static power (8)

- Power gating
  - Turn OFF power to block when they are idle.
  - Use virtual V_{DD} (V_{DDV})
  - Gate outputs to prevent invalid logic level to next block

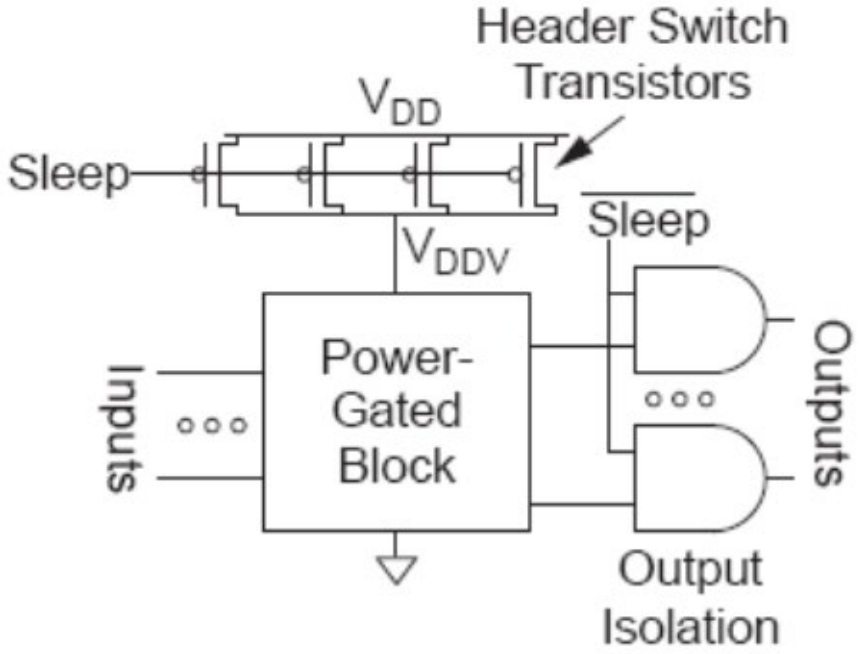


Fig. 5.24

Thank you!