Digital Integrated Circuit
Lecture 3 Introduction

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Review of Previous Lecture

Lecture 2

- Complementary CMOS gates
  - Pull-down & pull-up: Conduction complements
  - Inverter, NAND, NOR, and compound gates
- Pass transistors
  - Transistors can be used as switches.
  - Transmission gate

1.4 CMOS Logic

1.4. CMOS logic (10)

- Tristates (0, 1, and Z)
  - Tristate buffer produces Z when not enabled
  - Transmission gate acts as a tristate buffer.
  - But, it is nonrestoring.

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

Truth table of a tristate buffer

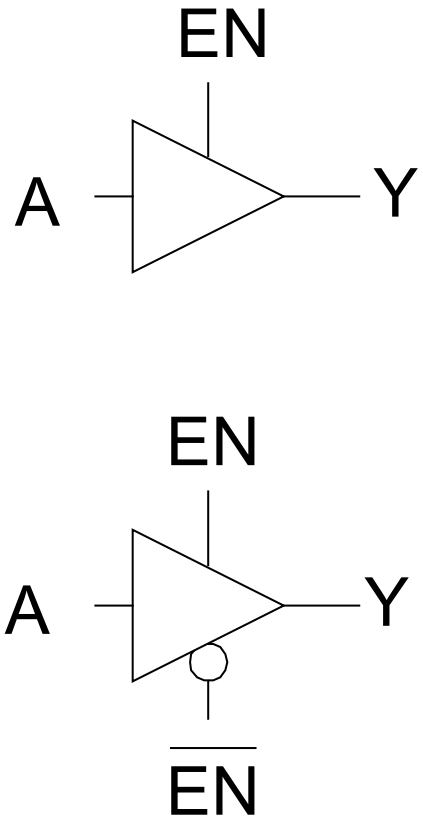


Fig. 1.25

1.4. CMOS logic (11)

- Tristate inverter
  - It produces a restored output.
  - It violates the conduction complements rule. (Why?)

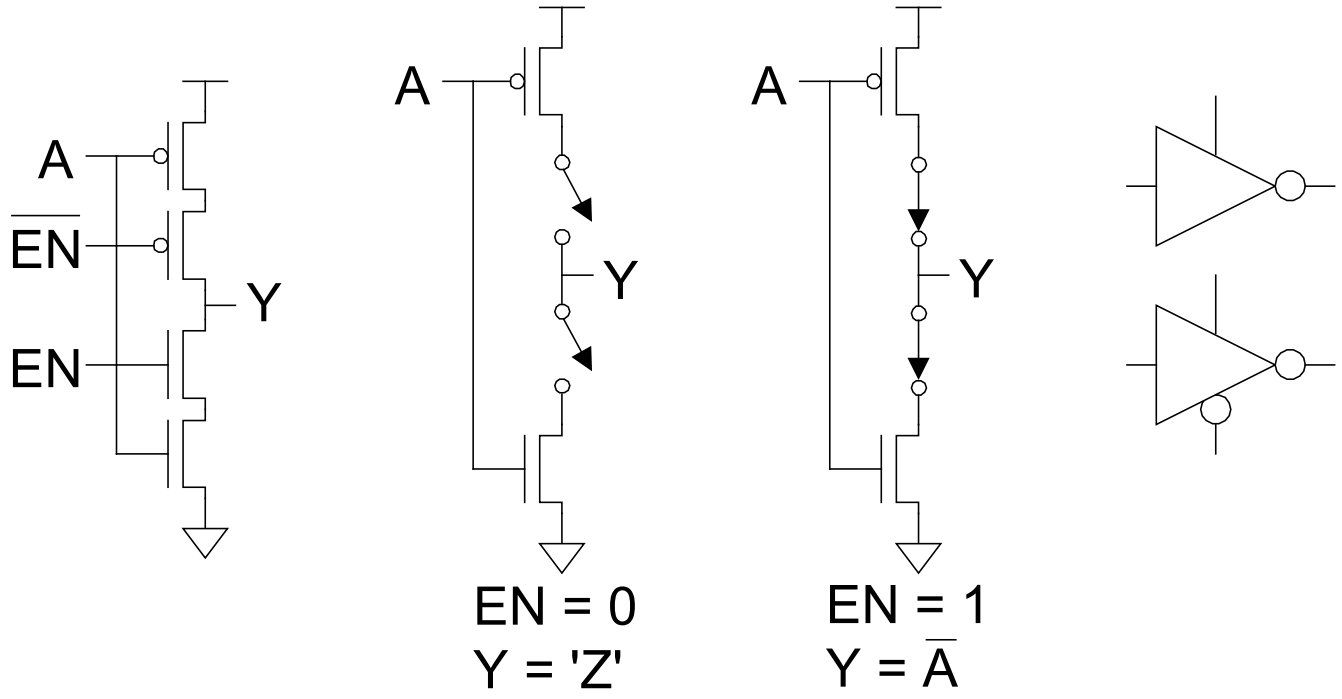


Fig. 1.27

1.4. CMOS logic (12)

- Multiplexers (muxes)
  - It chooses the output from several inputs based on a select signal.

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

Truth table of a 2:1 multiplexer

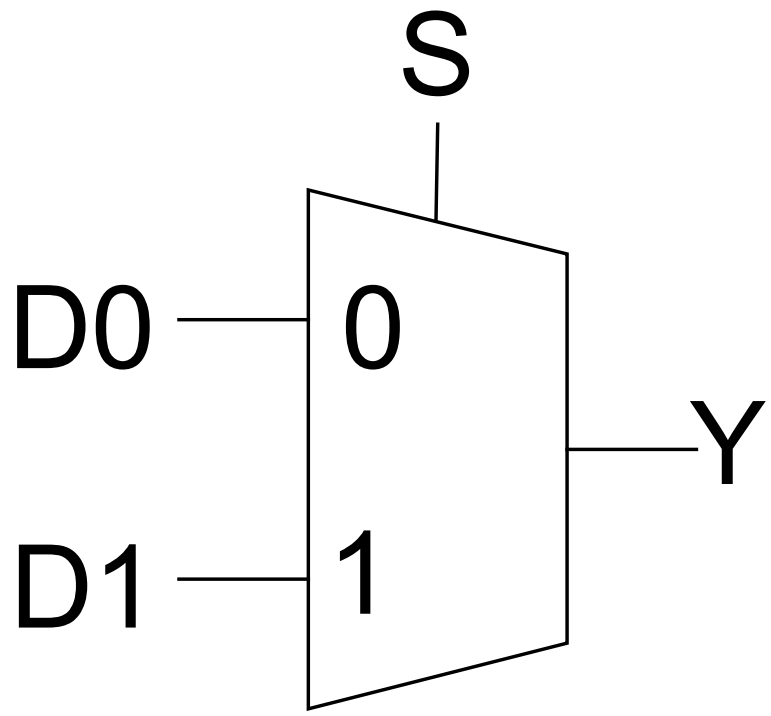


Fig. 1.28(b)

1.4. CMOS logic (13)

- Implementation
  - Using transmission gates (nonrestoring)
  - Using tristate inverters (inverting)

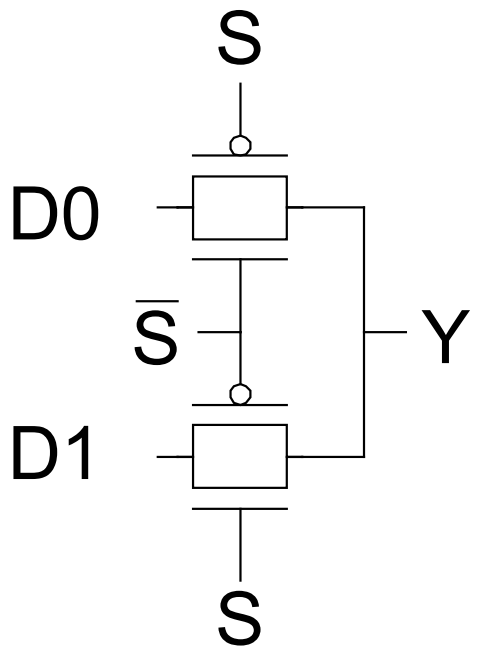


Fig. 1.28(a)

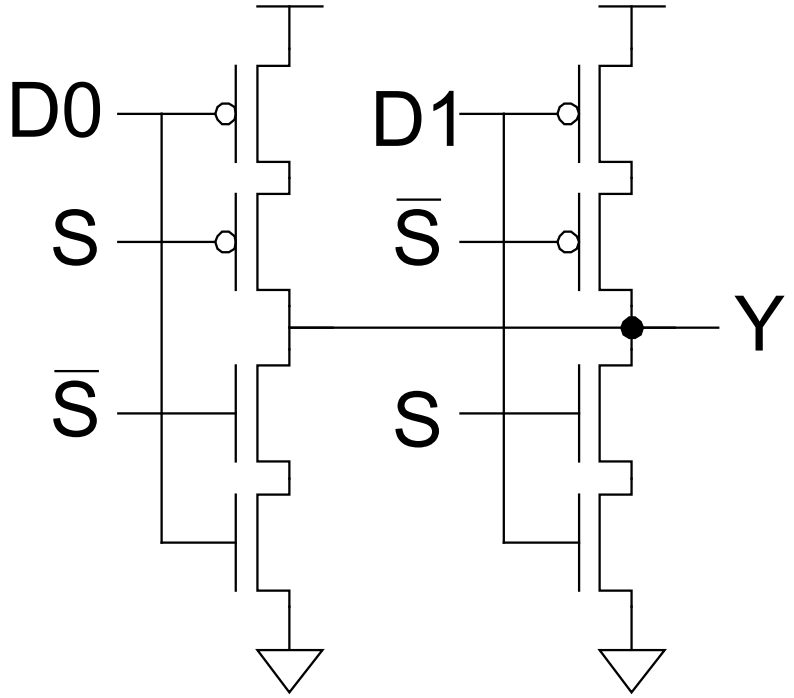


Fig. 1.29(b)

1.4. CMOS logic (14)

- Larger multiplexers
  - Example) 4:1 multiplexer
  - Two levels of 2:1 muxes
  - Or four tristates

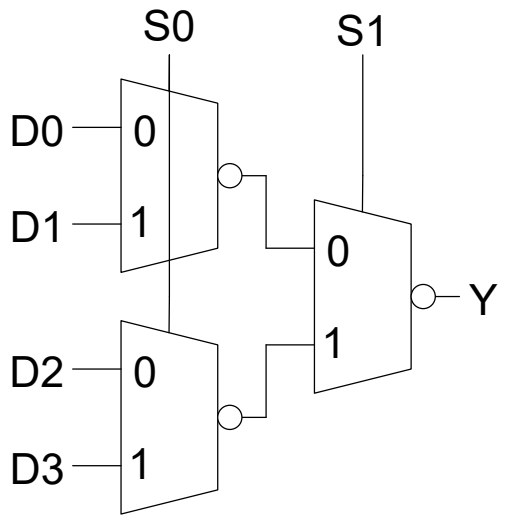
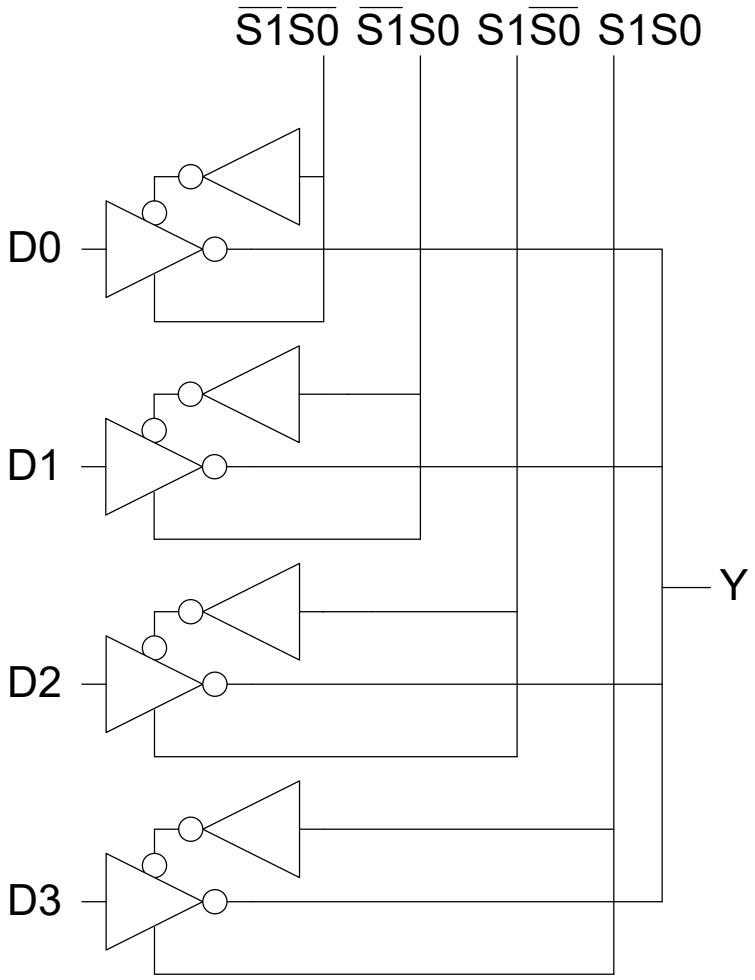


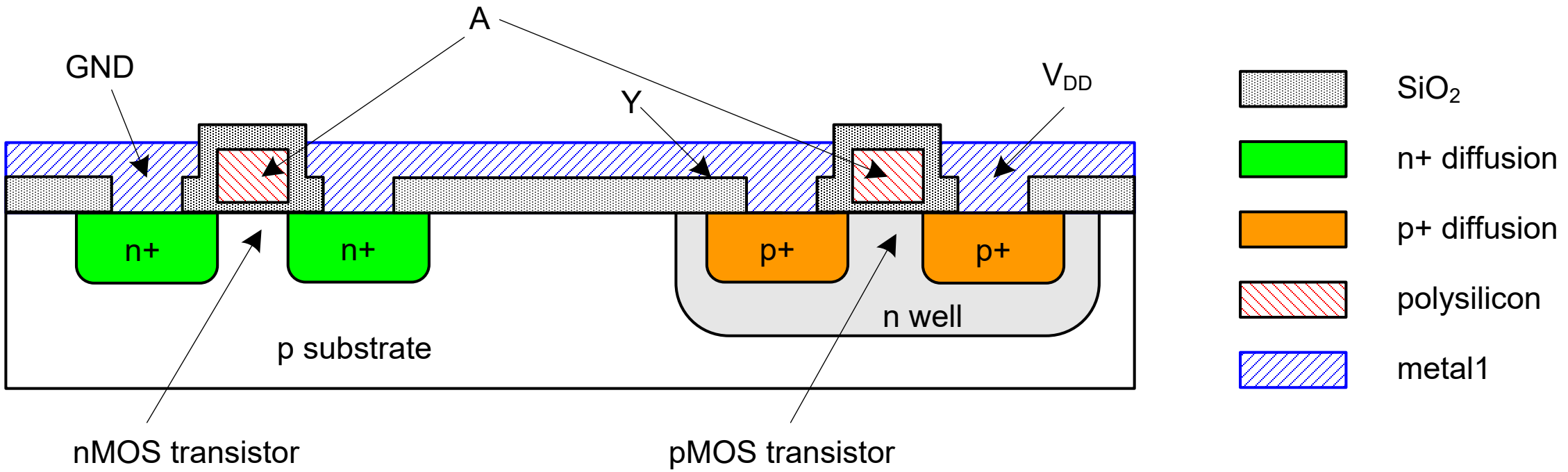
Fig. 1.30



1.5 CMOS Fabrication and Layout

1.5. CMOS fabrication (1)

- Inverter cross-section
  - P-type substrate for NMOS transistors
  - N-well for body of PMOS transistors



1.5. CMOS fabrication (2)

- Well and substrate taps
  - The substrate must be tied to GND. Likewise, the n-well must be tied to V_{DD}.
  - Taps to connect GND and V_{DD} to the substrate and n-well, respectively

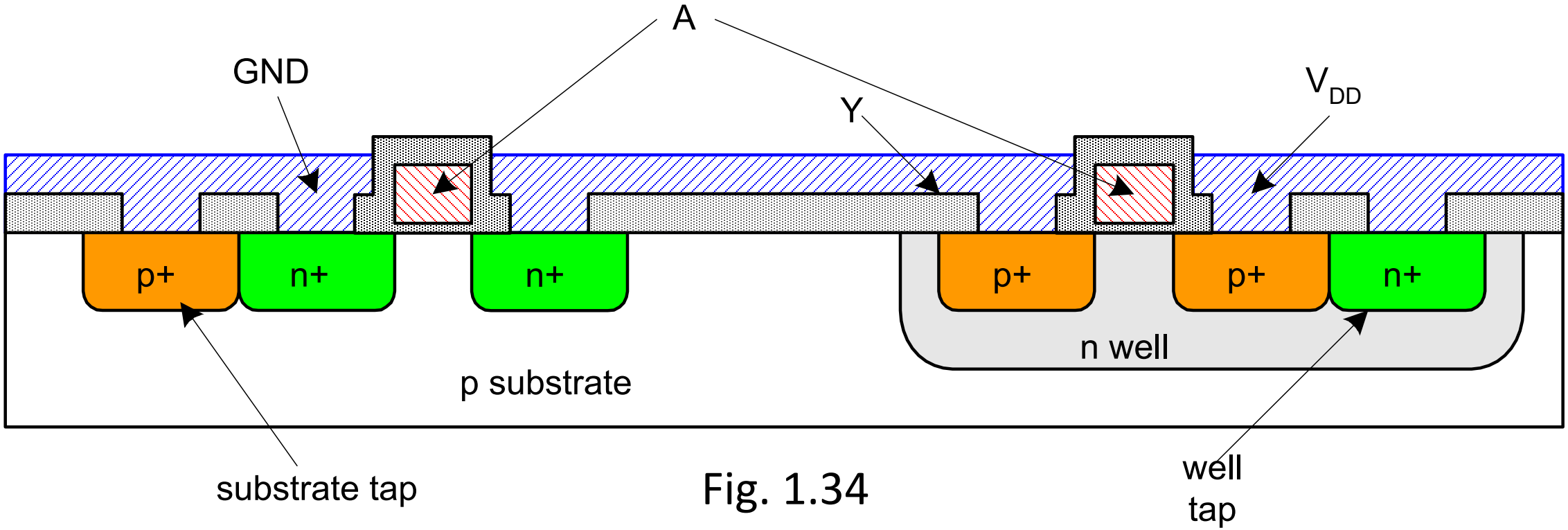


Fig. 1.34

1.5. CMOS fabrication (3)

- Interver mask

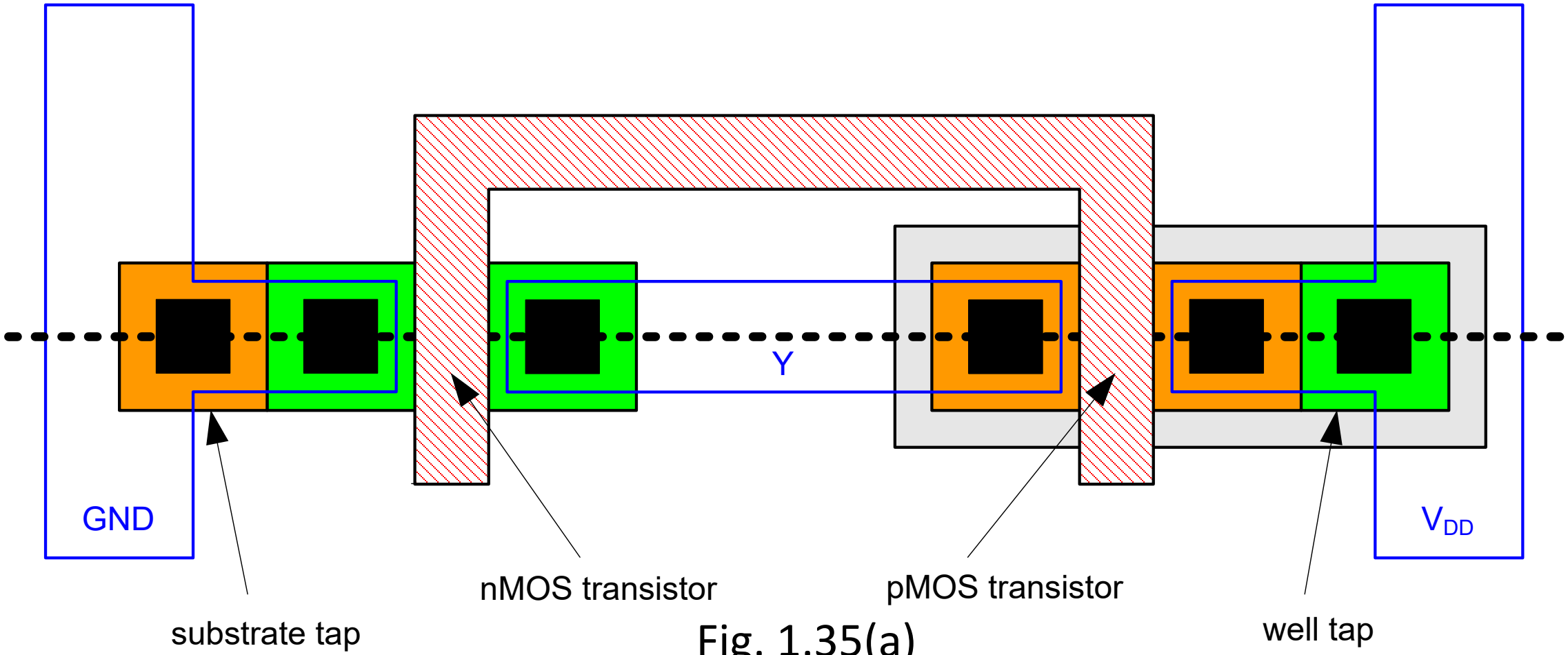


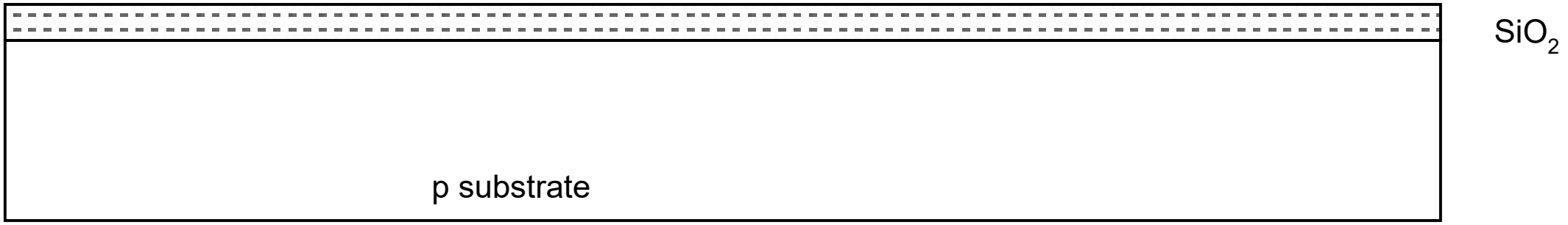
Fig. 1.35(a)

1.5. CMOS fabrication (4)

- Blank wafer

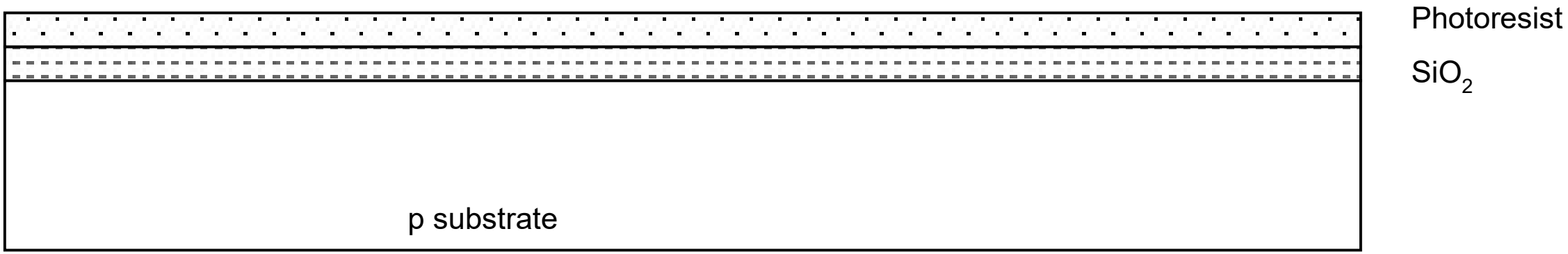
1.5. CMOS fabrication (5)

- Oxidation
  - Grow SiO_2 on top of Si wafer
  - High temperature (typically 900 ~ 1200 ˚C)



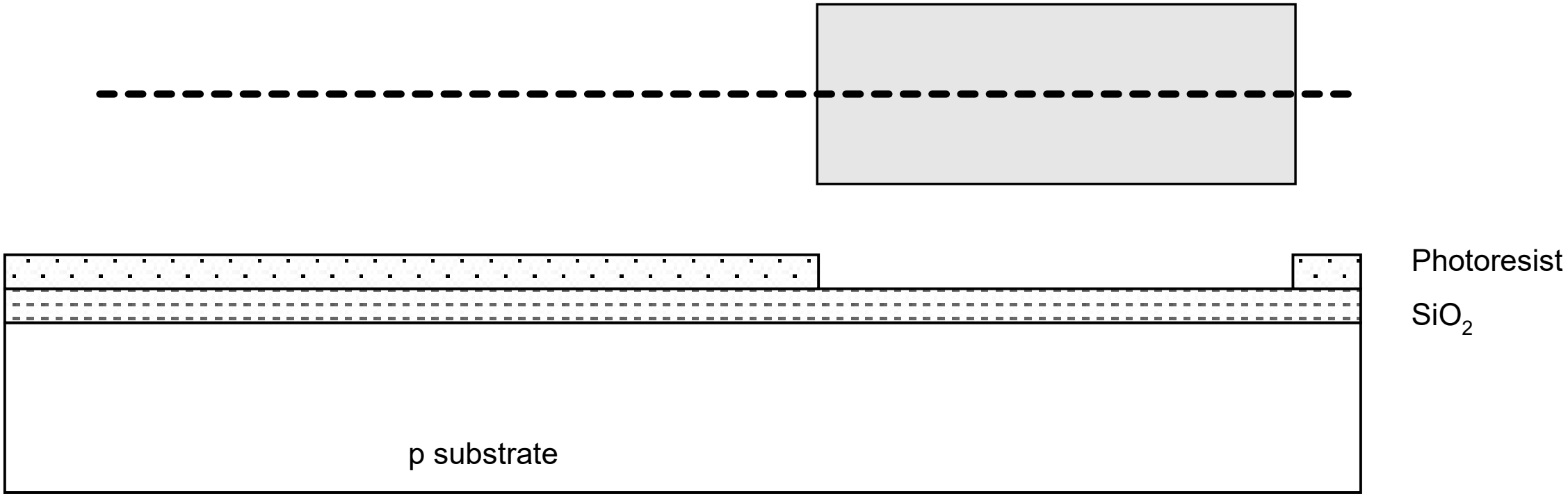
1.5. CMOS fabrication (6)

- Photoresist
  - Photoresist is a light-sensitive organic polymer.



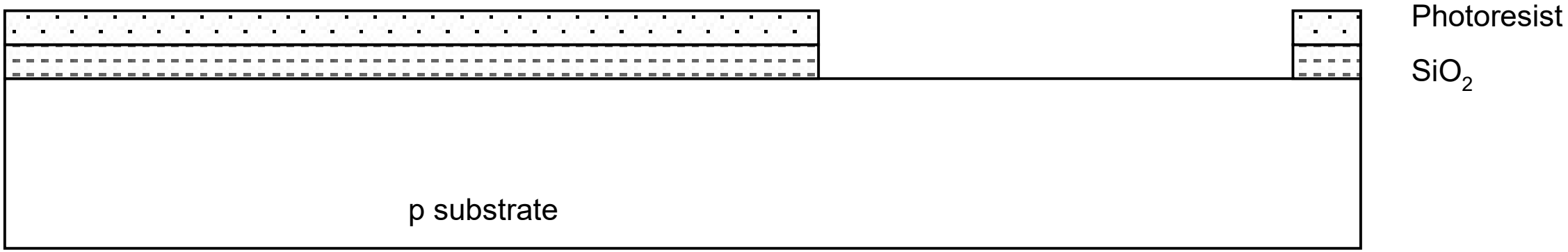
1.5. CMOS fabrication (7)

- Lithography
  - The photoresist is exposed through the n-well mask.
  - The soften photoresist is removed to expose the oxide.



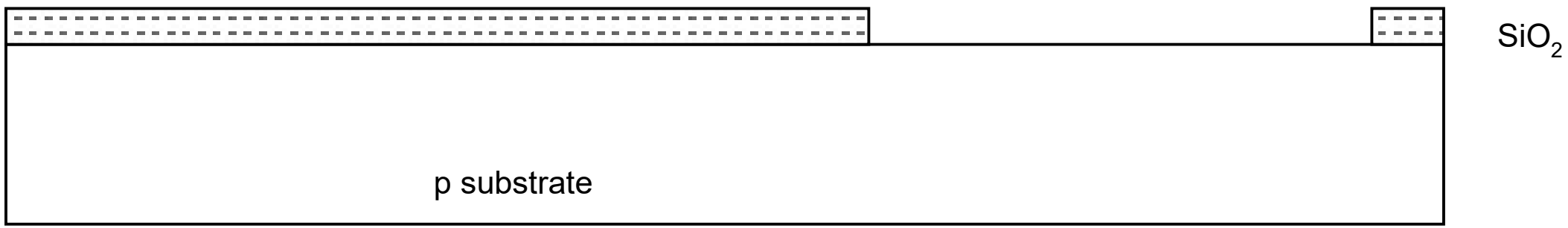
1.5. CMOS fabrication (8)

- Etch
  - The oxide is etched with hydrofluoric acid (HF). (The photoresist protects the oxide.)



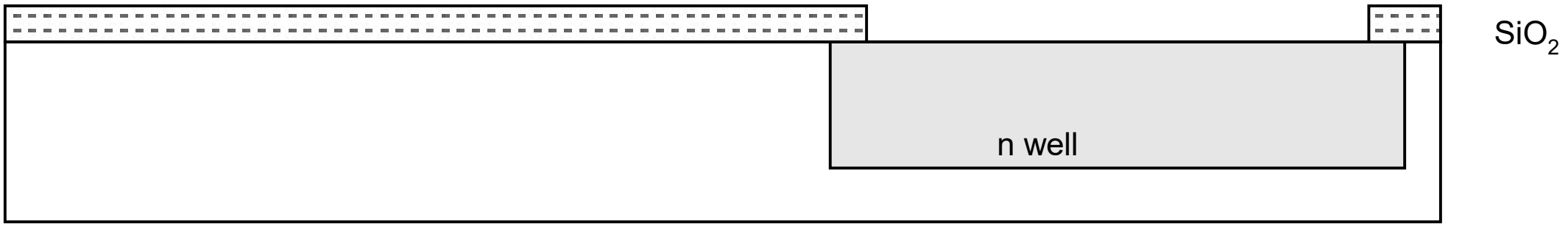
1.5. CMOS fabrication (9)

- Strip photoresist
  - The remaining photoresist is stripped away.



1.5. CMOS fabrication (10)

- N-well
  - The well is formed where the substrate is not covered with oxide.
  - Two ways to add dopants are diffusion and ion implantation.

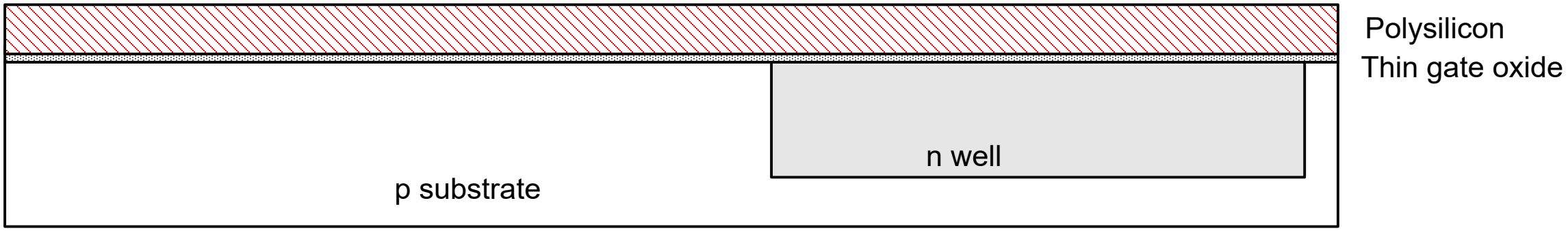


1.5. CMOS fabrication (11)

- Strip oxide
  - The remaining oxide is stripped with HF to leave the bare wafer with wells in the appropriate places.

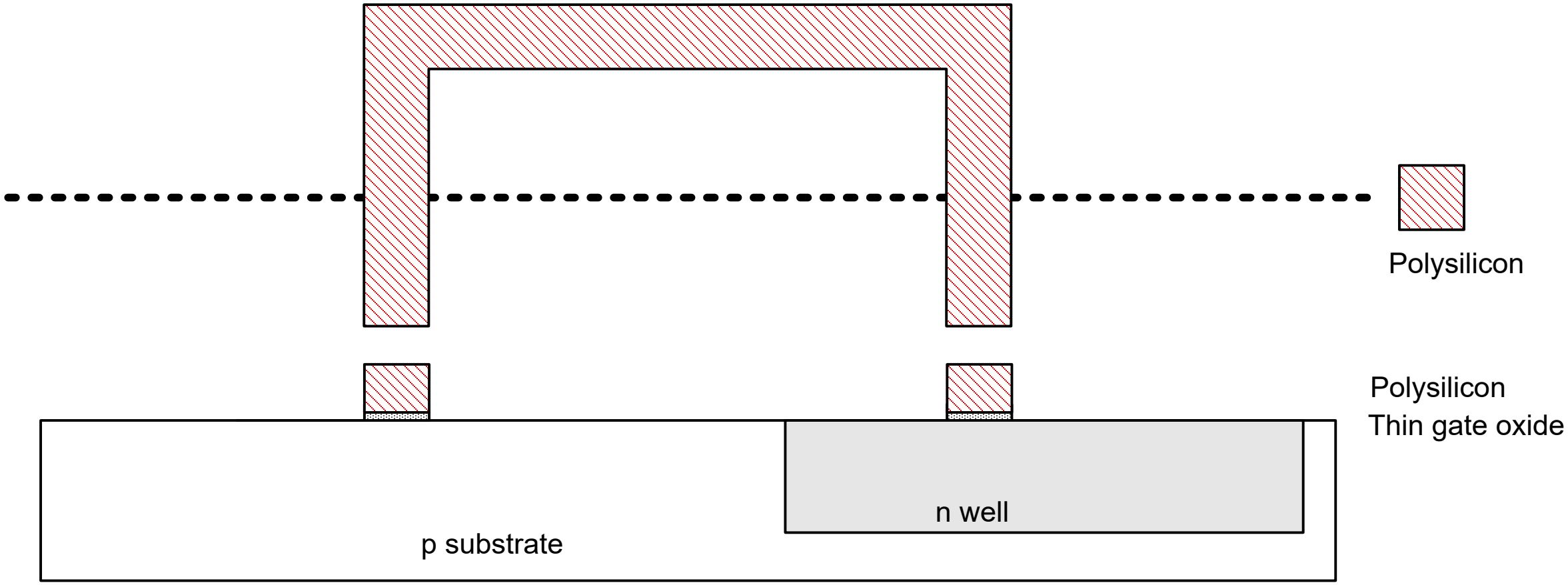
1.5. CMOS fabrication (12)

- Gate oxide and polysilicon
  - The thin oxide is grown in a furnace.
  - Then, the polysilicon layer is grown.



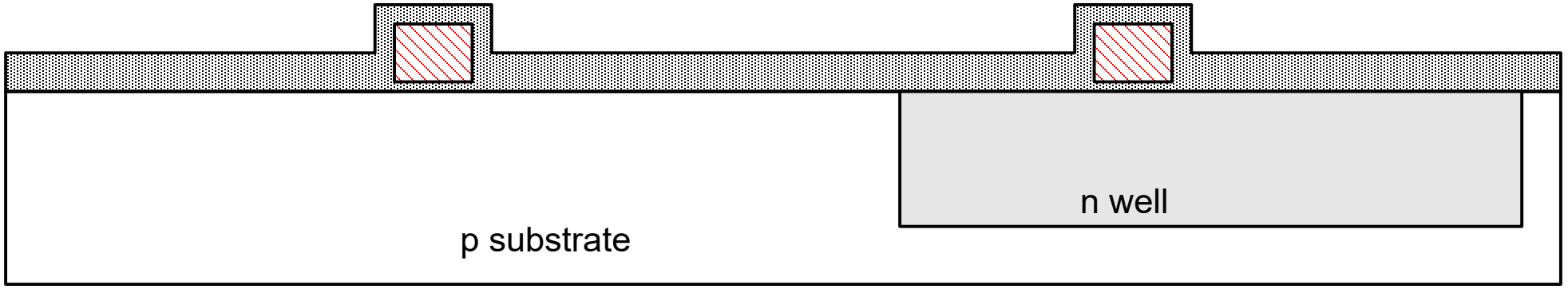
1.5. CMOS fabrication (13)

- Gate patterning



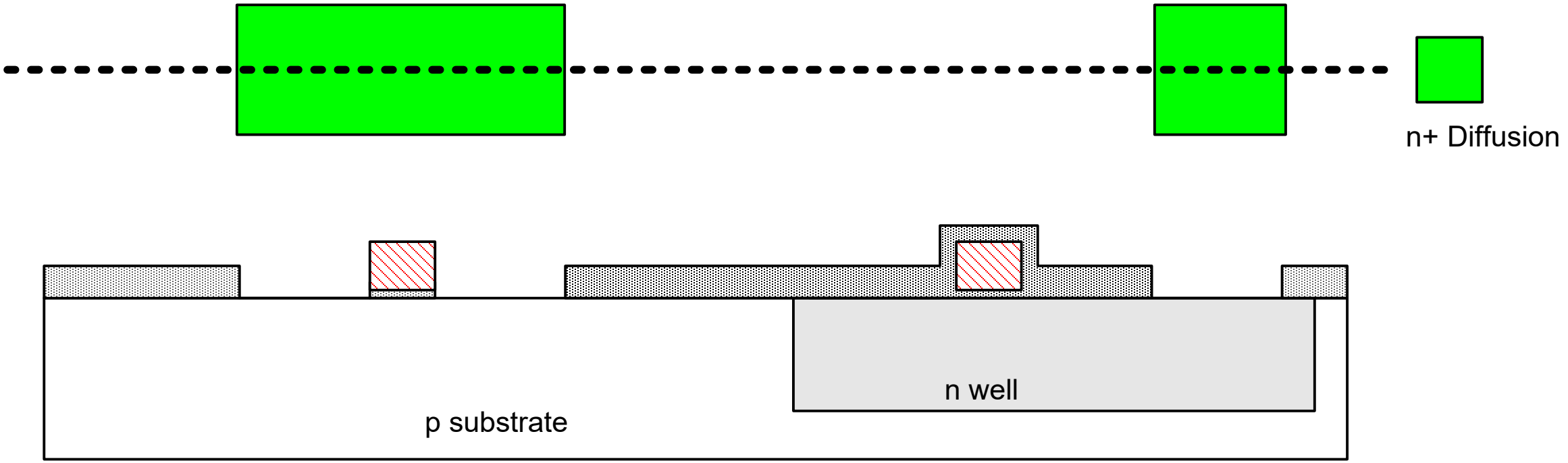
1.5. CMOS fabrication (14)

- Protective layer



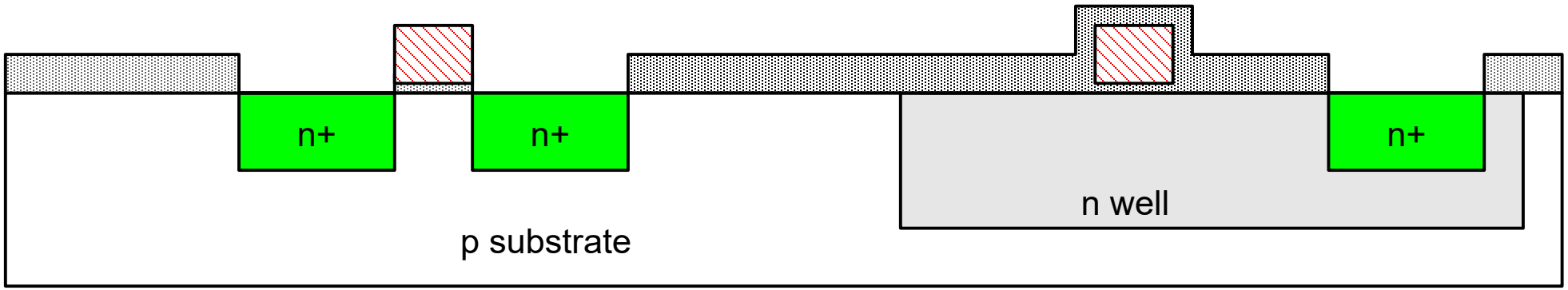
1.5. CMOS fabrication (15)

- N-diffusion
  - Patterned with the n-diffusion mask



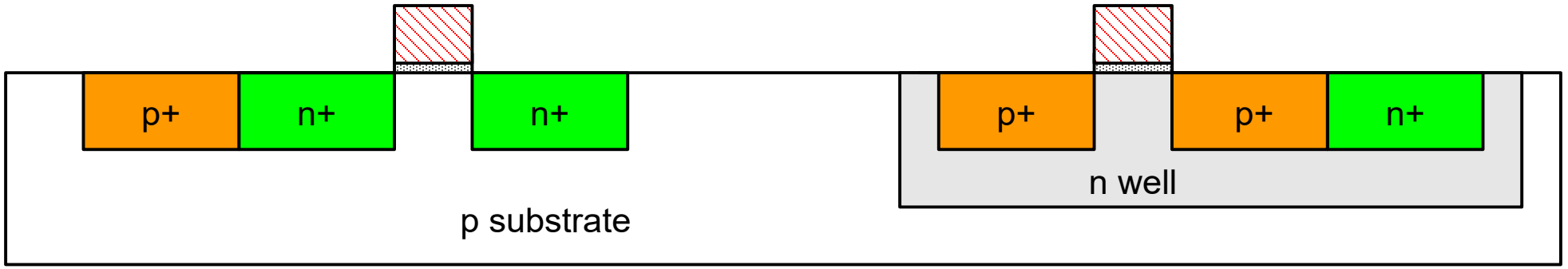
1.5. CMOS fabrication (16)

- Ion implantation
  - Due to the historical reason, it is called *n-diffusion*.
  - The gate blocks the diffusion so the source & drain are separated by a channel under the gate.
  - This is called a *self-aligned* process.



1.5. CMOS fabrication (17)

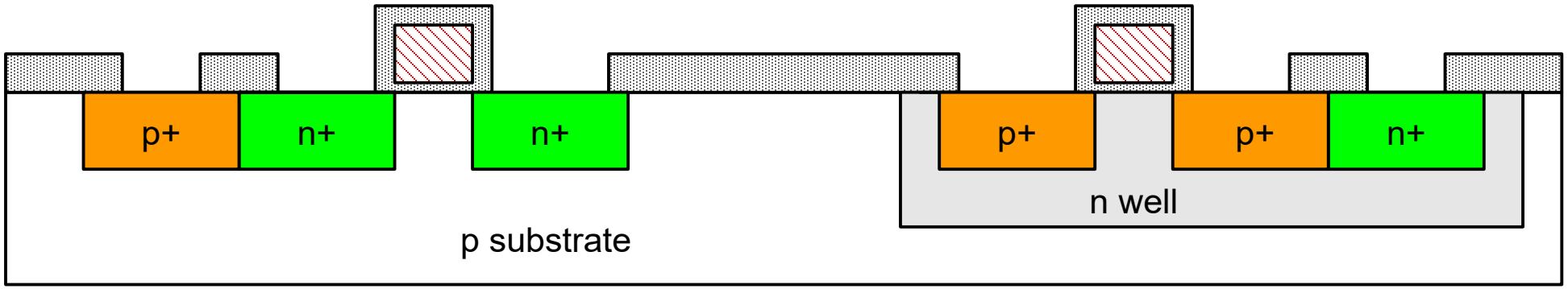
- P-diffusion
  - Repeat the previous process for the p-diffusion mask.



1.5. CMOS fabrication (18)

- Contacts
  - The field oxide is grown to insulate the wafer from metal.
  - It is patterned with the contact mask.

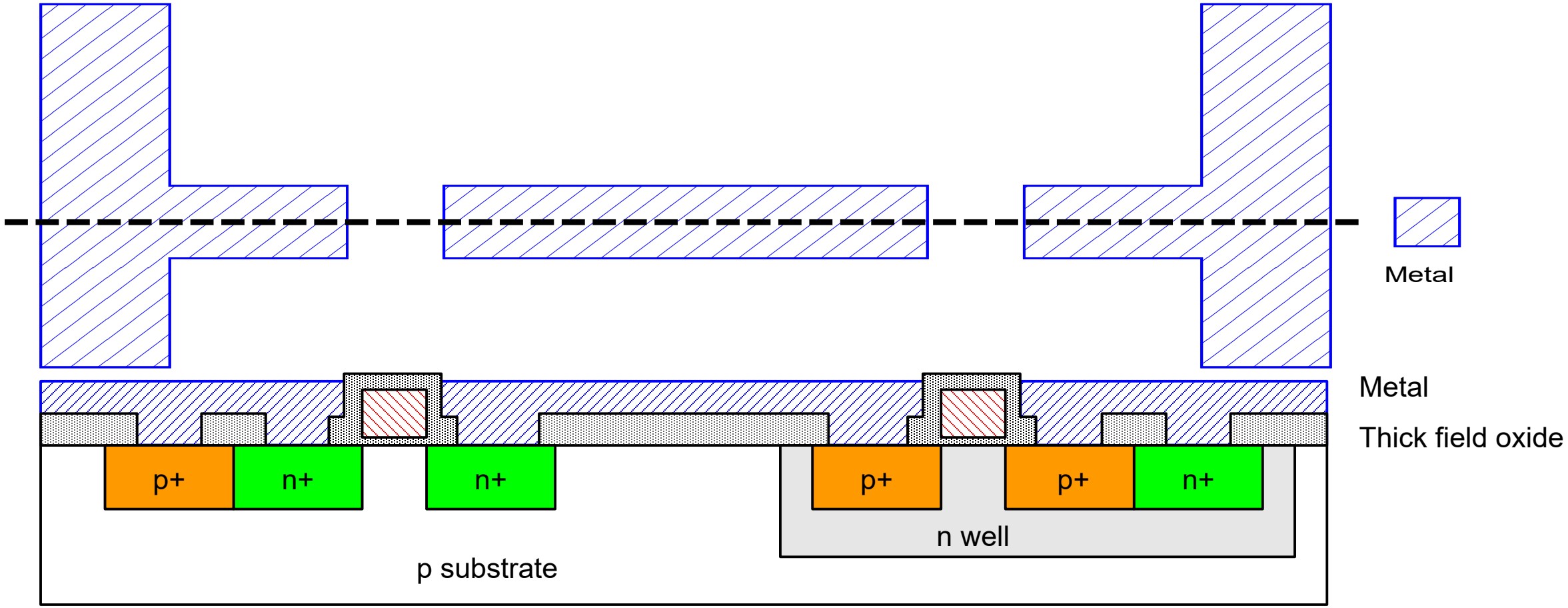
Contact



Thick field oxide

1.5. CMOS fabrication (19)

- Metalization



1.5. CMOS layout (1)

- Layout
  - Minimum dimensions of masks determine transistor size.
  - Feature size refers to minimum transistor length.
  - λ is half the feature size.
  - Transistor dimensions specified as Width / Length in λ.
  - In digital systems, transistors are typically chosen to have the minimum possible length.

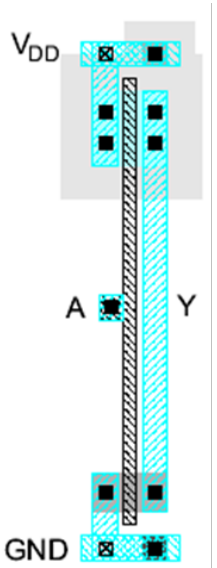
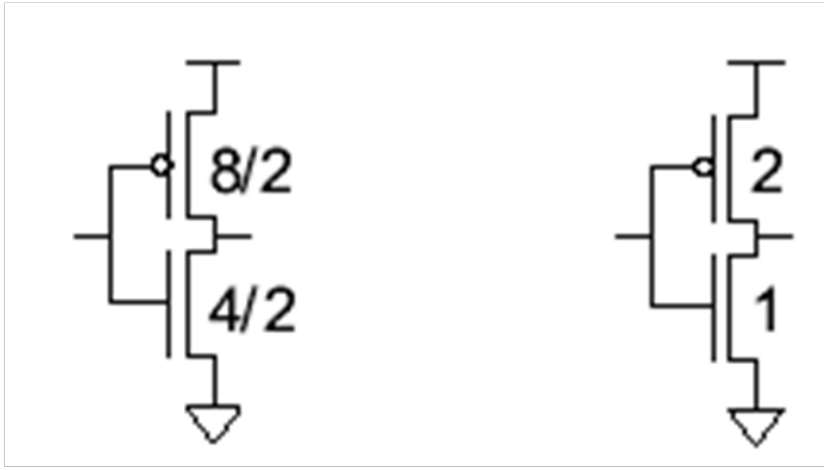


Fig. 1.40



1.5. CMOS layout (2)

- Standard cell design methodology
  - Four horizontal strips: metal groun at the bottom, n-diffusion, p-diffusion, and metal power at the top
  - The power and ground lines are often called *supply rails*.
  - Gate lines run vertically to form transistor gates.

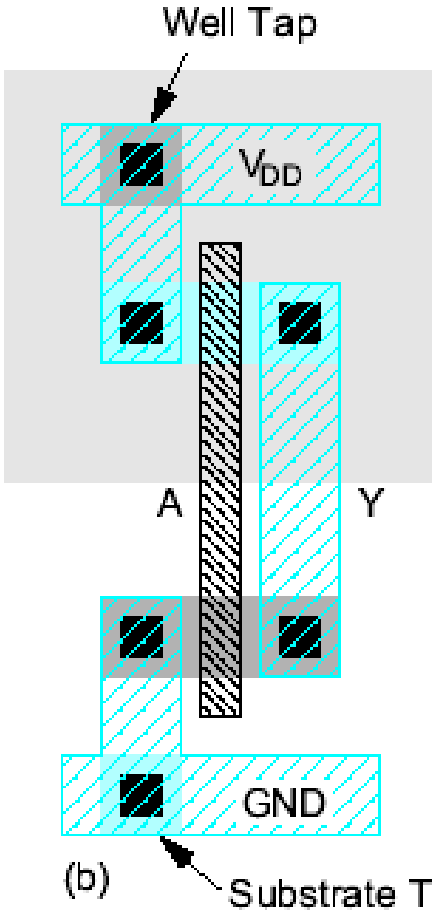


Fig. 1.41(b)

1.5. CMOS layout (3)

- NAND3

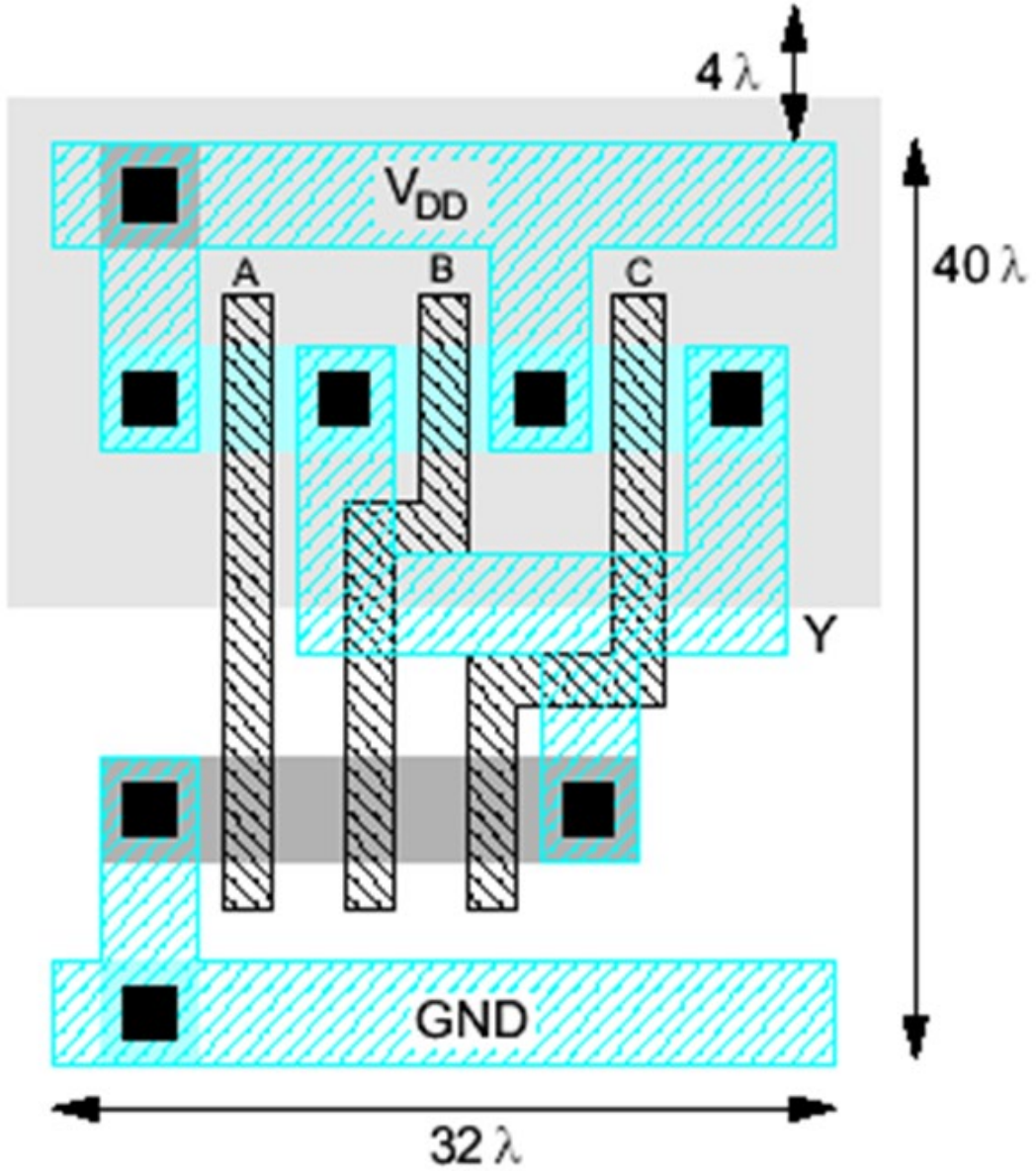


Fig. 1.42

Thank you!