Digital Integrated Circuit
Lecture 16 Power

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Review of Previous Lecture

Lecture 15

- Power
  - Instanteneous power

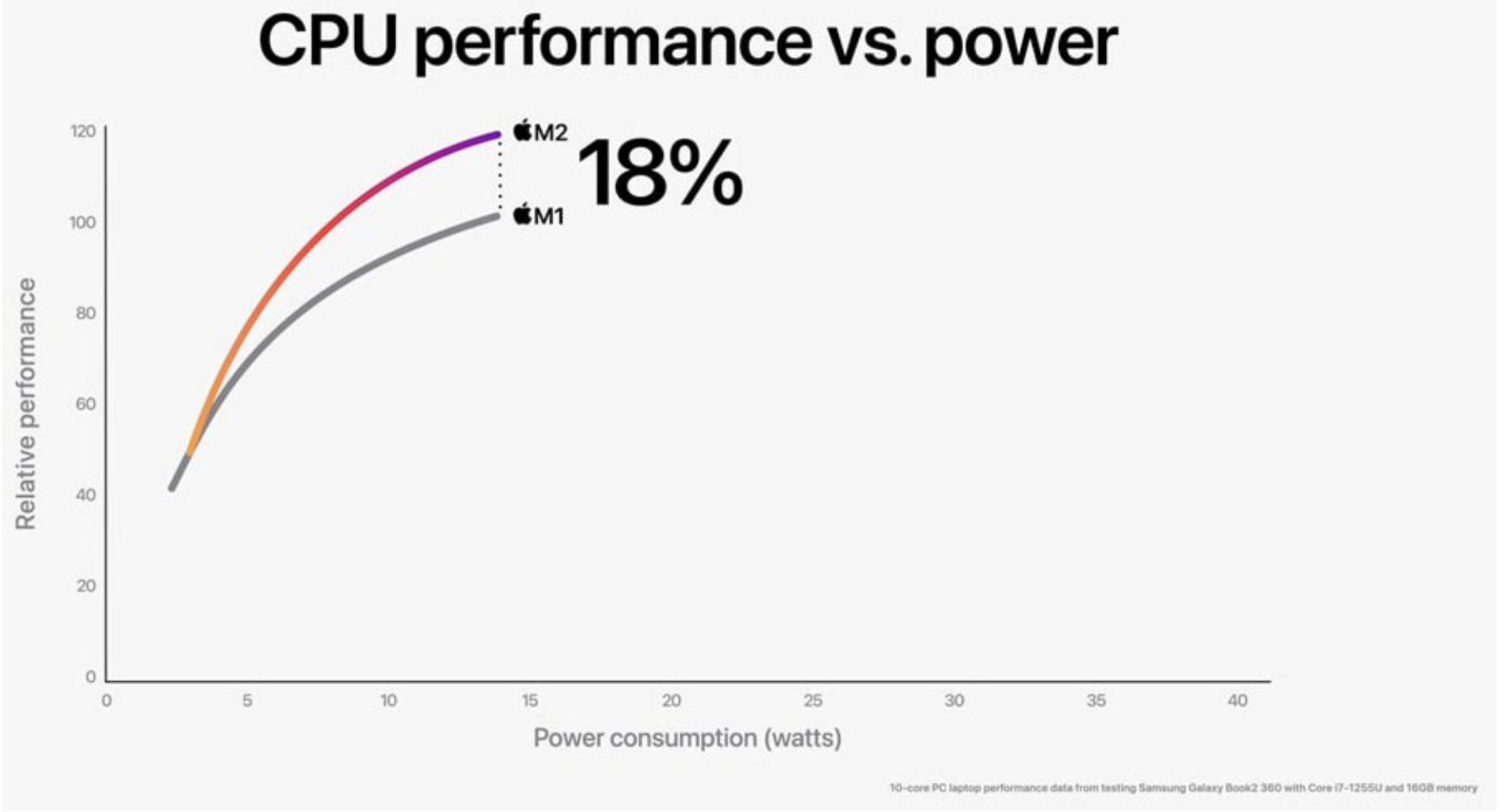
$$P(t) = I(t)V(t)$$

  - Switching power consumption

$$P_{switching} = \frac{CV_{DD}^2}{T} = CV_{DD}^2 f_{sw}$$

Apple M2 CPU performance

- Performance-power graph



(Apple)

5.2 Dynamic Power

5.2. Dynamic power (1)

- Estimate the switching power when operating at 1 GHz.
  - 1.0 V 65 nm process (λ is 25 nm.)
  - C = 1 fF/μm (gate) + 0.8 fF/μm (diffusion)
  - 50M logic transistors (Average width: 12λ), activity factor = 0.1
  - 950M memory transistors (Average width: 4λ)), activity factor = 0.02
  - Each transistor has a capacitance of 1.8 fF/μm.
  - For logic transistors, the capacitance is 27 nF.
  - For memory transistors, the capacitance is 171 nF.
  - The answer is 6.1 W.

5.2. Dynamic power (2)

- Remember that

$$P_{switching} = \alpha C V_{DD}^2 f$$

  - Try to minimize:
  - Activity factor (α)
  - Capacitance (C)
  - Suply voltage (V_{DD}^2)
  - Frequency (f)

5.2. Dynamic power (3)

- Activity factor estimation
  - Define P_i to be the probability that node i is 1. Also, $\overline{P_i} = 1 - P_i$.
  - Then,

$$\alpha_i = \overline{P_i}\, P_i$$

Assumption?

  - Completely random data has $P_i = 0.5$ and $\alpha = 0.25$. (It is the maximum value of $\overline{P_i}\, P_i$.)
  - Data is often not completely random.

5.2. Dynamic power (5)

- Switching probability
  - Activity factor of the output is $\overline{P_Y}\ P_Y$.

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \overline{P}_A \overline{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\overline{P}_A \overline{P}_B$
XOR2	$P_A \overline{P}_B + \overline{P}_A P_B$

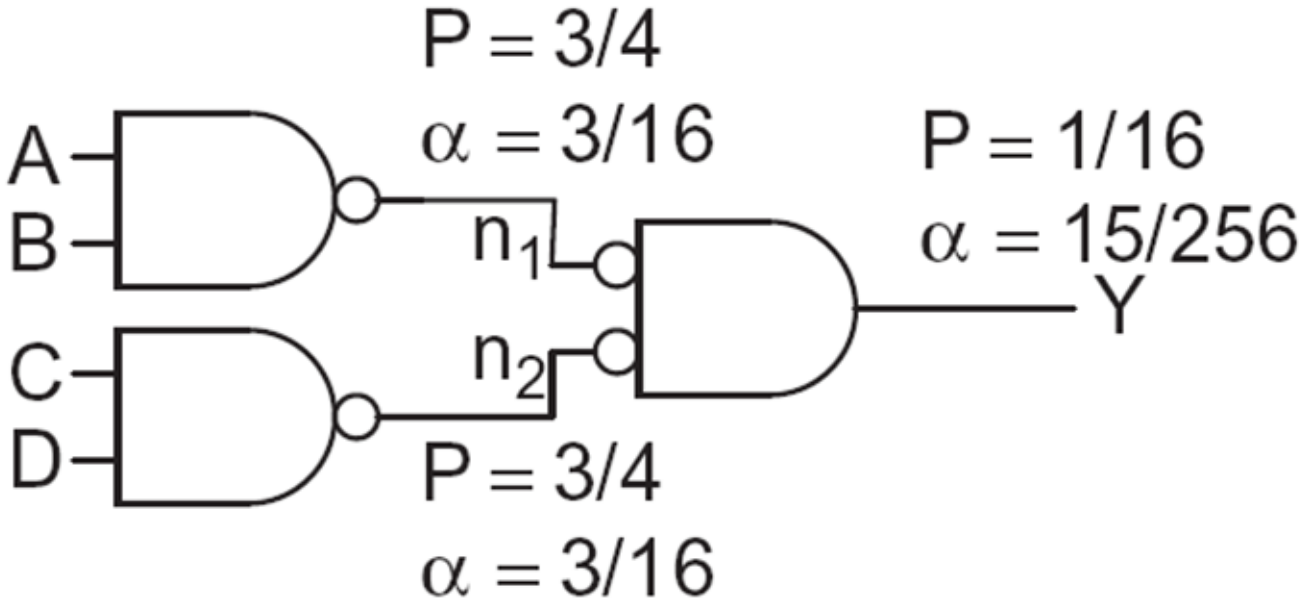
Table 5.1

5.2. Dynamic power (6)

- A 4-input AND
  - Two-level implementation

$$Y = \overline{\overline{AB} + \overline{CD}} = \overline{\overline{AB}}\,\overline{\overline{CD}} = ABCD$$

  - Estimate the activity factor at each node if the inputs have $P = 0.5$.



5.2. Dynamic power (7)

- Capacitance
- Gate capacitance (In this text, “gate” is not a contact.)
  - Fewer stages of logic
  - Small gate sizes
- Wire capacitance
  - Good floorplanning to keep communicating blocks close to each other
  - Drive long wires with inverters or buffers rather than complex gates

5.2. Dynamic power (8)

- Voltage domains
  - Provide separate supplies to different blocks
  - Level converters required when crossing from low to high V_{DD} domains

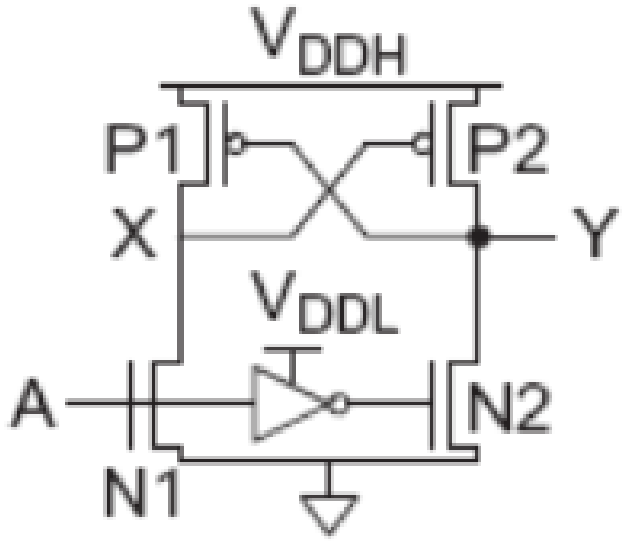


Fig. 5.15

- Frequency
  - Dynamic power is directly proportional to frequency. A chip should not run faster than neccessary.

Thank you!