Digital Integrated Circuit
Lecture 9 MOS Transistor Theory

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Review of Previous Lecture

Lecture 8

- Nonideal IV
  - Analysis on the velocity saturation

$$V_{dsat} = \frac{V_{GT}V_c}{V_{GT} + V_c}$$

$$V_c = E_c L$$

$$I_{dsat} = C_{OX}W\frac{V_{GT}^2}{V_{GT} + V_c}v_{sat}$$

  - Body effect

2.4 Nonideal IV

2.4. Nonideal IV (13)

- Leakage
  - Subthreshold slope

$$S = \left[\frac{d(\log_{10} I_d)}{dV_{gs}}\right]^{-1} = nv_T \ln 10$$

  - Drain-induced barrier lowering
  - Gate-induced drain leakage

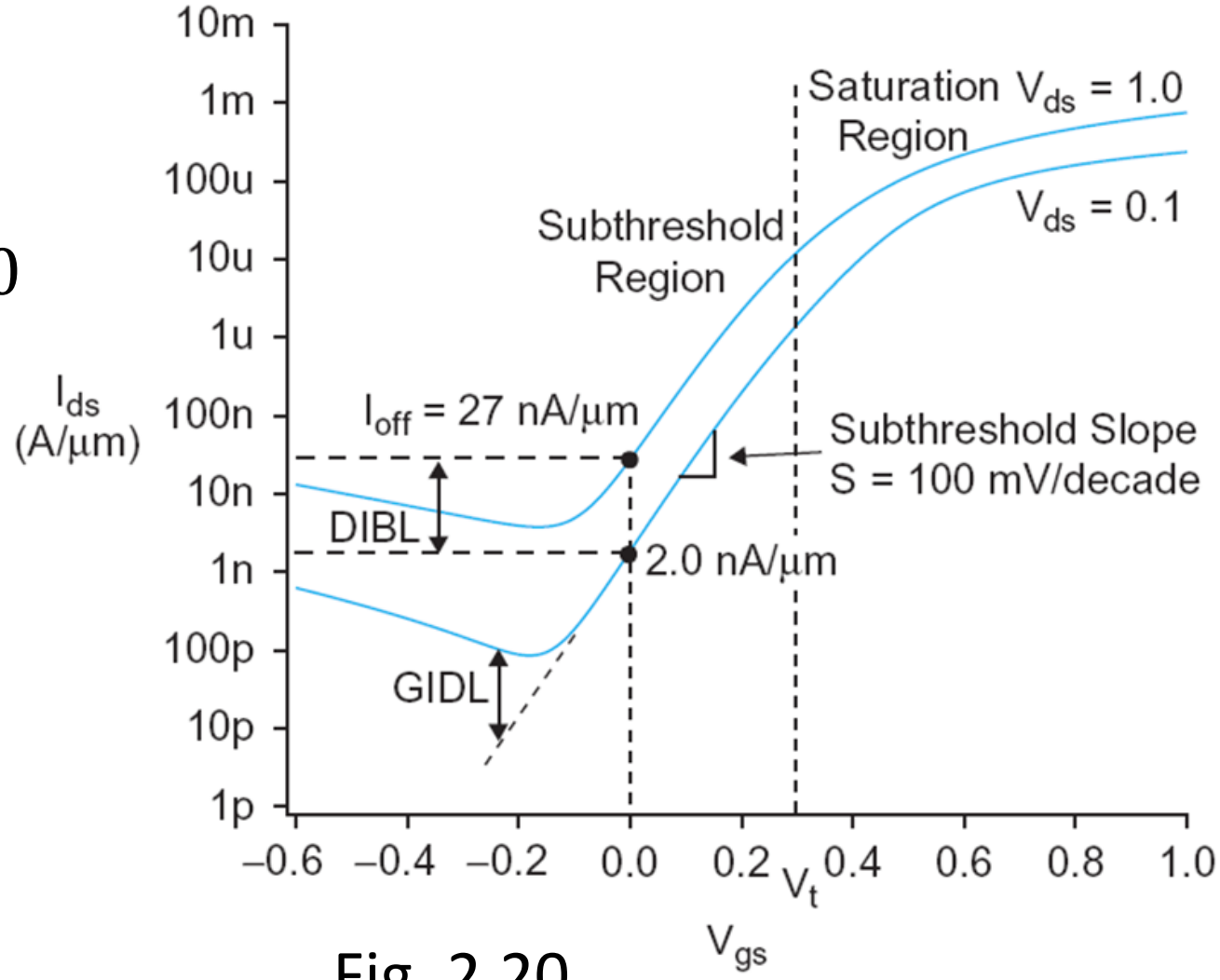


Fig. 2.20

2.5 DC Transfer

2.5. DC transfer (1)

- A CMOS inverter
  - The transistor is a switch with an infinite off-resistance and a finite on-resistance.

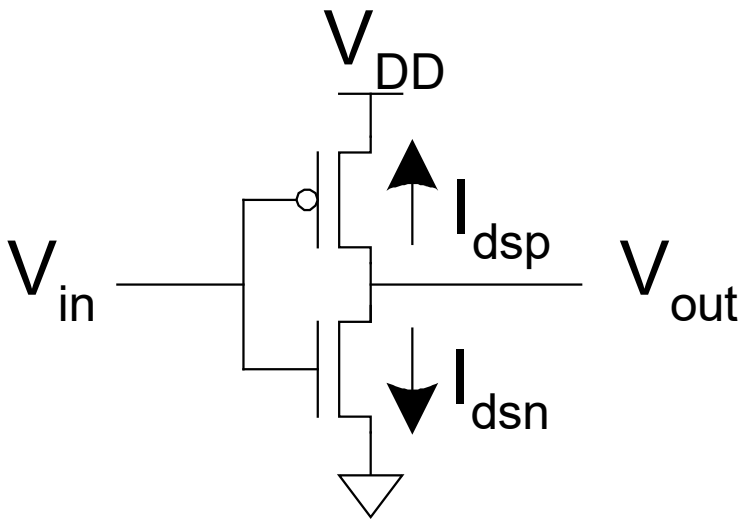
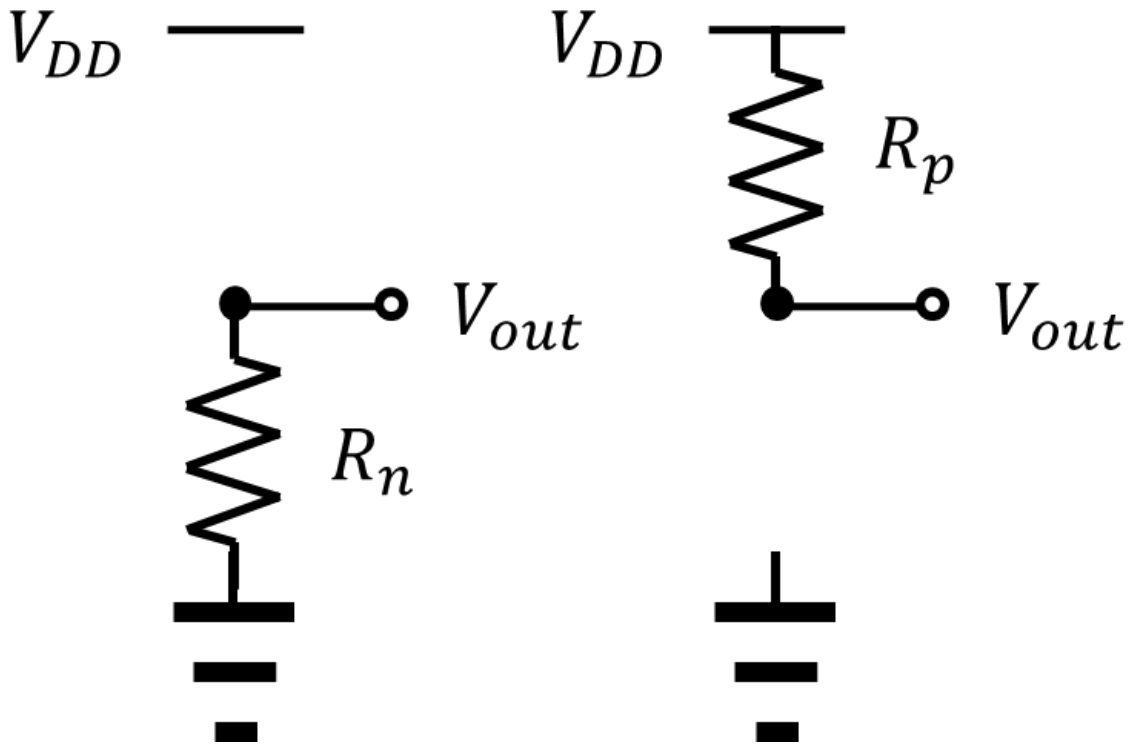


Fig. 2.25



2.5. DC transfer (2)

- Important properties (Taken from Rabaey's book)
  - The HIGH and LOW output levels equal V_{DD} and GND, respectively.
  - The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size. (Ratioless)
  - A well-designed CMOS inverter has a low output impedance.
  - The input resistance of the CMOS inverter is extremely high.
  - The absence of current flow between V_{DD} and GND means that the logic gate does not consume any static power.

2.5. DC transfer (3)

- We have five points. Identify the operational modes of transistors.

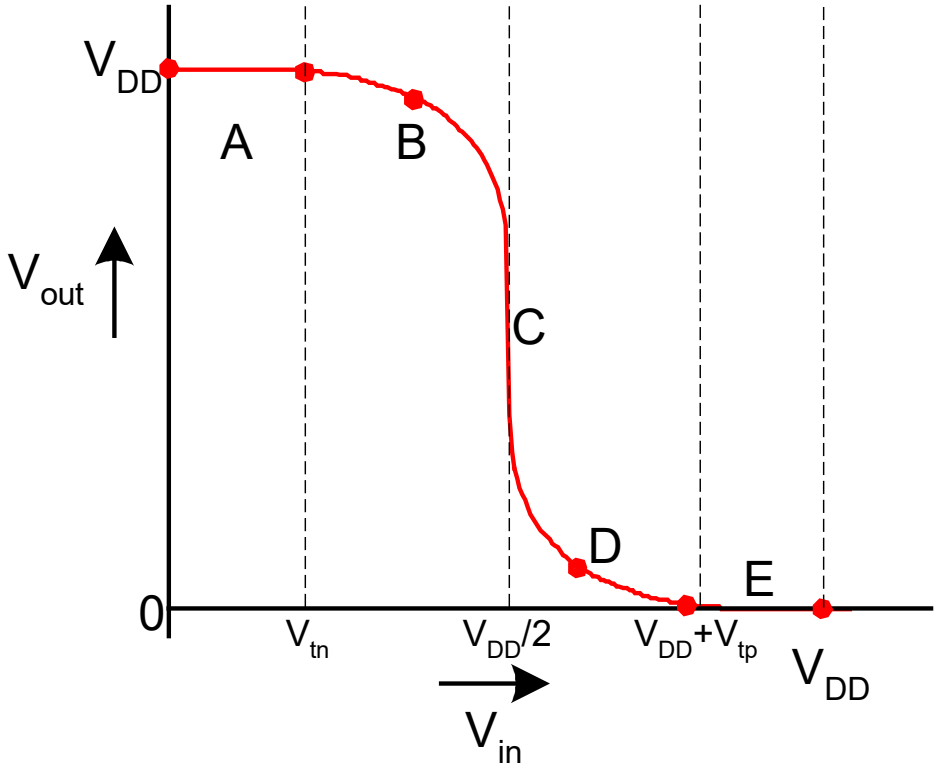


Fig. 2.26(c)

2.5. DC transfer (4)

- Input threshold, V_{inv} (or switching threshold)
  - When $V_{in} = V_{out} = V_{inv}$
- β ($\frac{W}{L}\mu C_{OX}$) ratio
  - HIGH-skewed, $\frac{\beta_p}{\beta_n} > 1$, stronger PMOS
  - LOW-skewed, $\frac{\beta_p}{\beta_n} < 1$, weaker PMOS

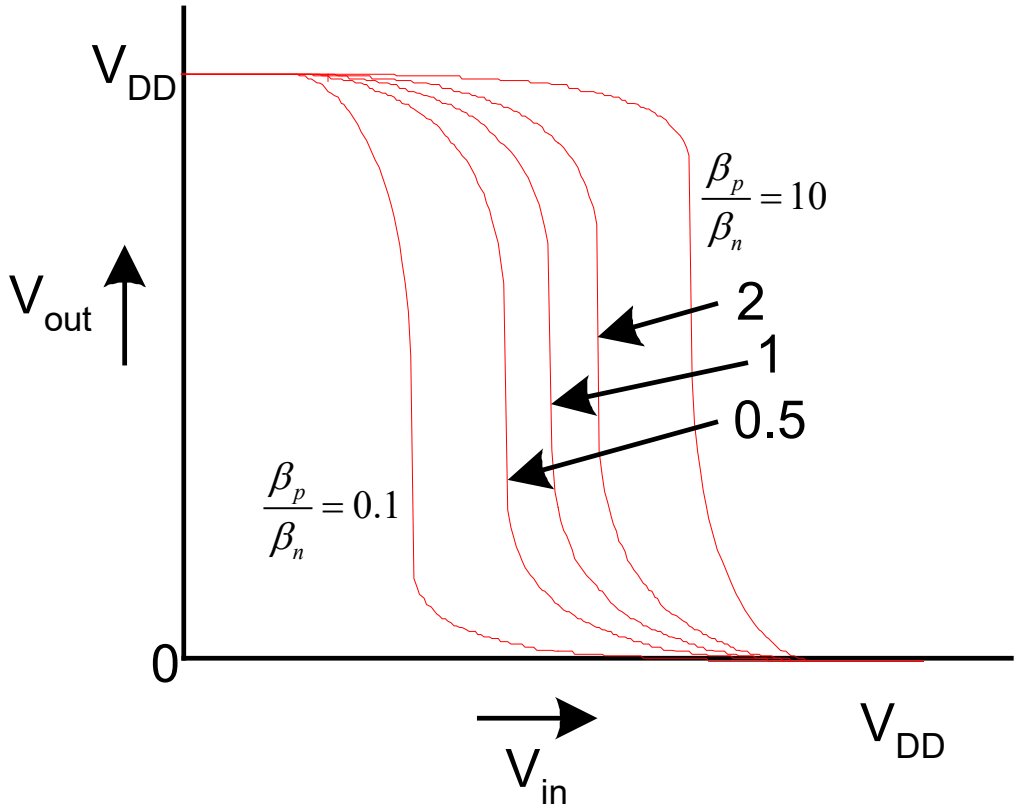


Fig. 2.28

2.5. DC transfer (5)

- Quantitative analysis for V_{inv}
  - Use the long-channel IV

$$I_{dn} = \frac{\beta_n}{2}(V_{inv} - V_{tn})^2 \text{ and } I_{dp} = -\frac{\beta_p}{2}\left(V_{inv} - V_{DD} - V_{tp}\right)^2$$

  - After manipulation, we have

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$

  - (Here, $r = \frac{\beta_p}{\beta_n}$)
  - For a special case with $r = 1$, $V_{inv} = \frac{V_{DD}+V_{tn}+V_{tp}}{2}$

2.5. DC transfer (6)

- Quantitative analysis for V_{inv} with velocity saturation
  - Use the following expressions:

$$I_{dn} = W_n C_{ox} v_{sat-n}(V_{inv} - V_{tn})$$
$$I_{dp} = -W_p C_{ox} v_{sat-p}(V_{inv} - V_{DD} - V_{tp})$$

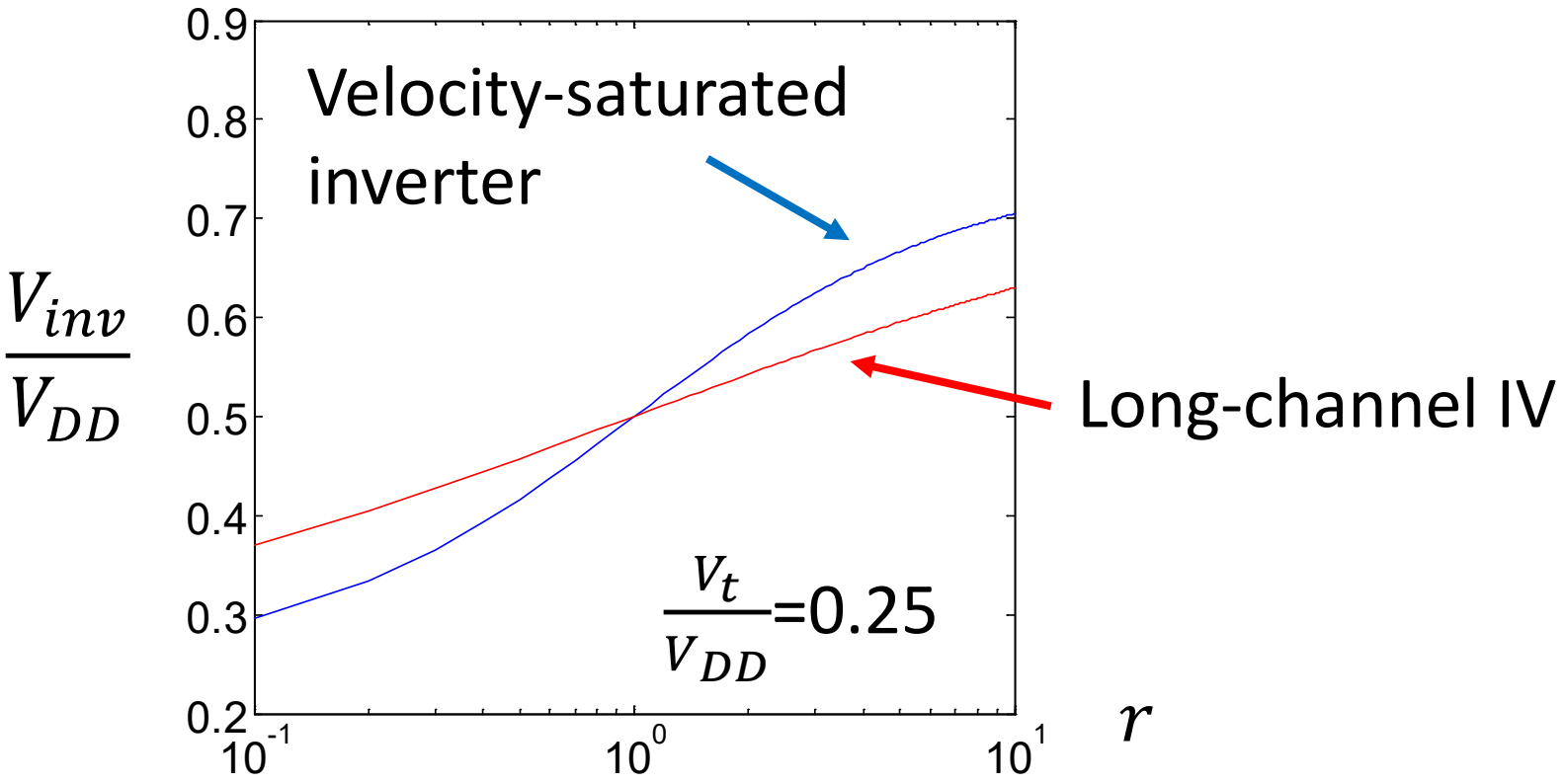
  - After manipulation, we have

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}}$$

  - (Here, $r = \frac{W_p v_{sat-p}}{W_n v_{sat-n}}$)
  - For a special case with $r = 1$, $V_{inv} = \frac{V_{DD}+V_{tn}+V_{tp}}{2}$

2.5. DC transfer (7)

- Compare them.
  - Let's draw $\frac{V_{inv}}{V_{DD}}$ as a function of r. Assume that $V_t = V_{tn} = -V_{tp}$.



2.5. DC transfer (8)

- Width ratio (Velocity-saturated inverter)
  - It is found that

$$r = \frac{W_p v_{sat-p}}{W_n v_{sat-n}} = \frac{V_{inv} - V_{tn}}{V_{DD} - V_{tp} - V_{inv}}$$

  - The width ratio is given by

$$\frac{W_p}{W_n} = \frac{v_{sat-n}(V_{inv} - V_{tn})}{v_{sat-p}\left(V_{DD} - V_{tp} - V_{inv}\right)}$$

2.5. DC transfer (9)

- Noise margin
  - Two unity gain points
  - Input voltage is V_{IL}.
  - Input voltage is V_{IH}.

  - In this case,
    $NL_L = V_{IL}$
    $NL_H = V_{DD} - V_{IH}$

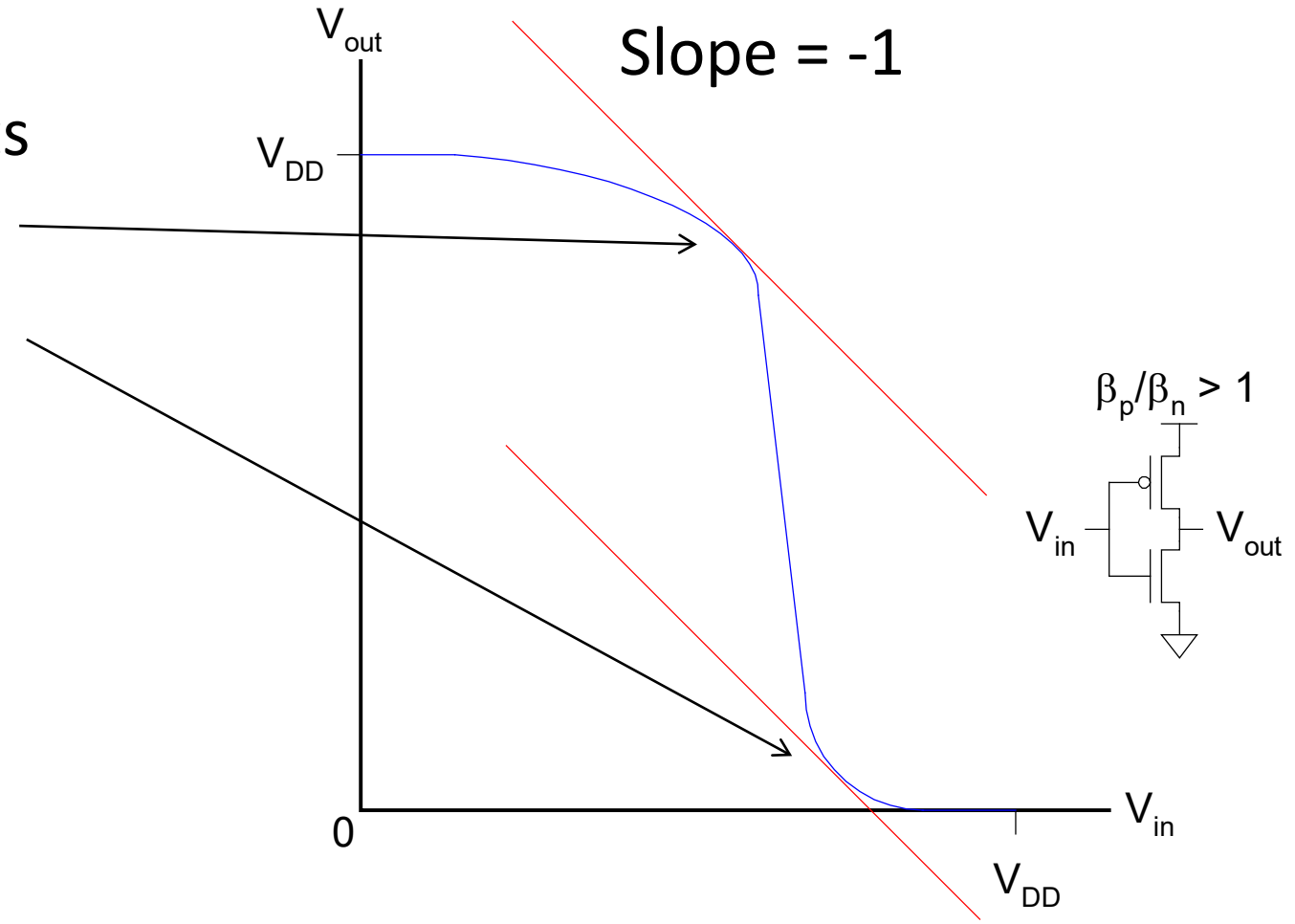


Fig. 2.30

Homework#3

- Due: AM08:00, October 5
- Problem#1
  - Calculate V_{IL} with the ideal IV characterstics. It can be found from a condition of $\frac{dV_{out}}{dV_{in}} = -1$. Neglect the channel length modulation. Assume $\mu_n C_{OX} \frac{W_n}{L_n} = \mu_p C_{OX} \frac{W_p}{L_p}$ and $V_{tn} = -V_{tp}$ for simplicity.
  - Hint: The NMOSFET is in the saturation mode, while the PMOSFET in the linear mode.

Homework#3

- Problem#2
  - Using the solution of Problem#1, calculate V_{IL} when V_{DD} is 1.8 V and V_{tn} is 0.5 V.

Thank you!