Digital Integrated Circuit
Lecture 18 Interconnect

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Review of Previous Lecture

Lecture 17

- Static power
  - Two major causes of the leakage current are the subthreshold current and the gate leakage current.
  - Subthreshold current: 60 mV/dec is the limiting value of the subthreshold slope.
  - Stack effect
  - Gate leakage current: Due to the tunneling. Extremely sensitive to the thickness. By introducing the high-k metal gate, it can be significantly reduced.

5.3. Static power (7)

- NAND3 leakage example (Leakage current in nA)

Input State (ABC)	I_{sub}	I_{gate}	I_{total}	V_x	V_z
000	0.4	0	0.4	stack effect	stack effect
001	0.7	0	0.7	stack effect	$V_{DD} - V_t$
010	0.7	1.3	2.0	intermediate	intermediate
011	3.8	0	3.8	$V_{DD} - V_t$	$V_{DD} - V_t$
100	0.7	6.3	7.0	0	stack effect
101	3.8	6.3	10.1	0	$V_{DD} - V_t$
110	5.6	12.6	18.2	0	0
111	28	18.9	46.9	0	0

Table 5.2

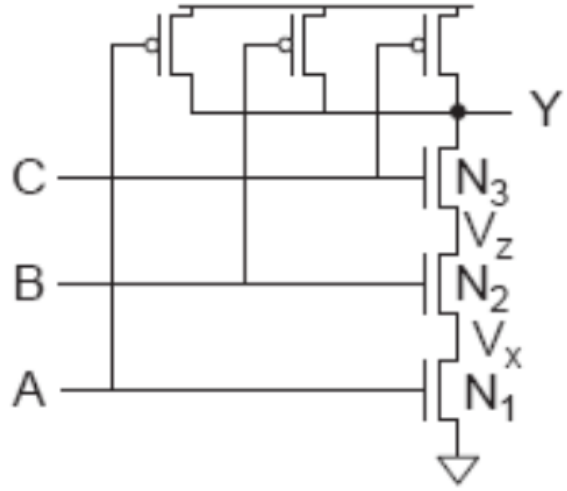


Fig. 5.23

5.3. Static power (8)

- Power gating
  - Turn OFF power to block when they are idle.
  - Use virtual V_{DD} (V_{DDV})
  - Gate outputs to prevent invalid logic level to next block

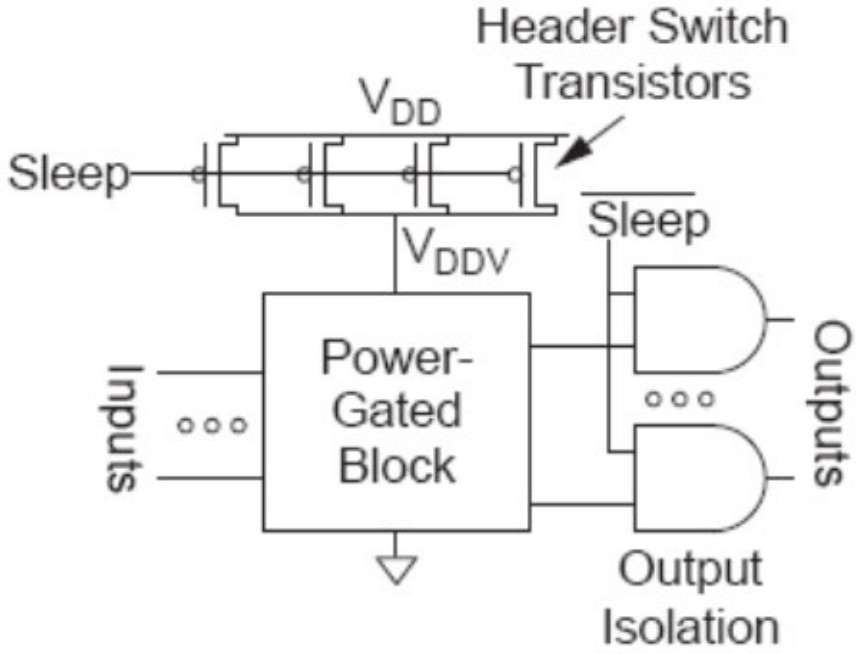


Fig. 5.24

6.1 Introduction

6.1. Introduction (1)

- Wire geometry
  - Pitch = $w + s$
  - Aspect ratio (AR) = $\frac{t}{w}$
  - Older processes had AR << 1.
  - Modern processes have AR ≈ 2.

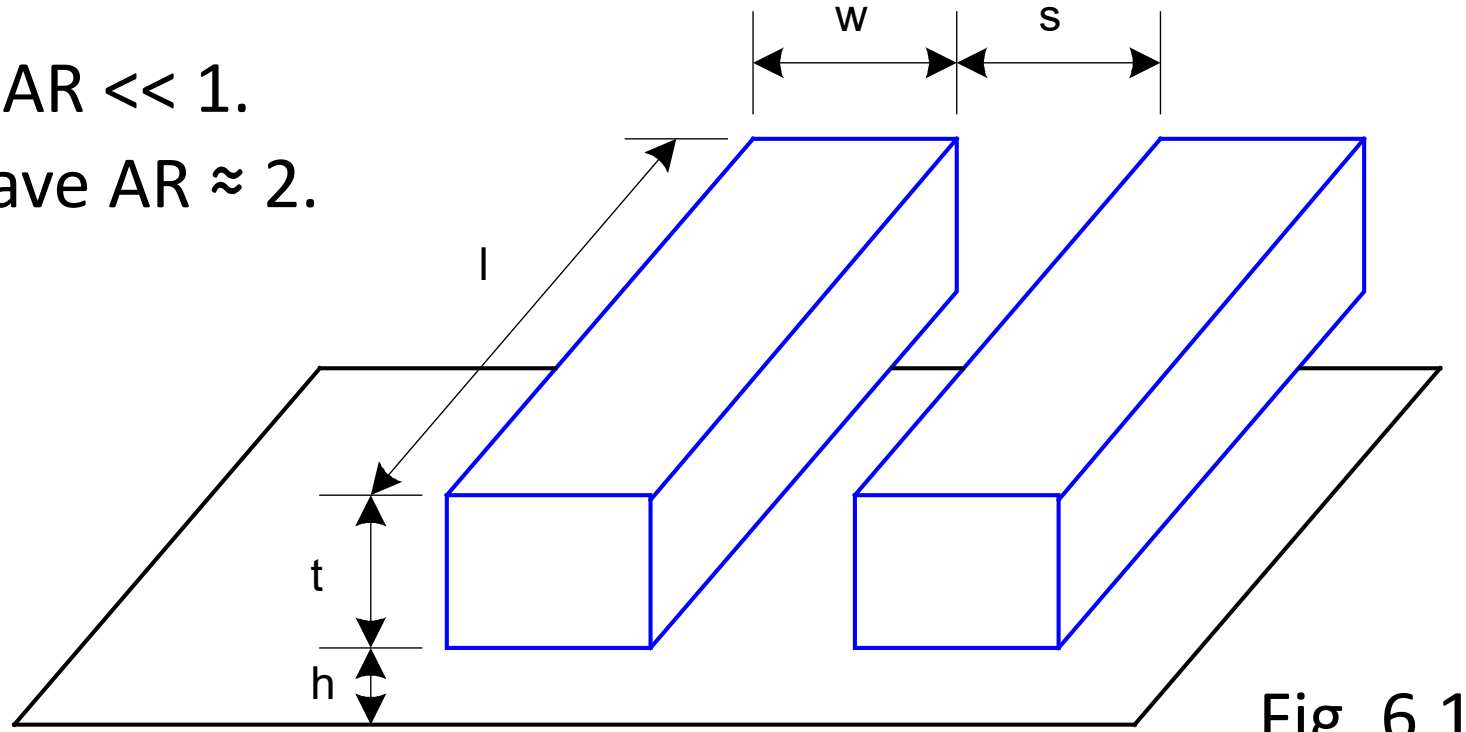


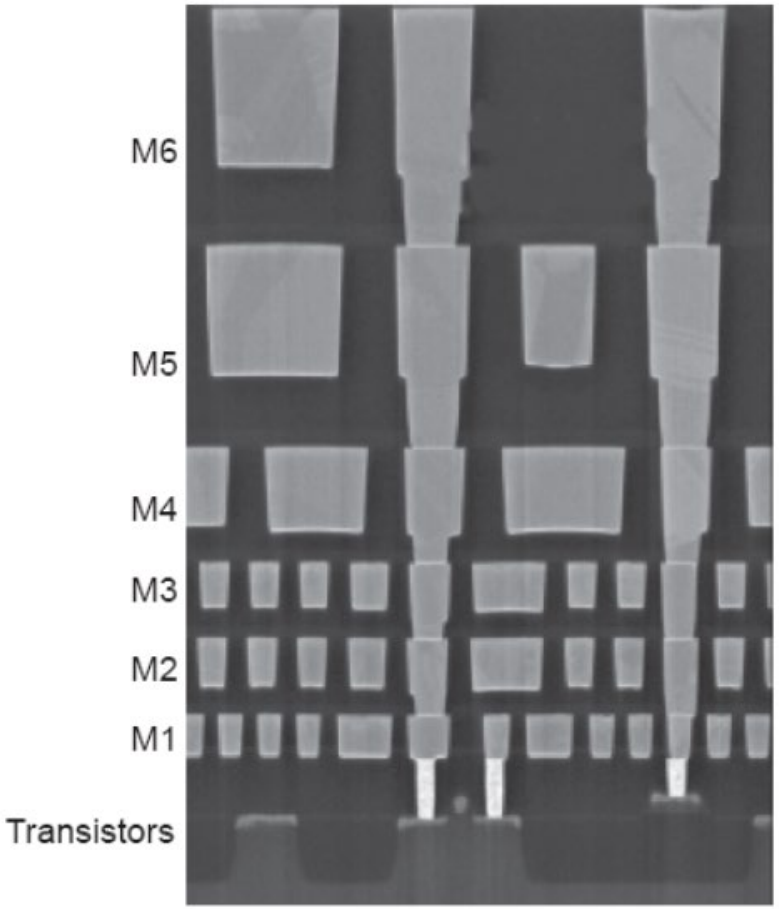
Fig. 6.1

6.1. Introduction (2)

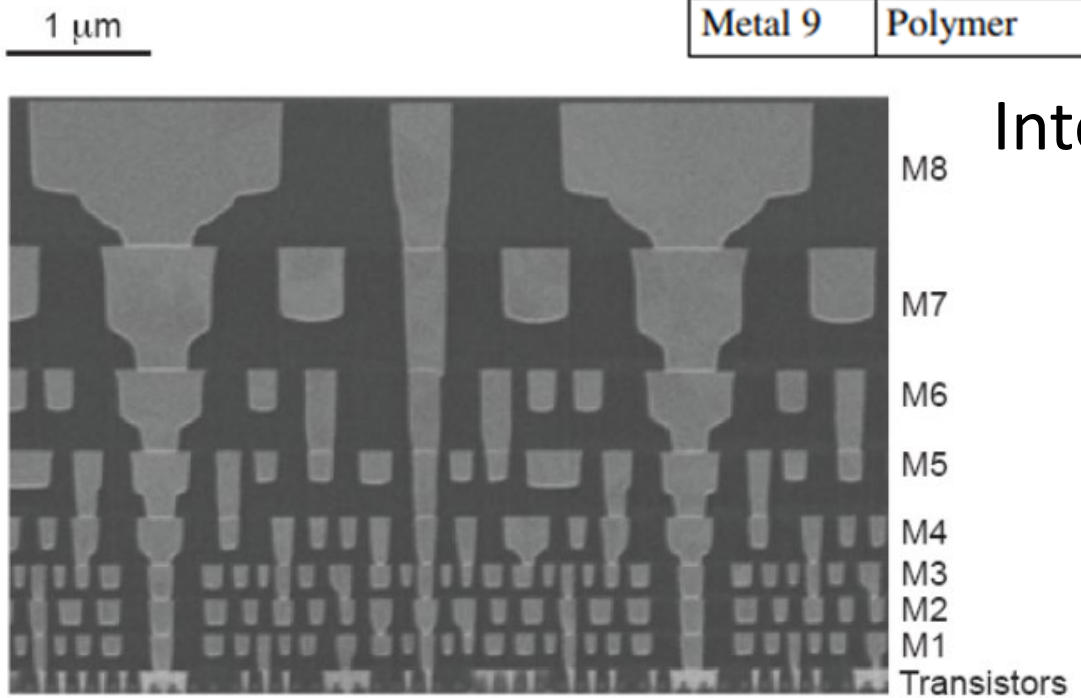
- Example: Intel metal stacks

Layer	Dielectric Material	Pitch (nm)	Thick (nm)	Aspect Ratio
Metal 1	Low k	160	144	1.8
Metal 2	Low k	160	144	1.8
Metal 3	Low k	160	144	1.8
Metal 4	Low k	240	216	1.8
Metal 5	Low k	280	252	1.8
Metal 6	Low k	360	324	1.8
Metal 7	Low k	560	504	1.8
Metal 8	SiO_2	810	720	1.8
Metal 9	Polymer	30.5µm	7µm	0.4

Intel 45 nm metal stack



90 nm technology

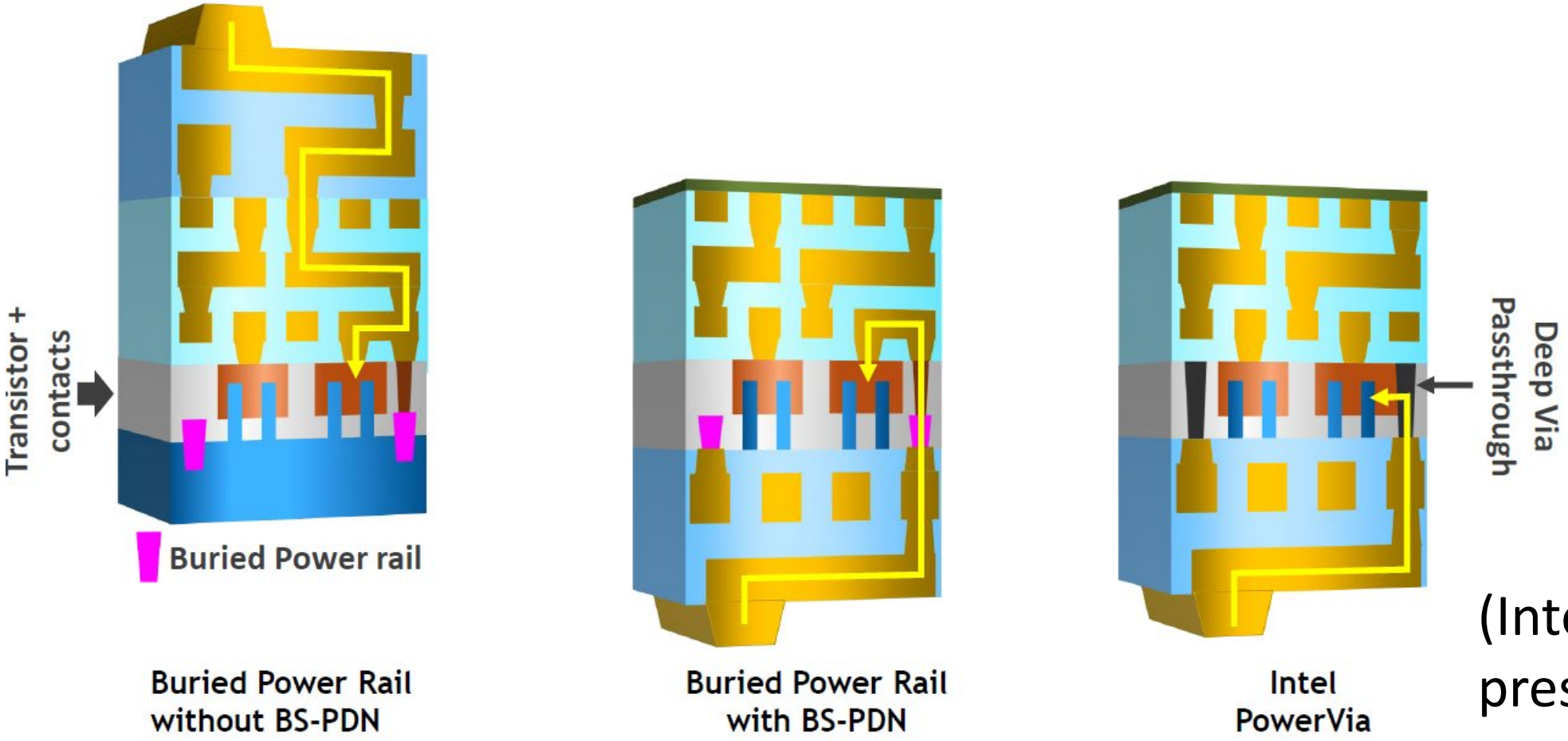


45 nm technology

Fig. 6.2

6.1. Introduction (3)

- Backside power delivery network (BSPDN)
  - The hottest topic in VLSI in these days!



(Intel's VLSI 2023 presentation)

6.2. Interconnect modeling (1)

- Lumped element models
  - A wire is a distributed circuit with a resistance and capacitance per unit length.

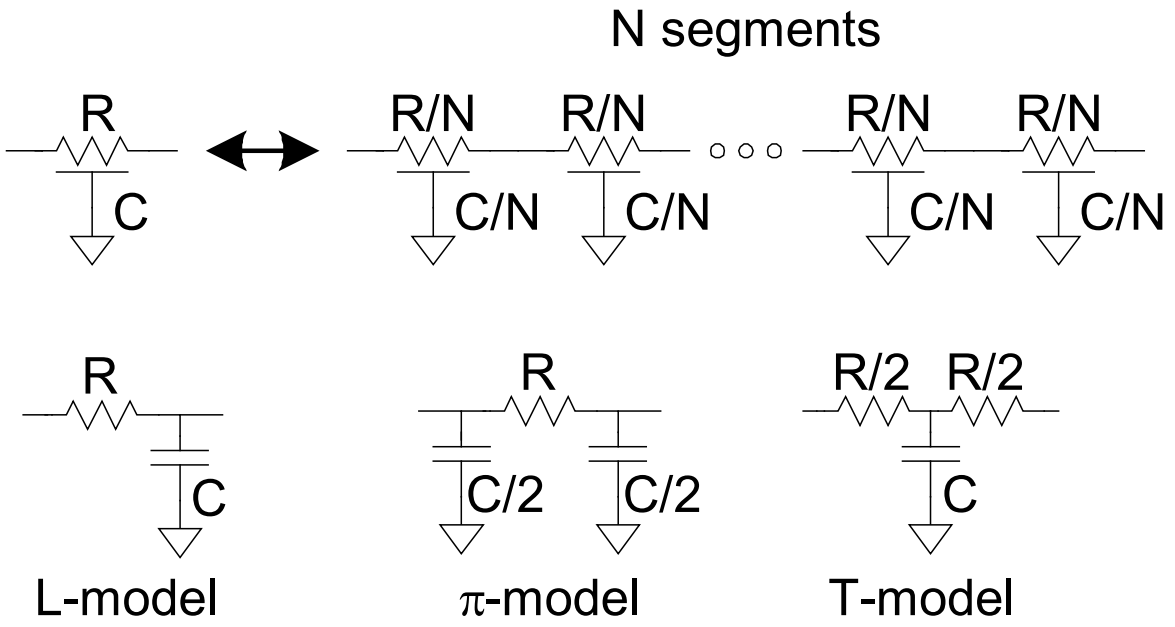


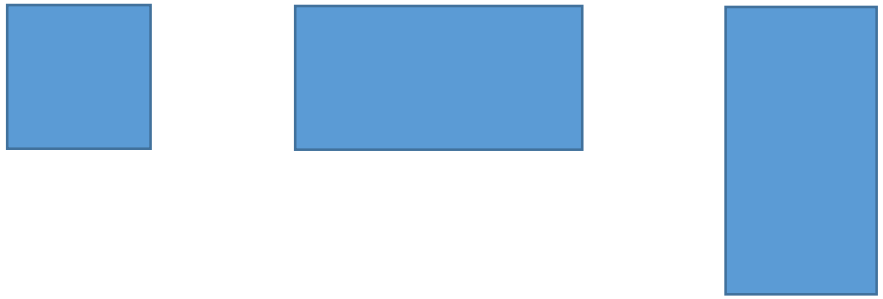
Fig. 6.5

6.2. Interconnect modeling (2)

- Wire resistance
  - Resistance of a wire

$$R = \frac{\rho}{t}\frac{l}{w} = R_{\square}\frac{l}{w}$$

  - $R_{\square}$ is the sheet resistance.



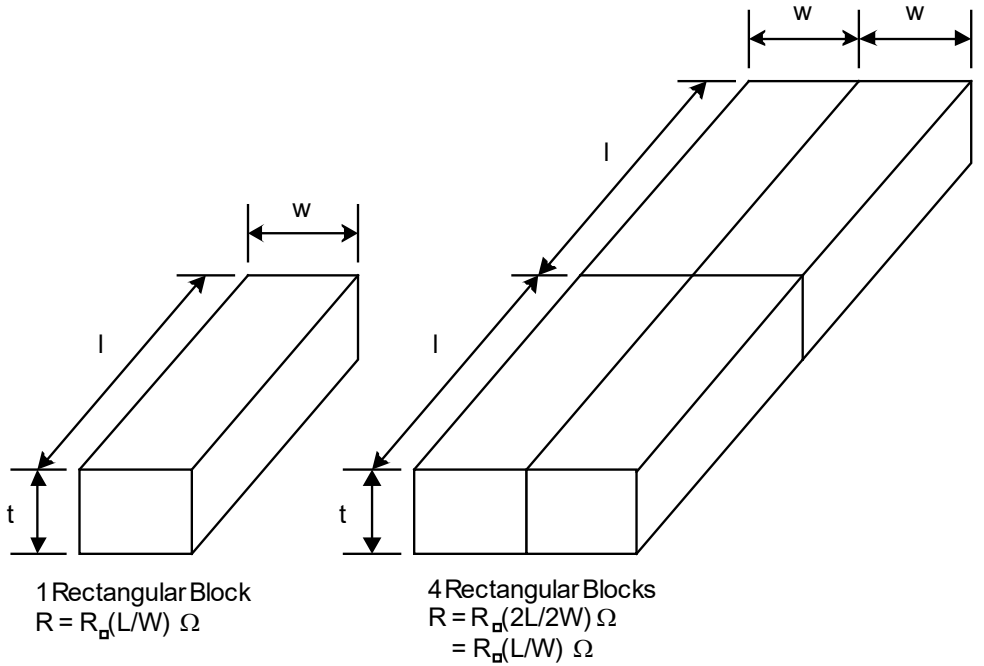


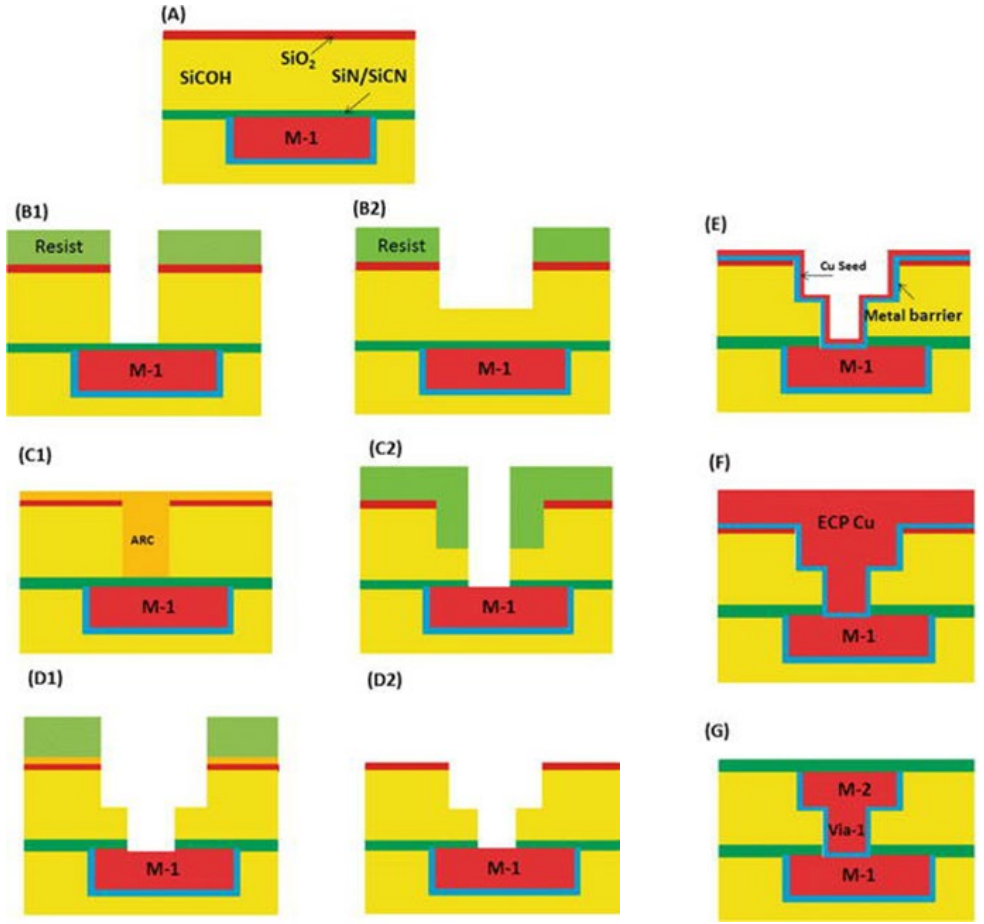
Fig. 6.6

6.2. Interconnect modeling (3)

- Al versus Cu
  - Dual damascene process

Metal	Bulk resistivity ($\mu\Omega \cdot cm$)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Titanium (Ti)	43.0

Table 6.2



(Chang et al., "Copper metal for semiconductor interconnects")

6.2. Interconnect modeling (4)

- Wire capacitance
  - For a parallel plate, $C = \epsilon_{ox} \frac{A}{d}$

$$C_{total} = C_{top} + C_{bot} + 2C_{adj} \approx \epsilon_o l \left[2k_{vert} \frac{w}{h} + 2k_{horiz} \frac{t}{s} \right] + C_{fringe}$$

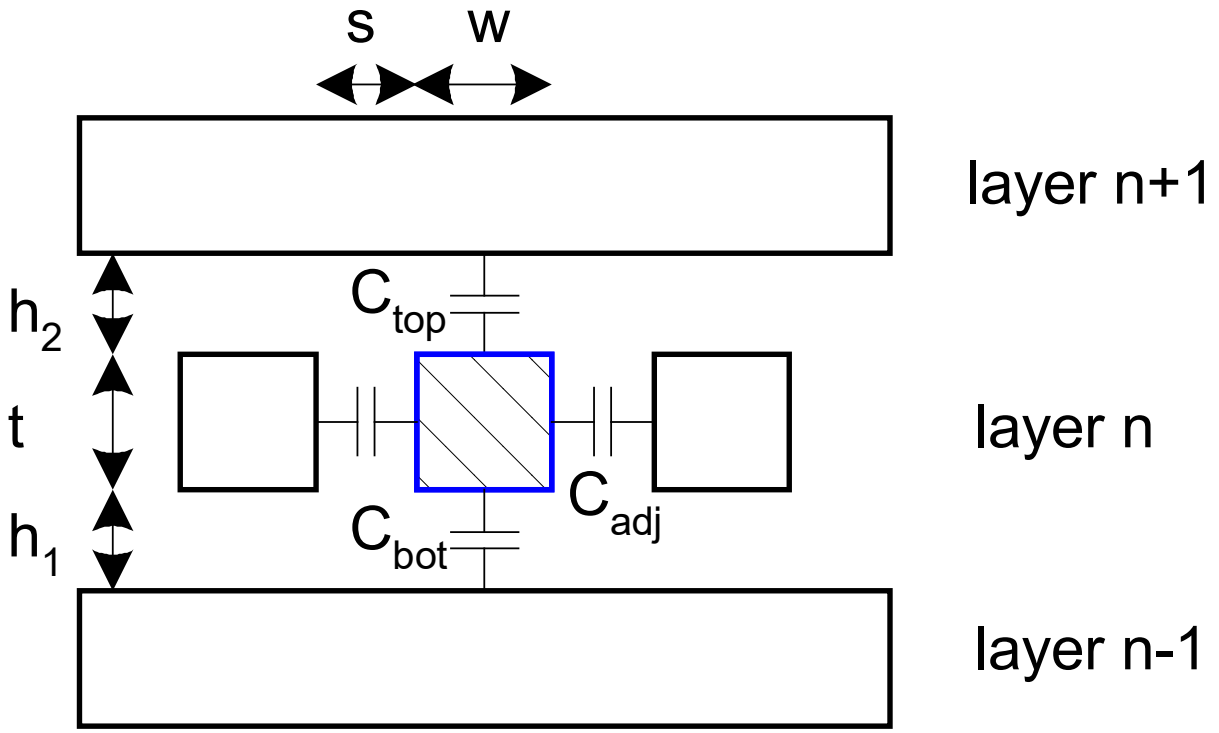


Fig. 6.11

6.2. Interconnect modeling (5)

- M2 capacitance data (180nm process)
  - Wire and oxide thicknesses of 0.7 µm
  - Minimun width/spacing of 0.32 µm
  - Typical dense wires have 0.2 fF/µm.

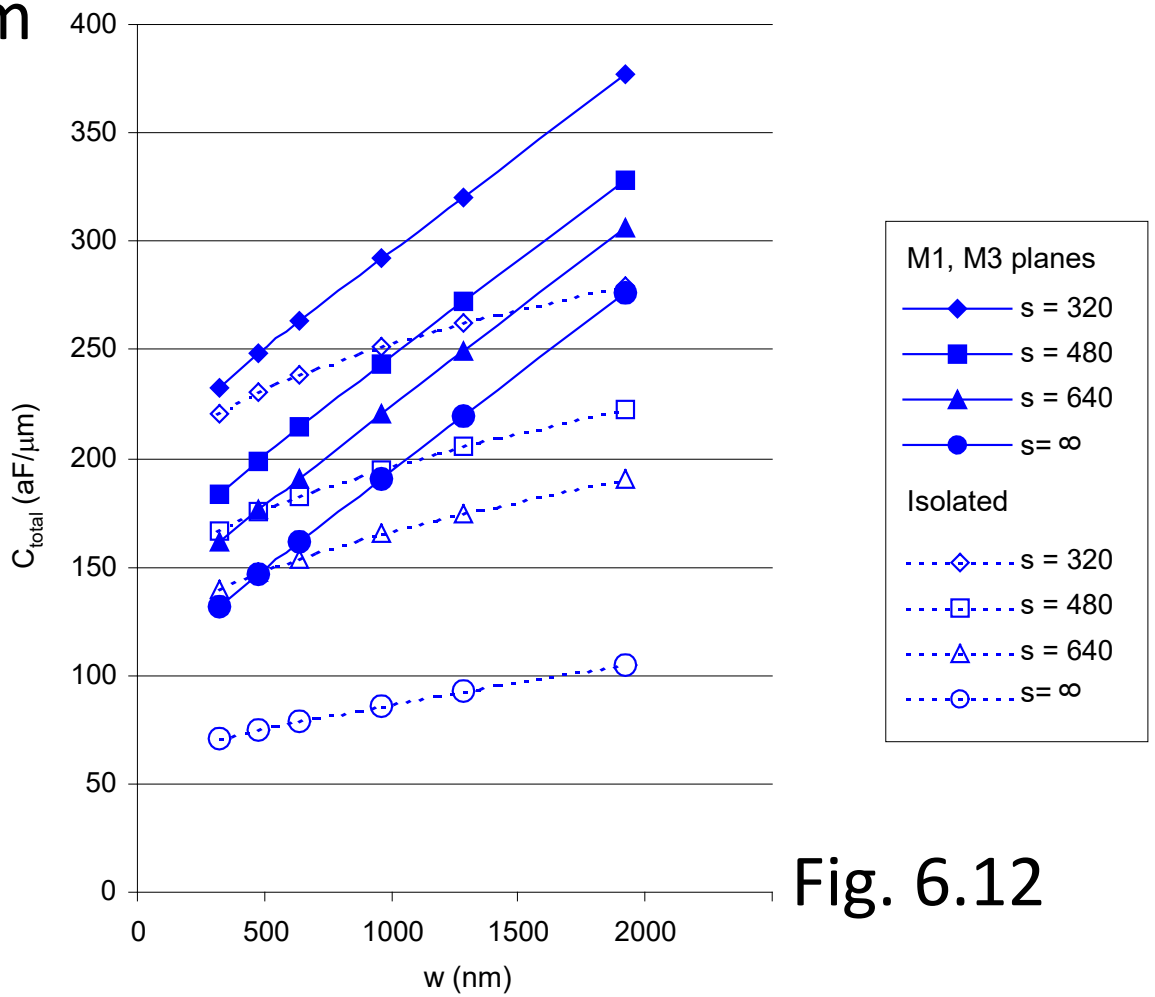


Fig. 6.12

Thank you!