# Digital Integrated Circuit
# Lecture 24 Sequential Circuit Design

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# Review of Previous Lecture

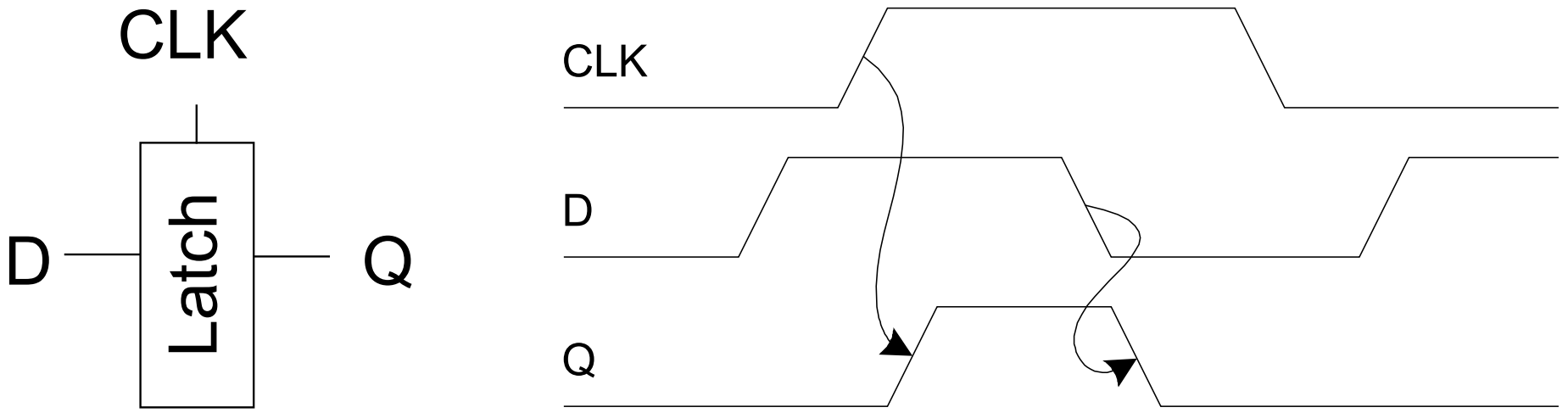
# Lecture 23

- Dynamic circuits
  - "Clocked" pull-up
  - *Precharge* and *evaluate*
  - Domino logic

# 10.2 Sequencing Static Circuits

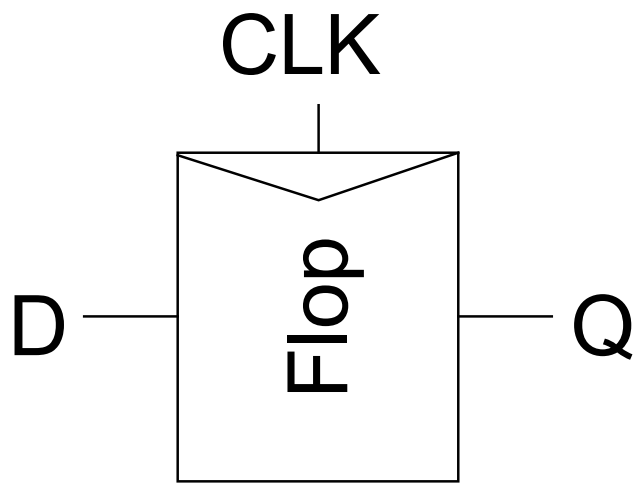
# 10.2. Sequencing static circuits (1)

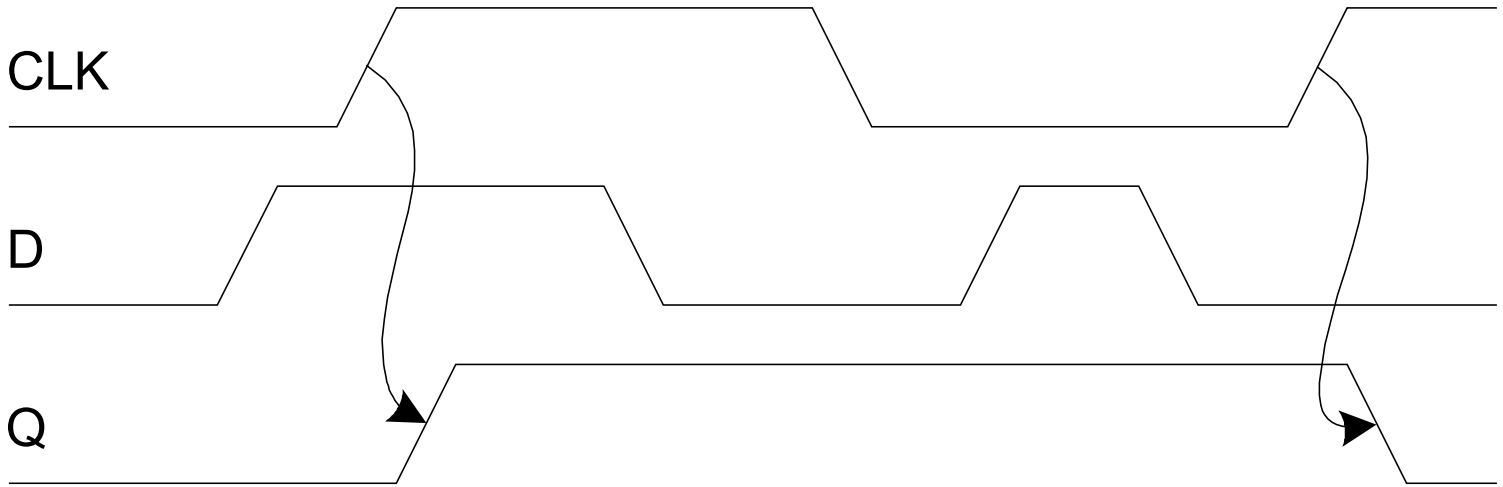
- Latches
  - When CLK=1, the latch is transparent. D flows through to Q like a buffer.
  - When CLK=0, the latch is opaque. The latch holds its present Q output even if D changes.



# 10.2. Sequencing static circuits (2)

- Flip-flops (An edge-triggered device)
  - It copies D to Q on the rising edge of the clock.
  - It ignores D at all other time.



# 10.2. Sequencing static circuits (3)

- Static sequencing methods

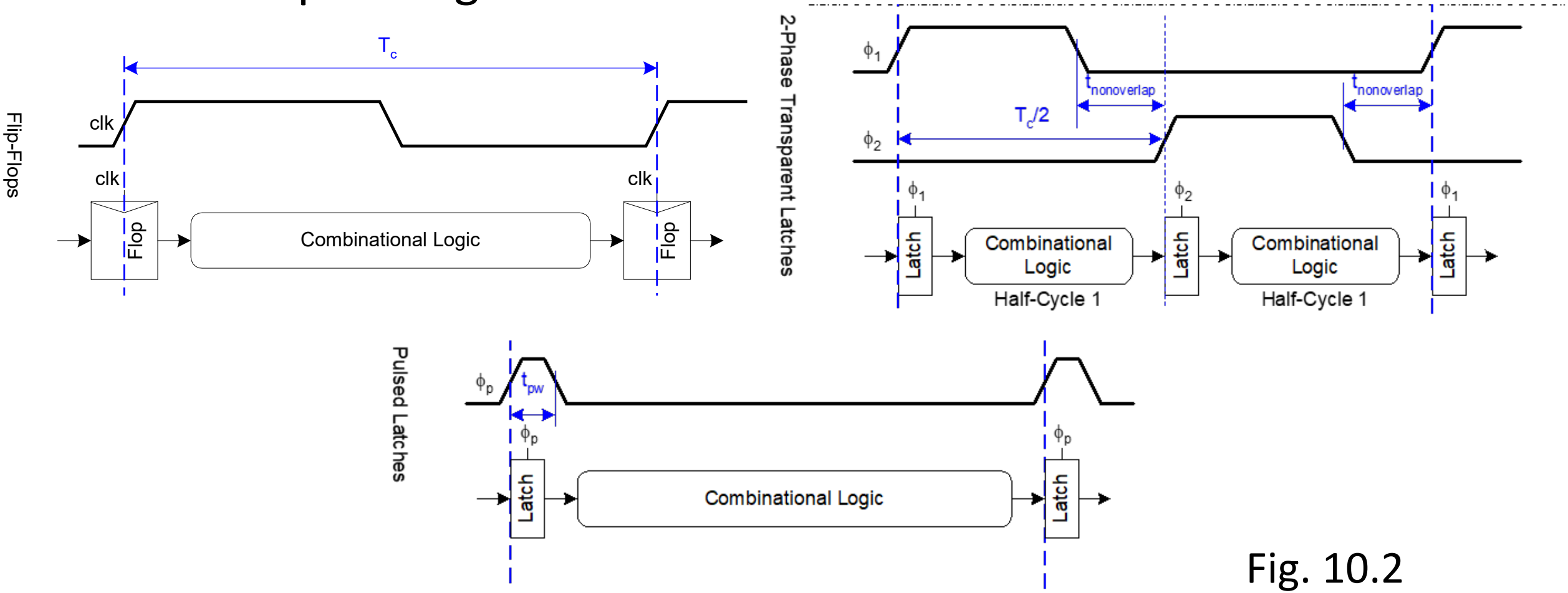



Fig. 10.2

# 10.3 Circuit Design of Latches and Flip-Flops

# 10.3. Circuit design of latches and flip-flops (1)

- A very simple transparent latch built from a single transistor
  - It is compact and fast.
  - The output does not swing from rail-to-rail. (From GND to $V_{DD}$) It never raises above $V_{DD} - V_t$.
  - The output floats when the latch is opaque.
  - D drives the diffusion input of a pass transistor.
  - The state node is exposed, so noise on the output can corrupt the state.

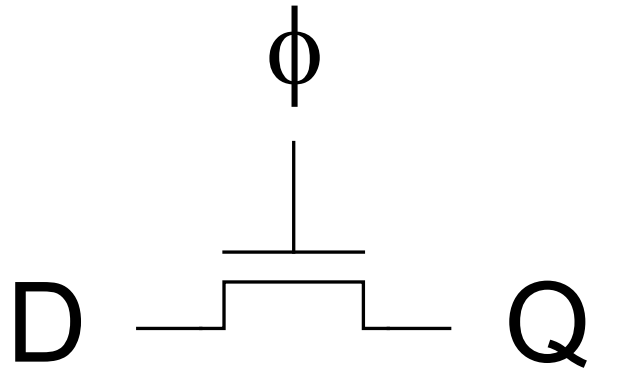



Fig. 10.17(a)

# 10.3. Circuit design of latches and flip-flops (2)

- CMOS transmission gate
  - It offers rail-to-rail output swings.
  - It requires a complementary clock, $\overline{\phi}$, which can be provided as an additional input or locally generated from $\phi$ through an inverter.

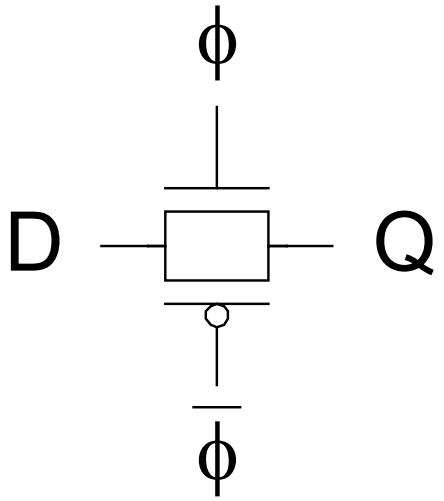



Fig. 10.17(b)

# 10.3. Circuit design of latches and flip-flops (3)

- Inverting latch
  - Fast dynamic latches

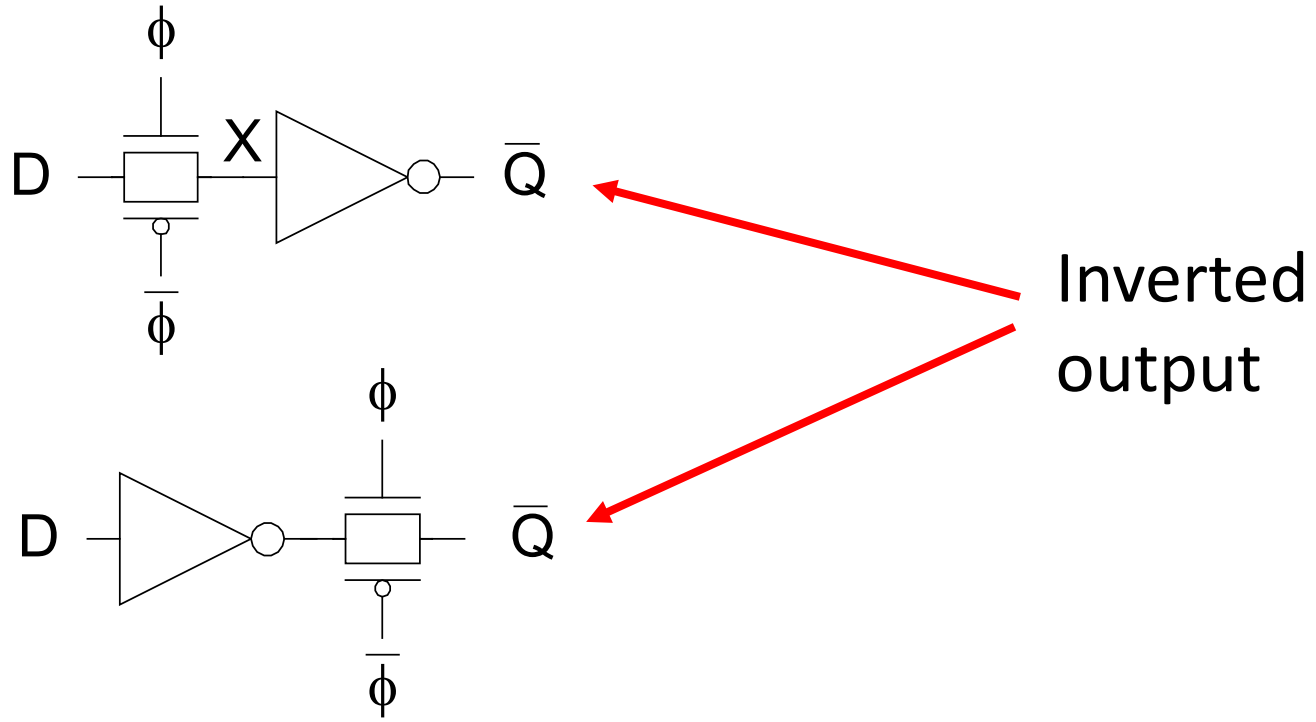
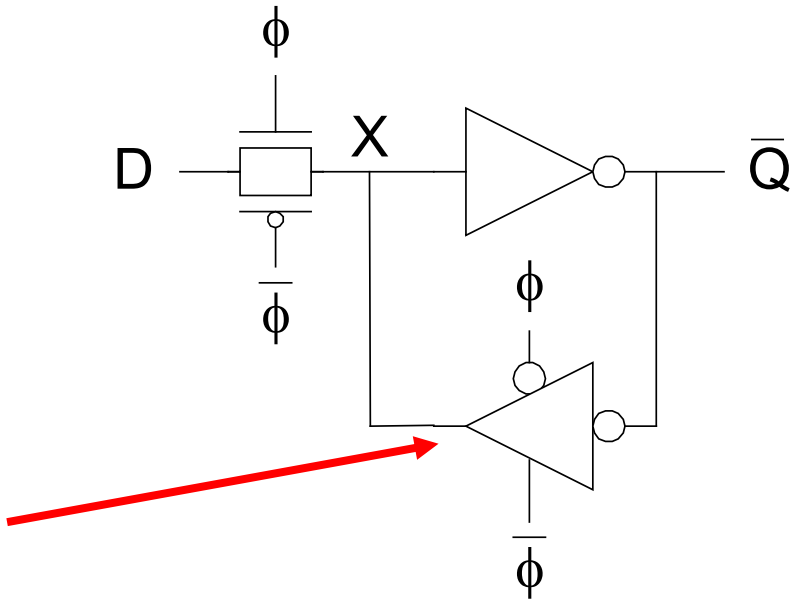



Fig. 10.17(c) and (d)

# 10.3. Circuit design of latches and flip-flops (4)

- Static latch, having feedback to prevent the output from floating
  - When CLK=1, the latch is transparent.
  - When CLK=0, the feedback tristate turns ON, holding X at the correct level.




Feedback tristate

Fig. 10.17(e)

# 10.3. Circuit design of latches and flip-flops (5)

- Buffered input
  - The input is a transistor gate rather than unbuffered diffusion.
  - It is noninverting.
  - A large noise spike on the output can propagate backward through the feedback gate and corrupt the state node X.

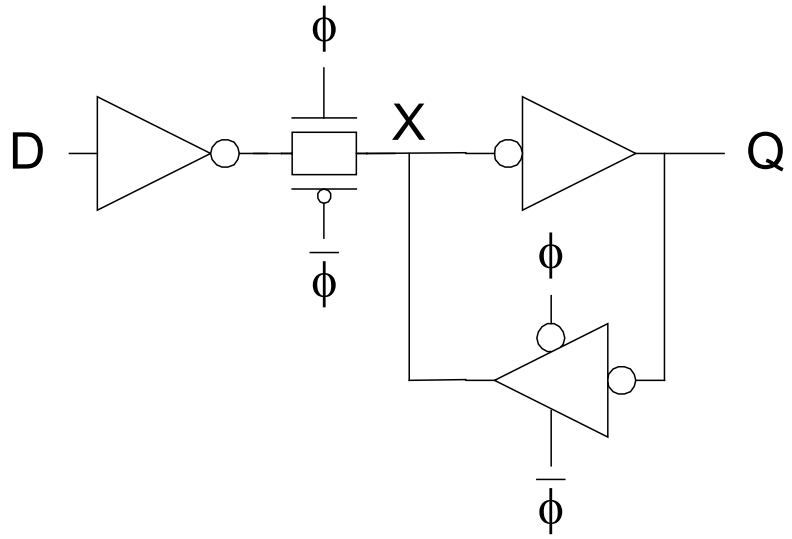
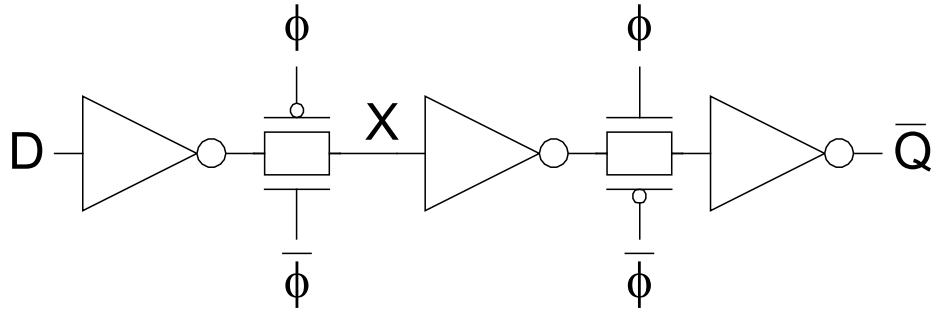



Fig. 10.17(e)

# 10.3. Circuit design of latches and flip-flops (6)

- A dynamic inverting flip-flop built from a pair of back-to-back dynamic latches



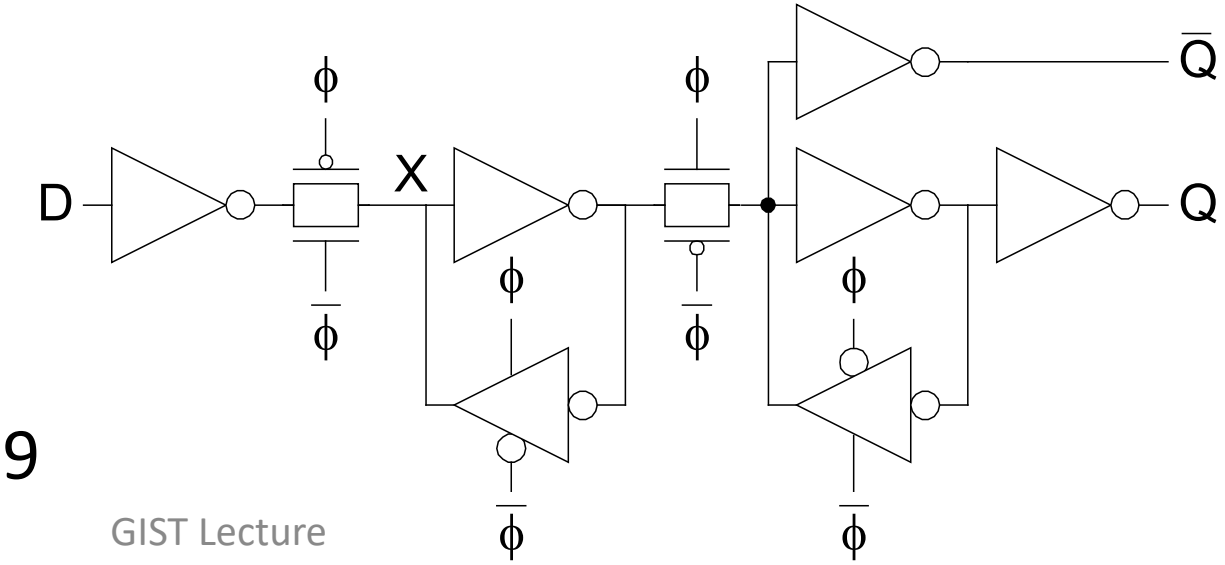




Fig. 10.19

# Thank you!