Digital Integrated Circuit
Lecture 1 Introduction

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Welcome

Welcome!

- Digital Integrated Circuit (디지털 집적회로)
  - Code: EC4202
  - Lecture 3, no experiment, credit 3

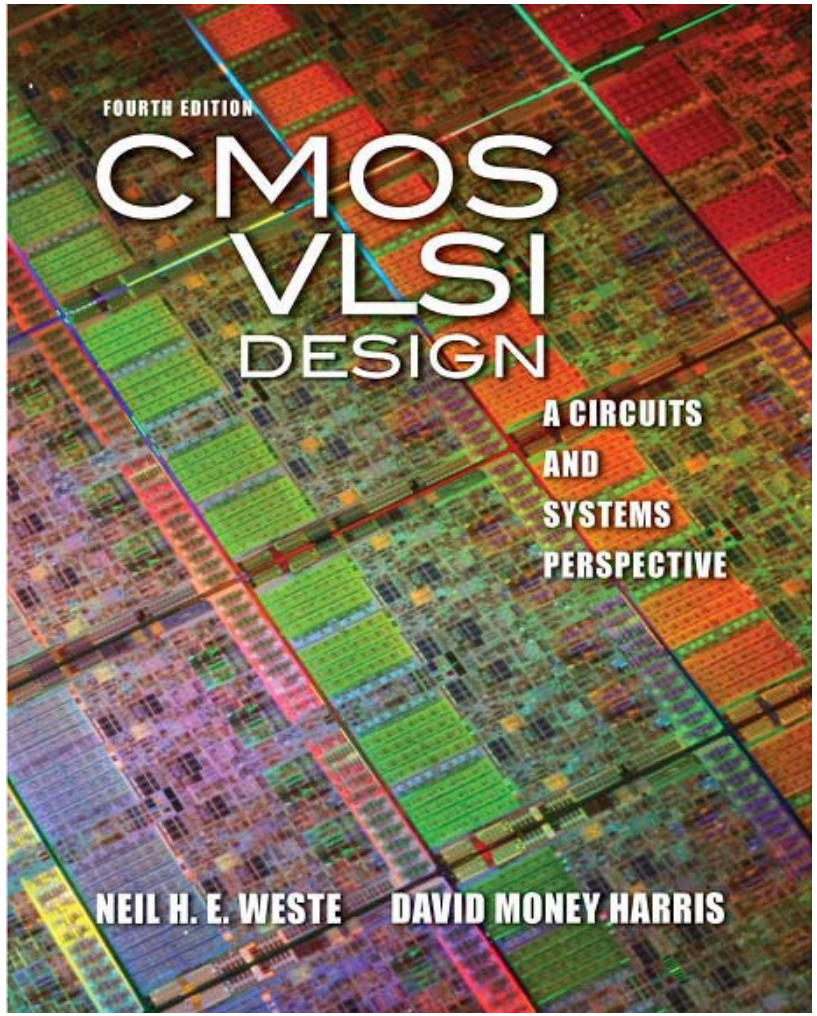
- Instructor: Sung-Min Hong
  - School of EECS

Resources

- Presentation materials
  https://github.com/hi2ska2/dic2023f
  – There is an archived repository for 2019.

- Homework submission
  – GIST LMS system

- YouTube channel
  https://www.youtube.com/@SungMinHong



Evaluation

- Attendance (10%)
- Homework (30%)
- Mid-term examination (30%)
- Final examination (30%)

1.3 MOS Transistors

1.3. MOS transistors (1)

- Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)
  - Four terminals: Gate, source, drain, and body(/substrate)
  - NMOSFET & PMOSFET

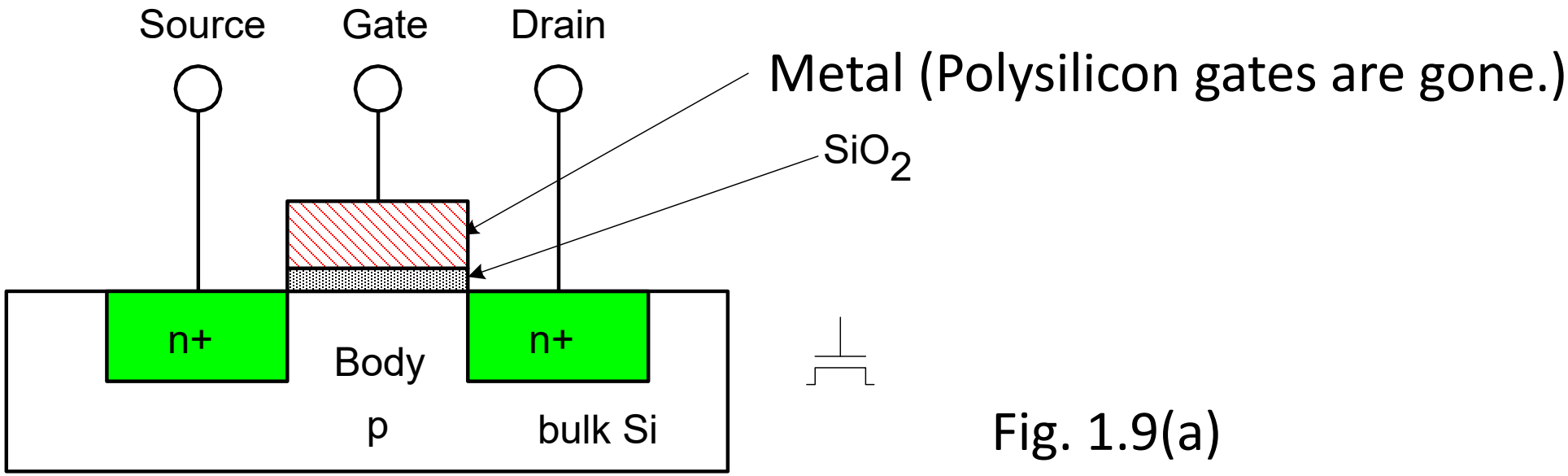
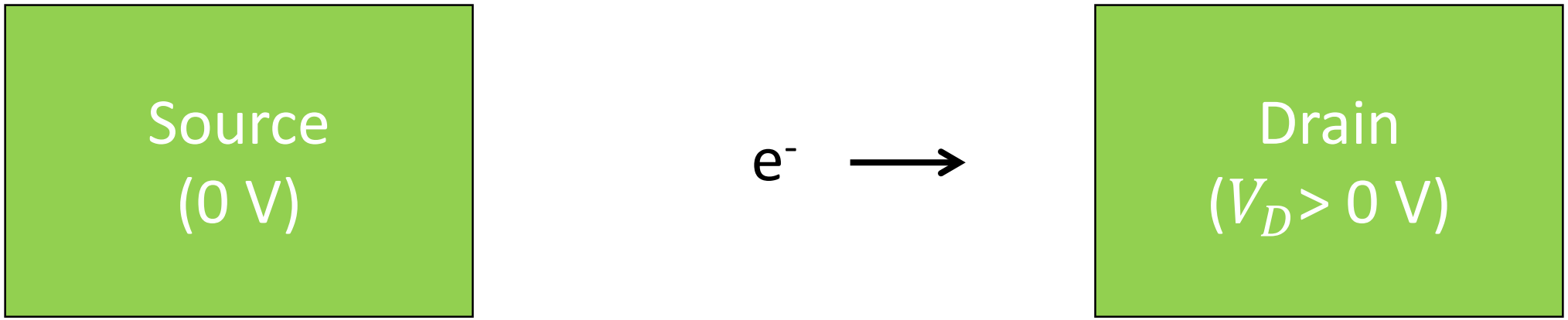


Fig. 1.9(a)

1.3. MOS transistors (2)

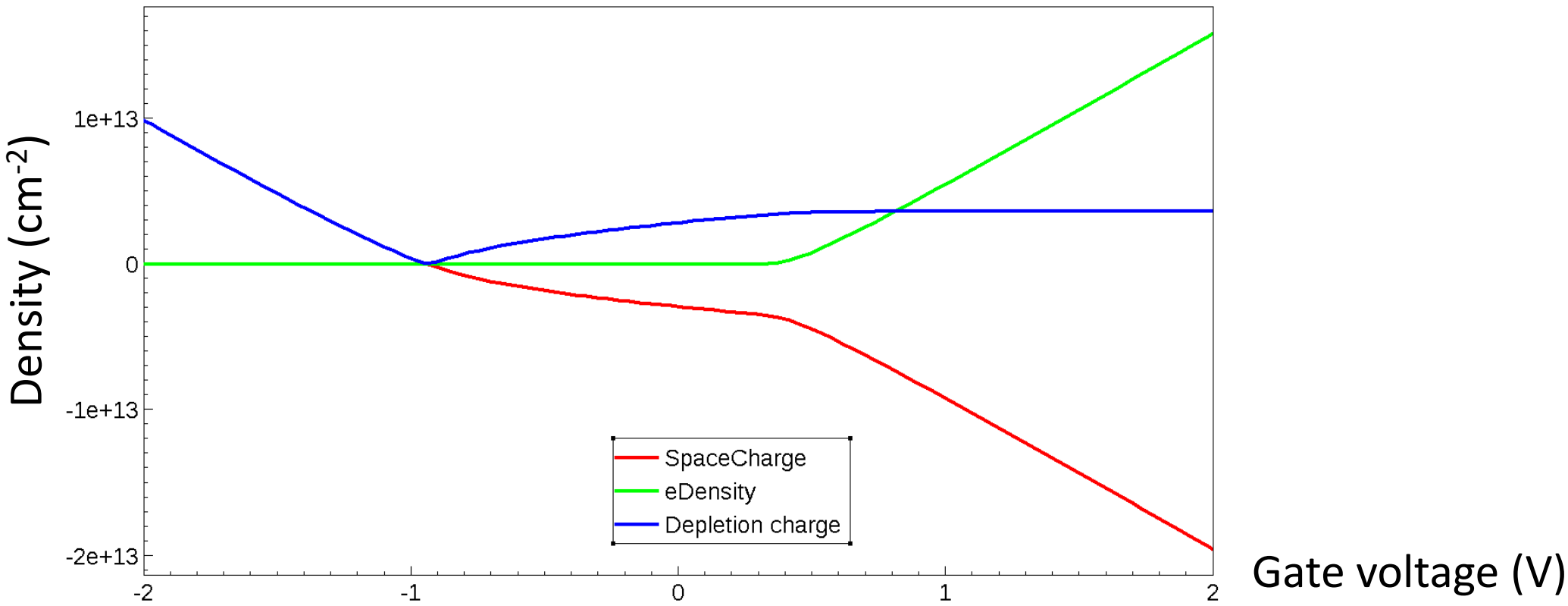
- Usually, $V_D > V_S$.
  - When we have an electron between the source/drain regions, it is drifted toward the drain. (Current conduction)



  - The key is to control the number of electrons.
  - (# of electrons) ≠ (# of negatively charged particles)

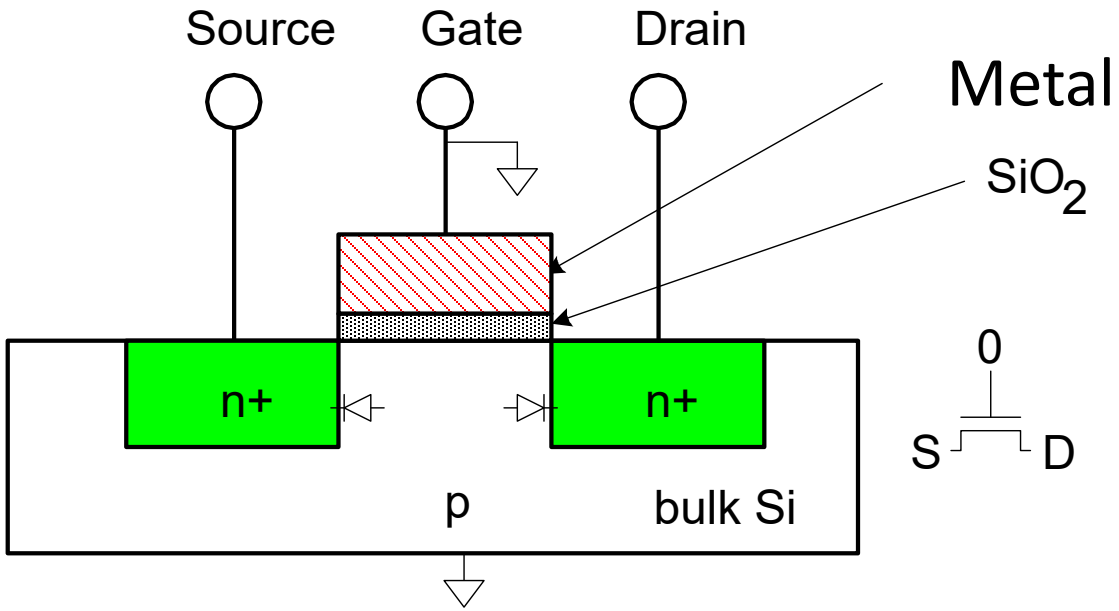
1.3. MOS transistors (3)

- MOS capacitor
  - It is a “nonlinear” capacitor.



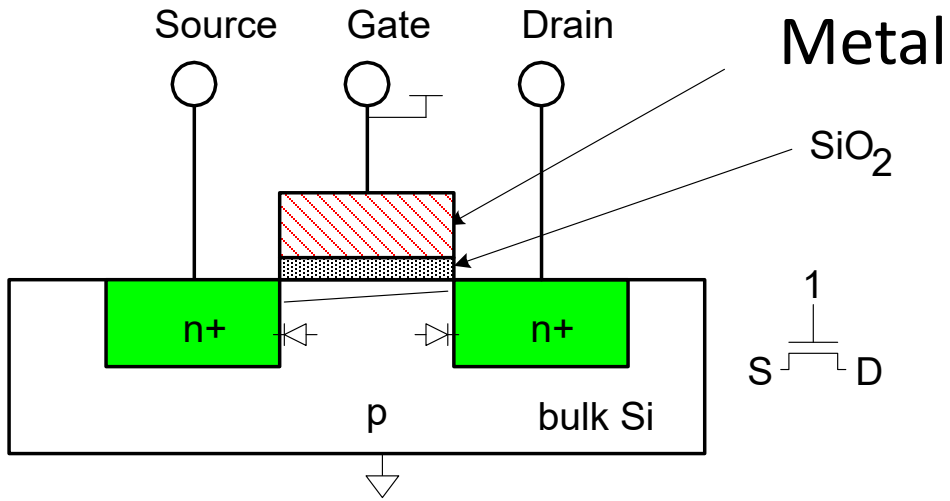
1.3. MOS transistors (4)

- Body is tied to ground (GND).
- When $V_{GS} \equiv V_G - V_S$ is low, (BTW, “low” means what?)
  - No current flows.
  - The transistor is said to be OFF.



1.3. MOS transistors (5)

- When $V_{GS} \equiv V_G - V_S$ is high, (Again, “high” means what?)
  - Current can flow from the source thorugh the channel to the drain.
  - The transistor is said to be ON.



1.3. MOS transistors (6)

- PMOS
  - Similar, but doping and voltages are reversed.
  - Body is tied to V_{DD}.
  - V_{GS} is negative.

Metal (Polysilicon gates are gone.)

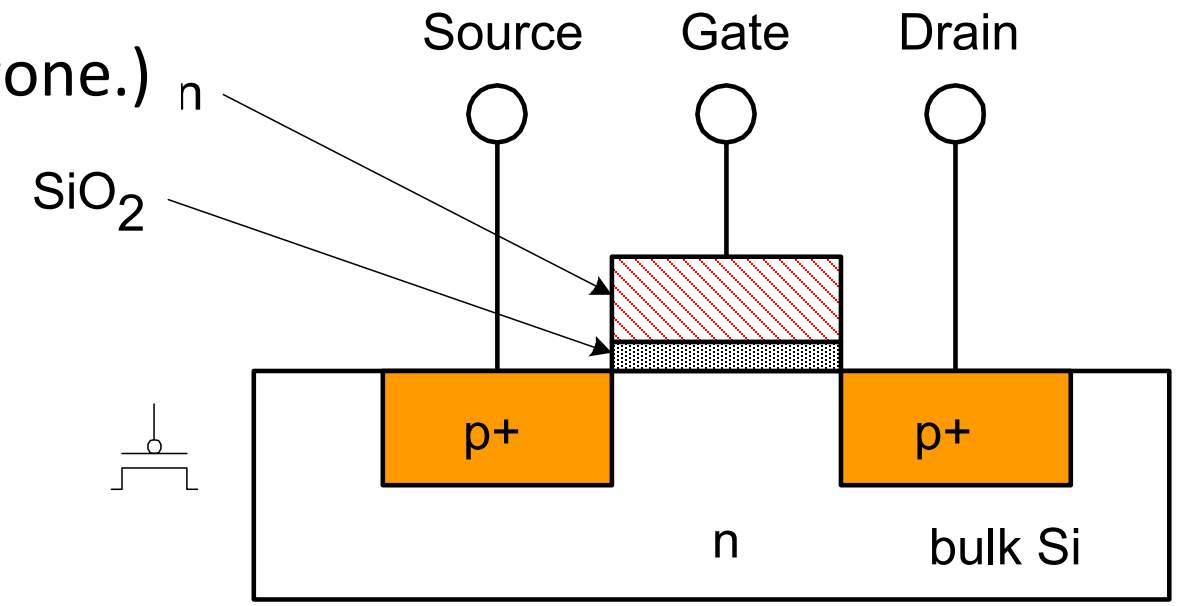
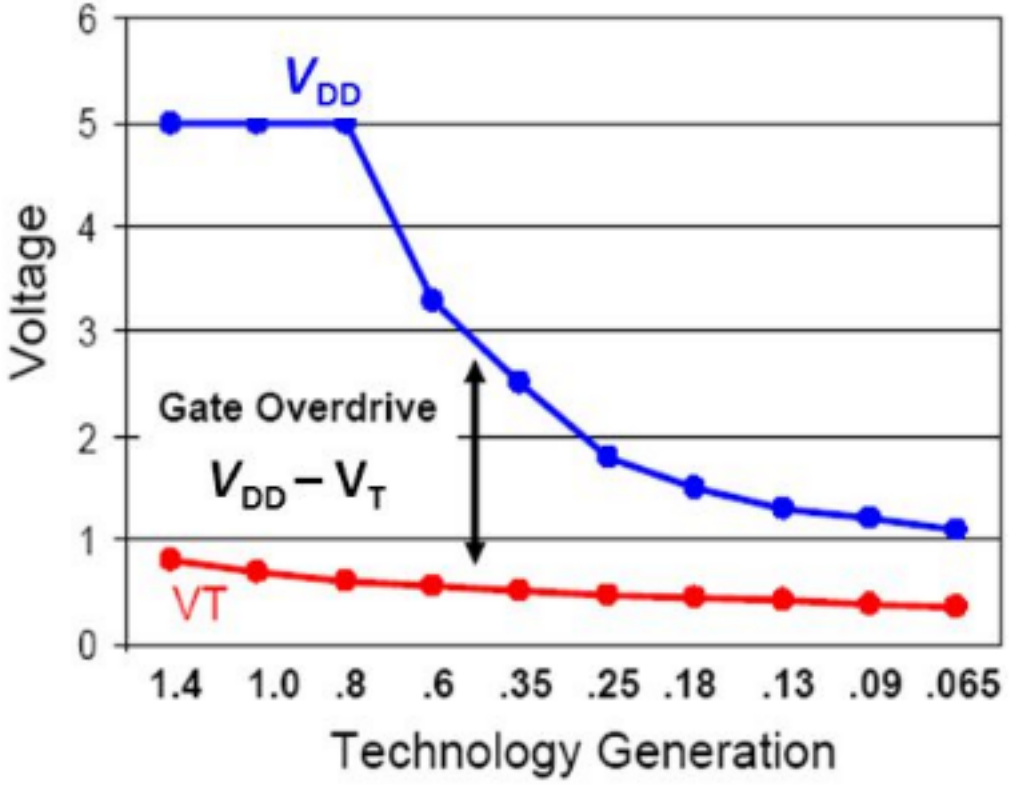


Fig. 1.9(b)

1.3. MOS transistors (7)

- Power supply voltage
  - In 1980's, V_{DD} was 5 V.
- IEDM(or VLSI) papers
  - 130nm: 2000
  - 90nm: 2003
  - 65nm: 2004
  - 45nm: 2007
  - 32nm: 2008
  - 22nm: 2012
  - 14nm (or 16nm): 2014



Source: P. Packan (Intel), 2007 IEDM Short Course

1.3. MOS transistors (8)

- Transistors as switches
  - V_G controls path from source to drain.

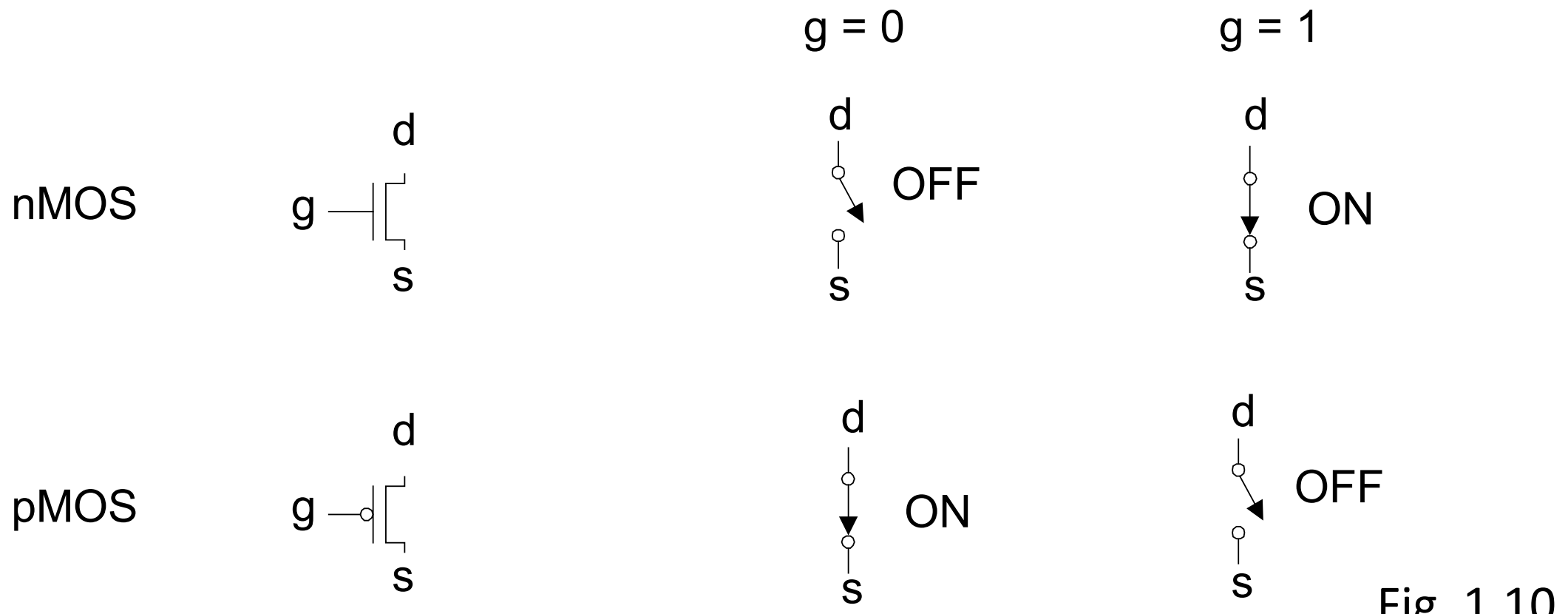


Fig. 1.10

Thank you!