Digital Integrated Circuit
Lecture 22 Combinational Circuit Design

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Review of Previous Lecture

Lecture 21

- SPICE MOSFET modes
  - Level 1
  - Level 3
  - BSIM
  - Neural compact model

9.1 Introduction

9.1. Introduction (1)

- Combinational circuit
  - Its outputs depend only on the present inputs.
  - Its building blocks are logic gates.
- Sequential circuit (Ch. 10)
  - It has memory.
  - Its building blocks are registers and latches.

9.1. Introduction (2)

- Static CMOS gates
  - They use complementary NMOS and PMOS networks to drive 0 and 1 outputs, respectively.
  - It is robust, fast, energy-efficient, and easy to design.
- Other circuit families
  - Ratioed circuits
  - Dynamic circuits
  - Pass-transistor circuits

9.1. Introduction (3)

- What makes a circuit fast?

$$t_{pd} \propto \frac{C}{I}\Delta V$$

  - We need:
  - Low capacitance (C)
  - High current (I)
  - Small swing (ΔV)
- NMOS is preferred.
  - Static CMOS has a relatively large logical effort, due to the PMOS transistors.

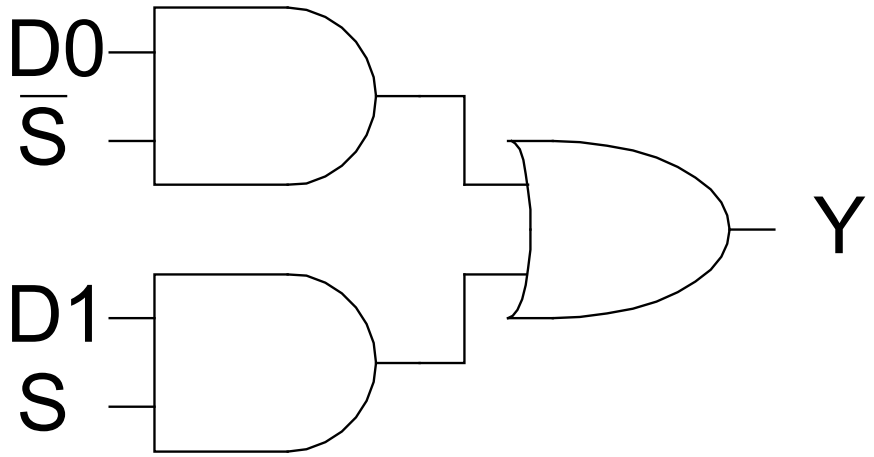
9.2 Circuit Families

9.2. Circuit families (1)

- Consider a multiplexer. ($D0$, $D1$, and S)
  - It can be expressed as

$$Y = D0 \cdot \bar{S} + D1 \cdot S$$

  - So, in general, we need a circuit to compute $F = AB + CD$.



9.2. Circuit families (2)

- Static CMOS
  - DeMorgan's law

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$
$$\overline{A + B} = \bar{A} \cdot \bar{B}$$

  - *Bubble pushing*

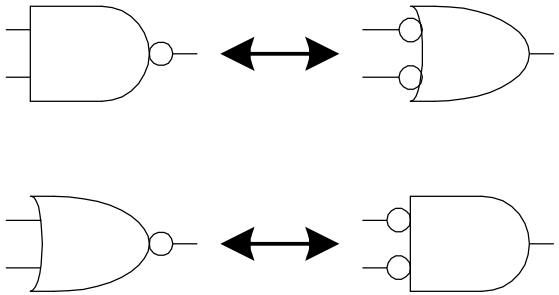
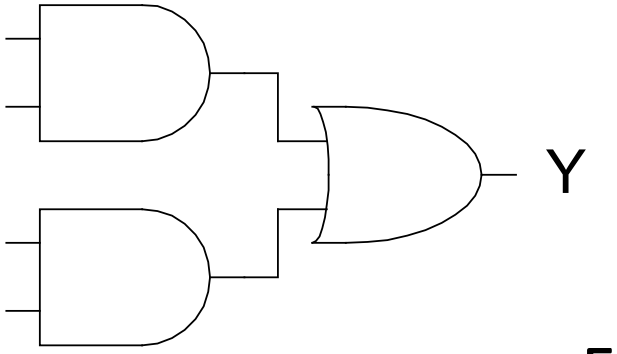


Fig. 9.1

- Design a circuit to compute $F = AB + CD$.



(a)

Fig. 9.2(a)

9.2. Circuit families (3)

- Static CMOS

$$F = AB + CD = \overline{\overline{AB} \cdot \overline{CD}}$$

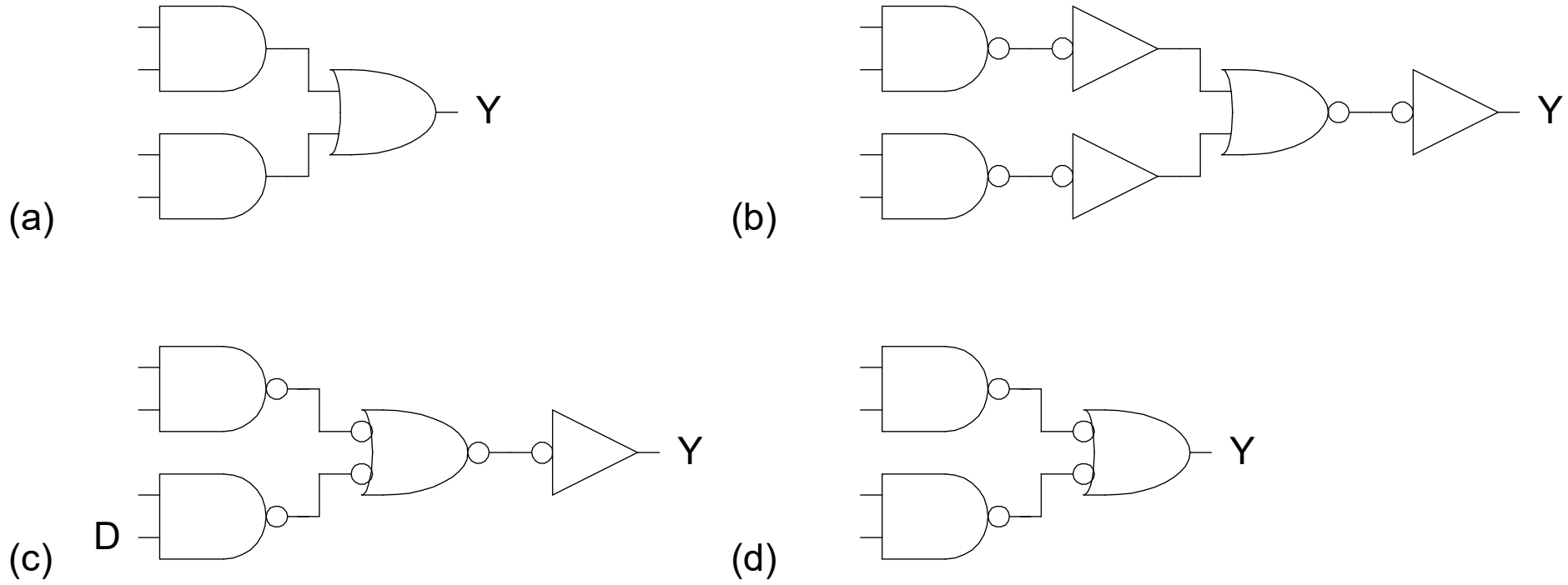


Fig. 9.2

9.2. Circuit families (4)

- Using a compound gate (Recall L2.)

$$F = AB + CD = \overline{\overline{AB} \cdot \overline{CD}}$$

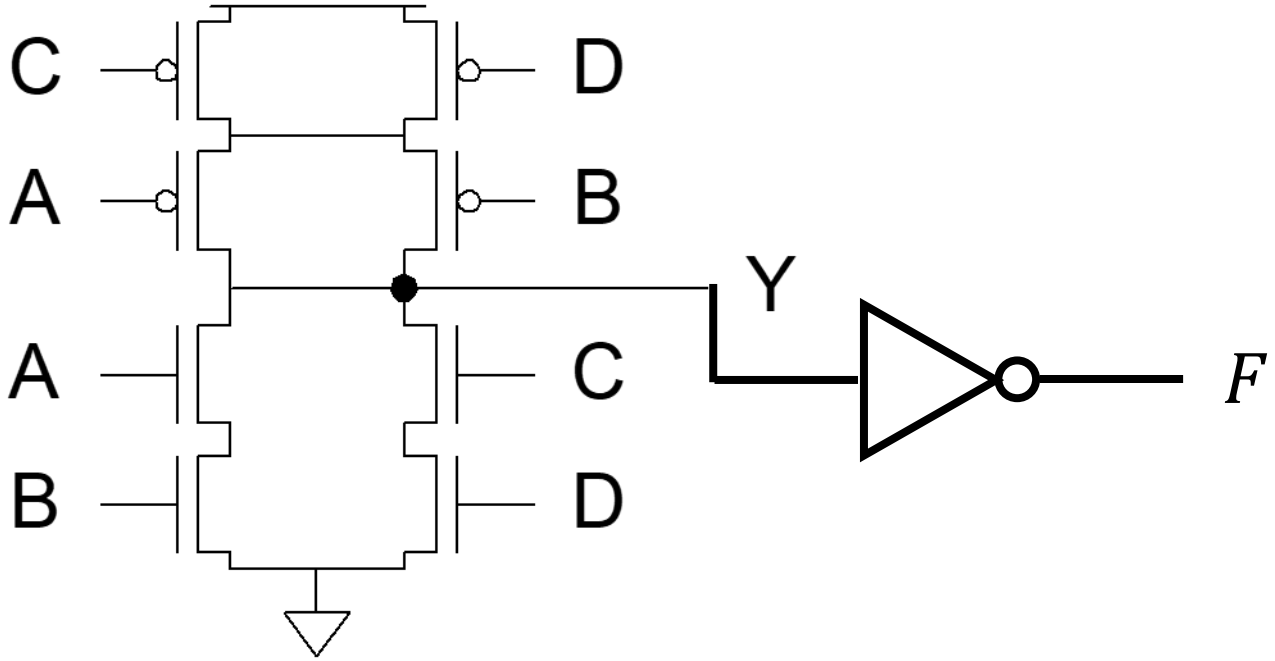


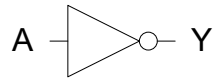
Fig. 1.18(e)

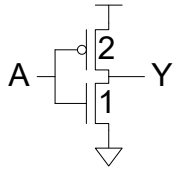
9.2. Circuit families (5)

- Logical effort of compound gates

unit inverter

$Y = \overline{A}$



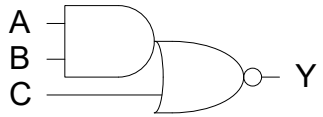


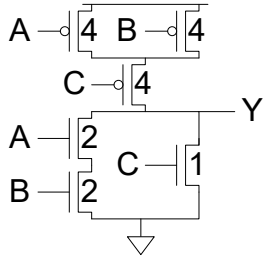
$g_A = 3/3$

$p = 3/3$

AOI21

$Y = \overline{A \cdot B + C}$





$g_A = 6/3$

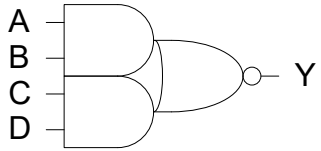
$g_B = 6/3$

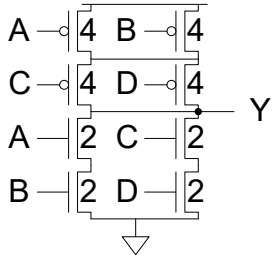
$g_C = 5/3$

$p = 7/3$

AOI22

$Y = \overline{A \cdot B + C \cdot D}$





$g_A = 6/3$

$g_B = 6/3$

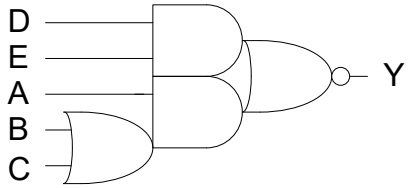
$g_C = 6/3$

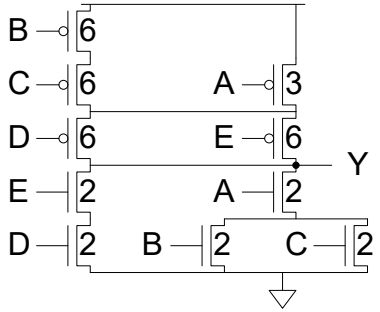
$g_D = 6/3$

$p = 12/3$

Complex AOI

$Y = \overline{A \cdot (B + C) + D \cdot E}$





$g_A = 5/3$

$g_B = 8/3$

$g_C = 8/3$

$g_D = 8/3$

$g_E = 8/3$

$p = 16/3$

9.2. Circuit families (6)

- Input order
  - Consider the falling output transition. (One input holds a stable 1.)
  - If input B rises later, the Elmore delay is 7RC.
  - If input A rises later, the Elmore delay is 6RC.
  - If one signal is known to arrive later than the others, connect the latest signal to the inner input.

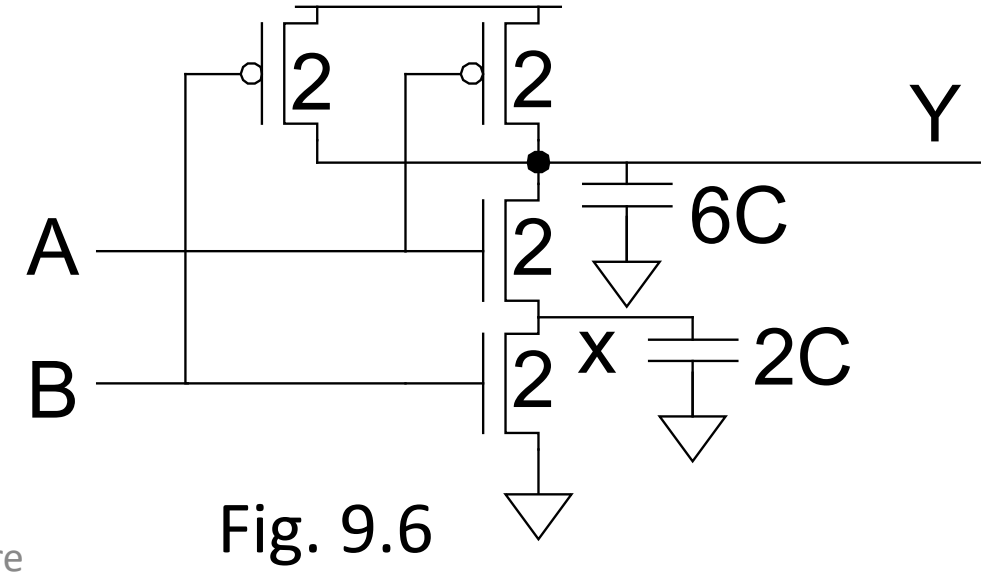


Fig. 9.6

9.2. Circuit families (7)

- Asymmetric gates
  - In this example, suppose that A is most critical.
  - The circuit is optimized for input-to-output delay at the expense of reset.

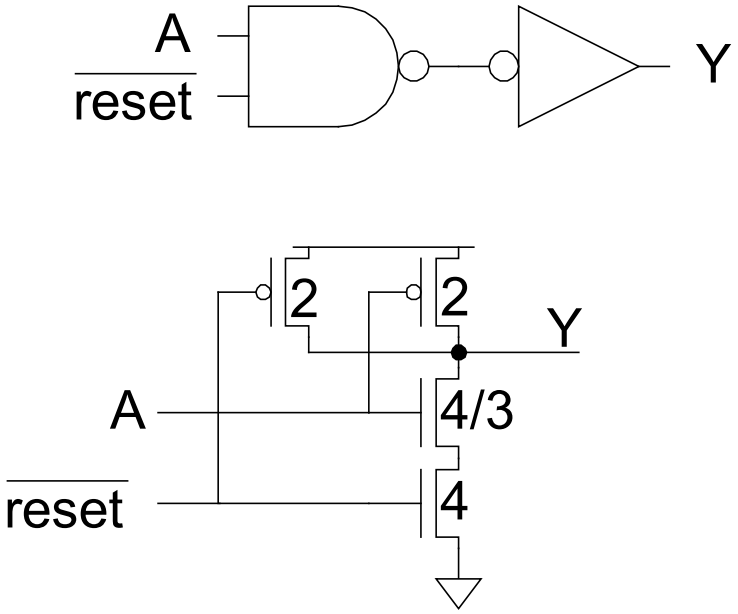


Fig. 9.7

9.2. Circuit families (8)

- Skewed gates
  - Skewed gates favor one edge over another.
  - In this example, suppose that the rising output of the inverter is most critical.
  - Then, we may downsize the noncritical NMOS transistor.
  - Improvement of the critical transition at the expense of noncritical one

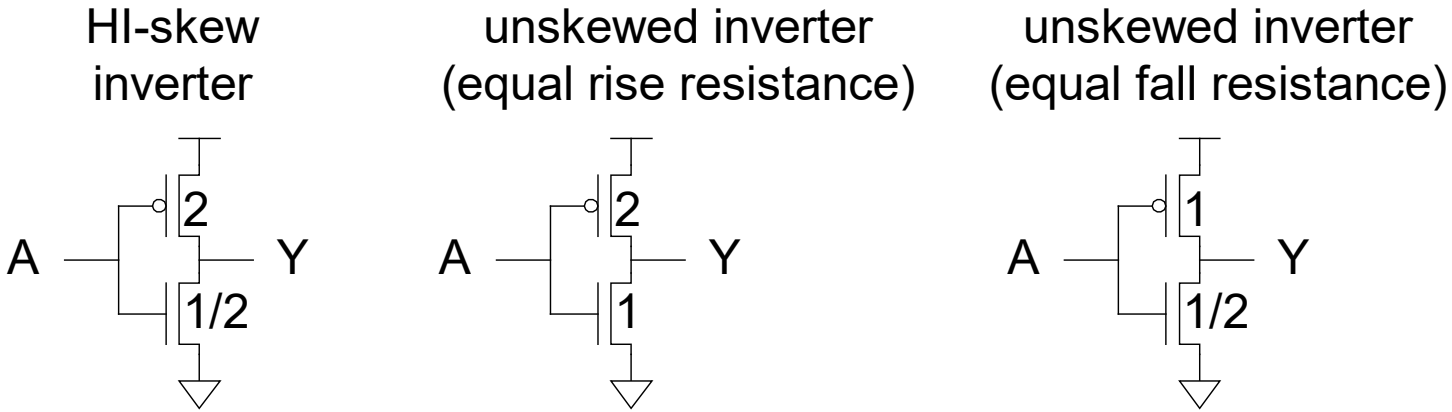


Fig. 9.9

9.2. Circuit families (9)

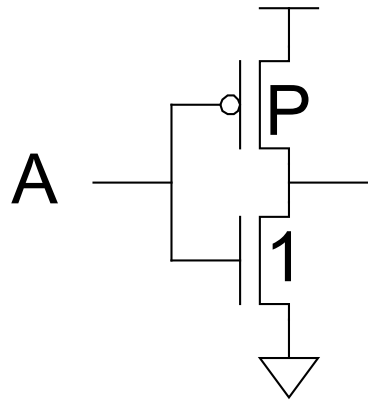
- Best P/N ratio?
  - Assume that the PMOS has μ times higher resistance.
  - Then,

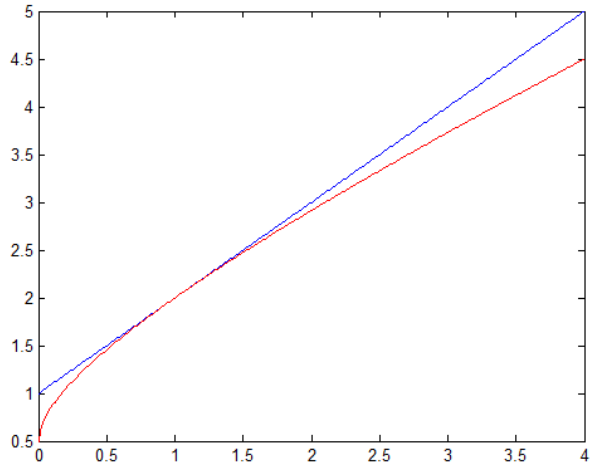
$$t_{pdf} = (P+1)$$

$$t_{pdr} = (P+1)\frac{\mu}{P}$$

$$t_{pd} = \frac{1}{2}(P+1)\left(1+\frac{\mu}{P}\right)$$

  - When we have $P = \mu$, t_{pd} becomes $(\mu+1)$.
  - When we have $P = \sqrt{\mu}$, t_{pd} becomes $\frac{1}{2}\left(\sqrt{\mu}+1\right)^2$.





- Area, power, and reliability should be considered.

Thank you!