Digital Integrated Circuit
Lecture 5 MOS Transistor Theory

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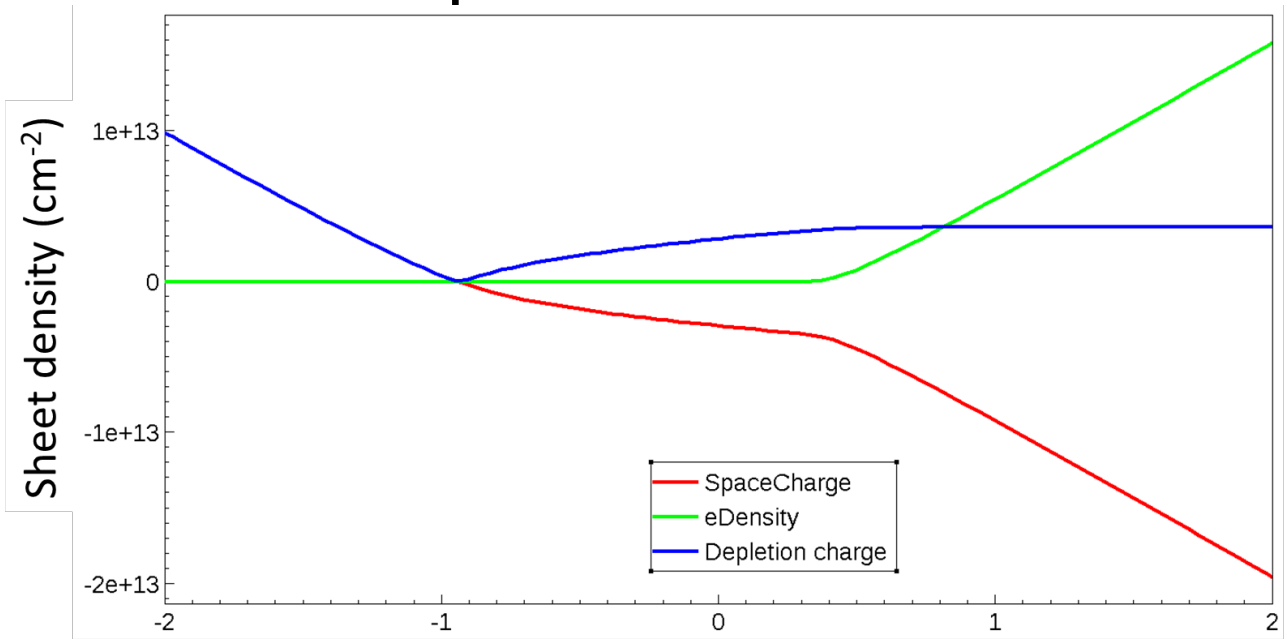
Review of Previous Lecture

Lecture 4

- CMOS fabrication
- CMOS layout
  - Standard cell design
  - NAND3
- MOS capacitor



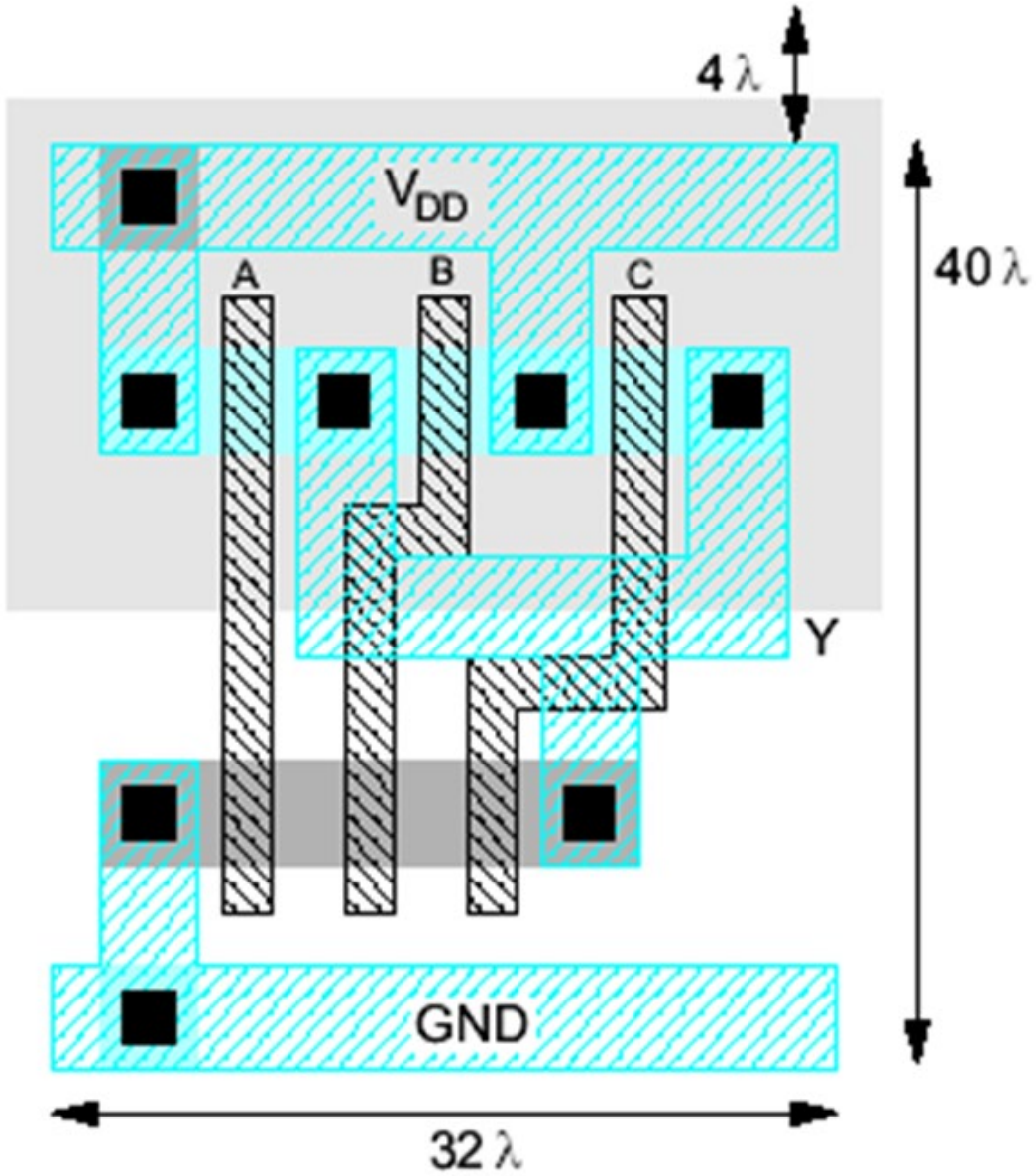
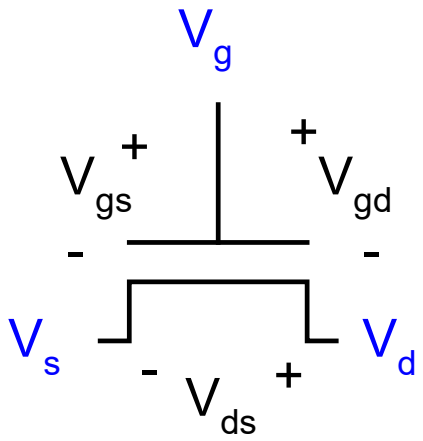


Fig. 1.42

2.1 Introduction

2.1. Introduction (3)

- MOSFET is a four-terminal device.
  - Source and drain are symmetric.



  - By convention, the source is biased with a lower voltage. Therefore, $V_{ds} \geq 0$.
  - The body of an NMOSFET is grounded.
  - Operation regions: Subthreshold, linear, and saturation

2.1. Introduction (4)

- When the gate-to-source voltage is lower than the threshold voltage (V_t),
  - No mobile carrier. Therefore,

$$I_d \approx 0$$

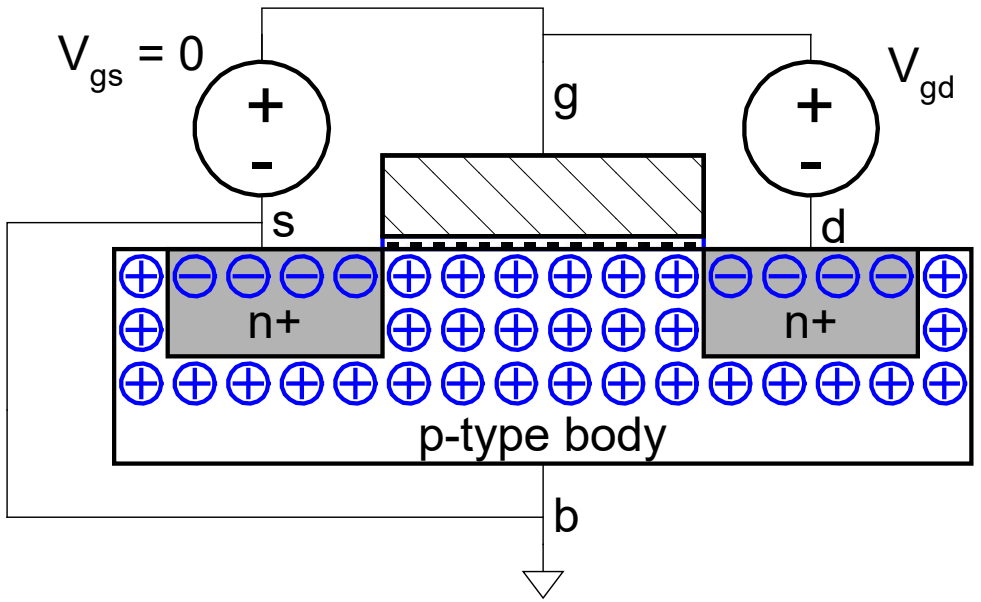
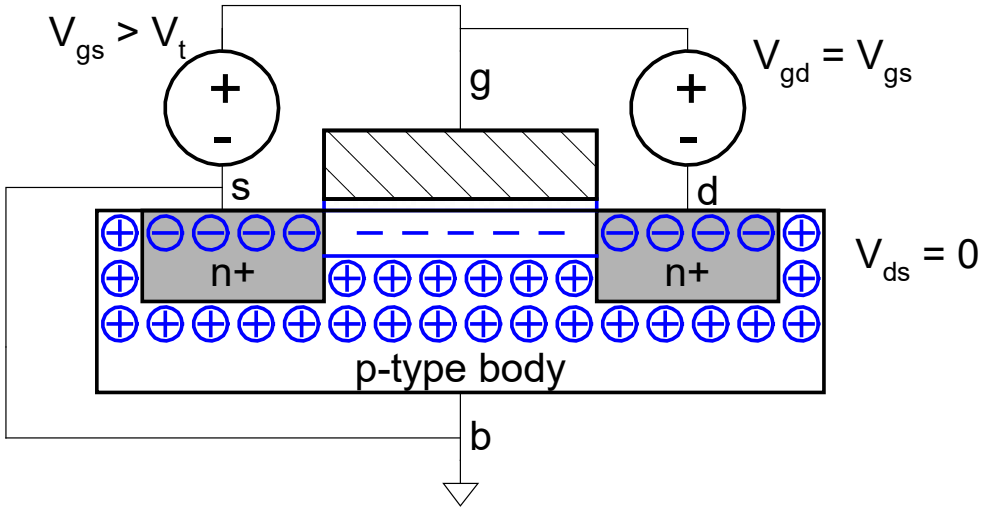


Fig. 2.3(a)

2.1. Introduction (5)

- Linear mode
  - When $V_{gs} > V_t$,
    we have an inversion channel.



  - By applying a positive V_{ds},
    we have $I_d > 0$.

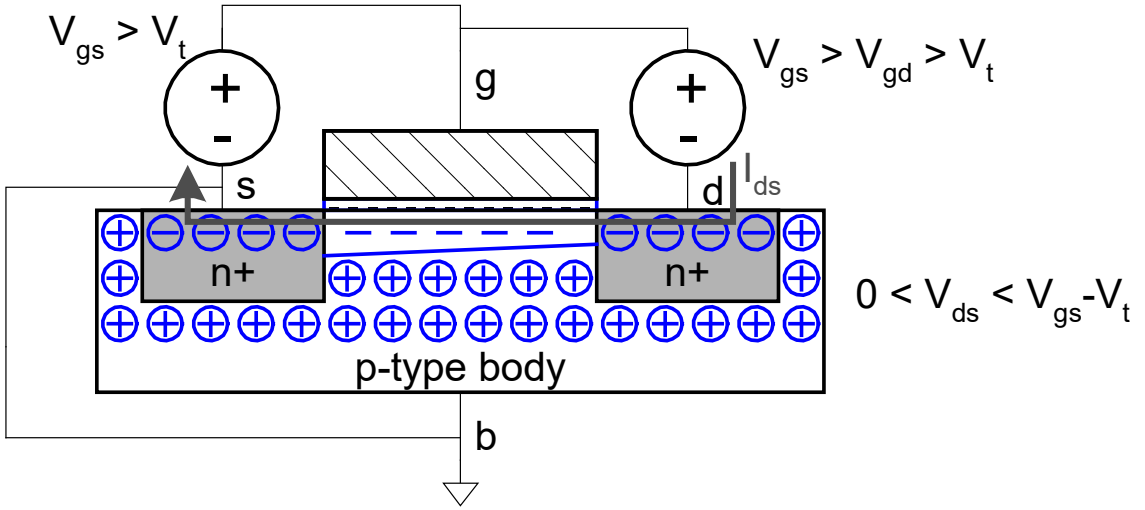


Fig. 2.3(b) & (c)

2.1. Introduction (6)

- Saturation
  - When $V_{ds} > V_{gs} - V_t$, the drain current is controlled only by the gate voltage and ceases to be influenced by the drain.

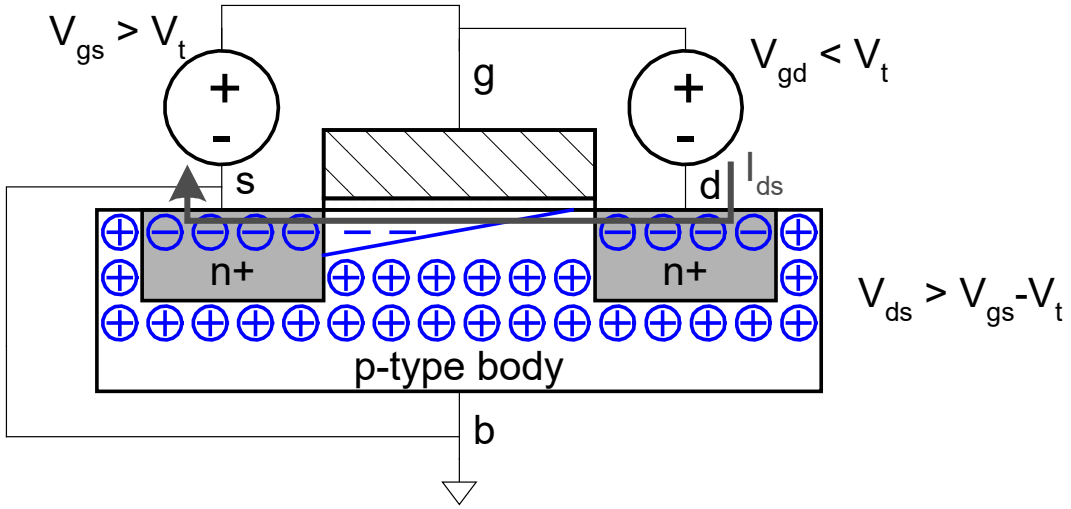


Fig. 2.3(d)

2.2 Long-channel IV

2.2. Long-channel IV (1)

- Current through the channel depends on
  - How much “electron” charge is in the channel?
  - How fast is the charge moving?
- Charge

$$Q_{channel} = C_g\left(V_{gc} - V_t\right)$$

  - Note) $Q_{channel}$ for electrons. (It should be negative, but in the above equation, it is understood.)

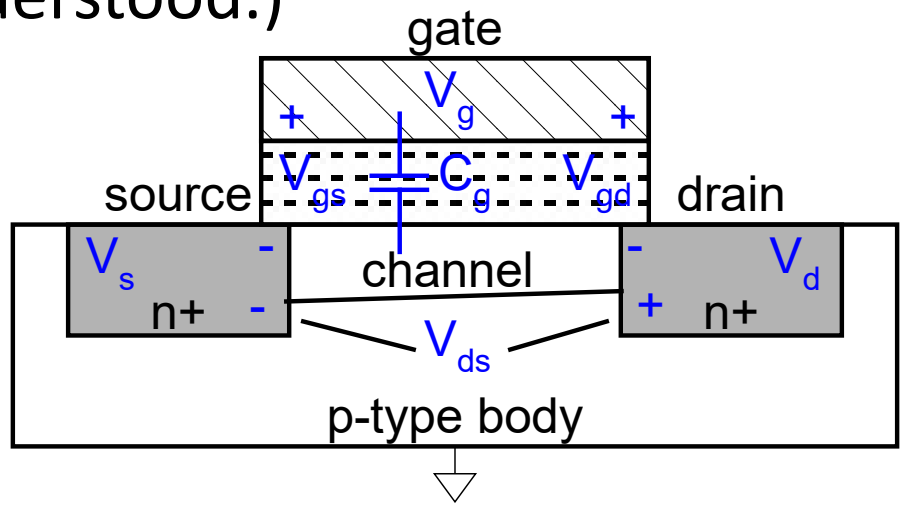


Fig. 2.5

2.2. Long-channel IV (2)

- Capacitance

$$C_g = C_{OX} W L$$

  - The "oxide capacitance," C_{OX}, is given as

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$$

Calculate C_{OX} , when the effective oxide thickness is 1 nm.

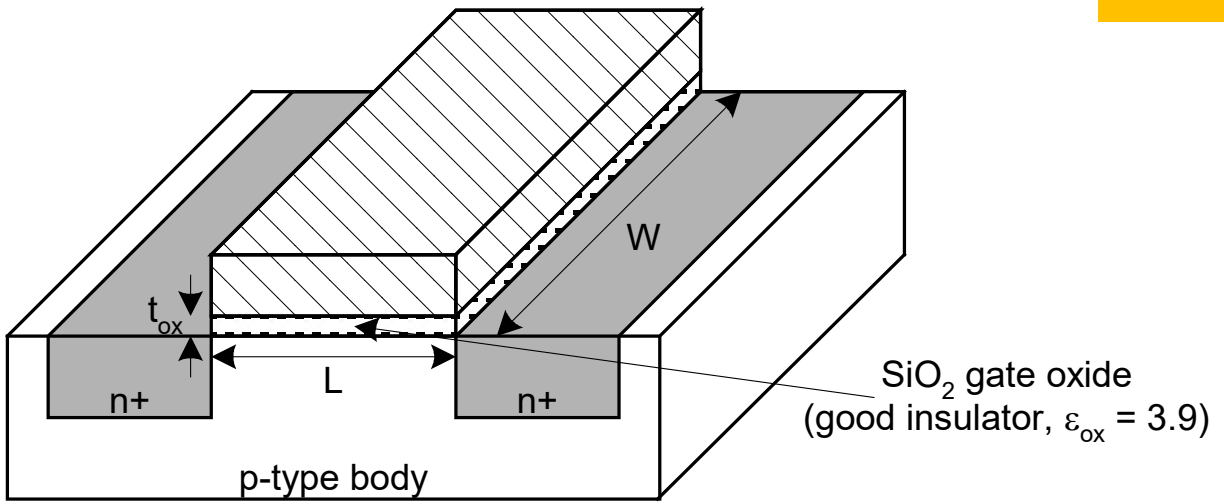


Fig. 2.6

2.2. Long-channel IV (3)

- IV characteristics
  - After some manipulation, we have

Subthreshold

$$I_d = 0$$

Linear

$$I_d = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$

Saturation

$$I_d = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

  - Here,

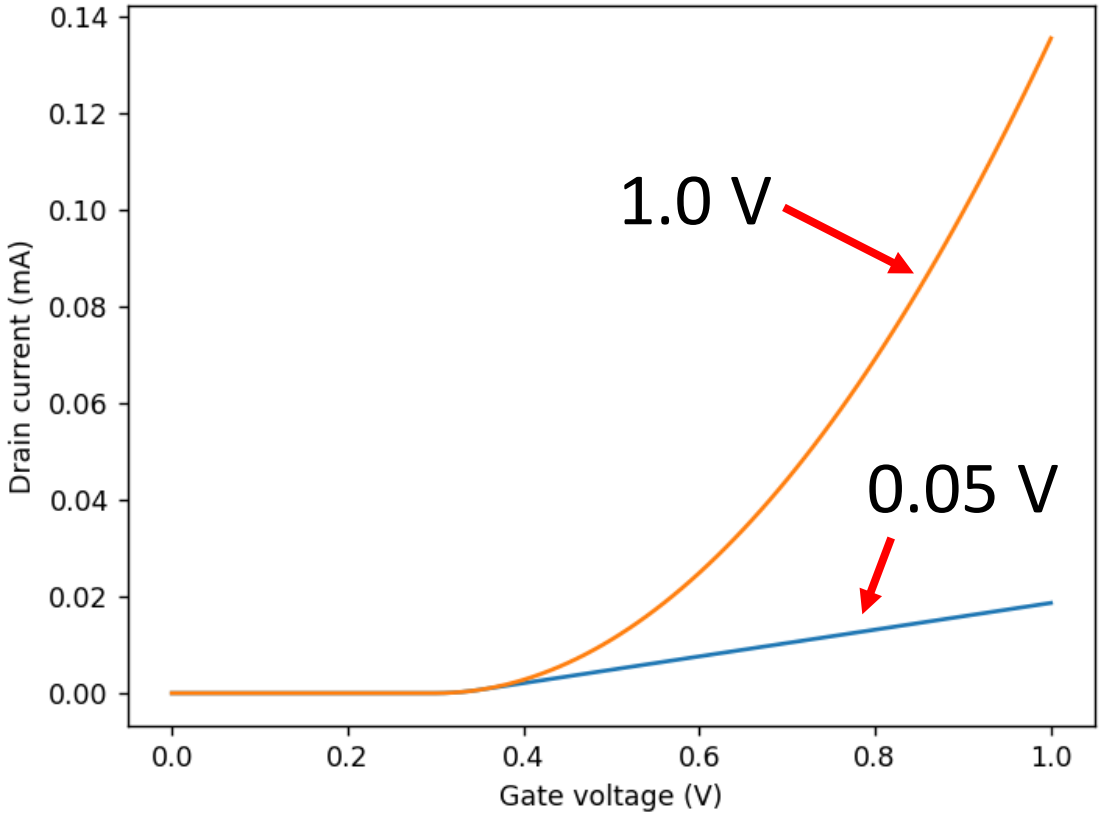
$$\beta = \mu_n C_{OX}\frac{W}{L}$$

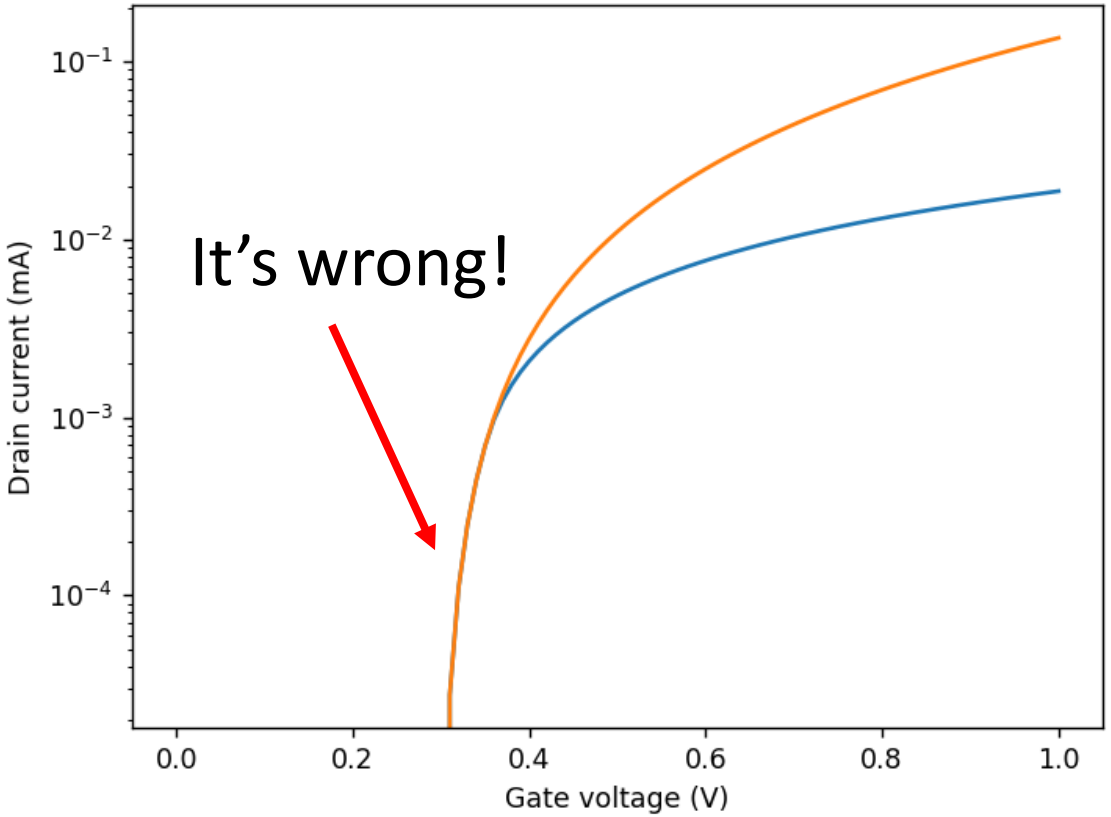
Calculate I_d at $V_{gs} = V_{ds}$ = 1.0 V, when W/L = 2, t_{ox} = 1 nm, μ_n = 80 cm^2/V sec, and V_t is 0.3 V.

2.2. Long-channel IV (4)

V_{DD} = 1.0 V, W/L = 2, t_{ox} = 1 nm, μ_n = 80 cm^2/V sec, and V_t is 0.3 V.

- IV characteristics of an NMOSFET
  - Input characteristics

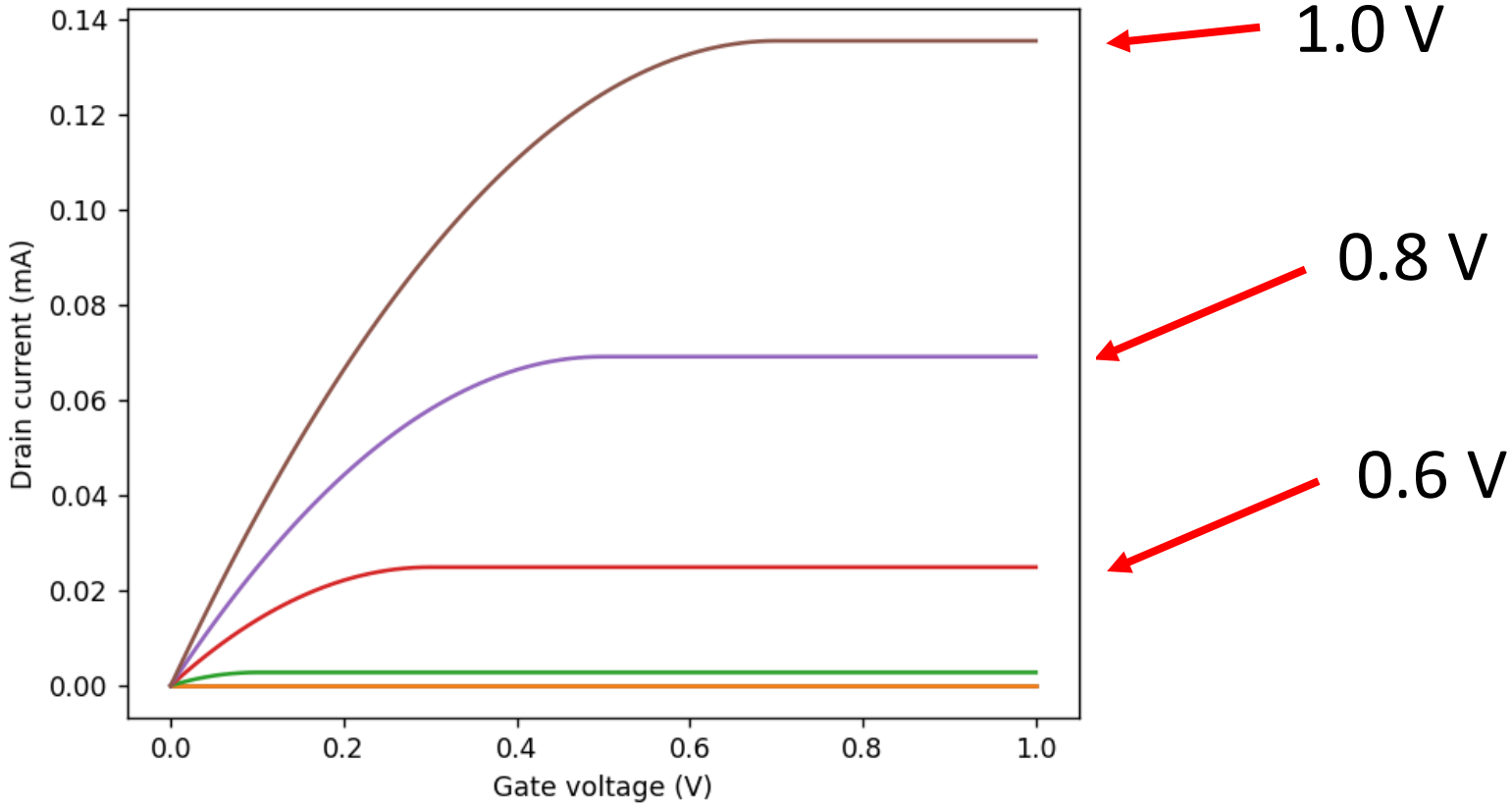




2.2. Long-channel IV (5)

V_{DD} = 1.0 V, W/L = 2, t_{ox} = 1 nm, μ_n = 80 cm^2/V sec, and V_t is 0.3 V.

- IV characteristics of an NMOSFET
  - Output characteristics



2.3. Capacitance (1)

- Any two conductors separated by an insulator have capacitance.
- Gate-to-channel capacitance is very important.
  - It creates channel charge which is necessary for operation.
- Source and drain have capacitance to body across the reverse-biased diodes.
  - It is called the diffusion capacitance, because it is associated with source/drain diffusion regions.

2.3. Capacitance (2)

- Gate capacitance
  - It is given as $C_g = C_{OX}WL$.
- Overlap capacitance, C_{gs} and C_{gd}

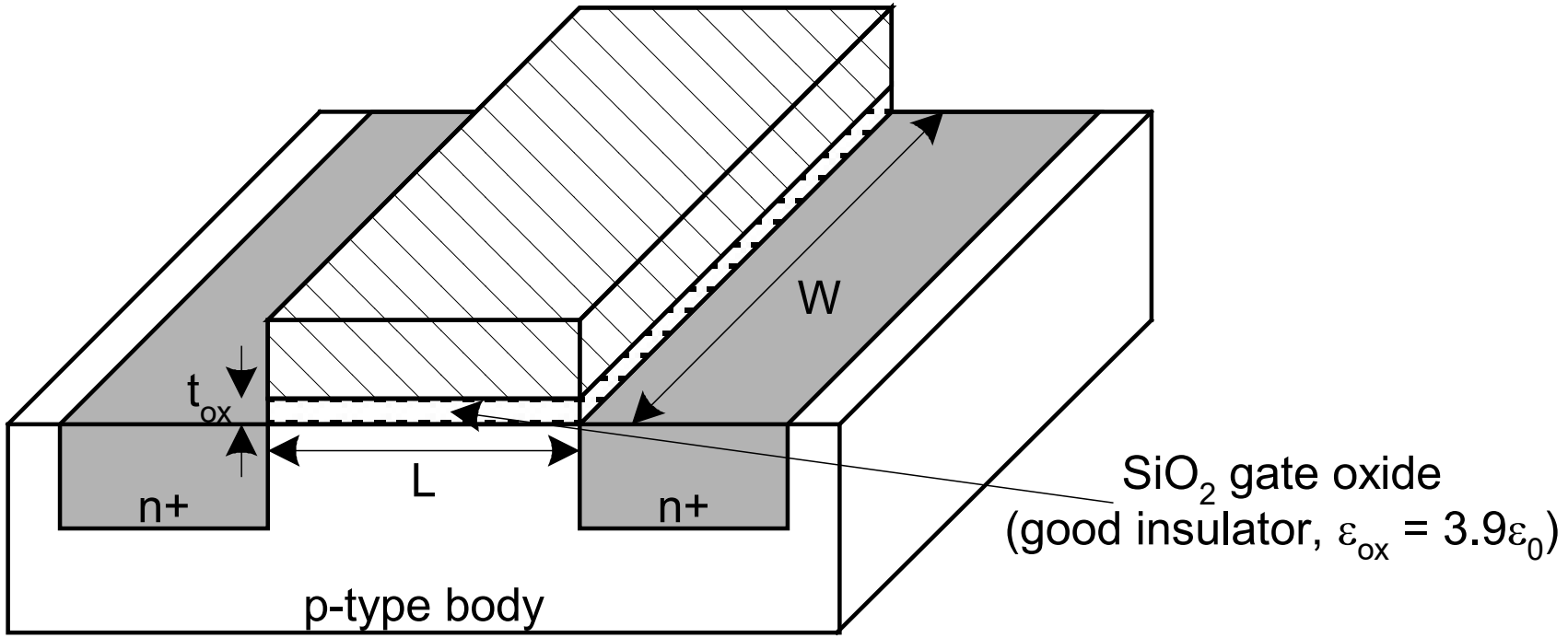


Fig. 2.6

2.3. Capacitance (3)

- Diffusion capacitance, C_{sb} and C_{sb}
  - Parasitic capacitance
  - Due to the PN junction between a diffusion region and the substrate

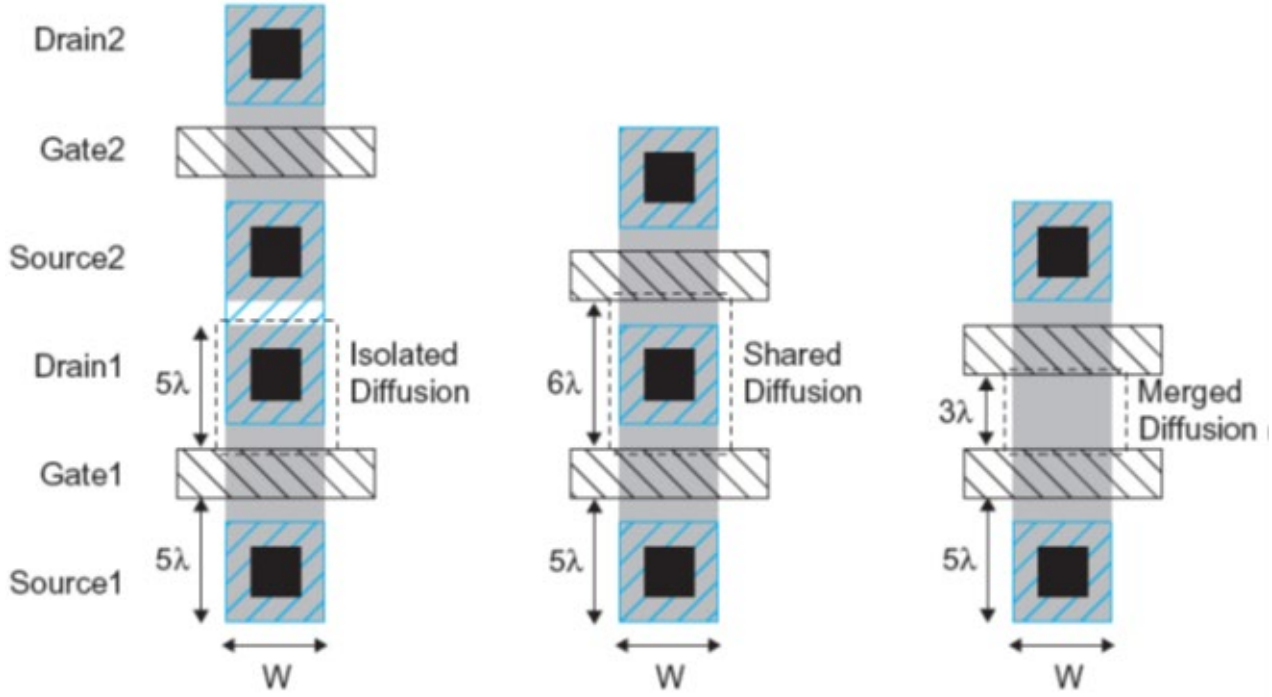


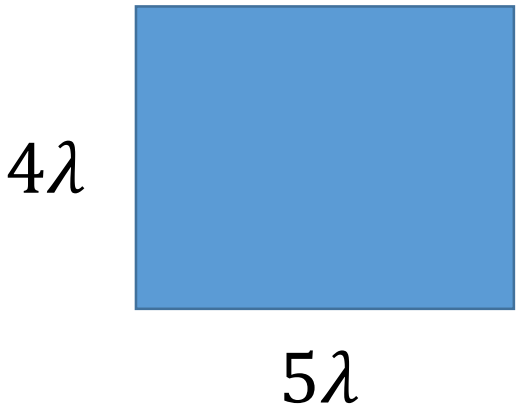
Fig. 2.8

2.3. Capacitance (4)

- Total source parasitic capacitance is

$$C_{sb} = AS \times C_{jbs} + PS \times C_{jbssw}$$

- Example 2.2) (Assume that is 25 nm.)
  - Area is $4\lambda \times 5\lambda = 20\lambda^2 = 0.0125\ \mu\text{m}^2$.
  - Perimeter is $2(4\lambda + 5\lambda) = 18\lambda = 0.45\ \mu\text{m}$.
  - Since $C_{jbd} = 1.2fF/\mu\text{m}^2$, the capacitance is 0.015 fF.
  - Assume that $C_{jbdsw} = 0.1fF/\mu\text{m}$.
  - Contribution from sidewalls is 0.071 fF.
  - The overall diffusion capacitance is 0.086 fF.



Homework#1

- Due: AM08:00, September 14
- Submit a single PDF file for your solutions.
- Problem#1
  - Draw the input charactersitics of an NMOSFET. Its threshold voltage is 0.4 V and W/L = 2. The oxide thickness is 2 nm. The electron mobility is 80 cm2/V sec. The channel length is 180 nm. V_{DD} = 1.8 V. Consider two drain voltages, 0.05 V and V_{DD}.
- Problem#2
  - For the same device, draw the output charactersitics.

Thank you!