

Digital Integrated Circuit

Lecture 13 Delay

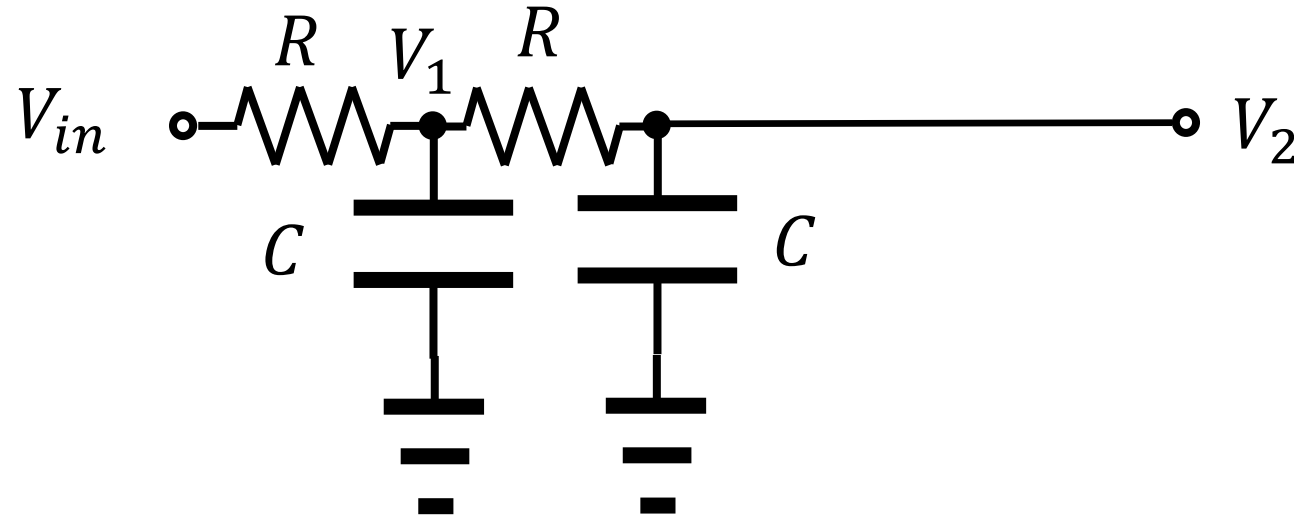
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Review of Previous Lecture

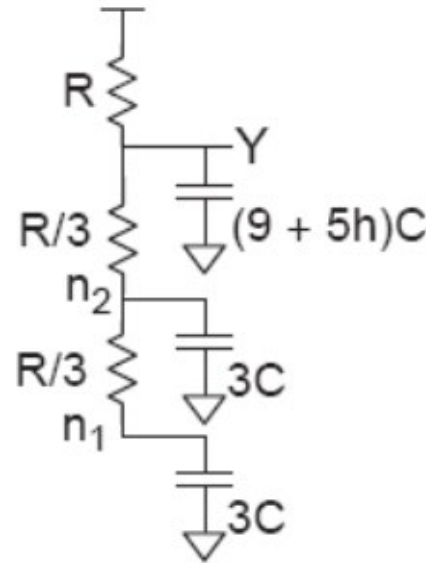
Lecture 12

- Elmore delay
 - When V_2 is the output voltage, $\tau = 3RC$.
 - When V_1 is the output voltage, $\tau = 2RC$.



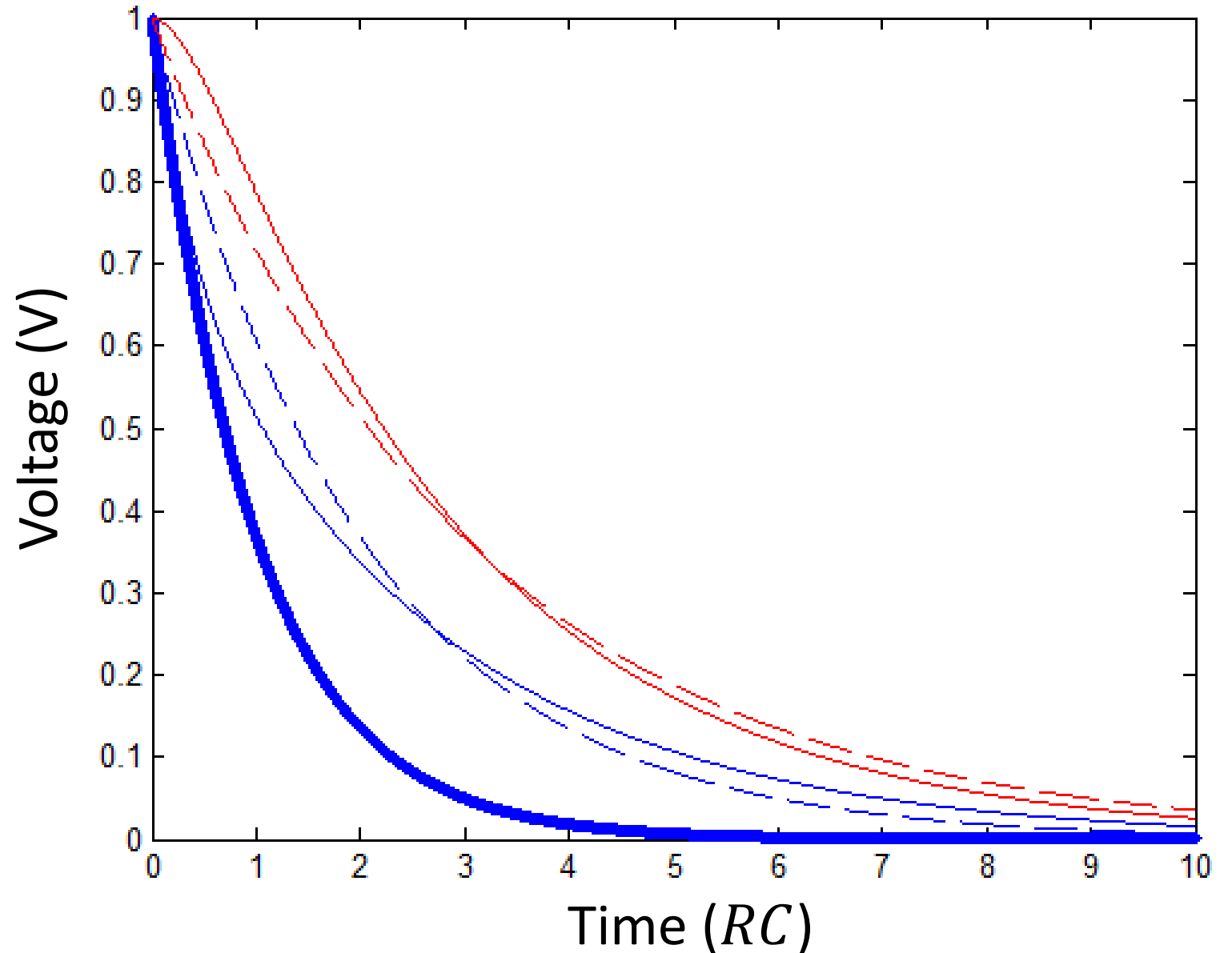
Lecture 12

- Rising propagation delay
 - In the worst case, $\tau = (15 + 5h)RC$.



Lecture 12

- Homework#4
 - Solid (Solution)
 - Dash (Approx.)
 - Red (V_2)
 - Blue (V_1)
 - Blue dot (Wrong!)



4.3 RC Delay Model

4.3. RC delay model (11)

- Delay components
 - *Parastic delay*: Time for a gate to drive its own internal diffusion capacitance
 - *Effort delay*: It depends on the ratio of external load capacitance to input capacitance.
 - The normalized delay, $d = \frac{t_{pd}}{3RC}$, can be written as

$$d = \text{parastic delay} + \text{effort delay}$$

4.3. RC delay model (12)

- Layout dependence of capacitance
 - A good layout minimizes the diffusion area.

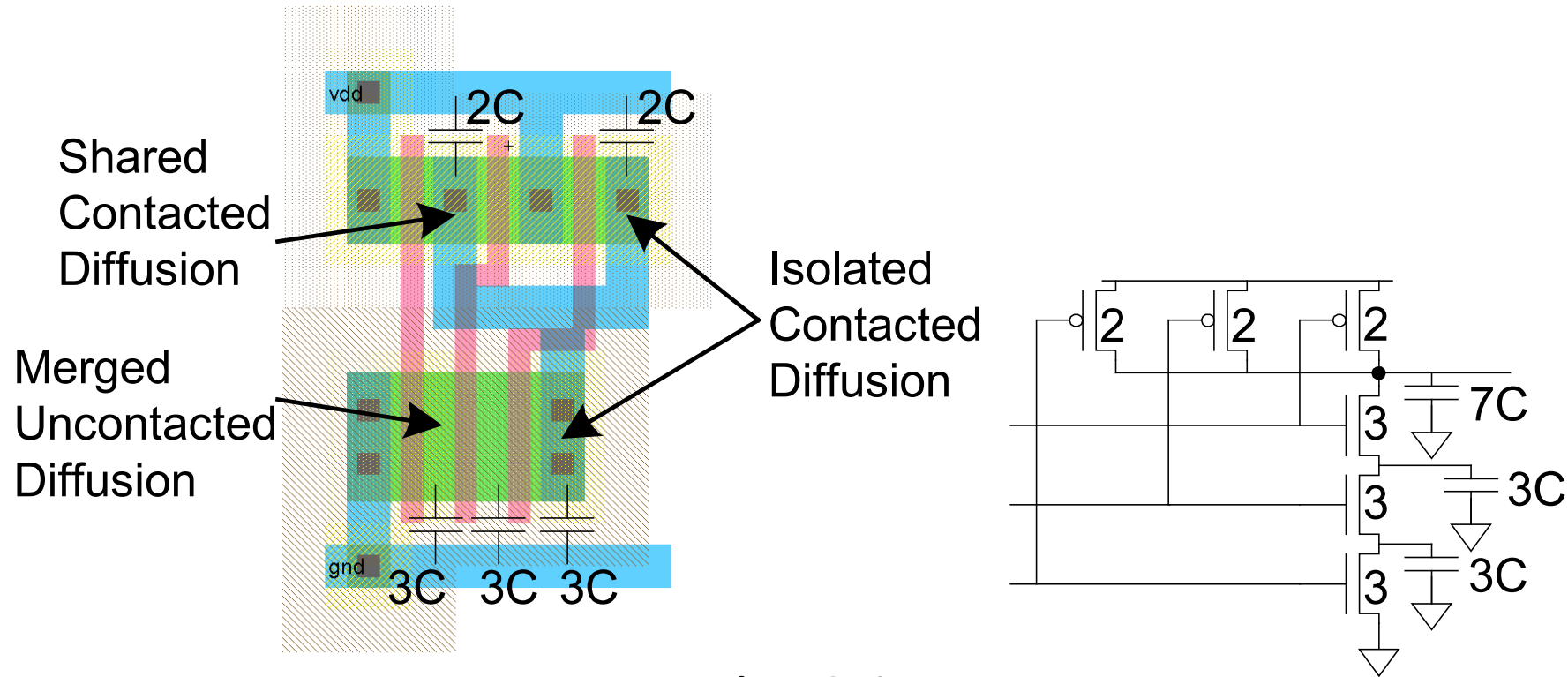


Fig. 4.17

4.4 Linear Delay Model

4.4. Linear delay model (1)

- Delay in a logic gate
 - Normalized delay

$$d = \frac{t_{pd}}{3RC}$$

- Delay has two components:

$$d = f + p = gh + p$$

- Effort delay:

$$f = gh$$

(g is the logical effort.)

4.4. Linear delay model (2)

- Delay in a logic gate

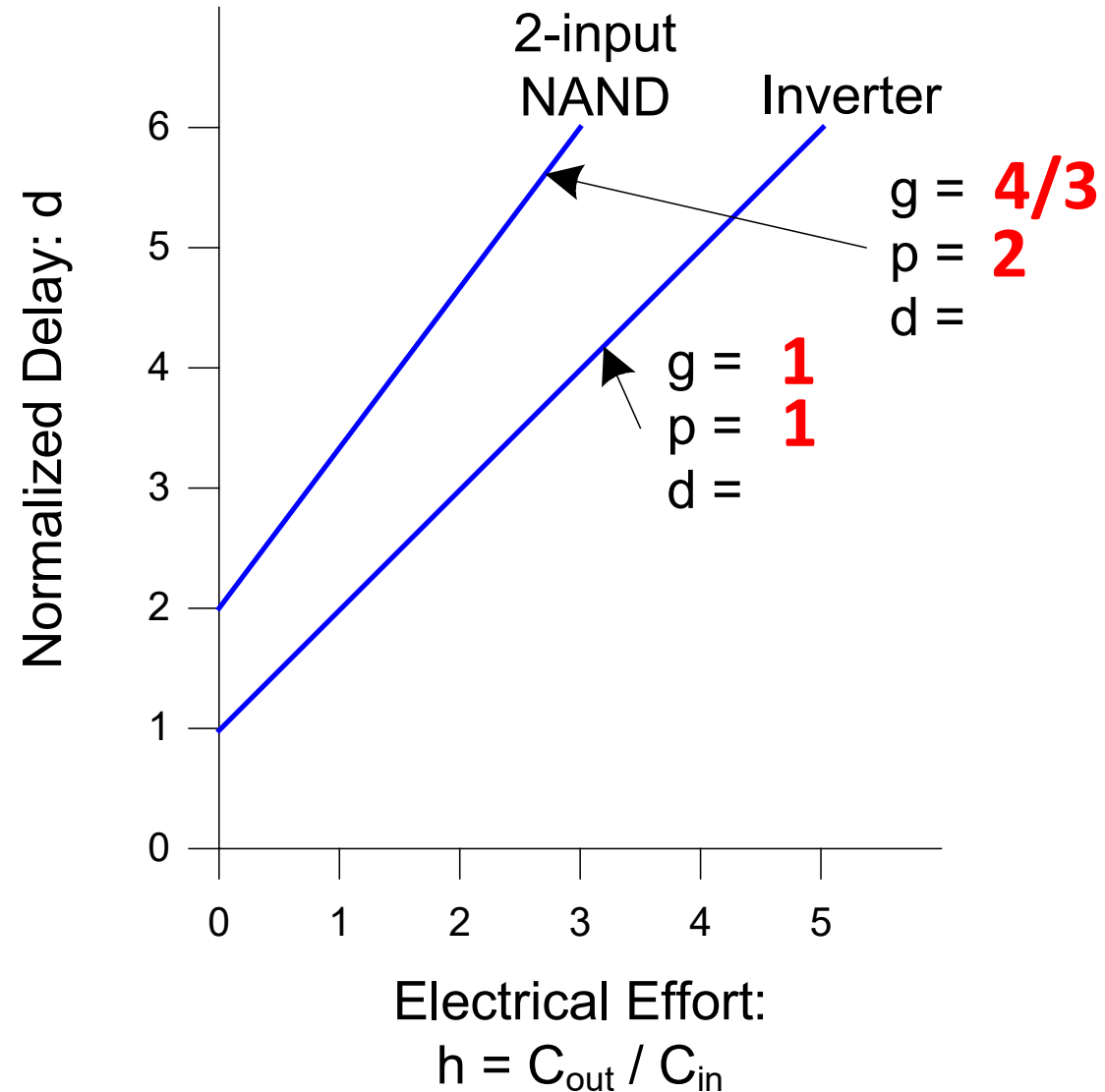
- Fanout (or electrical effort)

$$h = \frac{C_{out}}{C_{in}}$$

(Ratio of output to input capacitance)

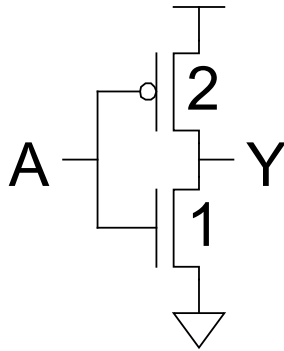
- Parasitic delay, p , represents delay of gate driving no load.

- p is set by internal parasitic capacitance.

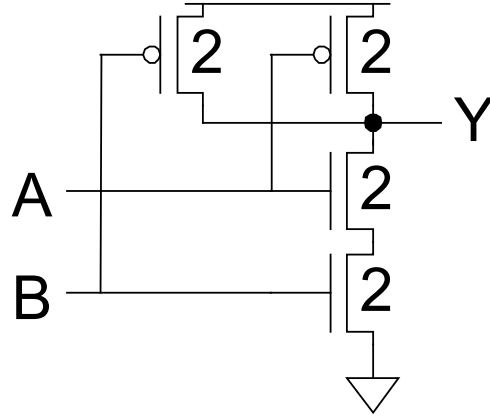


4.4. Linear delay model (3)

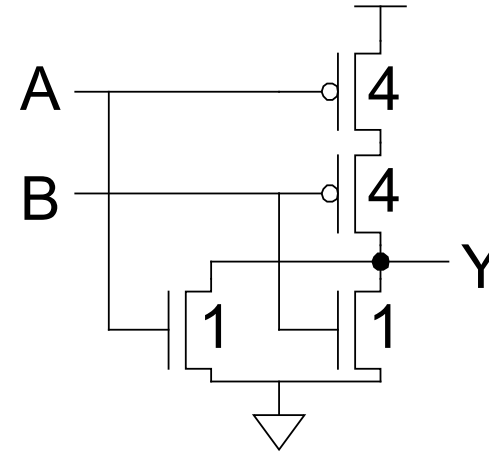
- Computing logical effort
 - *Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current.*



$$C_{in} = 3$$
$$g = 3/3$$



$$C_{in} = 4$$
$$g = 4/3$$



$$C_{in} = 5$$
$$g = 5/3$$

4.4. Linear delay model (4)

- Logical effort of common gates

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		$4/3$	$5/3$	$6/3$	$(n+2)/3$
NOR		$5/3$	$7/3$	$9/3$	$(2n+1)/3$
Tristate / mux	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

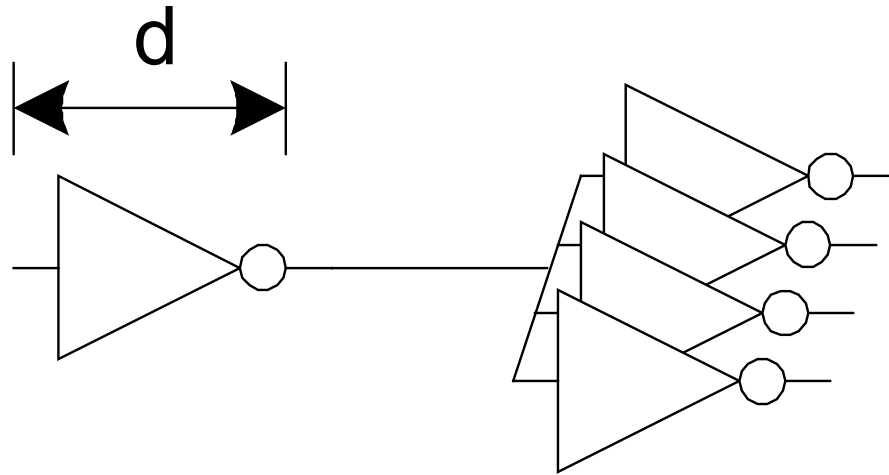
4.4. Linear delay model (5)

- Parasitic delay of common gates

Gate type	Number of inputs				
	1	2	3	4	n
Inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n
Tristate / mux	2	4	6	8	2n
XOR, XNOR		4	6	8	

4.4. Linear delay model (6)

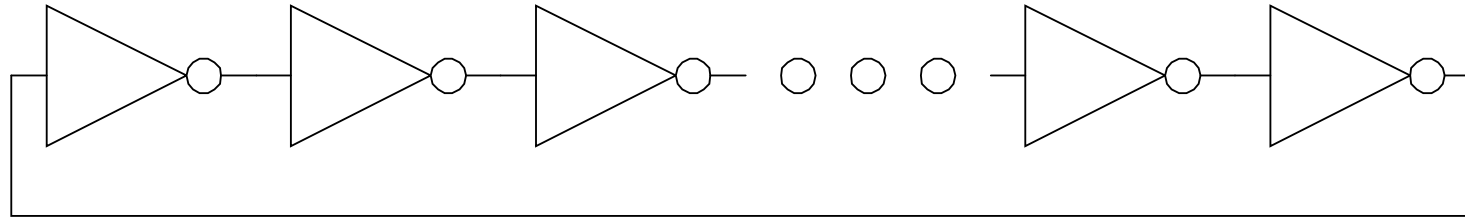
- Example 4.10



- Logical effort: $g = 1$
- Electrical effort: $h = 4$
- Parasitic delay: $p = 1$
- Stage delay: $d = 5$
- When $\tau = 3RC = 3$ ps, the total delay is 15 ps.

4.4. Linear delay model (7)

- Example 4.11



- A ring oscillator with an odd number (N) of inverters
- Logical effort: $g = 1$
- Electrical effort: $h = 1$
- Parasitic delay: $p = 1$
- Stage delay: $d = 2$
- Frequency: $f_{osc} = \frac{1}{2Nd} = \frac{1}{4Nd}$

4.5 Logical Effort of Paths

4.5. Logical effort of paths (1)

- Multistage logic networks
 - Logical effort is independent of size.
 - Electrical effort depends on sizes.

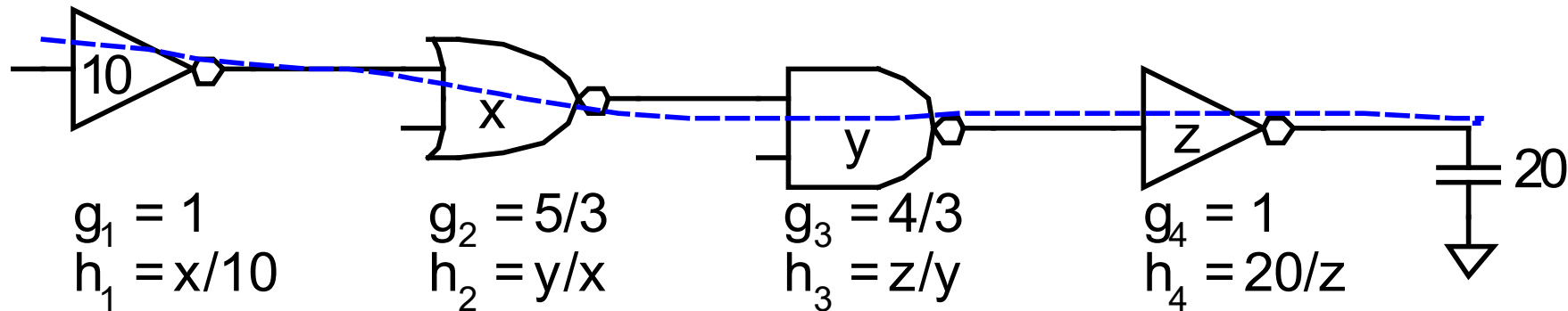


Fig. 4.29

- What is the total propagation delay?

$$D = \frac{x}{10} + 1 + \frac{5y}{3x} + 2 + \frac{4z}{3y} + 2 + \frac{20}{z} + 1$$

4.5. Logical effort of paths (2)

- Minimum propagation delay?

- Parasitic delay is given as 6.

$$D = 6 + \frac{x}{10} + \frac{5y}{3x} + \frac{4z}{3y} + \frac{20}{z}$$

- Minimize the effort delay.

- Recall the inequality of arithmetic and geometric means

$$f_1 + f_2 + \cdots + f_N \geq N \sqrt[N]{f_1 f_2 \cdots f_N}$$

The equality holds if and only if $f_1 = f_2 = \cdots = f_N$.

4.5. Logical effort of paths (3)

- Product of effort delays is a constant.

– In our example,

$$D = 6 + \frac{x}{10} + \frac{5y}{3x} + \frac{4z}{3y} + \frac{20}{z} \geq 6 + 4 \sqrt[4]{\frac{40}{9}}$$

– The equality holds when $\frac{x}{10} = \frac{5y}{3x} = \frac{4z}{3y} = \frac{20}{z} = \sqrt[4]{\frac{40}{9}} \approx 1.45$.

- Minimum possible delay of an N –state path

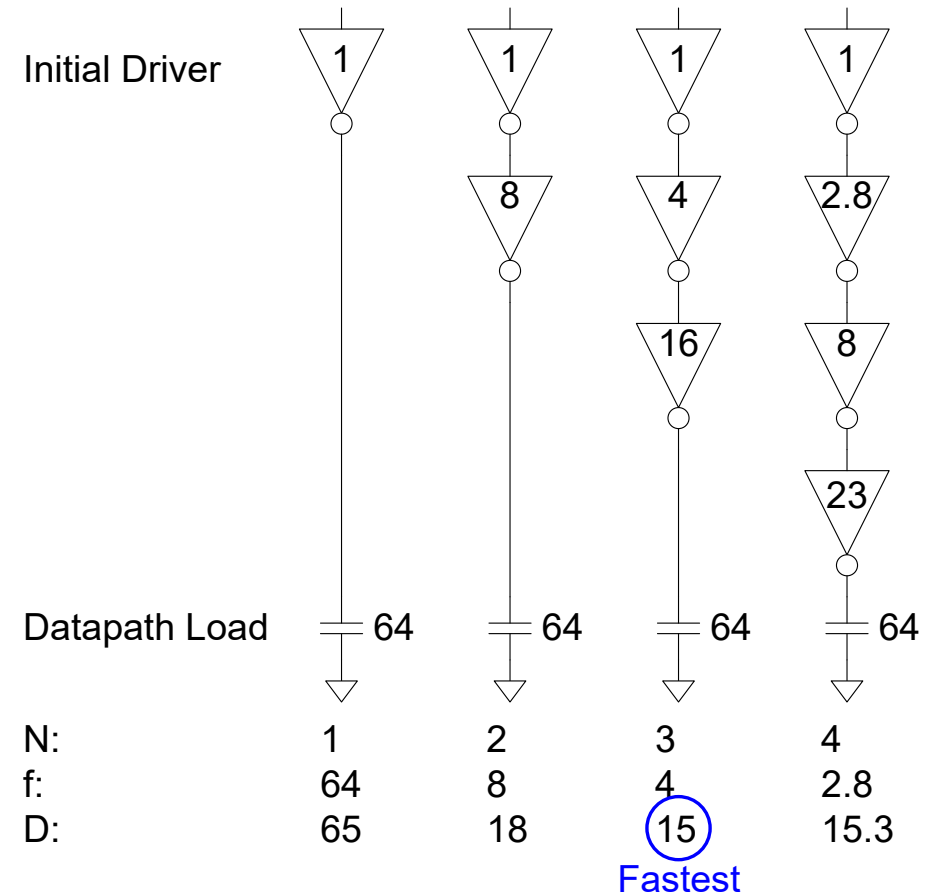
$$D = N \sqrt[N]{F} + P$$

– F : Path effort

– P : Path parasitic delay

4.5. Logical effort of paths (4)

- Exampe 4.14
 - Determine the number of stages.
 - $N = 1: D = 1 + 64$
 - $N = 2: D = 2 + 2\sqrt{64}$
 - $N = 3: D = 3 + 3\sqrt[3]{64}$



Thank you!