Digital Integrated Circuit
Lecture 8 MOS Transistor Theory

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Review of Previous Lecture

Lecture 7

- Nonideal IV
  - Mobility degradation due to the vertical electric field
  - Velocity saturation

2.4 Nonideal IV

2.4. Nonideal IV (7)

- Velocity saturation
  - Saturation velocity (Canali model)
  - Electrons: 1.07×10^7 cm/sec
  - Holes: 8.37×10^6 cm/sec
  - A simple model

$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases}$$

$$E_c = \frac{2 v_{\text{sat}}}{\mu_{\text{eff}}}$$

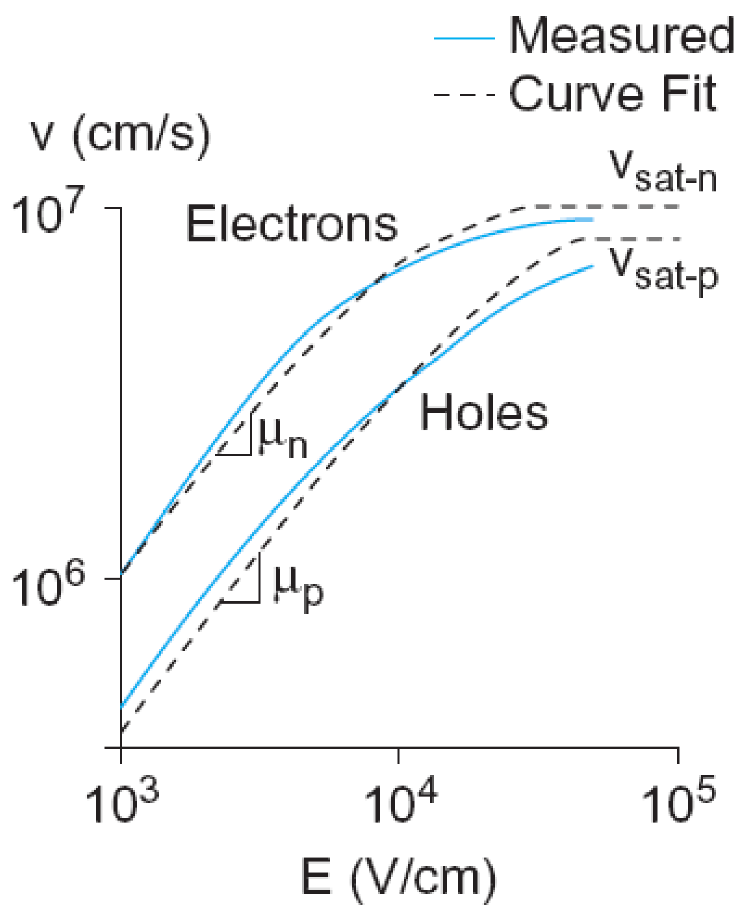


Fig. 2.15

2.4. Nonideal IV (8)

- When the electric field is lower than E_c,

$$E = \frac{I_d}{\mu_n C_{OX} W\left(V_g - V_t - V_c\right) - \frac{I_d}{E_c}} = \frac{dV_c}{dx}$$

  - (Note that the sign is not correct but understood.)
  - Then, the integration gives

$$LI_d = \int_{V_s}^{V_d} \left[\mu_n C_{OX} W\left(V_g - V_t - V_c\right) - \frac{I_d}{E_c}\right] dV_c$$

$$= \mu_n C_{OX} W\left[\left(V_g - V_t\right)V_{ds} - \frac{1}{2}V_{ds}^2\right] - \frac{I_d}{E_c} V_{ds}$$

2.4. Nonideal IV (9)

- Drain current with the velocity saturation

$$I_d = \frac{1}{L + \frac{V_{ds}}{E_c}} \mu_n C_{OX} W \left[\left(V_g - V_t \right) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

  – With $V_c = E_c L$,

$$I_d = \frac{1}{1 + \frac{V_{ds}}{V_c}} \mu_n C_{OX} \frac{W}{L} \left[\left(V_g - V_t \right) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

  – The factor, $\frac{1}{1+\frac{V_{ds}}{V_c}}$, describes the velocity saturation.

  – Then, when do we have the saturation?

2.4. Nonideal IV (10)

- Condition for saturation, $E = E_c$ @ $x = L$
  - In this case, $V_d = V_{dsat}$ and $I_d = I_{dsat}$

$$E_c = \frac{I_{dsat}}{\mu_n C_{OX} W\left(V_g - V_t - V_{dsat}\right) - \frac{I_{dsat}}{E_c}}$$

  - The saturation current becomes

$$I_{dsat} = \frac{1}{2}\mu_n C_{OX} W\left(V_g - V_t - V_{dsat}\right) E_c$$

  - What is V_{dsat}?

2.4. Nonideal IV (11)

- Equating two expressions,

$$I_{dsat} = \frac{1}{2}\mu_n C_{OX} W \left(V_g - V_t - V_{dsat}\right) E_c$$

$$I_{dsat} = \frac{1}{1 + \frac{V_{dsat}}{V_c}} \mu_n C_{OX} \frac{W}{L}\left[\left(V_g - V_t\right) V_{dsat} - \frac{1}{2} V_{dsat}^2\right]$$

  - With the gate overdrive voltage, $V_{GT} \equiv V_g - V_t$, we can find

$$V_{dsat} = \frac{V_{GT} V_c}{V_{GT} + V_c}$$

$$I_{dsat} = C_{OX} W \frac{V_{GT}^2}{V_{GT} + V_c} v_{sat}$$

  - Two extreme cases, $V_{GT} \ll V_c$ and $V_{GT} \gg V_c$

Homework#2

- Due: AM08:00, September 26
- Problem#1
  - Compare three modes for the velocity saturation:
  - 1) The one studied in this lecture.
  - 2) $v_{sat} = \frac{\mu_{eff}E}{\sqrt{1+\left(\frac{E}{E_c}\right)^2}}$
  - 3) $v_{sat} = \frac{\mu_{eff}E}{1+\frac{E}{E_c}}$ for any E value
  - Draw the velocity-field graph in the semi-logarithmic scale. μ_{eff} is 710 cm^2/V sec and E_c is 11 kV/cm. The electric field varies from 100 V/cm to 100 kV/cm.

Homework#2

- Problem#2
  - Draw the output characteristics of an NMOSFET, by using two IV models. Compare them.
  - 1) Long-channel IV
  - 2) The one studied in this lecture.
  - Parameters are: W is 100 µm. L is 1 µm. t_{ox} is 25 nm. The effective mobility is assumed to be a constant of 500 cm^2/V sec, for simplicity. E_c is 11 kV/cm. Consider five values of V_{GT}: 0.5 V, 1.0 V, 1.5 V, 2.0 V, and 2.5 V. Increase the drain voltage up to 3.0 V.

2.4. Nonideal IV (12)

- Threshold voltage (Body effect)
  - It is given by

$$V_t = \frac{\sqrt{2\epsilon_{si} q N_A}}{C_{ox}} \sqrt{\phi_s + V_{sb}} + V_{FB} + \phi_s$$

$$\phi_s = 2v_T \log \frac{N_A}{n_i}$$

  - At zero V_{sb},

$$V_{t0} = \gamma \sqrt{\phi_s + V_{sb}} + V_{FB} + \phi_s$$

  - Therefore,

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

2.4. Nonideal IV (13)

- Leakage
  - Subthreshold slope
  - Drain-induced barrier lowering
  - Gate-induced drain leakage

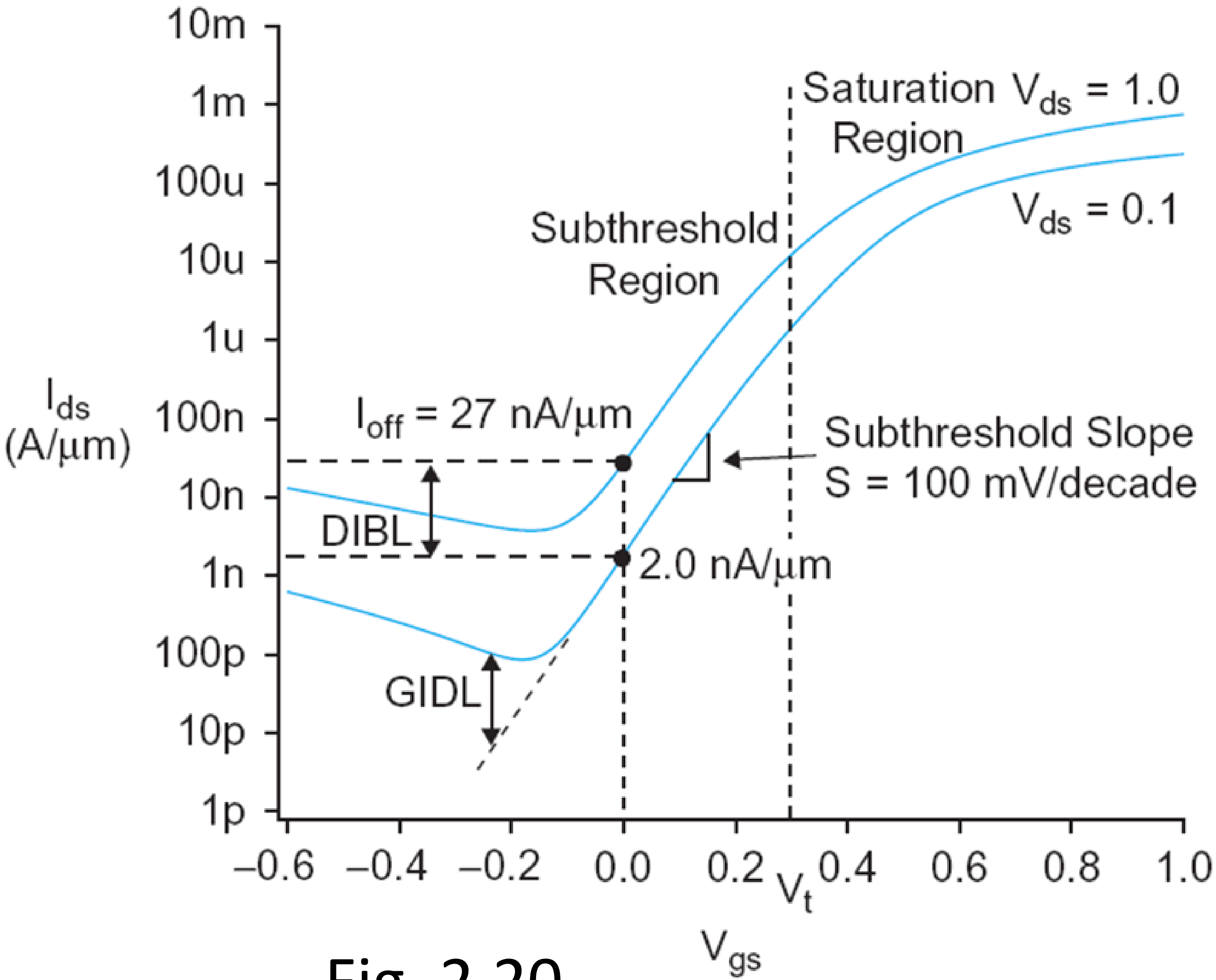


Fig. 2.20

2.5 DC Transfer

2.5. DC transfer (1)

- A CMOS inverter
  - The transistor is a switch with an infinite off-resistance and a finite on-resistance.

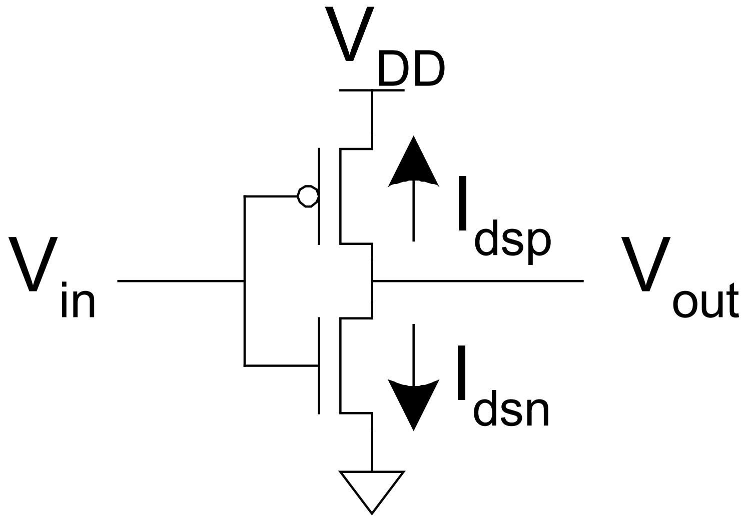
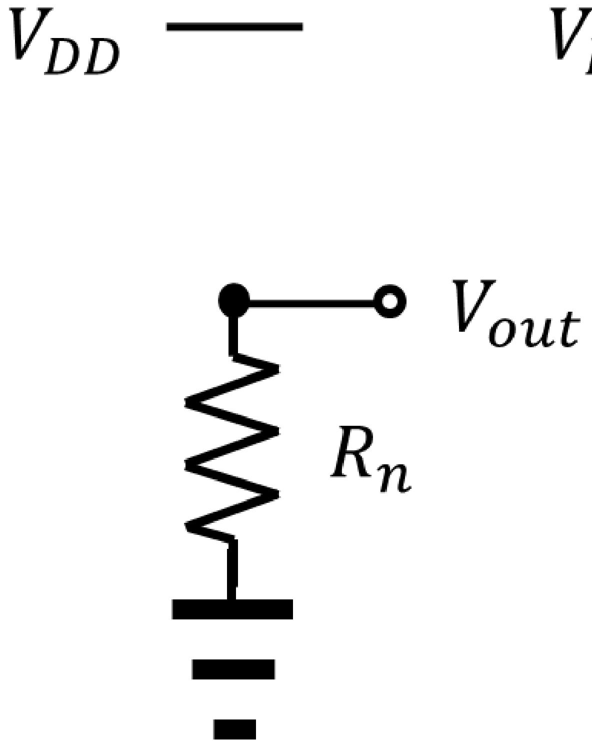
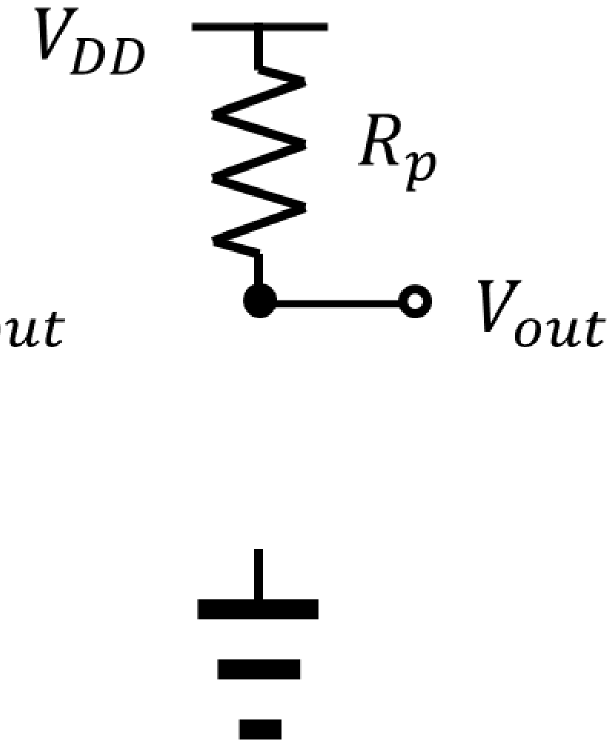


Fig. 2.25





2.5. DC transfer (2)

- Important properties (Taken from Rabaey's book)
  - The HIGH and LOW output levels equal V_{DD} and GND, respectively.
  - The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size. (Ratioless)
  - A well-designed CMOS inverter has a low output impedance.
  - The input resistance of the CMOS inverter is extremely high.
  - The absence of current flow between V_{DD} and GND means that the logic gate does not consume any static power.

2.5. DC transfer (3)

- We have five points. Identify the operational modes of transistors.

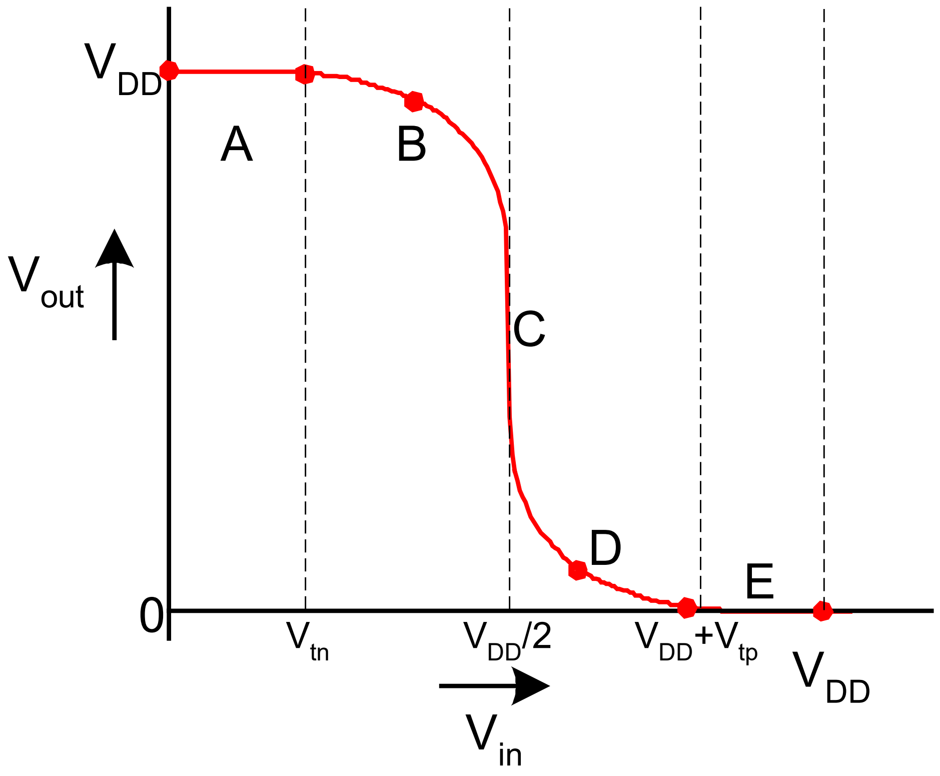


Fig. 2.26(c)

2.5. DC transfer (4)

- Input threshold, V_{inv} (or switching threshold)
  - When $V_{in} = V_{out} = V_{inv}$
- β ($\frac{W}{L}\mu C_{OX}$) ratio
  - HIGH-skewed, $\frac{\beta_p}{\beta_n} > 1$, stronger PMOS
  - LOW-skewed, $\frac{\beta_p}{\beta_n} < 1$, weaker PMOS

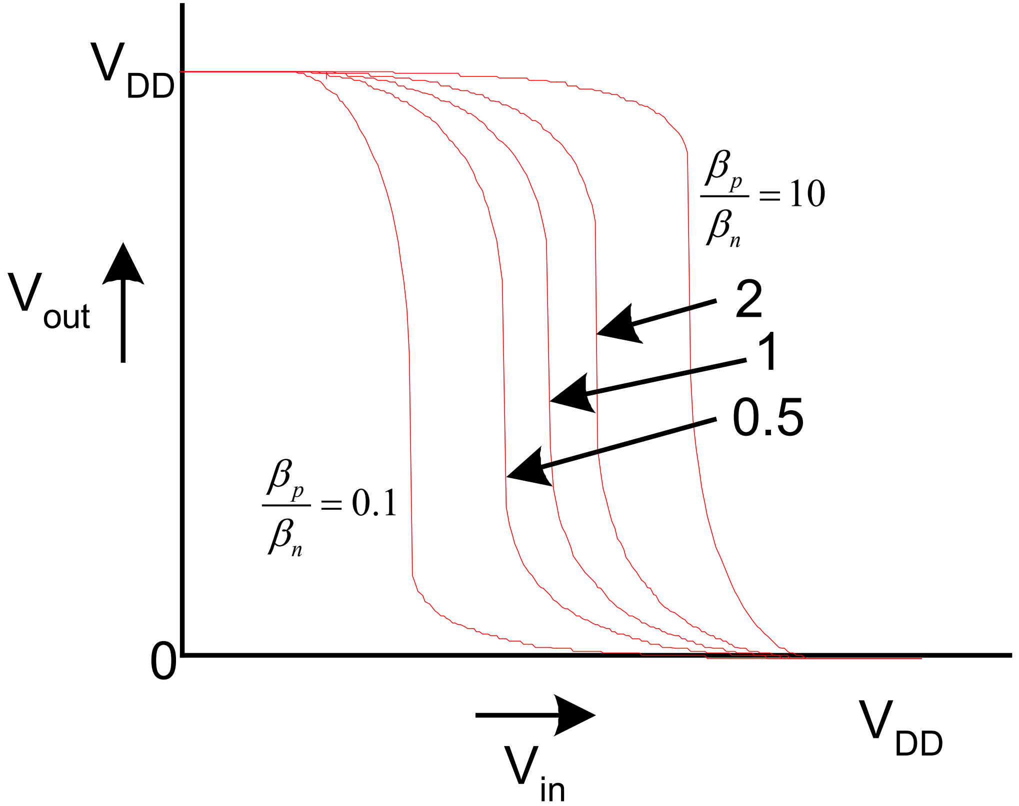


Fig. 2.28

2.5. DC transfer (5)

- Quantitative analysis for V_{inv}
  - Use the long-channel IV

$$I_{dn} = \frac{\beta_n}{2}(V_{inv} - V_{tn})^2 \text{ and } I_{dp} = -\frac{\beta_p}{2}\left(V_{inv} - V_{DD} - V_{tp}\right)^2$$

  - After manipulation, we have

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$$

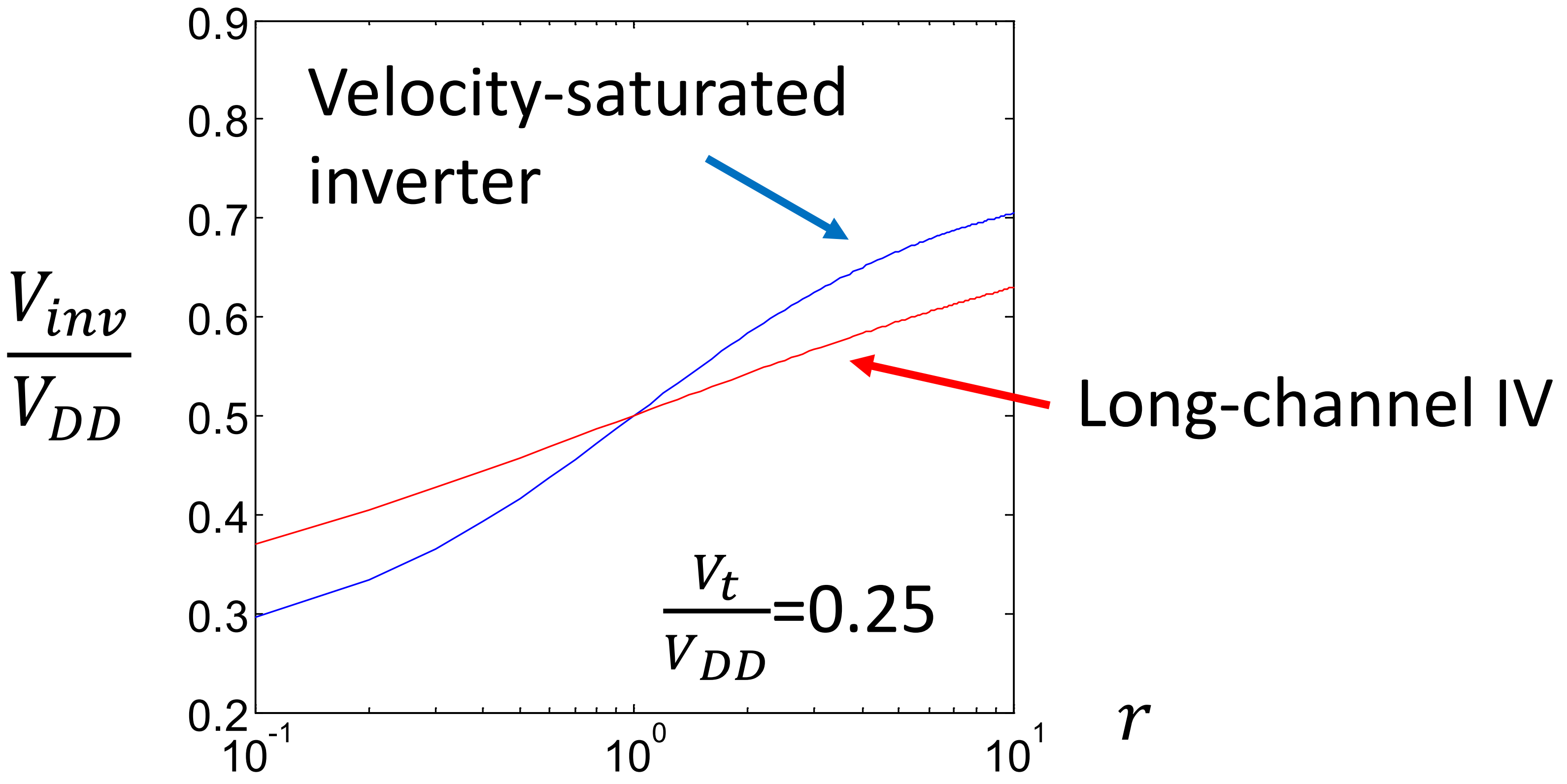
  - (Here, $r = \frac{\beta_p}{\beta_n}$)
  - For a special case with $r = 1$, $V_{inv} = \frac{V_{DD}+V_{tn}+V_{tp}}{2}$

2.5. DC transfer (6)

- Quantitative analysis for V_{inv} with velocity saturation
  - Use the following expressions:
$$I_{dn} = W_n C_{ox} v_{sat-n}(V_{inv} - V_{tn})$$
$$I_{dp} = -W_p C_{ox} v_{sat-p}\left(V_{inv} - V_{DD} - V_{tp}\right)$$
  - After manipulation, we have
$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}}$$
  - (Here, $r = \frac{W_p v_{sat-p}}{W_n v_{sat-n}}$)
  - For a special case with $r = 1$, $V_{inv} = \frac{V_{DD}+V_{tn}+V_{tp}}{2}$

2.5. DC transfer (7)

- Compare them.
  - Let's draw $\frac{V_{inv}}{V_{DD}}$ as a function of r. Assume that $V_t = V_{tn} = -V_{tp}$.



2.5. DC transfer (8)

- Width ratio (Velocity-saturated inverter)
  - It is found that

$$r = \frac{W_p v_{sat-p}}{W_n v_{sat-n}} = \frac{V_{inv} - V_{tn}}{V_{DD} - V_{tp} - V_{inv}}$$

  - The width ratio is given by

$$\frac{W_p}{W_n} = \frac{v_{sat-n}(V_{inv} - V_{tn})}{v_{sat-p}\left(V_{DD} - V_{tp} - V_{inv}\right)}$$

Thank you!