Digital Integrated Circuit
Lecture 21 Circuit Simulation

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Review of Previous Lecture

Lecture 20

- SPICE
  - Modified nodal analysis: KCL for every circuit node
  - We need expressions for branch currents.
  - MOSFET models:

```
Mname drain gate source body type W=<width>
L=<length>
```

  - Simulation methods: .dc, .tran, …

8.3 Device Models

8.3. Device models (1)

- Level 1 model (Shichman-Hodges)
  - Its basic current model is:
  - Cutoff region, $V_{gs} < V_t$

$$I_d = 0$$

  - Linear region, $V_{ds} < V_{gs} - V_t$

$$I_d = KP \frac{W_{eff}}{L_{eff}} (1 + LAMBDA \times V_{ds}) \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

  - Saturation region, $V_{ds} > V_{gs} - V_t$

$$I_d = \frac{KP}{2} \frac{W_{eff}}{L_{eff}} (1 + LAMBDA \times V_{ds}) \left(V_{gs} - V_t \right)^2$$

  - (Red-colored quantities are the SPICE model parameters.)

8.3. Device models (2)

- Level 1 model (Shichman-Hodges)
  - Threshold voltage:
  - For nonnegative V_{sb},

$$V_t = VTO + GAMMA\left(\sqrt{PHI + V_{sb}} - \sqrt{PHI}\right)$$

  - VTO is the "zero-bias" threshold voltage.
  - $GAMMA$ is the body effect coefficient.
  - PHI is the surface potential.

8.3. Device models (3)

- Level 1 model (Shichman-Hodges)
  - Gate capacitance:
  - It is calculated from the oxide thickness TOX.

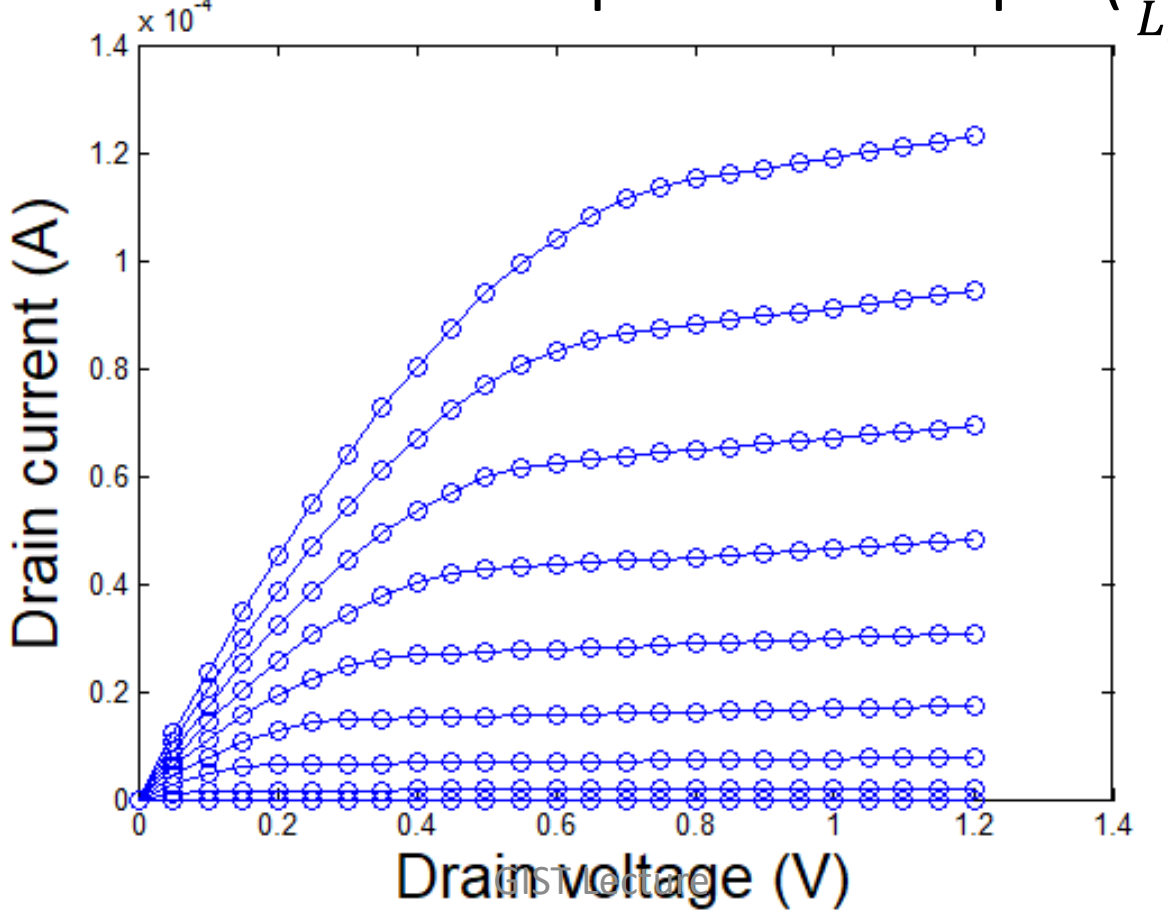
8.3. Device models (4)

- Level 1 model (Shichman-Hodges)
  - Sample level 1 model (taken from Fig. 8.12)

```
.model NMOS NMOS (LEVEL=1 TOX=40e-10 KP=155e-6
+                 LAMBDA=0.2 VTO=0.4 PHI=0.93
+                 GAMMA=0.6 CJ=9.8e-5 PB=0.72
+                 MJ=0.36 CJSW=2.2e-10 PHP=7.5
+                 MJSW=0.1)
```

8.3. Device models (5)

- Level 1 model (Shichman-Hodges)
  - DC output characteristics of the previous sample ($\frac{W_{eff}}{L_{eff}} = 2$)



8.3. Device models (6)

- Level 3 model
  - It is based on empirical equations.
  - Cutoff region, $V_{gs} < V_t$

$$I_d = 0$$

  - On region, $V_{gs} > V_t$

$$I_d = KP \frac{W_{eff}}{L_{eff}} \left(V_{gs} - V_t - \frac{1 + fb}{2} V_{de} \right) V_{de}$$

  - V_{de} is the smaller one between V_{ds} and V_{dsat}.

$$fb = f_n + \frac{GAMMA\ f_s}{4\sqrt{PHI + V_{sb}}}$$

  - f_n and f_s are considering the narrow width effect and the short channel effect, respectively.

8.3. Device models (7)

- BSIM (Berkeley Short-Channel IGFET) model
  - Currently, there are five modesl in the BSIM family:
  - BSIM-CMG: A model for common multi-gate, i.e., FinFET device
  - BSIM-IMG: A model for independent multigate device
  - BSIM-SOI: A model for silicon-on-insulator device
  - BSIM-BULK: A charge-based model for bulk MOSFET
  - BSIM4: A threshold voltage-based model for bulk MOSFET
  - There were BSIM versions 1, 2, and 3.

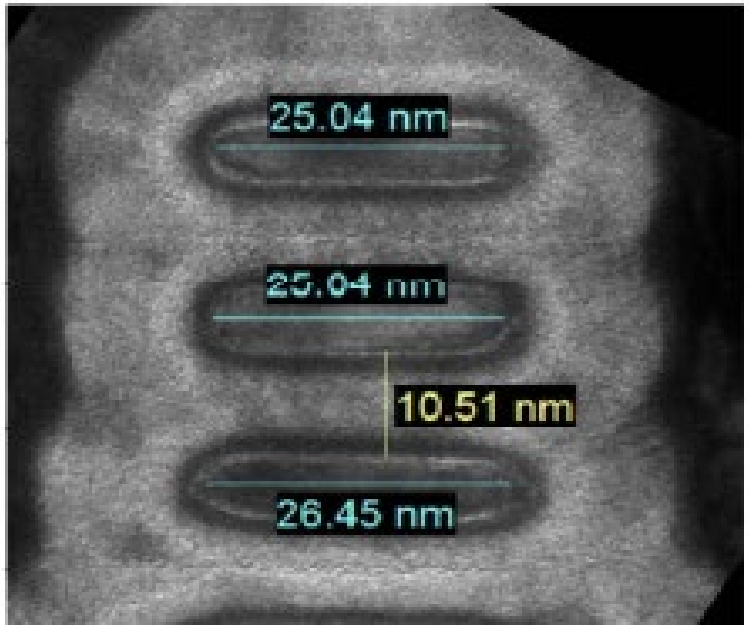
Prof. Chenming Hu

8.3. Device models (8)

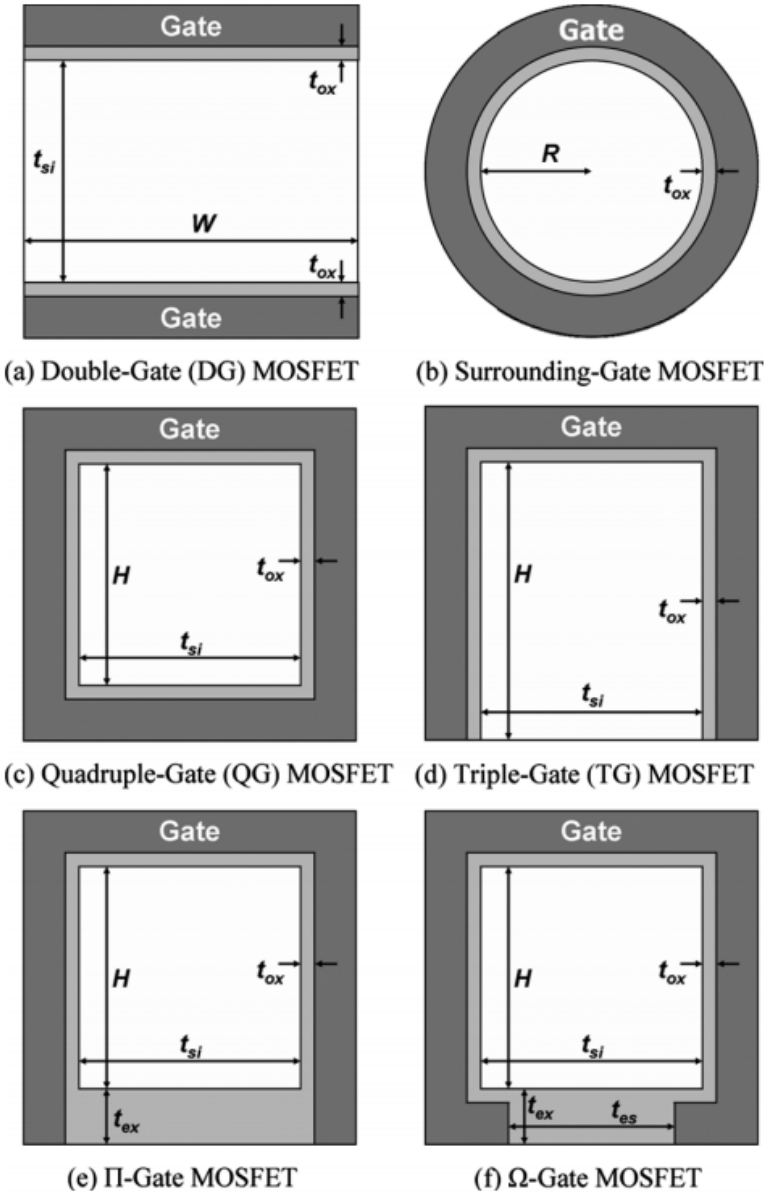
- BSIM (Berkeley Short-Channel IGFET) model
  - Some features:
  - Continuous and differentiable IV characteristics across subthreshold, linear, and saturation regions for good convergence
  - Sensitivity of parameters such as V_t to transistor length and width
  - Detailed threshold voltage model including body effect and drain-induced barrier lowering
  - Velocity saturation, mobility degradation, and other short-channel effects
  - Multiple gate capacitance models
  - Diffusion capacitance and resistance models
  - Gate leakage models

8.3. Device models (9)

- Arbitrary cross-section
  - Double-gate, nanowire, …
  - There have been many many models.
  - Non-trivial shapes



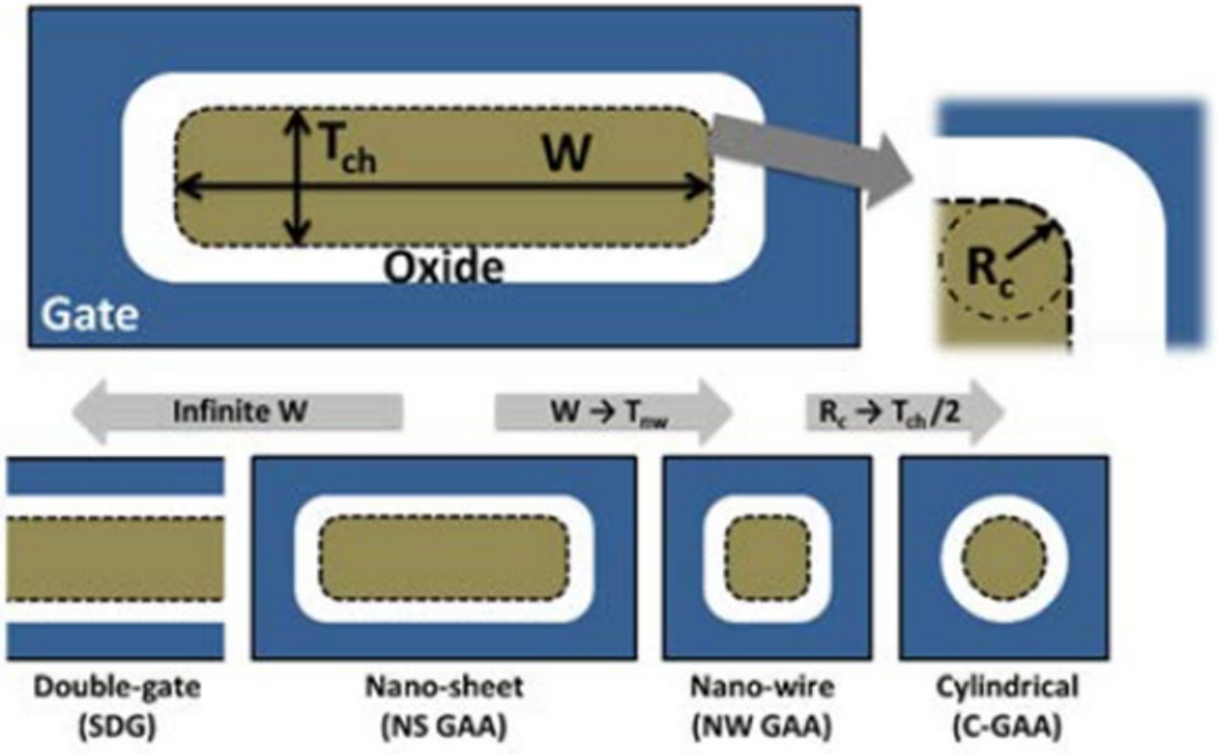
(J. Zhang et al.'s IEDM abstract, 2017)

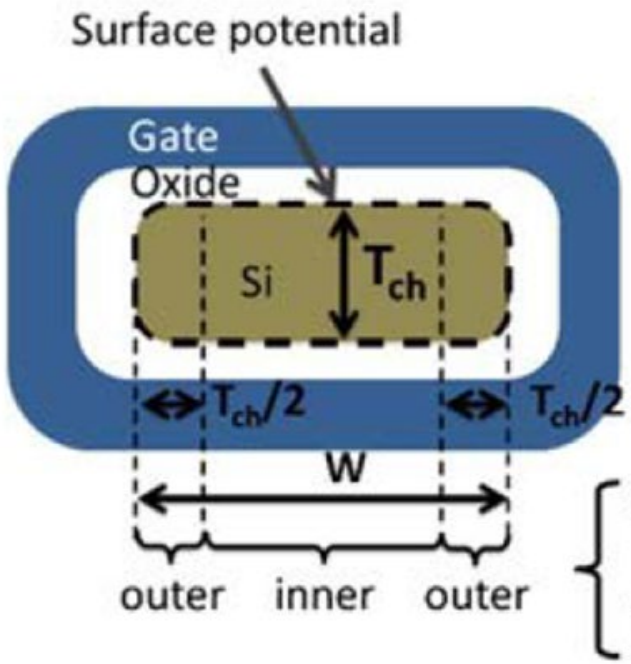


(J. Song et al.'s IEEE TCASI paper, 2009)

8.3. Device models (10)

- Arbitrary cross-section
  - Linear combination is adopted.





$$W = W_{outer} + W_{inner}$$

$$H = \frac{W_{outer}}{W} \cdot H_{outer} + \frac{W - T_{ch}}{W} \cdot T_{ch}$$

$$C'_{ox} = \frac{W_{outer}}{W} \cdot C'_{ox,outer} + \frac{W - T_{ch}}{W} \cdot C'_{ox,inner}$$

$$C'_{si} = \frac{\varepsilon_{si}}{H}$$

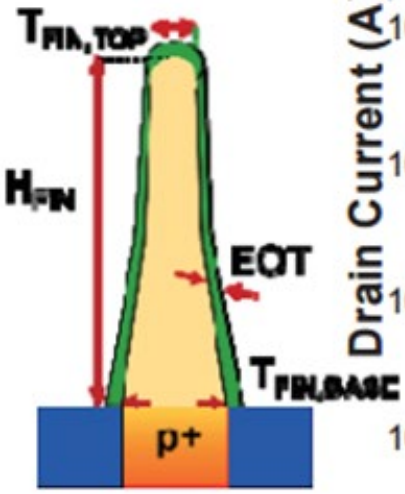
Outer parts: W_{outer}, $C'_{ox,outer}$, H_{outer}

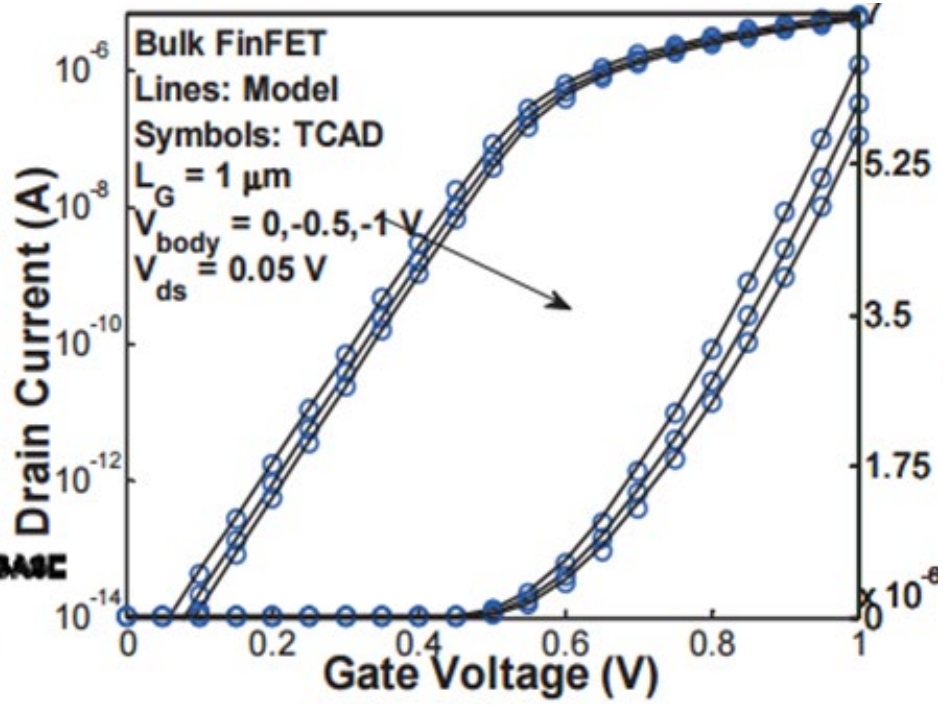
Inner part: W_{inner}, $C'_{ox,inner}$

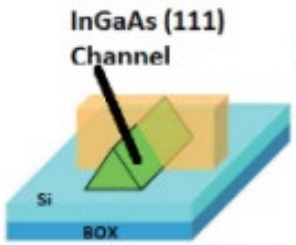
NSP model (O. Rozeau et al.'s IEEE IEDM abstract, 2016)

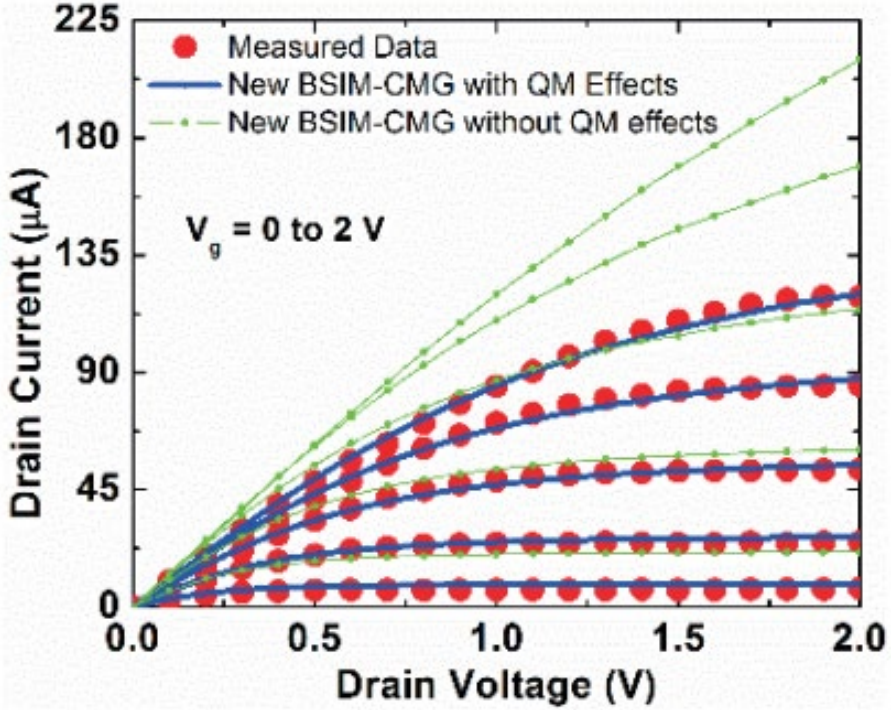
8.3. Device models (11)

- Arbitrary cross-section
  - "Unified FinFET Compact Model"









Various devices tested using BSIM-CMG (VLSI 2015)

8.3. Device models (12)

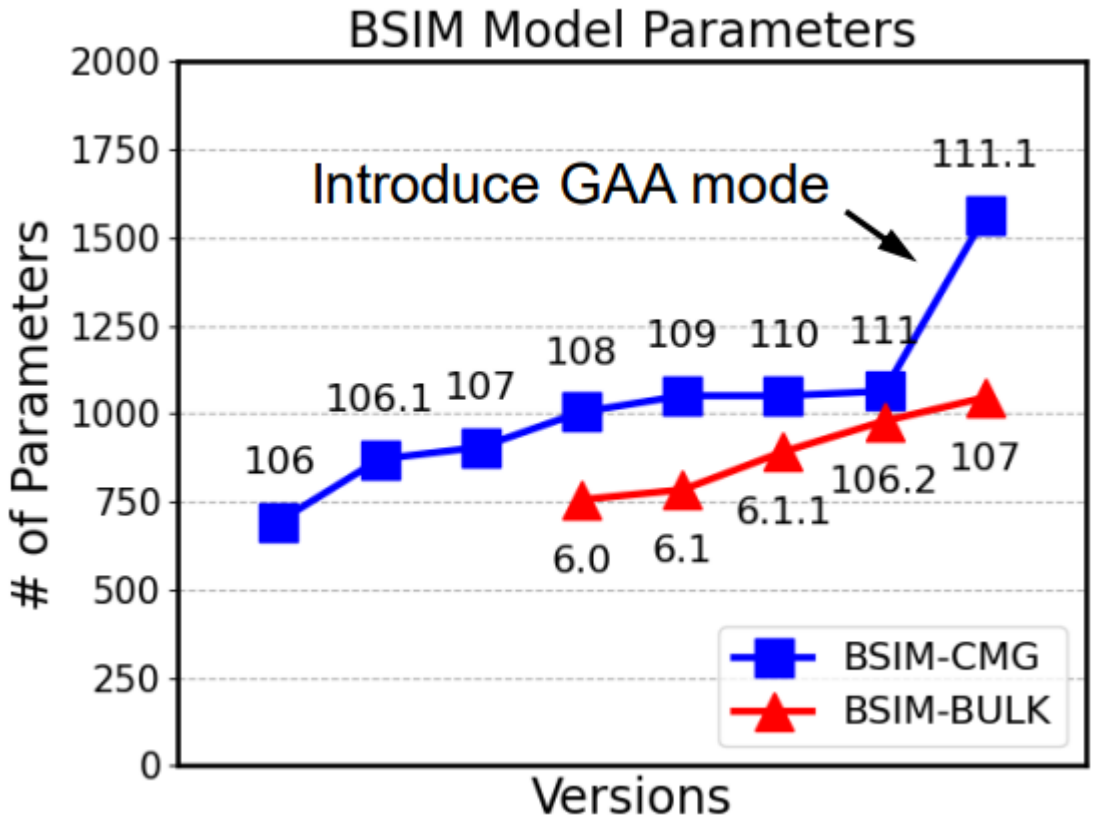
- Arbitrary cross-section
  - It can be rigorously derived.

$$V_G - \Phi_{MS} + \frac{Q_d}{P\langle C_{ins}\rangle_s} + \frac{Q_e}{P\langle C_{ins}\rangle_s}$$

$$\approx V + V_T \log\left(\frac{\frac{1}{2}Q_e^2 + (1-\alpha_e)Q_eQ_d}{q\epsilon P^2 V_T n_{int}\left(1-\beta\exp\left(\frac{A^*}{P^2}\frac{2\alpha_e Q_e + Q_d}{2\epsilon V_T}\right)\right)}\right)$$

8.3. Device models (13)

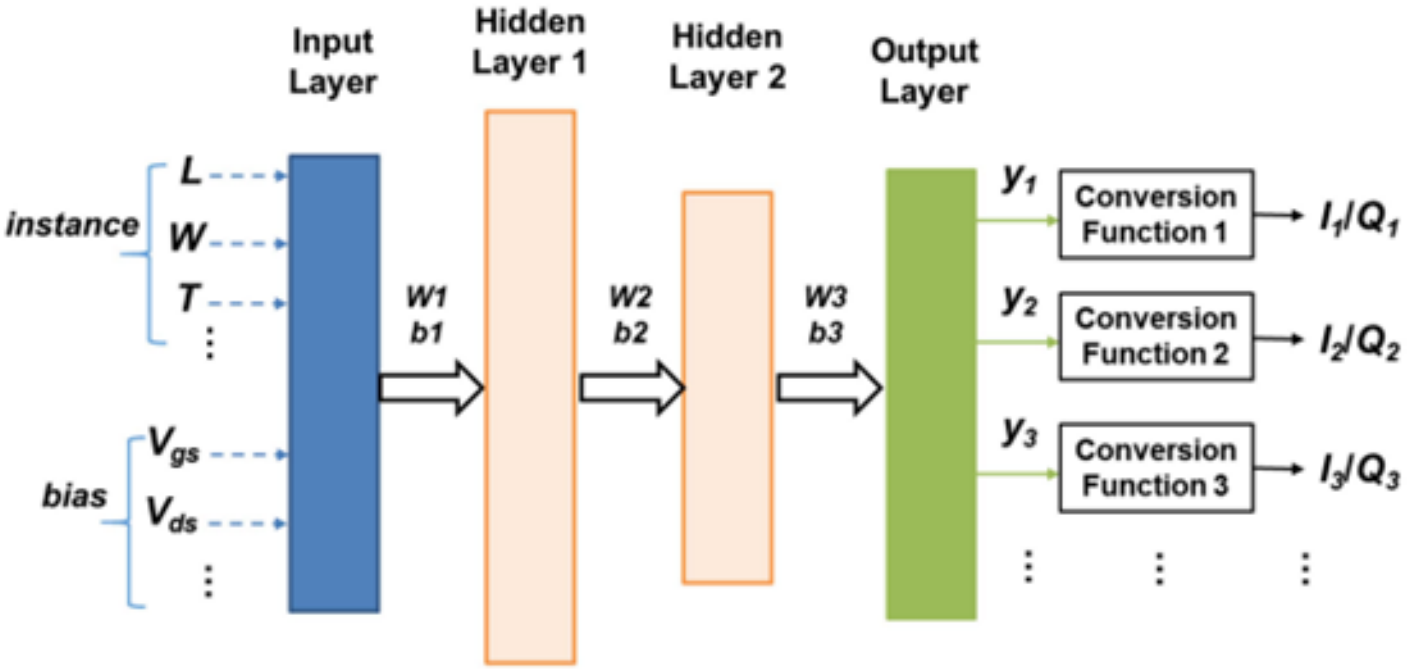
- Neural-network model
  - Number of model parameters is ever increasing!



(Zhihong Liu's MOS-AK presentation, 2021)

8.3. Device models (14)

- Neural-network model
  - As an alternative way, neural compact models are being investigated.



Samsung's neural compact model (IEEE TED, 2021)

Thank you!