Digital Integrated Circuit
Lecture 4 Introduction, MOS Transistor Theory

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Review of Previous Lecture

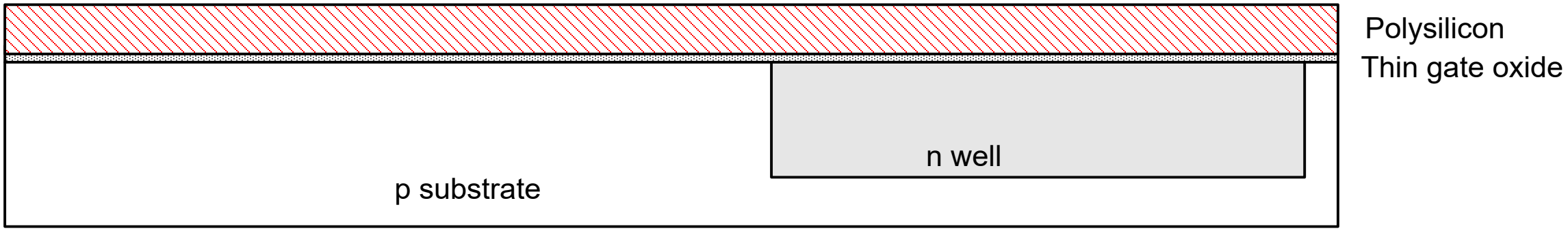
Lecture 3

- Multiplixer
  - Using the tristates, we can implement multiplexers.
- CMOS fabrication
  - Inverter cross-section
  - N-well formation: Lithography, ion-implantation, thermal diffusion

1.5 CMOS Fabrication and Layout

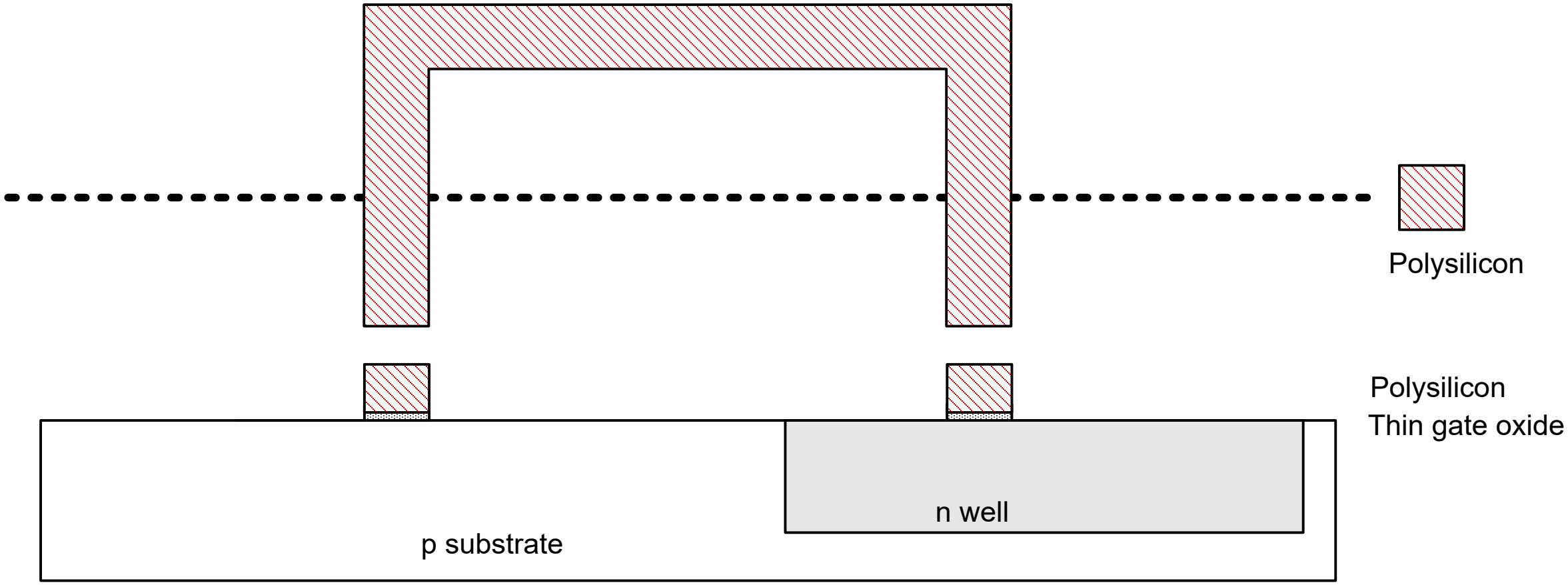
1.5. CMOS fabrication (12)

- Gate oxide and polysilicon
  - The thin oxide is grown in a furnace.
  - Then, the polysilicon layer is grown.



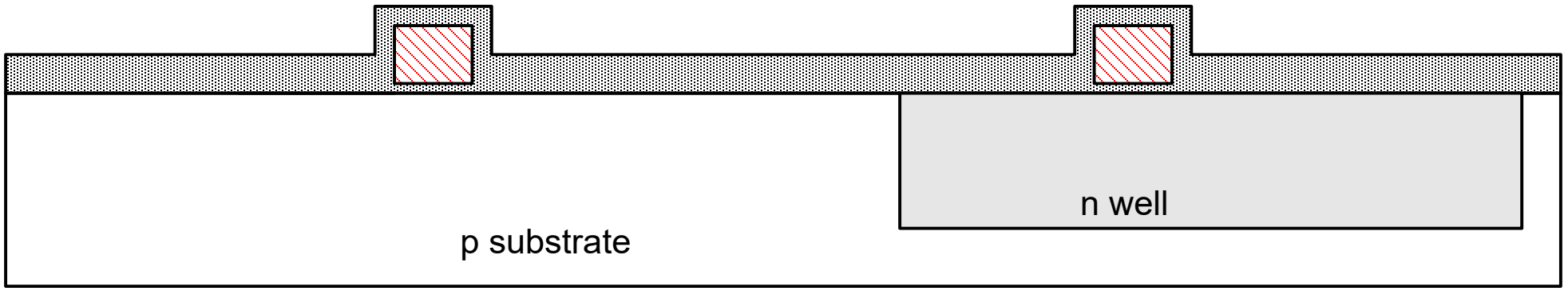
1.5. CMOS fabrication (13)

- Gate patterning



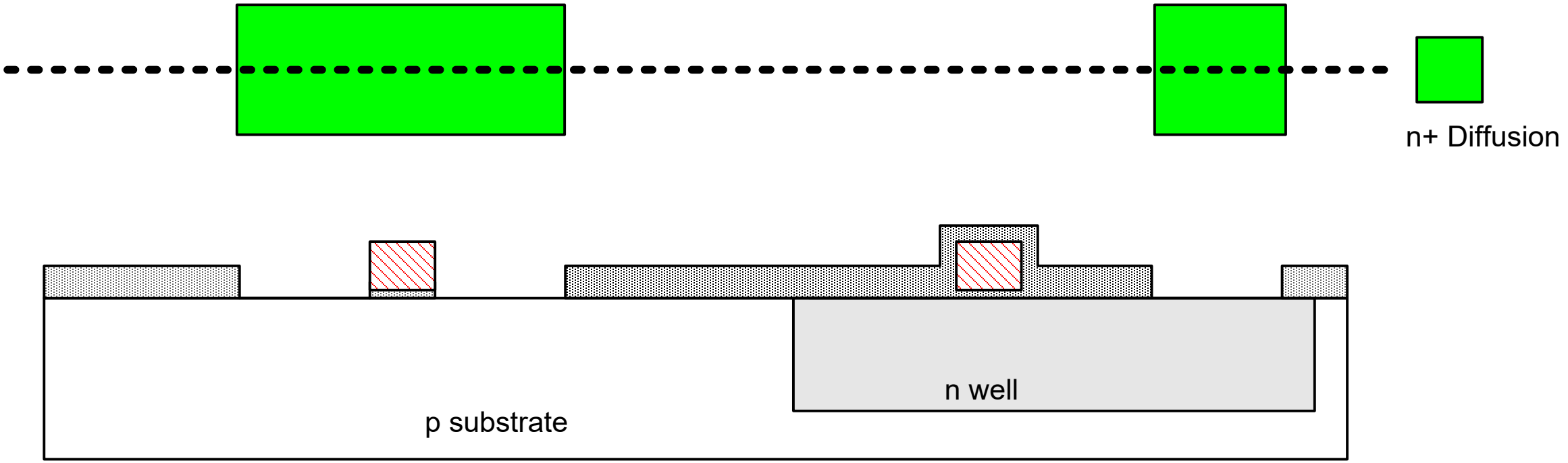
1.5. CMOS fabrication (14)

- Protective layer



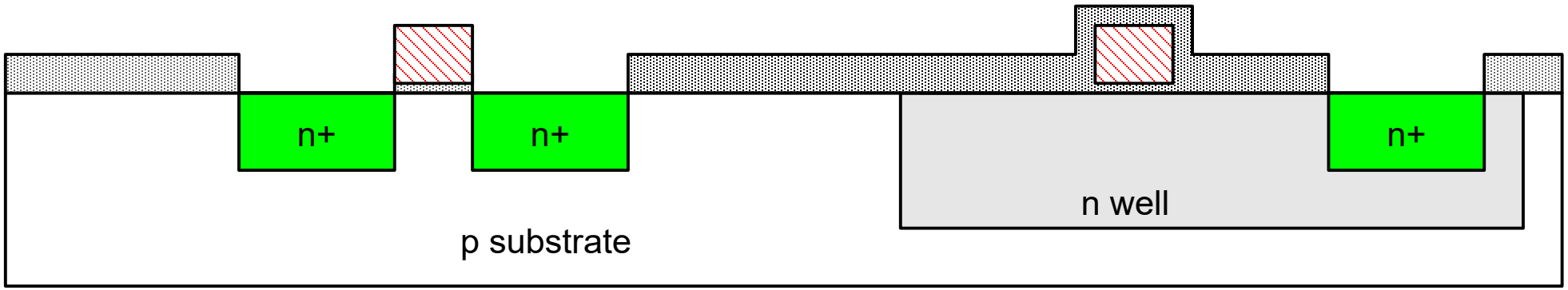
1.5. CMOS fabrication (15)

- N-diffusion
  - Patterned with the n-diffusion mask



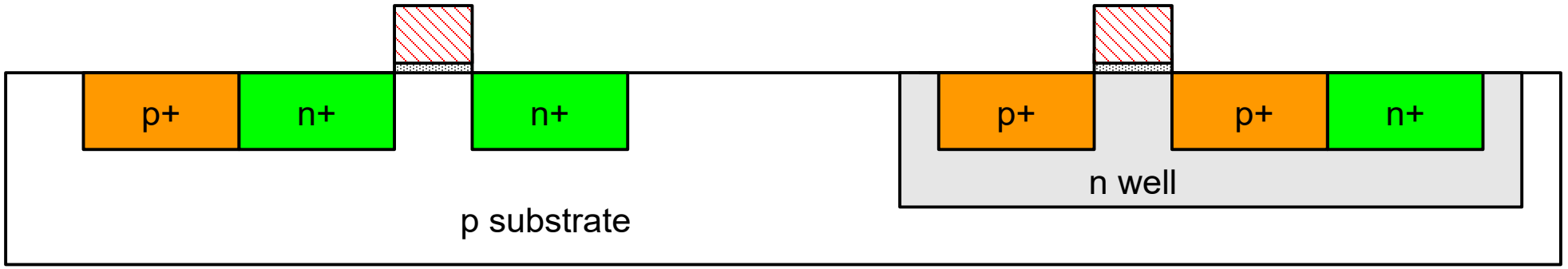
1.5. CMOS fabrication (16)

- Ion implantation
  - Due to the historical reason, it is called *n-diffusion*.
  - The gate blocks the diffusion so the source & drain are separated by a channel under the gate.
  - This is called a *self-aligned* process.



1.5. CMOS fabrication (17)

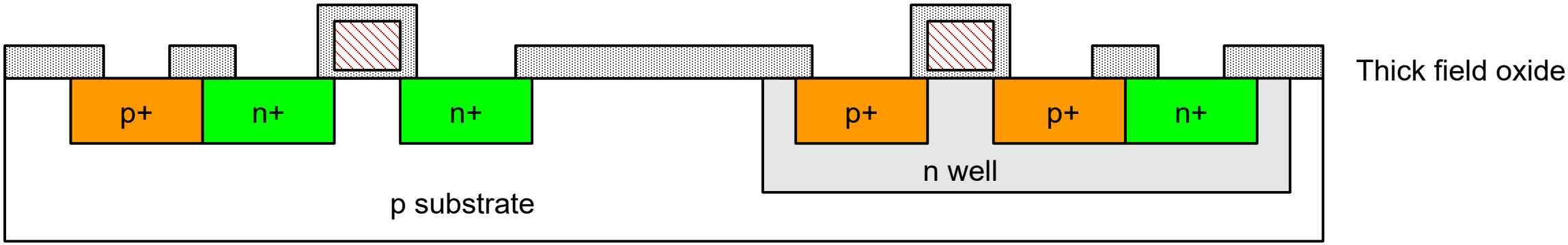
- P-diffusion
  - Repeat the previous process for the p-diffusion mask.



1.5. CMOS fabrication (18)

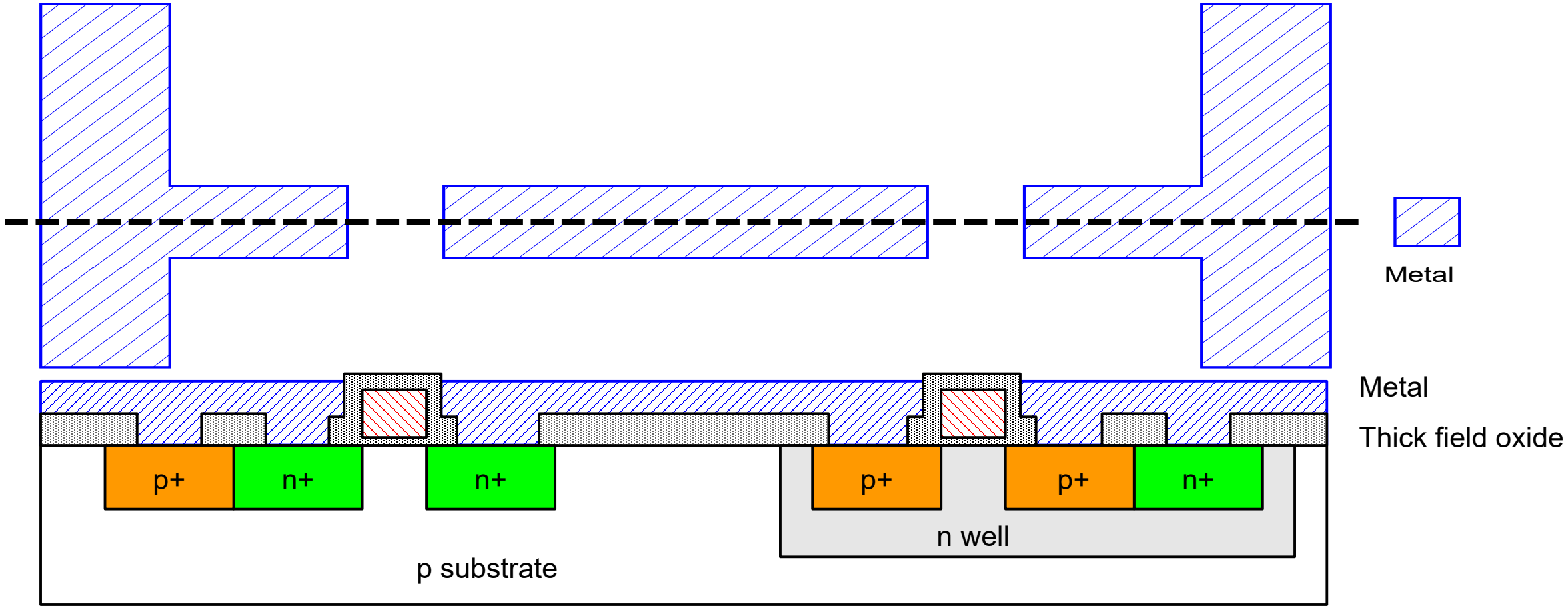
- Contacts
  - The field oxide is grown to insulate the wafer from metal.
  - It is patterned with the contact mask.

Contact



1.5. CMOS fabrication (19)

- Metalization



1.5. CMOS layout (1)

- Layout
  - Minimum dimensions of masks determine transistor size.
  - Feature size refers to minimum transistor length.
  - λ is half the feature size.
  - Transistor dimensions specified as Width / Length in λ.
  - In digital systems, transistors are typically chosen to have the minimum possible length.

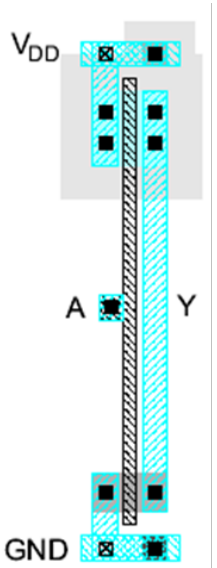
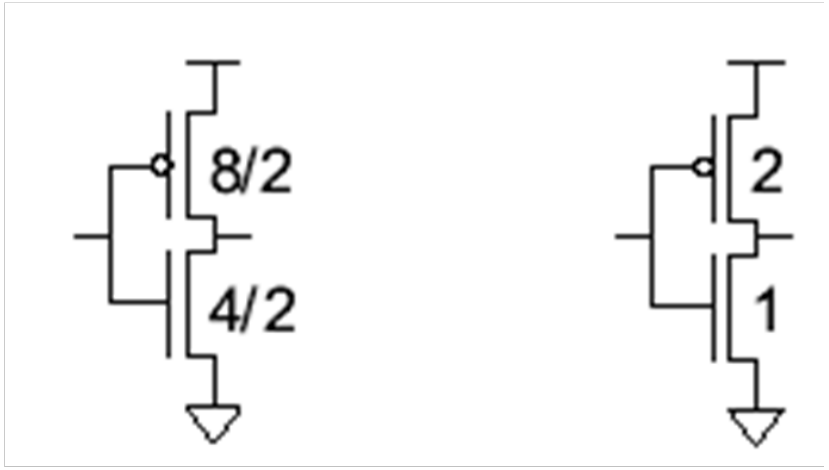


Fig. 1.40



1.5. CMOS layout (2)

- Standard cell design methodology
  - Four horizontal strips: metal groun at the bottom, n-diffusion, p-diffusion, and metal power at the top
  - The power and ground lines are often called *supply rails*.
  - Gate lines run vertically to form transistor gates.

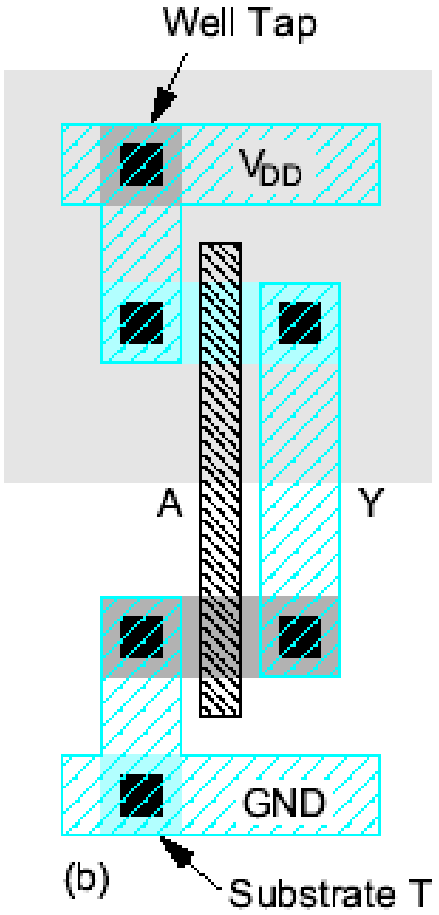


Fig. 1.41(b)

1.5. CMOS layout (3)

- NAND3

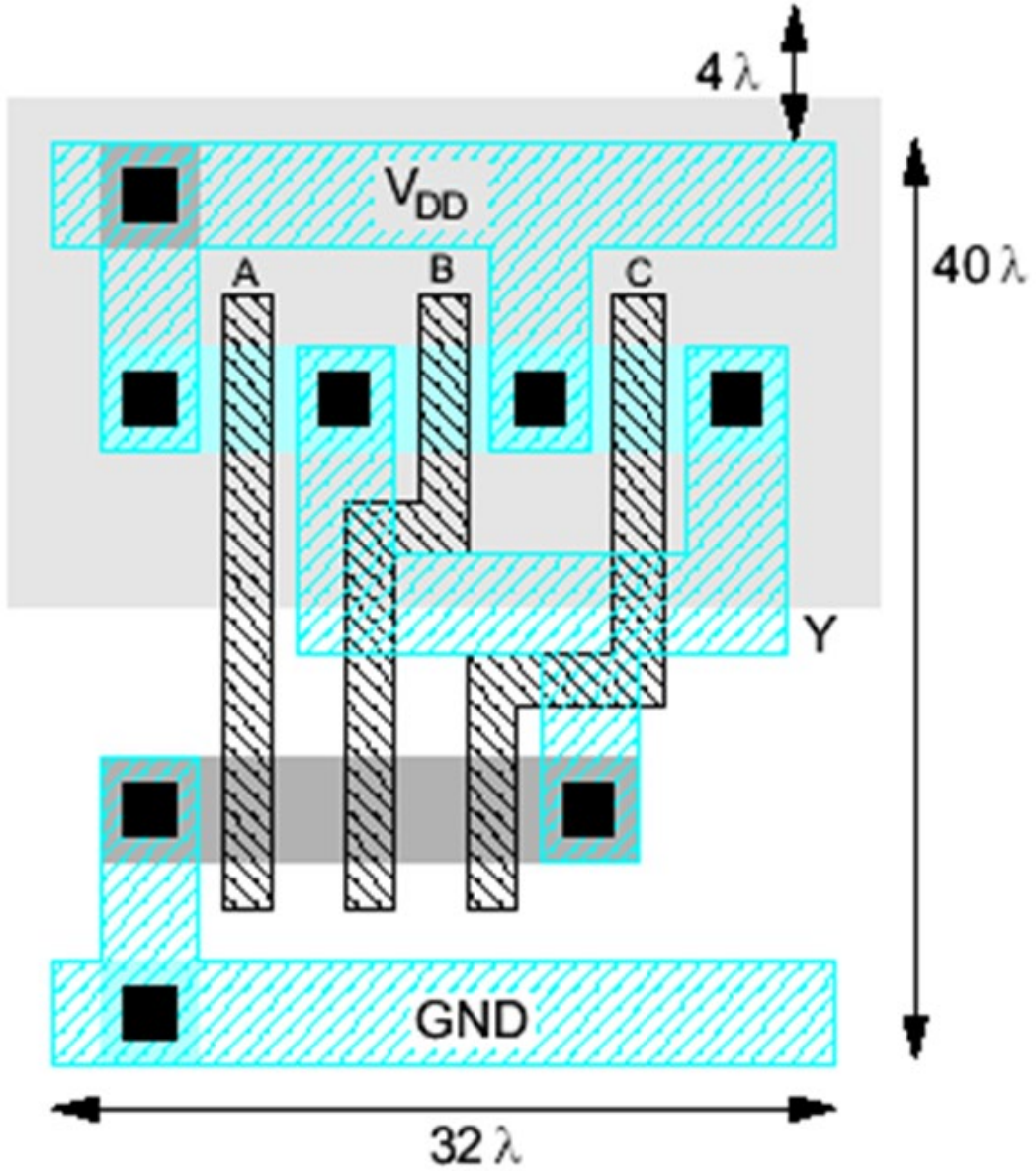


Fig. 1.42

2.1 Introduction

2.1. Introduction (1)

- MOS capacitor
  - Gate / oxide / body
- Operating modes
  - (a) Accumulation
  - (b) Depletion
  - (c) Inversion

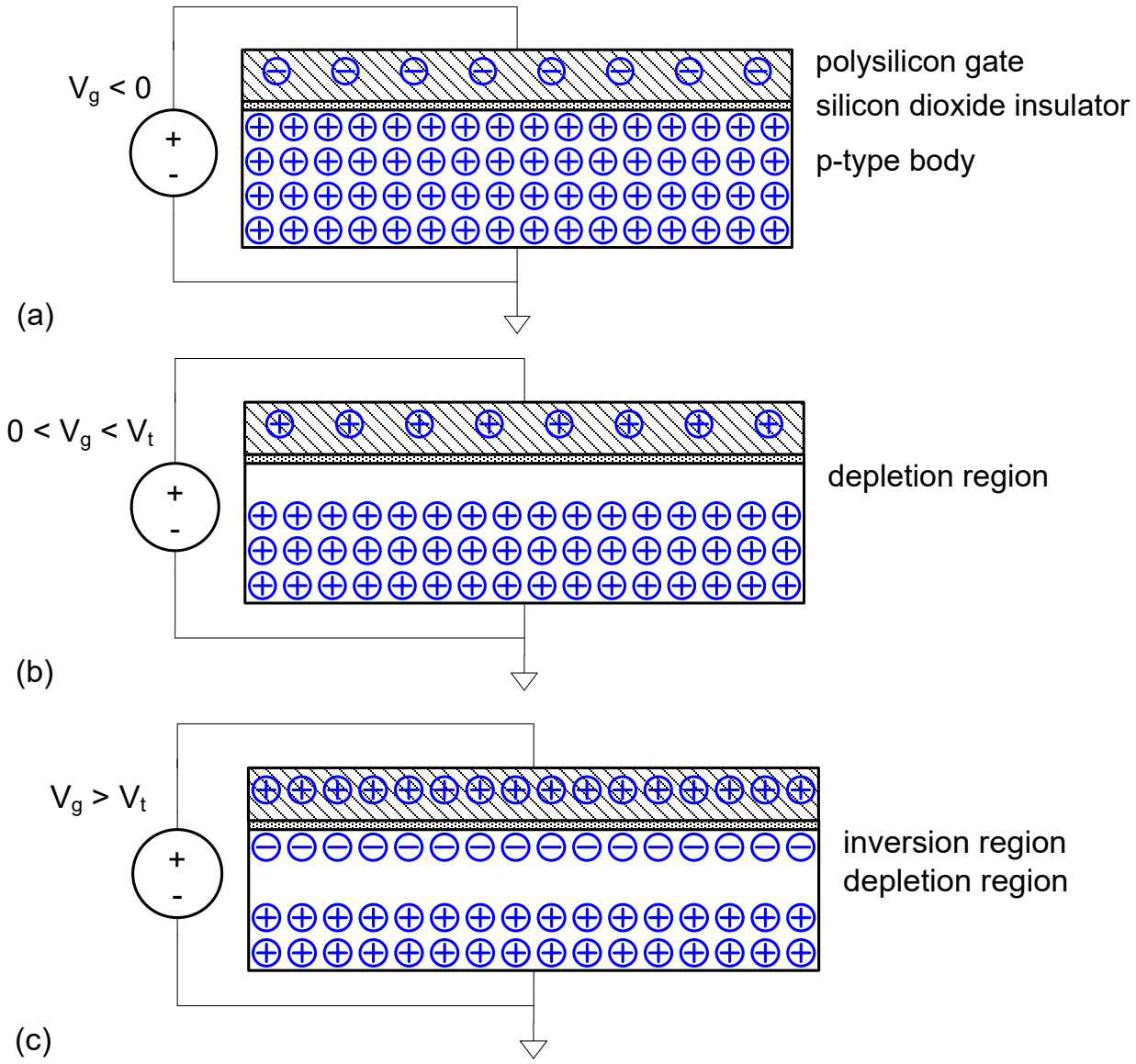
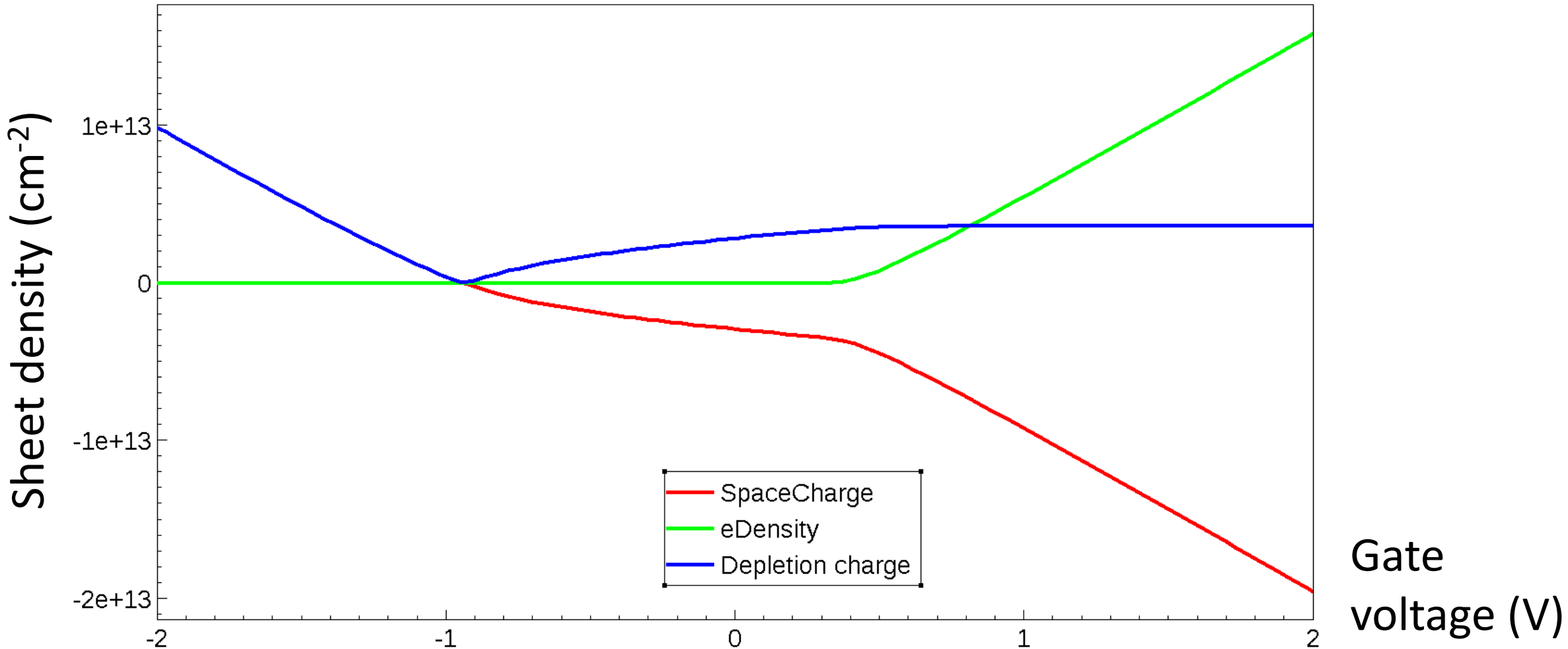


Fig. 2.2

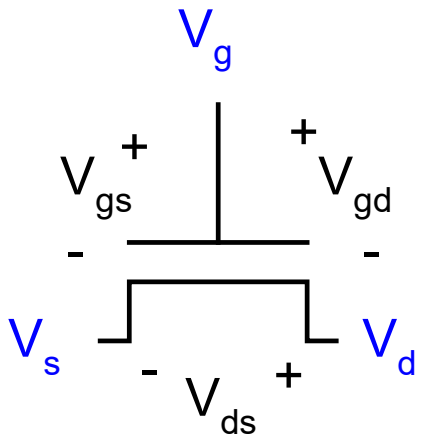
2.1. Introduction (2)

- An example



2.1. Introduction (3)

- MOSFET is a four-terminal device.
  - Source and drain are symmetric.



  - By convention, the source is biased with a lower voltage. Therefore, $V_{ds} \geq 0$.
  - The body of an NMOSFET is grounded.
  - Operation regions: Subthreshold, linear, and saturation

2.1. Introduction (4)

- When the gate-to-source voltage is lower than the threshold voltage (V_t),
  - No mobile carrier. Therefore,

$$I_d \approx 0$$

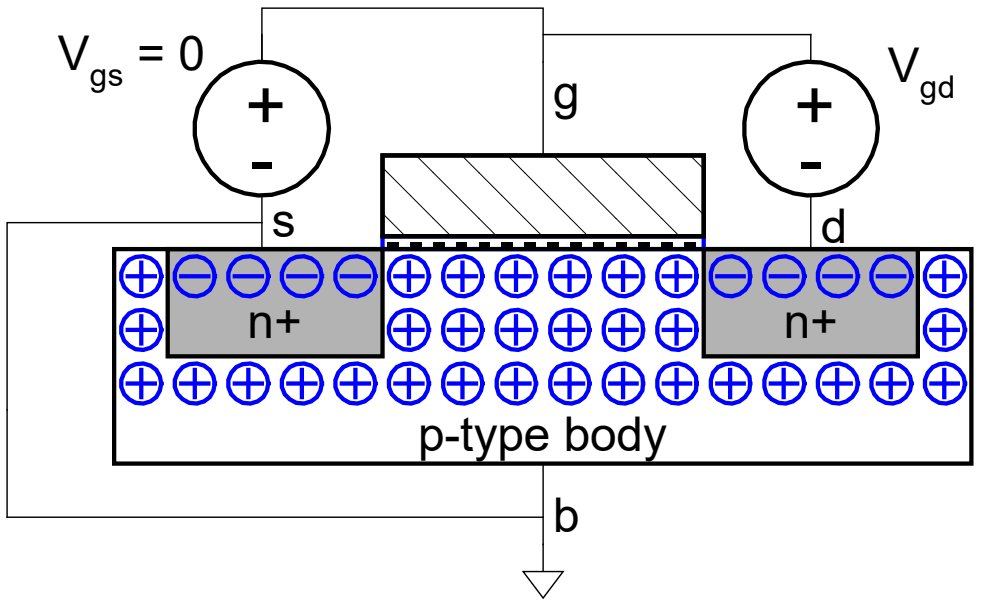
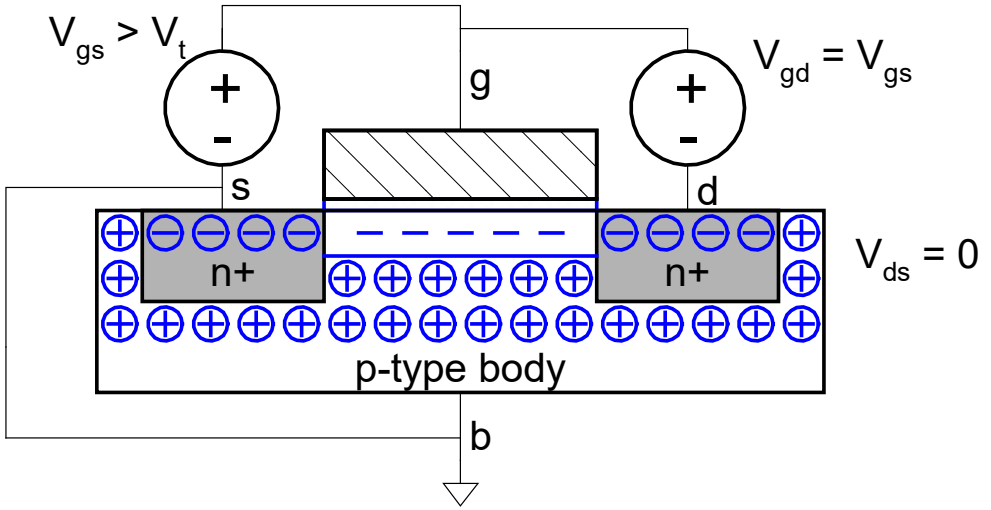


Fig. 2.3(a)

2.1. Introduction (5)

- Linear mode
  - When $V_{gs} > V_t$,
    we have an inversion channel.



  - By applying a positive V_{ds},
    we have $I_d > 0$.

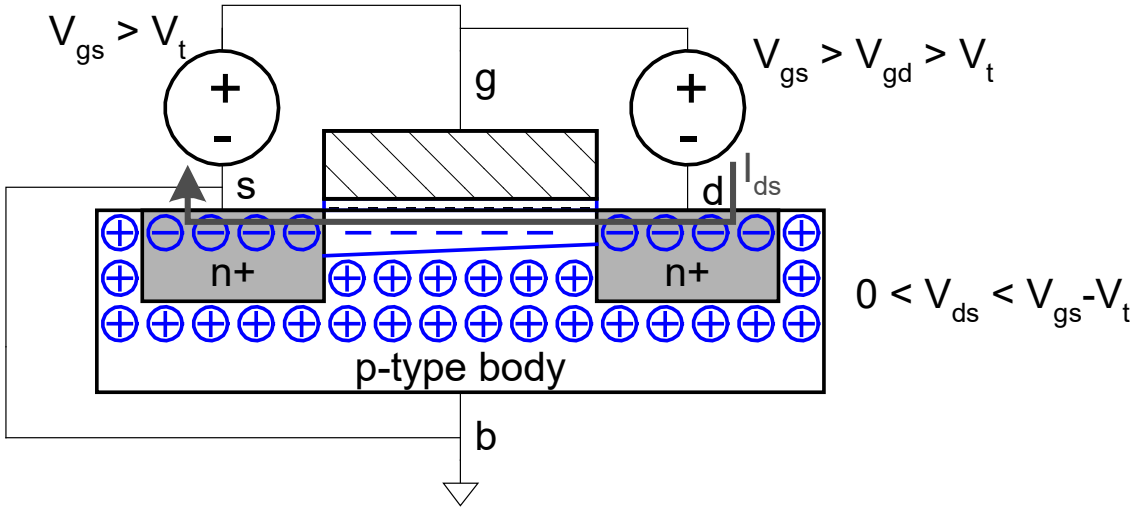


Fig. 2.3(b) & (c)

2.1. Introduction (6)

- Saturation
  - When $V_{ds} > V_{gs} - V_t$, the drain current is controlled only by the gate voltage and ceases to be influenced by the drain.

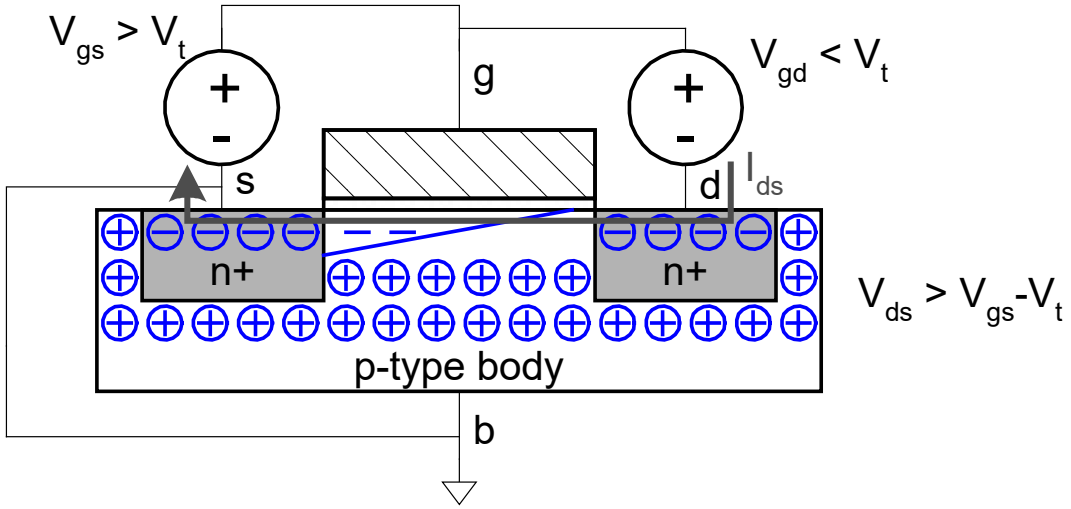


Fig. 2.3(d)

2.2 Long-channel IV

2.2. Long-channel IV (1)

- Current through the channel depends on
  - How much “electron” charge is in the channel?
  - How fast is the charge moving?
- Charge

$$Q_{channel} = C_g\left(V_{gc} - V_t\right)$$

  - Note) $Q_{channel}$ for electrons. (It should be negative, but in the above equation, it is understood.)

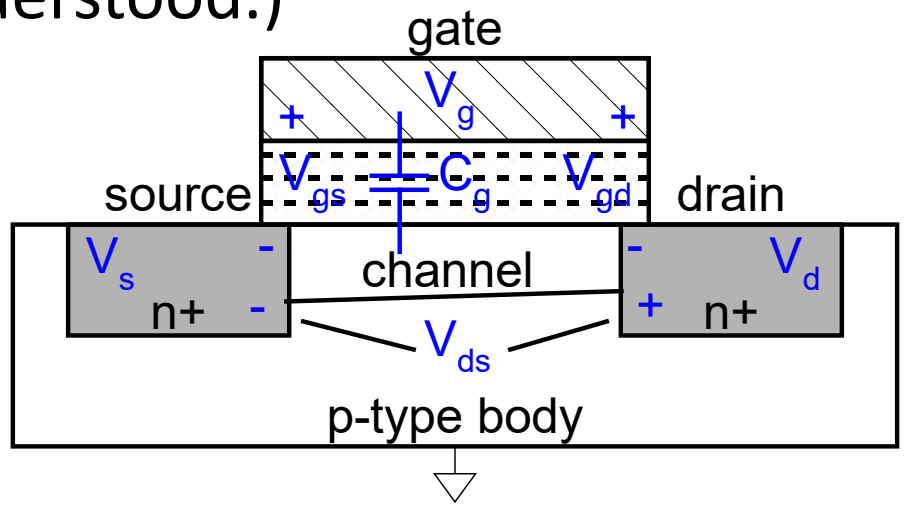


Fig. 2.5

2.2. Long-channel IV (2)

- Capacitance

$$C_g = C_{OX} W L$$

  - The "oxide capacitance," C_{OX}, is given as

$$C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$$

Calculate C_{OX} , when the effective oxide thickness is 1 nm.

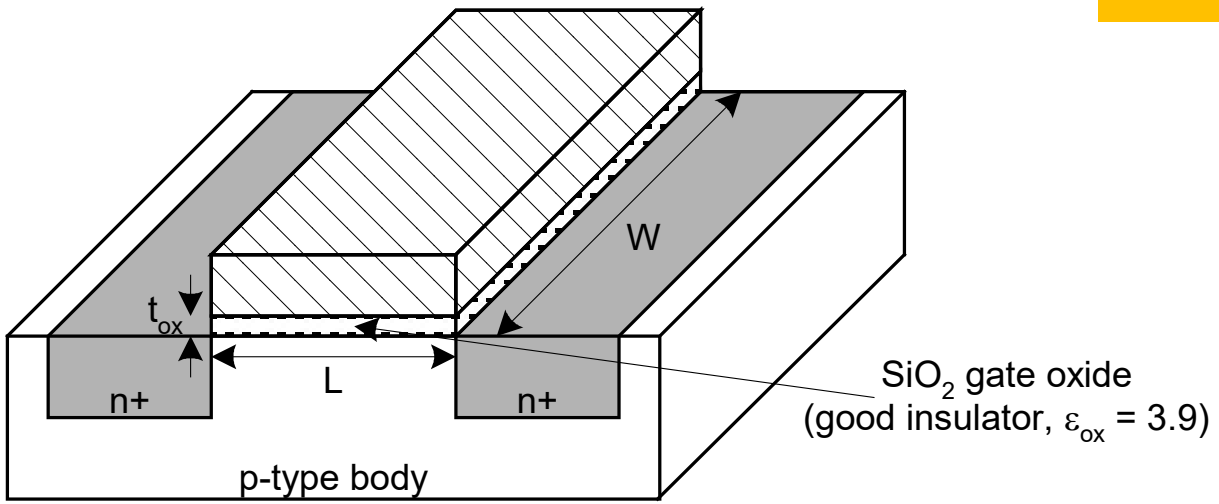


Fig. 2.6

2.2. Long-channel IV (3)

- IV characteristics
  - After some manipulation, we have

Subthreshold

$$I_d = 0$$

Linear

$$I_d = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$

Saturation

$$I_d = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

  - Here,

$$\beta = \mu_n C_{OX}\frac{W}{L}$$

Calculate I_d at $V_{gs} = V_{ds}$ = 1.0 V, when W/L = 2, t_{ox} = 1 nm, μ_n = 80 cm^2/V sec, and V_t is 0.3 V.

Thank you!