Digital Integrated Circuit
Lecture 10 Delay

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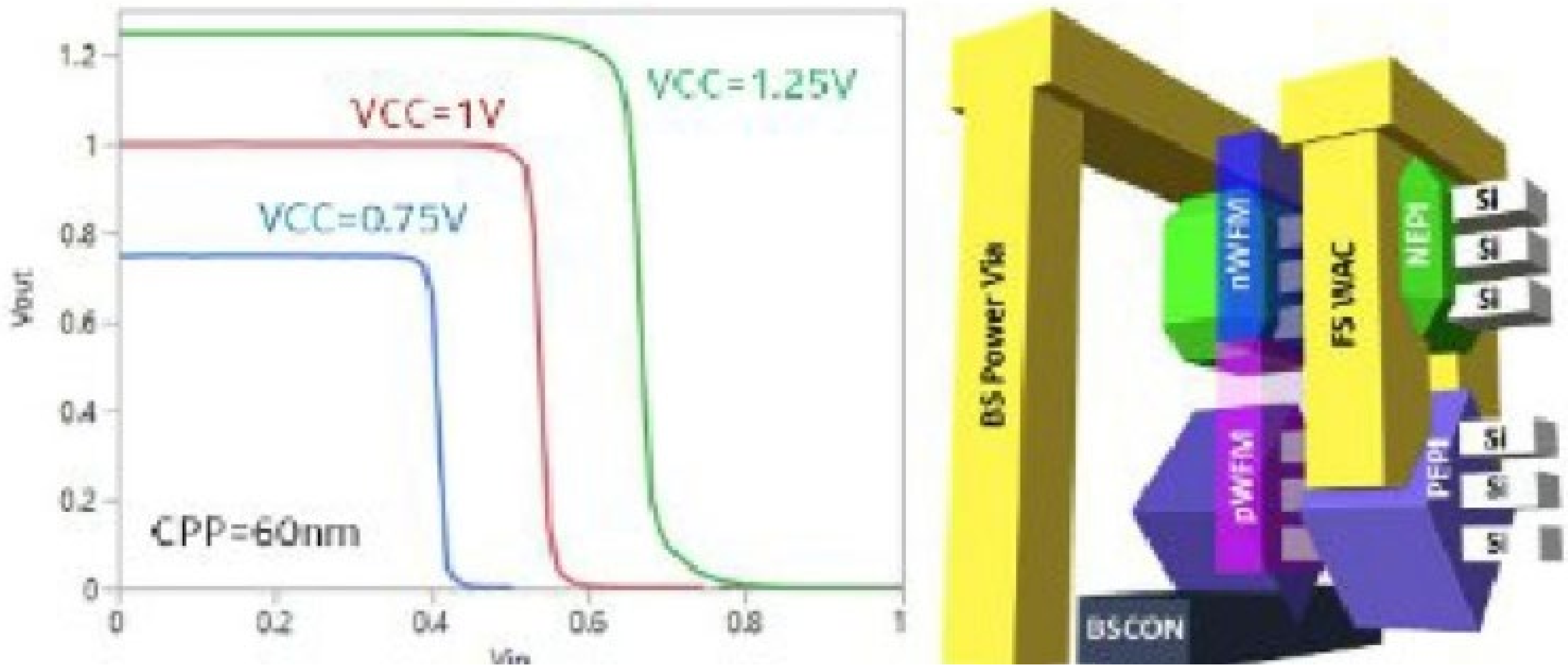
Review of Previous Lecture

Lecture 9

- CMOS inverter
  - Skewed due to the N/P mismatch



(Taken from IEDM 2023 press kit)

2.5 DC Transfer

2.5. DC transfer (9)

- Noise margin
  - Two unity gain points
  - Input voltage is V_{IL}.
  - Input voltage is V_{IH}.

  - In this case,
$NL_L = V_{IL}$
$NL_H = V_{DD} - V_{IH}$

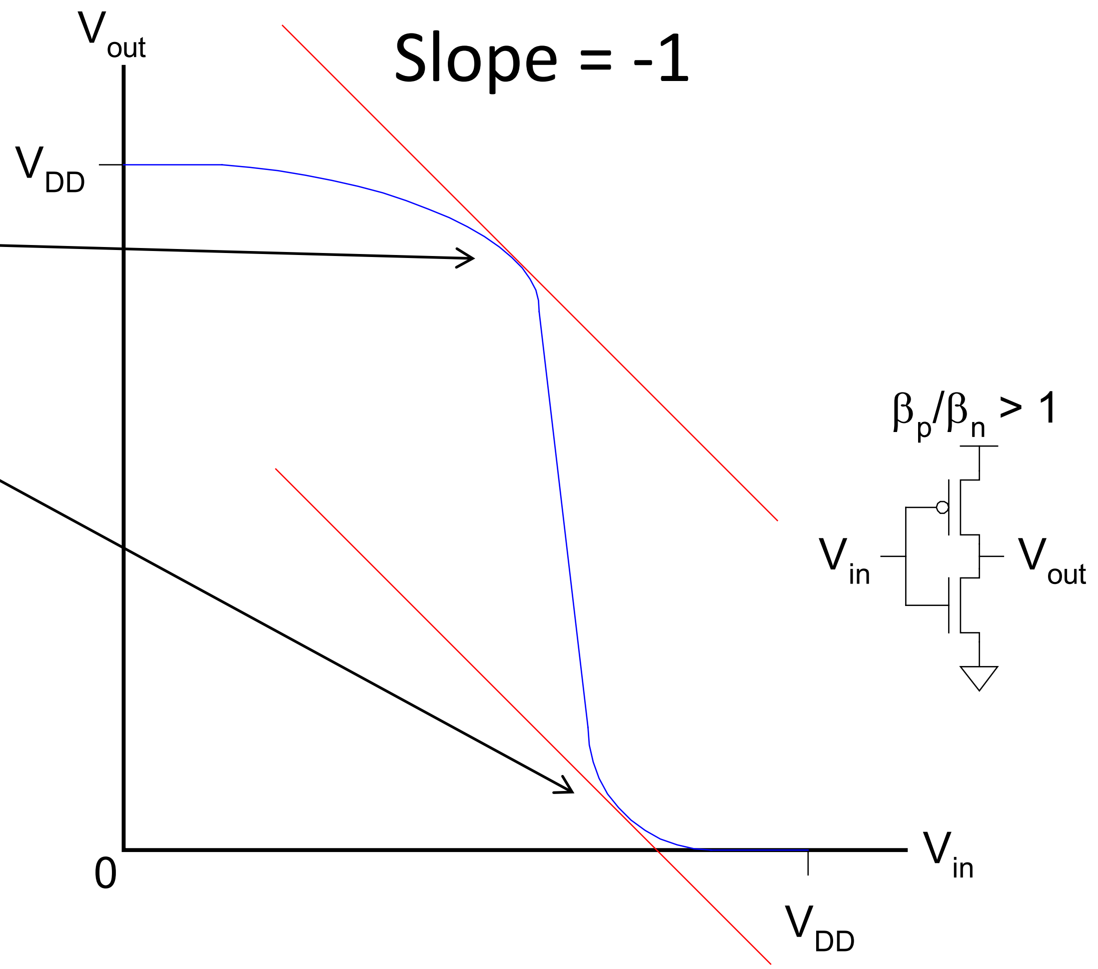


Fig. 2.30

Homework#3

- Due: AM08:00, October 10
- Problem#1
  - Calculate V_{IL} with the ideal IV characterstics. It can be found from a condition of $\frac{dV_{out}}{dV_{in}} = -1$. Neglect the channel length modulation. Assume $\mu_n C_{OX} \frac{W_n}{L_n} = \mu_p C_{OX} \frac{W_p}{L_p}$ and $V_{tn} = -V_{tp}$ for simplicity.
  - Hint: The NMOSFET is in the saturation mode, while the PMOSFET in the linear mode.

Homework#3

- Problem#2
  - Using the solution of Problem#1, calculate V_{IL} when V_{DD} is 1.8 V and V_{tn} is 0.5 V.

4.1 Introduction

4.1. Introduction (1)

- Transient response
  - DC analysis: V_{out} if V_{in} is a constant
  - Transisent analysis: $V_{out}(t)$ if $V_{in}(t)$ changes
  - A set of differential equations should be solved.
  - For a vector of state variable, $\mathbf{x}$,
$$\frac{d}{dt}(\mathbf{C}\,\mathbf{x}) + G(\mathbf{x}) = \mathbf{b}$$
  - Input is usually considered to be a step of ramp. (From 0 to V_{DD} or vice versa)

4.1. Introduction (2)

- Definitions
  - $\mathbf{t_{pdr}}$: *rising propagation delay*
    From input to rising output crossing $V_{DD}/2$
  - $\mathbf{t_{pdf}}$: *falling propagation delay*
    From input to falling output crossing $V_{DD}/2$
  - $\mathbf{t_{pd}}$: *average propagation delay*
    $t_{pd} = (t_{pdr} + t_{pdf})/2$
  - $\mathbf{t_r}$: *rise time*
    From output crossing 0.2 V_{DD} to 0.8 V_{DD}
  - $\mathbf{t_f}$: *fall time*
    From output crossing 0.8 V_{DD} to 0.2 V_{DD}

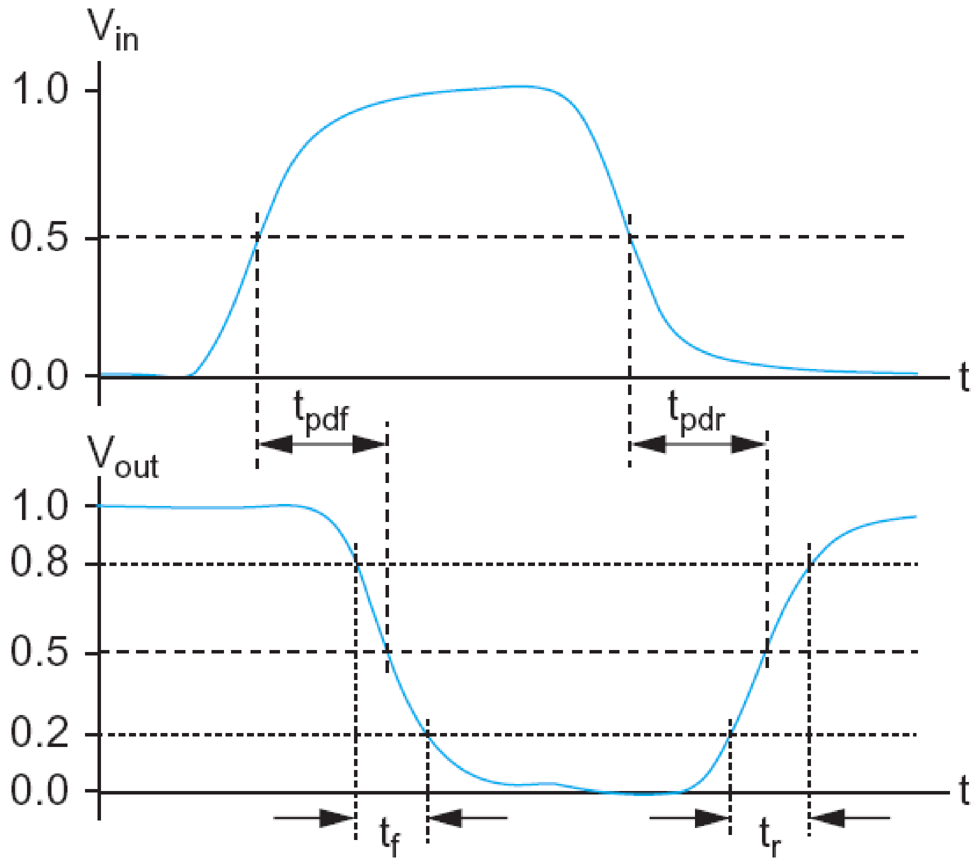
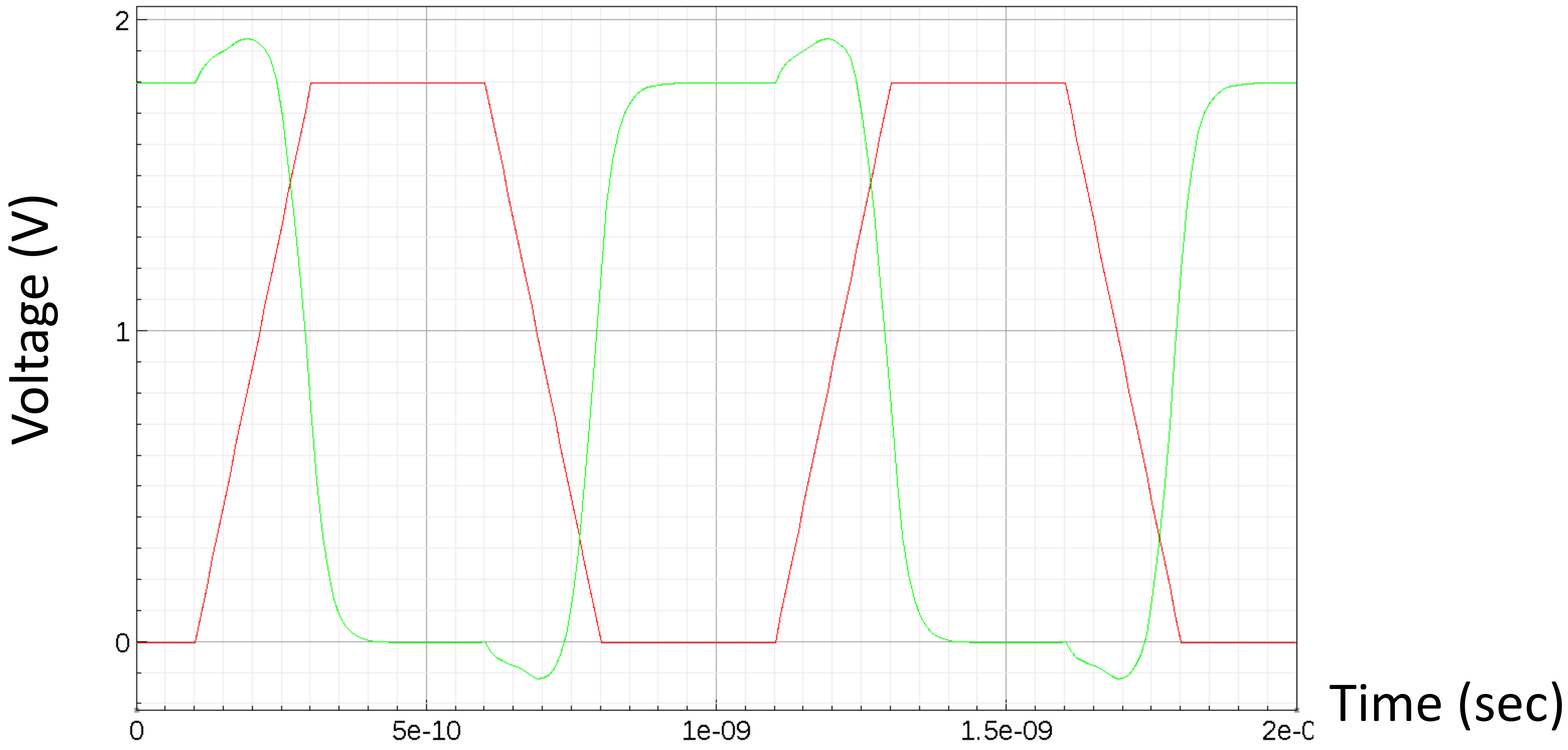


Fig. 4.1

4.2. Transient response (1)

- Example of an inverter (V_{DD} = 1.8 V)



4.2. Transient response (2)

- Consider the response of the inverter to a step input.
  - Initially, V_{in} = 0 V and $V_{out} = V_{DD}$.
  - With a sudden turn-on, $V_{in} = V_{DD}$. The PMOSFET is turned off.

$$C_{out}\frac{dV_{out}}{dt} = -I_{dn}$$

  - For saturation,

$$I_{dn} = \frac{\beta}{2}(V_{DD} - V_t)^2$$

It is a constant.

  - For linear,

$$I_{dn} = \beta\left(V_{DD} - V_t - \frac{V_{out}}{2}\right)V_{out}$$

Homework#3

- Problem#3
  - Draw the response of the inverter to a step input. (LOW➔HIGH) For the NMOSFET, W is 1 um and L is 50 nm. Its oxide thickness is 10.5 Å and the mobility is 80 cm^2/V sec. The output capacitance is 20 fF. V_{DD} is 1.0 V and V_{tn} is 0.3 V.
  - (You may use the computer to draw the curve accurately.)
- Problem#4
  - In Problem#3, estimate the rising propagation delay.

Thank you!