Digital Integrated Circuit
Lecture 15 Power

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Review of Mid-Term Examination

Problem 5

- Derive $V_{out}(V_{in})$ of a CMOS inverter, when both transistors are in the saturation mode.
  - We must have $I_{dn} + I_{dp} = 0$.
  - Then, we have a lengthy expression.

Problem 6

- Derive V_{inv} of a CMOS inverter
  - It was covered in our lecture.
  - When $r = \frac{\beta_p}{\beta_n}$,

$$V_{inv} = \frac{V_{DD} + V_{tp} + \frac{1}{\sqrt{r}} V_{tn}}{1 + \frac{1}{\sqrt{r}}}$$

Problem 8

- What is n for the subthreshold slope of 100 mV/dec?
  - We can find that

$$\exp \frac{100\ \text{mV}}{nV_T} = 10$$

  - From the above relation,

$$nV_T = \frac{100\ \text{mV}}{\log 10}$$

Problem 9

- Important properties of CMOS inverters
  - The HIGH and LOW output levels equal V_{DD} and GND, respectively.
  - The logic levels are not dependent upon the relative device sizes, so that the transistors can be minimum size. (Ratioless)
  - A well-designed CMOS inverter has a low output impedance.
  - The input resistance of the CMOS inverter is extremely high.
  - The absence of current flow between V_{DD} and GND means that the logic gate does not consume any static power.

Problem 10

- When the input voltage is 0 V, only the PMOSFET is turned on.
  - The PMOSFET is in its linear mode.

Problem 11

- The minimum effort delay is $4\sqrt[4]{\frac{40}{9}}$.
  - Then, what are x, y, and z?

5.1 Introduction

5.1. Introduction (1)

- Definitions
  - Instanteneous power

$$P(t) = I(t)V(t)$$

  - Energy

$$E = \int_0^T P(t)dt$$

  - Average power

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt$$

5.1. Introduction (2)

- Charging a capacitor
  - Energy stored in the capacitor

$$\int_0^\infty I(t)V_{out}(t)dt = \frac{1}{2}C_L V_{DD}^2$$

  - Energy delivered from the power supply

$$\int_0^\infty I(t)V_{DD}dt = C_L V_{DD}^2$$

  - Half of the energy from V_{DD} is dissipated in the PMOS transistor as heat.

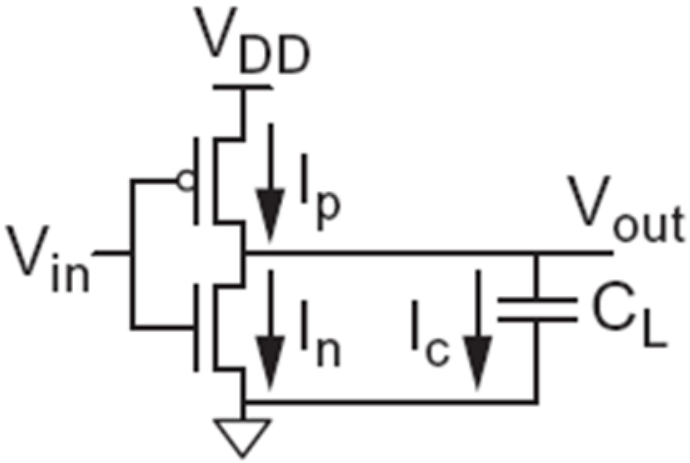

Fig. 5.4

5.1. Introduction (3)

- Switching waveforms

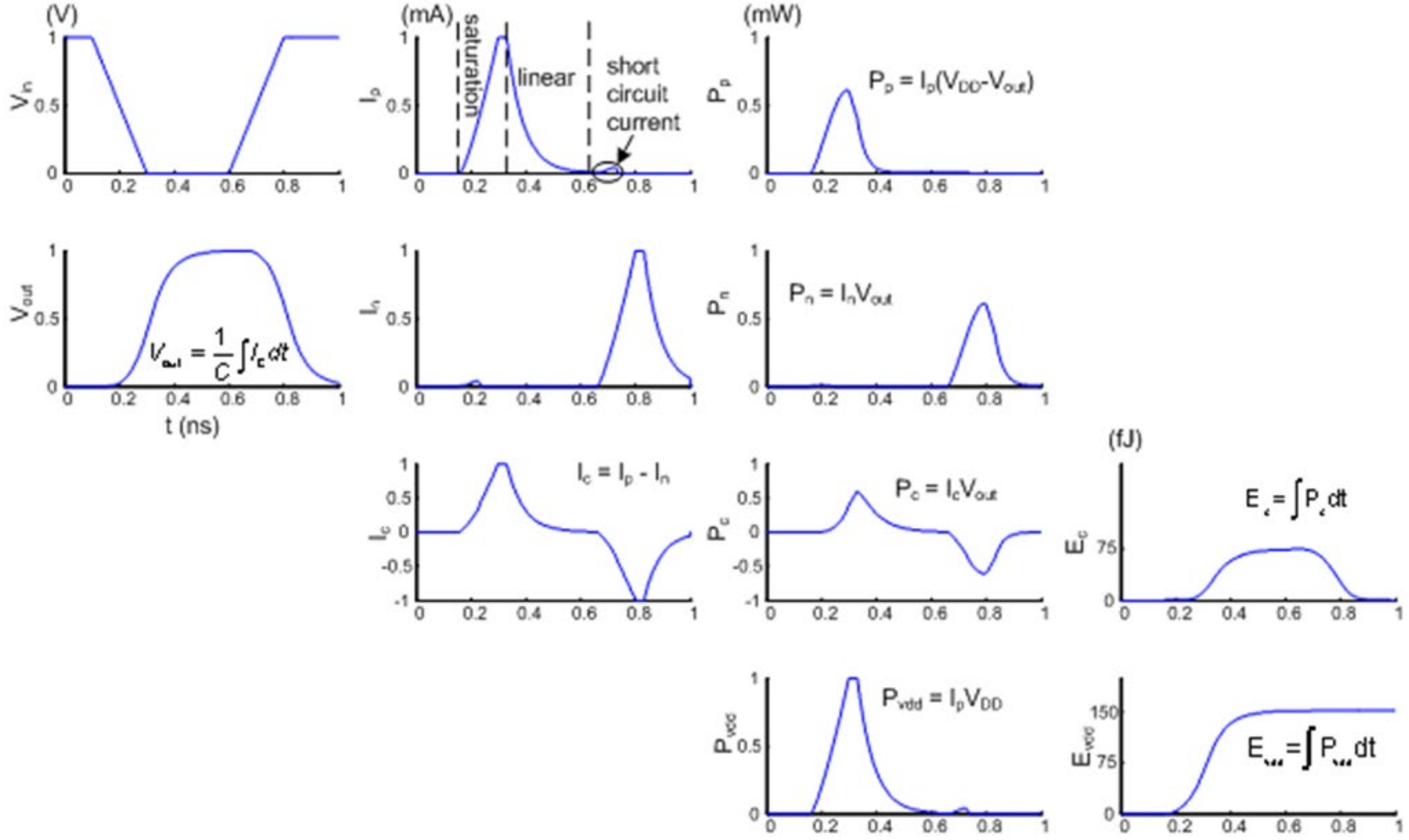

Fig. 5.5

5.1. Introduction (4)

- Average power dissipation
  - When a gate is switched with a switching frequency of f_{sw},

$$P_{switching} = \frac{CV_{DD}^2}{T} = CV_{DD}^2 f_{sw}$$

- Most gates do not switch every clock cycle.
  - Let $f_{sw} = \alpha f$, where α is the activity factor.
  - Then, the dynamic power is written as

$$P_{switching} = \alpha CV_{DD}^2 f$$

5.1. Introduction (5)

- Power dissipation sources

$$P_{total} = P_{dynamic} + P_{static}$$

  - Dynamic power

$$P_{dynamic} = P_{switching} + P_{shortcircuit}$$

  - Static power

$$P_{static} = \left(I_{sub} + I_{gate} + I_{junct} + I_{contention}\right)V_{DD}$$

Thank you!