# Digital Integrated Circuit
# Lecture 2 Introduction

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# Review of Previous Lecture

# Lecture 1

- MOS transistors
  - Its structure: Gate, source, drain and body(/substrate)
  - Controlling the number of charge carriers by using the field effect.
  - (NMOSFET) When $V_{GS} < V_{TH}$, no electron in the channel region
  - (NMOSFET) When $V_{GS} > V_{TH}$, electron density increases linearly with $V_{GS} - V_{TH}$.
  - PMOSFET

# 1.4 CMOS Logic

# 1.4. CMOS logic (1)

- CMOS inverter
  - When the input $A$ is 0, the NMOS transistor is OFF and the PMOS transistor is ON.
  - Thus, the output $Y$ is pulled up to 1.

| $\boldsymbol{A}$ | $\boldsymbol{Y = NOT\ A}$ |
|---|---|
| $0$ | $1$ |
| $1$ | $0$ |

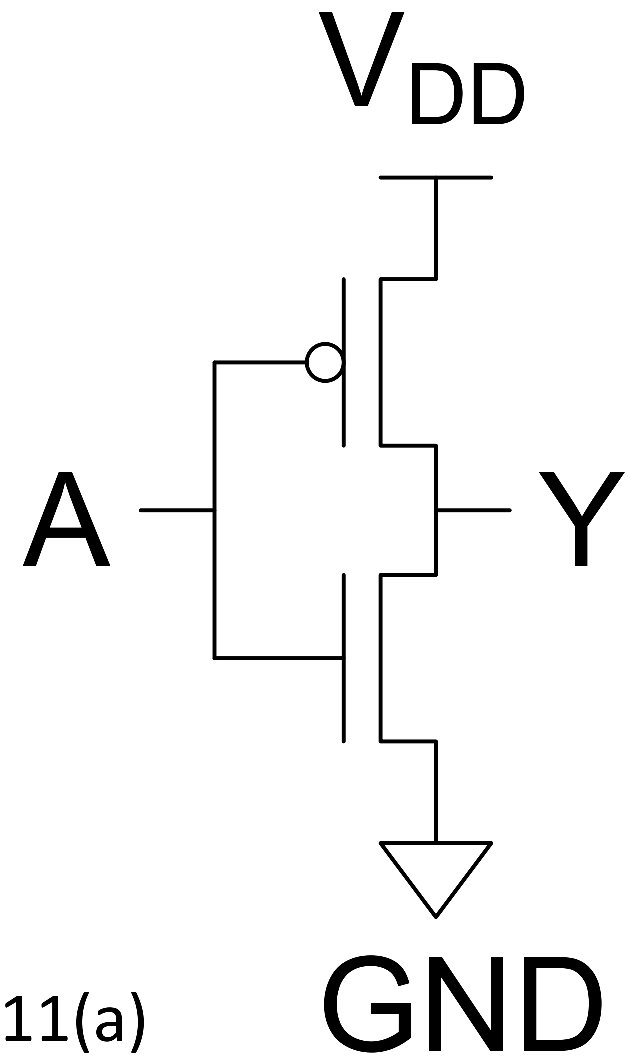


Fig. 1.11(a)

# 1.4. CMOS logic (2)

- CMOS NAND
  - If either input $A$ or $B$ is 0, at least one of the NMOSFETs will be OFF, breaking the path from $Y$ to GND.

| $\boldsymbol{A}$ | $\boldsymbol{B}$ | $\boldsymbol{Y = A}$ **NAND** $\boldsymbol{B}$ |
|---|---|---|
| $0$ | $0$ | $1$ |
| $0$ | $1$ | $1$ |
| $1$ | $0$ | $1$ |
| $1$ | $1$ | $0$ |

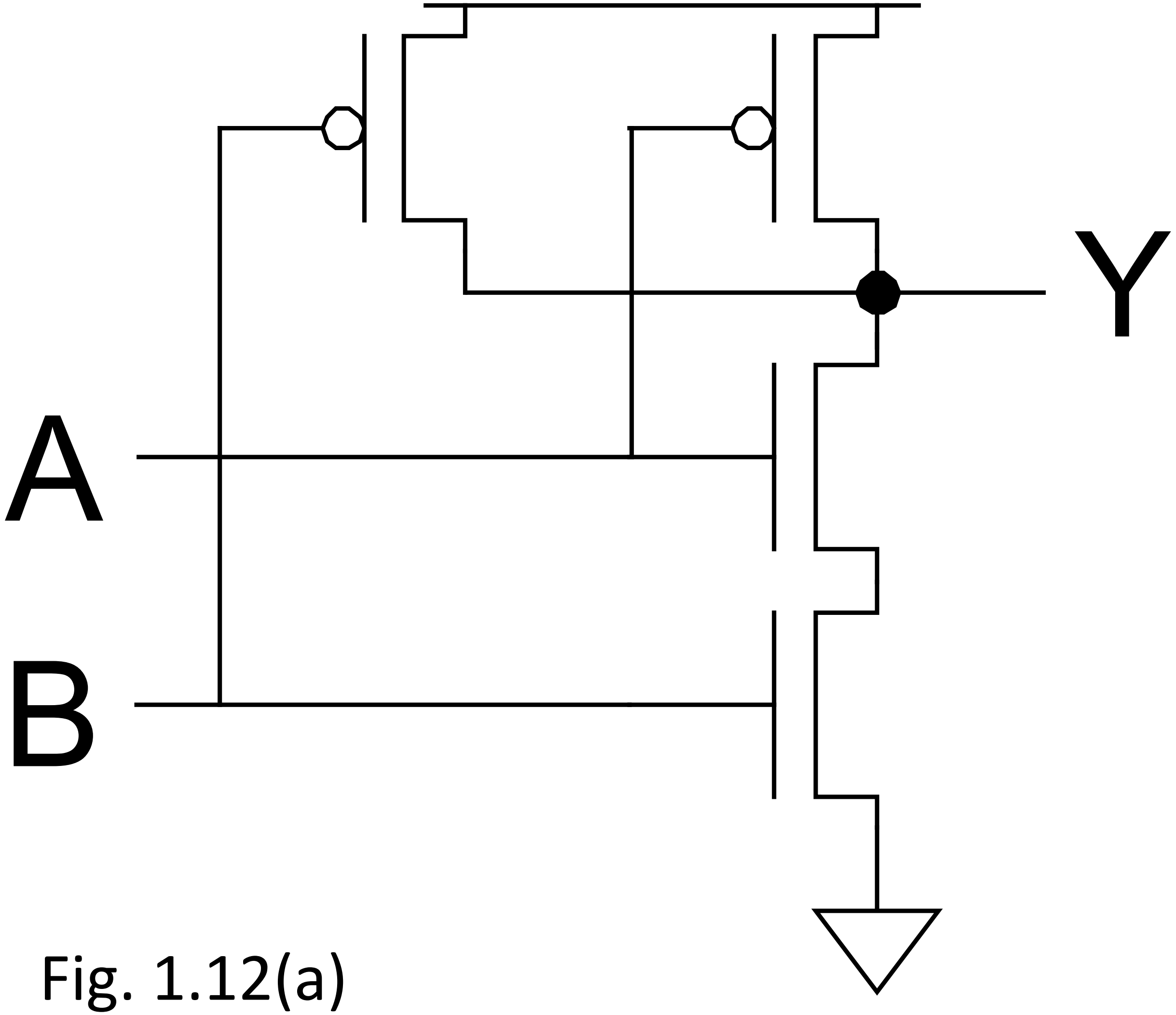


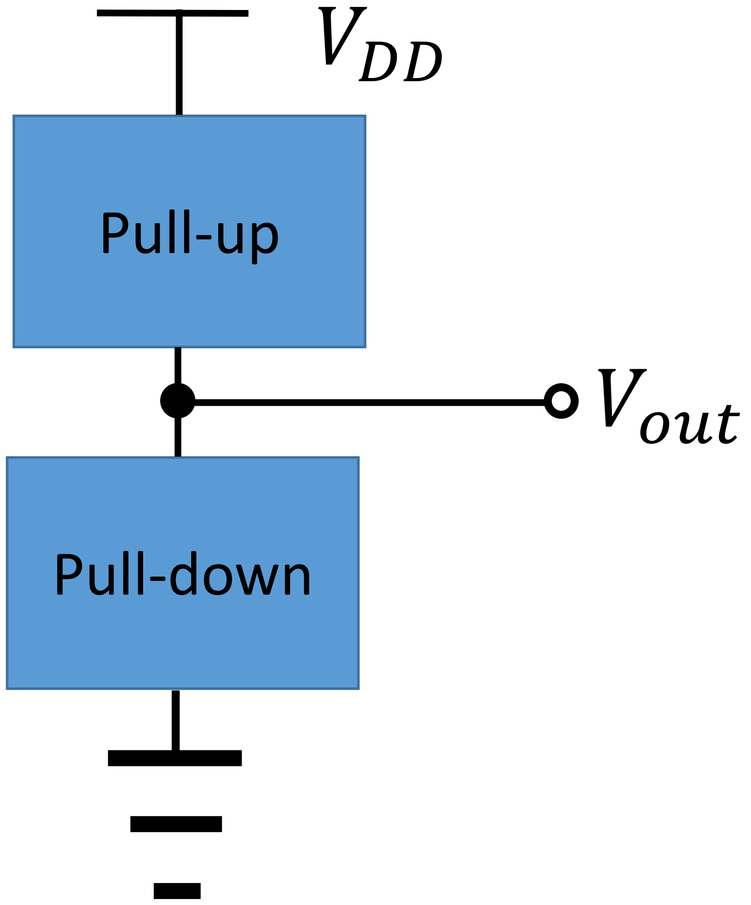
Fig. 1.12(a)

# 1.4. CMOS logic (3)

- Complementary CMOS gates
- Pull-down and pull-up networks
  - NMOS pull-down
  - PMOS pull-up

Floating

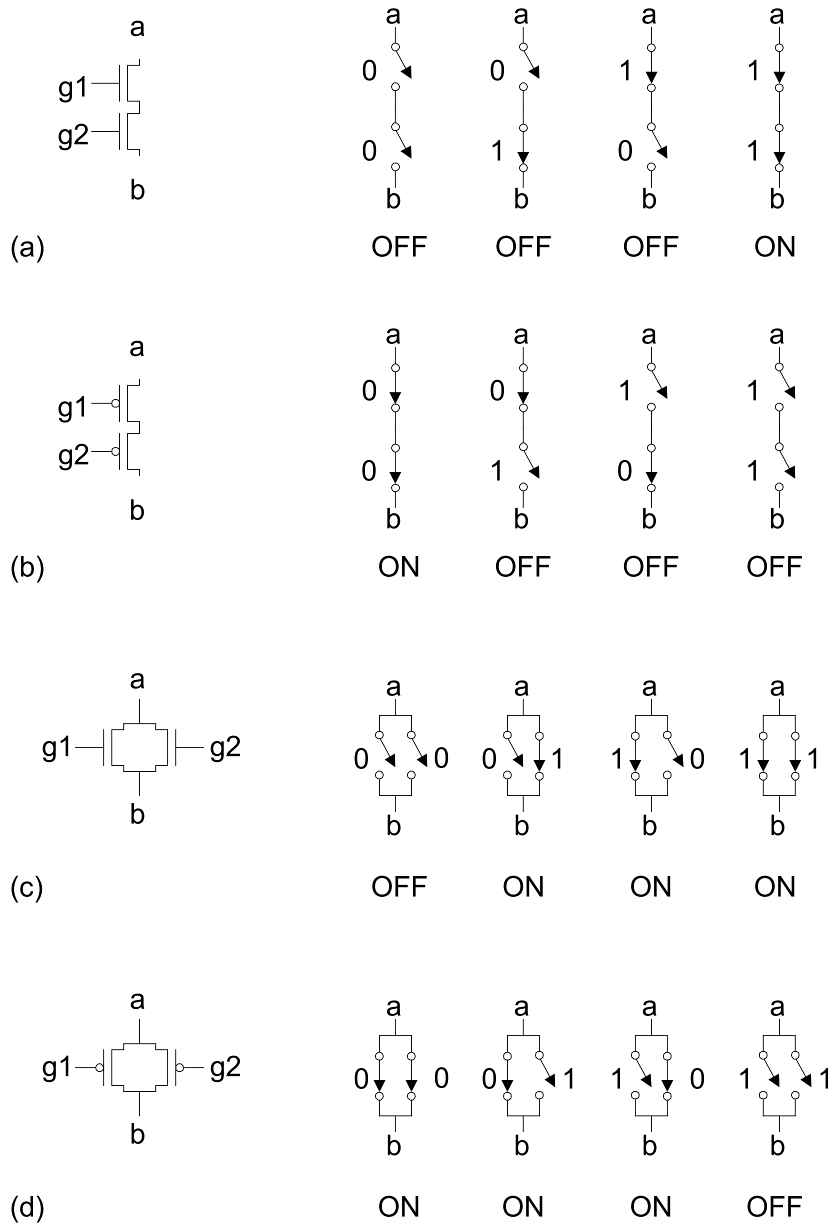
| | Pull-up OFF | Pull-up ON |
|---|---|---|
| Pull-down OFF | Z | 1 |
| Pull-down ON | 0 | Crowbarred (X) |



# 1.4. CMOS logic (4)

- Series and parallel
  - NMOS: 1 = ON
  - PMOS: 0 = ON
  - Series: Both must be ON.
  - Parallel: Either can be ON.
- Conduction complements
  - Pull-up 🡸🡺 pull-down

Fig. 1.15



# 1.4. CMOS logic (5)

- CMOS NOR

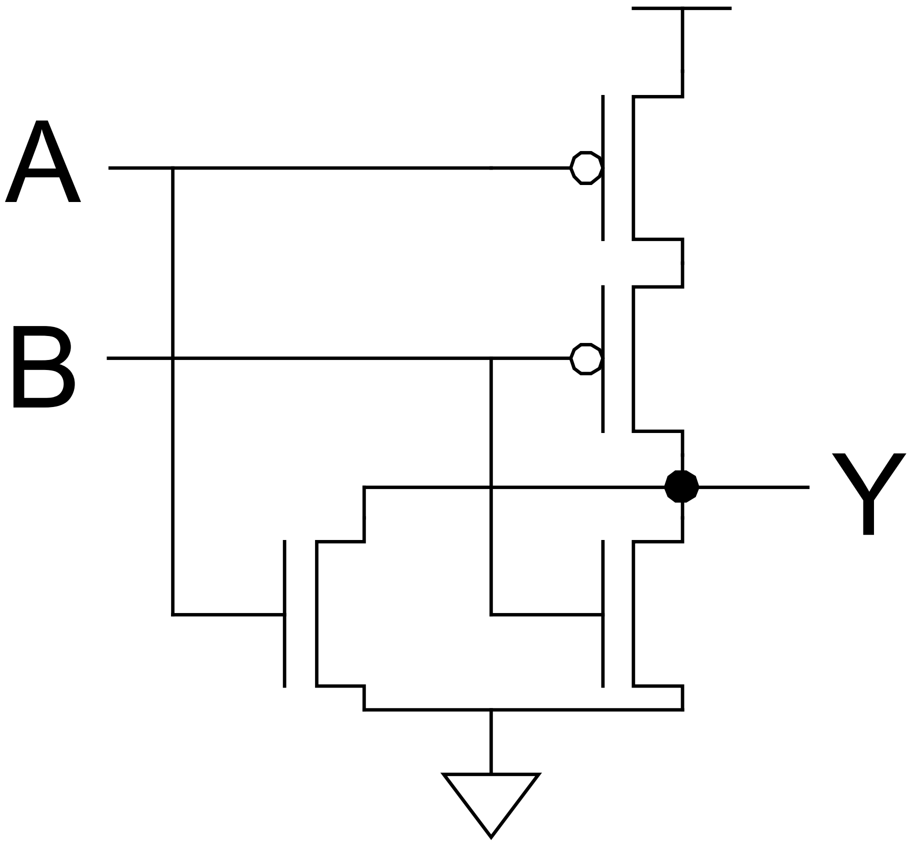


Fig. 1.16(a)

- Example 1.1
  - Sketch a 3-input CMOS NOR gate.

# 1.4. CMOS logic (6)

- Compound gates
  - A more complex logic function in a single stage of logic
  - Consider $Y = \overline{(A \cdot B) + (C \cdot D)}$, AND-OR-INVERT-22 (AOI22).

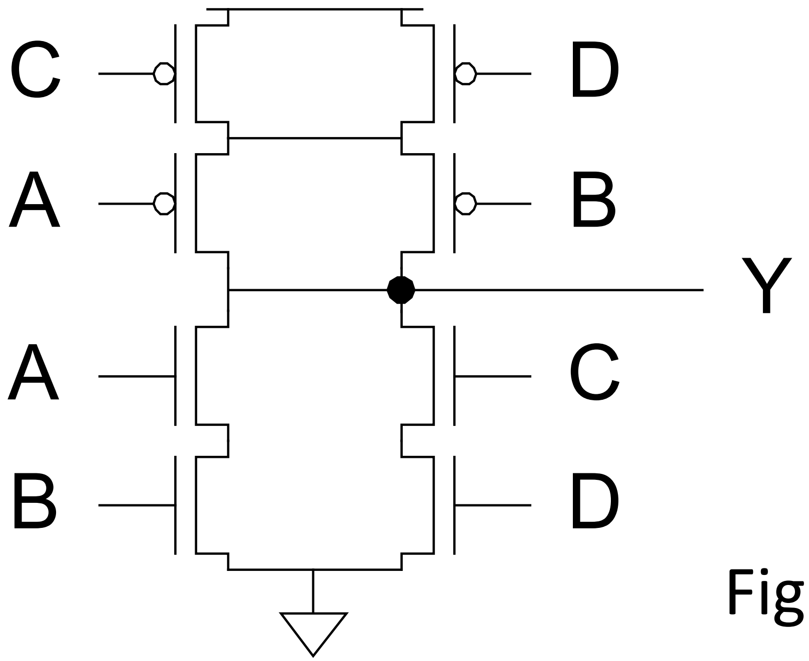


Fig. 1.18(e)

# 1.4. CMOS logic (7)

- Example 1.2
  - Sketch a static CMOS gate computing $Y = \overline{(A + B + C) \cdot D}$.

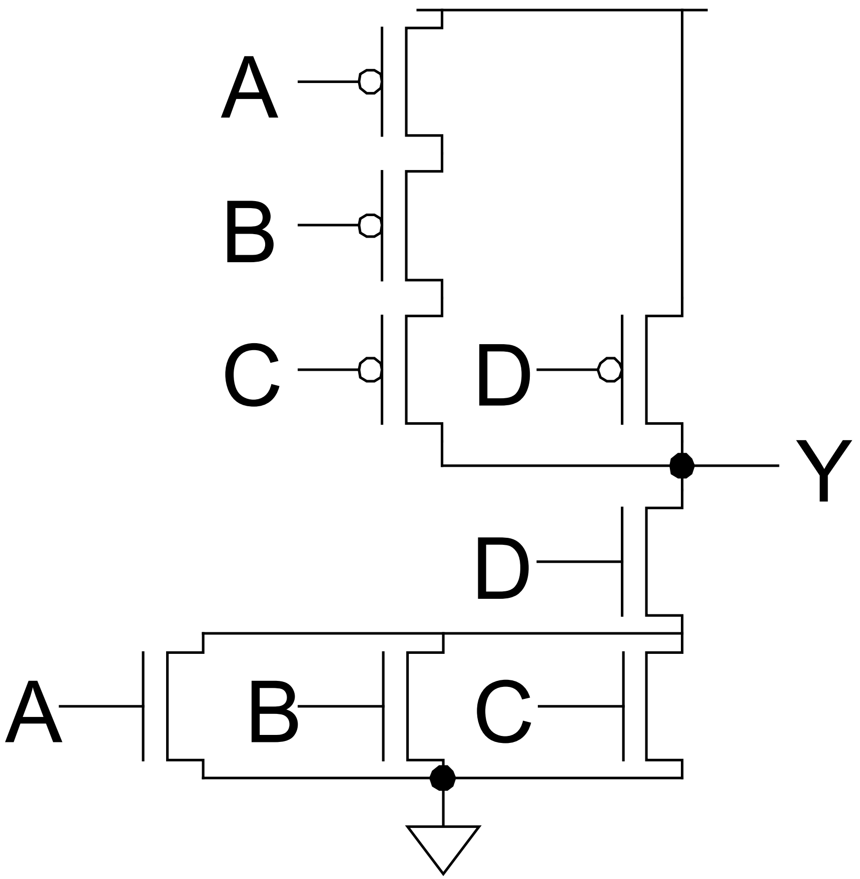


Fig. 1.19

# 1.4. CMOS logic (8)

- Pass transistors
  - Transistors can be used as switches.
  - Pass transistors may produce degraded (weak) outputs.

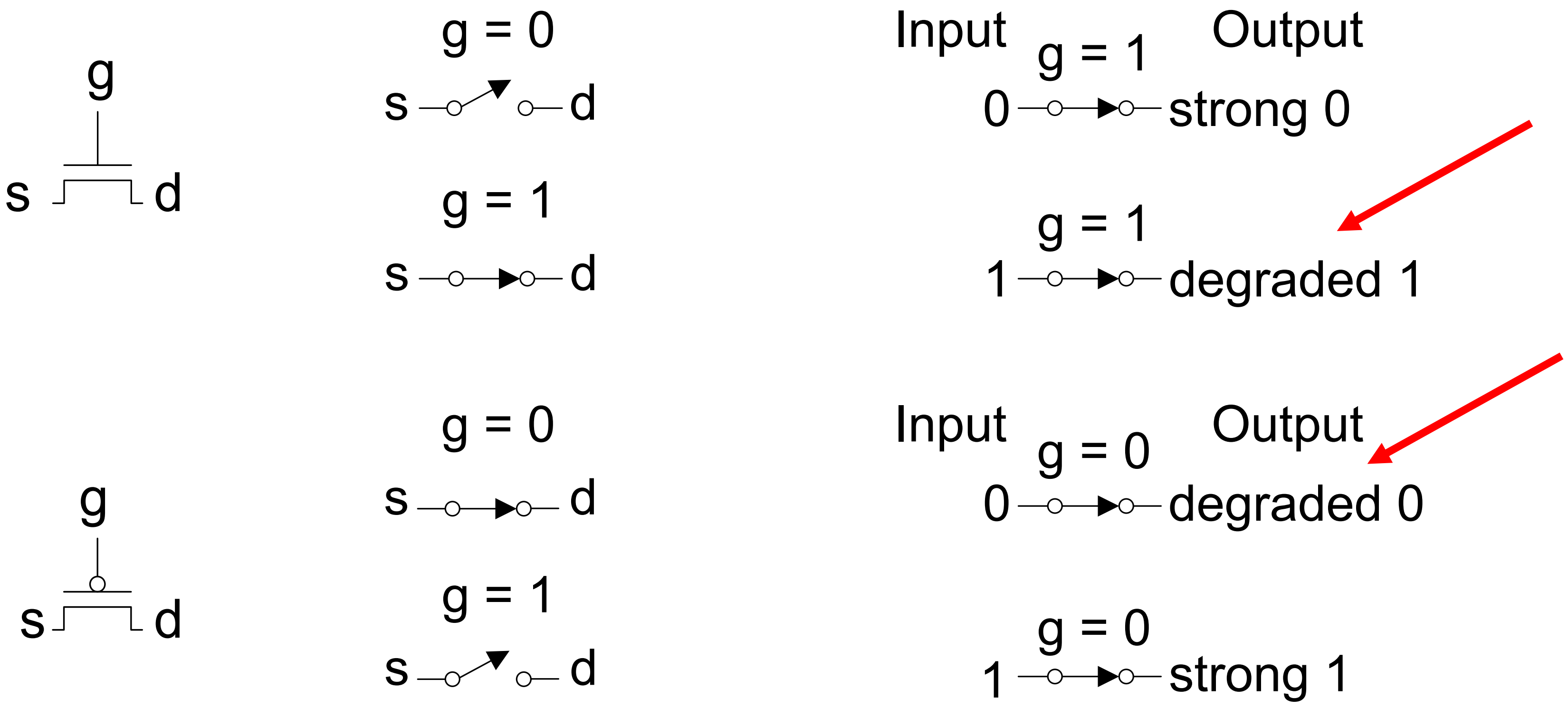


Fig. 1.20

# 1.4. CMOS logic (9)

- Transmission gate
  - By combining an NMOS and a PMOS transistor in parallel, we obtain a switch that passes both 0 and 1 well. (Transmission gate)

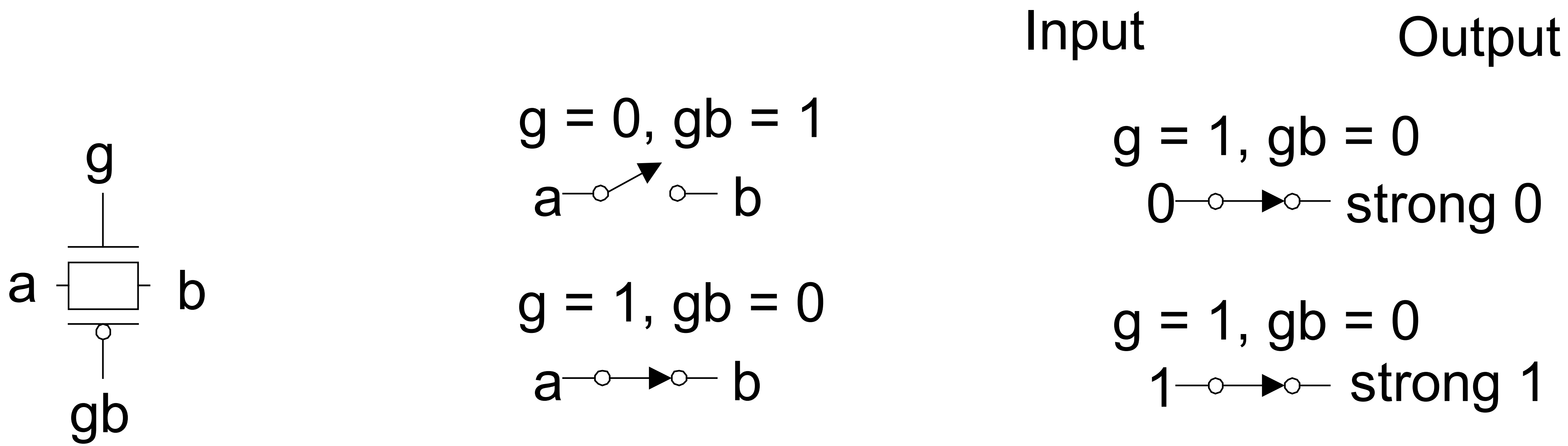


Fig. 1.21

# 1.4. CMOS logic (10)

- Tristates (0, 1, and Z)
  - Tristate buffer produces Z when not enabled
  - Transmission gate acts as a tristate buffer.
  - But, it is nonrestoring.

| EN | A | Y |
|---|---|---|
| 0 | 0 | Z |
| 0 | 1 | Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Truth table of a tristate buffer

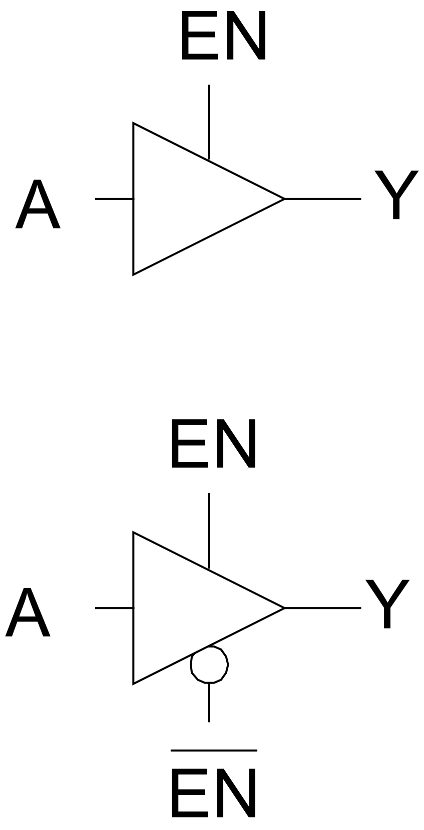
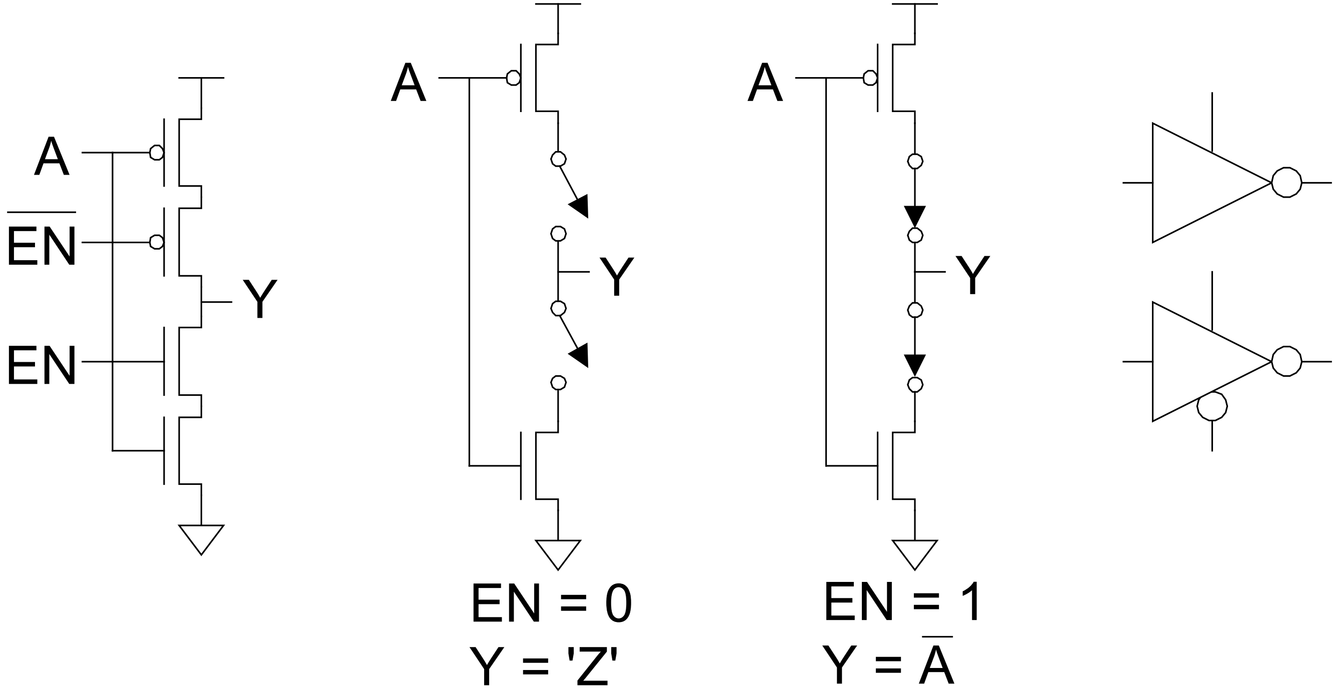


Fig. 1.25

# 1.4. CMOS logic (11)

- Tristate inverter
  - It produces a restored output.
  - It violates the conduction complements rule. (Why?)



EN = 0
Y = 'Z'

EN = 1
Y = $\overline{A}$

Fig. 1.27

# 1.4. CMOS logic (12)

- Multiplexers (muxes)
  - It chooses the output from several inputs based on a select signal.

| S | D1 | D0 | Y |
|---|---|---|---|
| 0 | X | 0 | 0 |
| 0 | X | 1 | 1 |
| 1 | 0 | X | 0 |
| 1 | 1 | X | 1 |

Truth table of a 2:1 multiplexer

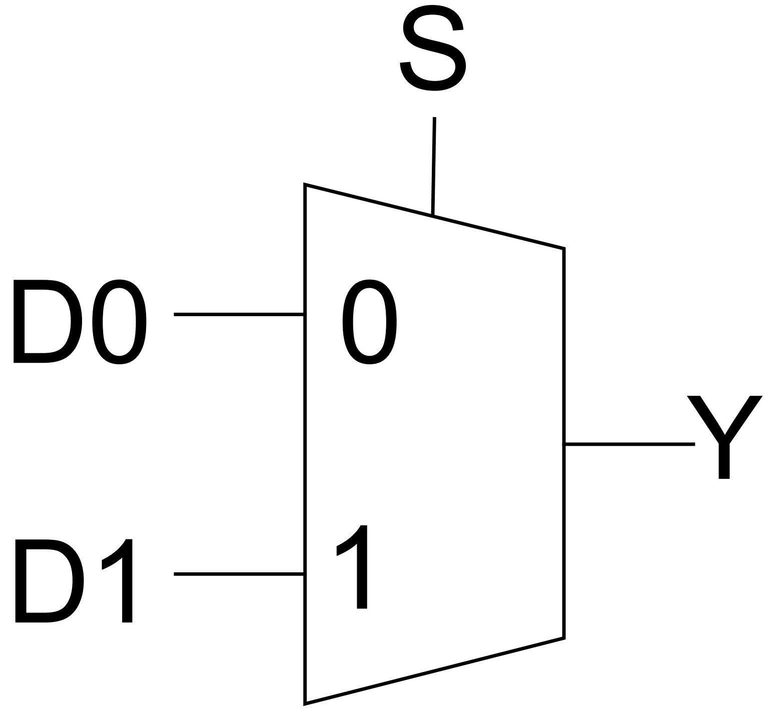


Fig. 1.28(b)

# 1.4. CMOS logic (13)

- Implementation
  - Using transmission gates (nonrestoring)
  - Using tristate inverters (inverting)

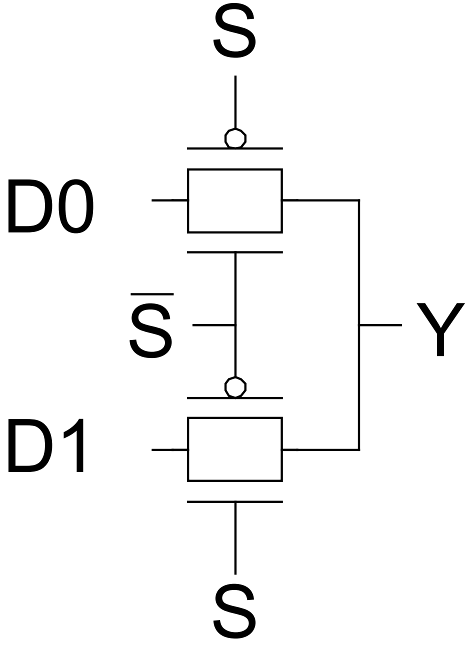


Fig. 1.28(a)

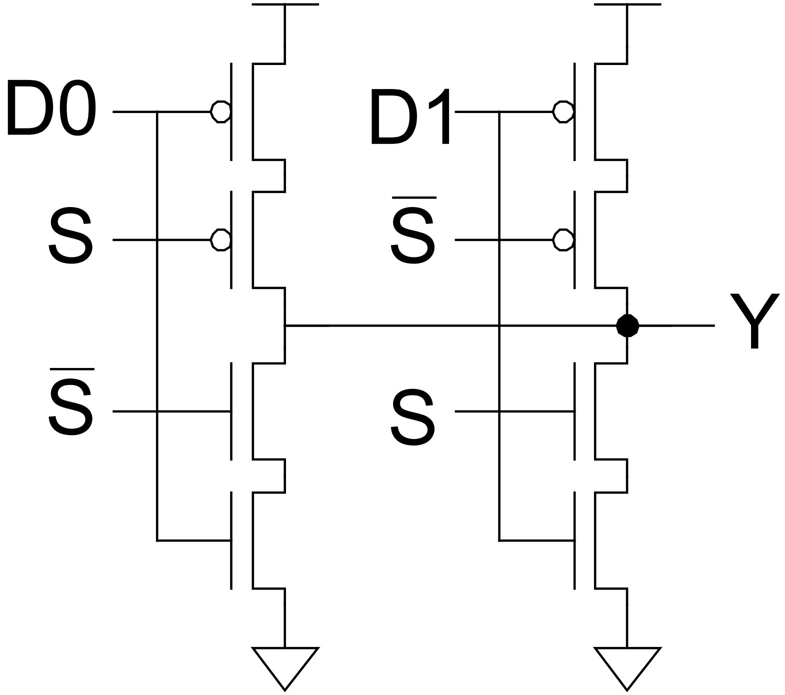


Fig. 1.29(b)

# 1.4. CMOS logic (14)

- Larger multiplexers
  - Example) 4:1 multiplexer
  - Two levels of 2:1 muxes
  - Or four tristates

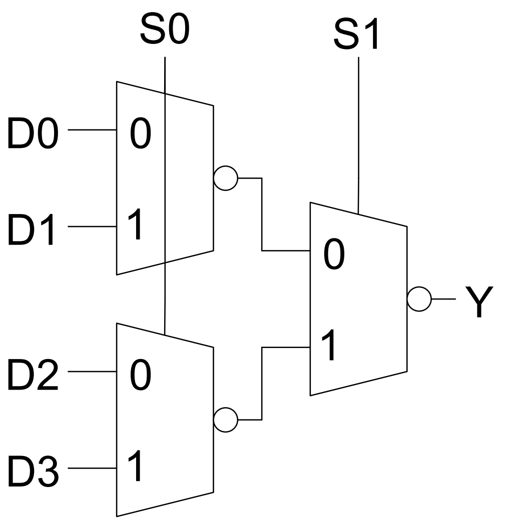
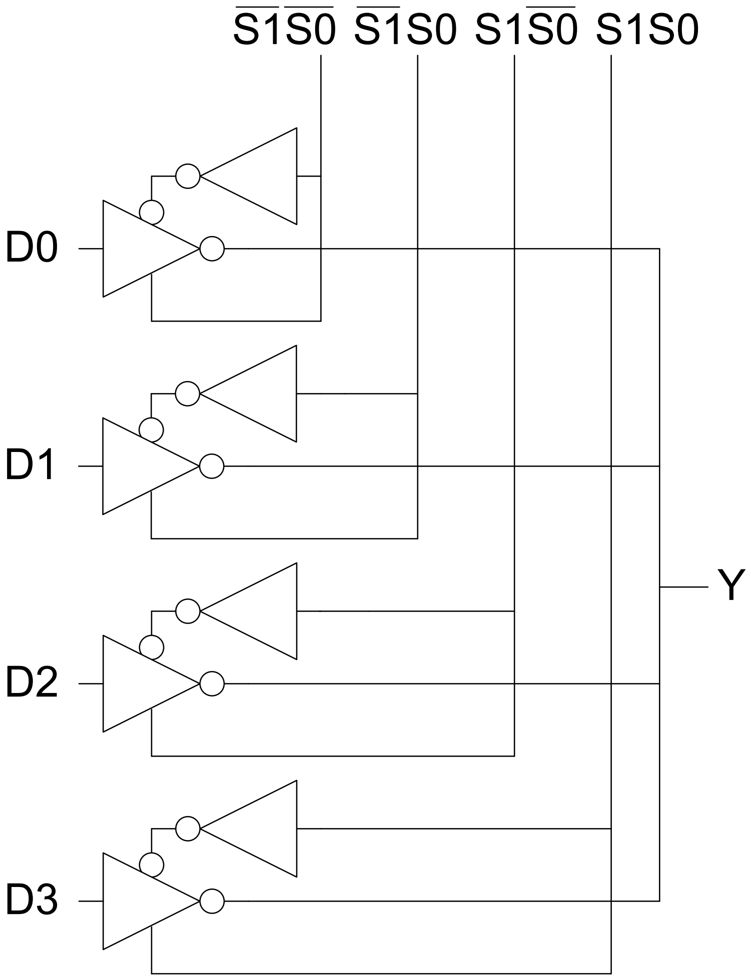


Fig. 1.30


$\overline{S1}\,\overline{S0}$ $\overline{S1}S0$ $S1\overline{S0}$ S1S0
D0
D1
D2
D3
Y

# Thank you!