Digital Integrated Circuit
Lecture 23 Combinational Circuit Design

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Review of Previous Lecture

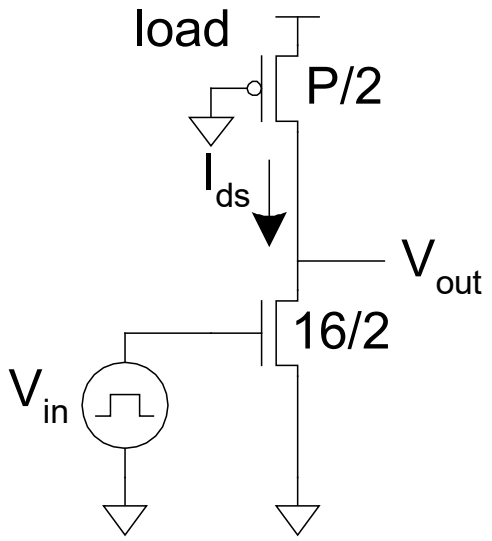
Lecture 22

- Static CMOS
  - Any logical function can be implemented with NAND/NOR/NOT gates.
  - Compound gates
  - By sizing transistors, t_{pdf} and t_{pdr} can be affected. (But, a benefit always comes with a cost.)

9.2 Circuit Families

9.2. Circuit families (10)

- Pseudo-NMOS
  - The static load is built from a single PMOS that has its gate grounded. (It is always ON.)
  - Voltage transfer curve affected by P.
  - Static DC current…



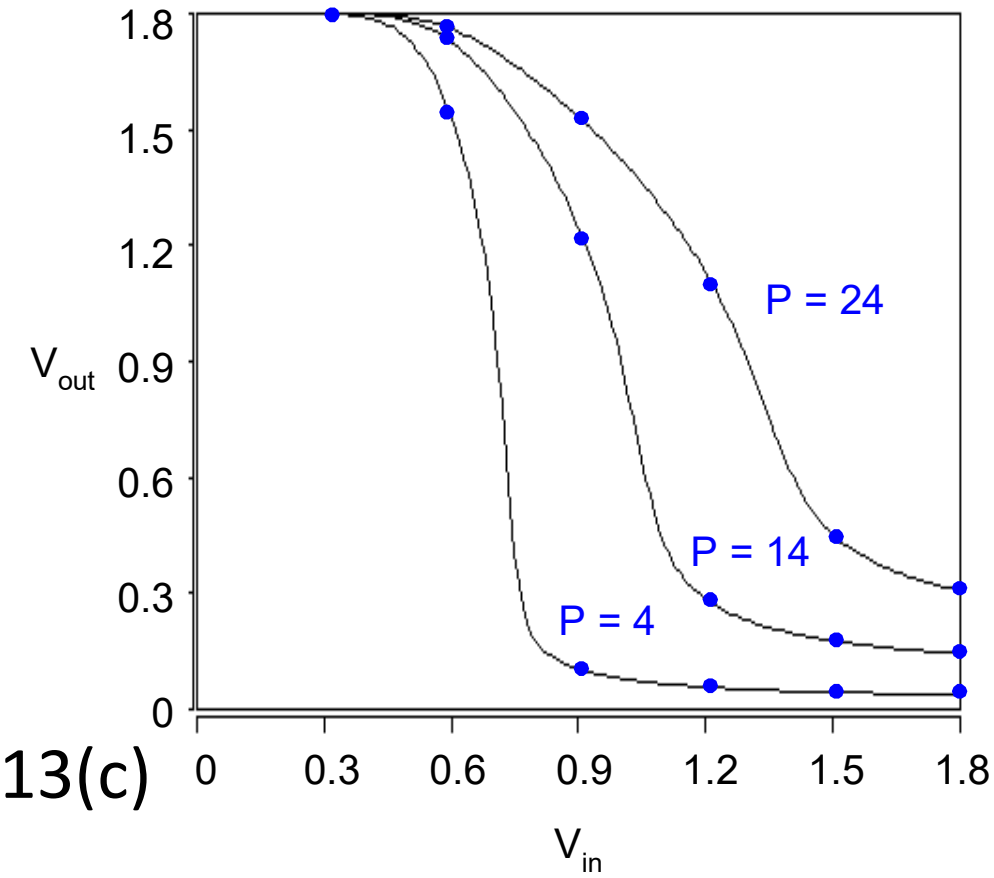
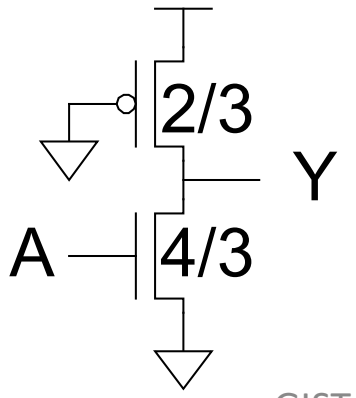


Fig. 9.13(c)

9.2. Circuit families (11)

- Compare the inverter design. (PMOS is 4 times weaker tha NMOS.)
  - In the (output) falling transition, the following inverter drives the same current with the unit inverter. (*Why?*)
  - Certainly, it is faster for the falling transition.
  - On the other hand, it is slower for the rising transition.



$g_u = 4/3$
$g_d = 4/9$
$g_{avg} = 8/9$
$p_u = 6/3$
$p_d = 6/9$
$p_{avg} = 12/9$

9.2. Circuit families (12)

- Comments on ratioed circuits
  - They reduce the input capacitance by replacing the PMOS transistors connected to the input with a single resistive pullup.
  - Drawbacks:
  - Slow rising transitions
  - Contention on the falling transitions
  - Static power dissipation
  - Nonzero V_{OL}

9.2. Circuit families (13)

- Dynamic gates use a clocked PMOS pullup.
- Two modes: *precharge* and *evaluate*

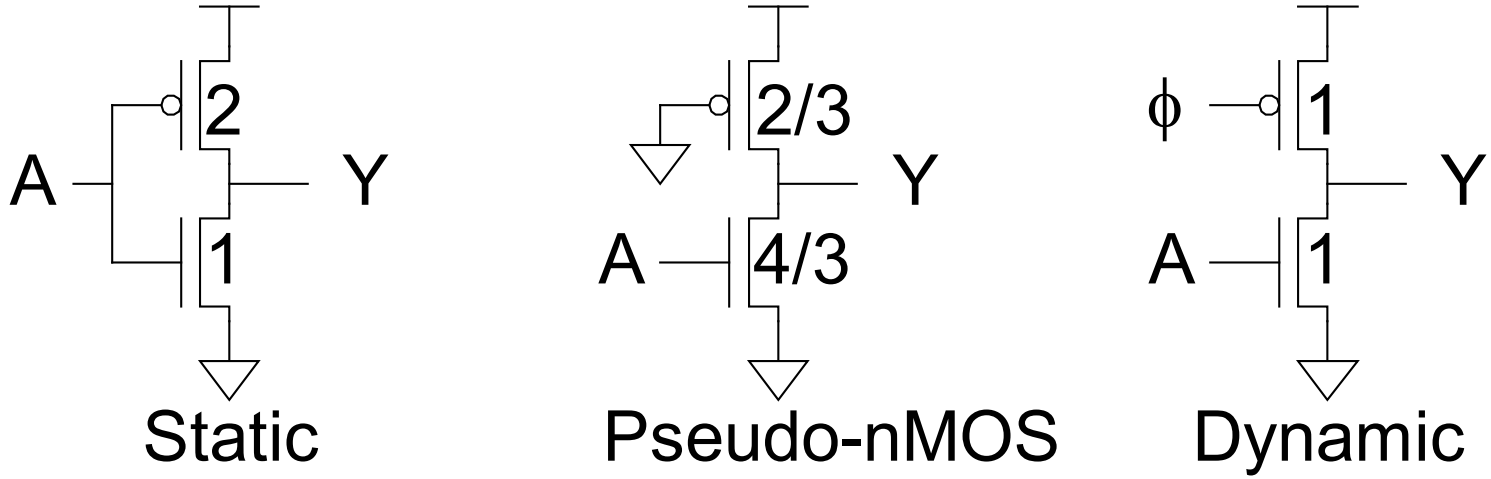


Fig. 9.21

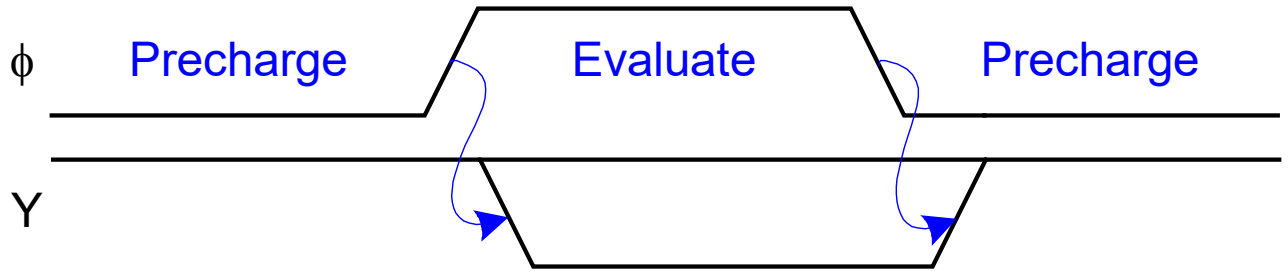


Fig. 9.22

9.2. Circuit families (14)

- What if pulldown network is ON during precharge?
- An extra clocked evaluation transistor can be added to avoid contention.

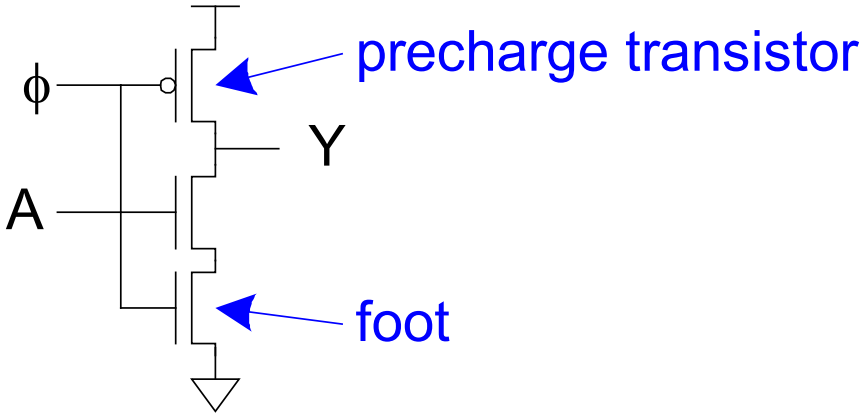
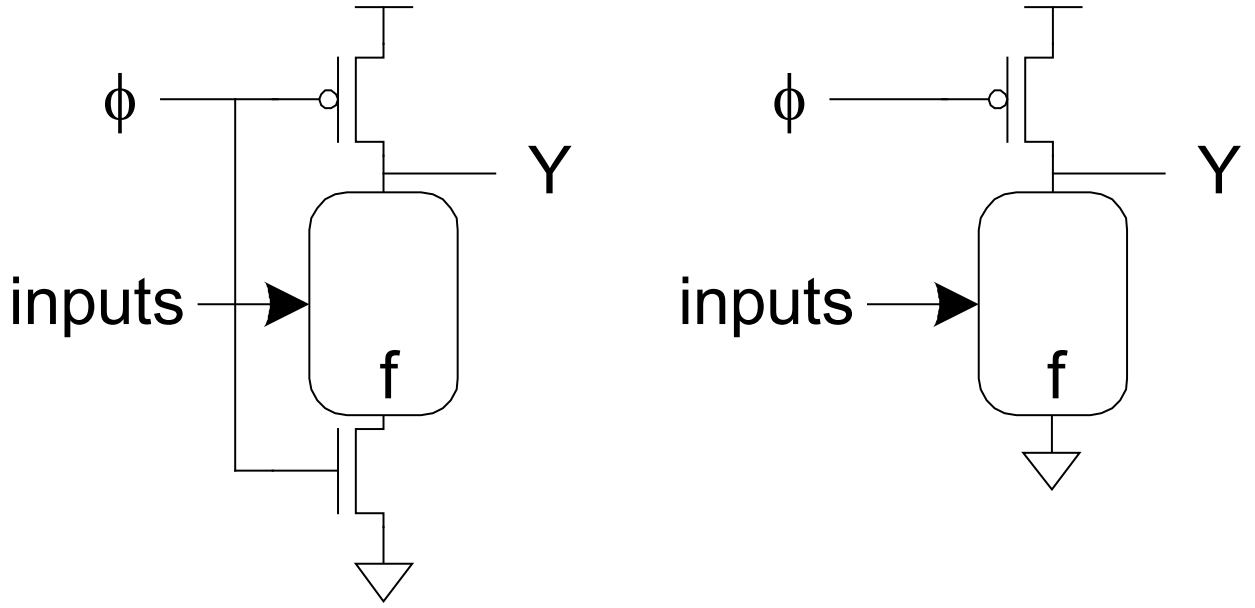


Fig. 9.23



footed unfooted

Fig. 9.24

9.2. Circuit families (15)

- Catalog of dynamic gates

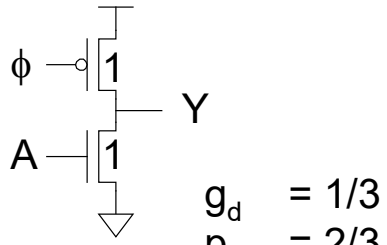
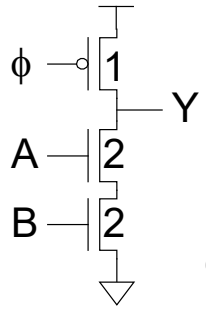
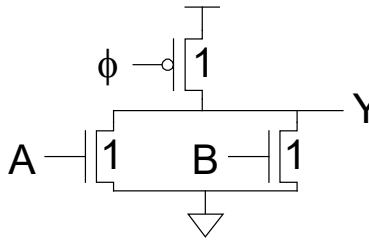
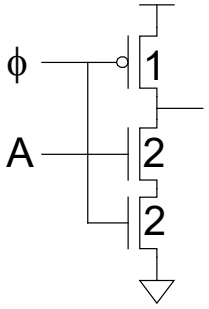
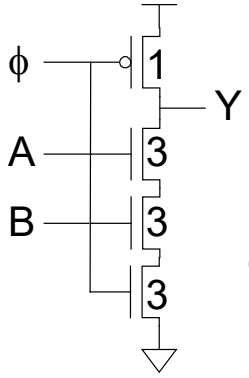
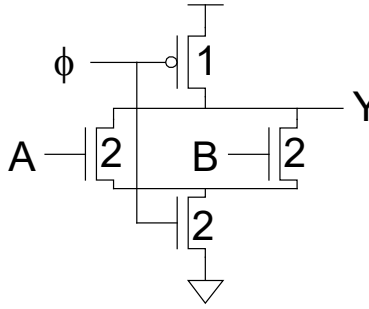
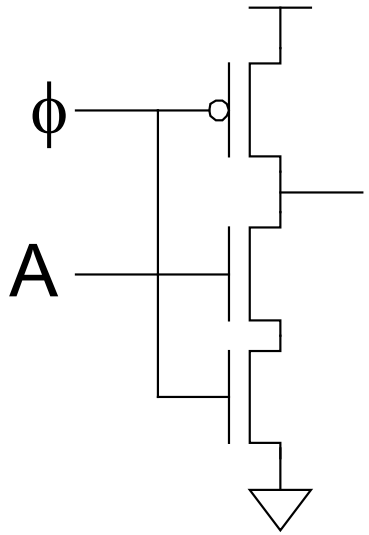
	Inverter	NAND2	NOR2
unfooted	 $g_d = 1/3$ $p_d = 2/3$	 $g_d = 2/3$ $p_d = 3/3$	 $g_d = 1/3$ $p_d = 3/3$
footed	 $g_d = 2/3$ (1) $p_d = 3/3$ (1)	 (4/3) $g_d = 3/3$ $p_d = 4/3$ (2)	 (5/3) $g_d = 2/3$ $p_d = 5/3$ (2)

Fig. 9.25

9.2. Circuit families (16)

- Dynamic gates require *monotonically rising* inputs during evaluation.
  - 0 ➔ 0, 0 ➔ 1, 1 ➔ 1. But not 1 ➔ 0



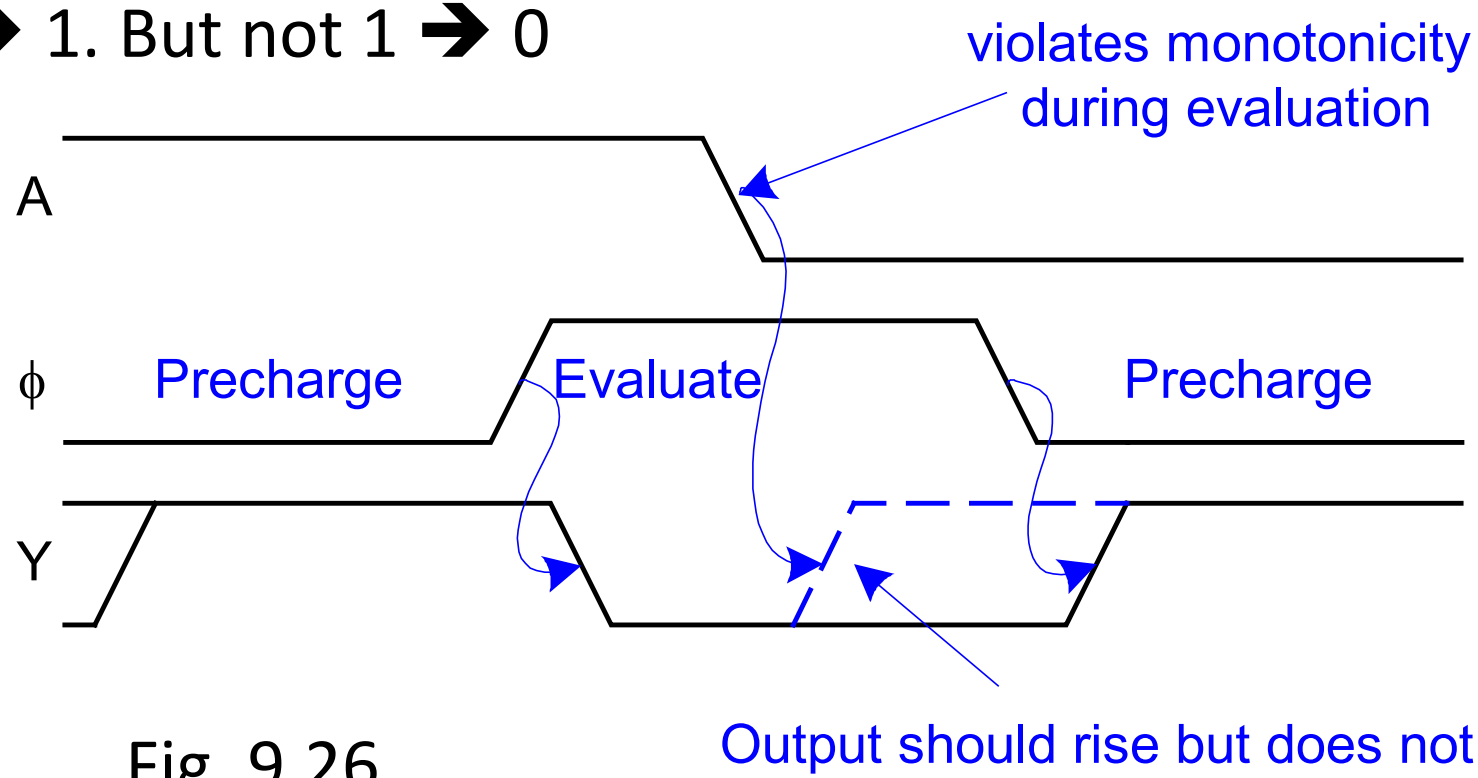
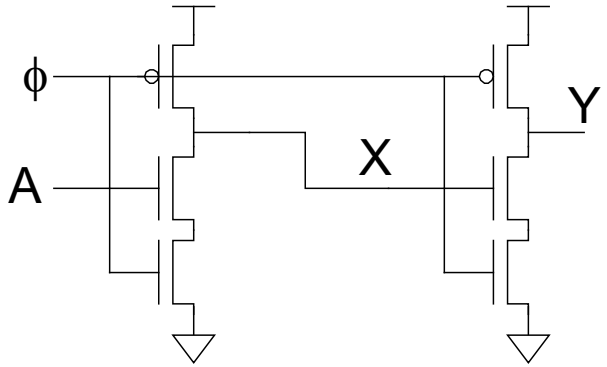
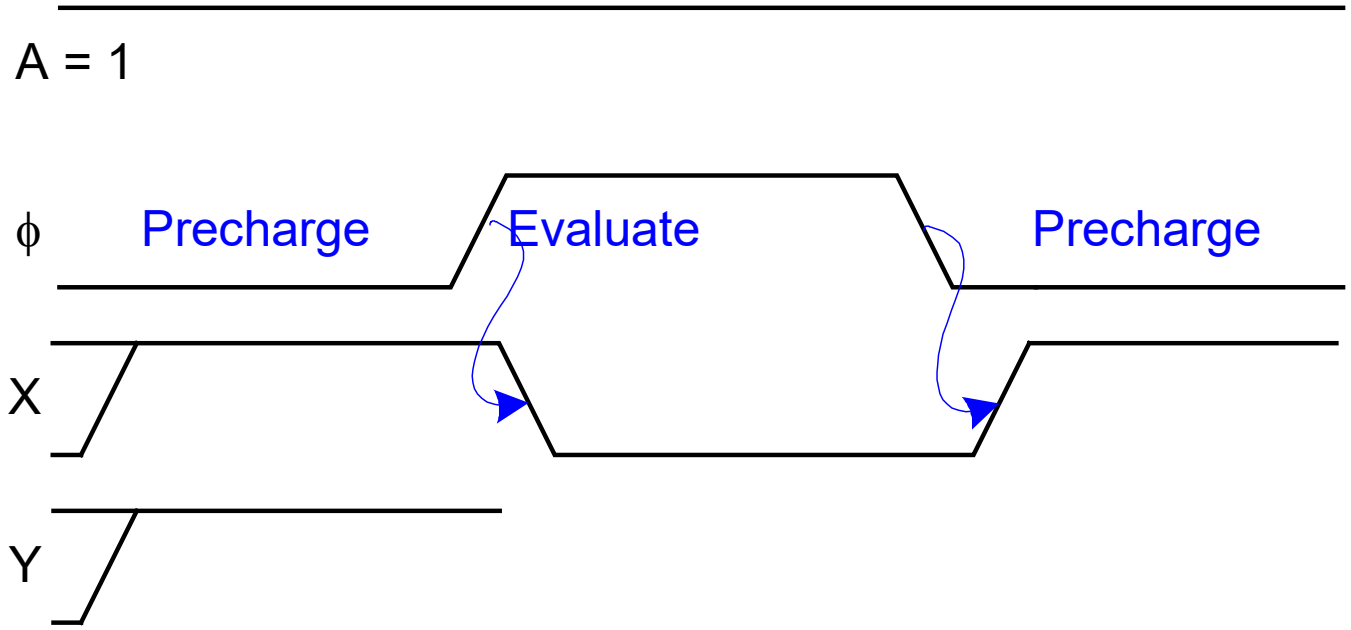


Fig. 9.26

9.2. Circuit families (17)

- But, dynamic gates produce monotonically falling outputs during evaluation.
  - Dynamic gates sharing the same clock cannot be directly connected.

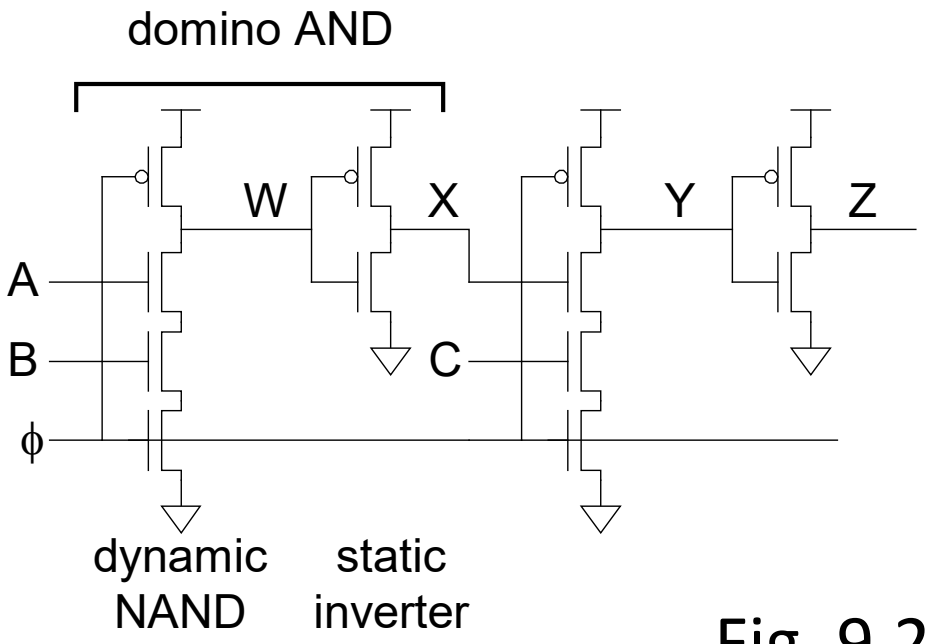


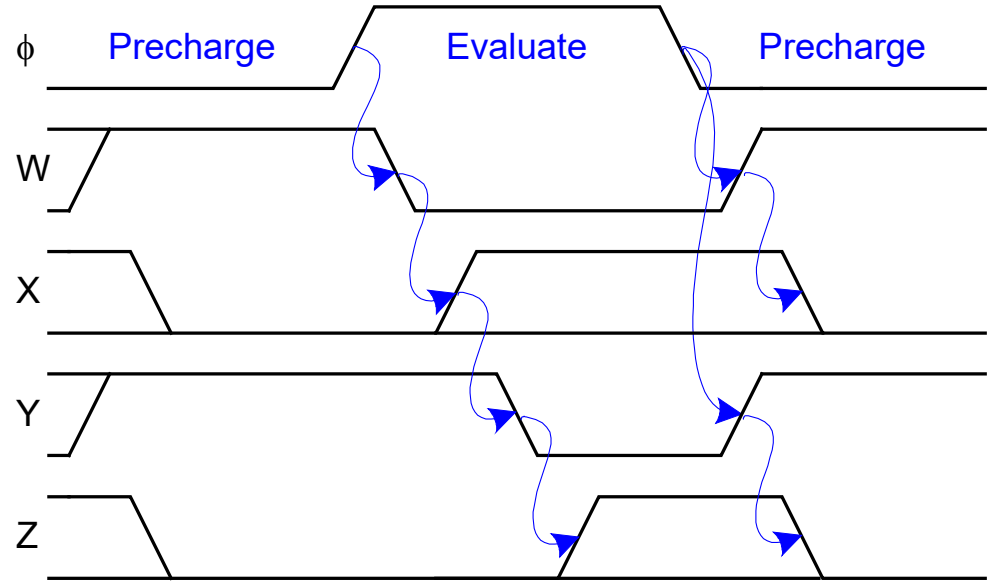


Draw it!

9.2. Circuit families (18)

- Place a static CMOS inverter between dynamic gates.
  - The dynamic-static pair is called a *domino* gate.
  - The dynamic output is monotonically falling during evaluation.





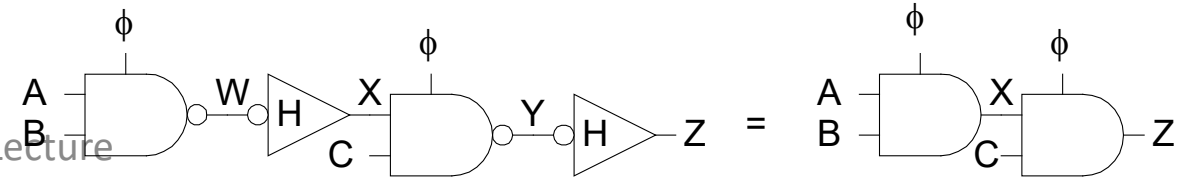


Fig. 9.28

9.2. Circuit families (19)

- Each domino gate triggers next one, like a string of dominos toppling over.
  - Precharge occurs in parallel, but evaluation occurs sequentially.
  - Thus, evaluation is more critical than precharge.
  - HI-skewed static stages can perform logic.

9.2. Circuit families (20)

- Compound domino
  - More complex inverting static CMOS gates such as NANDs or NORs in placed of the inverter

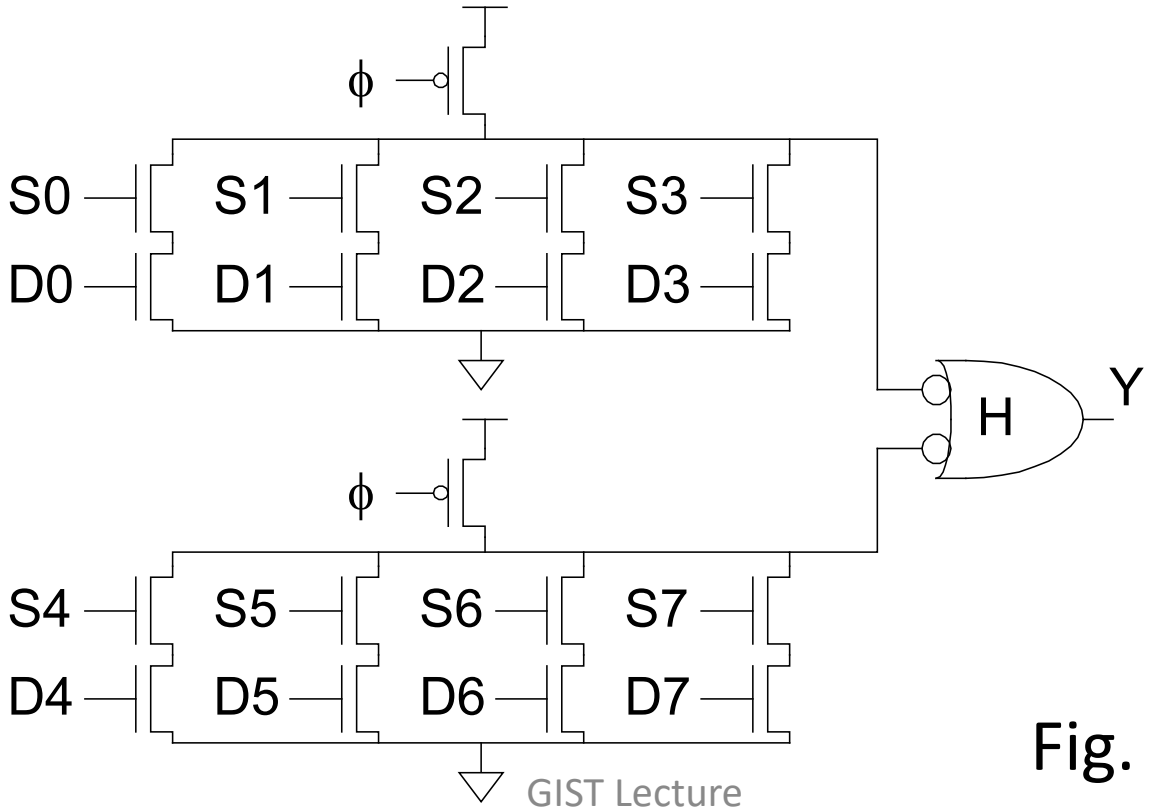
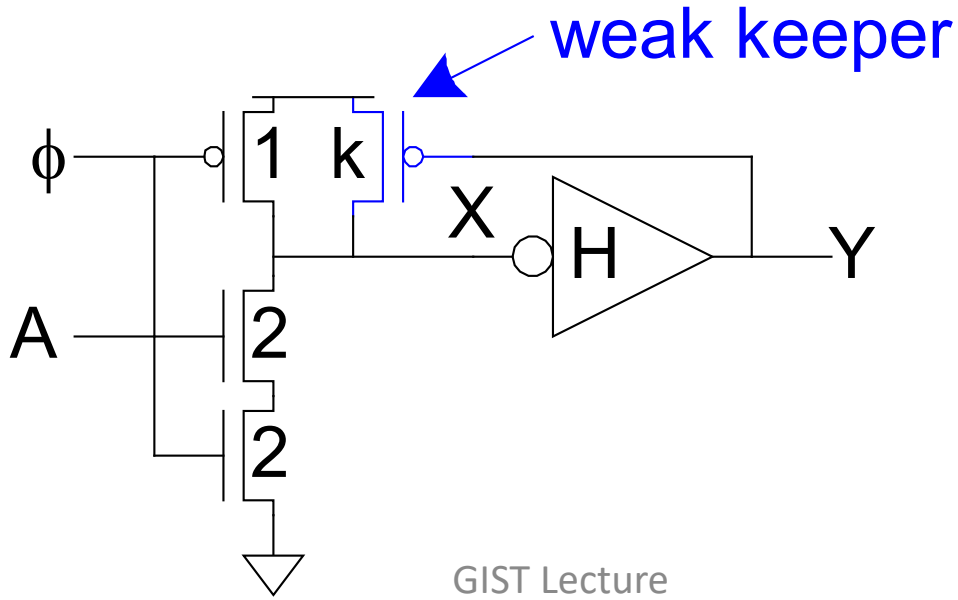


Fig. 9.29

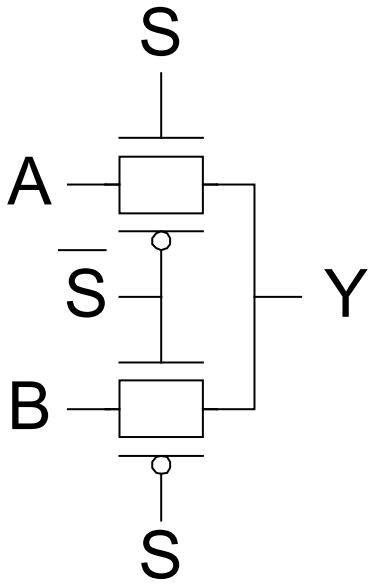
9.2. Circuit families (21)

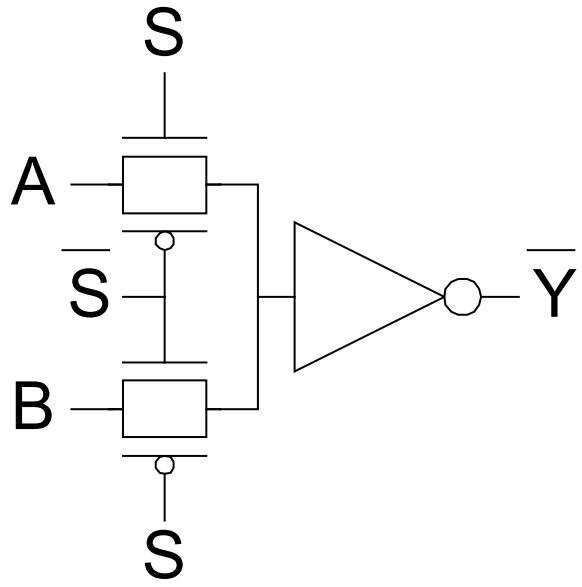
- Dynamic node floats high during evaluation.
  - Transistors are leaky. (We have non-negligible I_{OFF}.)
  - Dynamic value will leak away over time.
- Use keeper to hold dynamic node.
  - Must be weak enough not to fight evaluation



9.2. Circuit families (22)

- Pass transistor circuits
  - Use pass transistors like switches to do logic
  - Example) 2-input multiplexer





Thank you!