Digital Integrated Circuit
Lecture 6 MOS Transistor Theory

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Review of Previous Lecture

Lecture 5

- Long-channel IV
  - Oxide thickness is important. (C_{OX})
  - After some manipulation, we have

$$I_d = 0$$

Subthreshold

$$I_d = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$

Linear

$$I_d = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

Saturation

  - Here,

$$\beta = \mu_n C_{OX}\frac{W}{L}$$

Supplementary

- Derivation of linear IV
  - At any x,

$$I_d = WC_{OX}\left(V_g - V_c(x) - V_t\right)\mu_n \frac{dV_c(x)}{dx}$$

  - Integration from 0 to L,

$$LI_d = \mu_n C_{OX} W \int_0^L \left(V_g - V_c(x) - V_t\right)\frac{dV_c(x)}{dx}dx$$

$$= \mu_n C_{OX} W \int_{V_s}^{V_d} \left(V_g - V_c - V_t\right)dV_c = \mu_n C_{OX} W \left[\left(V_g - V_t\right)V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

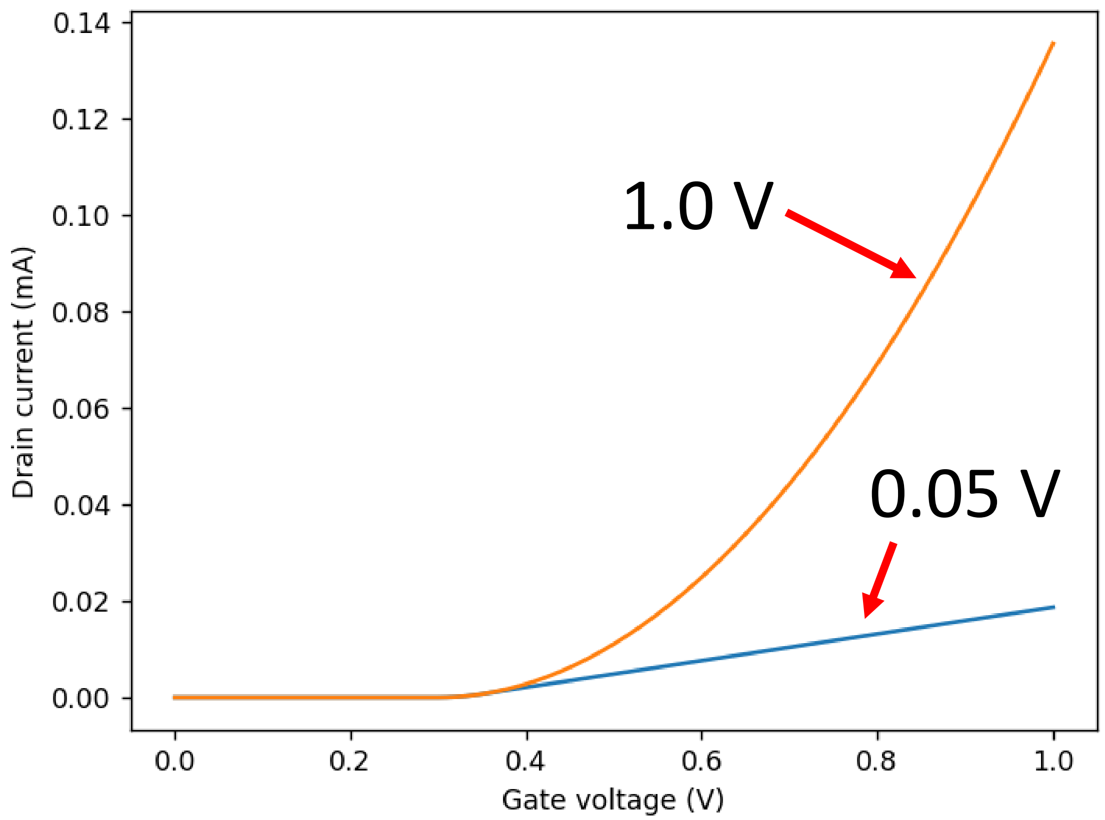
  - (This slide will be used in this lecture.)

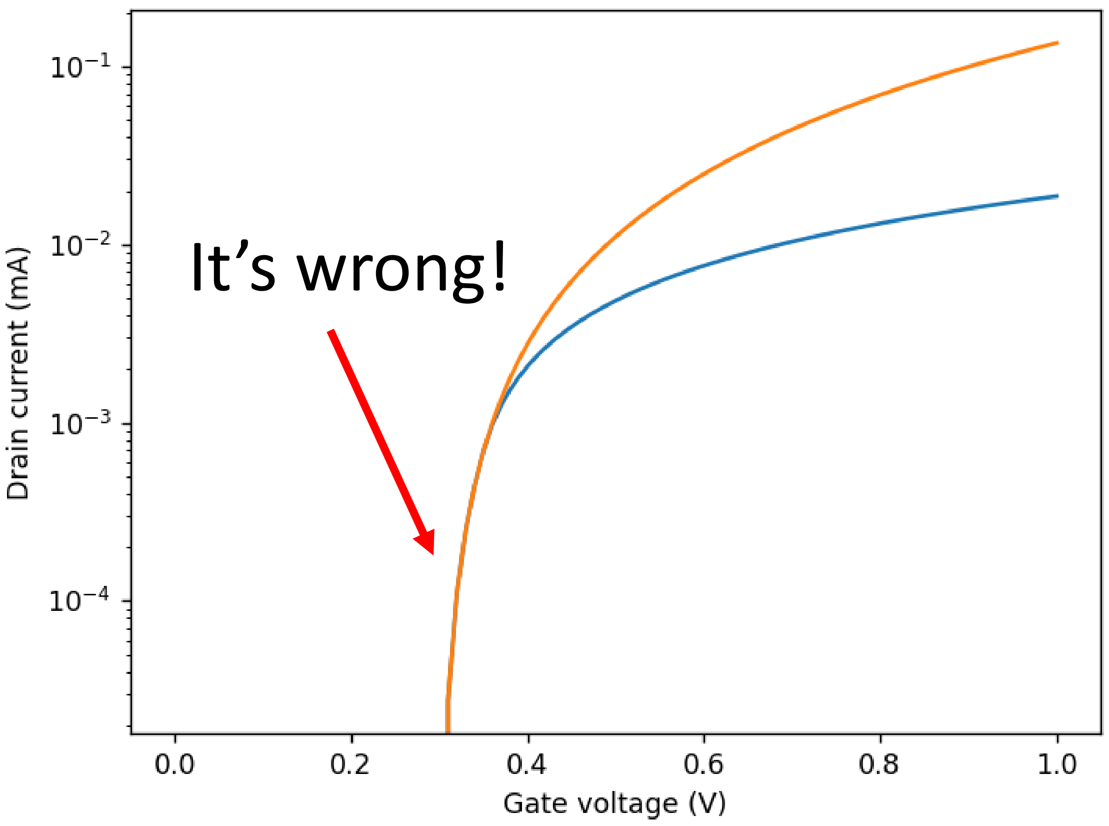
2.2 Long-channel IV

2.2. Long-channel IV (4)

- IV characteristics of an NMOSFET
  - Input characteristics

V_{DD} = 1.0 V, W/L = 2, t_{ox} = 1 nm, μ_n = 80 cm^2/V sec, and V_t is 0.3 V.

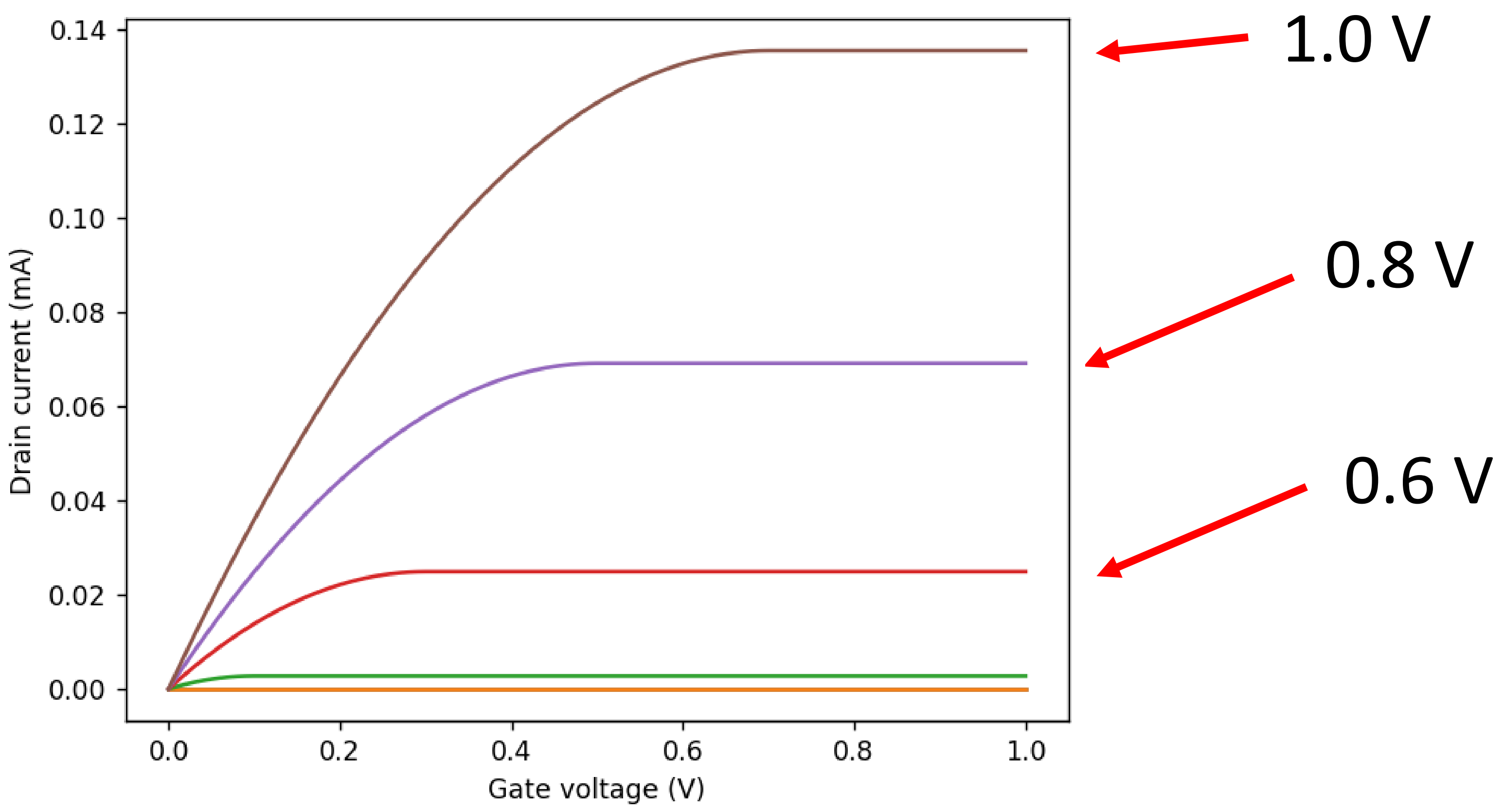




2.2. Long-channel IV (5)

V_{DD} = 1.0 V, W/L = 2, t_{ox} = 1 nm, μ_n = 80 cm^2/V sec, and V_t is 0.3 V.

- IV characteristics of an NMOSFET
  - Output characteristics



2.3 Capacitance

2.3. Capacitance (1)

- Any two conductors separated by an insulator have capacitance.
- Gate-to-channel capacitance is very important.
  - It creates channel charge which is necessary for operation.
- Source and drain have capacitance to body across the reverse-biased diodes.
  - It is called the diffusion capacitance, because it is associated with source/drain diffusion regions.

2.3. Capacitance (2)

- Gate capacitance
  - It is given as $C_g = C_{OX}WL$.
- Overlap capacitance, C_{gs} and C_{gd}

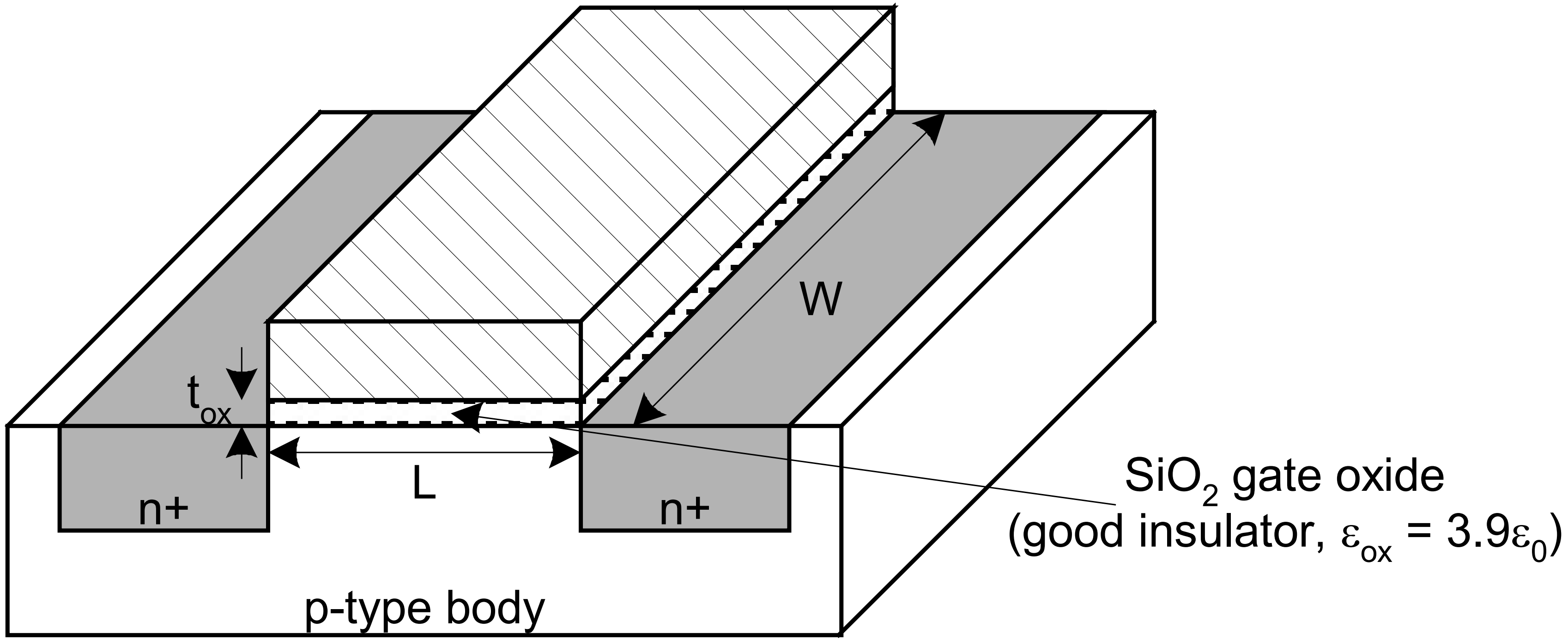


Fig. 2.6

2.3. Capacitance (3)

- Diffusion capacitance, C_{sb} and C_{sb}
  - Parasitic capacitance
  - Due to the PN junction between a diffusion region and the substrate

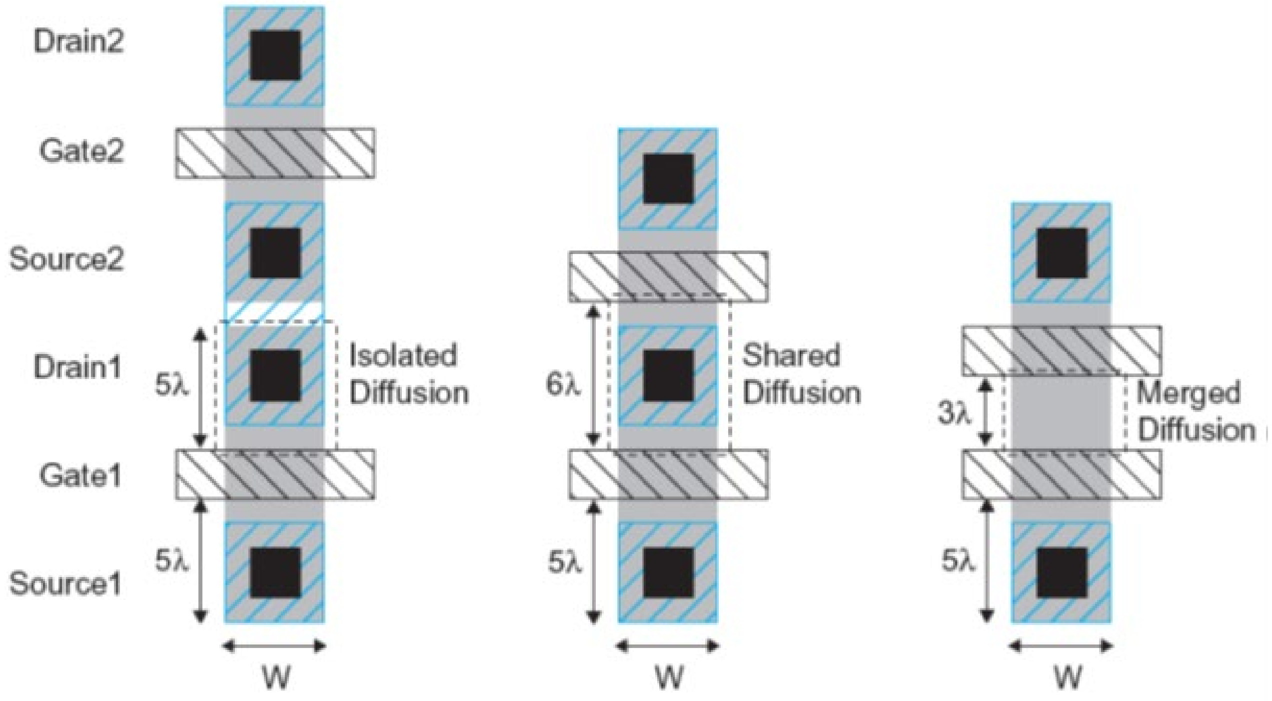
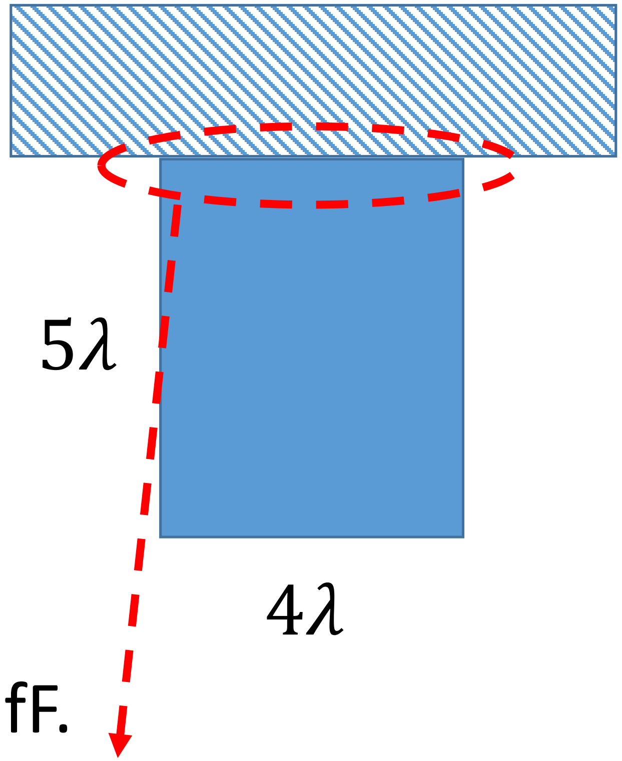


Fig. 2.8

2.3. Capacitance (4)



- Total source parasitic capacitance is

$$C_{sb} = AS \times C_{jbs} + PS \times C_{jbssw}$$

- Example 2.2) (Assume that is 25 nm.)
  - Area is $4\lambda \times 5\lambda = 20\lambda^2 = 0.0125\ \mu\text{m}^2$.
  - Perimeter is $2(4\lambda + 5\lambda) = 18\lambda = 0.45\ \mu\text{m}$.
  - Since $C_{jbd} = 1.2 fF/\mu\text{m}^2$, the capacitance is 0.015 fF.
  - Assume that $C_{jbdsw} = 0.1 fF/\mu\text{m}$. However, the sidewall facing the channel is more significant, $C_{jbdswg} = 0.36 fF/\mu\text{m}$.
  - Contribution from sidewalls is 0.071 fF (= 0.35 um X 0.1 fF/um + 0.1 um X 0.36 fF/um).
  - The overall diffusion capacitance is 0.086 fF.

2.4 Nonideal IV

2.4. Nonideal IV (1)

- 65nm IBM
  - Reduced current
  - Linear increase of saturation current
  - Nonzero slope in the saturation mode

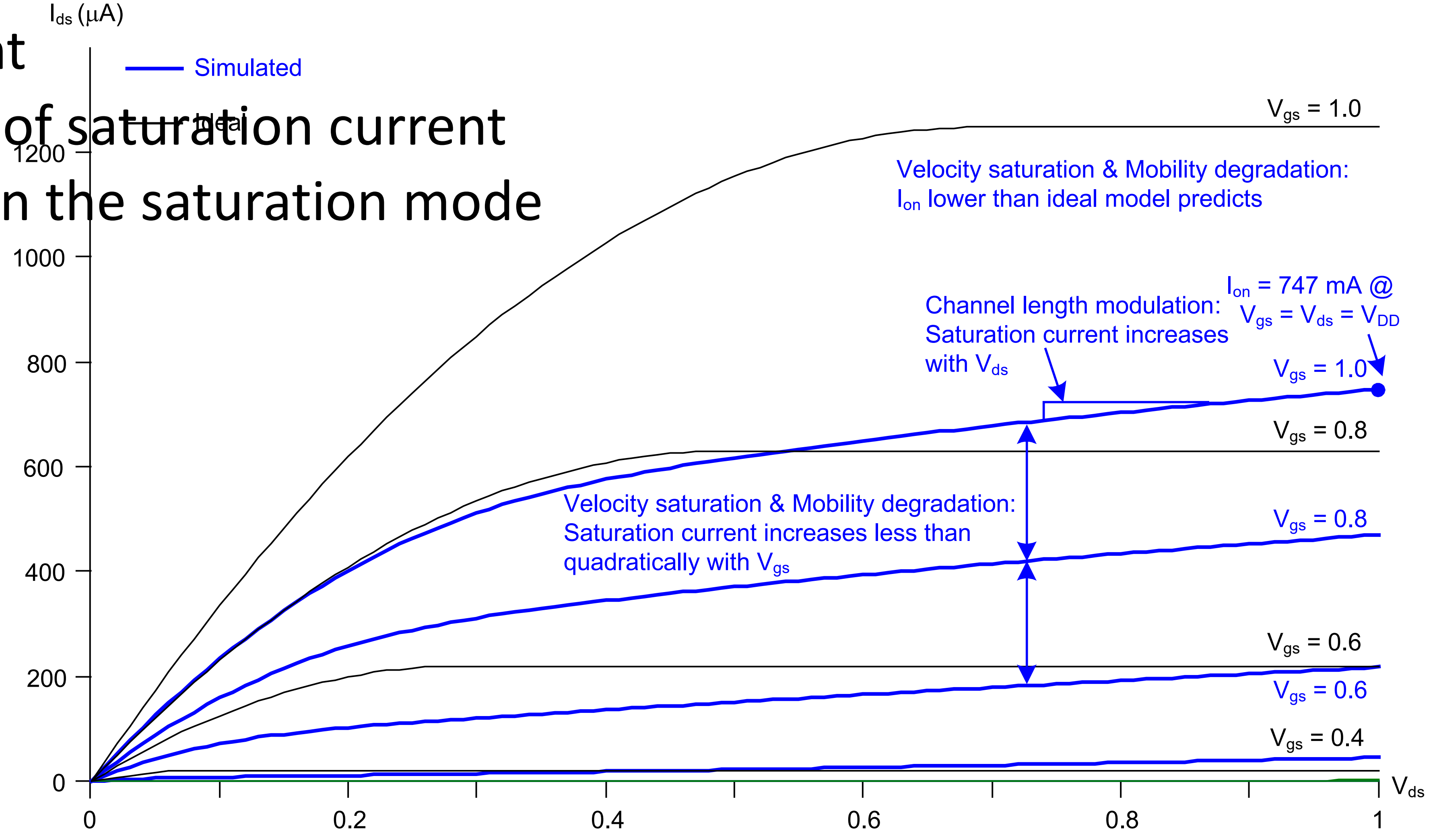
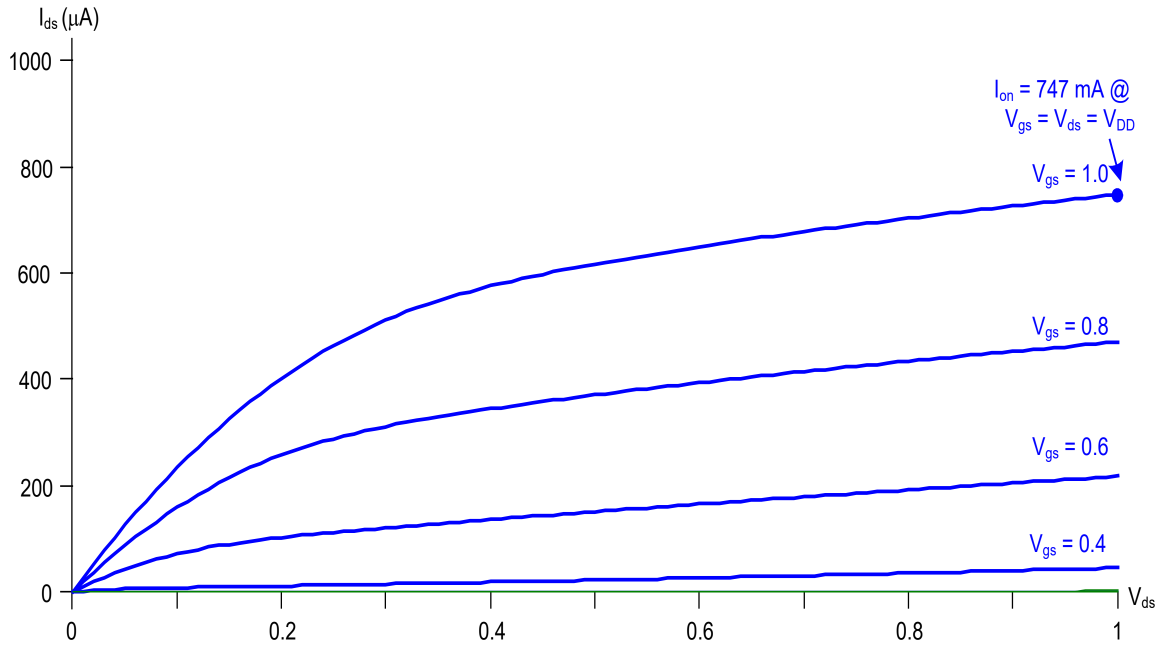
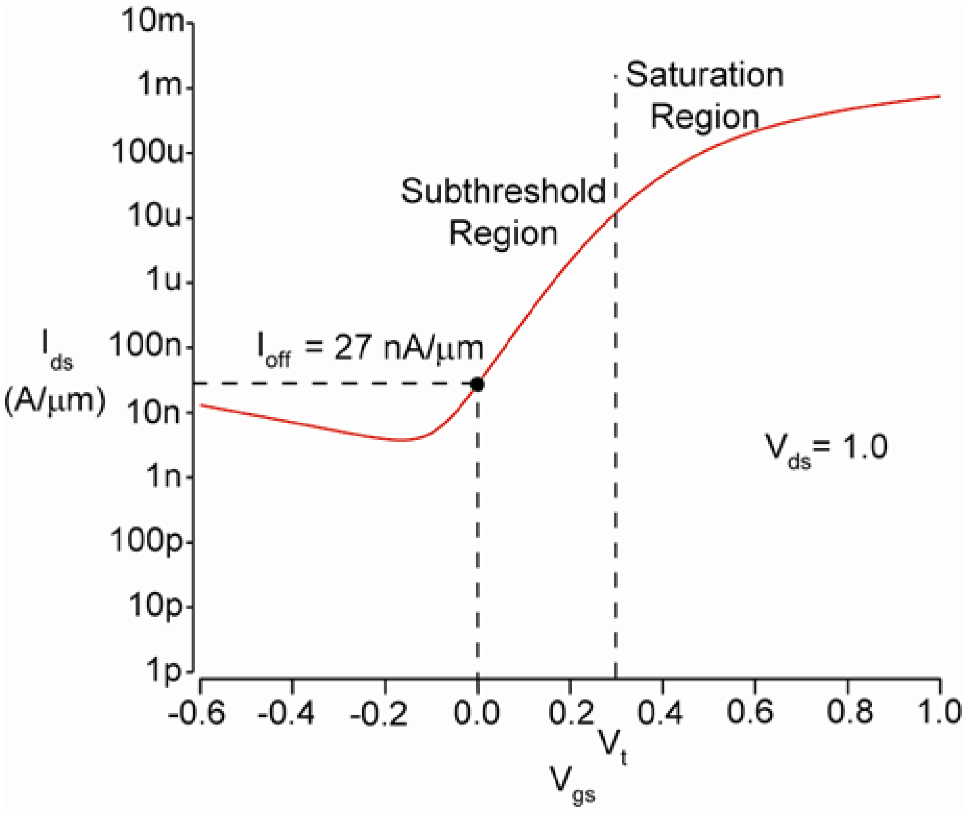


Fig. 2.14

2.4. Nonideal IV (2)

- ON and OFF current (Drain currents)
  - ON current: $V_{gs} = V_{ds} = V_{DD}$
  - OFF current: $V_{gs} = 0$ and $V_{ds} = V_{DD}$

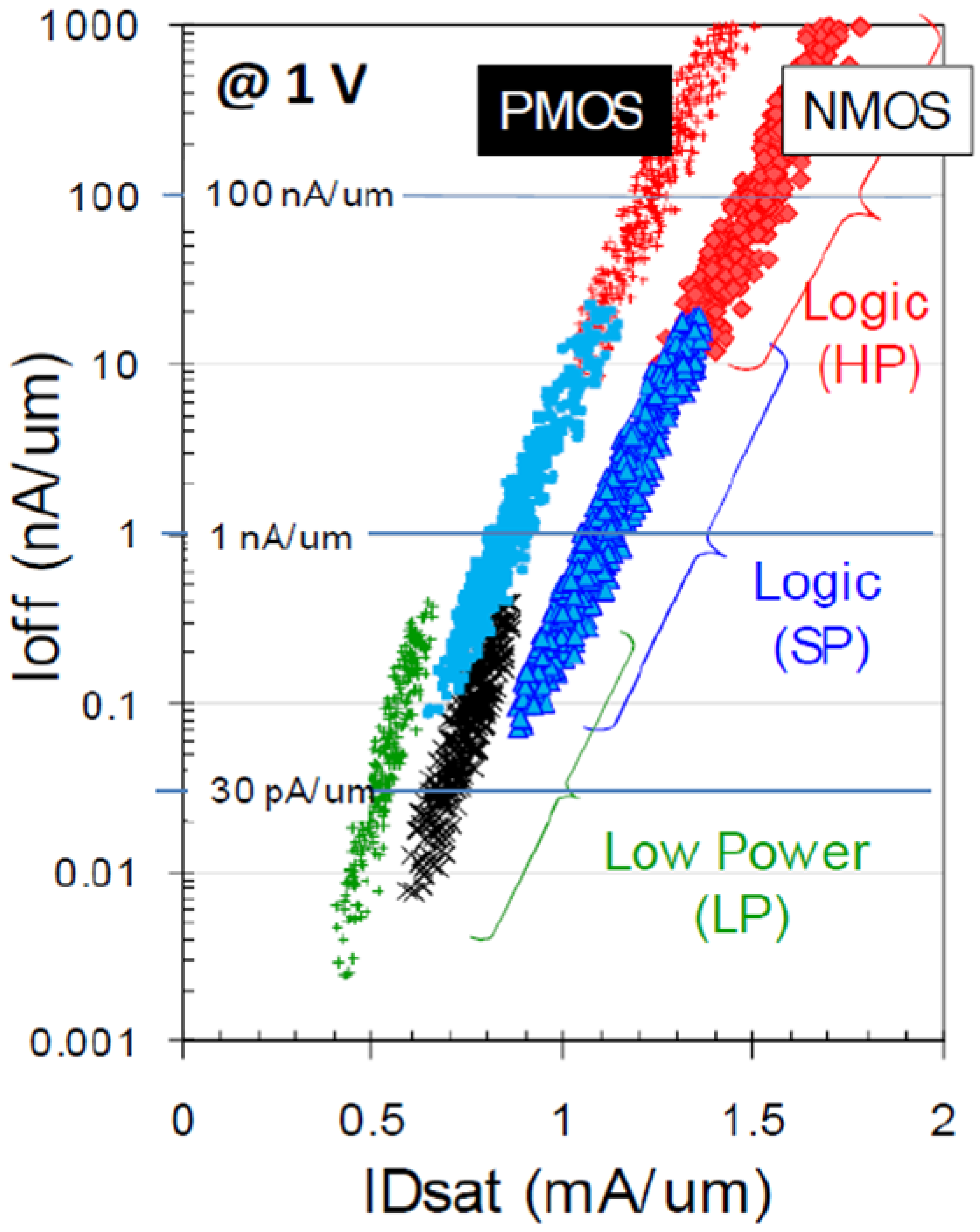




2.4. Nonideal IV (3)

- Intel 32 nm transistor
  - Various leakage options
  - Iff in log scale
  - Ion in linear scale
  - HP (high performance)
  - SP (standard performance/power)
  - LP (low power)

(Intel's 2011 IEDM abstract)



2.4. Nonideal IV (4)

- Intel 22 nm transistor

Table I. 22nm modular SoC transistor options and device characteristics

Transistor Type	High Speed Logic		Low Power Logic		High Voltage	
Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)	0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)	90	90	90	108	min. 180	min. 450
Lgate (nm)	30	34	34	40	min. 80	min. 280
N/PMOS Idsat/Ioff (mA/um)	1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V 30 pA/um	0.35 / 0.33 @ 0.75 V 15 pA/um	0.92 / 0.8 @ 1.8 V 10 pA/um	1.0 / 0.85 @ 3.3 V 10 pA/um

(Intel's 2012 IEDM abstract)

2.4. Nonideal IV (5)

- Mobility degradation due to the verteic E-field
  - Collisions with oxide interface

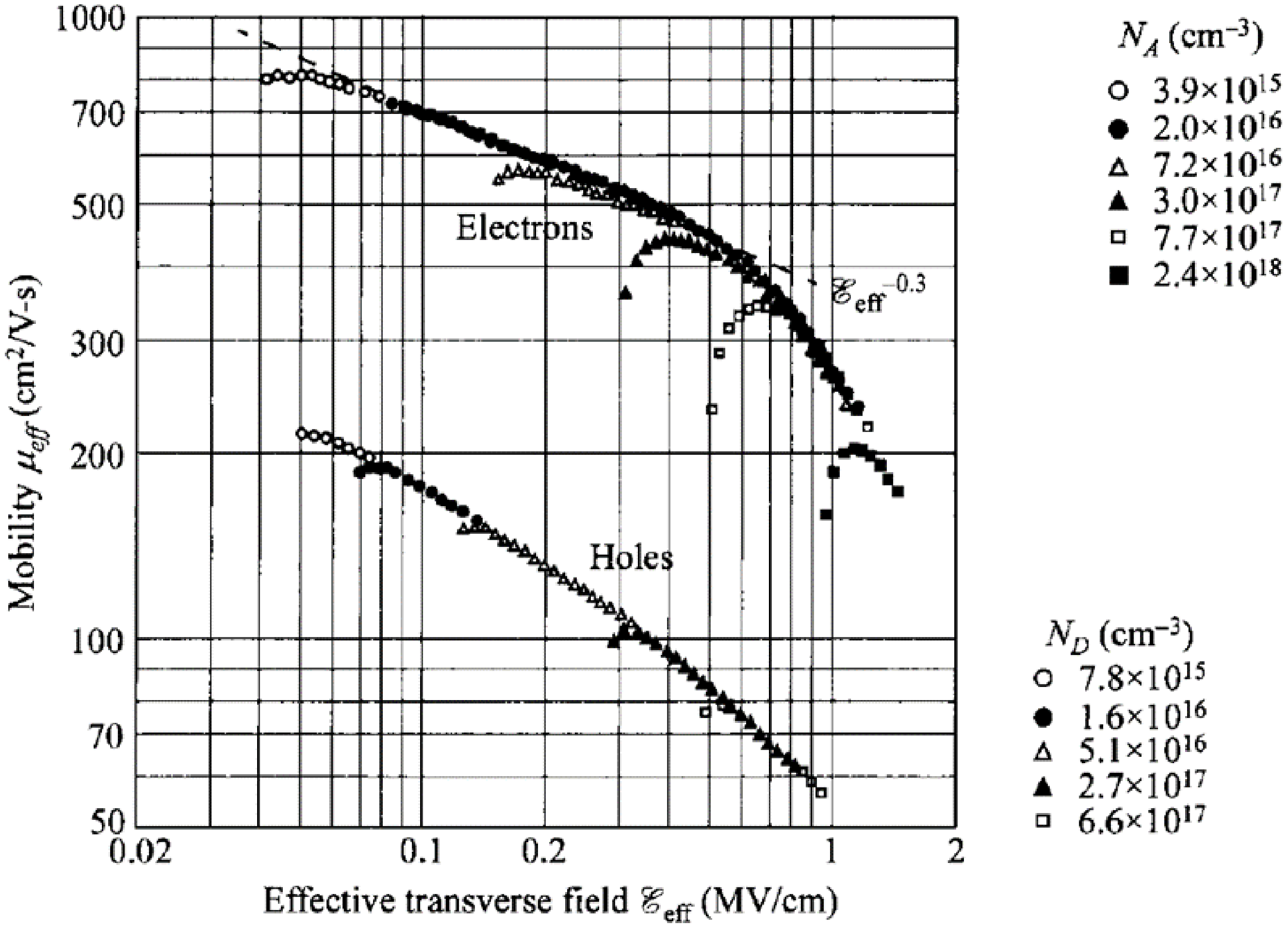
$$\mu_{\text{eff}-n} = \frac{540 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\left(\frac{V_{gs}+V_t}{0.54\frac{\text{V}}{\text{nm}}t_{\text{ox}}}\right)^{1.85}} \qquad \mu_{\text{eff}-p} = \frac{185 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\frac{\left|V_{gs}+1.5V_t\right|}{0.338\frac{\text{V}}{\text{nm}}t_{\text{ox}}}}$$

Calculate the mobilties at $|V_{gs}|$ = 1.0 V. Assume that t_{ox} = 1.05 nm and $|V_t|$ = 0.3 V.

  - Why do we have different behaviors for electrons and holes?

2.4. Nonideal IV (6)

- Experimental data (“Universal” mobility curve)



Inversion layer mobility (Sze’s book)

2.4. Nonideal IV (7)

- Velocity saturation
  - Saturation velocity (Canali model)
  - Electrons: 1.07×10^7 cm/sec
  - Holes: 8.37×10^6 cm/sec
  - A simple model

$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases}$$

$$E_c = \frac{2 v_{\text{sat}}}{\mu_{\text{eff}}}$$

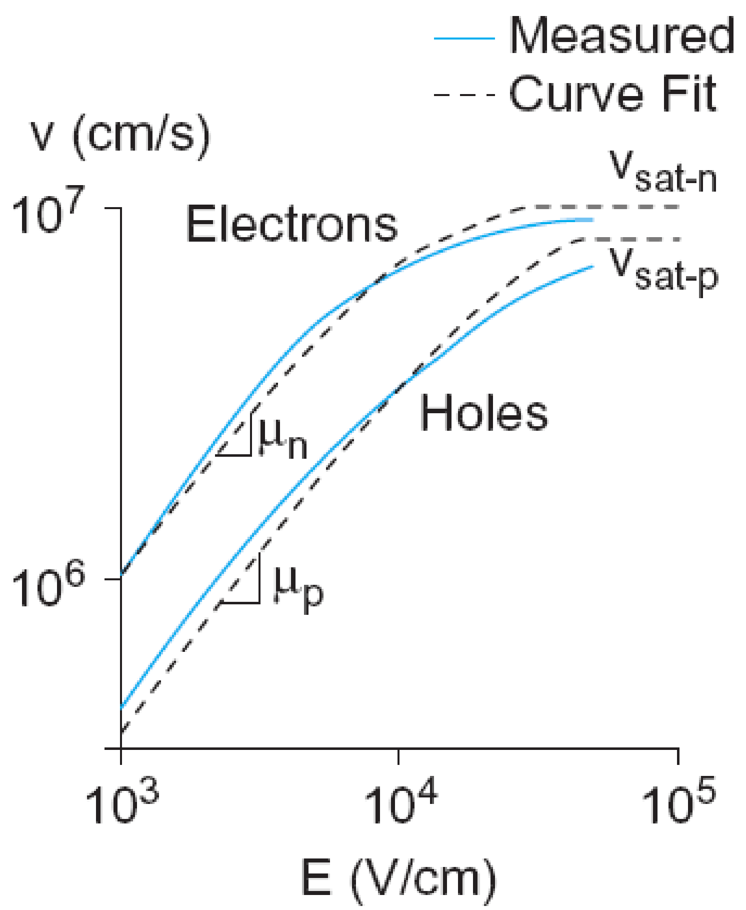


Fig. 2.15

2.4. Nonideal IV (8)

- When the electric field is lower than E_c,

$$E = \frac{I_d}{\mu_n C_{OX} W \left(V_g - V_t - V_c\right) - \frac{I_d}{E_c}} = \frac{dV_c}{dx}$$

  - (Note that the sign is not correct but understood.)
  - Then, the integration gives

$$LI_d = \int_{V_s}^{V_d} \left[\mu_n C_{OX} W \left(V_g - V_t - V_c\right) - \frac{I_d}{E_c}\right] dV_c$$

$$= \mu_n C_{OX} W \left[\left(V_g - V_t\right) V_{ds} - \frac{1}{2} V_{ds}^2\right] - \frac{I_d}{E_c} V_{ds}$$

2.4. Nonideal IV (9)

- Drain current with the velocity saturation

$$I_d = \frac{1}{L + \frac{V_{ds}}{E_c}} \mu_n C_{OX} W \left[\left(V_g - V_t \right) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

  - With $V_c = E_c L$,

$$I_d = \frac{1}{1 + \frac{V_{ds}}{V_c}} \mu_n C_{OX} \frac{W}{L} \left[\left(V_g - V_t \right) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

  - The factor, $\frac{1}{1+\frac{V_{ds}}{V_c}}$, describes the velocity saturation.
  - Then, when do we have the saturation?

2.4. Nonideal IV (10)

- Condition for saturation, $E = E_c$ @ $x = L$
  - In this case, $V_d = V_{dsat}$ and $I_d = I_{dsat}$

$$E_c = \frac{I_{dsat}}{\mu_n C_{OX} W\left(V_g - V_t - V_{dsat}\right) - \frac{I_{dsat}}{E_c}}$$

  - The saturation current becomes

$$I_{dsat} = \frac{1}{2}\mu_n C_{OX} W\left(V_g - V_t - V_{dsat}\right) E_c$$

  - What is V_{dsat}?

2.4. Nonideal IV (11)

- Equating two expressions,

$$I_{dsat} = \frac{1}{2}\mu_n C_{OX} W \left(V_g - V_t - V_{dsat}\right) E_c$$

$$I_{dsat} = \frac{1}{1 + \frac{V_{dsat}}{V_c}} \mu_n C_{OX} \frac{W}{L} \left[\left(V_g - V_t\right) V_{dsat} - \frac{1}{2} V_{dsat}^2\right]$$

  – With the gate overdrive voltage, $V_{GT} \equiv V_g - V_t$, we can find

$$V_{dsat} = \frac{V_{GT} V_c}{V_{GT} + V_c}$$

$$I_{dsat} = C_{OX} W \frac{V_{GT}^2}{V_{GT} + V_c} v_{sat}$$

Homework#2

- Due: AM08:00, September 19
- Problem#1
  - Compare three modes for the velocity saturation:
  - 1) The one studied in this lecture.
  - 2) $v_{sat} = \frac{\mu_{eff} E}{\sqrt{1+\left(\frac{E}{E_c}\right)^2}}$
  - 3) $v_{sat} = \frac{\mu_{eff} E}{1+\frac{E}{E_c}}$ for any E value
  - Draw the velocity-field graph in the semi-logarithmic scale. μ_{eff} is 710 cm^2/V sec and E_c is 11 kV/cm. The electric field varies from 100 V/cm to 100 kV/cm.

Homework#2

- Problem#2
  - Draw the output characteristics of an NMOSFET, by using two IV models. Compare them.
  - 1) Long-channel IV
  - 2) The one studied in this lecture.
  - Parameters are: W is 100 µm. L is 1 µm. t_{ox} is 25 nm. The effective mobility is assumed to be a constant of 500 cm^2/V sec, for simplicity. E_c is 11 kV/cm. Consider five values of V_{GT}: 0.5 V, 1.0 V, 1.5 V, 2.0 V, and 2.5 V. Increase the drain voltage up to 3.0 V.

Thank you!