Digital Integrated Circuit Lecture 19 Interconnect

Sung-Min Hong (smhong@gist.ac.kr)
Semiconductor Device Simulation Laboratory
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

GIST Lecture

Review of Previous Lecture

Lecture 18

- Backside power delivery network
 - A new way to further scale down a transistor
- Wires
 - We need several metal layers.
 - It can be modeled as a distributed RC network.
 - -Sheet resistance, R_{\Box}

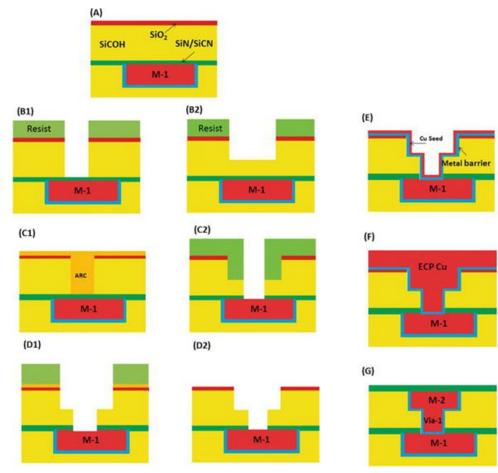
6.2 Interconnect modeling

6.2. Interconnect modeling (3)

- Al versus Cu
 - Dual damascene process

Metal	Bulk resistivity (μΩ • cm)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (AI)	2.8
Tungsten (W)	5.3
Titanium (Ti)	43.0

Table 6.2



(Cheng et al., "Copper metal for semiconductor interconnects")

6.2. Interconnect modeling (4)

Wire capacitance

– For a parallel plate,
$$C = \epsilon_{ox} \frac{A}{d}$$

– For a parallel plate,
$$C = \epsilon_{ox} \frac{A}{d}$$

$$C_{total} = C_{top} + C_{bot} + 2C_{adj} \approx \epsilon_o l \left[2k_{vert} \frac{w}{h} + 2k_{horiz} \frac{t}{s} \right] + C_{fringe}$$

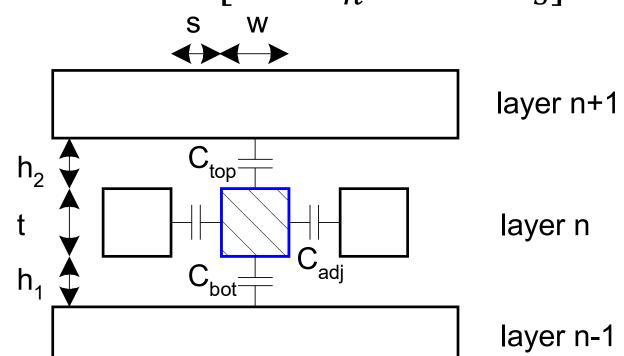
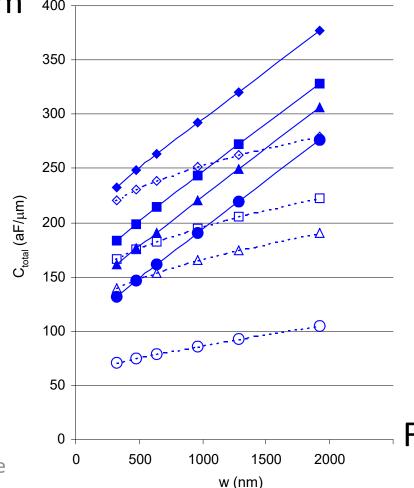


Fig. 6.11

6.2. Interconnect modeling (5)

- M2 capacitance data (180nm process)
 - Wire and oxide thicknesses of 0.7 μ m
 - Minimun width/spacing of 0.32 μm
 - -Typical dense wires have 0.2 fF/ μ m.



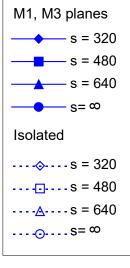


Fig. 6.12

6.3 Interconnect impact

6.3. Interconnect impact (1)

- Compute the sheet resistance of a 0.22 μm thick Cu wire in a 65 nm process.
 - -The sheet resistance is

$$R_{\Box} = \frac{\rho}{t} = \frac{2.2 \times 10^{-8} \,\Omega \,\mathrm{m}}{0.22 \,\mu\mathrm{m}} = 0.1 \,\Omega/_{\Box}$$

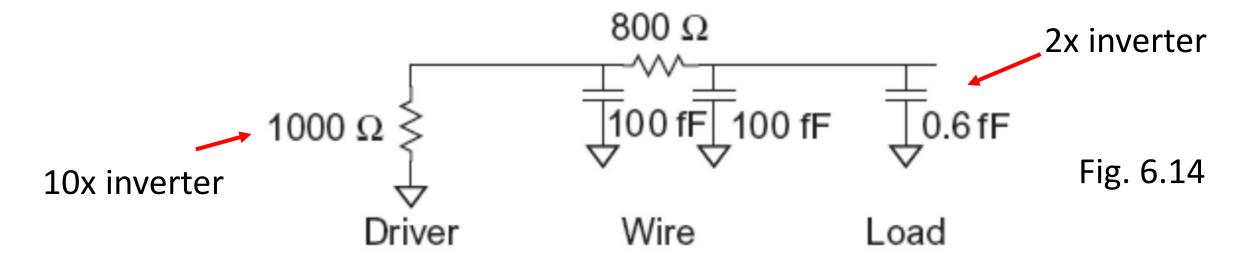
– If the wire is 0.125 μm wide and 1 mm long, the total resistance is

$$R = R_{\Box} \frac{l}{w} = 0.1 \,\Omega/_{\Box} \times \frac{1000 \,\mu\text{m}}{0.125 \,\mu\text{m}} = 800 \,\Omega$$

6.3. Interconnect impact (2)

- Estimate the delay of a 10x interver driving a 2x inverter at the end of the last slide.
 - The wire capacitance is 0.2 fF/ μ m.
 - The unit-sized NMOSFET has R = 10 $k\Omega$ and C = 0.1 fF.
 - Calculate the Elmore delay.

$$\tau = 1000\Omega \times 100 \text{ fF} + (1000\Omega + 800\Omega) \times (100 \text{ fF} + 0.6 \text{ fF})$$



6.3. Interconnect impact (3)

- Quadratic dependence of the delay on the wire length
- Consider the same wire in the last slide.
 - The 1 mm-long wire has R = 800 Ω and C = 0.2 pF.
 - When the length is doubled, both of R and C are doubled.
- N-segment L-model
 - Each segment has r and c. Then R = NX r and C = N X c.
 - -The Elmore delay

$$\sum_{i=1}^{N} irc = rc \sum_{i=1}^{N} i = rc \frac{N(N+1)}{2} \approx \frac{RC}{2}$$

6.3. Interconnect impact (4)

- Long wires have significant capacitance and thus require substantial amounts of energy to switch.
- Estimate the energy per unit length to send a bit of information (one rising and one falling transition) in the technology used in the previous slides.
 - -Assume that V_{DD} is 1 V. $E = (0.2 \text{ pF mm}^{-1})(1.0 \text{ V})^2 = 0.2 \text{ pJ bit}^{-1} \text{ mm}^{-1}$
 - If we 10⁹ bit per second, a 1-mm-long wire consumes 0.2 mW/Gbps.

Thank you!