Digital Integrated Circuit
Lecture 11 Delay

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Review of Previous Lecture

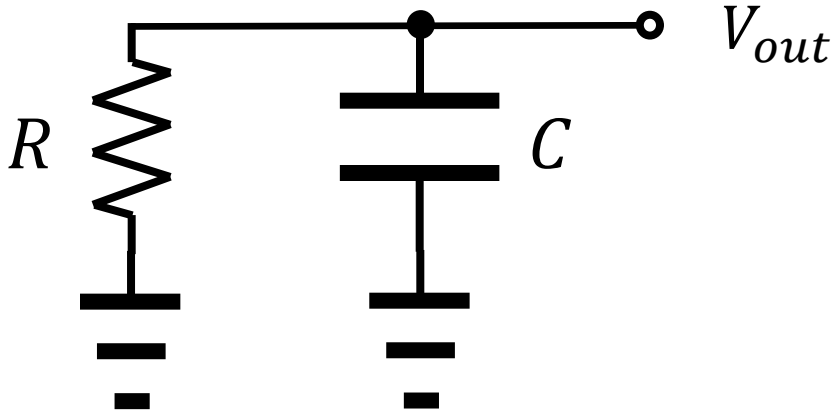
Lecture 10

- Noise margin of a CMOS inverter
- Delay
  - Transient simulation (SPICE)
  - Propagation delay

4.3 RC delay model

4.3. RC delay model (1)

- RC delay models approximate the nonlinear transistor IV and CV characteristics with an average resistance and capacitance over the switching range of the gate.
  - Total capacitance on output node: C
  - Effective resistance: R
  - Propagation delay ~ RC



4.3. RC delay model (2)

- Equivalent R, gate and diffusion capacitance
  - Unit NMOS (for example, $4\lambda/2\lambda$) is defined to have an effective resistance of R. An NMOS, whose width is k times unit width, has a resistance of R/k.
  - Let us assume that unit PMOS has an effective resistance of $2R$.
  - Capacitance is linearly scaled with the width.

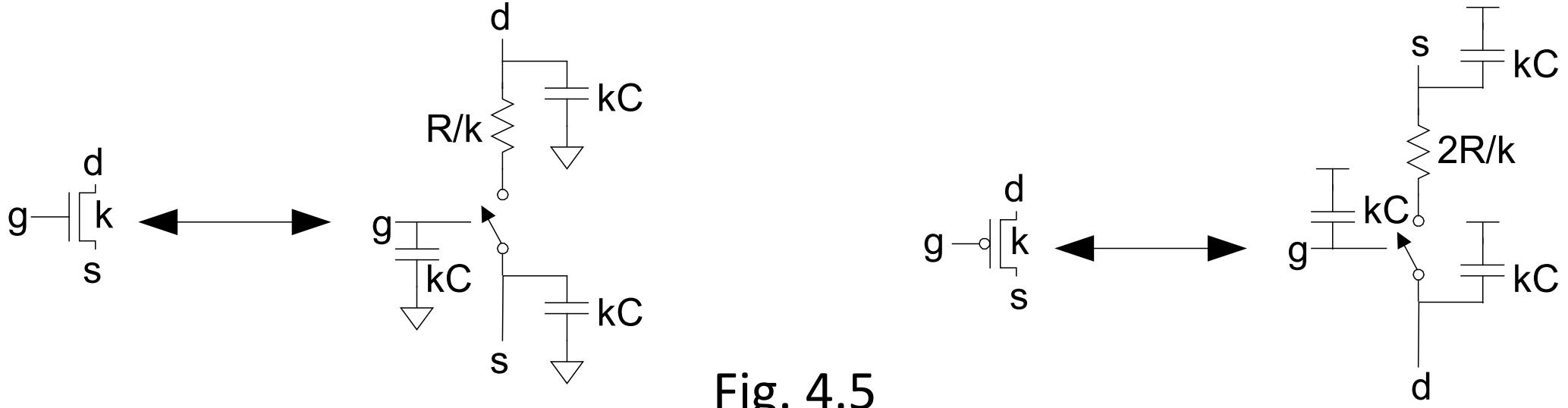


Fig. 4.5

4.3. RC delay model (3)

- A fanout-of-1 inverter
  - Estimate the delay.

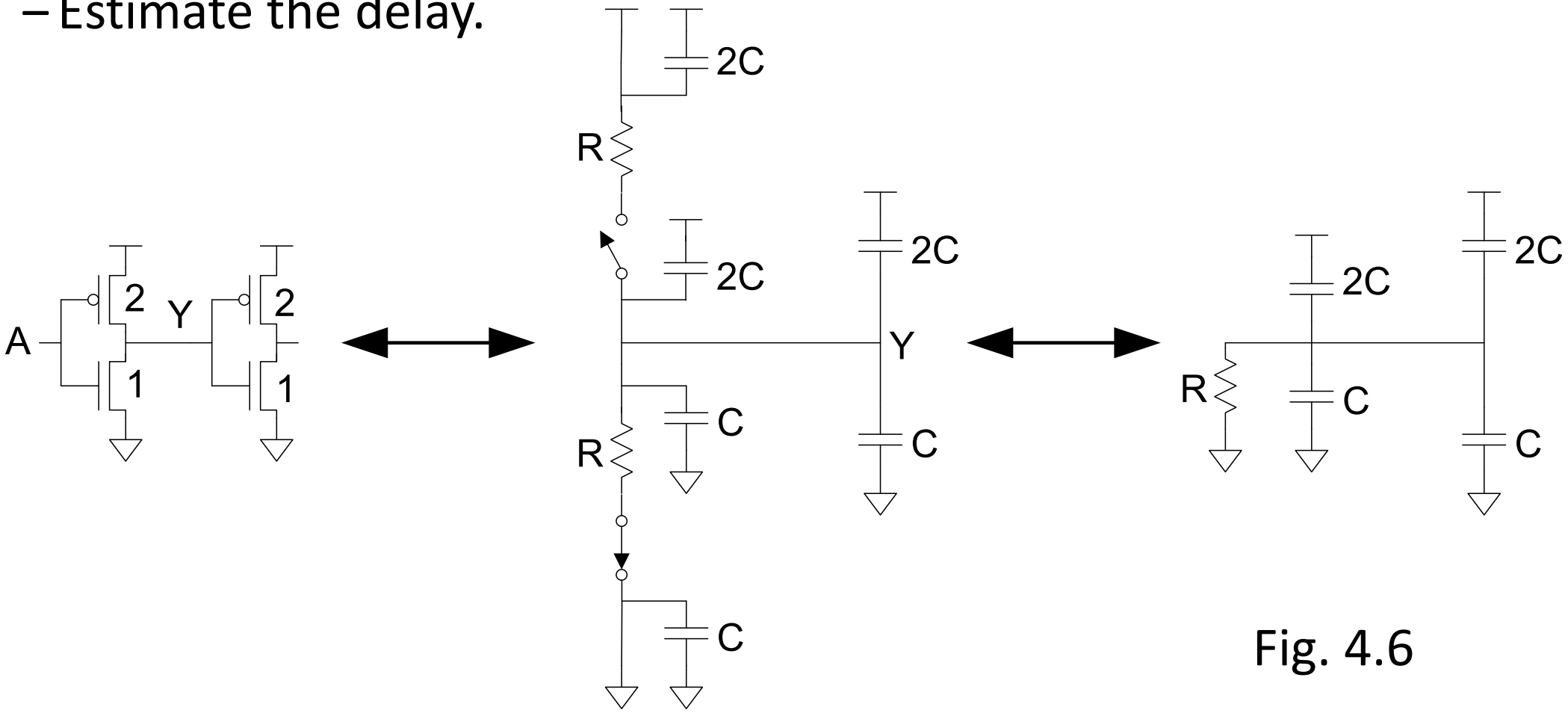


Fig. 4.6

4.3. RC delay model (4)

- Example 4.2
  - Consider a 3-input NAND gate.
  - What is the effective resistance?

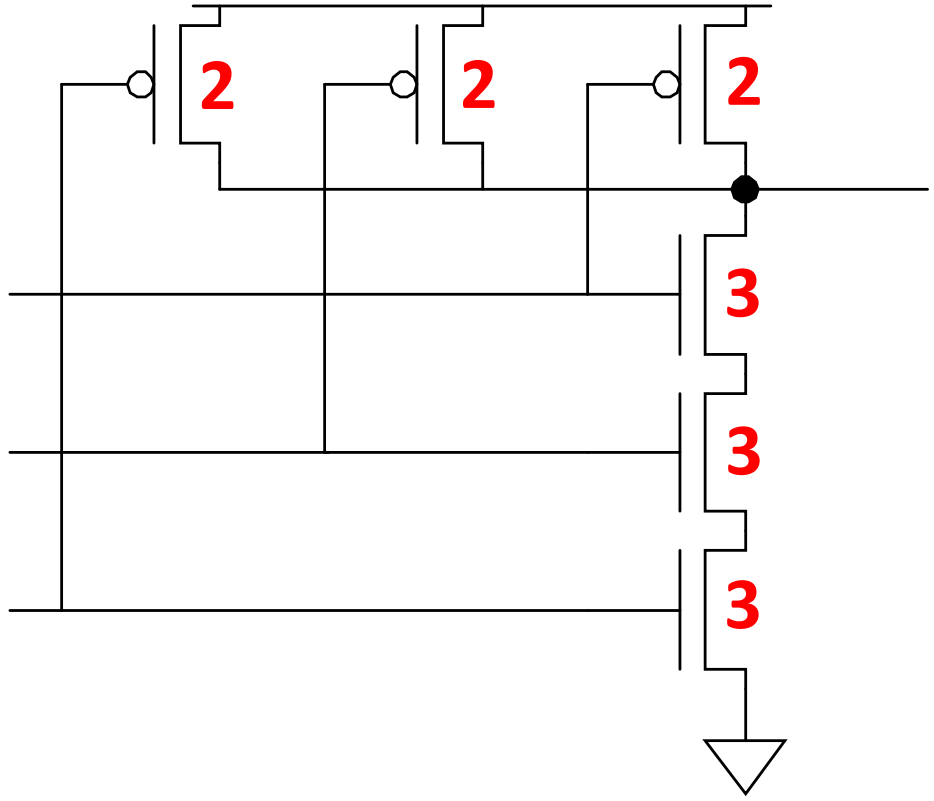


Fig. 4.7(a)

4.3. RC delay model (5)

- Anotate the gate with its gate and diffusion capacitances.

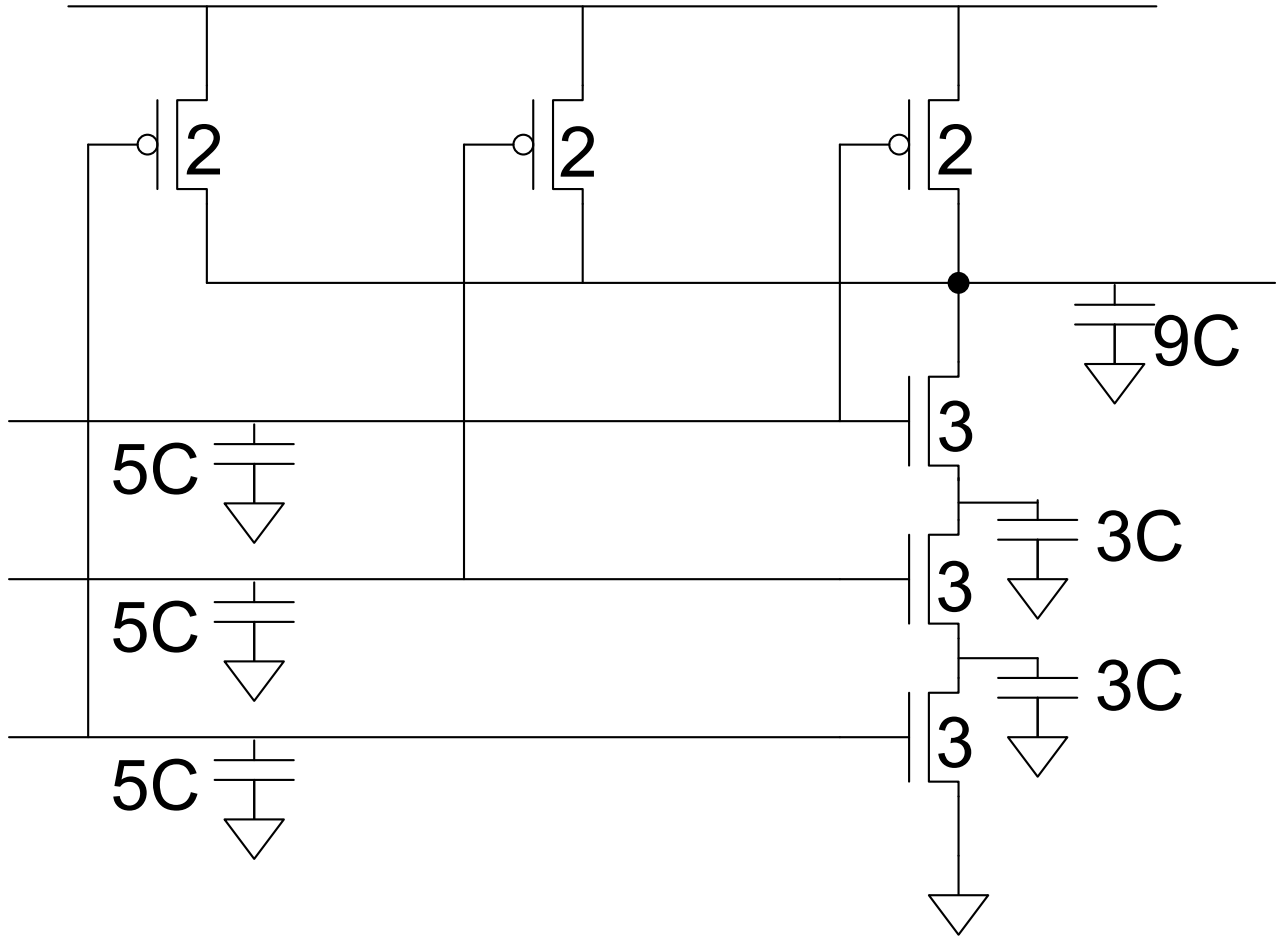


Fig. 4.7(c)

4.3. RC delay model (6)

- Example 4.4
  - Estimate t_{pd} for a “unit” inverter (PMOS width:NMOS width=2:1 & minimum length) driving identical “unit” inverters.
  - Effective resistance is R. (Same for NMOS and PMOS)
  - Capacitance is $(3 + 3m)C$.

$$t_{pd} = (3 + 3m)RC$$

4.3. RC delay model (7)

- Example 4.5
  - The driver is w times unit size.
  - The effective resistance is $\frac{R}{w}$ and the diffusion capacitance is wC.
  - Estimate t_{pd}.

$$t_{pd} = \left(3 + 3\frac{m}{w}\right) RC$$

  - With a fanout of $h = \frac{m}{w}$,

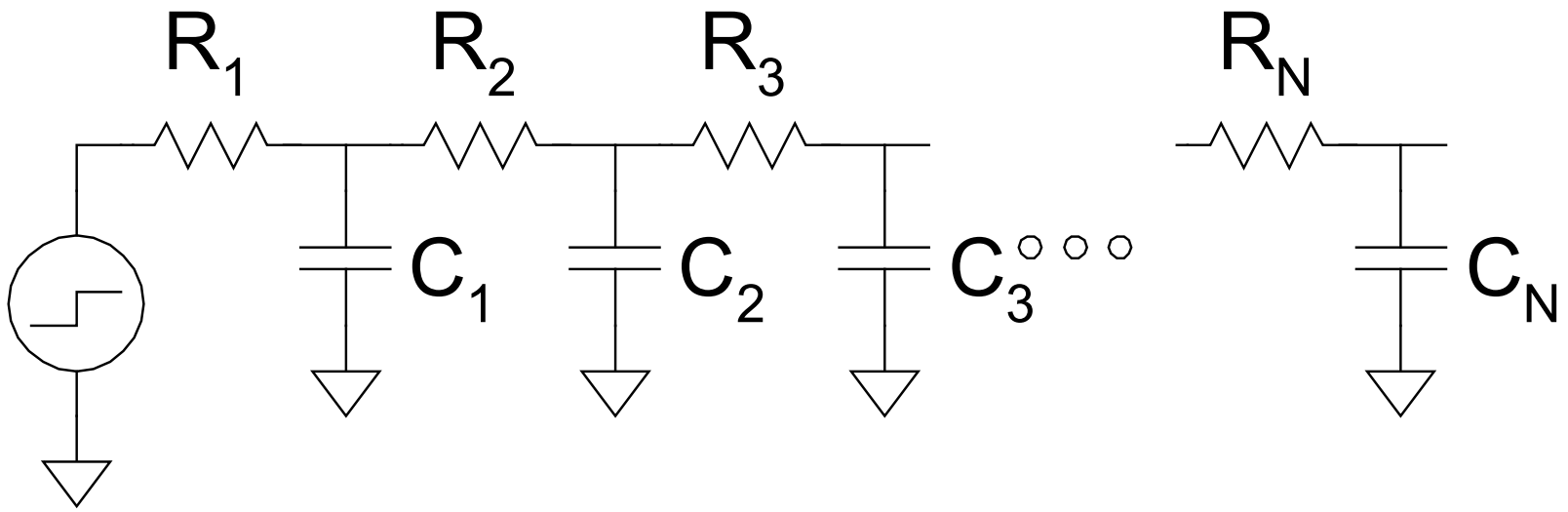
$$t_{pd} = (3 + 3h)RC$$

4.3. RC delay model (8)

- A chain of R and C
  - A simple single time constant approximation

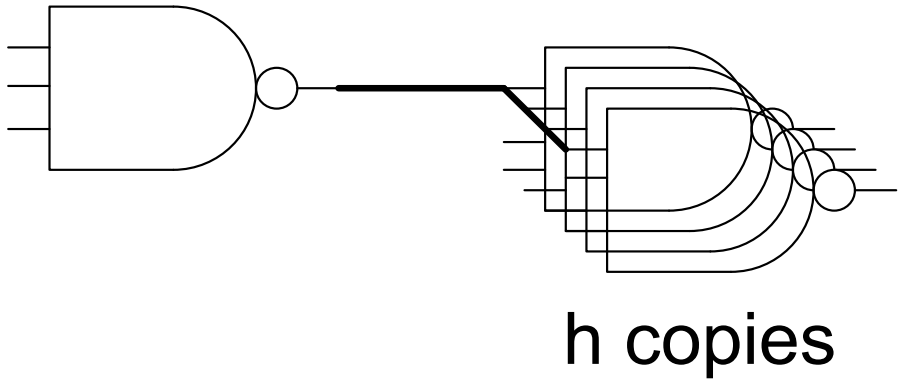
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

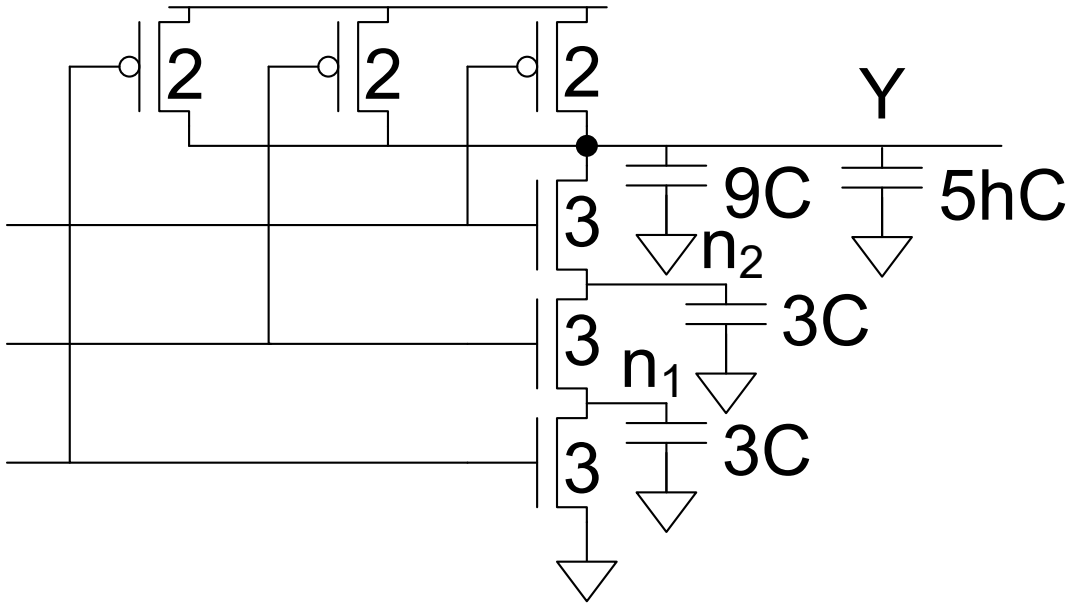
$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$



4.3. RC delay model (9)

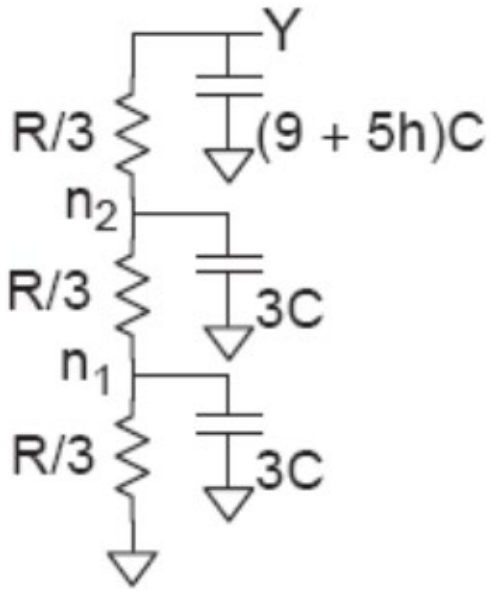
- Example 4.7 (h identical NANDs)
  - We studied it in Example 4.2.





4.3. RC delay model (10)

- For the falling transition
  - Estimate t_{pdf}.
- For the rising transition (in the worst case)
  - Estimate t_{pdr}.



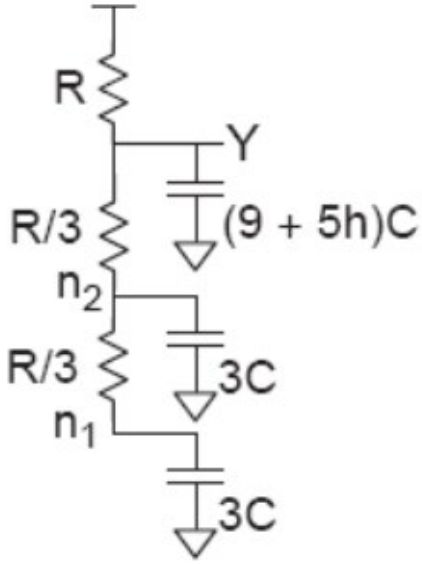
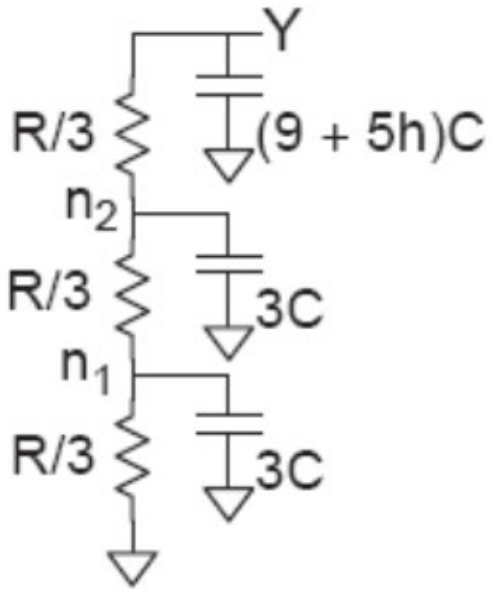


Fig. 4.15

4.3. RC delay model (11)

- For the falling transition
  - Estimate t_{pdf}.
- For the rising transition (in the worst case)
  - Estimate t_{pdr}.



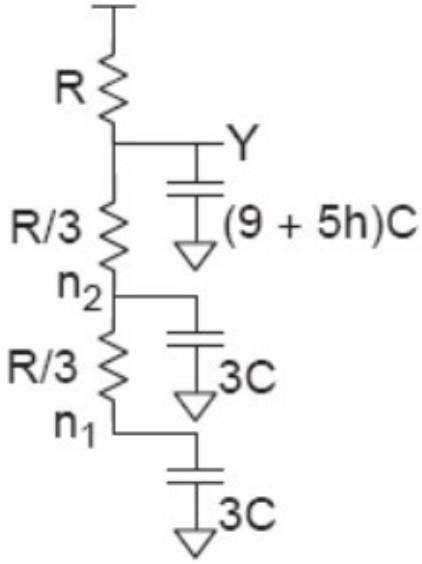


Fig. 4.15

4.3. RC delay model (12)

- Delay components
  - *Parastic delay*: Time for a gate to drive its own internal diffusion capacitance
  - *Effort delay*: It depends on the ratio of external load capacitance to input capacitance.
  - The normalized delay, $d = \frac{t_{pd}}{3RC}$, can be written as

$$d = parastic\ delay + effort\ delay$$

4.3. RC delay model (13)

- Layout dependence of capacitance
  - A good layout minimizes the diffusion area.

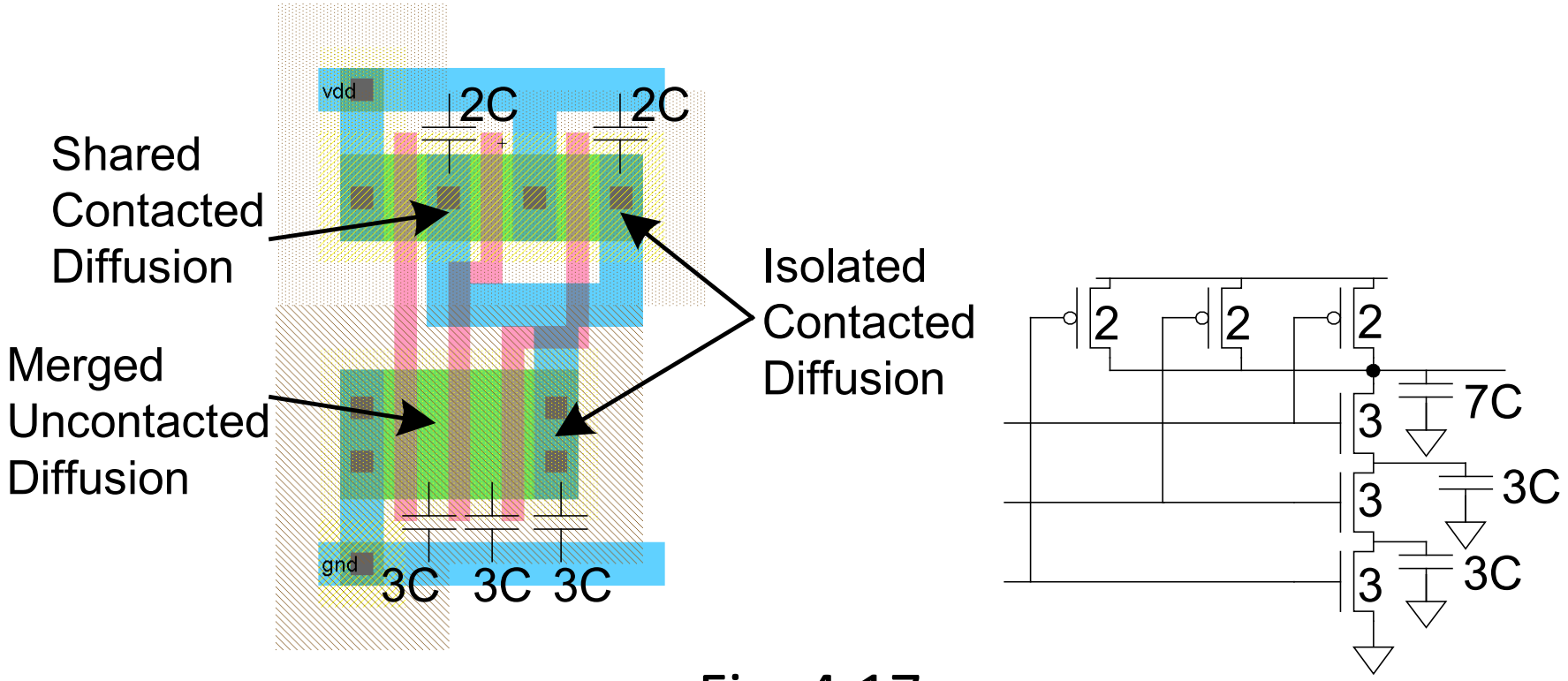


Fig. 4.17

Thank you!