Digital Integrated Circuit
Lecture 25 Array Subsystems

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Review of Previous Lecture

Lecture 24

- Latches and flip-flops
  - They can be used in sequencing static circuits.
  - A latch can be implemented with a transmission gate. Of course, for desirable properties (Input connected to the MOS gate, static latch, immunity to the output noise)
  - A flip-flop can be implemented by a pair of back-to-back latches.

12.1 Introduction

12.1. Introduction (1)

- Memory arrays

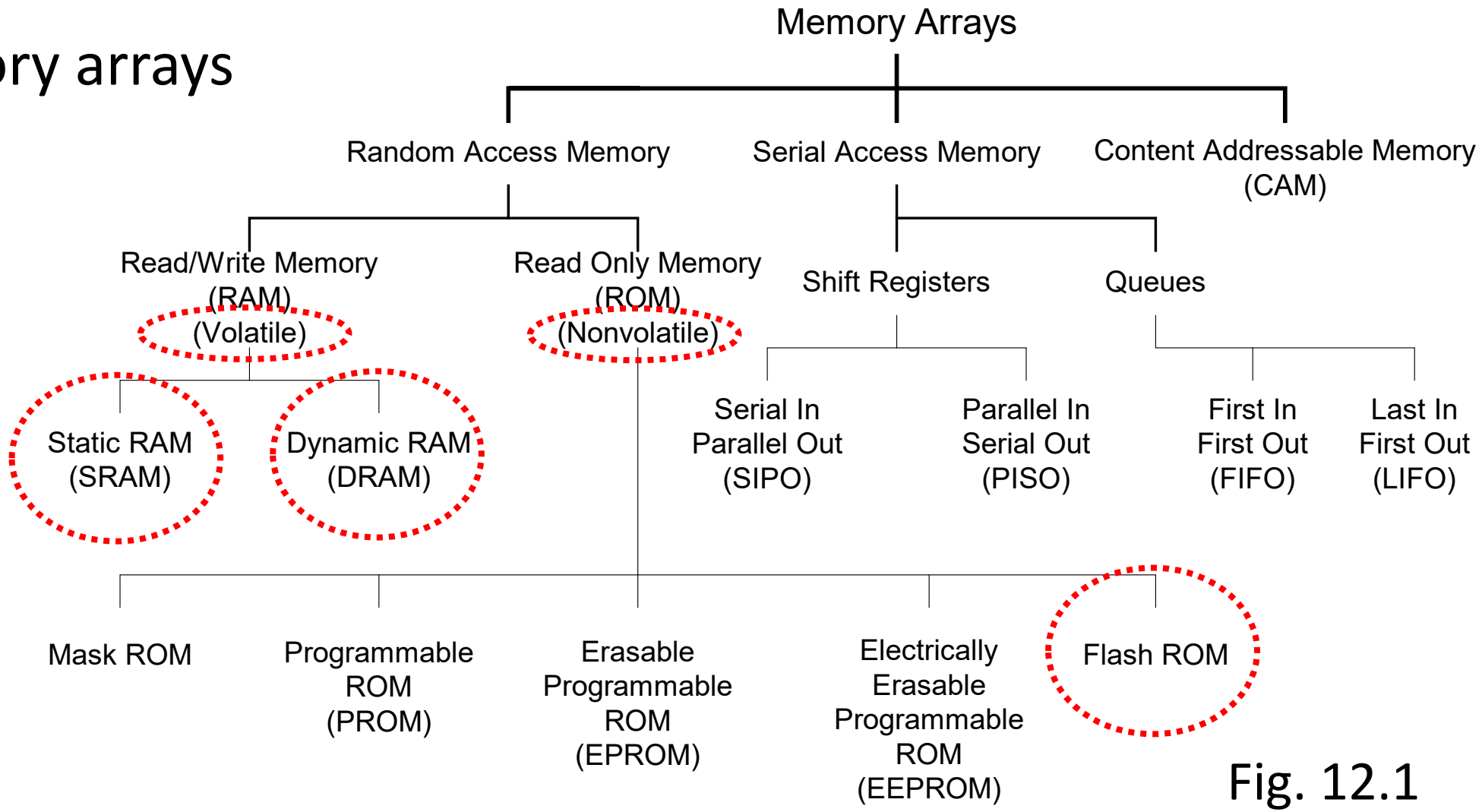


Fig. 12.1

12.1. Introduction (2)

- In volatile memories (RAMs),
  - There are *static* structures and *dynamic* structures.
  - SRAM: Static cells use some form of feedback to maintain their state.
  - DRAM: Dynamics cells use charge stored on a floating capacitor through an access transistor. Charge will leak away through the access transistor enven while the transistor is OFF. They must be periodically read and rewritten to refresh their state.
  - SRAMs are faster and less troublesome, but require more area per bit than DRAMs.

12.1. Introduction (3)

- Array architecture
  - Row decoder: It activates one of the rows by asserting the wordline.

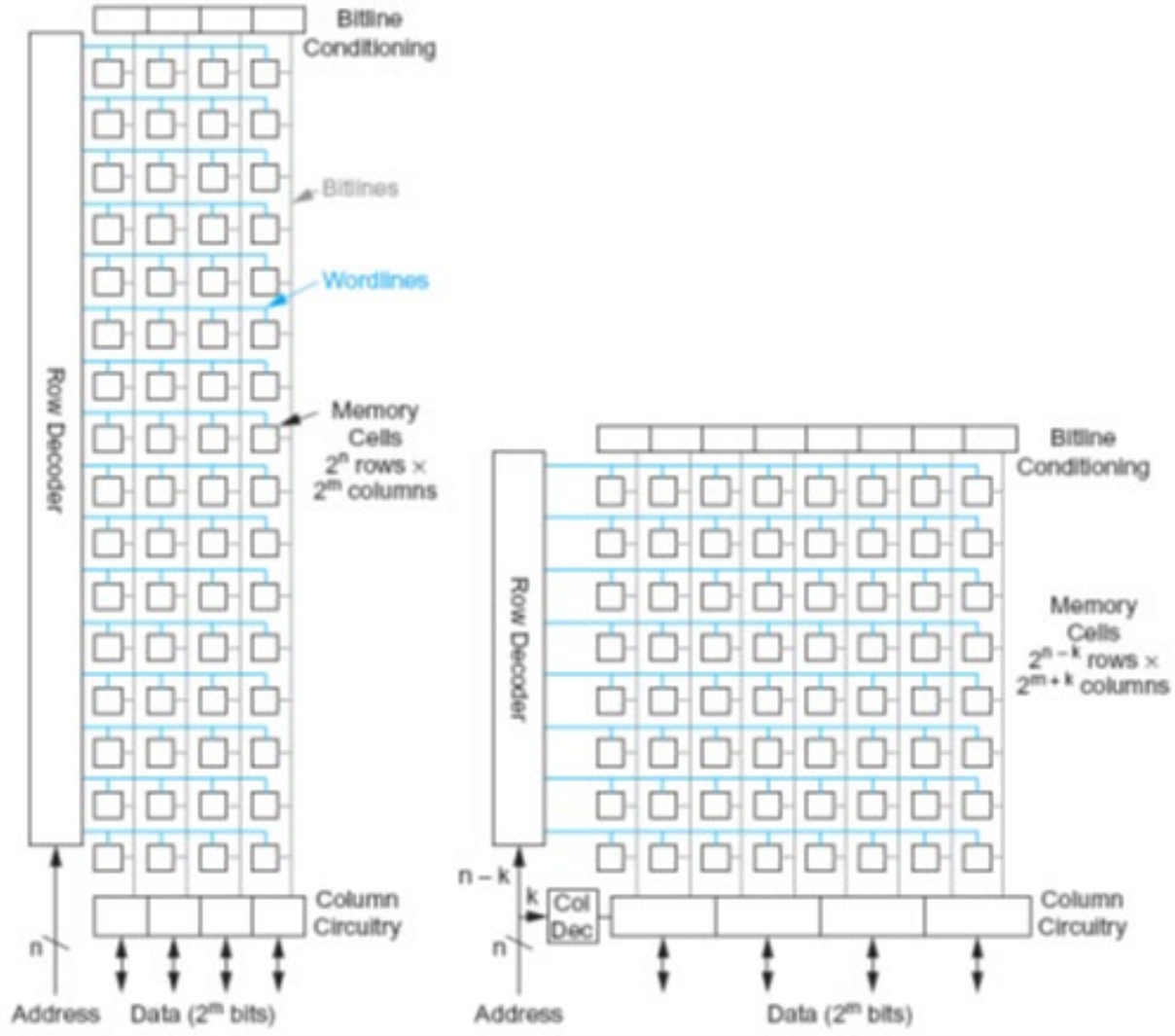


Fig. 12.2

12.2 SRAM

12.2. SRAM (1)

- Attractive properties
  - Denser than flip-flops
  - Compatible with standard CMOS processes
  - Faster than DRAM
  - Easier to use than DRAM

12.2. SRAM (2)

- 6T SRAM cell
  - It achieves its compactness at the expense of more complex peripheral circuitry for reading and writing the cells.
  - It contains a pair of weak cross-coupled inverters holding the state.
  - It contains a pair of access transistors to read or write the state.

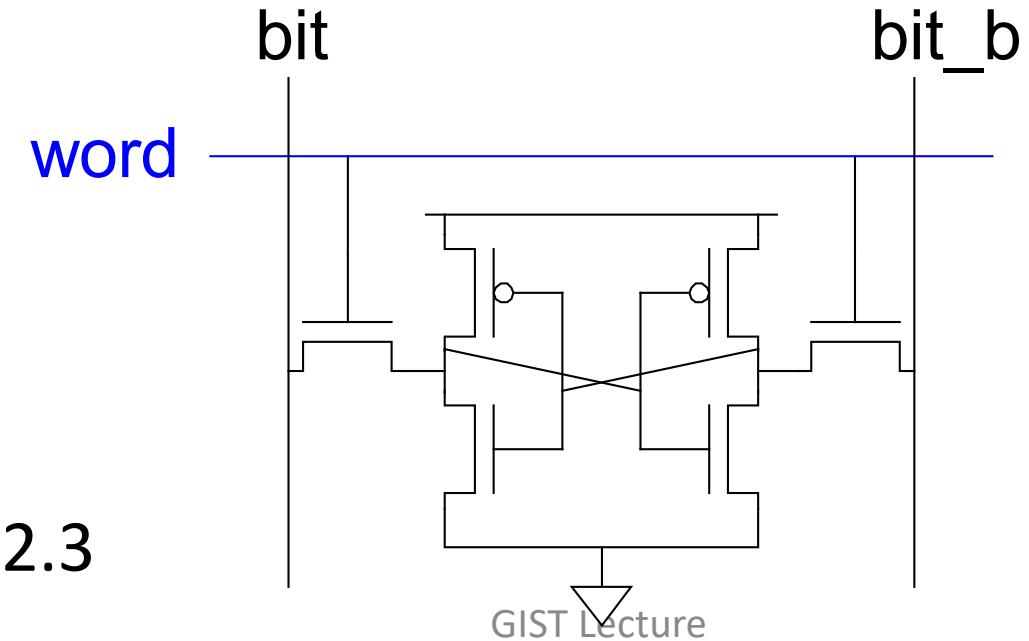
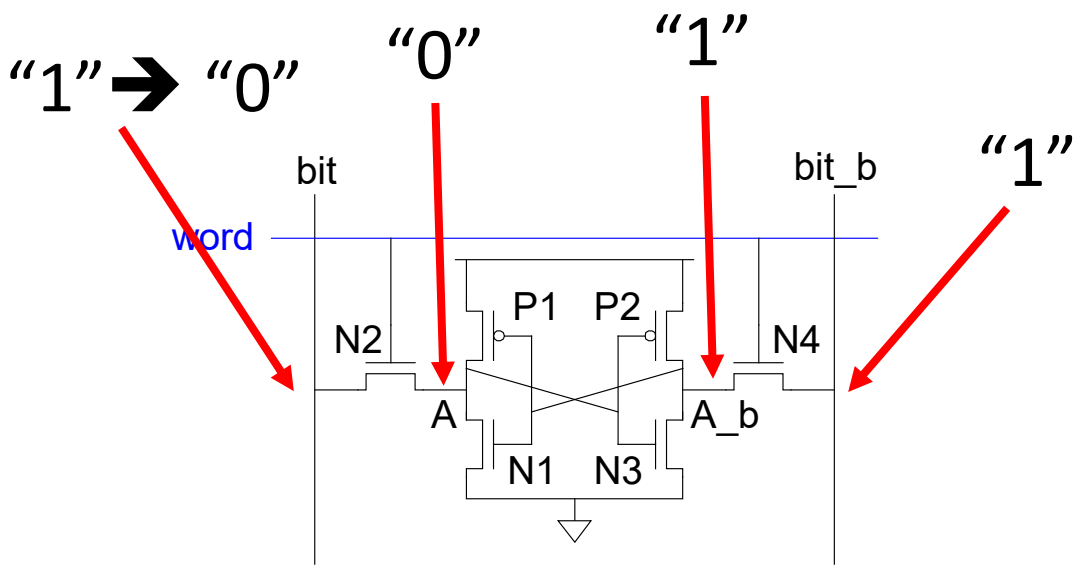
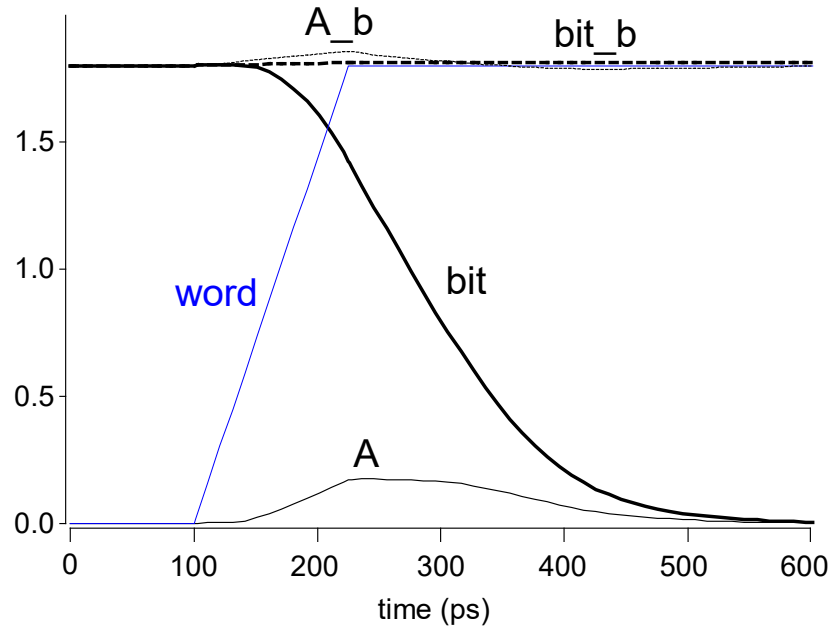


Fig. 12.3

12.2. SRAM (3)

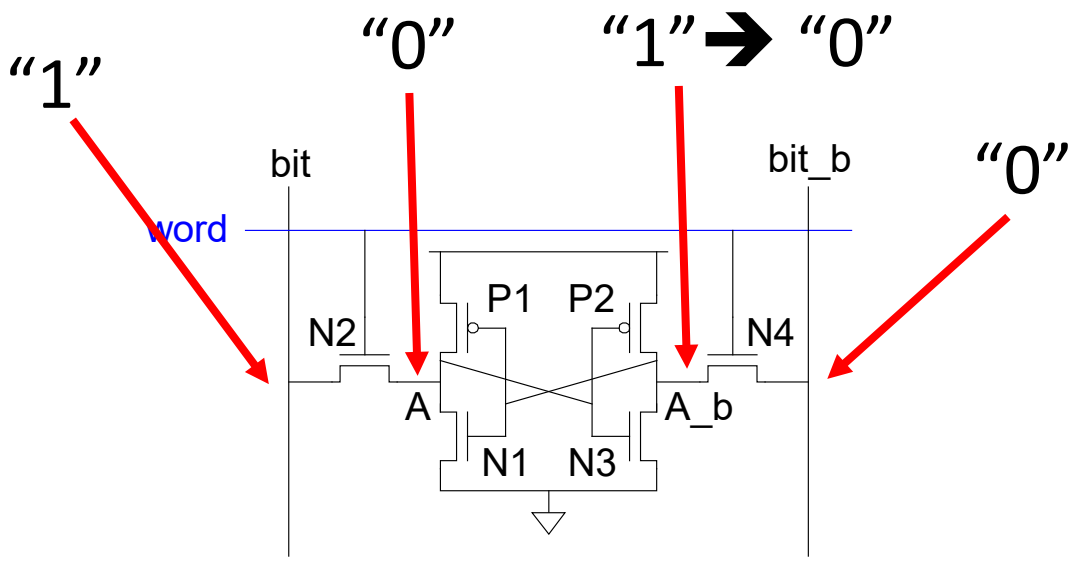
- READ
  - The bitlines are both initially floating high.
  - Then, the wordline is raised.
  - One of the two bitlines will be pulled down by the cell
  - Read stability, N1 >> N2

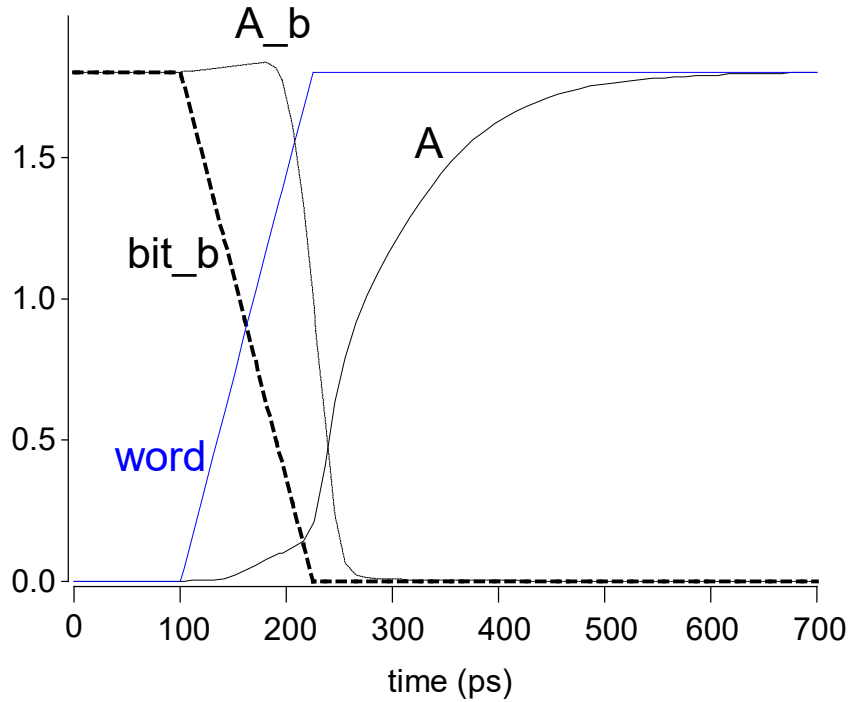




12.2. SRAM (4)

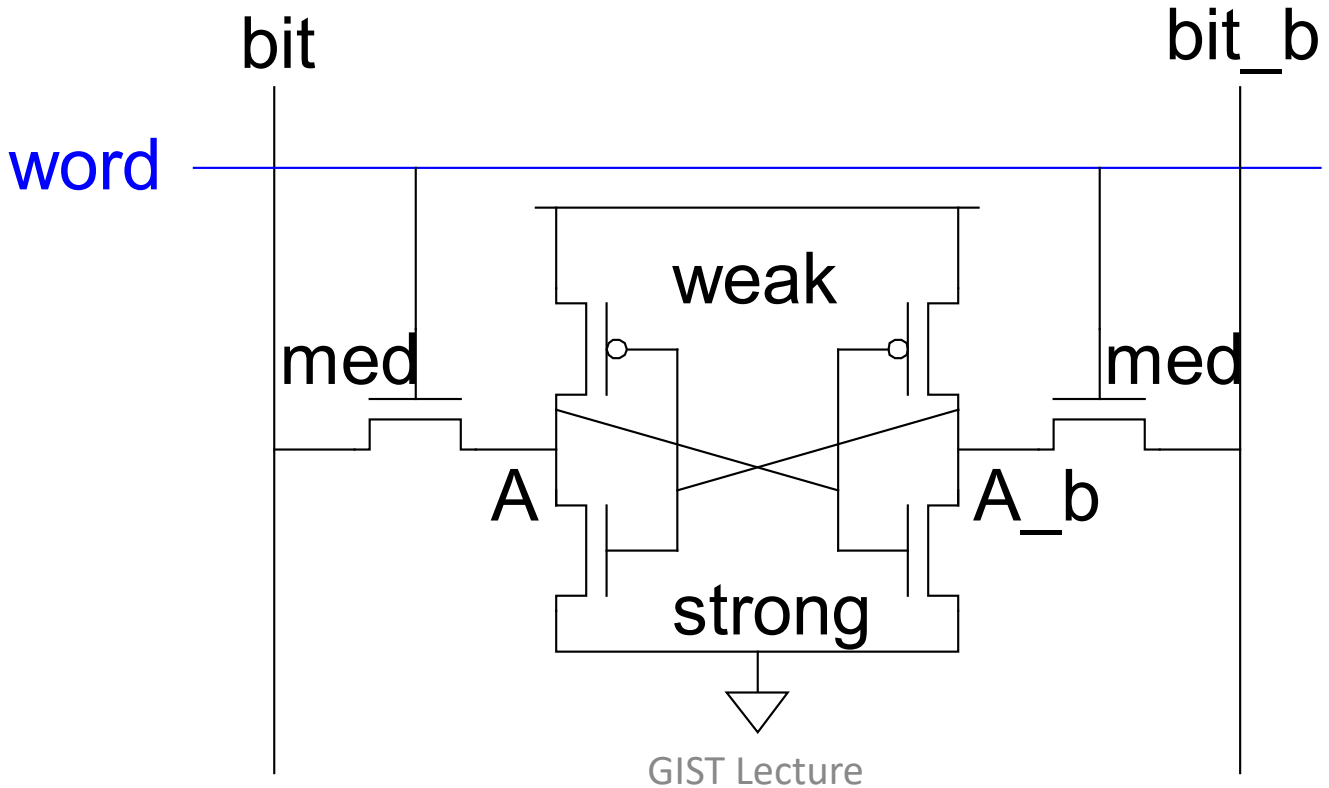
- WRITE
  - One bitline is precharged high and left floating. the other low
  - Then, the wordline is raised.
  - Bitlines overpower cell with new value
  - Writability, N4 >> P2





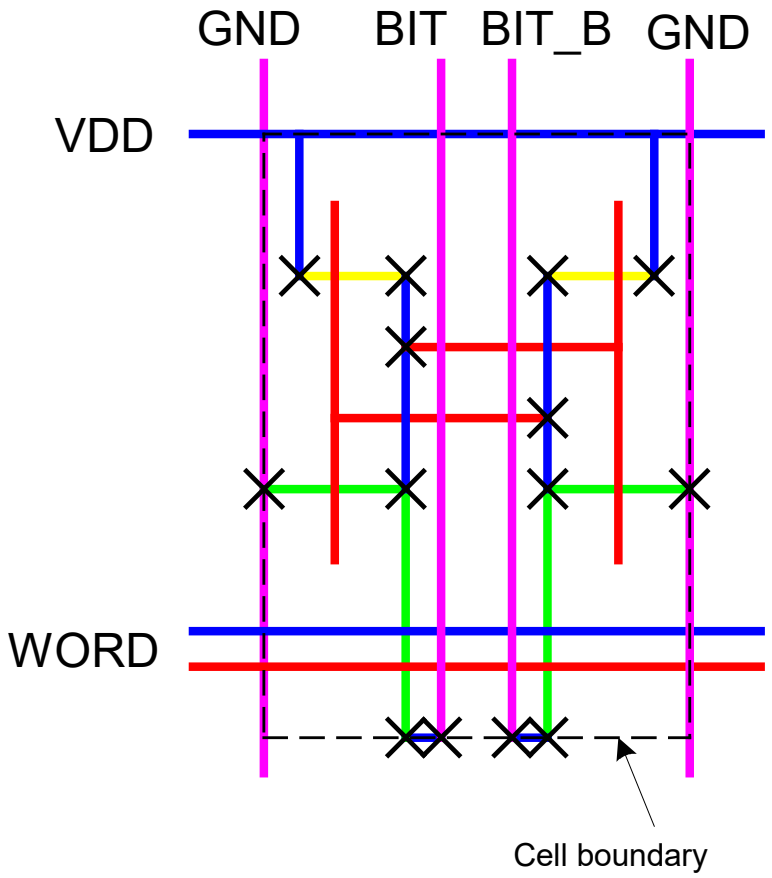
12.2. SRAM (5)

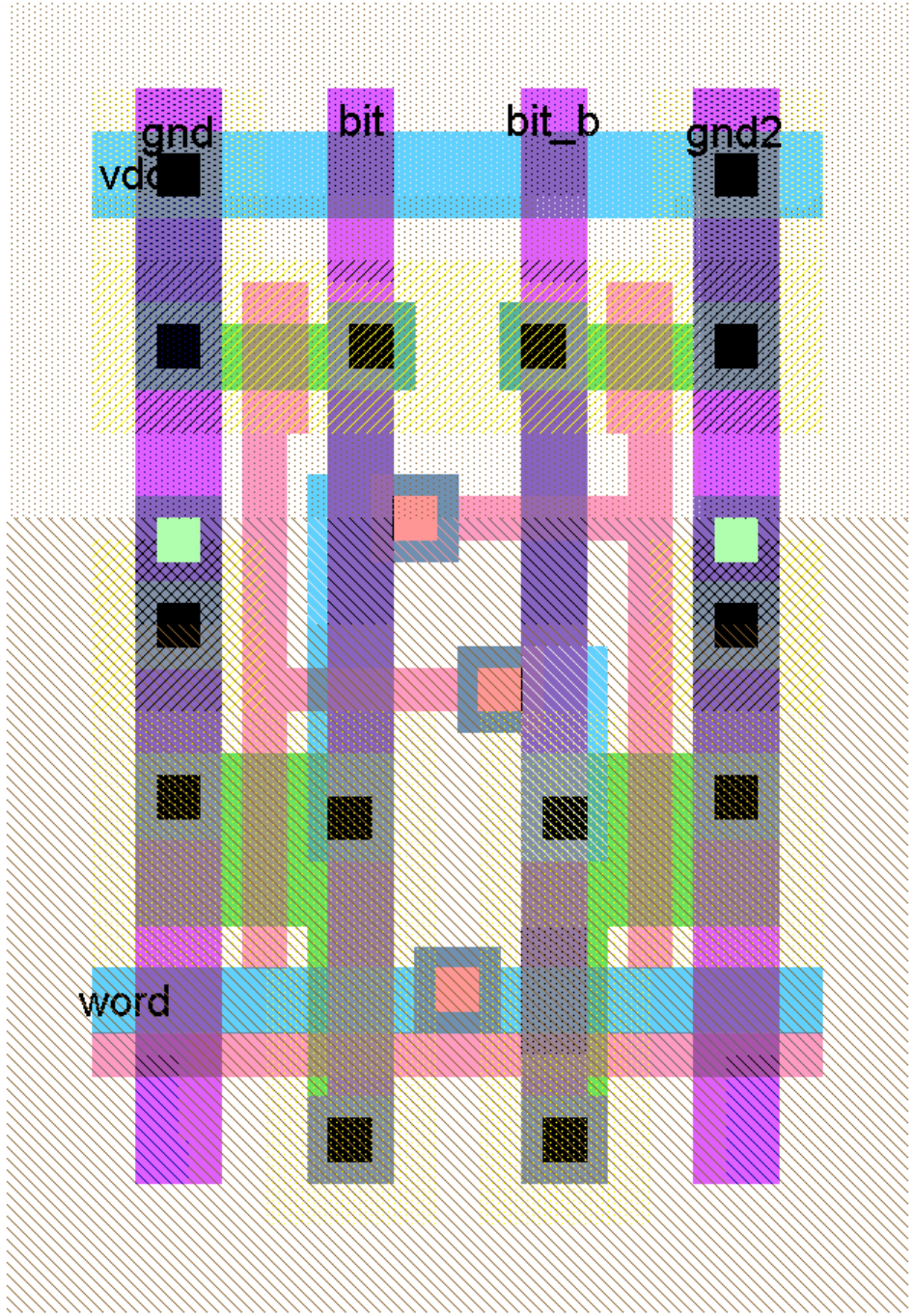
- SRAM sizing
  - To ensure both read stability and writability, the transistors must satisfy ratio constraints.



12.2. SRAM (6)

- SRAM layout
  - Find out transistors.





12.2. SRAM (7)

- Another SRAM layout
  - Find out transistors.

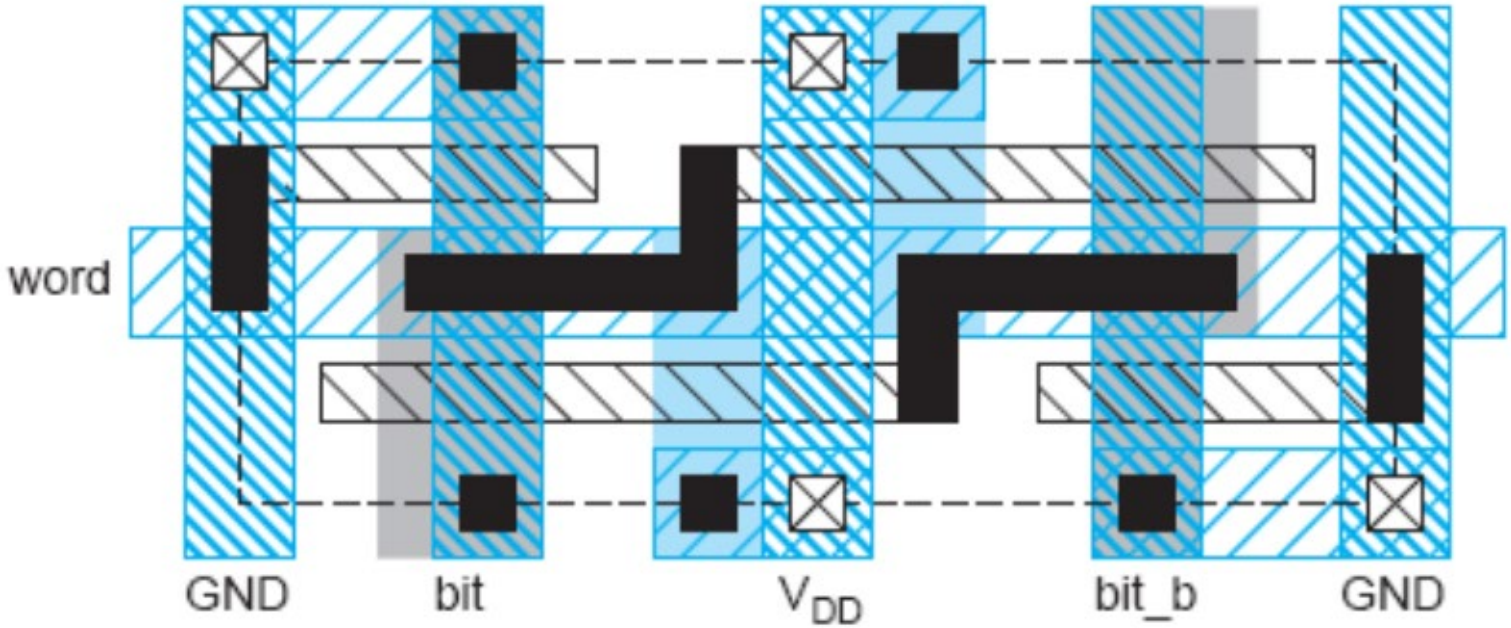


Fig. 12.15

12.2. SRAM (8)

- Commercial SRAMs
  - Five generations of Intel SRAM cell

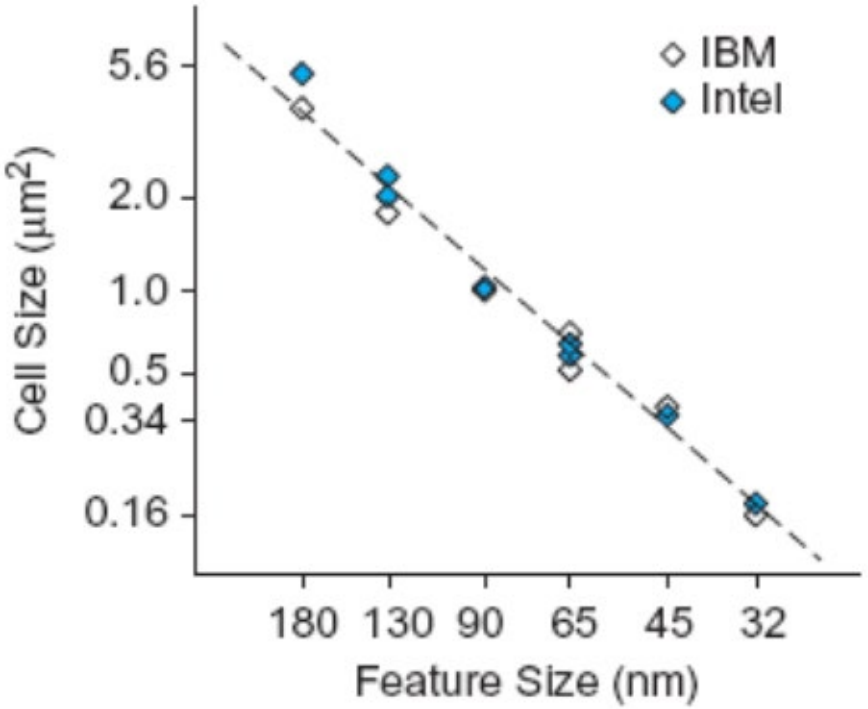


Fig. 12.17

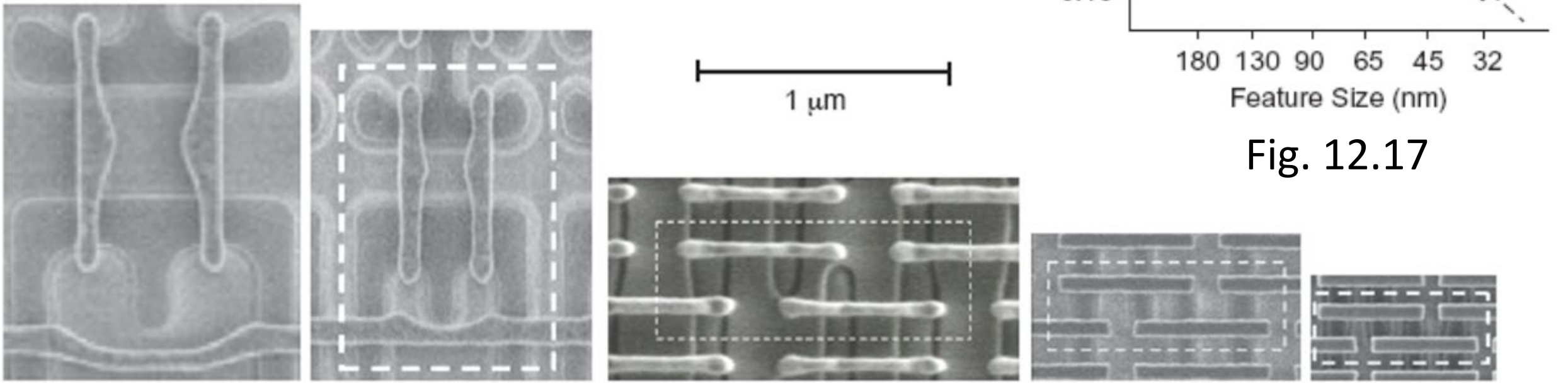
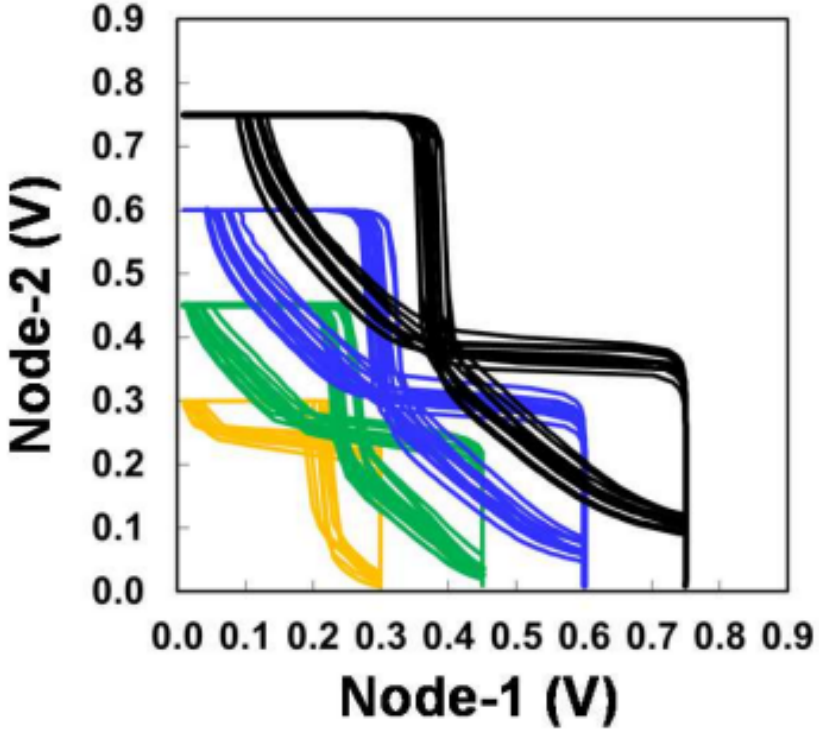


Fig. 12.16

12.2. SRAM (9)

- The latest SRAM (TSMC 3 nm technology, N3E, @ IEDM 2022)
  - Its area is 0.021 μm^2.
  - The SNM (static noise margin) of 97 mV and 124 mV are achieved for 0.45 V and 0.6 V operation, respectively.



(Taken from TSMC's IEDM 2022 paper)

Thank you!