Special Topics on Basic EECS I Design Technology Co-Optimization

Lecture 6

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L6

How to fabricate a FinFET

- High volume manufacturing (HVM) of FinFETs
  - Which companies can do it?
  - As of 2025, only a few companies remain:
  - TSMC (Taiwan): Leading foundry. N3 FinFET
  - Intel (US): Intel 3 (their last FinFET node)
  - Samsung (South Korea): No. 2 foundry. SF4
  - SMIC (China): Reportedly 7 nm without EUV
  - GlobalFoundries (US): Stopped at 12 nm FinFET. No further scaling
- Unfortunately, we don’t have a facility to fabricate it.

AngstromCraft

- Process emulator developed for this course (Still under development)
  - Type `angstromcraft YOUR_INPUT_FILE`
  - As a starter kit, `taecho.cmd` is prepared.

```
craft
(name="craft",lx=162,ly=288,lz=400,region="DeepS
ubstrate",thickness=1,cgns="taecho.cgns") {
   depo (region="Substrate",thickness=9)
}
```

Spec & body

- Simple grammar used in AngstromCraft (and G-Device).
  - Each statement must have the following form:

```
statement (spec) { body }
```

  - Example) For the previous statement,

```
craft
```
← statement

```
name="craft",lx=162,ly=288,lz=400,region="DeepSu
bstrate",thickness=1,cgns="taecho.cgns"
```
← spec

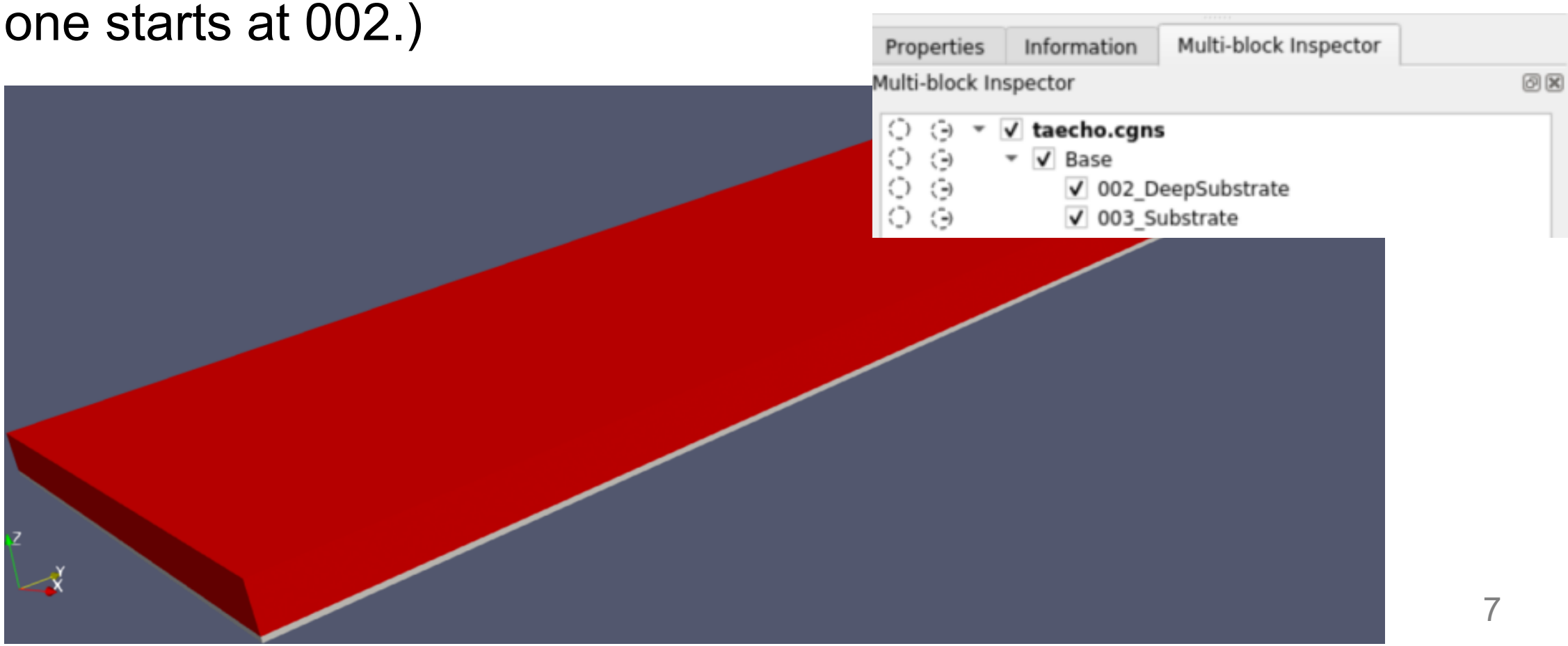
```
depo (region="Substrate",thickness=9)
```
← body

Meaning of the previous spec & body

- Create a craft object.
  - We can set its name: `name="craft"`
  - We can set the domain size: `lx=162,ly=288,lz=400`
  - We can set the very first (uniform in the xy plane) region: `region="DeepSubstrate",thickness=1`
  - We can set the output file: `cgns="taecho.cgns"`
- Deposition
  - We can set its name: `region="Substrate"`
  - We can set its thickness: `thickness=9`
- Now, we can expect two regions.

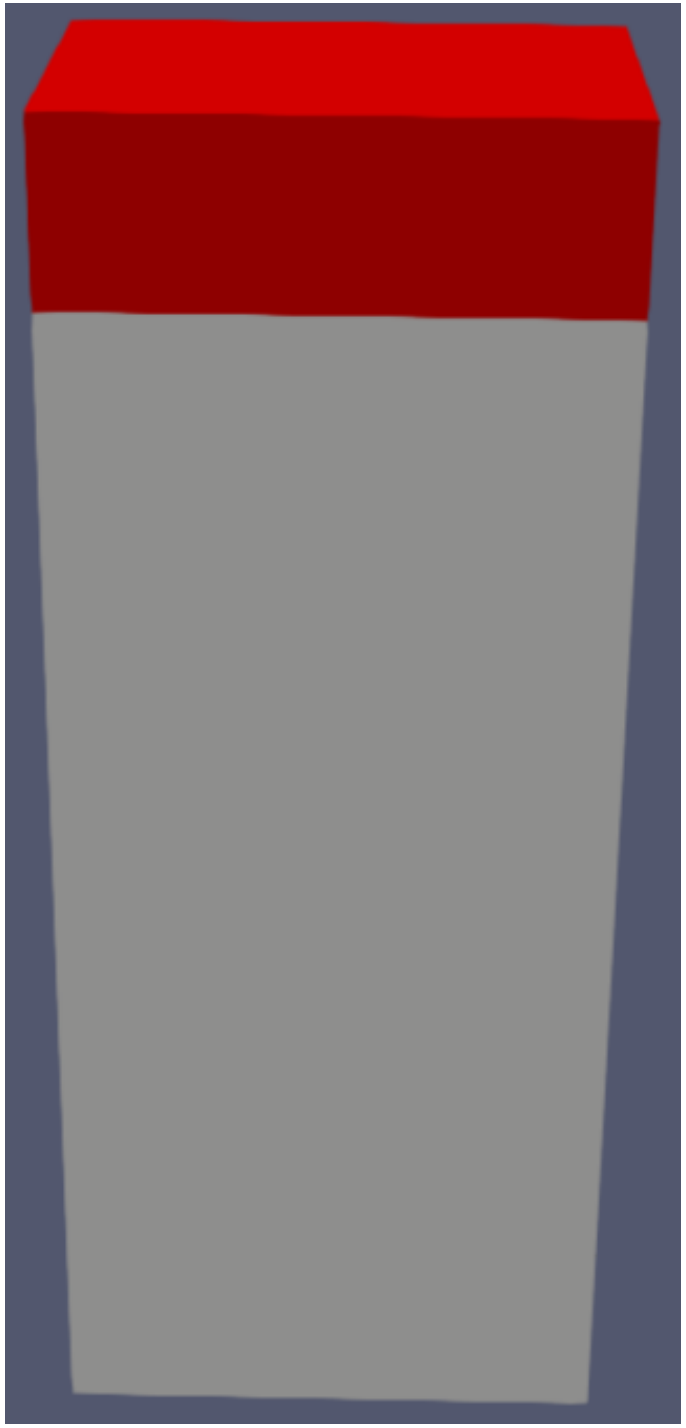
Screenshot of `taecho.cgns`

- It works, as expected.
  - Two regions (For some reasons, they are numbered. The first one starts at 002.)



Change some parameters.

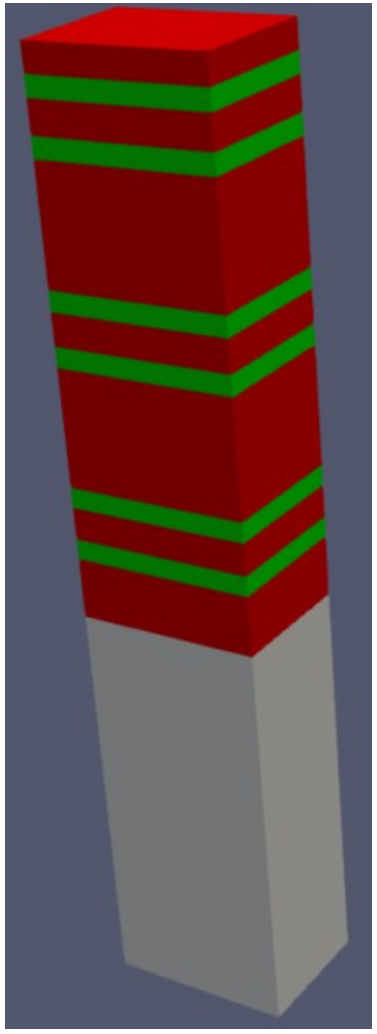
- Try this:
  - Smaller system size:
    `lx=46,ly=34,lz=450`
  - Much thicker initial region:
    `region="Si_Bulk",thickness=100`
  - Different output file name:
    `cgns="threetier.cgns"`
  - The second region:
    `region="SiGe",thickness=15`



Si/SiGe multilayer structure

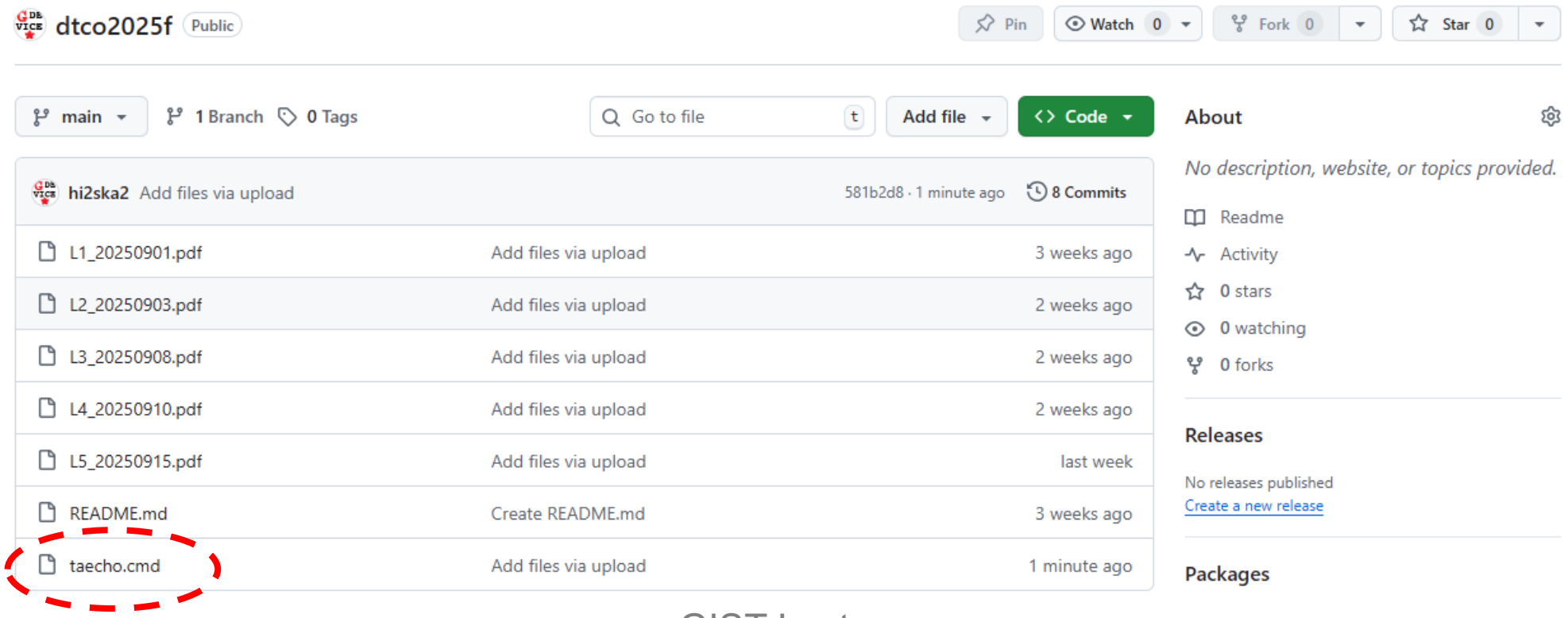
- Basic building block to fabricate multi-stacked nanosheet transistors
  - Try these sequential depositions as the body:

```
depo (region="SiGe",thickness=15)
depo (region="Si"  ,thickness=5)
depo (region="SiGe",thickness=8)
depo (region="Si"  ,thickness=5)
depo (region="SiGe",thickness=29)
depo (region="Si"  ,thickness=5)
depo (region="SiGe",thickness=8)
depo (region="Si"  ,thickness=5)
depo (region="SiGe",thickness=29)
depo (region="Si"  ,thickness=5)
depo (region="SiGe",thickness=8)
depo (region="Si"  ,thickness=5)
depo (region="SiGe",thickness=7)
```



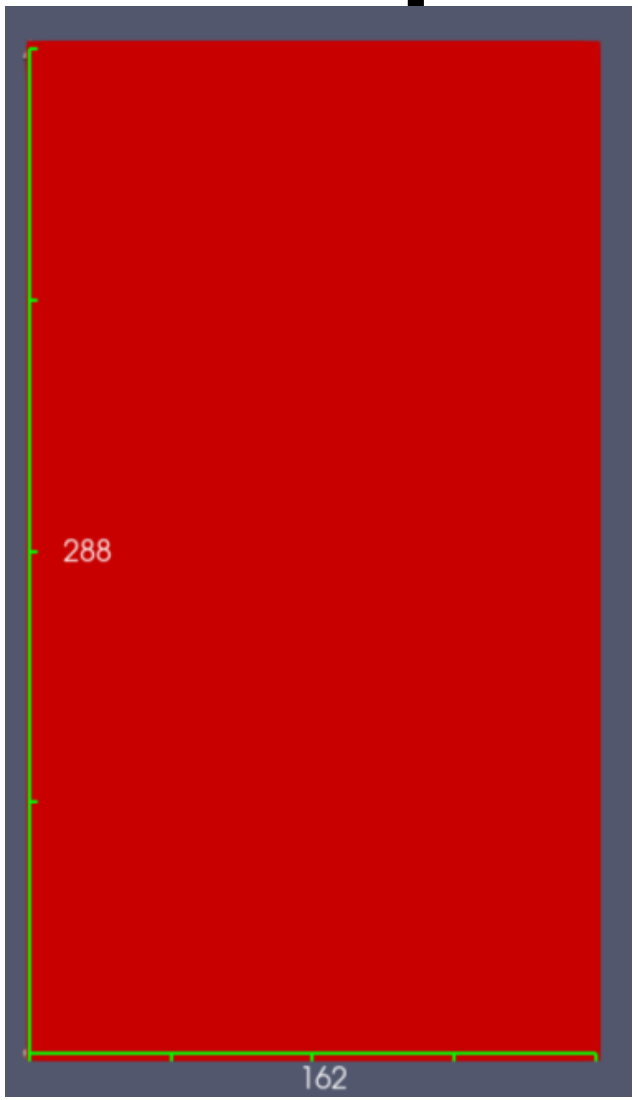
Exercise (It's not an official homework.)

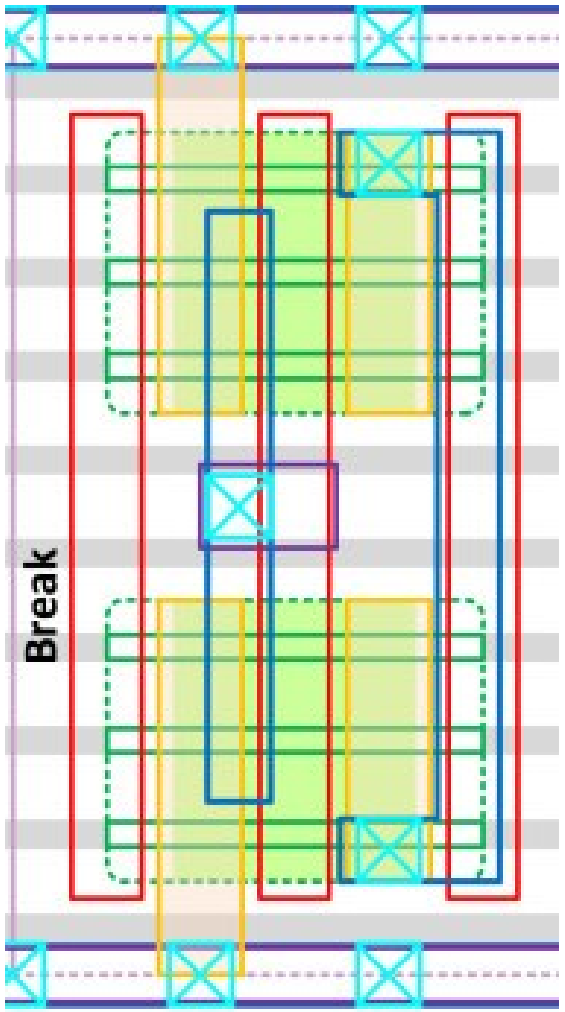
- You can find `taecho.cmd` in the GitHub repository.
  - Starting from this simplest file, create the three structures shown up to now.



Now, start an inverter example.

- We have fin pitch of 27 nm and CPP of 54 nm.
  - (For Intel 14 nm, fin pitch was 42 nm. CPP was 70 nm.)
  - (For TSMC 7 nm, fin pitch was 30 nm. CPP was 57 nm / 64 nm.)
  - Therefore, `lx=162,ly=288` means 3 CPPs and >10 fin pitches.





Inverter layout (ASAP7 PDK)

Thank you!