Special Topics on Basic EECS I Design Technology Co-Optimization

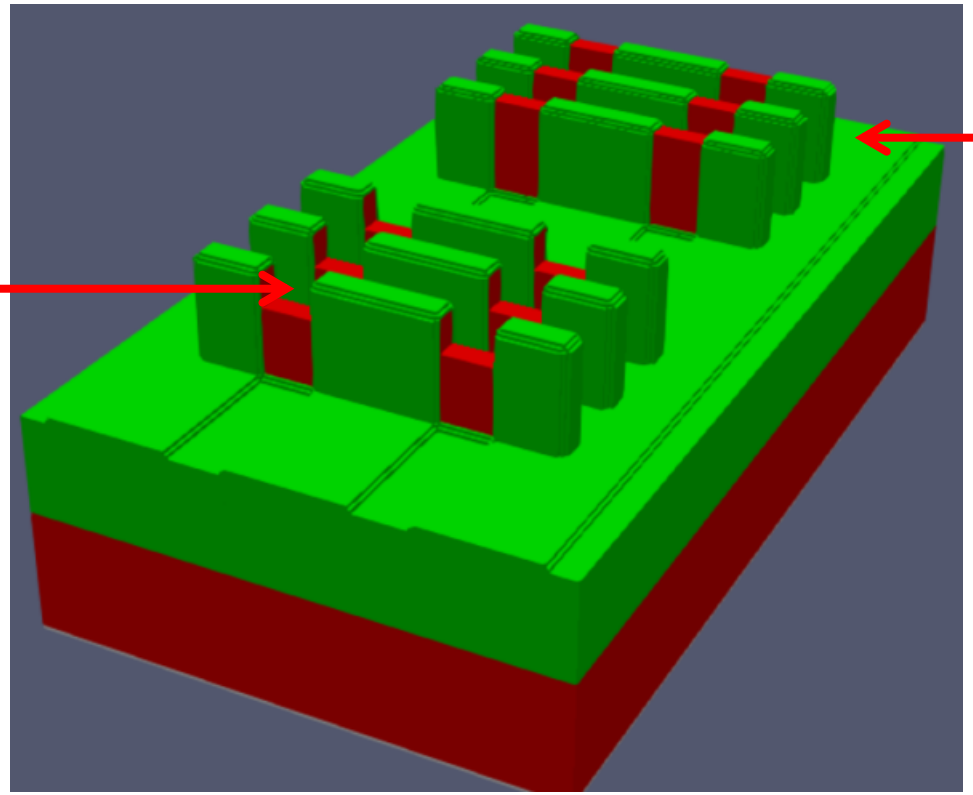
Lecture 14

Sung-Min Hong (smhong@gist.ac.kr)
Semiconductor Device Simulation Laboratory
Department of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology (GIST)

L14

NMOS cavity etch

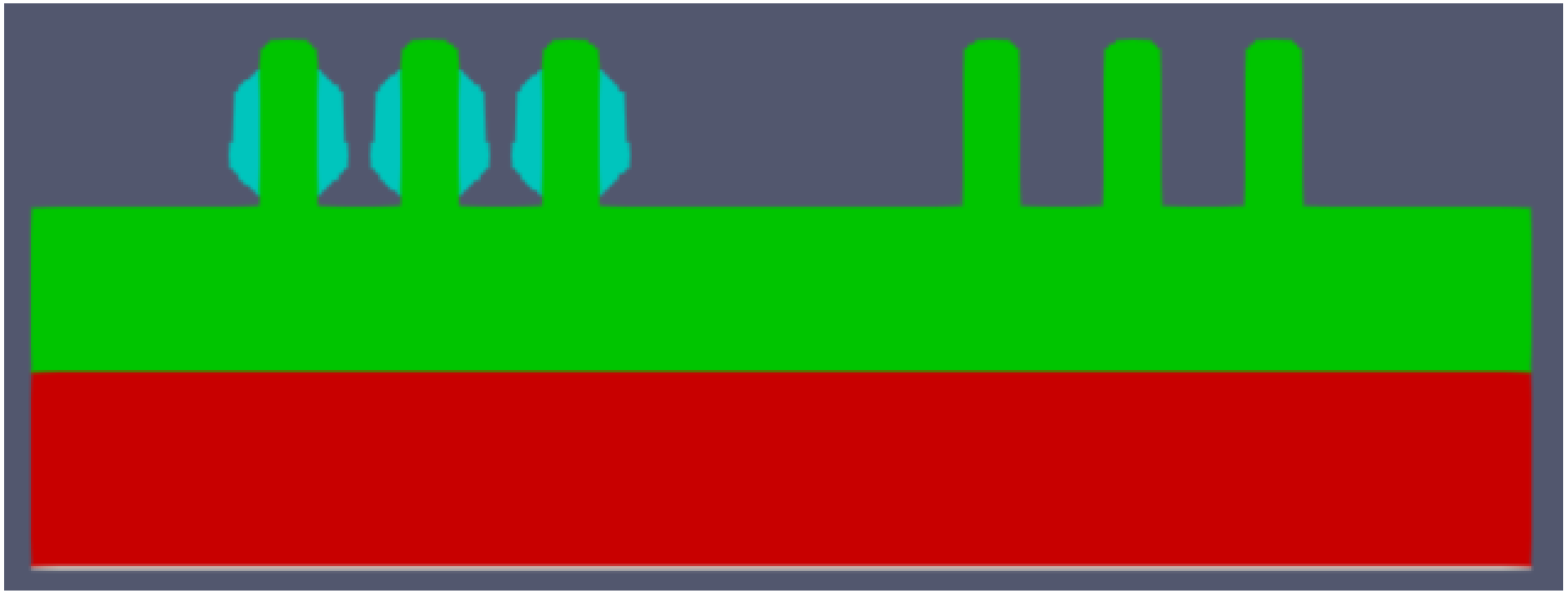
- First, prepare a mask for PMOS part
  - Then, etch the NMOS fins. Set the etch depth as 10 nm.



(Dummy gates, hard masks, spacers, and photoresists are not shown.)

NMOS S/D

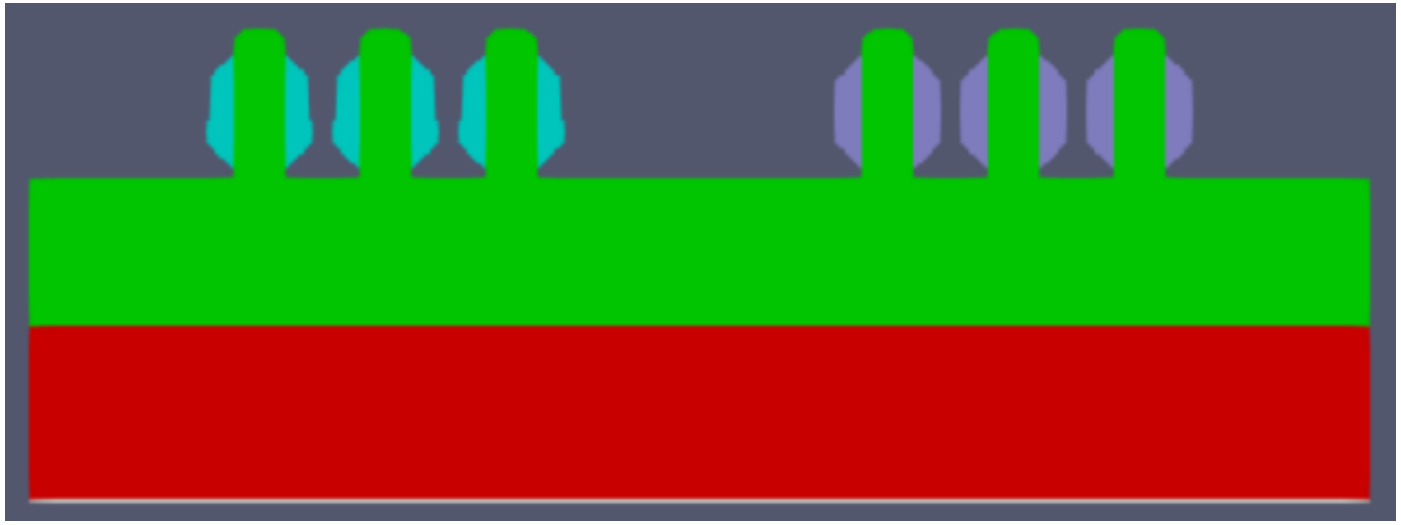
- Then, grow the epitaxial layer.
  - Keep the minimum distance between two fins. (In this example, 4 nm)

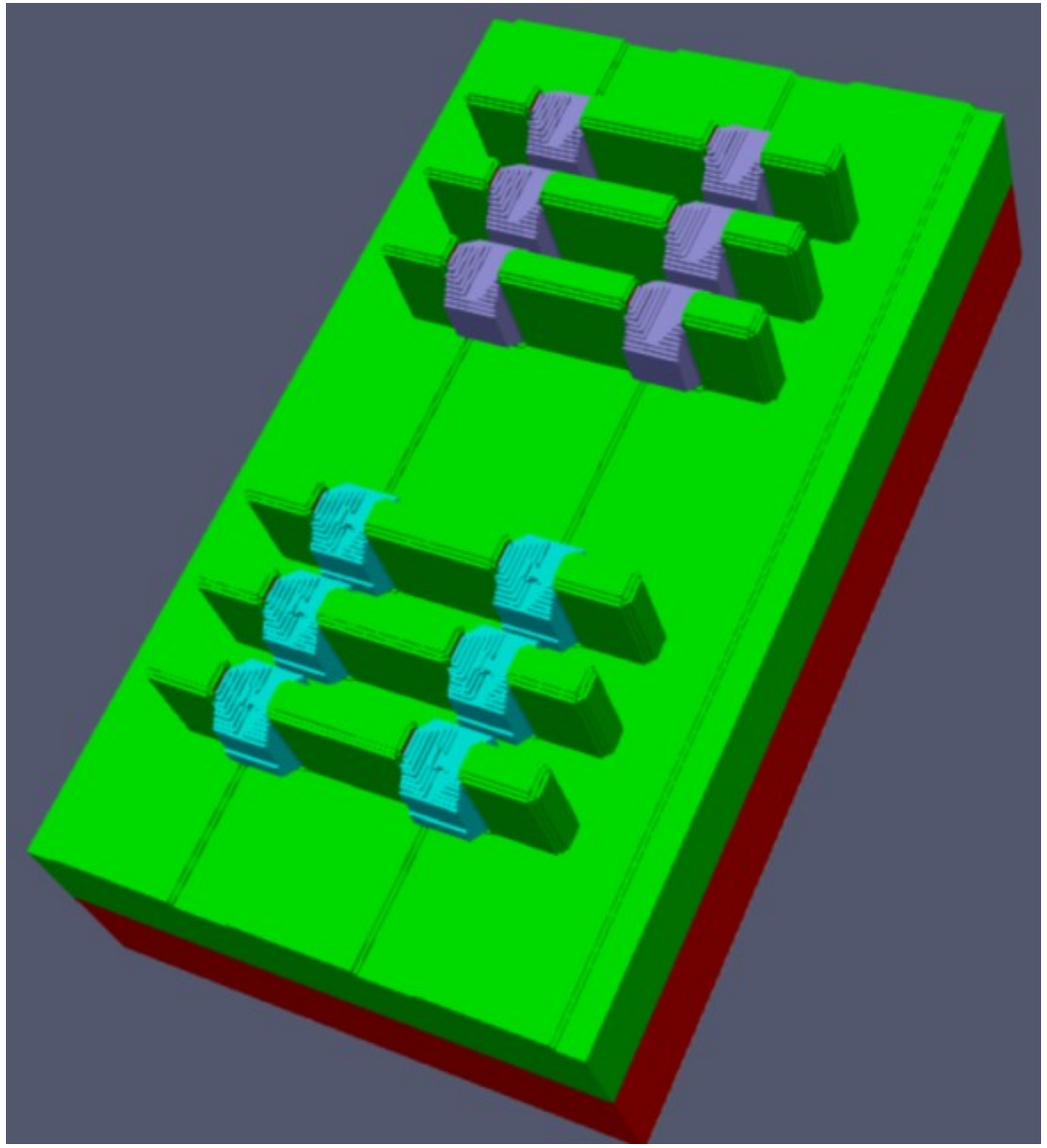


PMOS S/D

- A deeper cavity etch of 20 nm
  - Then, grow the SiGe epitaxial layer.
  - (Exact shapes may be different.)

NMOS PMOS

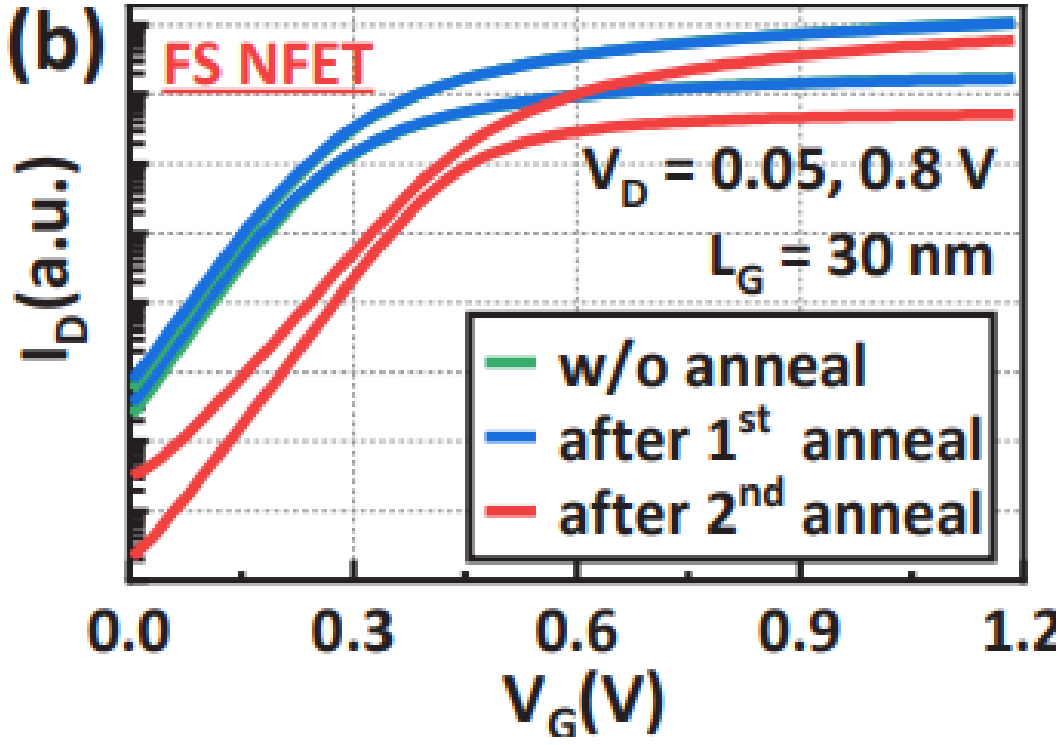




Thermal process

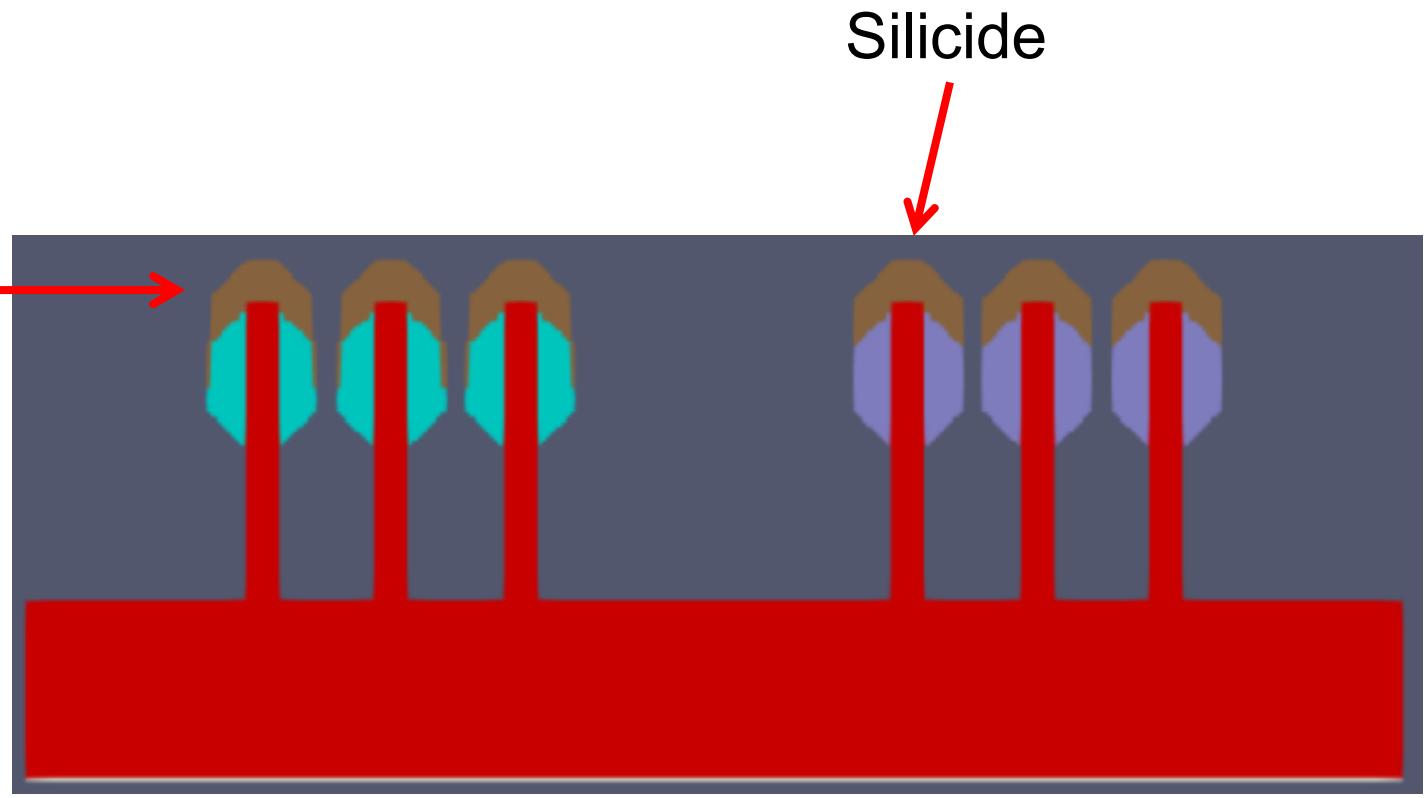
- Dopants must be activated.
  - Rapid thermal anneal (RTA)
  - High temperature, typically 950 ℃ ~ 1050 ℃
  - It must be performed before high-k/metal gate stack.

When 700 ℃ heat process is applied (the 2nd anneal), the device characteristics are heavily affected. (H. Wu et al., Peking University)



Salicide (self-aligned silicide)

- 10-nm-thick Ni deposition (anisotropic)
  - Then, anneal ➔ Silicide

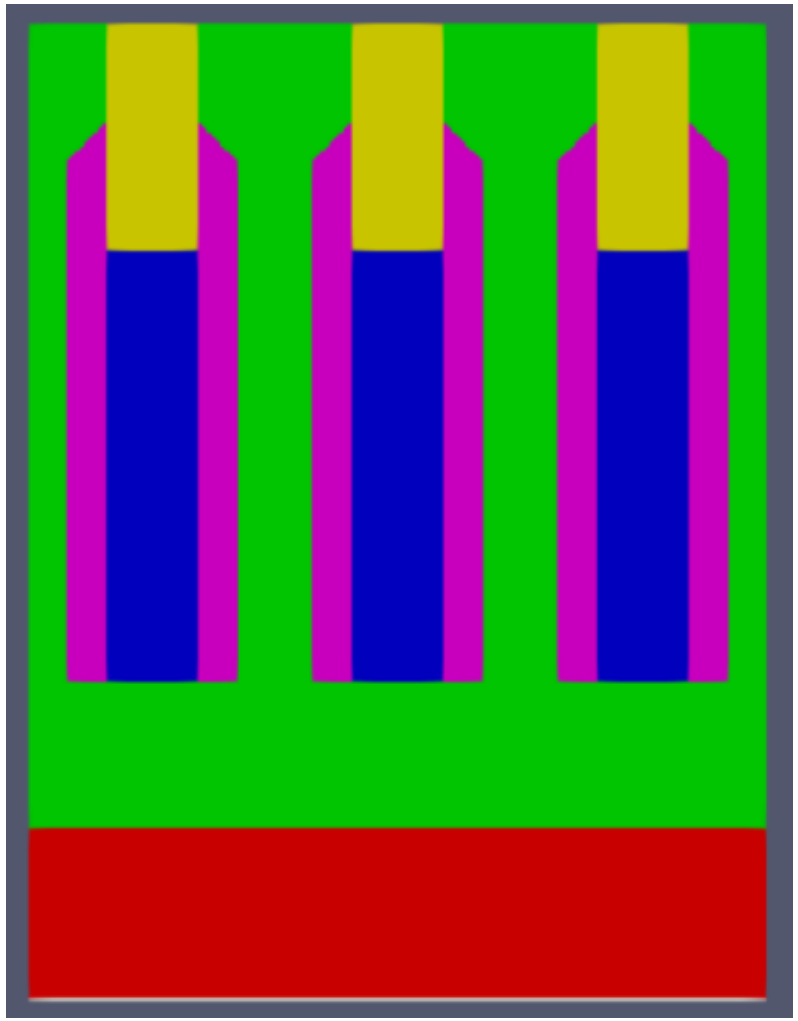


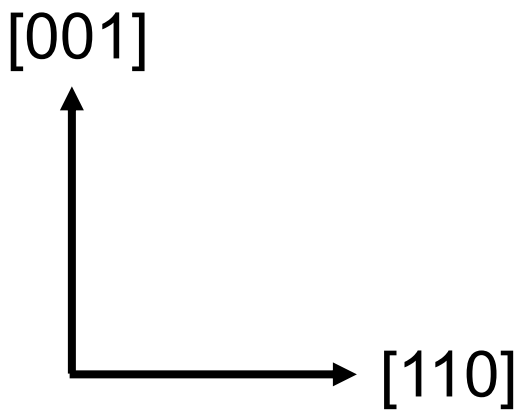

```
model (name="model_salicide") {
    select (region="Si:P")
    select (region="SiGe")
    select (region="Salicide")
}

depo (aniso,region="Salicide",model="model_salicide",thickness=10)
```

ILD0, inter-layer dielectric 0

- SiO_2 layer
  - CMP down to the hard mask (Slightly over-etch)

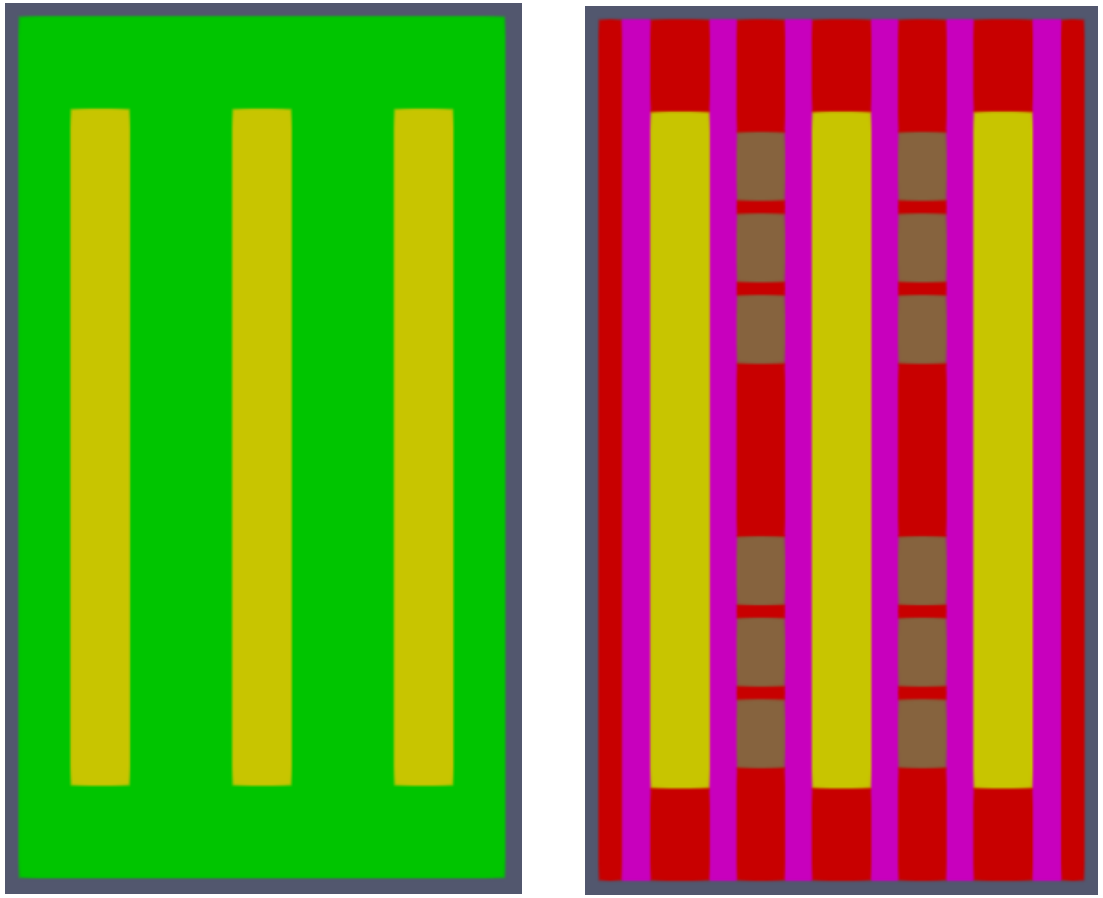
```
cmp (position=215)
```





Gate cut

- Dummy gates are running over several logic gates.
  - For the “gate cut” region, etch the hard mask and dummy gate.
  - Fill the cavity with SiO_2.
  - CMP, again

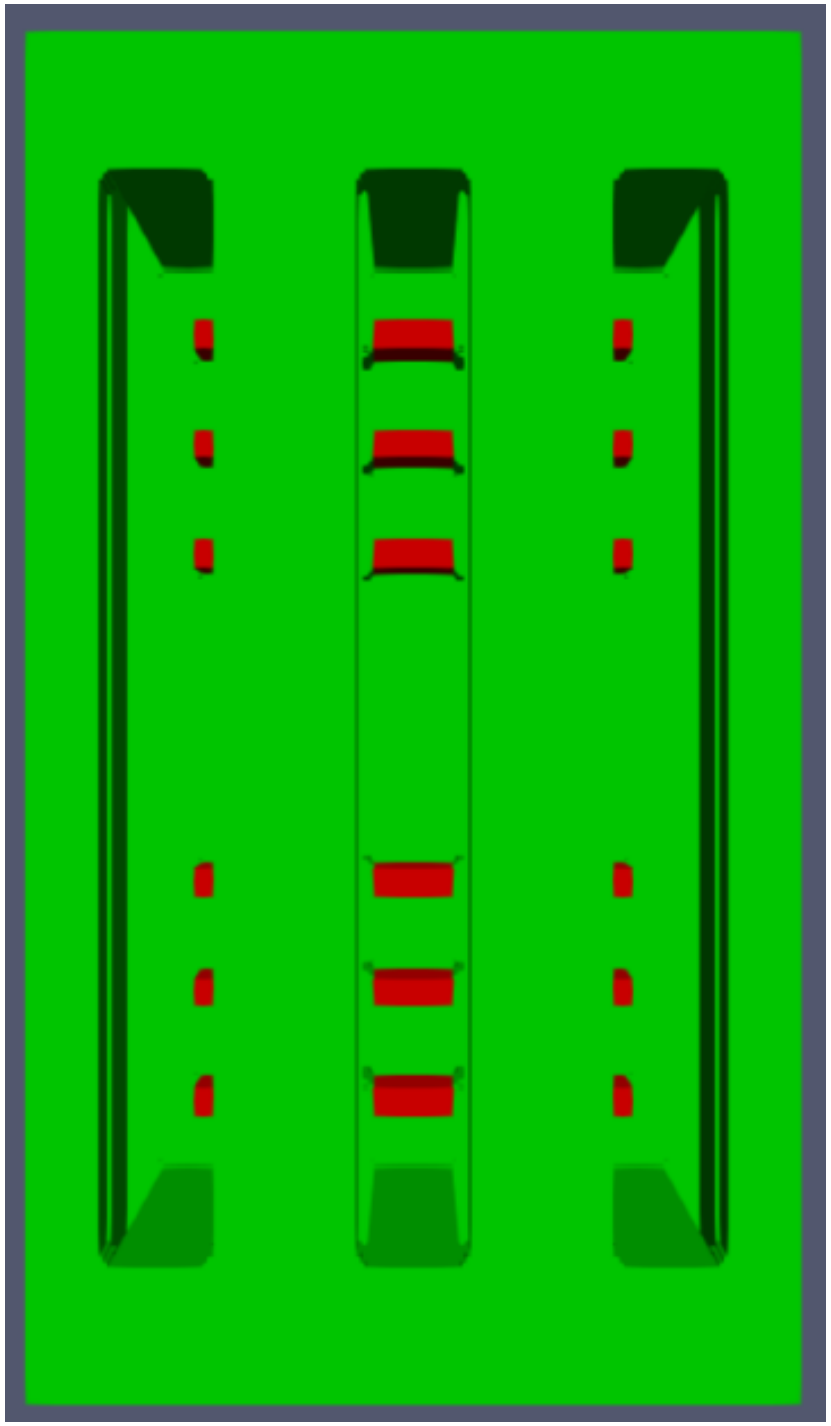


Top view (With/without SiO_2)

```
mask (name="mask_gatecut") {
    rectangle (x0=0,y0=31,x1=162,y1=257)
}
```

Dummy gate removal

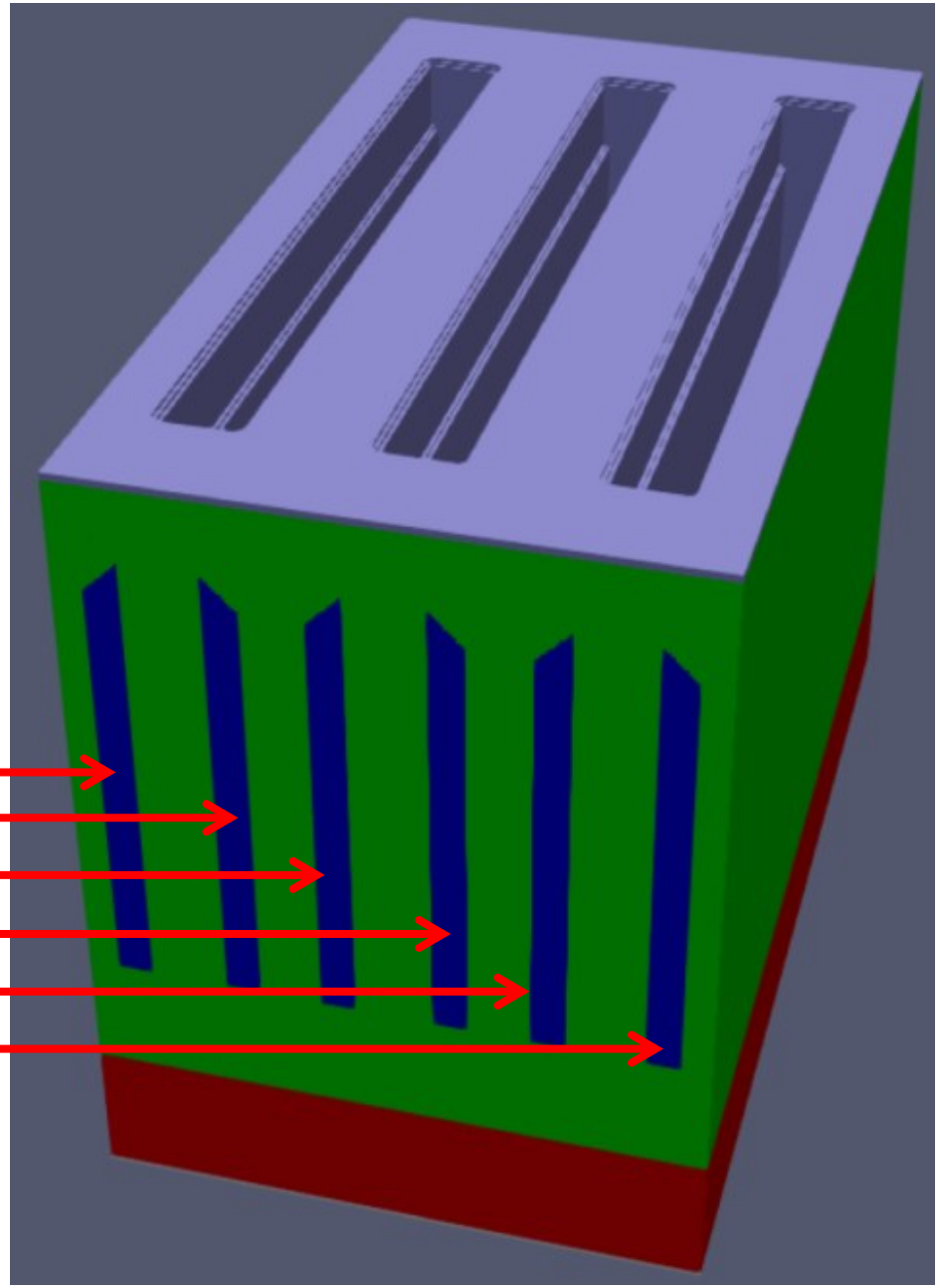
- Now, hard mask and dummy gate are removed.
  - Dummy dielectric is also etched.



High-k stack

- First, 1-nm-thick interfacial layer (Resolution limit)
  - Only on silicon
  - Then, 2-nm-thick high-k (HfO_2) layer

Spacers (Color changed)



Thank you!