# Special Topics on Basic EECS I Design Technology Co-Optimization Lecture 1

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#### **Outline**

- Design Technology Co-Optimization (DTCO)
  - A framework aimed at achieving continued scaling and performance improvements in advanced semiconductor technologies

#### Purpose

- Course dedicated to DTCO is rarely found.
- Initial exposure to DCTO

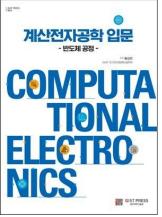
#### Contents

- Basic tools for layout, process emulation, device simulation, and circuit simulation
- Several (TCAD-based) DTCO examples

### Prerequisite and refrences

- Recommended courses
  - Electronic Circuit (EC3207)
  - -Semiconductor Materials and Devices (EC3206)
  - -VLSI Devices (EC4313)
- No textbook
  - -Lecture materials will be distributed.
- References
  - Fundamentals of Modern VLSI Devices by Taur & Ning
  - -계산전자공학 입문 by Hong & Park
  - 계산전자공학 입문 반도체 공정 by Hong





#### Resources

Presentation materials

https://github.com/hi2ska2/dtco2025f

- Homework submission and notice
  - -GIST LMS system
- YouTube channel

https://www.youtube.com/@TCADHong

# **Grading and policy**

- Attendance: 10 %
- Homework: 30 %
  - For some of them, you must submit recorded videos. (New in this semester)
- No paper examination
- Final project presentation: 60 %
  - You must submit a recorded video.
  - The submitted video will be posted on my YouTube channel.
- The offline lectures will be live-streamed.

#### Recorded lectures

- Week 2 (Sep. 8 and Sep. 10)
  - Business trip to Munich (ESSERC)



- Lecture 3: Recorded video, available at 09:00 on Sep. 8 (on my YouTube channel)
- Lecture 4: Recorded video, available at 09:00 on Sep. 10 (on my YouTube channel)
- -Attendance: Homework reports
- Additionally, Week 15 (Dec. 8 and Dec. 10)
  - -Business trip to San Francisco (IEDM)



December 6-10, 2025 San Francisco, CA

# L1

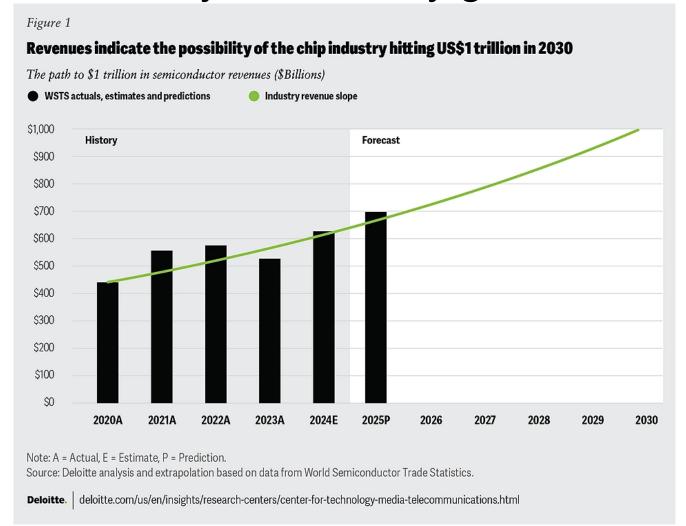
#### As of 2025,

Growth of semiconductor industry is driven by generative

Al chips.

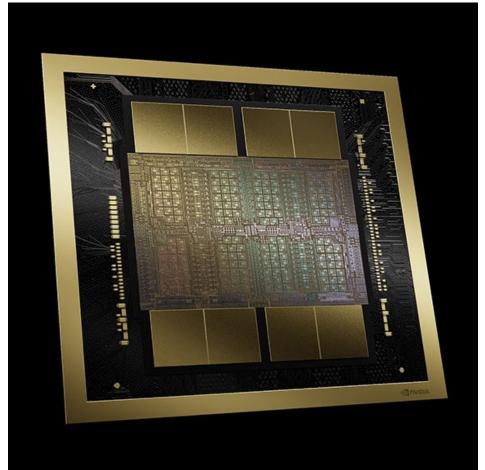
- -CPUs
- -GPUs
- Data centercommunications chips
- Memory
- -Power chips

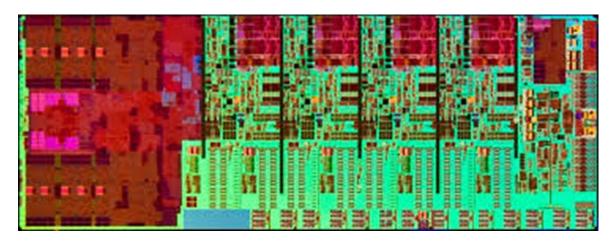
2025 global semiconductor industry outlook (Deloitte)



#### Nvidia B200

- A building block of DGX B200 or GB200 NVL72
  - -208 billion transistors





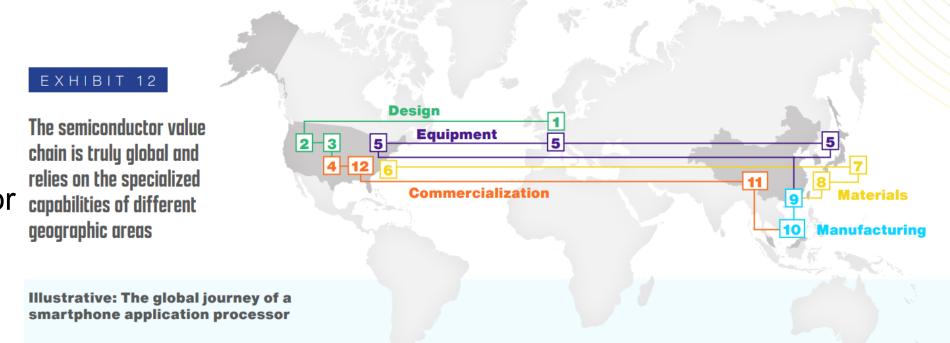
Intel Core i74770K, 2013, <u>1.4B</u> transistors (Intel)

Nvidia B200, 2024, <u>208B</u> transistors (Nvidia)

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# Geopolitical dimensions

- The semiconductor industry is not just economically important.
  - -Six major regions (US, South Korea, Japan, mainland China, Taiwan, and Europe)



(Semiconductor Industry Association)

# What is the key factor?

- If you run a restaurant, you must orchestrate:
  - -Ingredients & suppliers
  - -Recipes & standards
  - Chef & brigade
  - -Kitchen & equipment
  - -Execution on the pass
  - Consistency control
  - -Plating & presentation
  - -Service & guest experience
  - -Ambient & reputation
  - Cost & throughput



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(ChatGPT)

#### Ultimately, the key is taste.

- If the food is not great, nothing else makes up for it.
  - -That is the core value.
- What is the equivalent of "taste" in semiconductor manufacturing?

-Especially for Al chips, expectations are closer to fine dining

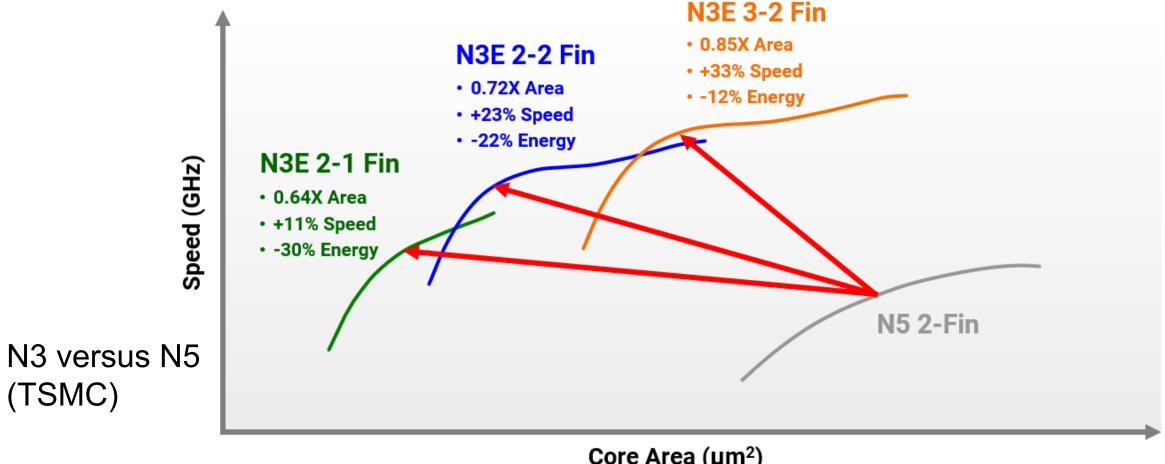
than fast food.



(Michelin guide)

# Power, performance, area (PPA)

 Low-power (mobile), high performance (high clock speed), and smaller area (more transistors)



# Snapdragon 8 Gen 1 / 8+ Gen 1

- Same architecture, different foundry (Samsung 4LPE / TSMC N4)
  - -Foundry choice changes PPA. (20 % area reduction)





#### Homework#1

- Due: 08:00 on Sep. 3 (Morning in this Wednesday)
- Submit a recorded video. Send it to me via e-mail.
  - Explain the operation of MOSFETs.
  - -The video length and scope are up to you.
  - Do not disclose your personal information except for your name.

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# Thank you!