Special Topics on Basic EECS I Design Technology Co-Optimization

Lecture 19

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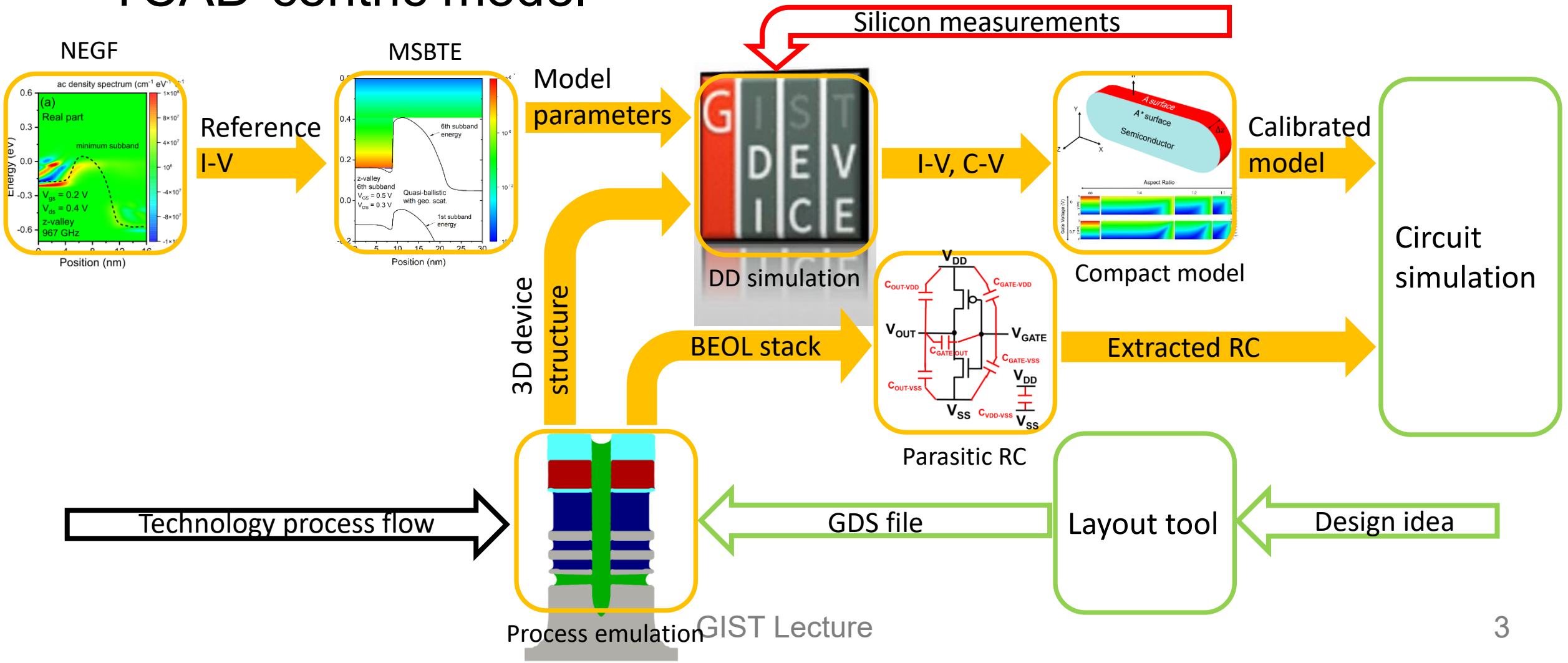
L19

DTCO toolchain

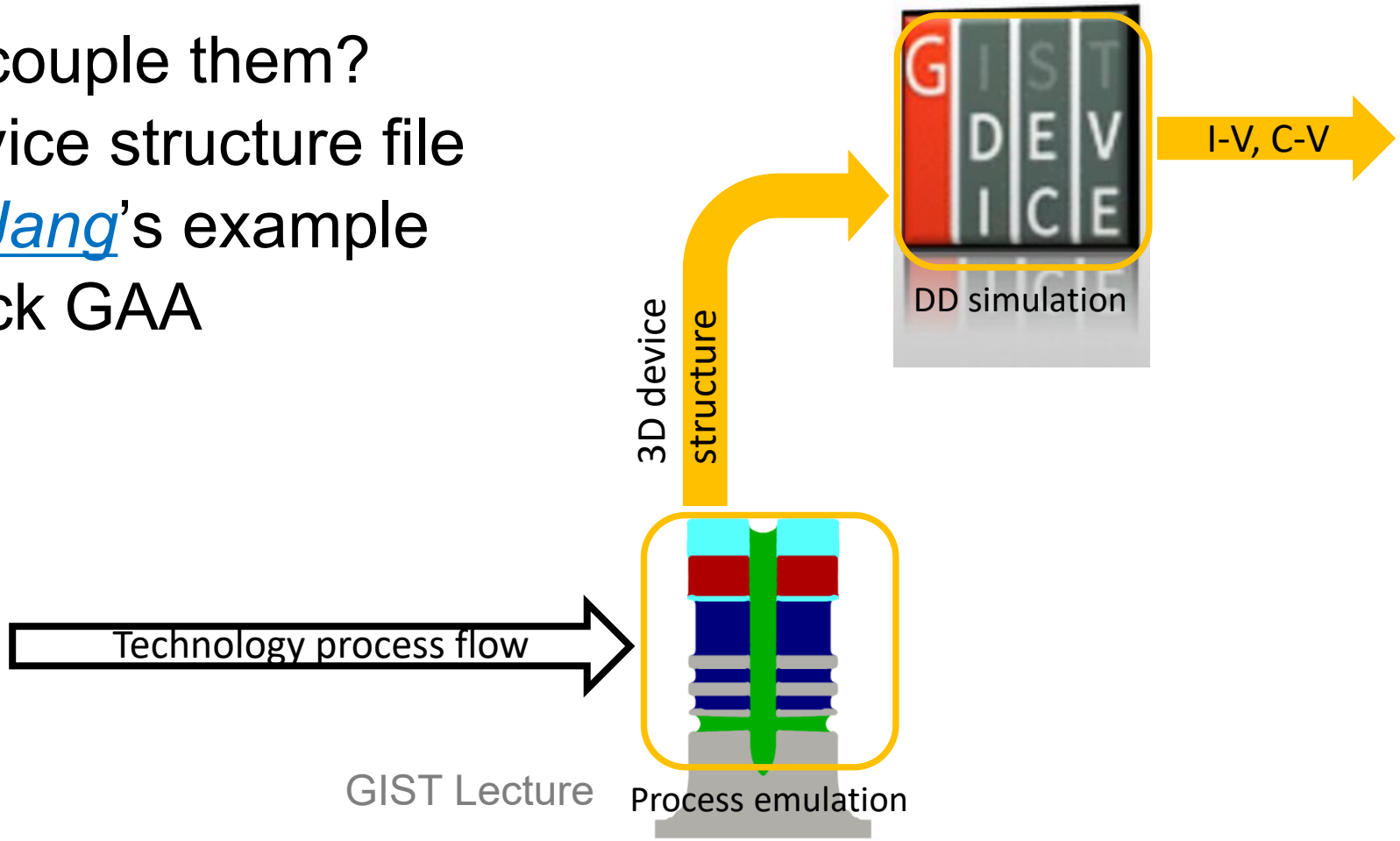
- TCAD-centric model



AngstromCraft & G-Device

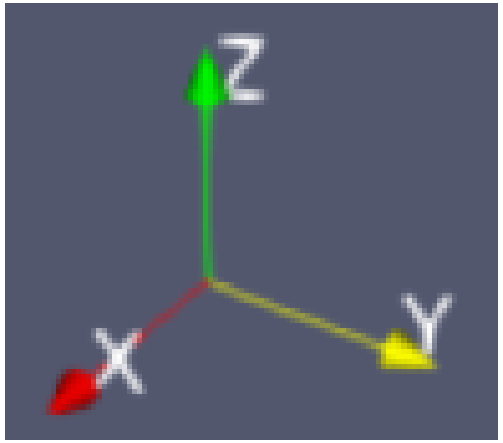
- They are two important building blocks in the DTCO workflow.
  - How can we couple them?
  - Sharing a device structure file
  - *Mr. Min-Seo Jang*'s example

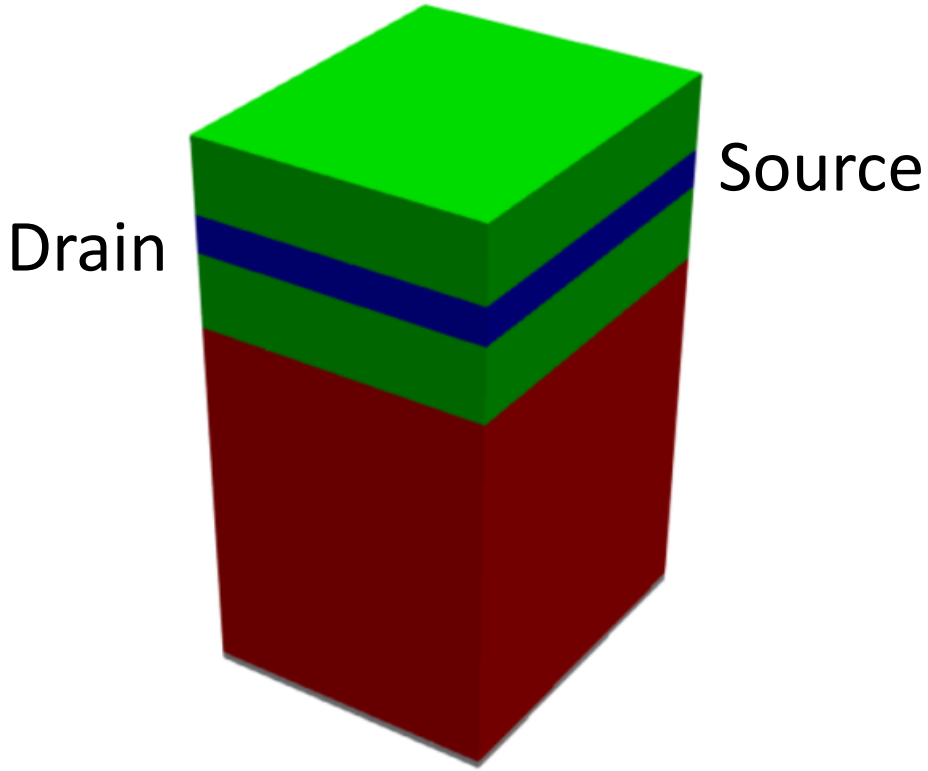
➔ A single stack GAA



Si/SiGe stack (48 nm X 40 nm)

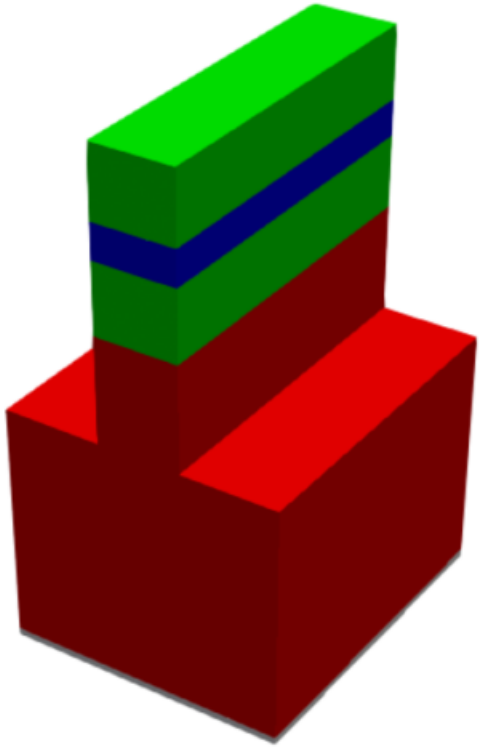
- 5-nm-thick Si channel
  - Sandwiched by two 10-nm-thick SiGe layers

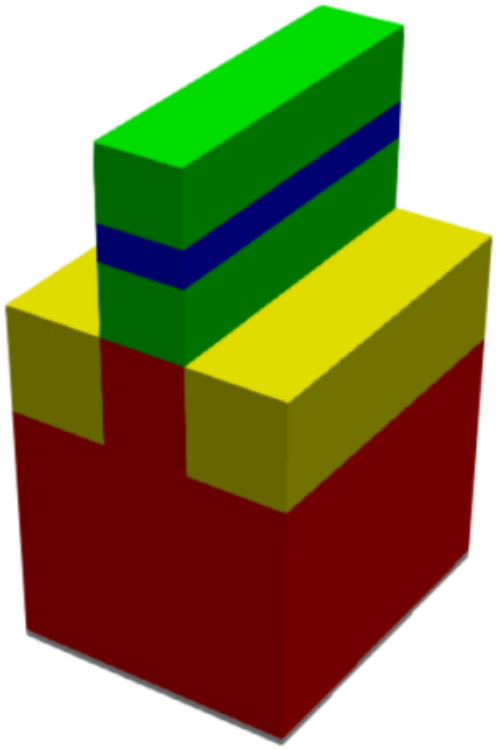




Fin formation & STI

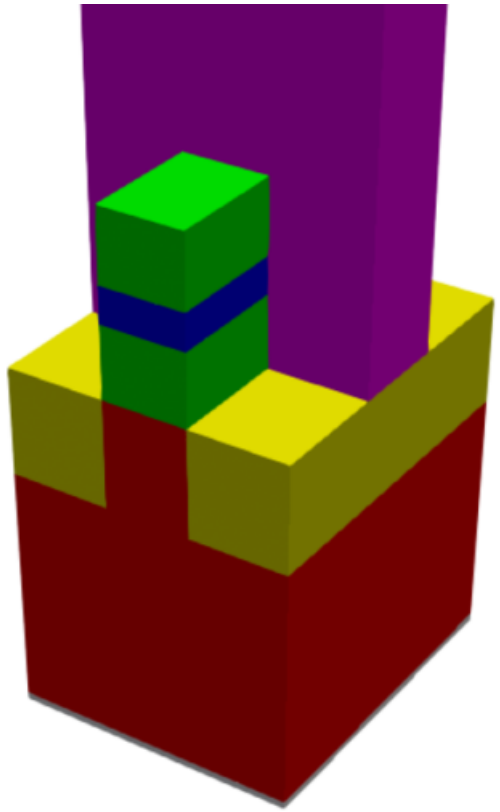
- 12-nm-wide fin
  - Then, STI is filled.

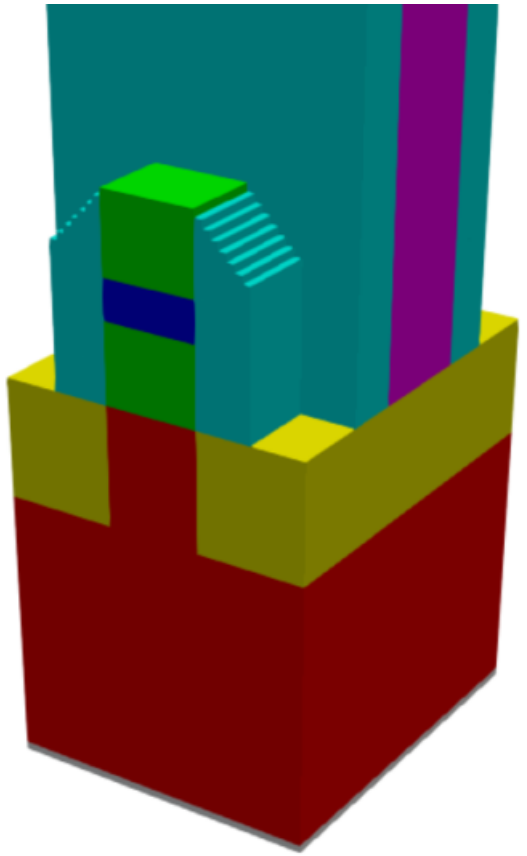




Dummy gate & outer spacer

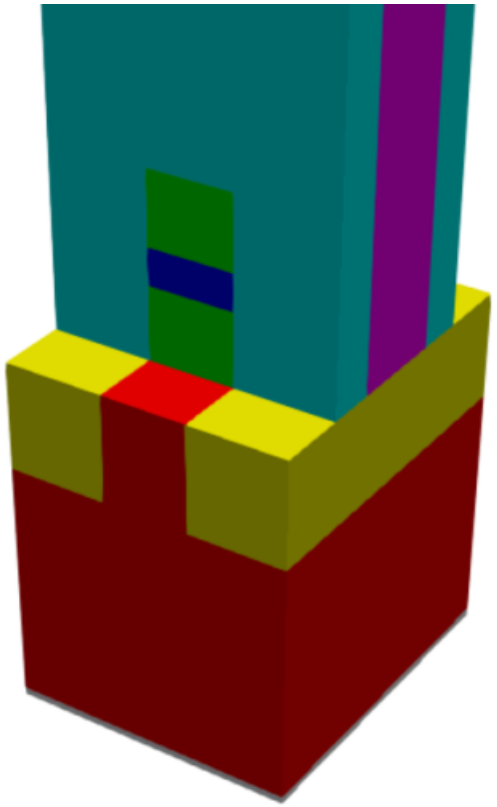
- 14-nm-long dummy gate
  - Then, 7-nm-thick outer spacer

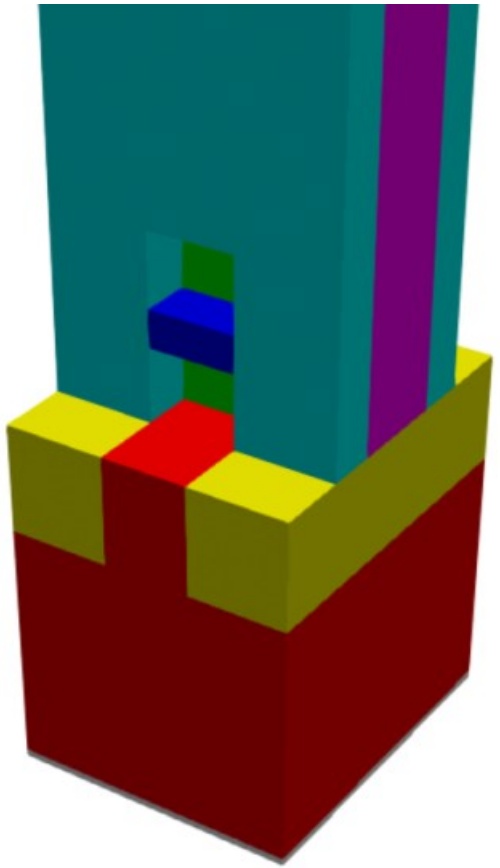




S/D cavity etch & inner spacer etch

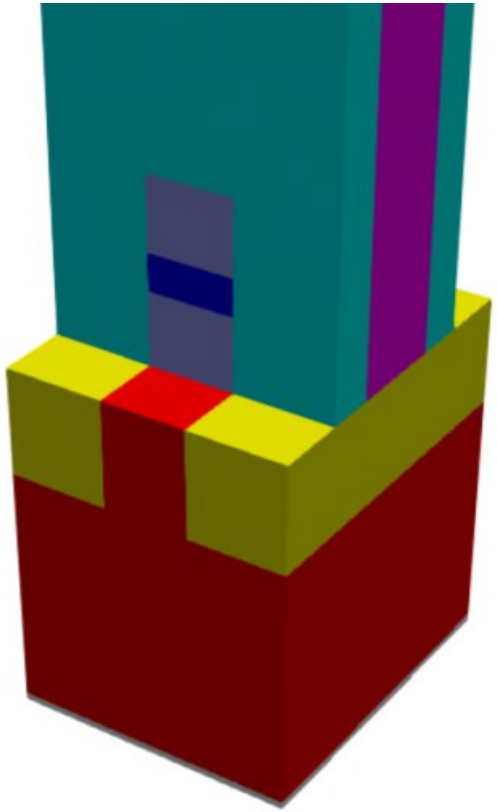
- Source/drain regions are completely etched away.
  - Then, inner spacer etch

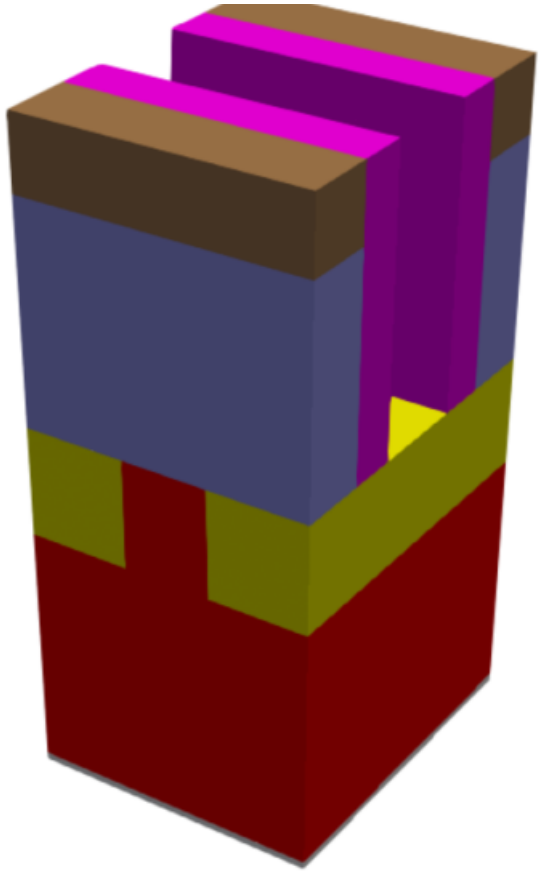


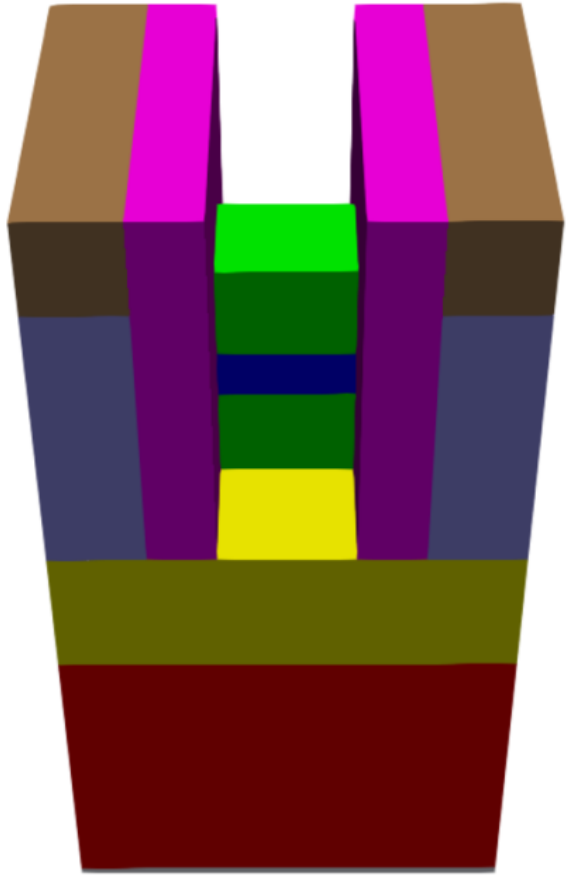


Inner spacer & S/D epitaxial growth

- In this simple example, S/D shapes are unrealistic.
  - Then, dummy gate removal

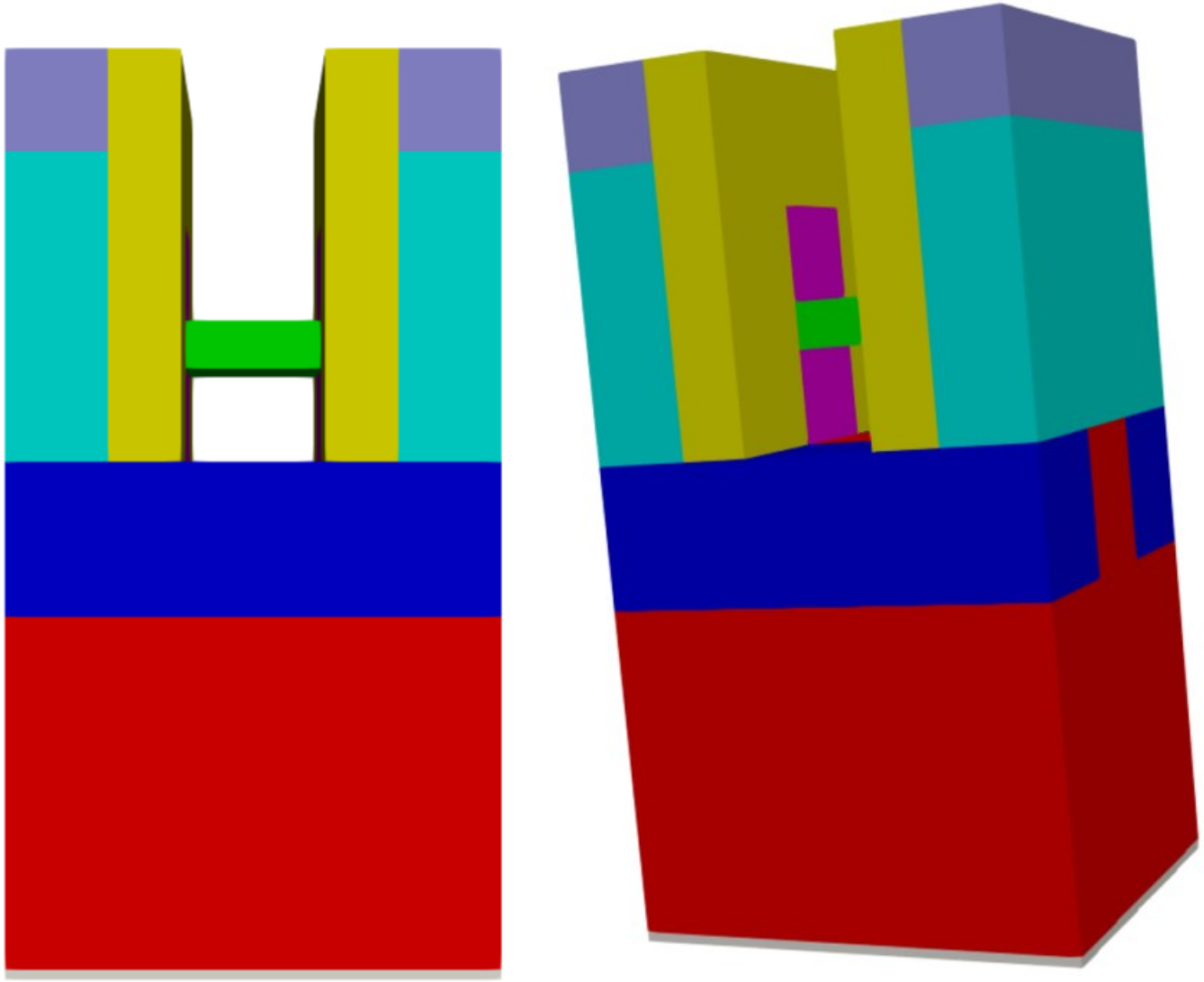






Channel release by etching SiGe layers

- If there is no inner spacer, what happens?
  - Difficult to separate S/D and G
  - Precise control of inner spacers is very important.

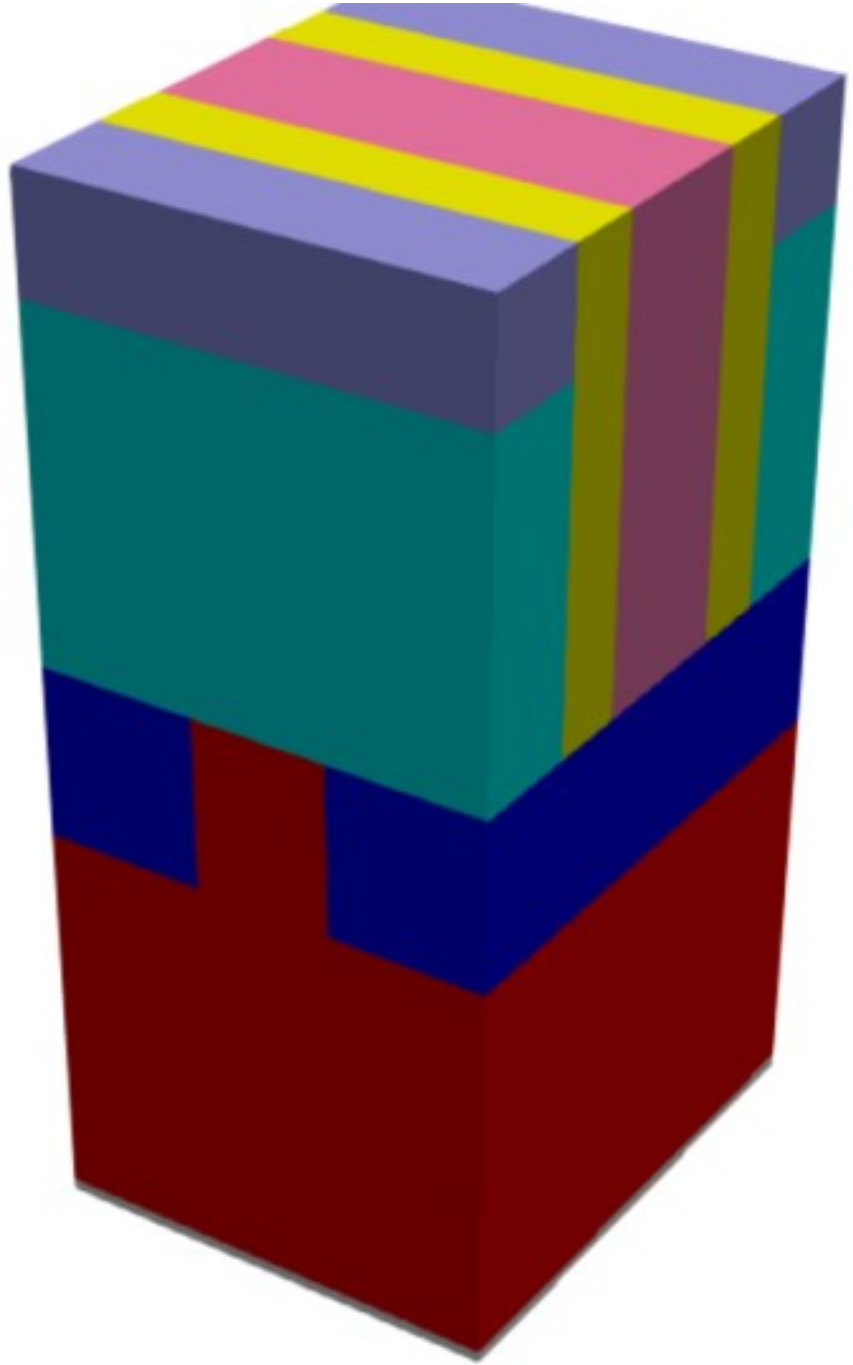


High-k/metal gate

- In reality, the high-k layer covers the spacers, too.
  - Simple, unrealistic shape

  (Completely okay for our present purpose)

- We have done a similar job for FinFETs. Then, what's the next step?



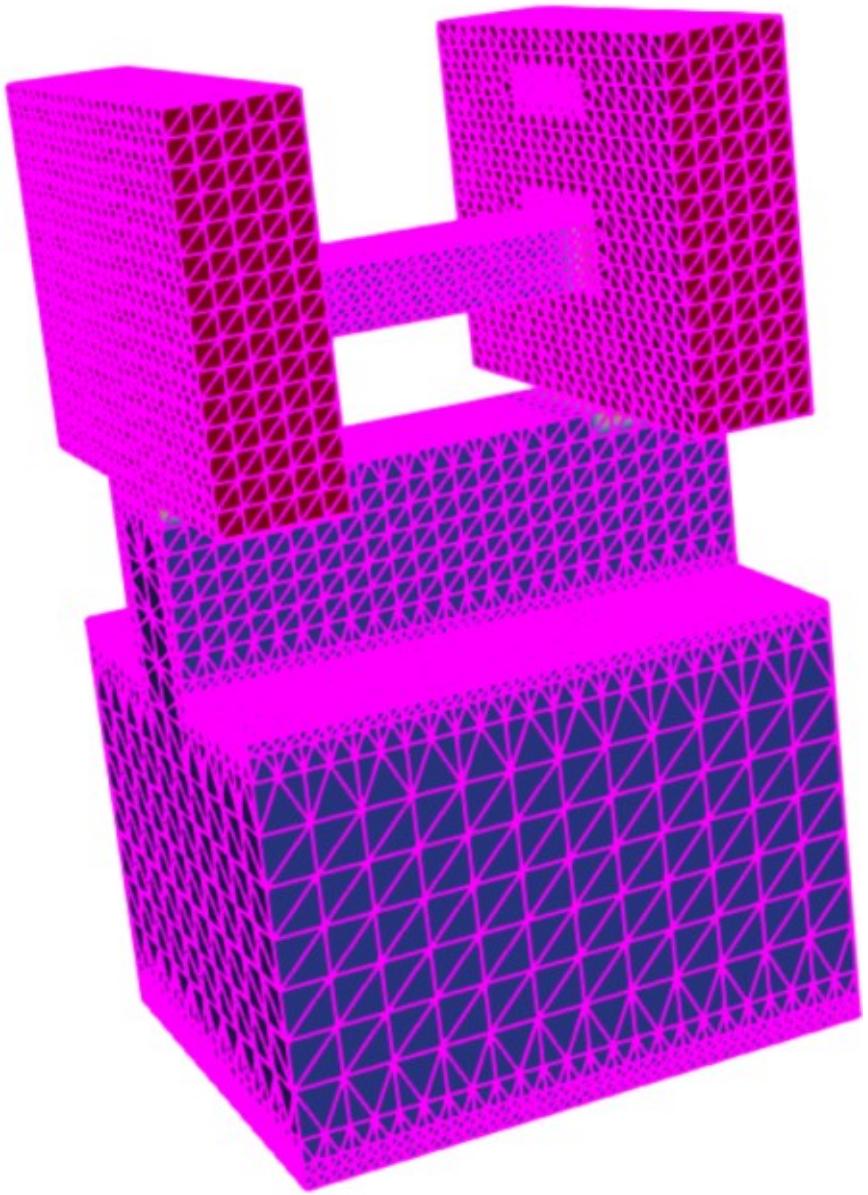
Two-step process

- Run `angstromcraft mesh.cmd` first.

```
mesh (lx=48,ly=40,lz=200,nx=48,ny=40,nz=200,nresolution=3,mapmaker,load="GAA.cgns",save="mesh.cgns") {
  region (material="Si",name="Si_Bulk",resolution=2)
  region (material="Si",name="deepsubstrate",resolution=2)
  region (material="Si",name="Si",resolution=0)
  region (material="SiO2",name="SiO2",resolution=2)
  region (material="Si3N4",name="SiN",resolution=2)
  region (material="Si3N4",name="inner",resolution=2)
  region (material="Si",name="SD",resolution=1)
  region (material="SiO2",name="gateoxide_SiO2",resolution=0)
  contact (name="gate_contact",type="this",region="gate")
  contact (name="body_contact",type="side",region="deepsubstrate",zmin)
  contact (name="sd_contact",type="this",region="MOL_Metal")
  selectcontact (input="sd_contact",output="source_contact",xmin=0)
  selectcontact (input="sd_contact",output="drain_contact",xmax=0)
  removecontact (name="sd_contact")
  contact (name="SD_Channel_interface",type="interface",first="Si",second="SD")
  doping (region="Si",type="gaussian",peakconc=1.0e26,baseconc=-1.0e22,diffusionlength=2,interface="SD_Channel_interface")
  removecontact (name="SD_Channel_interface")
  doping (region="Si_Bulk",type="uniform",conc=-1.0e22)
  doping (region="deepsubstrate",type="uniform",conc=-1.0e22)
  doping (region="SD",type="uniform",conc=1.0e26)
}
```

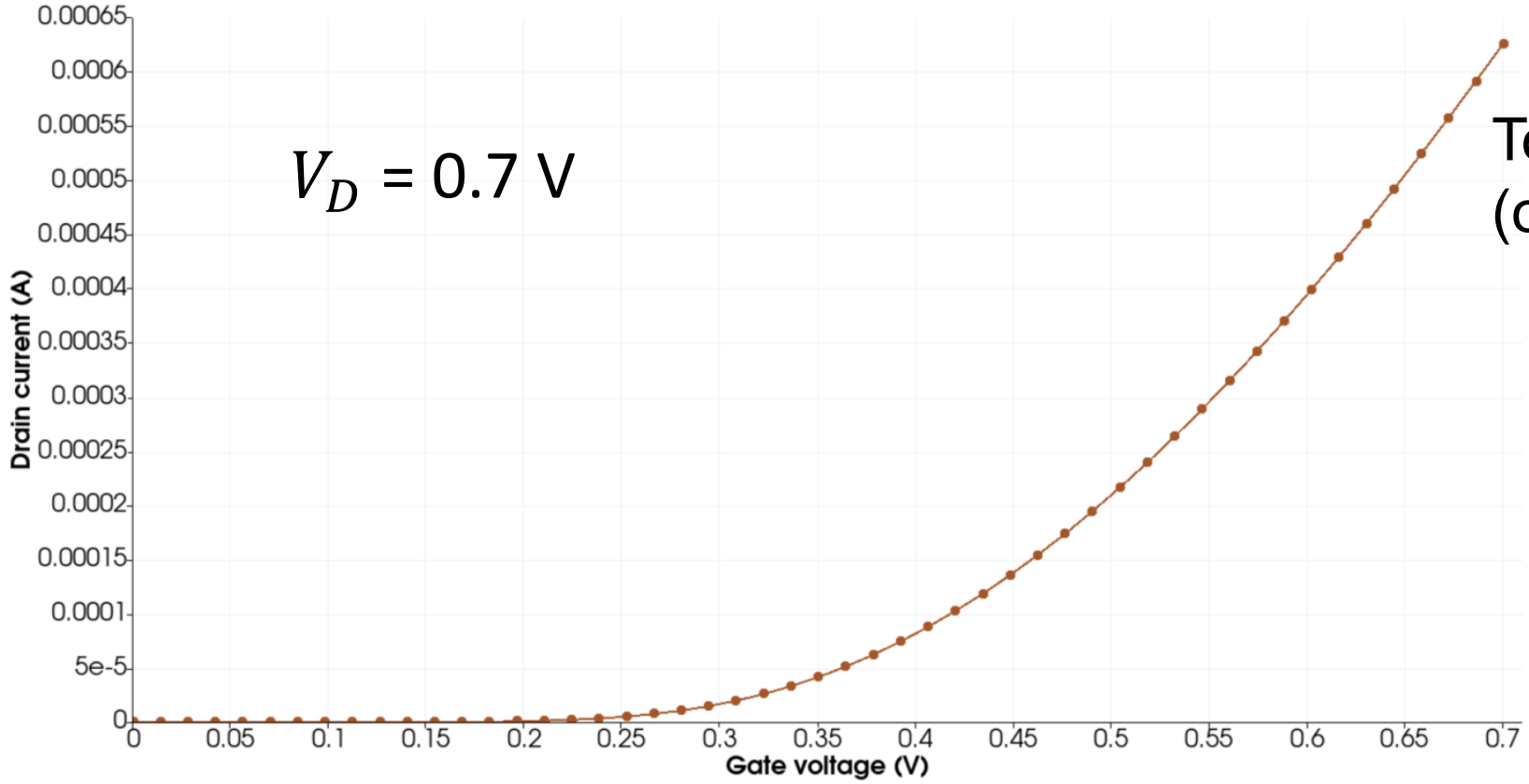
As a result, we have `mapmaker.cmd`.

- Run `gdevice mapmaker.cmd` for mesh generation.
  - Then, we have a device structure.
  - The name of final structure (`mesh.cgns`) can be found in mesh.cmd.



We can simulate it.

- Run `gdevice nmos.cmd` for IV curves.
  - Modify your `dbpath` appropriately.
  - The result (without any mobility model) is drawn below.



Too high current (overestimated)

Homework#19

- Due: 08:00 on Nov. 24
- Submit a report through the GIST LMS system.
  - Build the single stack GAA using the AngstromCraft code.
  - Then, calculate its IV characteristics using the G-Device code.
  - Three input files can be found in our GitHub repository.

Thank you!