Special Topics on Basic EECS I
Design Technology Co-Optimization
Lecture 18

Sung-Min Hong (smhong@gist.ac.kr)
Semiconductor Device Simulation Laboratory
Department of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology (GIST)

L18

Physical models

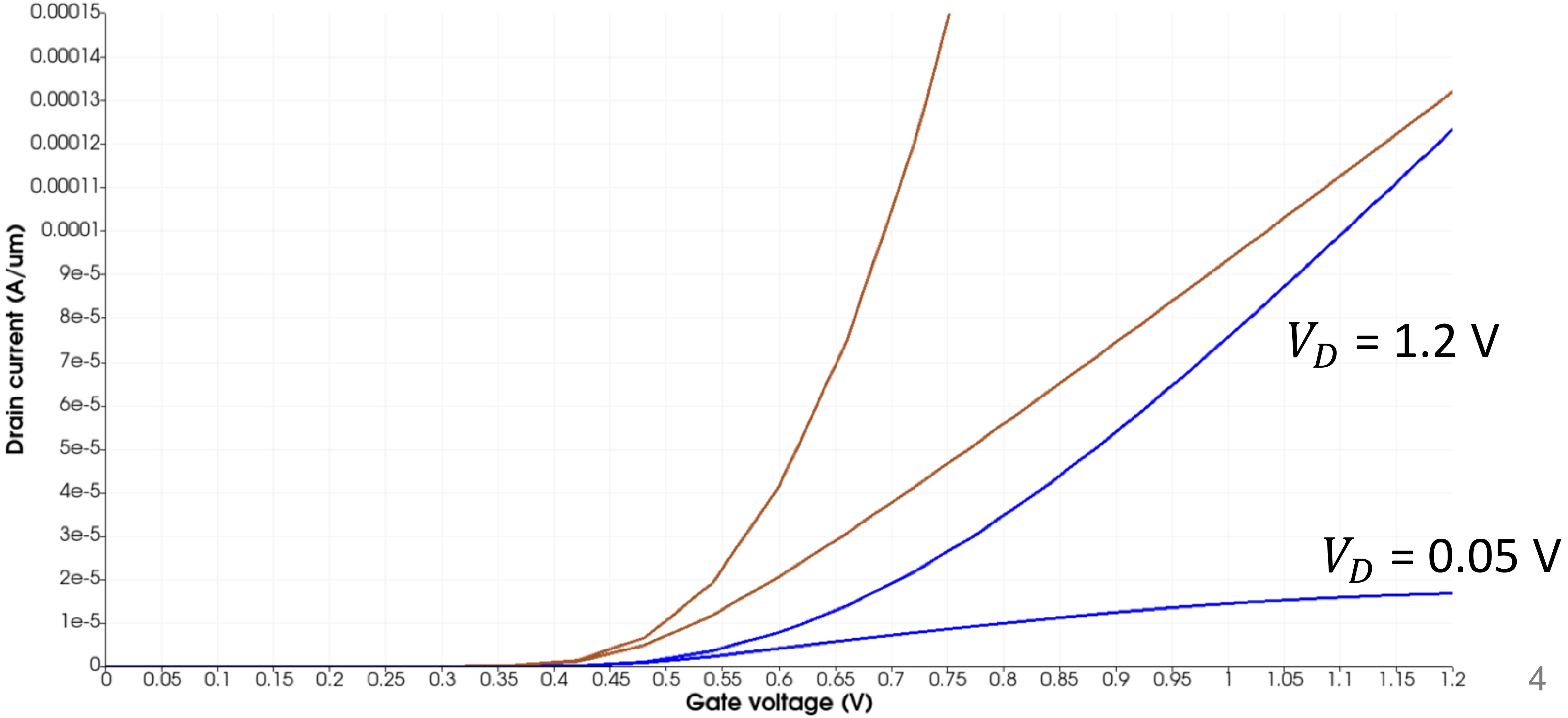
- Of course, we must include physical models.
  - Add the following lines.

```
property (thing="mosfet",model="mobility",mujtaba,canali)
property (thing="mosfet",model="recombination",srh)
```

  - Observe their effects.

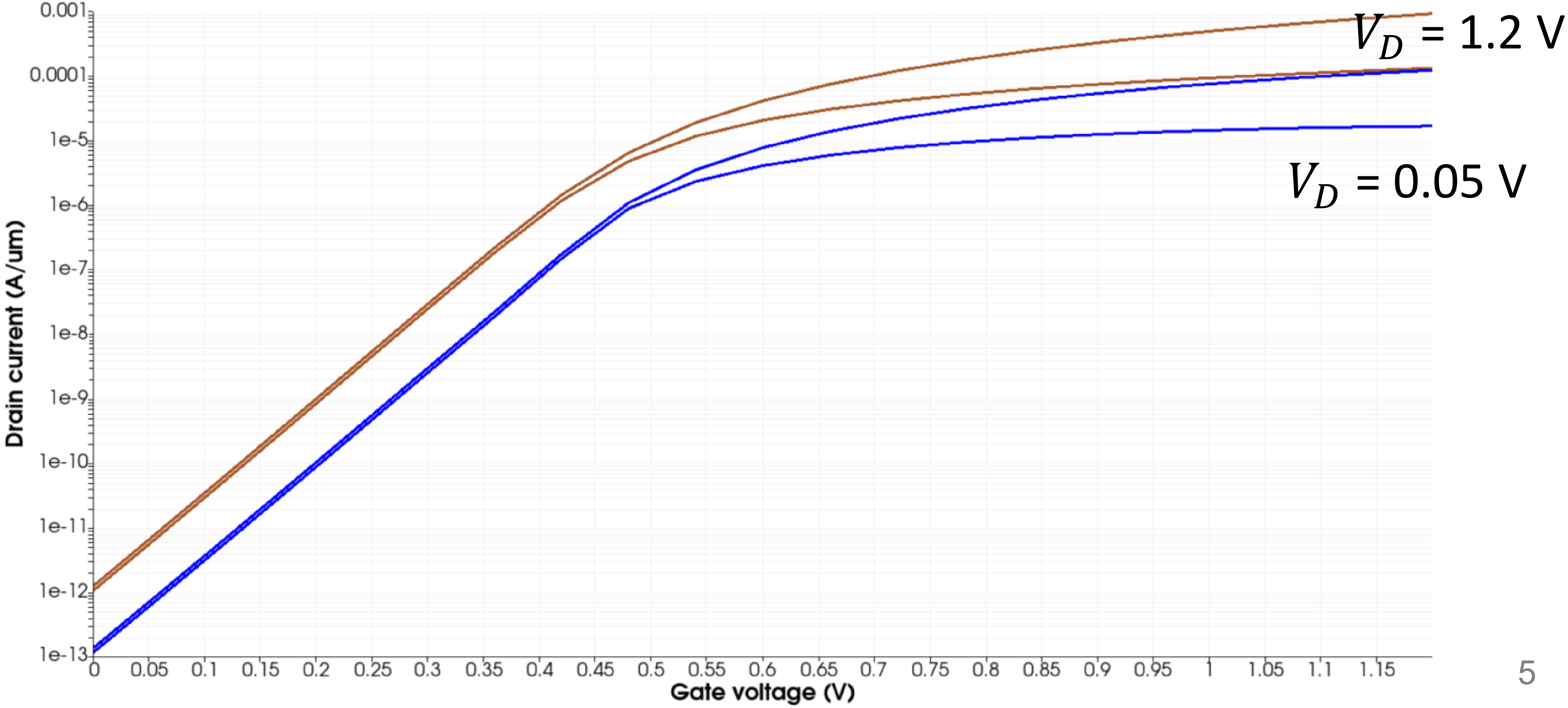
Linear curve

- Significantly reduced current (Blue curves)



Semi-logarithmic curve

- Significantly reduced current (Blue curves)



Ramping the drain voltage up

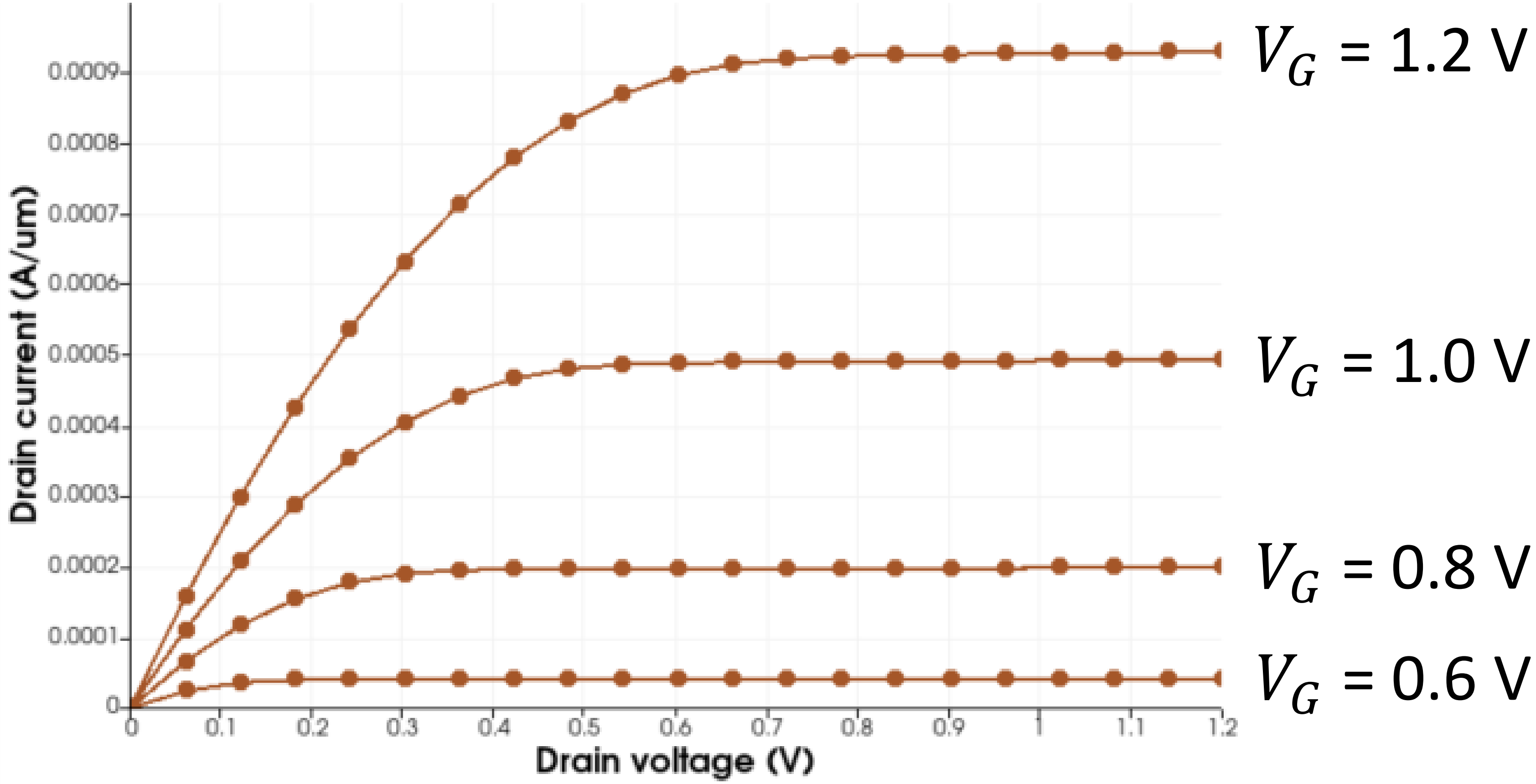
- We need several gate voltages.
  - Select a value and ramp up the gate voltage.
- Increase the drain voltage from 0 V to V_{DD}.

```
solve (law="dclaw",initialstep=0.05,maxstep=0.05,minstep=0.01,dozero,
        plot,plotprefix="long_dc",cgns,book="output_iv") {
  goal (thing="vd", quantity="voltage", value=1.2)
}
```

- Repeat it with other V_G values.

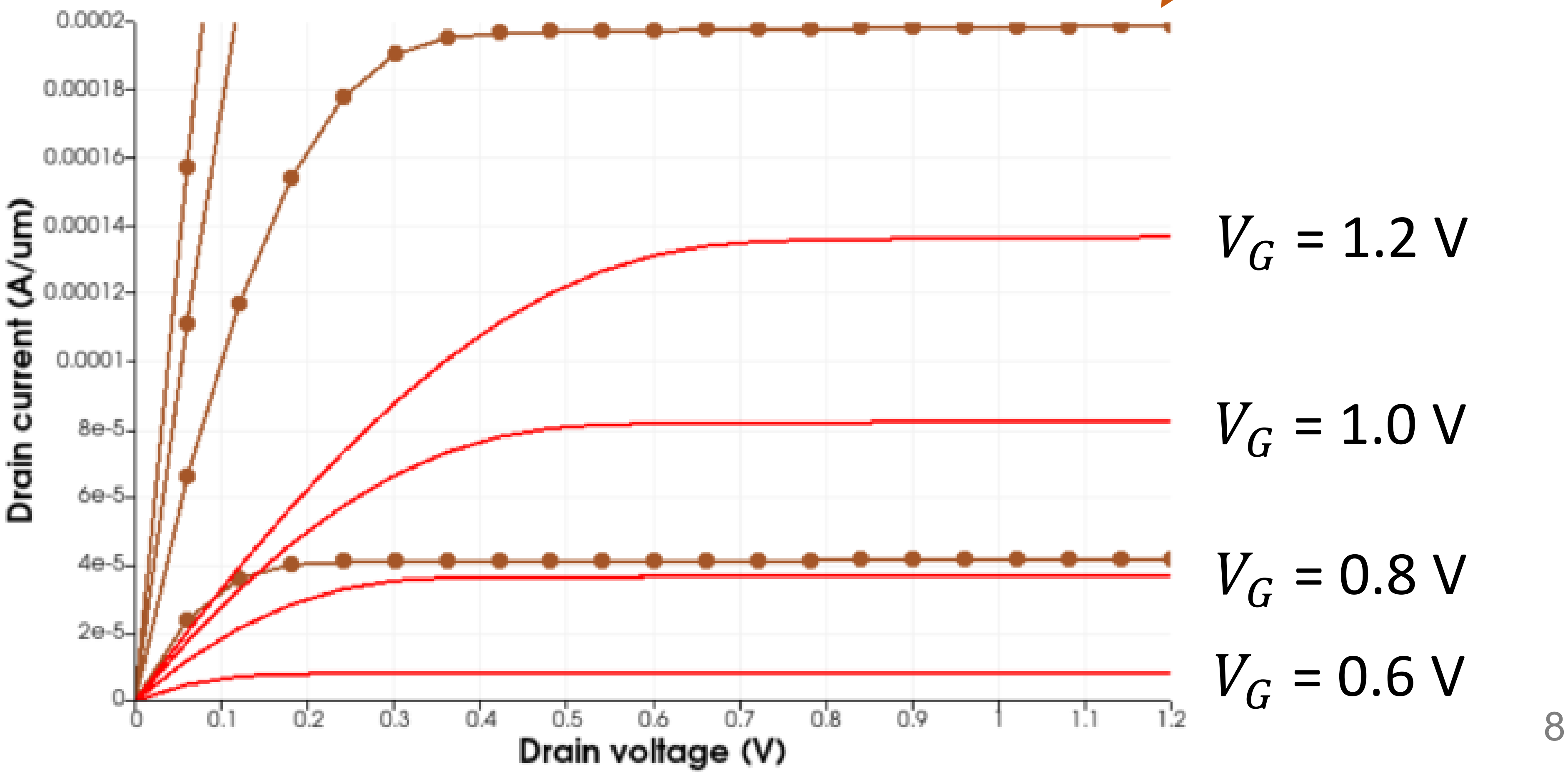
Without physical models

- Results WITHOUT any physical model from V_G = 0.6 V to 1.2 V (0.2 V step)



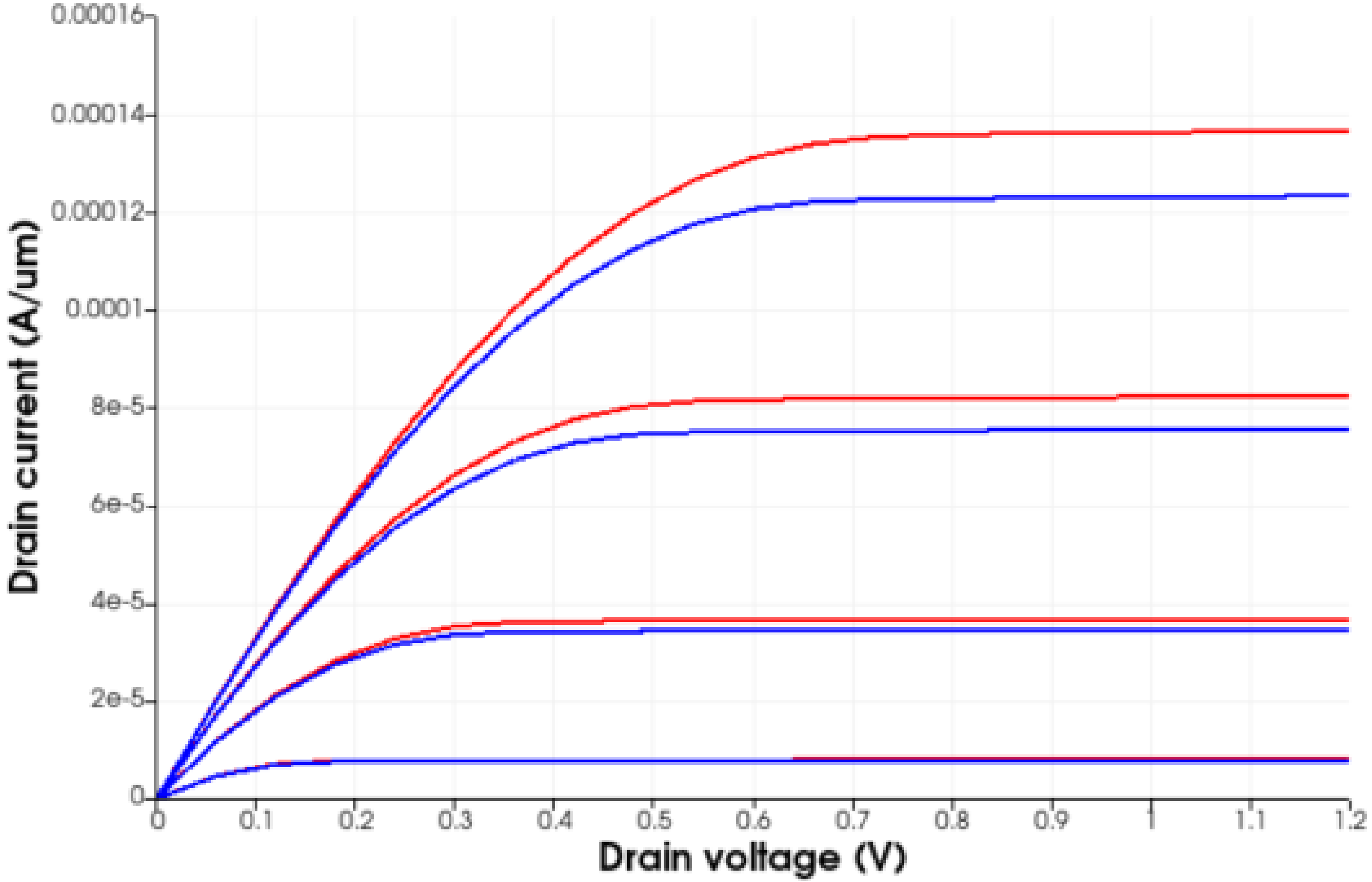
Inversion mobility model

- Results WITH inversion mobility model
  - Significantly reduced current (Brown versus red)



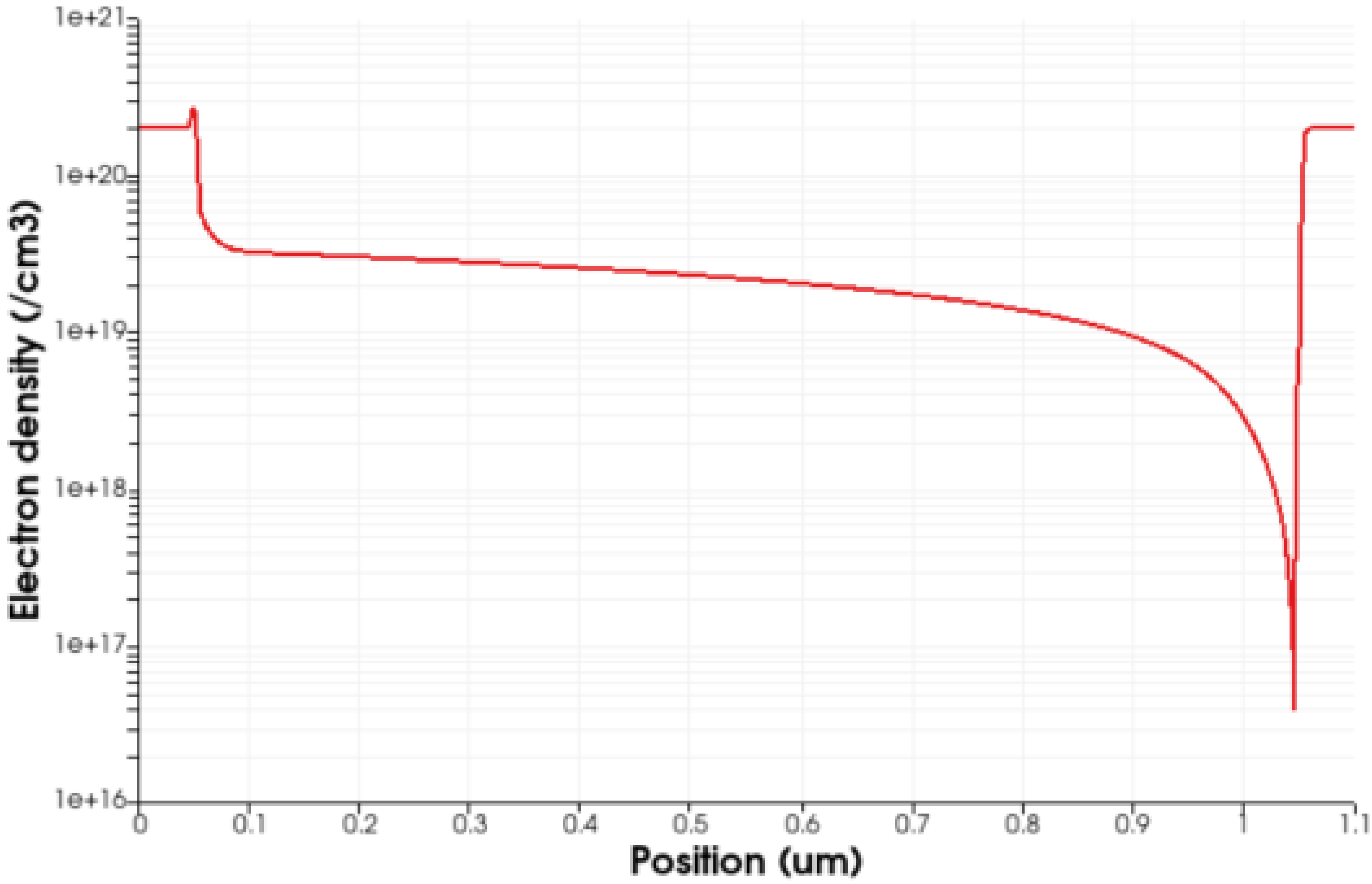
Velocity saturation

- Results WITH inversion mobility model + velocity saturation



Electron density

- Interface carrier density at $V_G = V_D = V_{DD}$



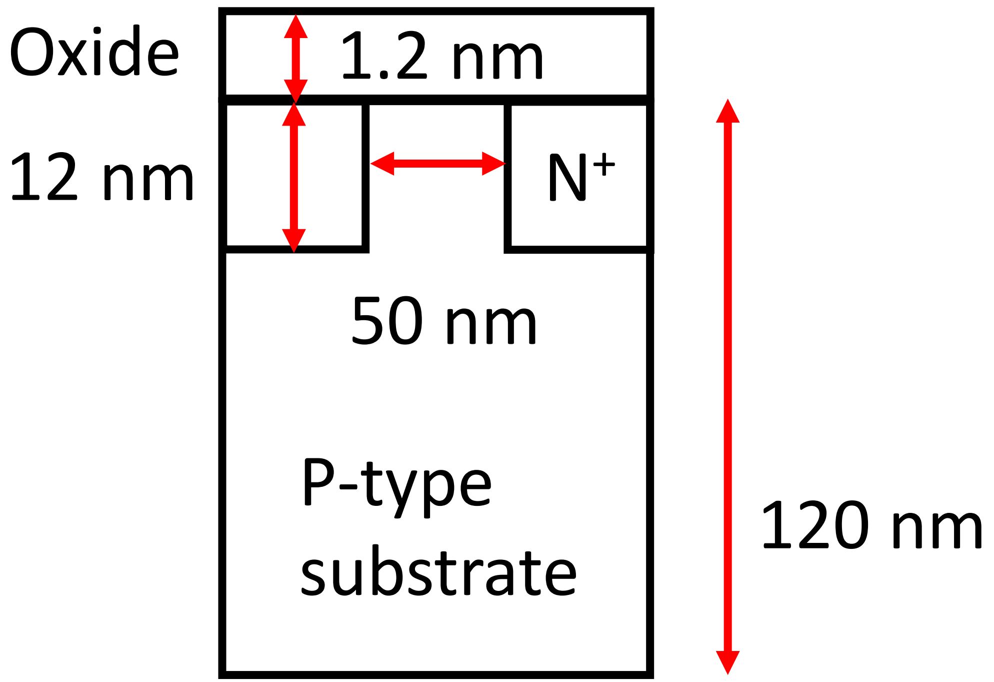
Homework#18

- Due: 08:00 on Nov. 19
- Submit a report through the GIST LMS system.
  - From the input IV characteristics of our long-channel MOSFET, estimate the DIBL. (Of course, you must consider physical models.)

Simulation of a short-channel MOSFET

- Effective oxide thickness of 1.2 nm
  - Gate workfunction of 4.3 eV
  - Substrate doping of $1.5\text{X}10^{18}$ cm^{-3}
  - V_{DD} of 1.2 V

- Channel length of 50 nm
  - 1 nm spacing



Mapmaker

- Input file
  - x: Depth
  - y: Channel
  - z: Width

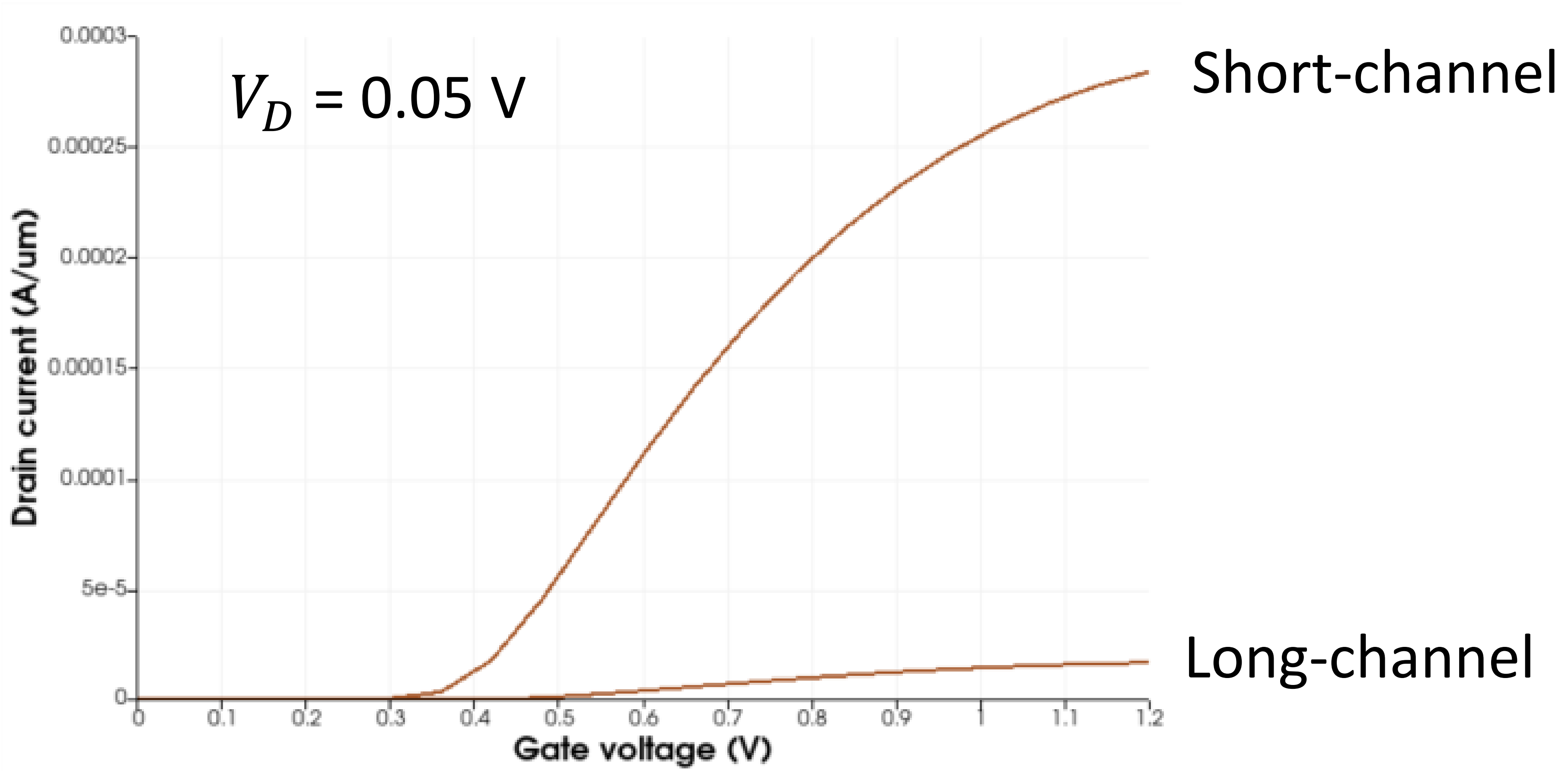
```
thing (type="mapmaker",name="structure") {
   mapmaker (type="3d",cgns="short.cgns") {
      cuboid (x0=-1.2nm,y0=-75nm,x1=120nm,y1=75nm,z0=0.0,z1=1.0um,nx=102,ny=151,nz=2)
      region (name="semiconductor",material="silicon",ix0=1,ix1=101,iy0=0,iy1=150,iz0=0,iz1=1)
      region (name="insulator",    material="oxide",  ix0=0,ix1=1,  iy0=0,iy1=150,iz0=0,iz1=1)
      doping (region="semiconductor",ix0=1,ix1=101,iy0=0,  iy1=150,iz0=0,iz1=1,density=-1.5e18/cm3)
      doping (region="semiconductor",ix0=1,ix1=11, iy0=0,  iy1=50, iz0=0,iz1=1,density=2e20/cm3)
      doping (region="semiconductor",ix0=1,ix1=11, iy0=100,iy1=150,iz0=0,iz1=1,density=2e20/cm3)
      contact (name="source",ix0=1,  ix1=6,  iy0=0,  iy1=0,  iz0=0,iz1=1)
      contact (name="gate",  ix0=0,  ix1=0,  iy0=50, iy1=100,iz0=0,iz1=1)
      contact (name="drain", ix0=1,  ix1=6,  iy0=150,iy1=150,iz0=0,iz1=1)
      contact (name="body",  ix0=101,ix1=101,iy0=0,  iy1=150,iz0=0,iz1=1)
   }
}
```

Short and long structures

- Drawn in the same scale

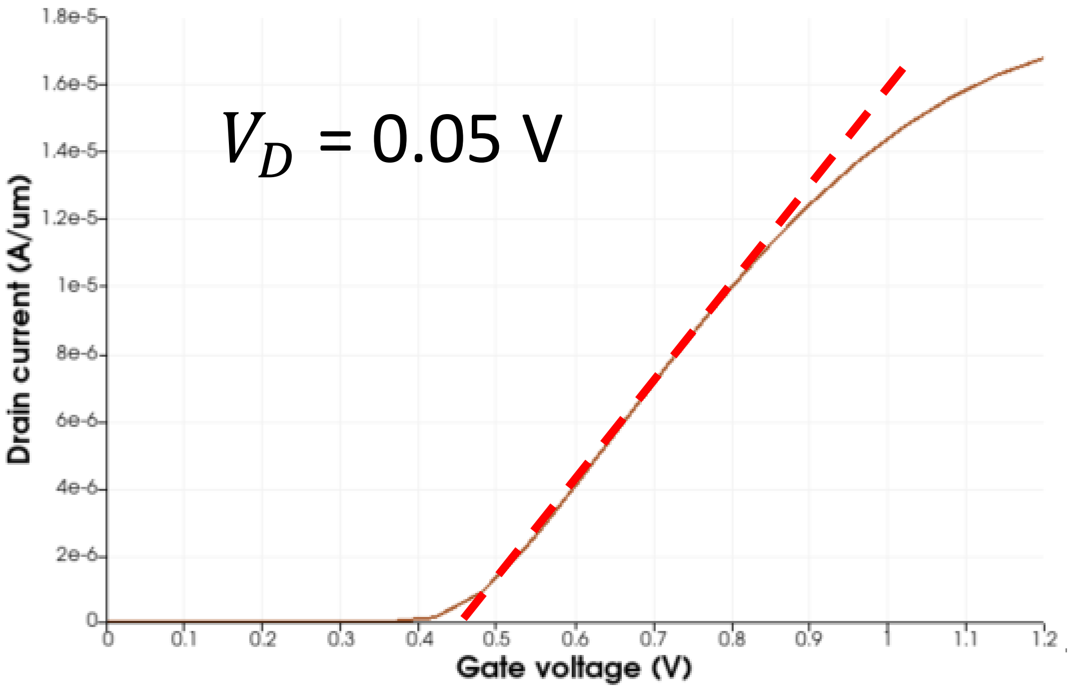
Input characteristics

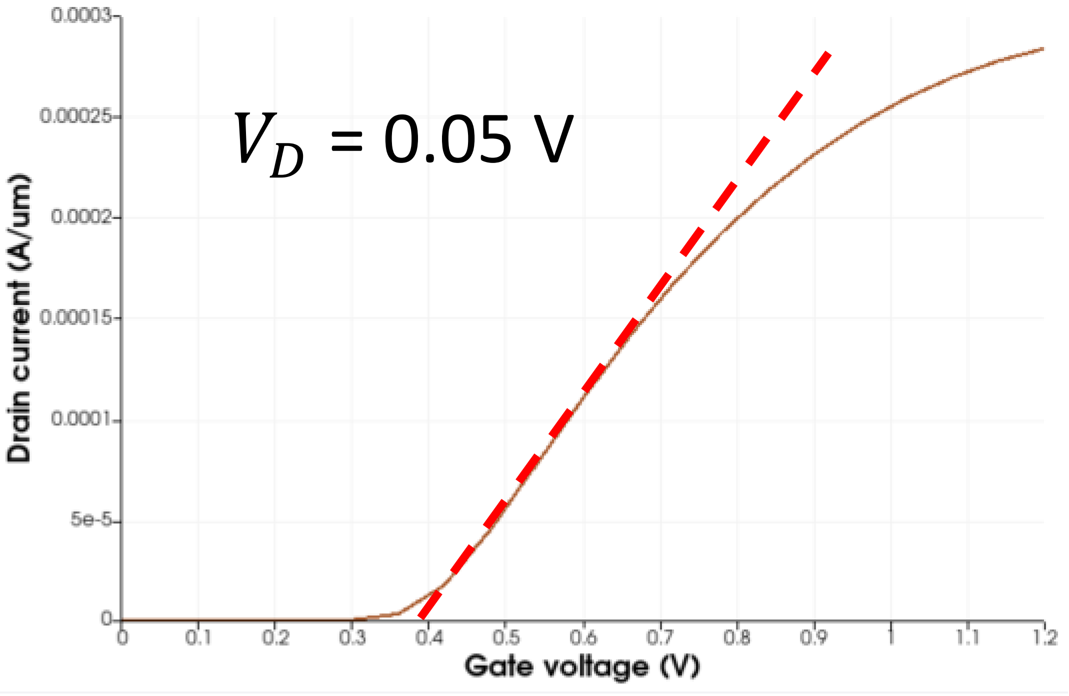
- Physical models included
  - Note that $I_D \propto \frac{1}{L}$.



Reduction of V_{TH}, even at a low V_D

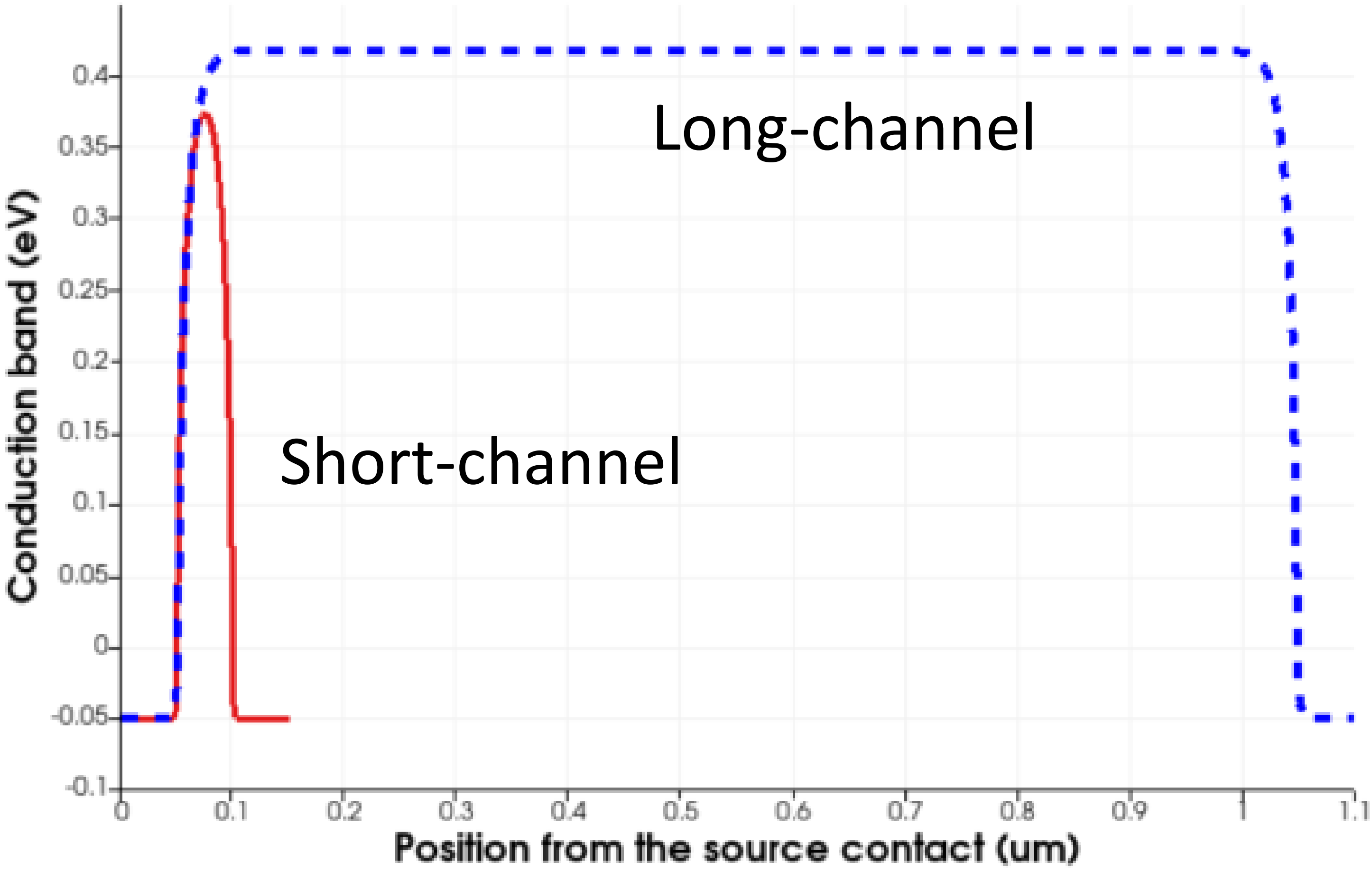
- For a short-channel device, the threshold voltage decreases.
  - ~ 0.45 V (Long-channel)
  - ~ 0.4 V (Short-channel)





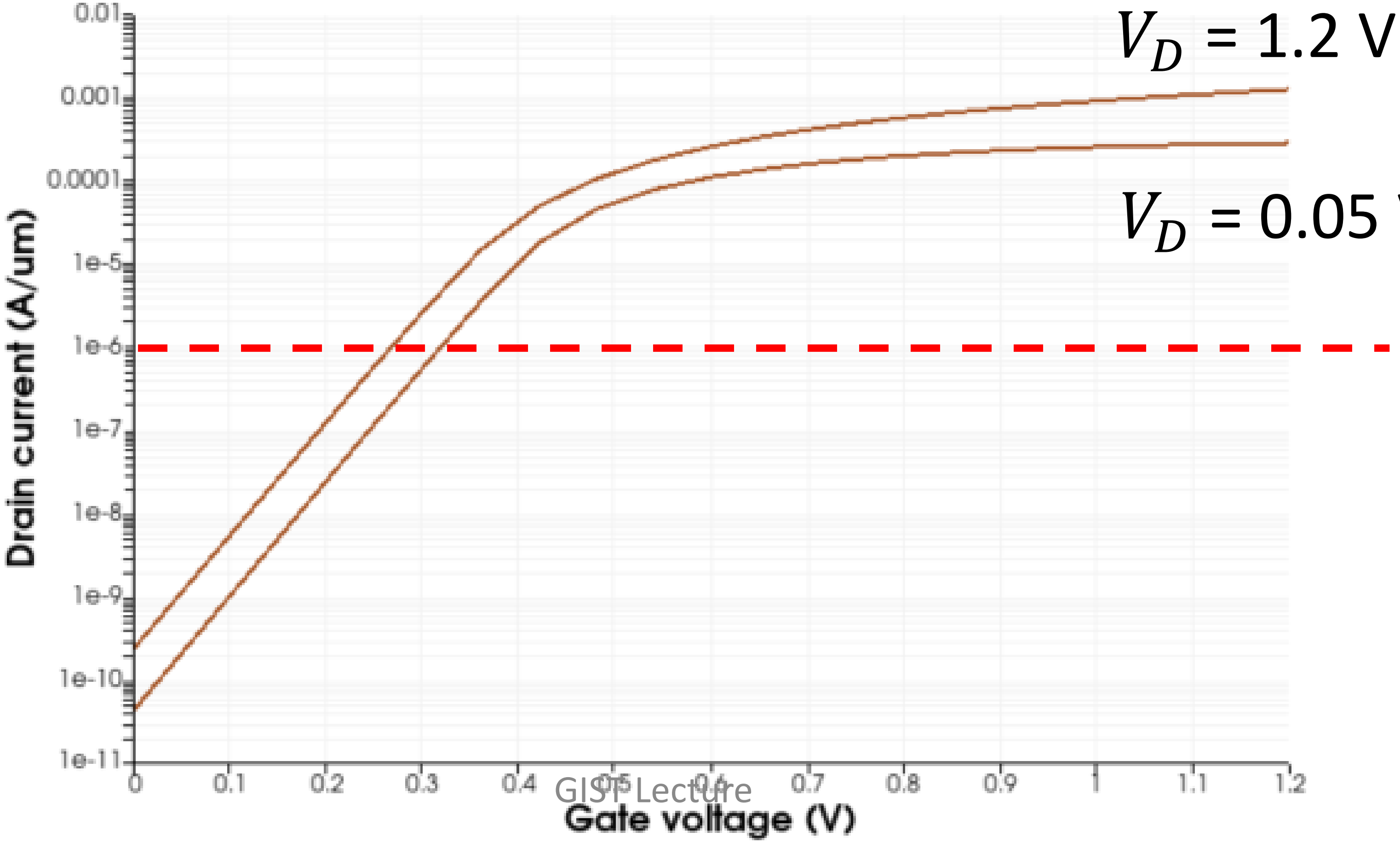
Charge sharing

- Even at $V_G = V_D = 0$ V, the conduction band profiles are different.



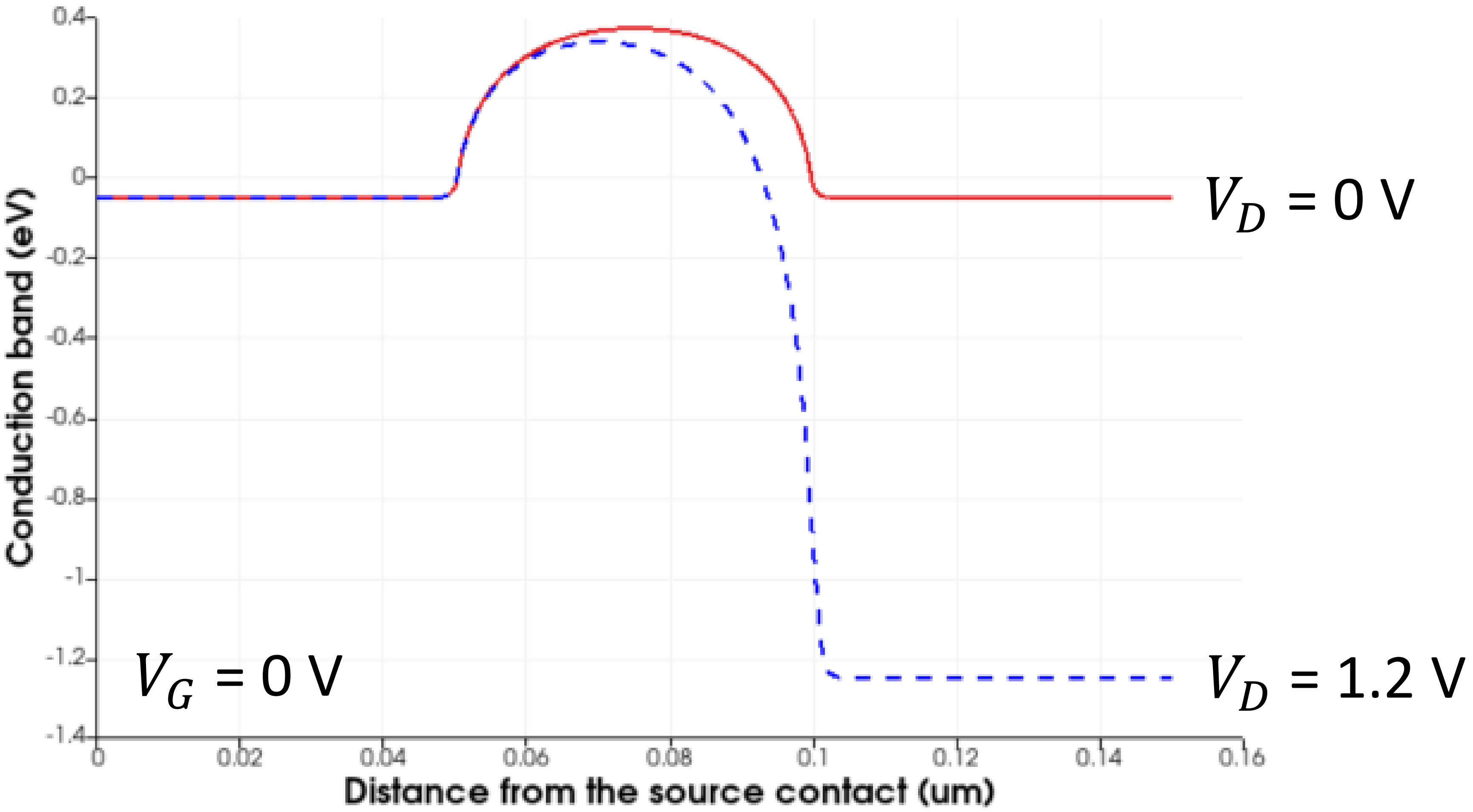
DIBL

- Much worse than the long-channel device
  - 45 mV/V @ I_D = 10^{-6} A/μm



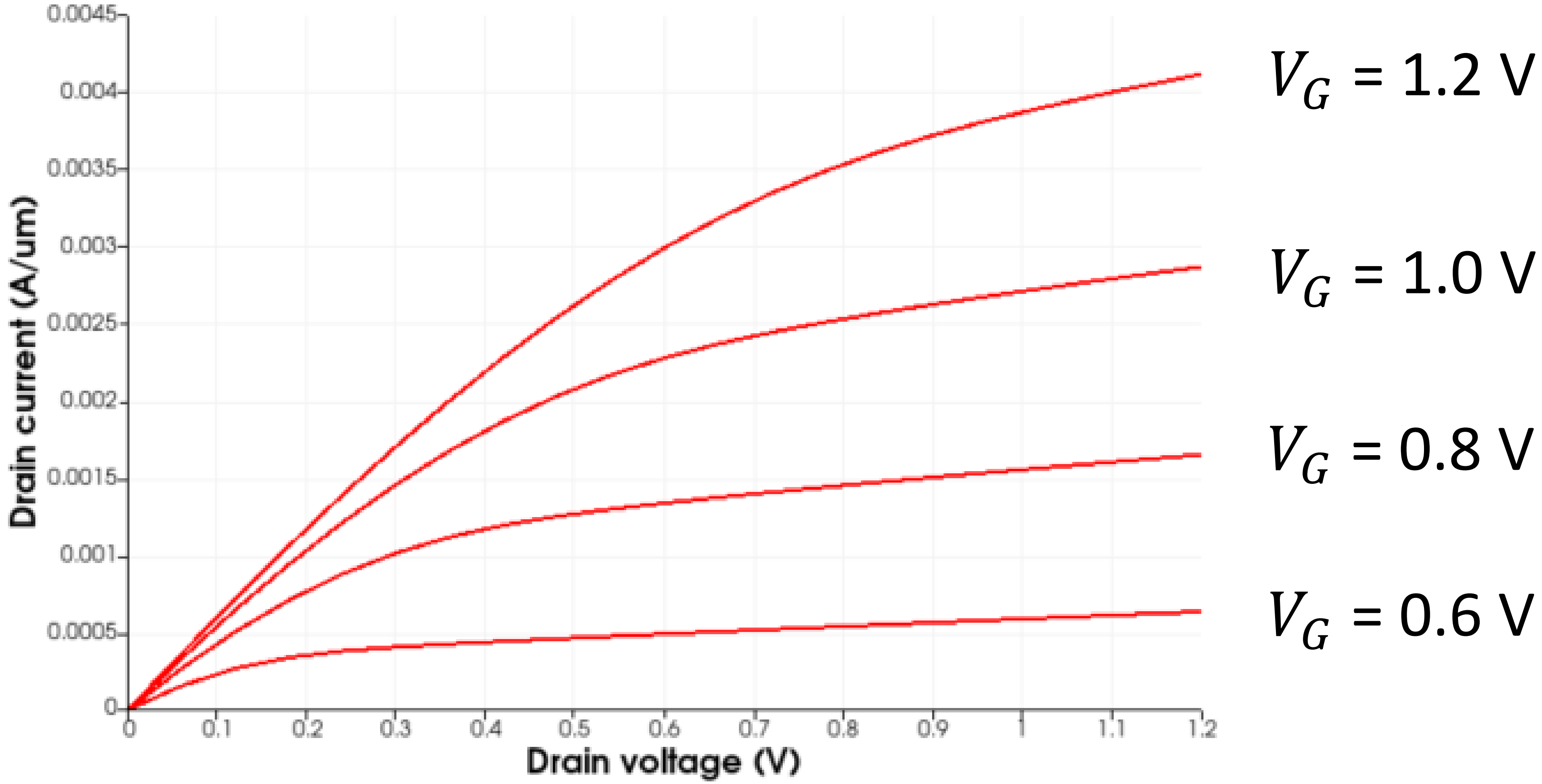
Conduction band

- At a high V_D, the energy barrier is further reduced.



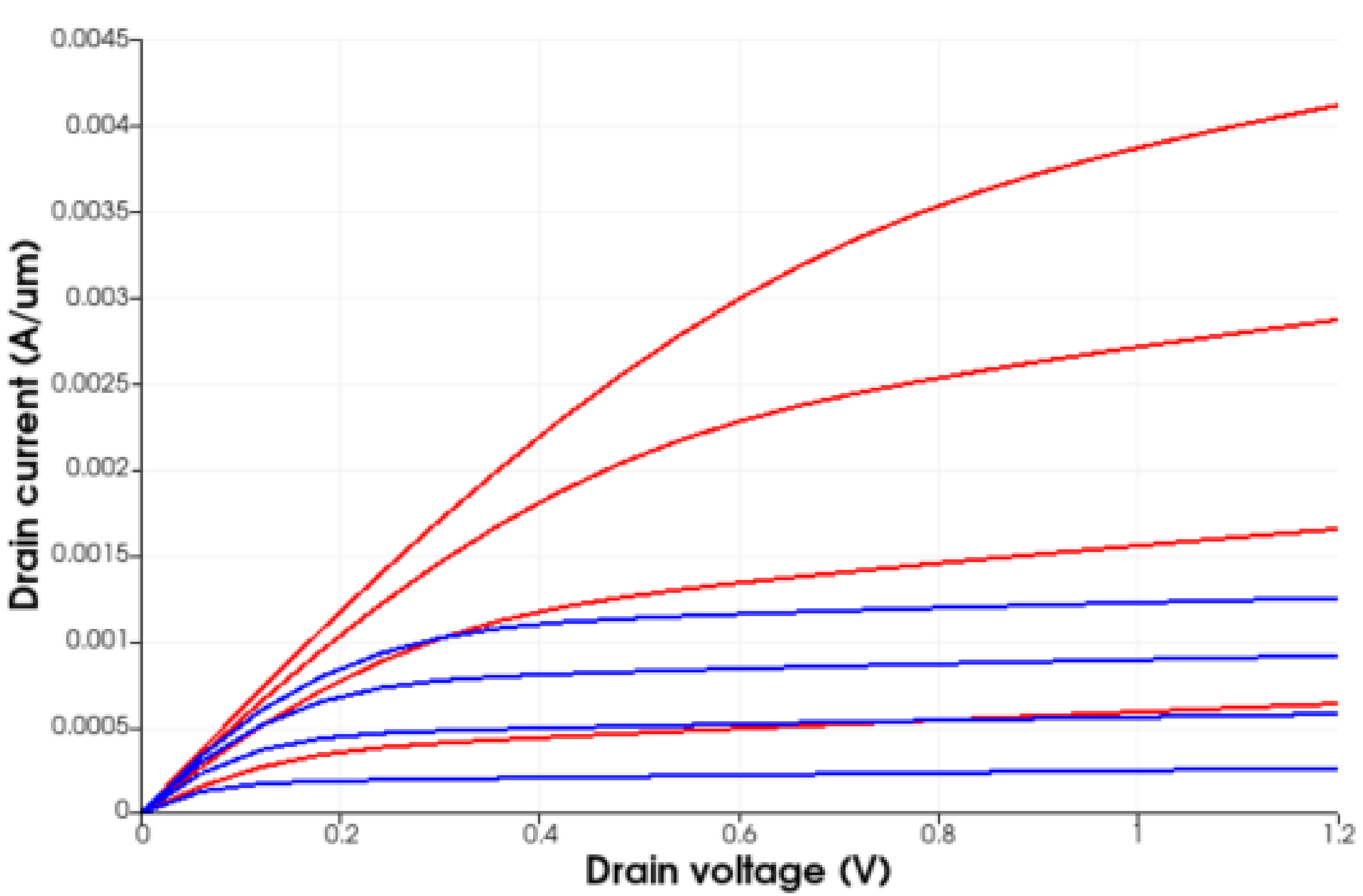
Channel-length modulation

- Results WITH inversion mobility model (No velocity saturation)



Velocity saturation

- Results WITH inversion mobility model + velocity saturation
  - Huge impact
  - Earlier saturation



Thank you!