Special Topics on Basic EECS I Design Technology Co-Optimization

Lecture 20

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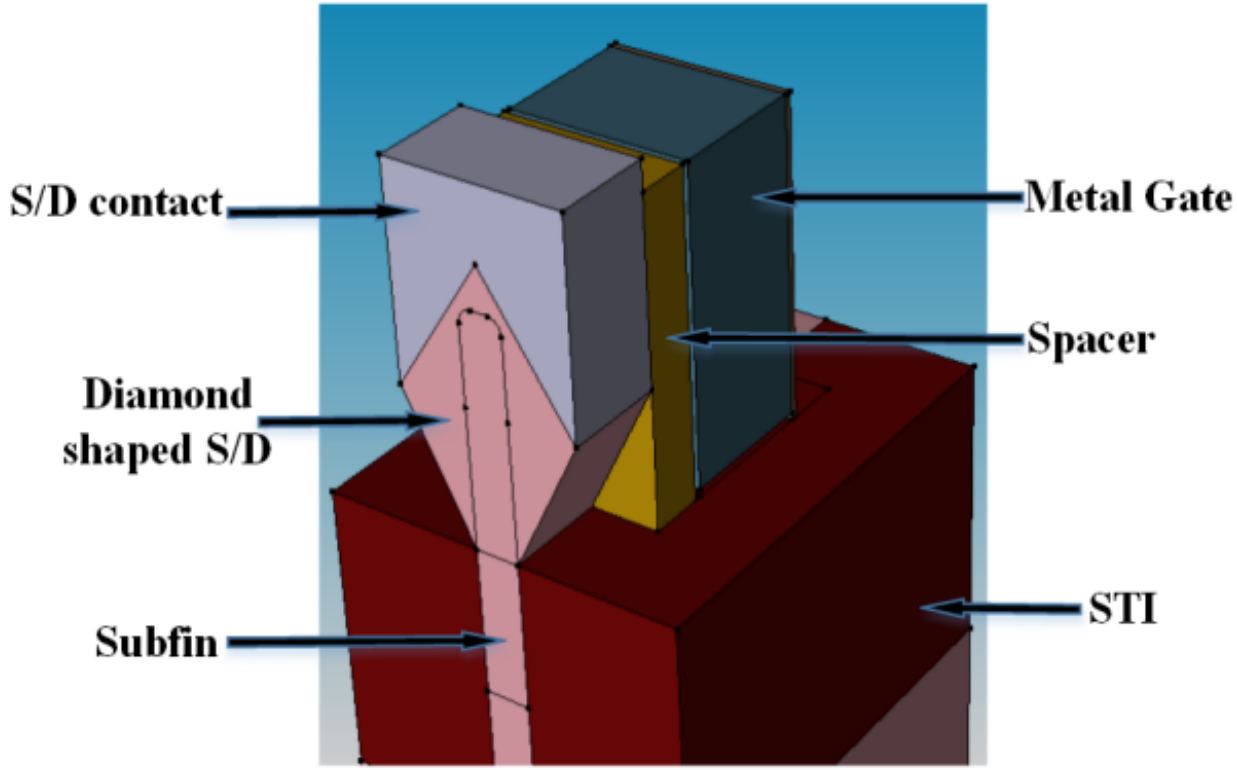
L20

Build a single NMOS FinFET.

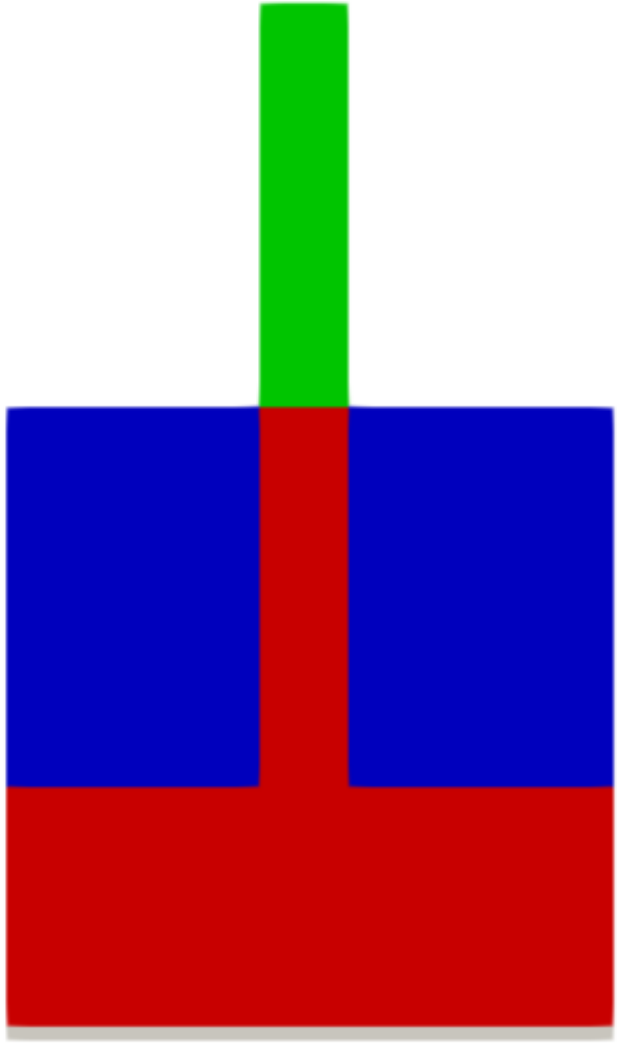
- A simplified version of our inverter example
  - Multples of 4
  - X: 108 (= 27 + 54 + 27) nm
  - Y: 48 (= 20+7+21) nm
  - ← Isolated from other fins
  - Prepare a fin. (32-nm-tall)



Device structure by ASAP7 PDK authors (V. Vashishtha et al., Arizona State University)

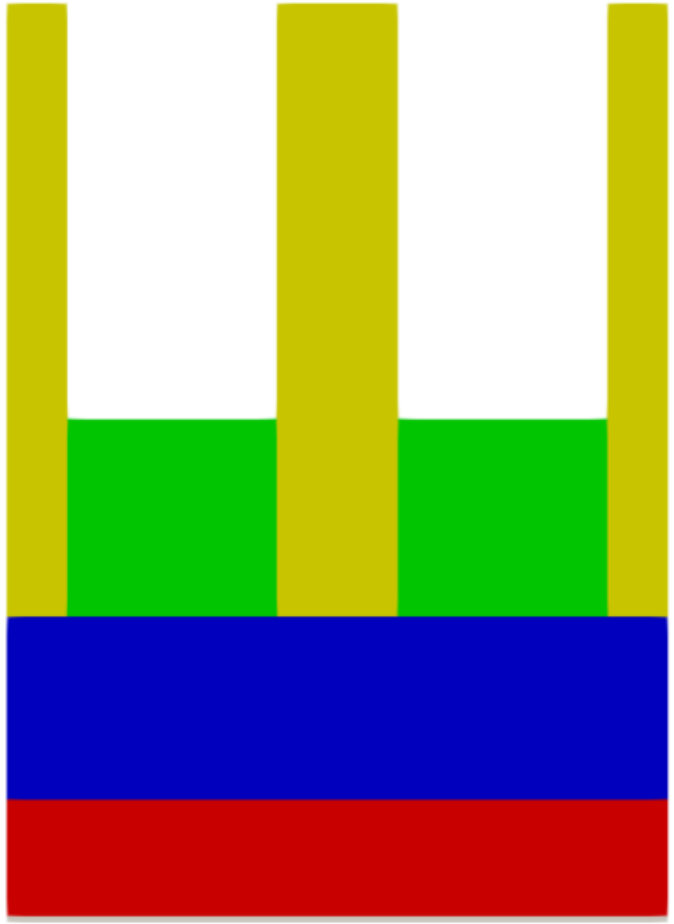
Now you can do it on your own.

- Fin & STI



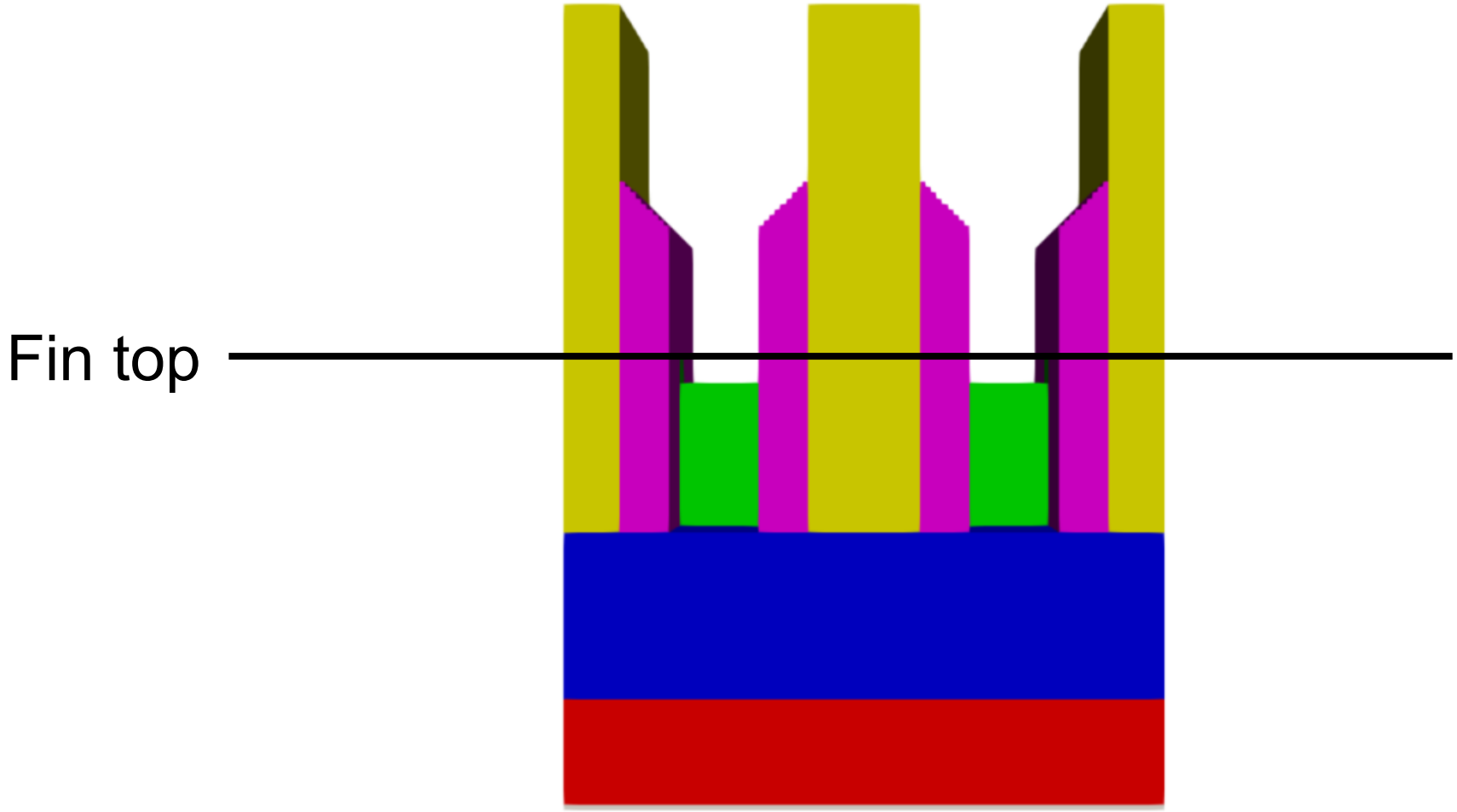
Dummy gates

- Hard masks are not considered explicitly.
  - Treat dummy gates as dummy gate + hard masks.



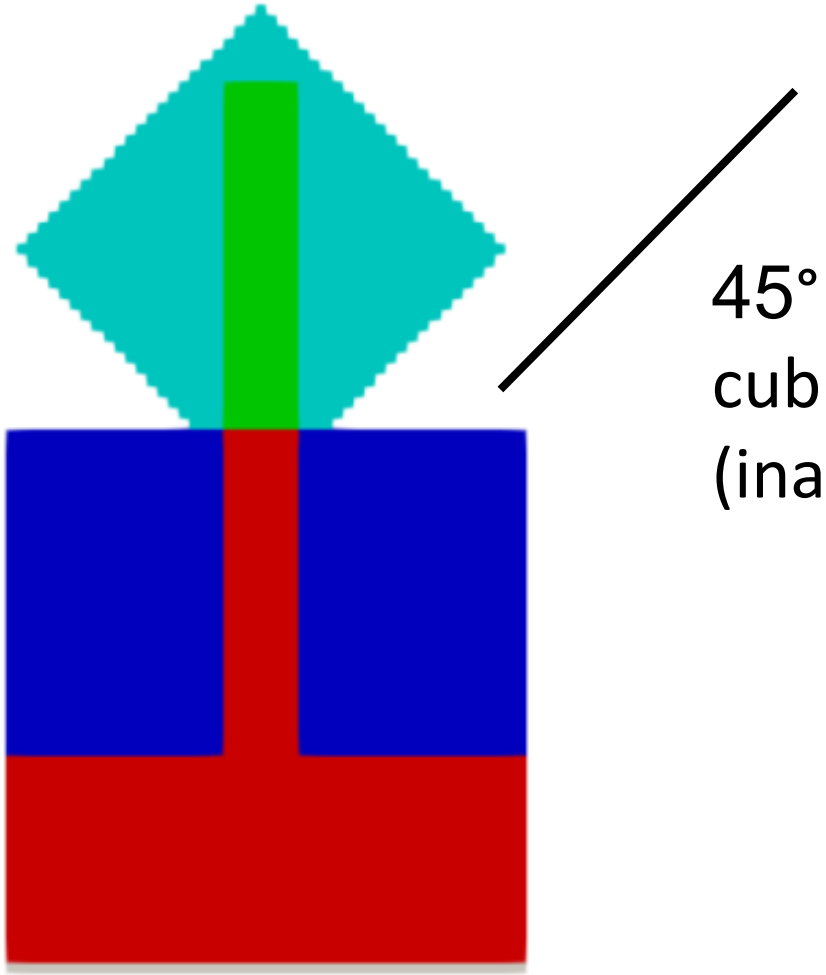
Spacer and fin recess

- Shallow fin recess (5 nm)



S/D epitaxial growth

- For the isolated fin, we allow to grow sufficiently.
  - Skip the salicide.

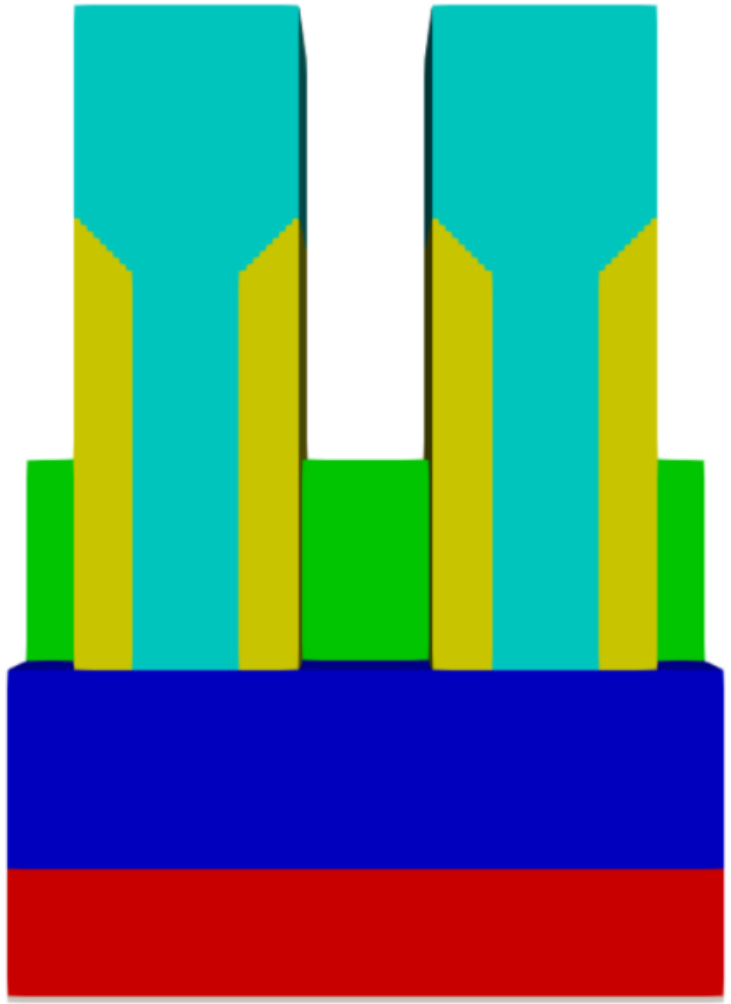


45° due to cubic voxels (inaccurate)

(Dummy gates and spacers are not shown.)

Dummy gate removal

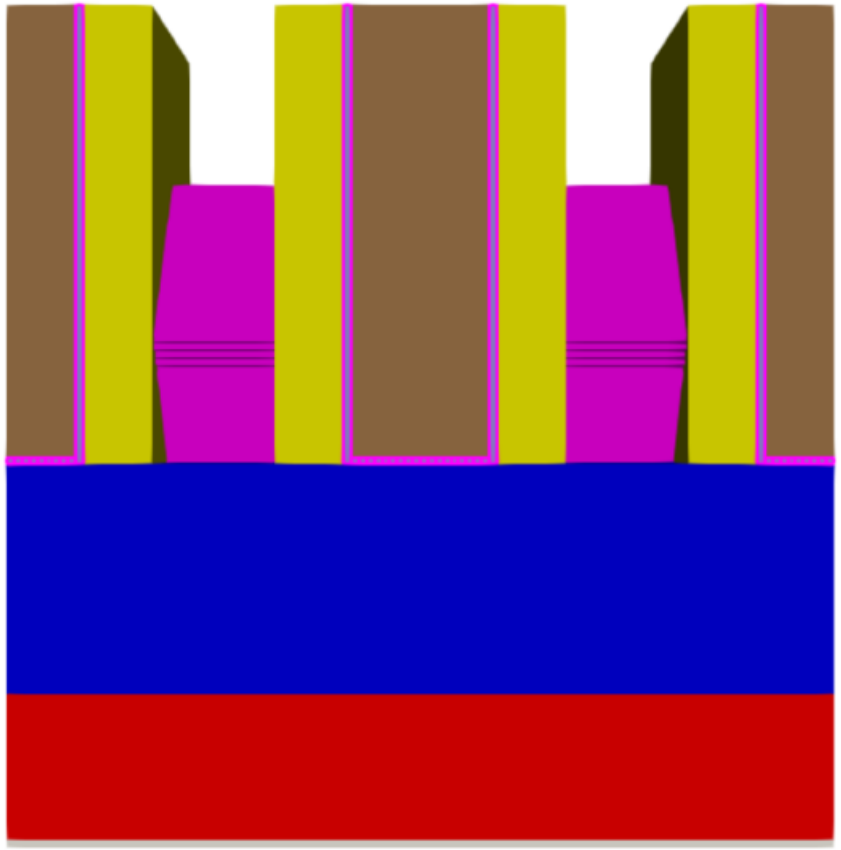
- After ILD0 deposition, remove the dummy gates.



1-nm-thick oxide (isotropically)

- Then, tungsten fill (End of FEOL)
  - Final height (from the STI top) is 60 nm.

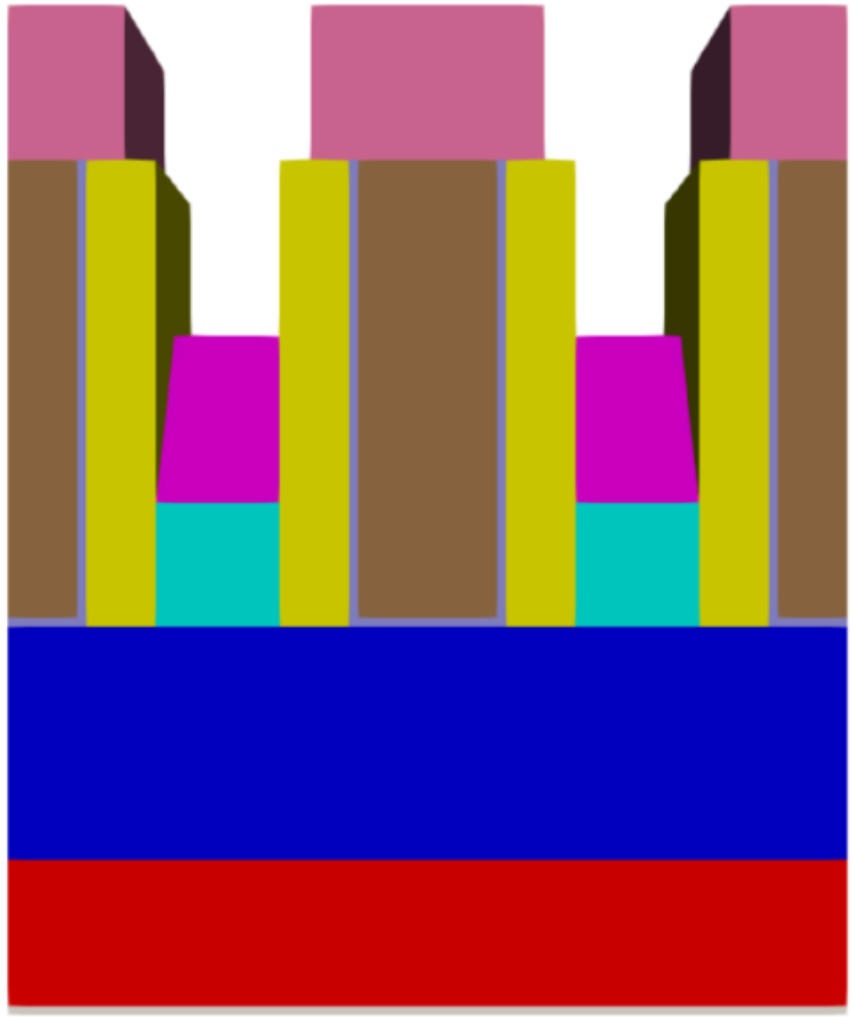
Gate dielectric
(Its thickness is not correct.)



(ILD0s are not shown.)

ILD1 & S/D contact

- 20-nm-thick ILD1, then etch ILDs (with patterns).
  - Robust against mismatch
    (5 nm in this example)
  - Gate and S/D are quite close.



(S/D metals are not shown.)

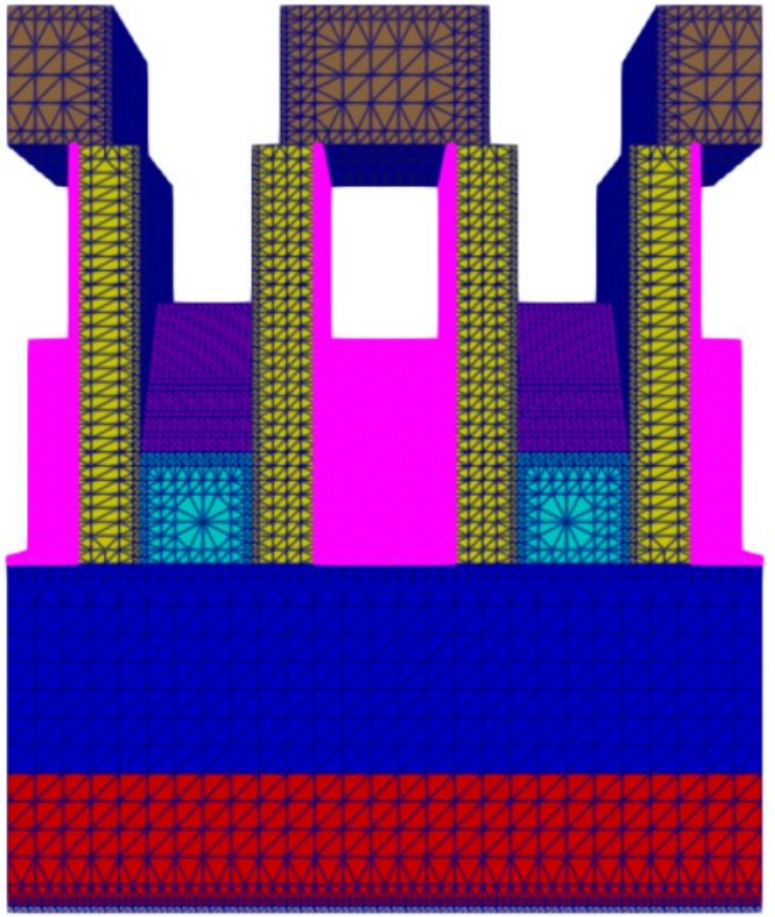
Construct a volume mesh.

- Depending on your naming convention, regions may have different names.
  - Top-level command and region specification (Do not include the metal regions.)

```
mesh (lx=108,ly=48,lz=200,nx=108,ny=48,nz=200,nresolution=3,mapmaker,load="FinFET.cgns",save="mesh.cgns") {
  region (material="Si",name="deepsubstrate",resolution=2)
  region (material="Si",name="Si_Bulk",resolution=2)
  region (material="Si",name="Si",resolution=0)
  region (material="SiO2",name="SiO2",resolution=2)
  region (material="Si3N4",name="SiN",resolution=2)
  region (material="Si",name="Si:P",resolution=1)
  region (material="SiO2",name="ILD0",resolution=2)
  region (material="SiO2",name="gatedielectric",resolution=0)
  region (material="SiO2",name="ILD1",resolution=2)
```

Only volume regions

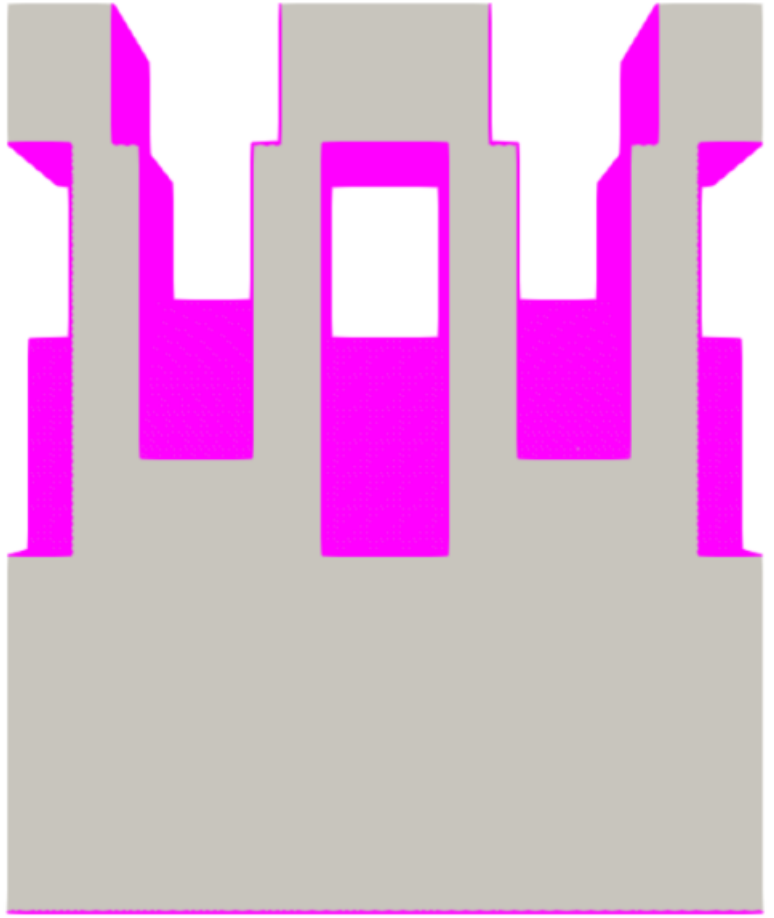
- In this example, we have 160 k vertex points.
  - In the present implementation, a thin and wide region takes many vertex points.
  - Gate dielectric ~ 30 k
  - Spacers ~ 50 k



Contacts

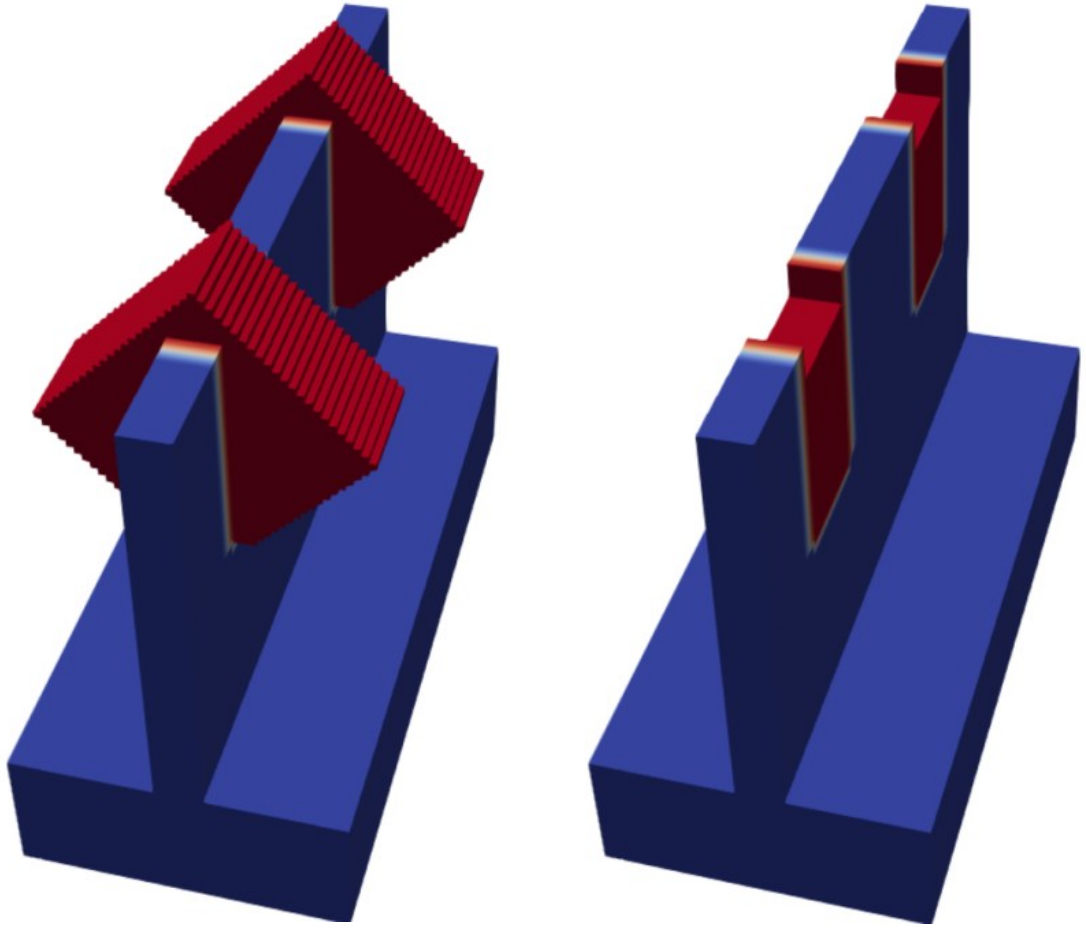
- Assign contacts.
  - We must separate source and drain contacts. (Fortunately, our previous input file works properly.)

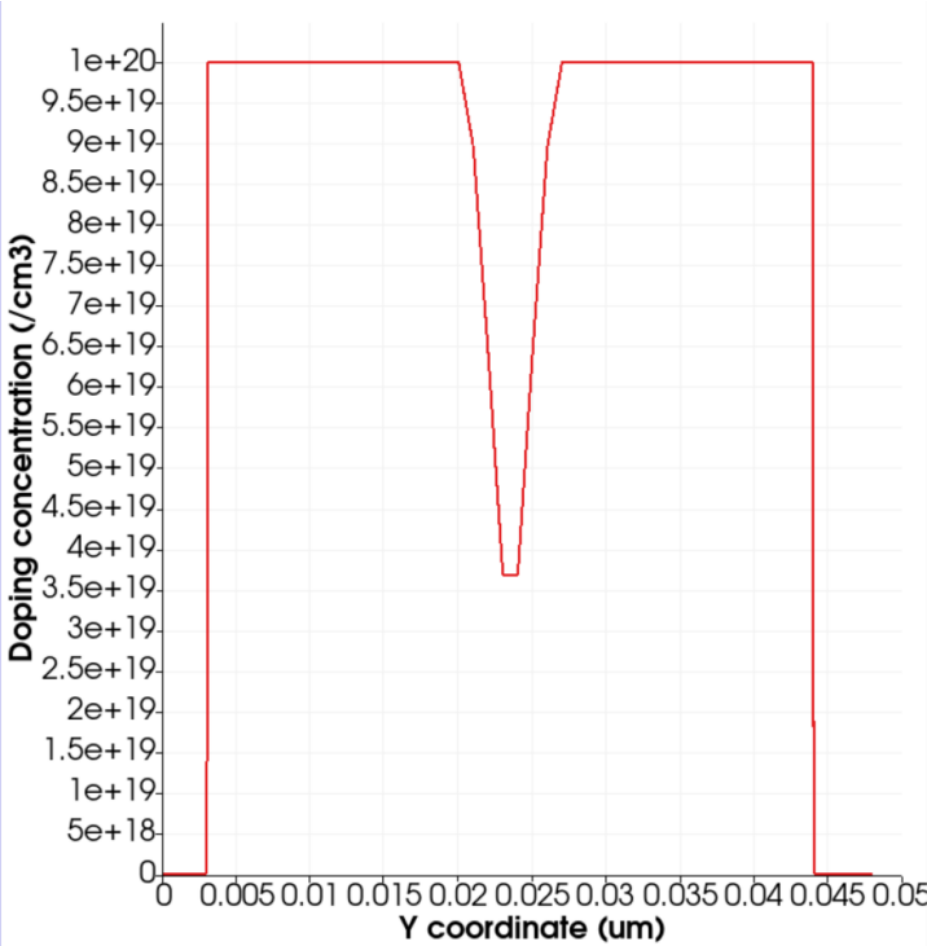
```
contact (name="gate_contact",type="this",region="gate")
contact (name="body_contact",type="side",region="deepsubstrate",zmin)
contact (name="sd_contact",type="this",region="MOL_metal")
selectcontact (input="sd_contact",output="source_contact",xmin=0)
selectcontact (input="sd_contact",output="drain_contact",xmax=0)
removecontact (name="sd_contact")
```



Doping

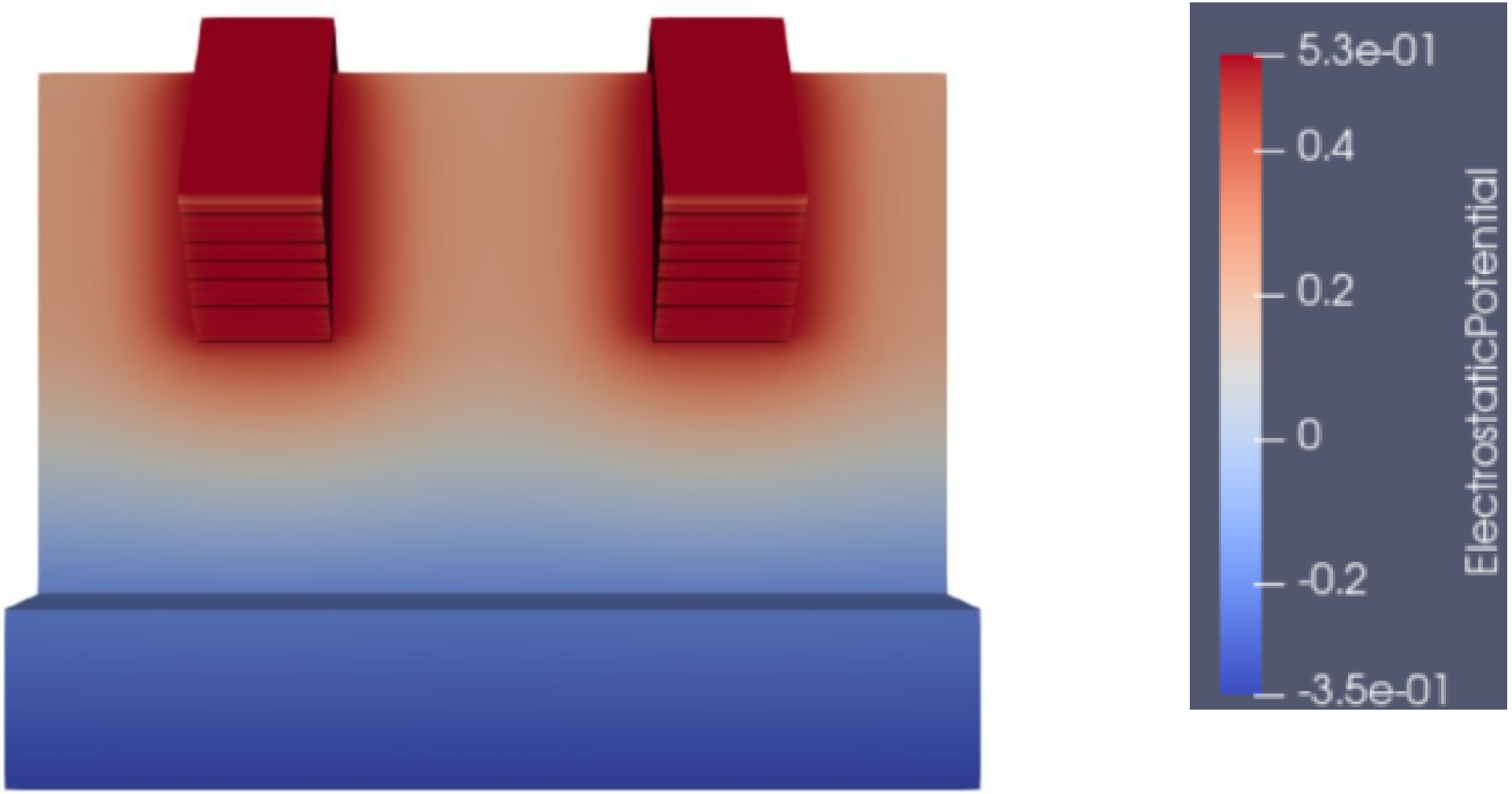
- Detect the interface between Si:P regions and the fin.
  - Gaussian profile with σ = 3 nm





Equilibrium solution

- Test your structure.



Thank you!