

Special Topics on Basic EECS I Design Technology Co-Optimization

Lecture 9

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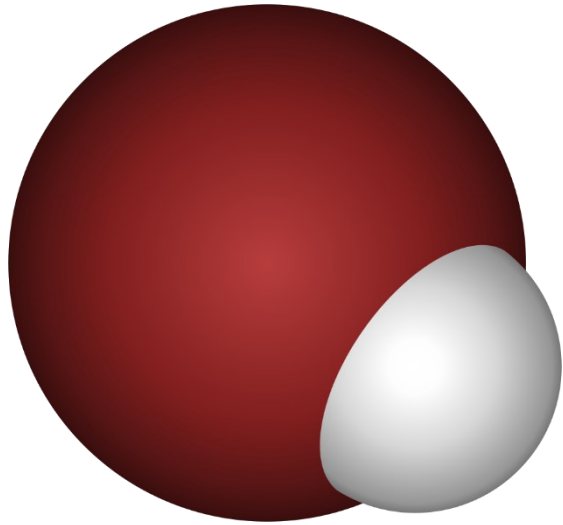
Department of Electrical Engineering and Computer Science

Gwangju Institute of Science and Technology (GIST)

L9

Silicon fin

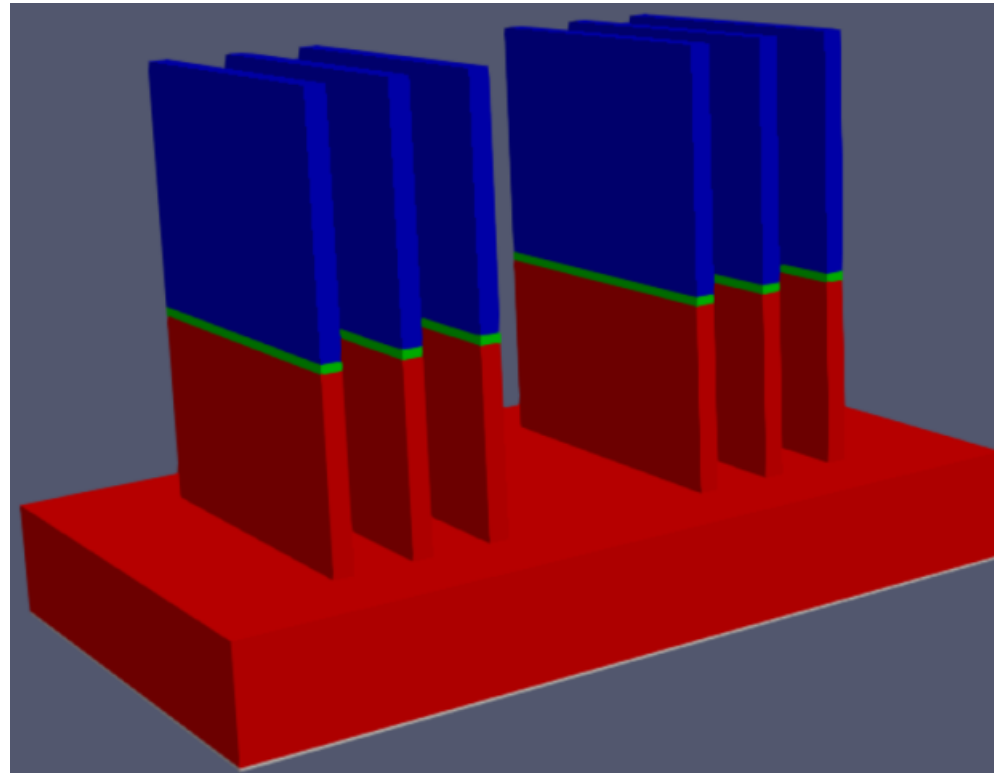
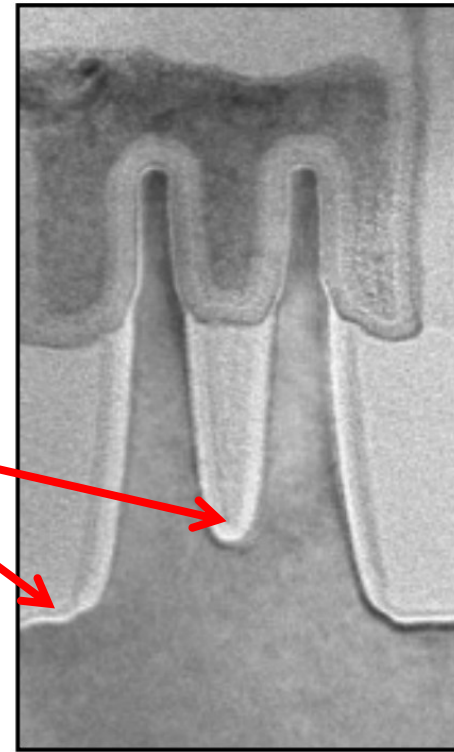
- Target fin height = 32 nm
 - Moreover, the STI depth is 30 nm.
(Our etched profile is too ideal.)
(Too thick hard mask?)



Hydrogen bromide (Wikipedia)

12-nm-node fin
image (Intel)

Etch depth



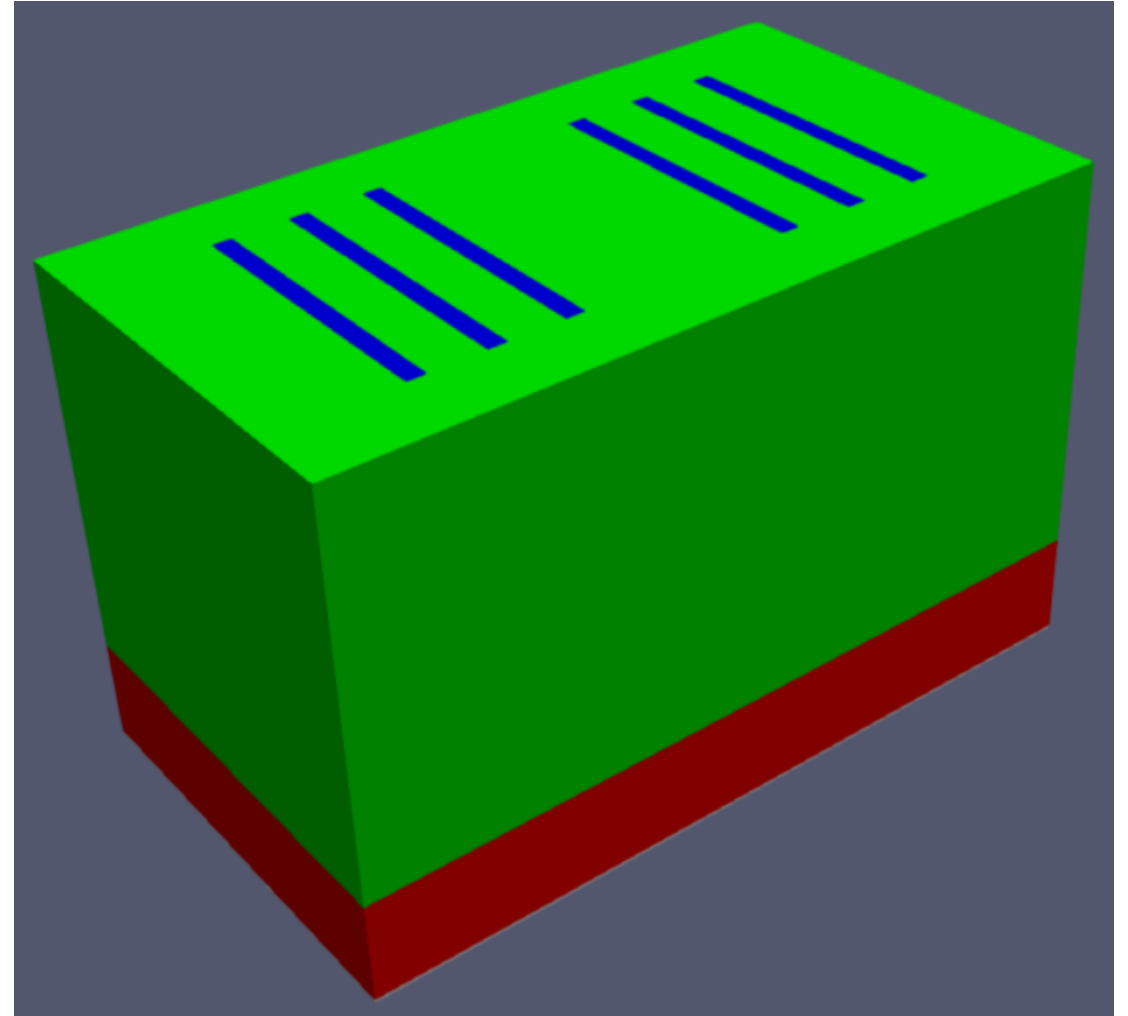
Fill the STI (shallow trench isolation).

- 100-nm-thick
 - Then, CMP (Chemical mechanical polishing)

```
depo (region="SiO2",thickness=100)
```

```
cmp (position=183)
```

Hard maks (Si_3N_4) as
the CMP stop layer



Fin reveal

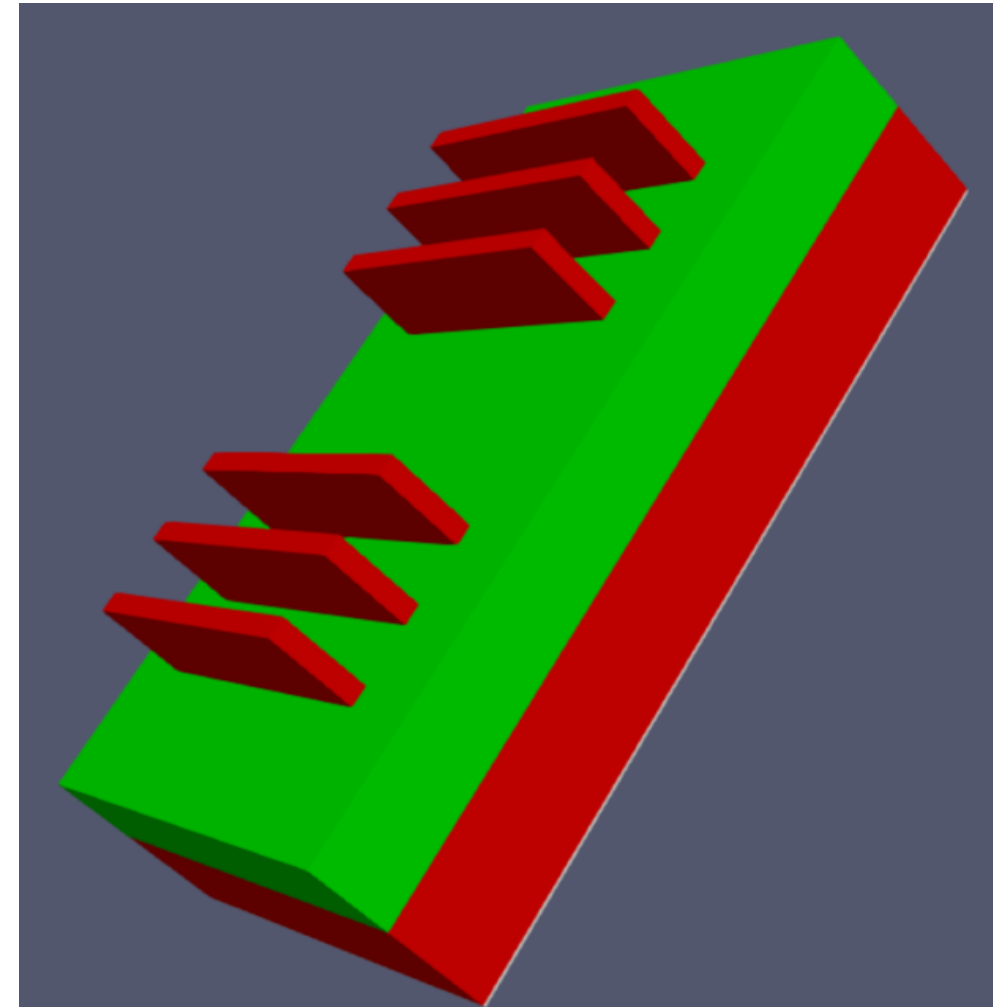
- Now, the STI is etched.
 - Then, fins are revealed.
 - For simplicity, anisotropic etch

```
etch (model="model_SiO2",thickness=112)
```

```
etch (model="model_Si3N4",thickness=80)
```

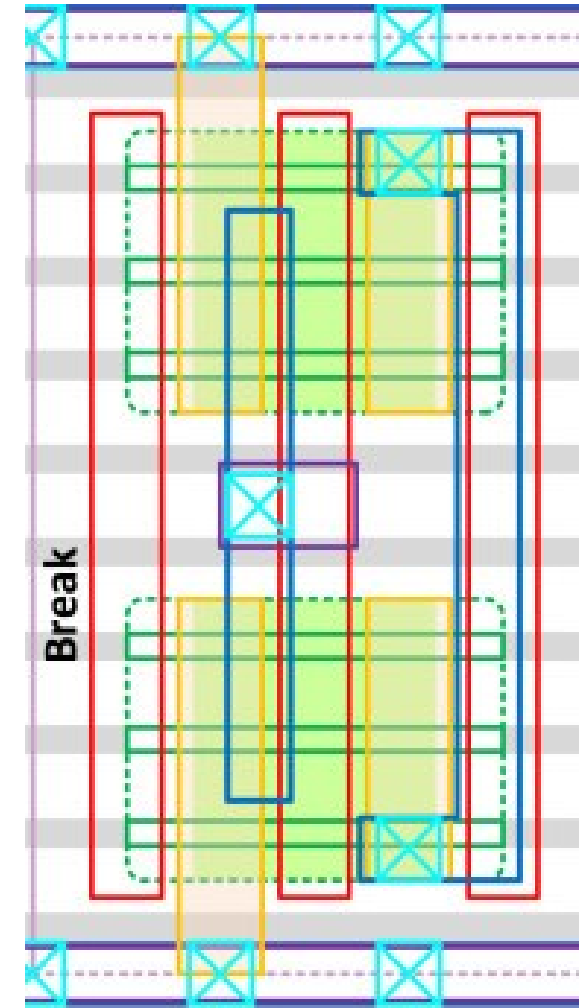
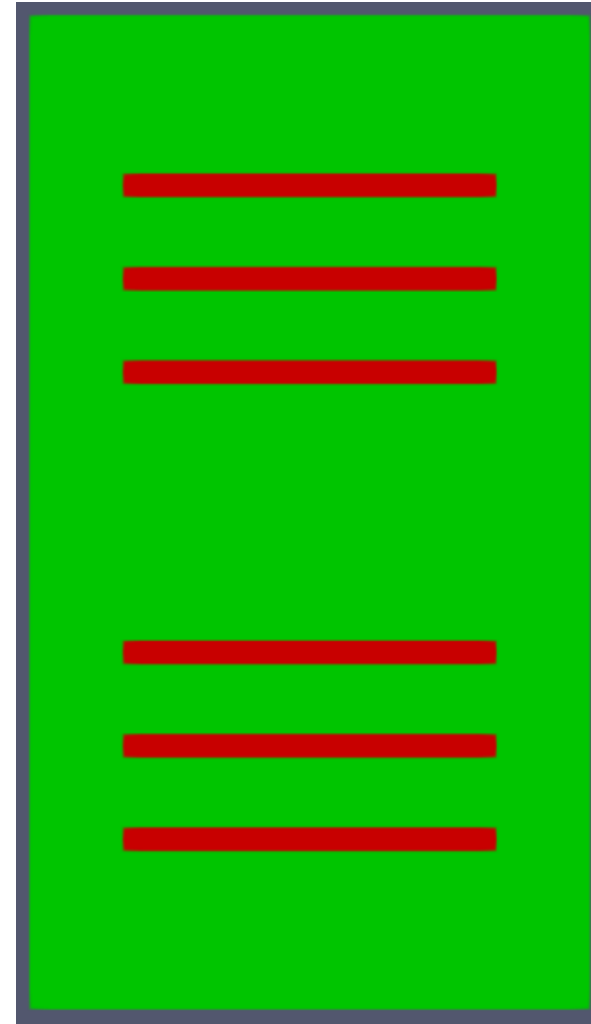
```
etch (model="model_SiO2",thickness=3)
```

(The final structure is highly idealized.)



Lessons from process emulation

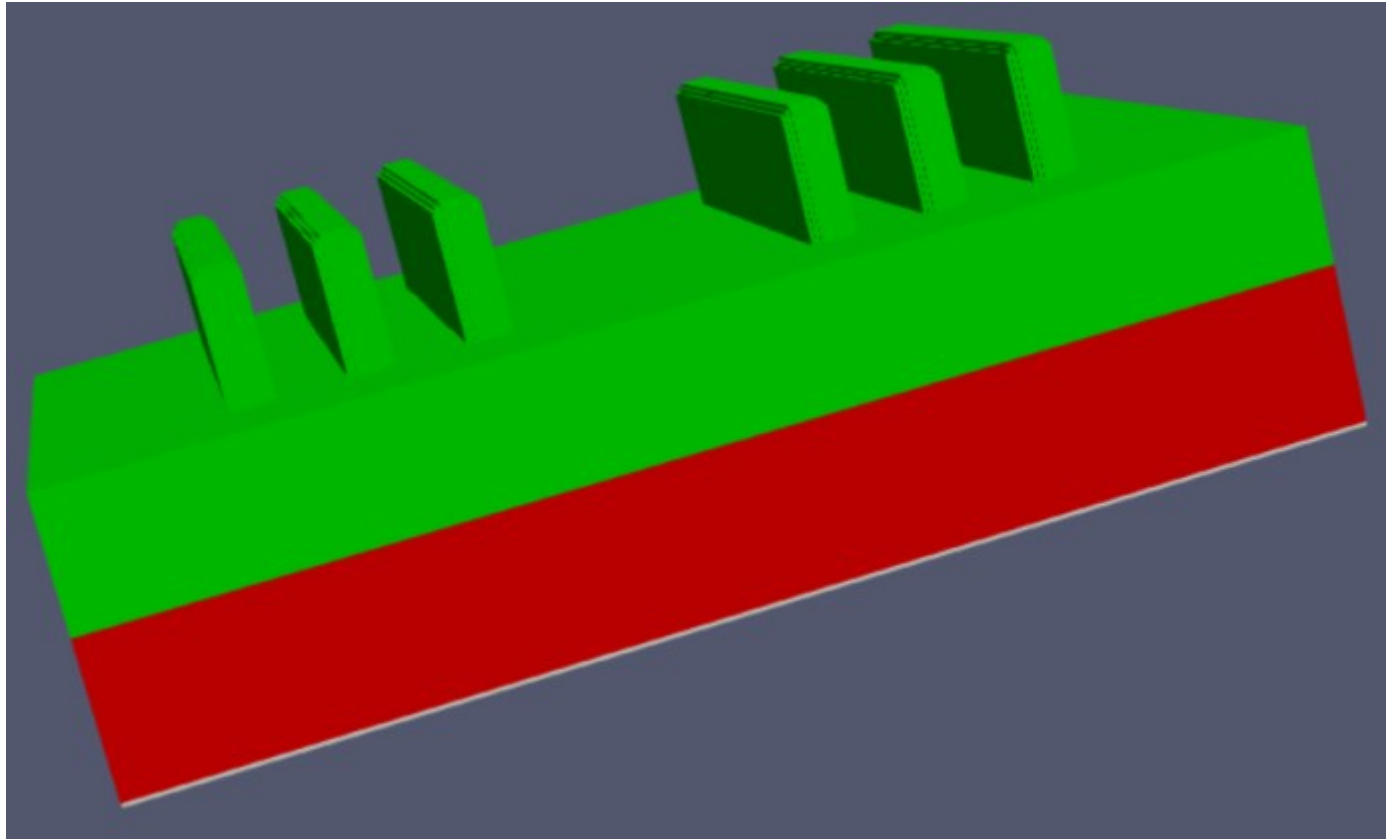
- We have just done the “fin patterning.”
 - It is very easy to say.
 - However, several intermediate steps were required...
 - Our structure is far from the realistic one.
- Anyway, much better than nothing!



Inverter layout
(ASAP7 PDK)

Dummy dielectric

- The thickness of this SiO_2 layer is 2 nm.
 - Protection of fins

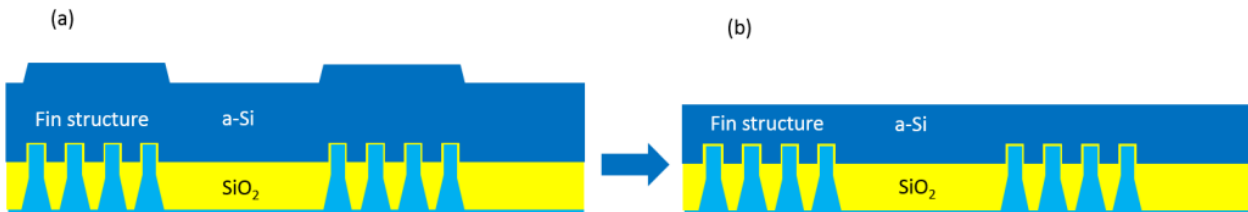


Dummy gate

- The target thickness of this amorphous silicon layer is 95 nm.
 - Thickness controlled by the CMP (Is it mandatory or not?)

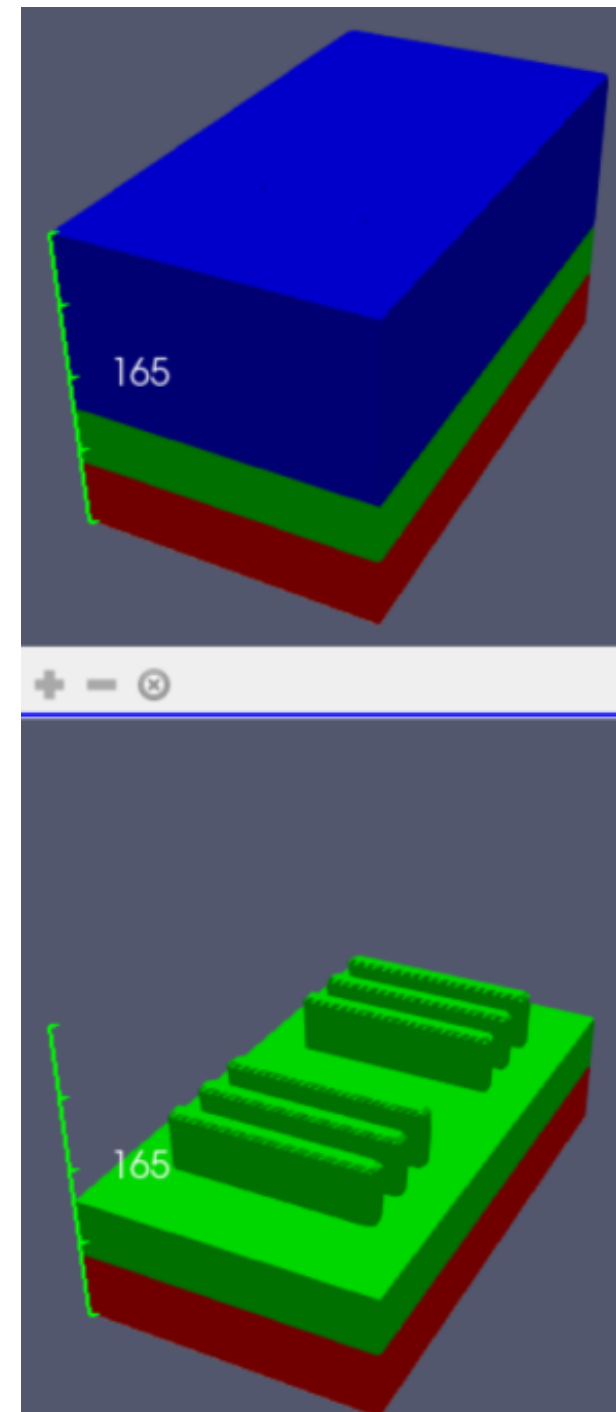
```
depo (region="AmorphousSilicon",thickness=100)
```

```
cmp (position=165)
```



FinFET process flow before/after a-Si
CMP process (IMEC)

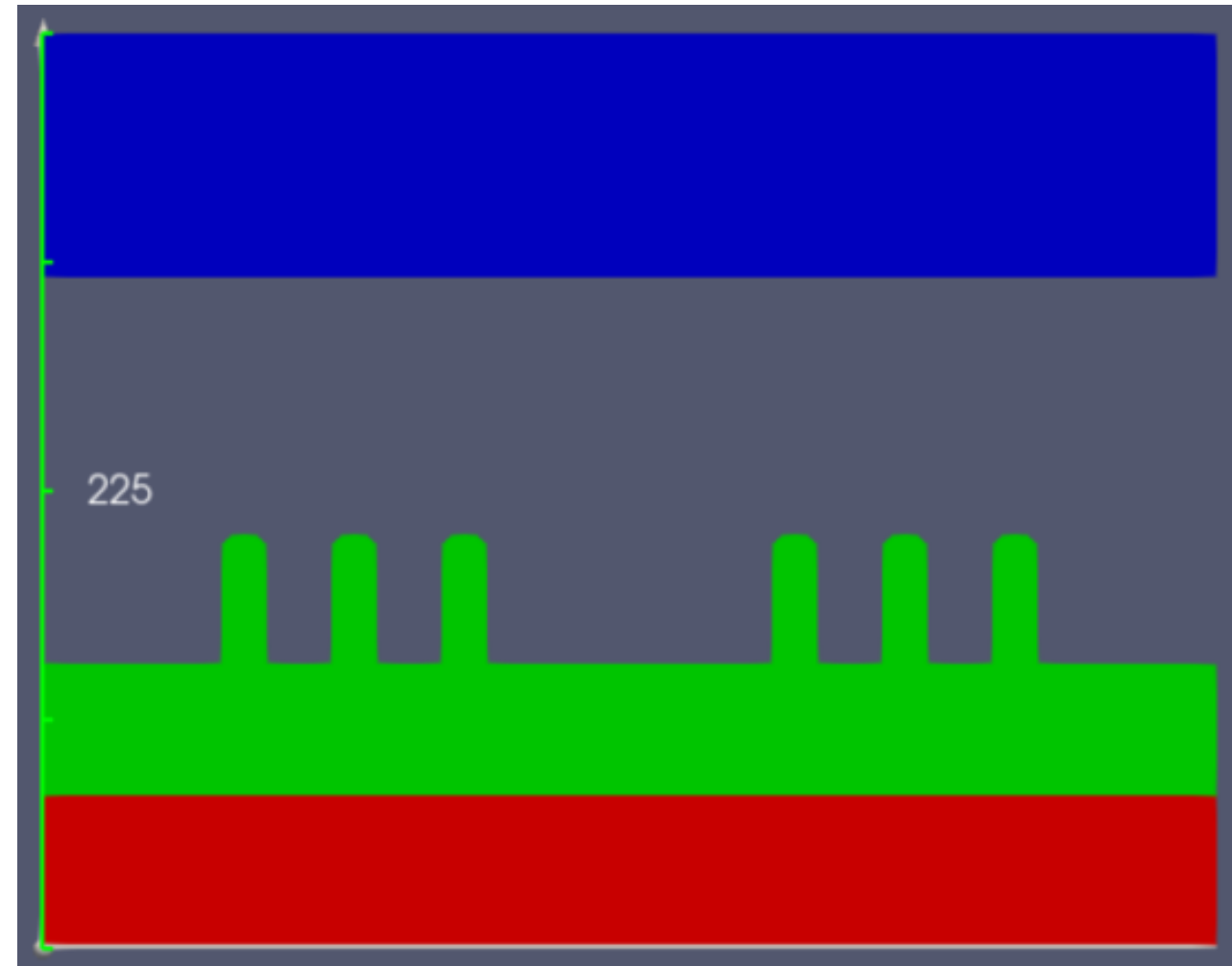
GIST Lecture



Hard mask on dummy gate

- 60 nm
 - Again, Si_3N_4
(Dummy gates are not drawn intentionally.)

```
depo (region="Si3N4",thickness=60)
```



Now, dummy gate patterning

- Actually, another SADP.

- It means:

- Mandrel layer

- Photoresist layer

- PR patterning

- Mandrel etching

- Sidewall deposition

- Anisotropic etching

- Mandrel removal

- Hard mask etching

- *Let's skip them all!*

Table 1. Key layer lithography assumptions, widths and pitches.

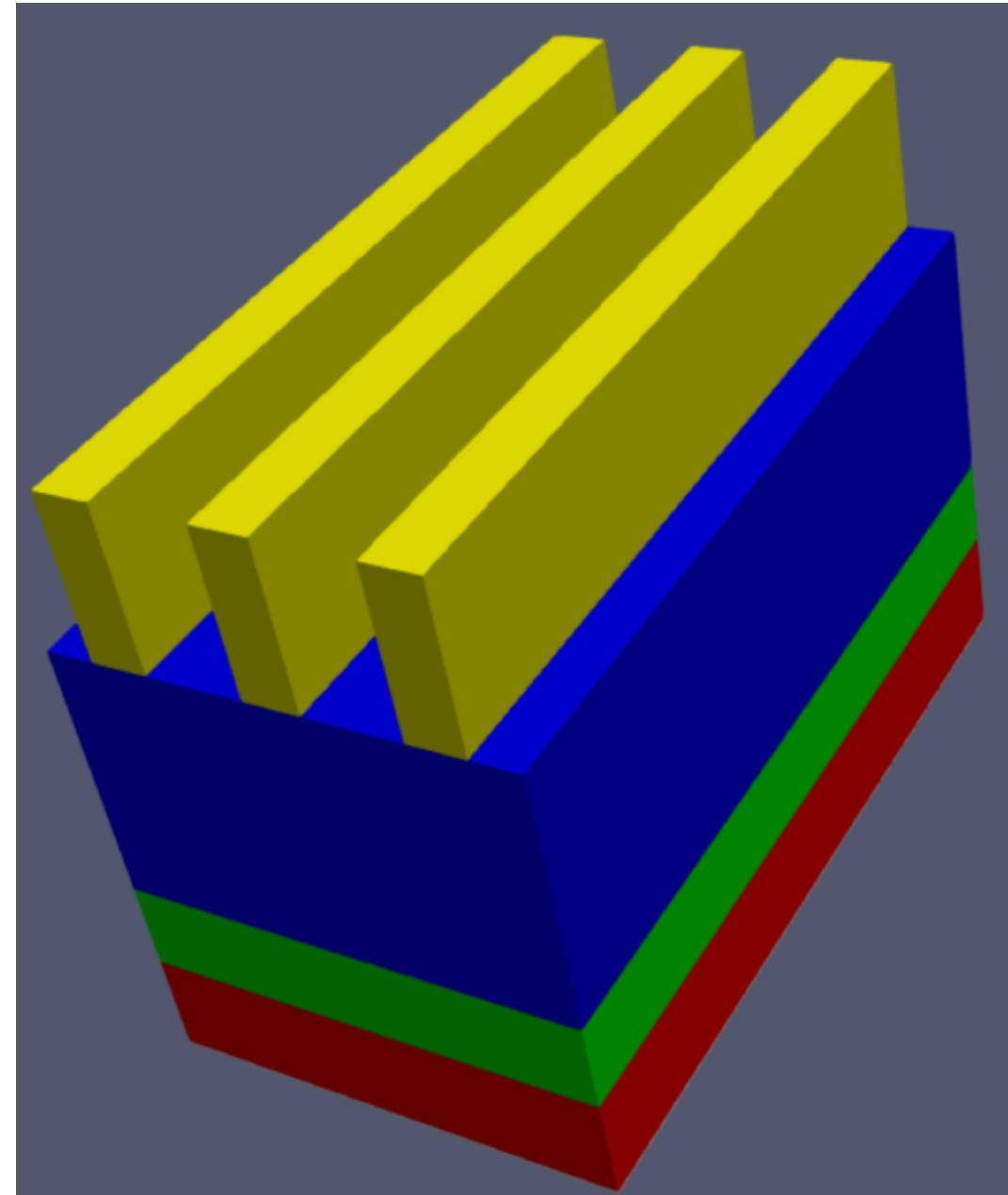
Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54 ^b
LIG	EUV	16/16	54
VIA0–VIA3	EUV	18/18	25 ^a
M1–M3	EUV	18/18	36
M4 and M5	SADP	24/24	48
VIA4 and VIA5	LELE	24/24	34 ^a
M6 and M7	SADP	32/32	64
VIA6 and VIA7	LELE	32/32	45 ^a
M8 and M9	SE	40/40	80
VIA8	SE	40/40	57 ^a

Hard mask patterned

- Structure after those steps
 - 20-nm-thick pattern
 - Gate pitch is 54 nm.

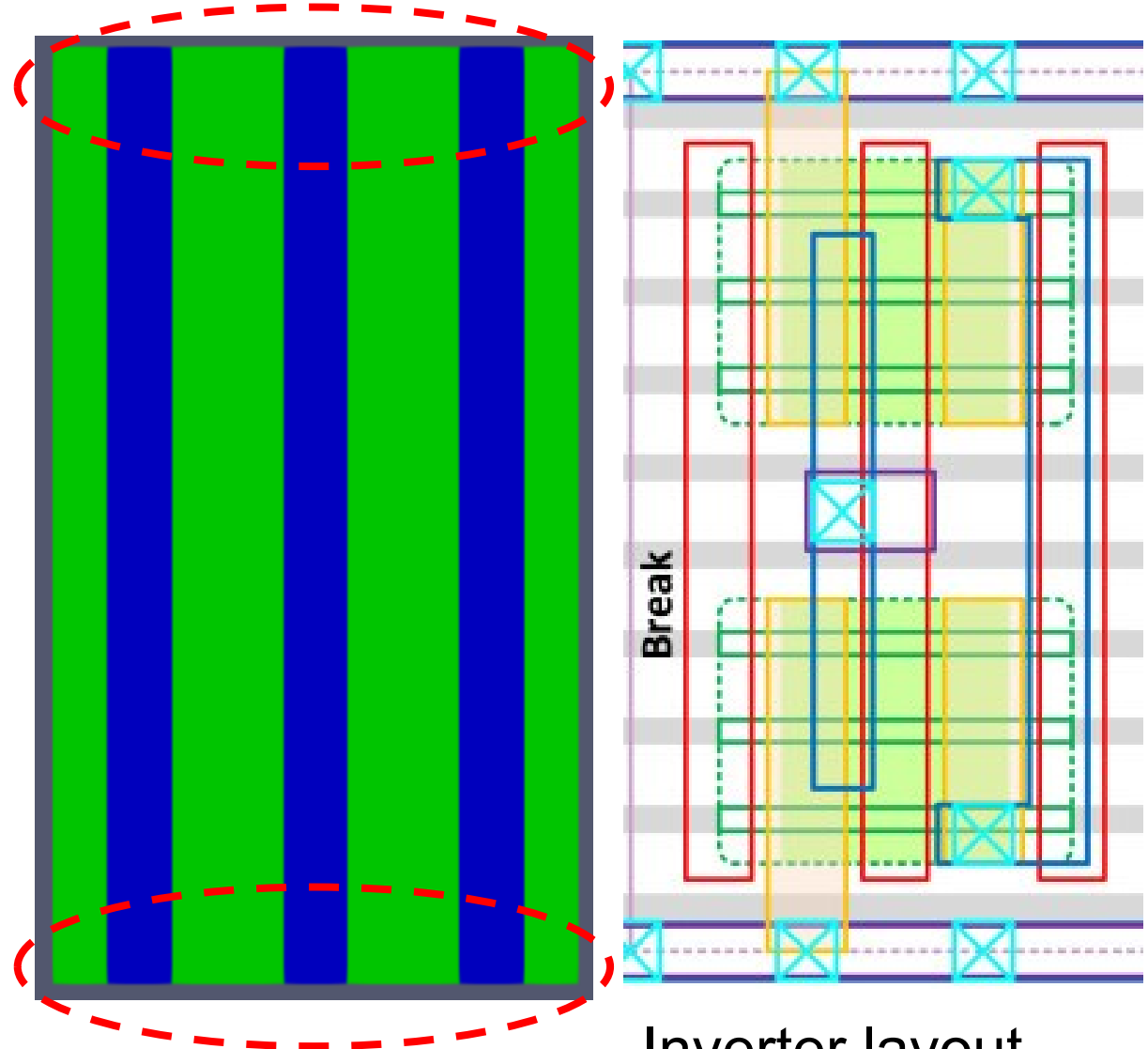
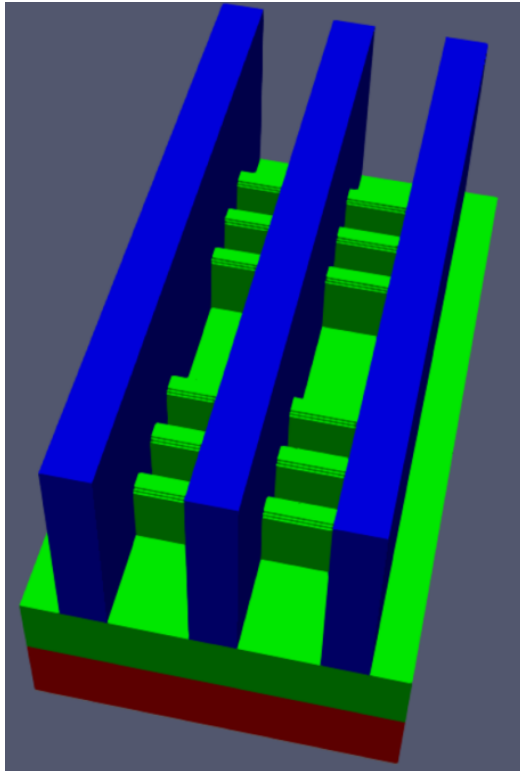
```
mask (name="mask_dummygate") {  
    rectangle (x0= 17,y0=0,x1= 37,y1=288)  
    rectangle (x0= 71,y0=0,x1= 91,y1=288)  
    rectangle (x0=125,y0=0,x1=145,y1=288)  
}  
  
etch (mask="mask_dummygate",thickness=60)
```

- What's next? Dummy gate etching
(Your own exercise)



Dummy gate patterned

- The hard mask is also removed.
 - Distance between dummy gates is 34 nm.



Homework#9

- Due: 08:00 on Oct. 13
 - You may have plenty of time to make up.
- Submit a report through the GIST LMS system.
 - By using the AngstromCraft code, follow L9 lecture material.
 - Your report must show structures and the input file.

Thank you!