Special Topics on Basic EECS I Design Technology Co-Optimization

Lecture 14

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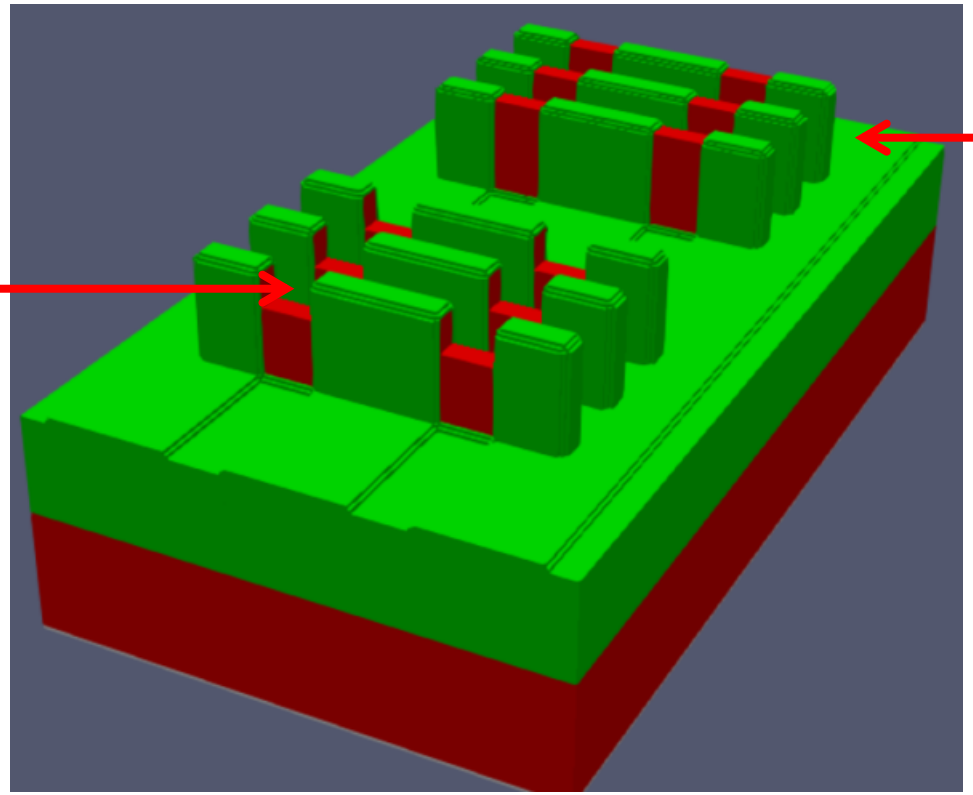
L14

NMOS cavity etch

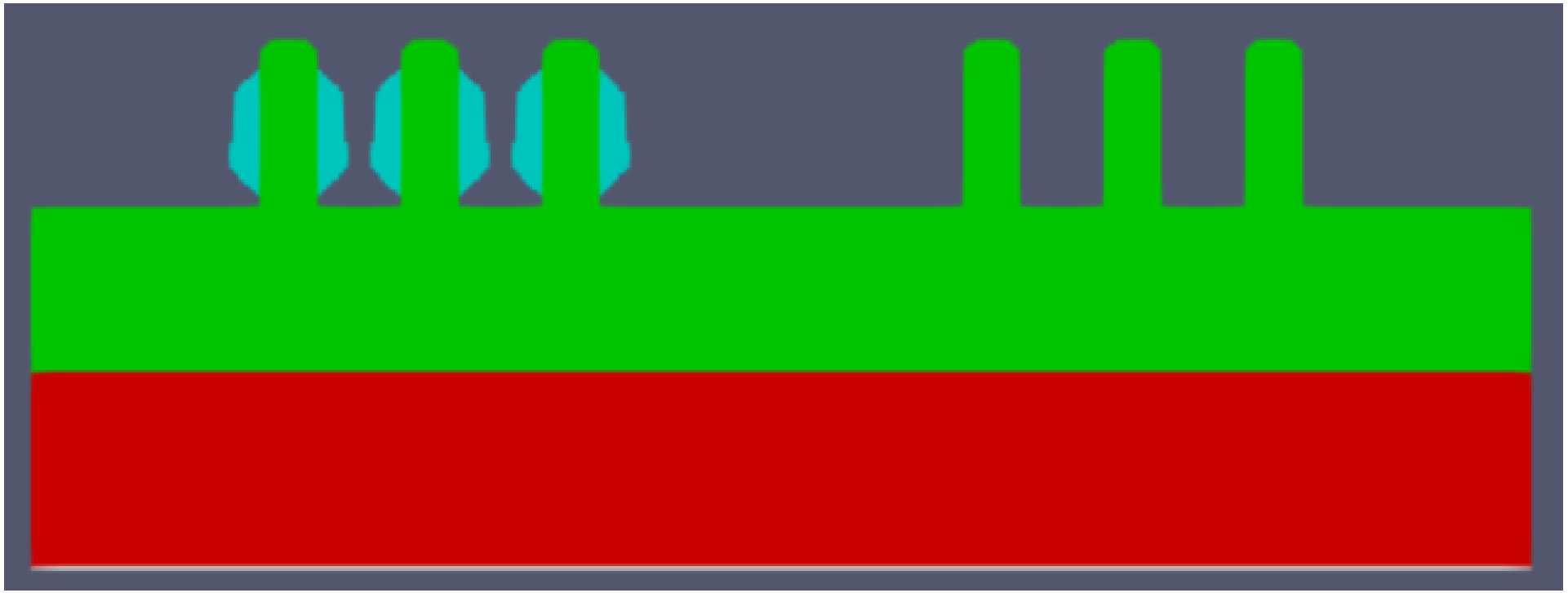
- First, prepare a mask for PMOS part
  - Then, etch the NMOS fins. Set the etch depth as 10 nm.



(Dummy gates, hard masks, spacers, and photoresists are not shown.)

NMOS S/D

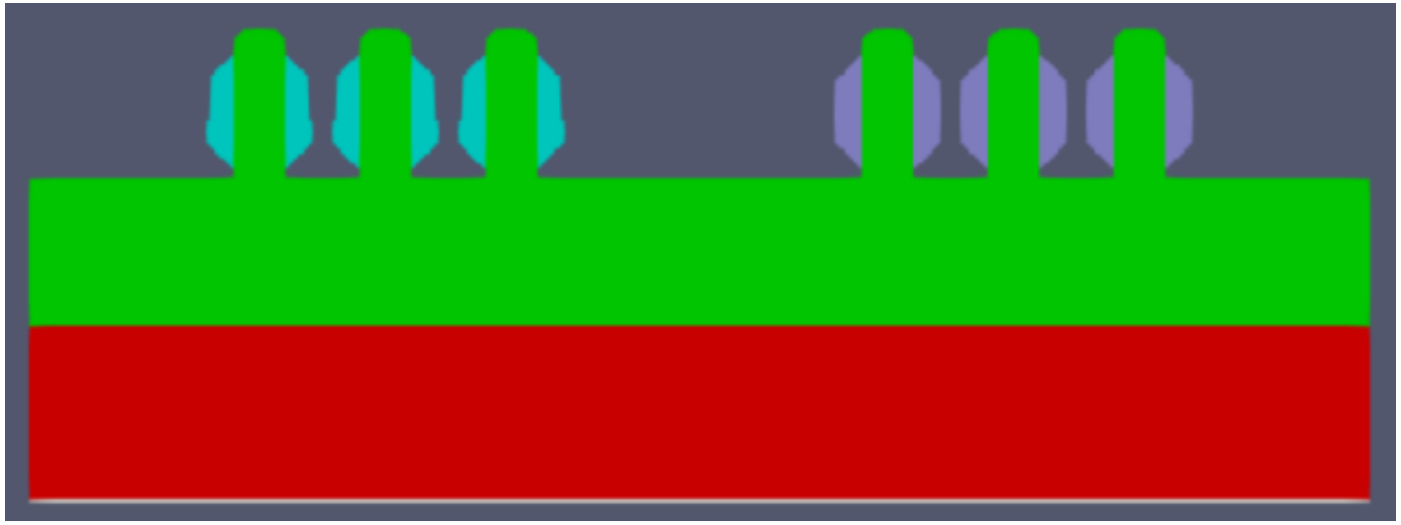
- Then, grow the epitaxial layer.
  - Keep the minimum distance between two fins. (In this example, 4 nm)

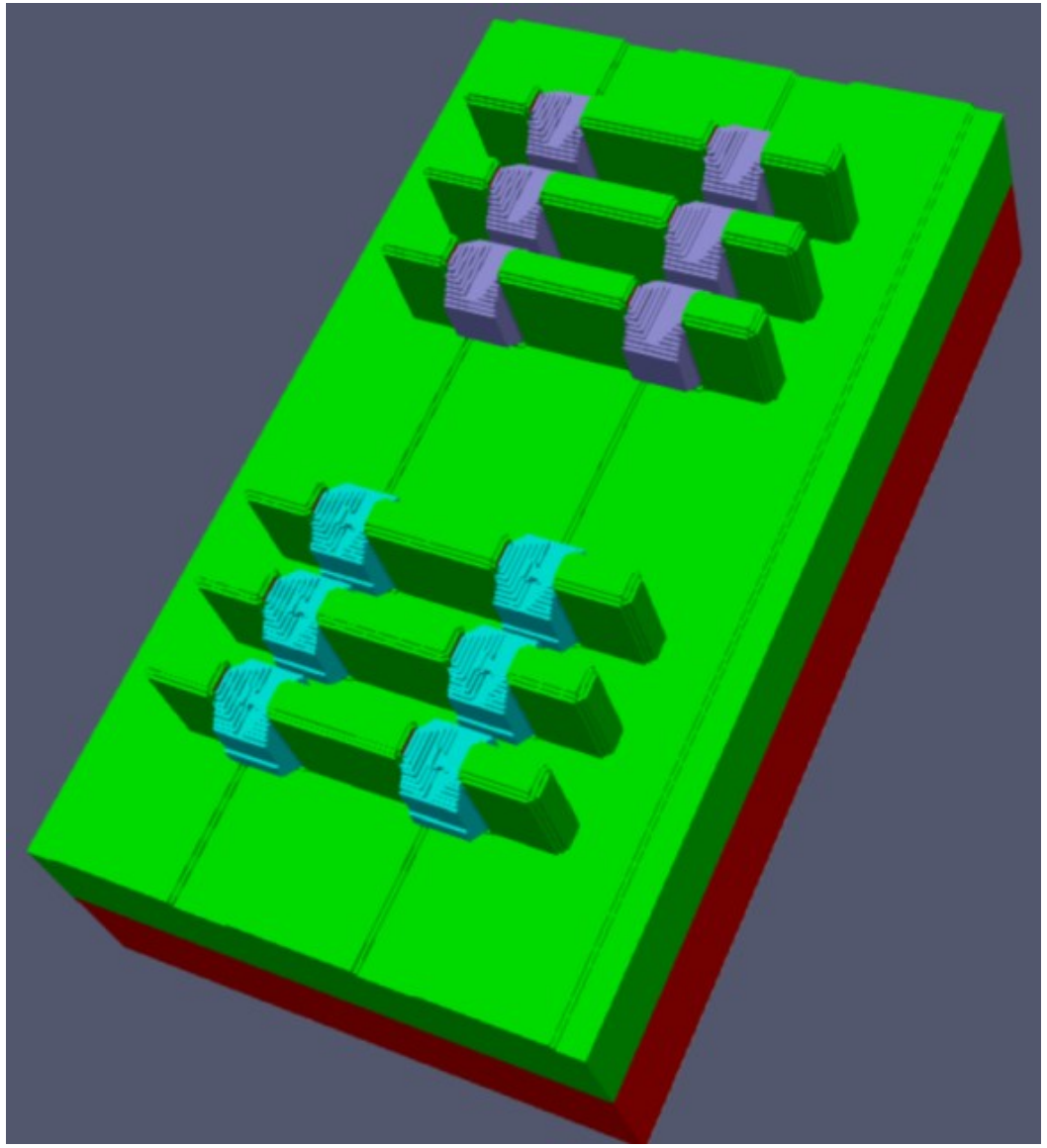


PMOS S/D

- A deeper cavity etch of 20 nm
  - Then, grow the SiGe epitaxial layer.
  - (Exact shapes may be different.)

NMOS PMOS

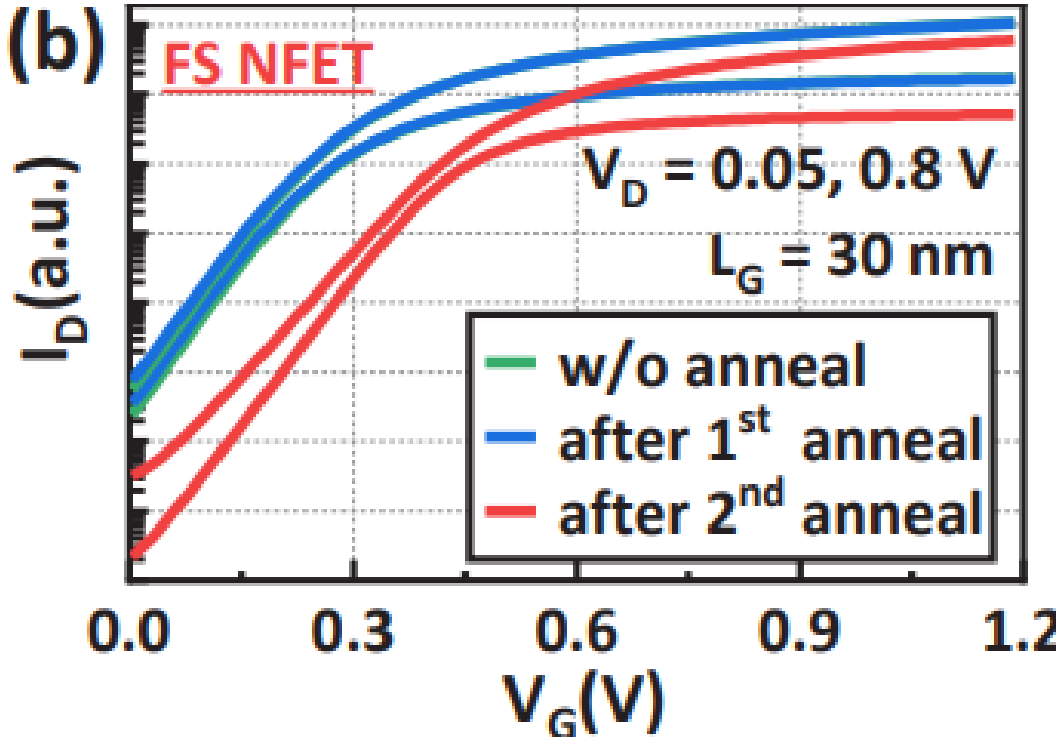




Thermal process

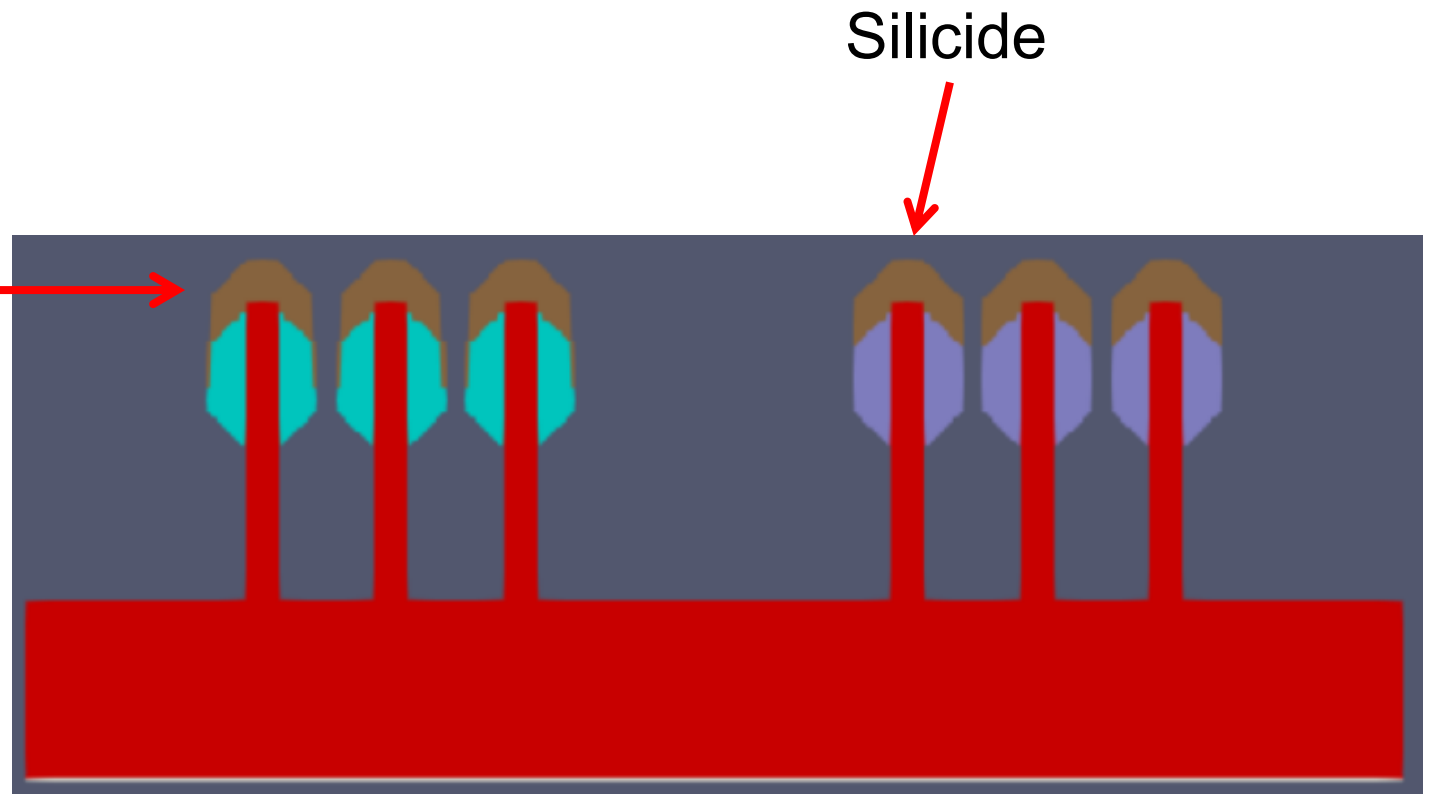
- Dopants must be activated.
  - Rapid thermal anneal (RTA)
  - High temperature, typically 950 ℃ ~ 1050 ℃
  - It must be performed before high-k/metal gate stack.

When 700 ℃ heat process is applied (the 2nd anneal), the device characteristics are heavily affected. (H. Wu et al., Peking University)



Salicide (self-aligned silicide)

- 10-nm-thick Ni deposition (anisotropic)
  - Then, anneal ➔ Silicide

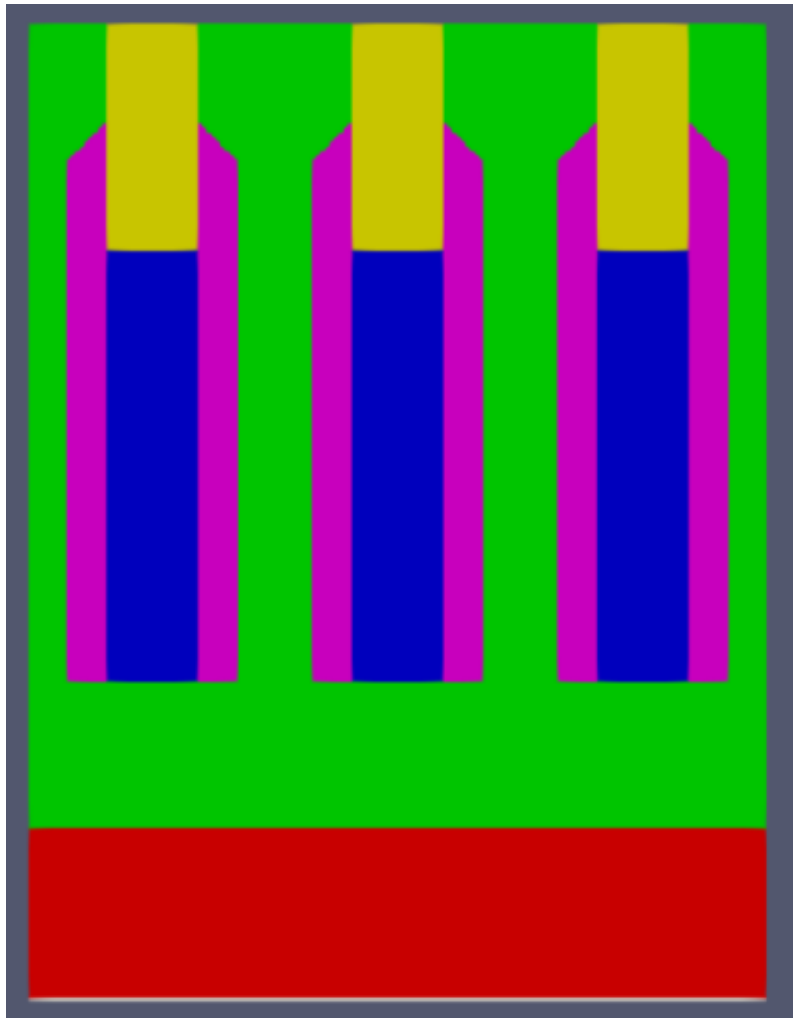


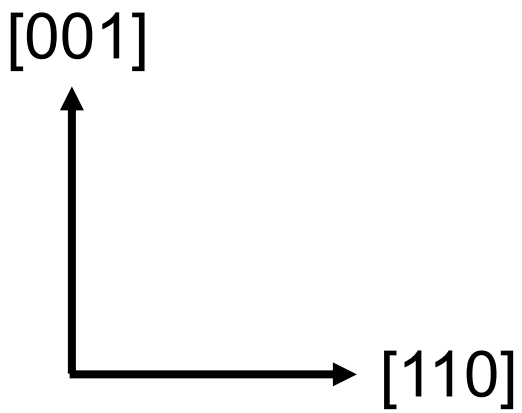

```
model (name="model_salicide") {
    select (region="Si:P")
    select (region="SiGe")
    select (region="Salicide")
}

depo (aniso,region="Salicide",model="model_salicide",thickness=10)
```

ILD0, inter-layer dielectric 0

- SiO_2 layer
  - CMP down to the hard mask (Slightly over-etch)

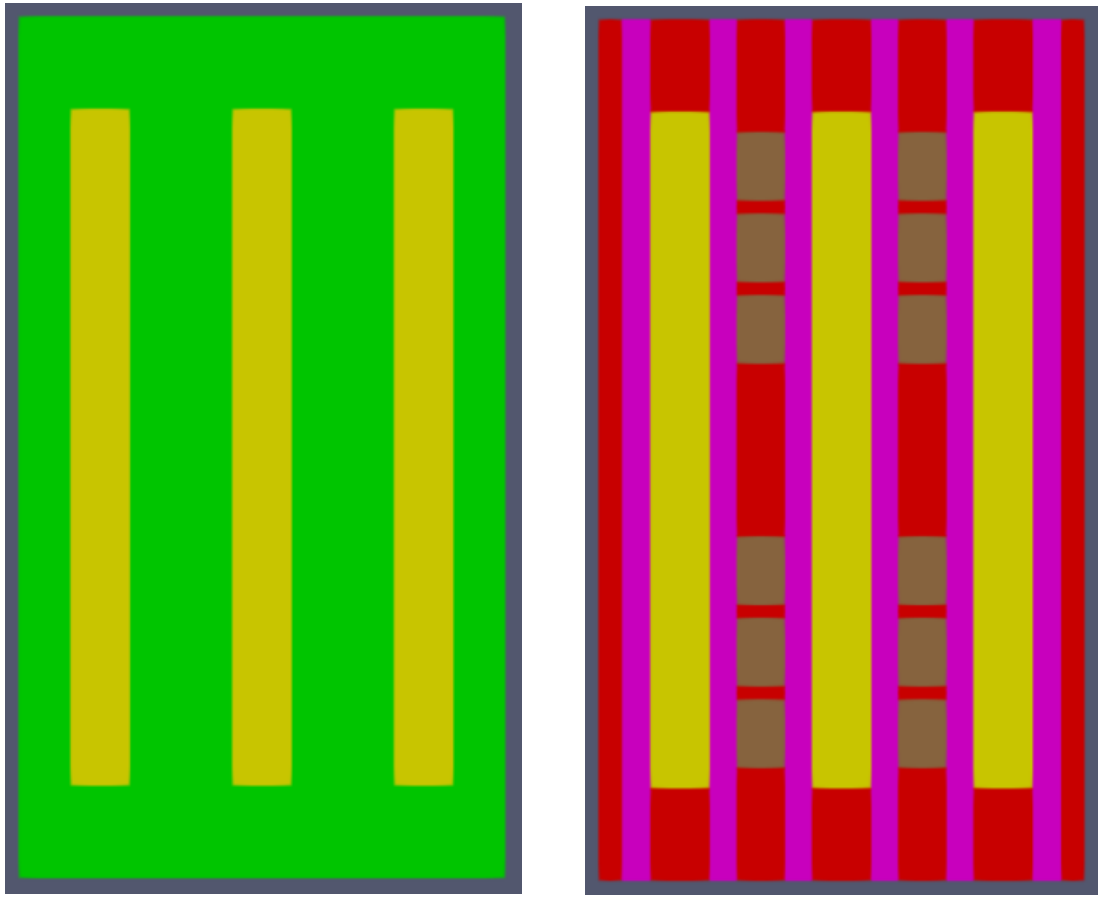
```
cmp (position=215)
```





Gate cut

- Dummy gates are running over several logic gates.
  - For the “gate cut” region, etch the hard mask and dummy gate.
  - Fill the cavity with SiO_2.
  - CMP, again

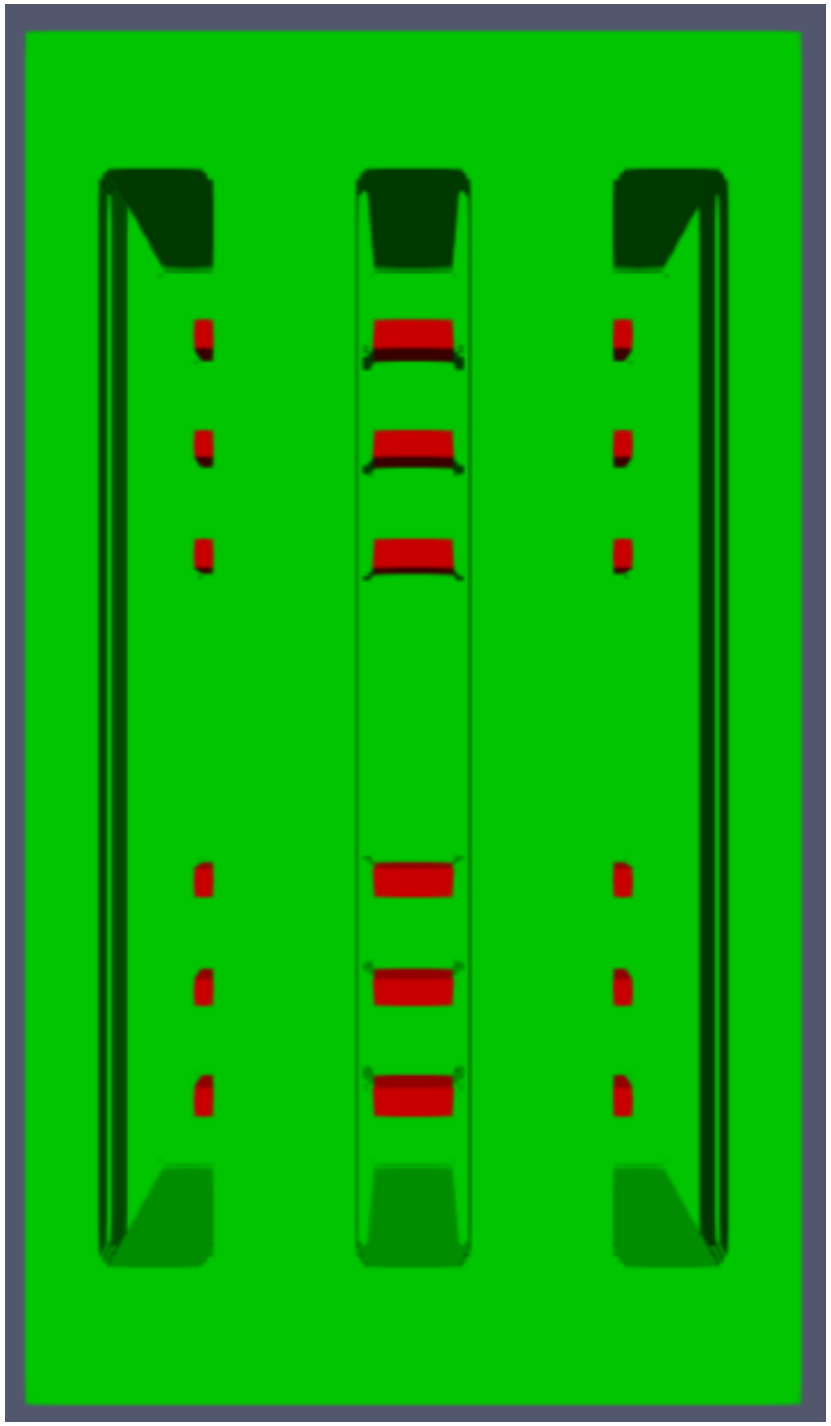


Top view (With/without SiO_2)

```
mask (name="mask_gatecut") {
    rectangle (x0=0,y0=31,x1=162,y1=257)
}
```

Dummy gate removal

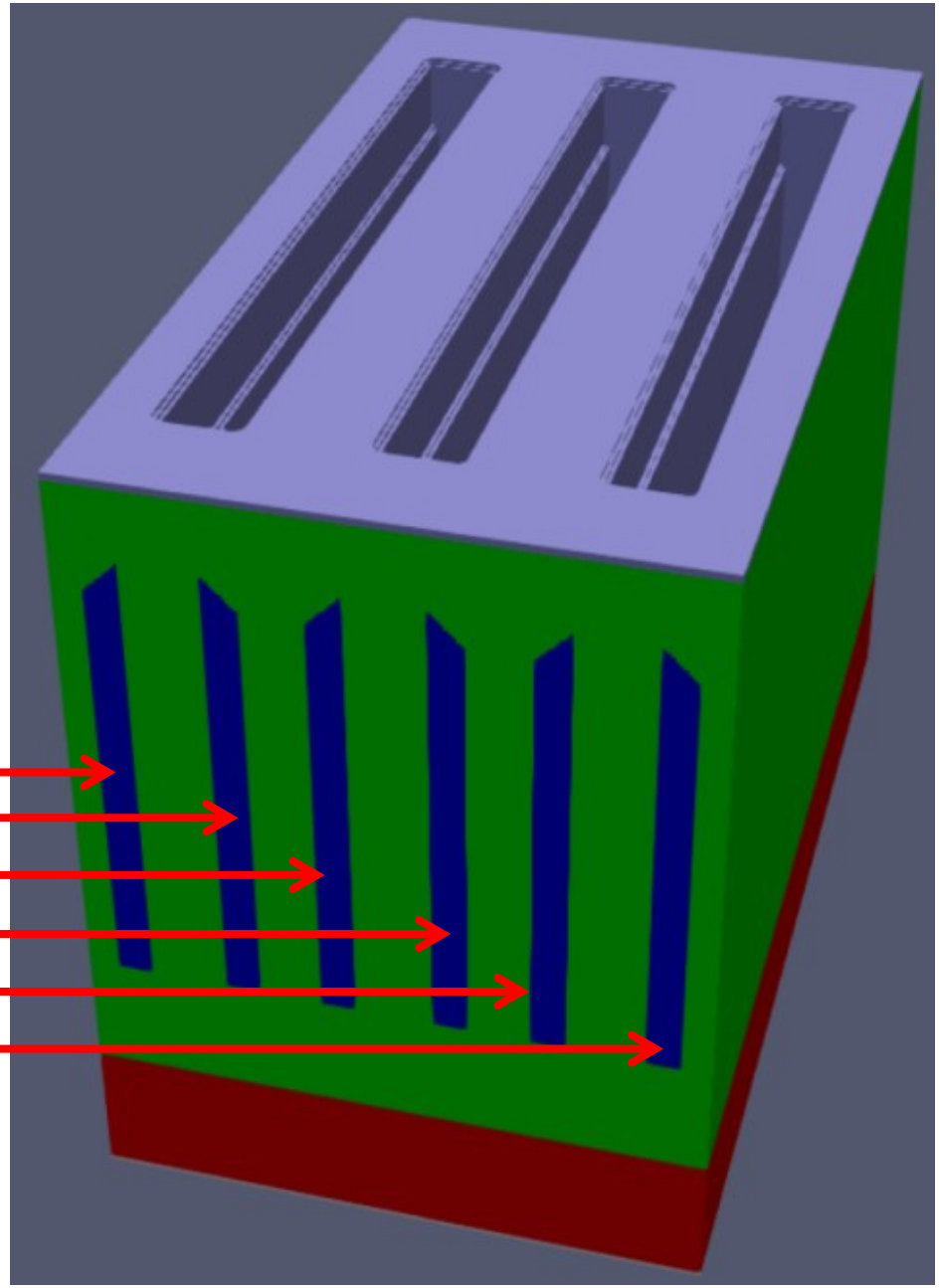
- Now, hard mask and dummy gate are removed.
  - Dummy dielectric is also etched.



High-k stack

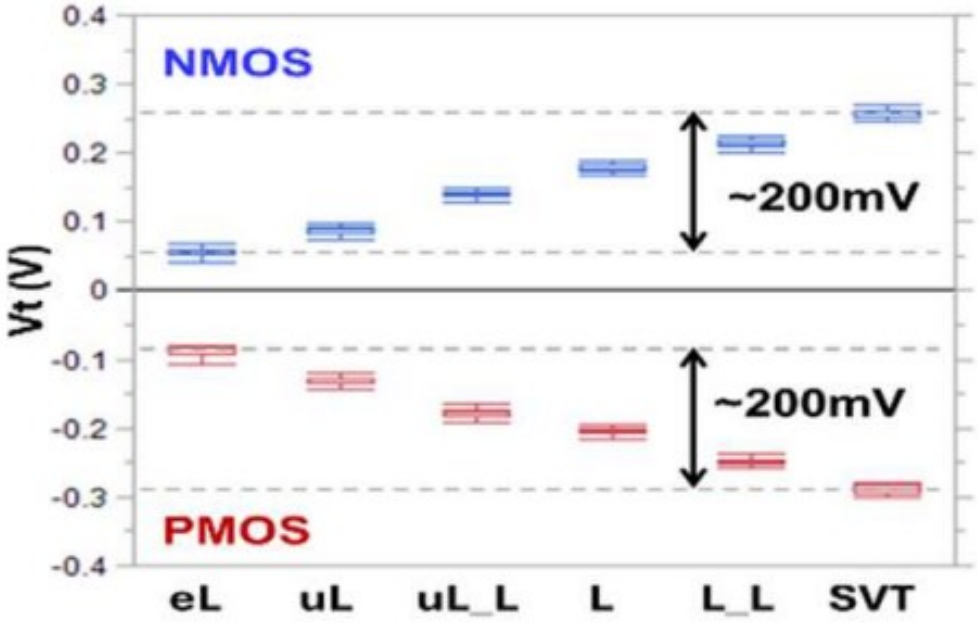
- First, 1-nm-thick interfacial layer (Resolution limit)
  - Only on silicon
  - Then, 2-nm-thick high-k (HfO_2) layer

Spacers (Color changed)



Gate workfunction

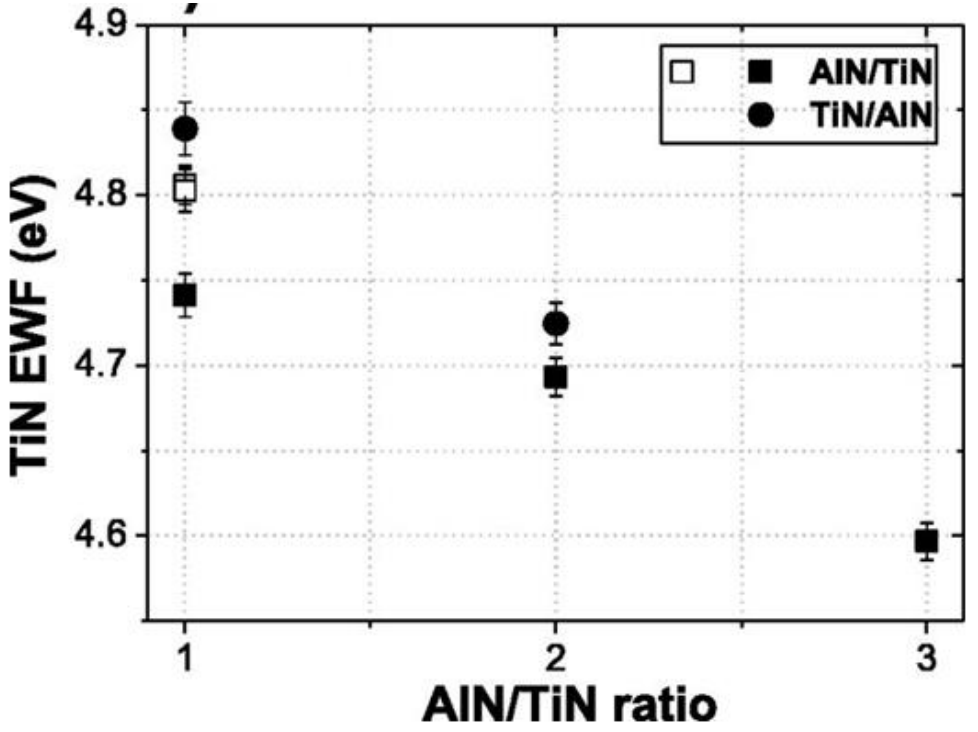
- We need multiple threshold voltages (V_ts).
  - Workfunction metal (WFM) was used.
  - In these days, dipole-based multi-V_t integration with both n-type and p-type dipoles



Six threshold voltage available in the N2 technology (TSMC)

TiAlN

- Workfunction of TiN on HfO_2 is 4.8 ~ 5.0 eV.
  - With Al, its workfunction on HfO_2 is reduced. (Suitable for NMOSFETs)



Workfunction versus AlN/TiN ratio for TiN/AlN liminate devices (L. P. B. Lima et al., IMEC)

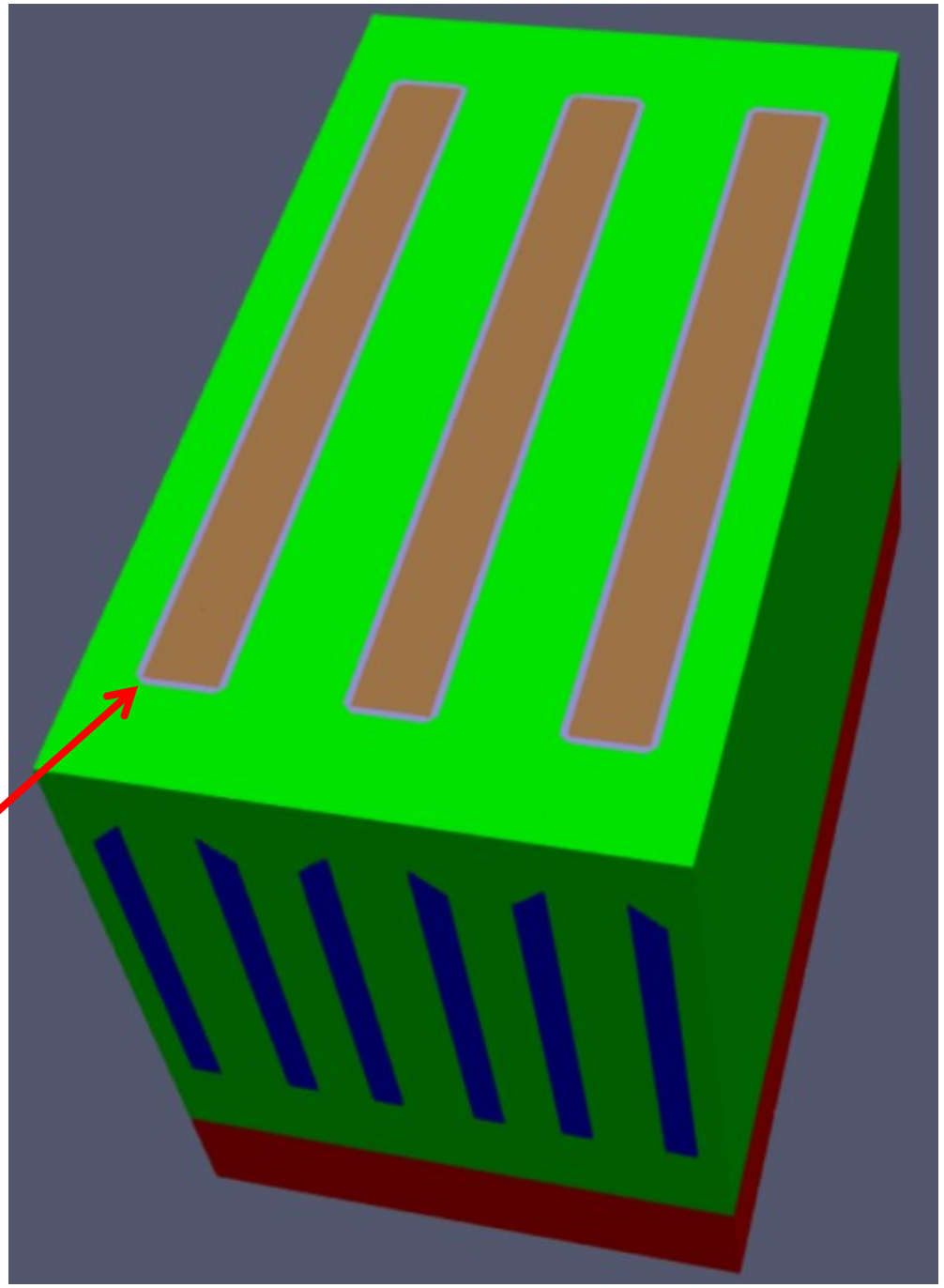
  - (Not considered in this example)

Tungsten fill

- Now, fill the remaining cavity with tungsten.
  - CMP, again

```
cmp (position=213)
```

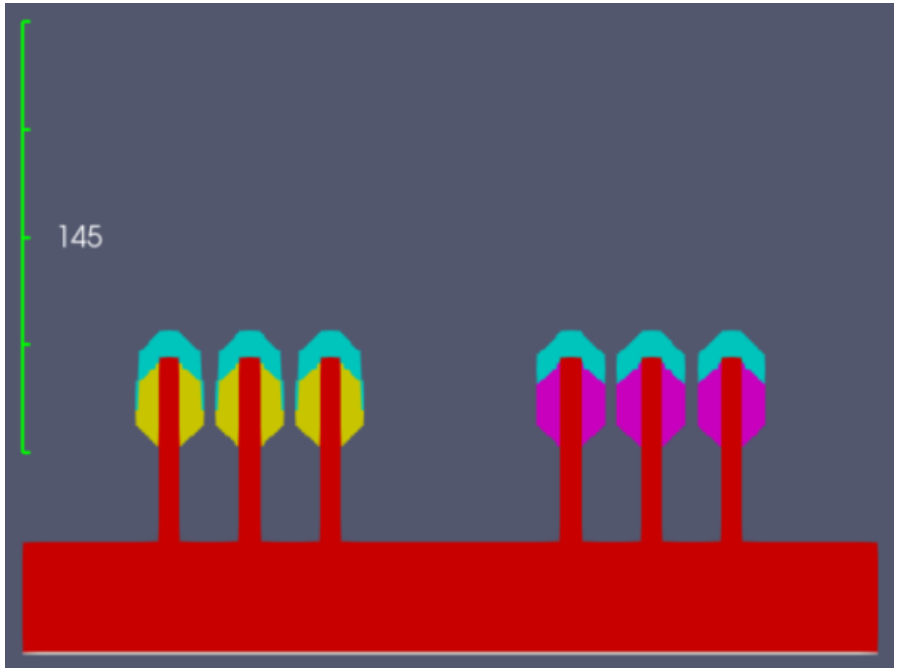
  - In this example, the ILD0 thickness is about 145 nm.

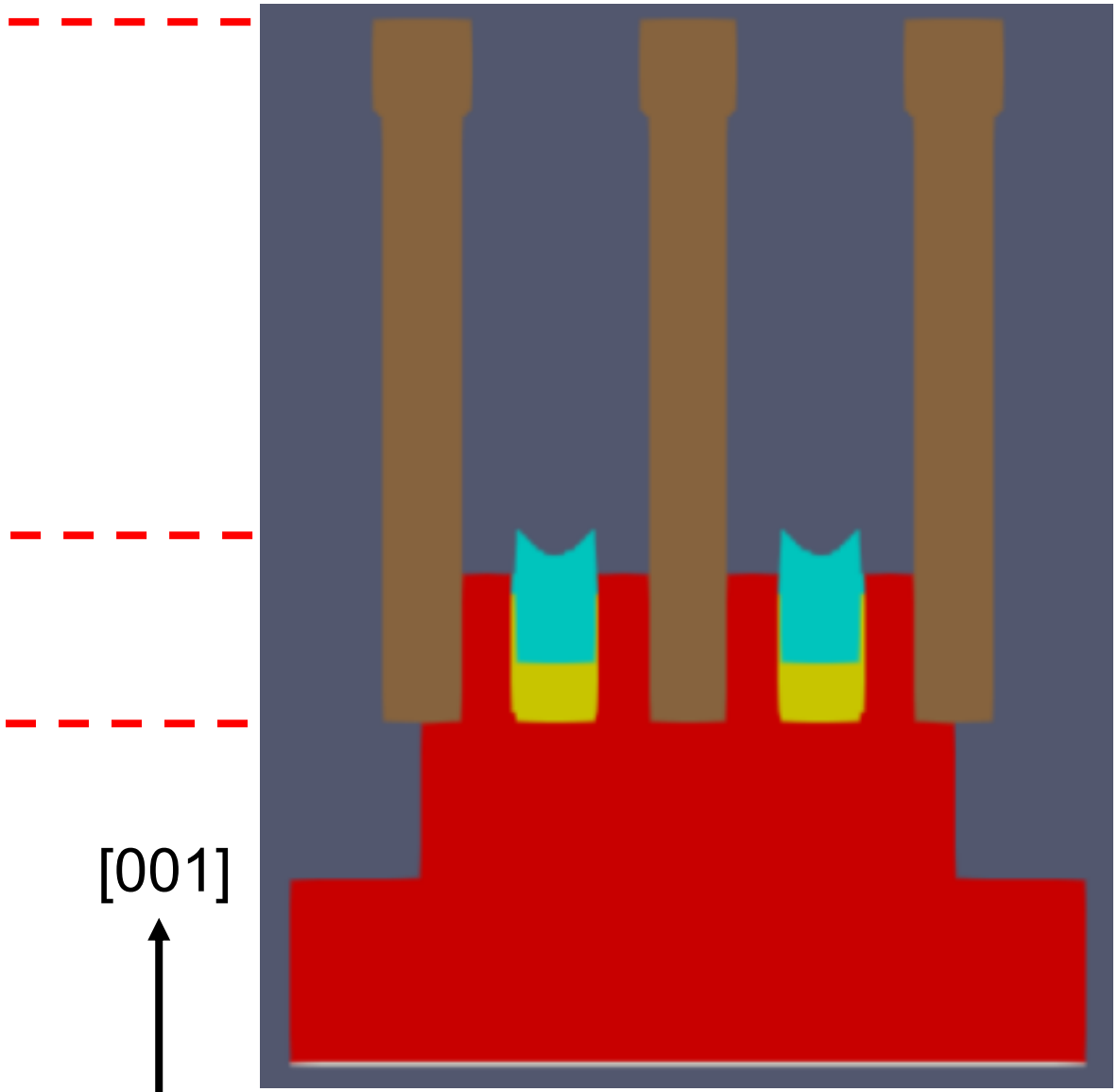


In reality, there are more layers between HfO_2 and tungsten to adjust V_t.

Side view

- Some comments
  - In order to prevent the merged S/D epi layers, they are not grown sufficiently.
  - Fins seem to be a little short.





FEOL (Front-End-of-Line)

- All process steps up to the completion of the transistor itself
  - Fin patterning (L9. Fins are already cut.) ➔ STI (L9) ➔ Dummy gate (L9) ➔ Spacer (L10) ➔ S/D epi (L13) ➔ Salicide (L14) ➔ Dummy gate removal (L14) ➔ High-k (L14) ➔ Gate fill (L14)
  - What's the next? MOL

Homework#14

- Due: 08:00 on Nov. 5
- Submit a report through the GIST LMS system.
  - Throughout several lectures (from L6 to L15), we have covered the FEOL processed of a virtual ASAP7 FinFET. Follow the lecture progress.

Thank you!