Special Topics on Basic EECS I Design Technology Co-Optimization

Lecture 2

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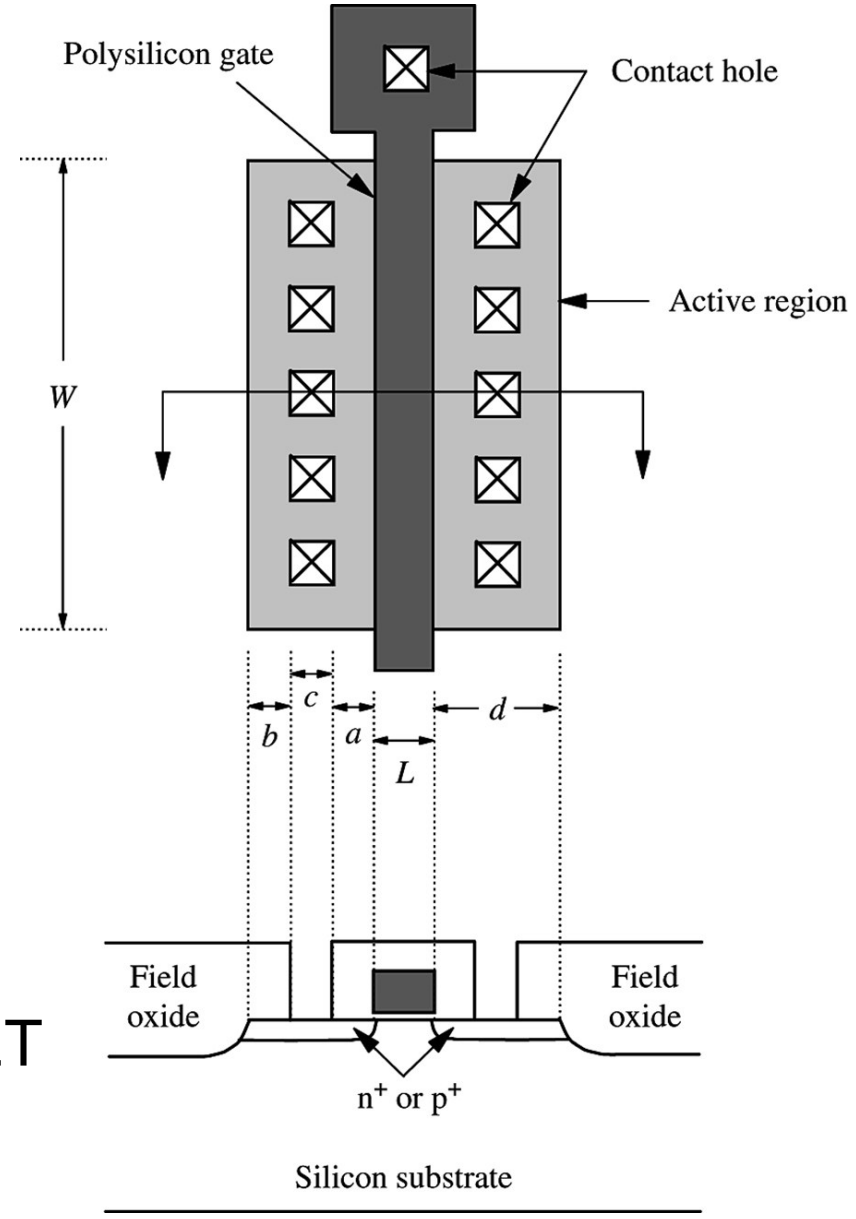
L2

Traditional MOSFET scaling

- Ground rules
  - Length: L
  - Width: W
  - Width of n^+ or p^+ diffusion: d
- Scaled by the same factor, κ (> 1)
  - Its typical value is $\kappa \approx 1.4$. $(\kappa^2 \approx 2)$
  - Area: $\times \frac{1}{\kappa^2}$
  - Oxide capacitance (per area): $\times \kappa$



Layout and cross-section of a MOSFET (Prof. Taur's book)

Constant-field scaling

- Discussion
  - Gate capacitance follows $C_{ox}WL$, $\times \frac{1}{\kappa}$.
  - Recall that the saturation current follows $\mu C_{ox} \frac{W}{L} (V_{DD} - V_t)^2$.
  - When V_{DD} becomes $\times \frac{1}{\kappa}$, the saturation current also becomes $\times \frac{1}{\kappa}$. ($\times$ 0.7 low current)
  - Charge stored (gate capacitance $\times V_{DD}$) scales $\times \frac{1}{\kappa^2}$.
  - The delay (~performance) becomes $\times \frac{1}{\kappa}$.
  - At an increased frequency ($\times \kappa$), power becomes $\times \frac{1}{\kappa^2}$.

Ideal case with $\kappa = 1.4$

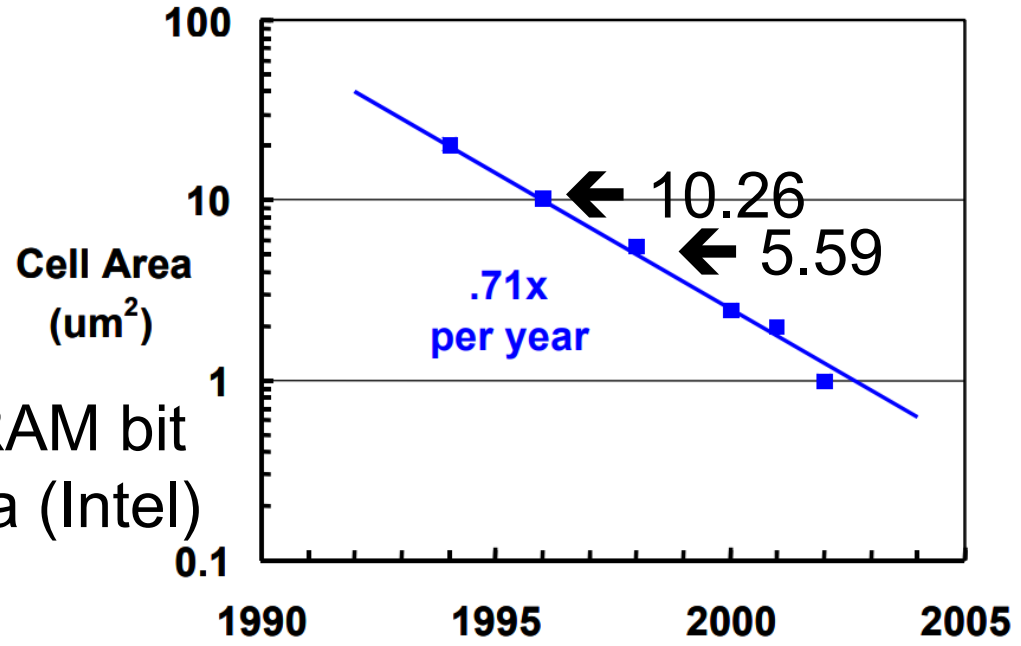
- Generation-to-generation improvement

  0.5X Area & +40% Speed & -50% Energy

  – From today's view, improvement seems to be tremendous.

  – Let's see an example, 0.25 μm (Intel Pentium II and III, 1997)
  ➔ 0.18 μm (Intel Pentium 4, 1999)

Intel SRAM bit cell area (Intel)



Intel 0.25 µm @ IEDM 1996

- Fact sheet
  - V_{DD} = 1.8 V. Actual channel length is 0.18 µm. Oxide thickness is 4.5 nm. Saturation currents are 0.70 mA/µm (N-ch) and 0.32 mA/µm (P-ch). Subthreshold slope is less than 85 mV/dec. N-ch/P-ch threshold voltage are 0.28/-0.27 V. DIBL values are 65/63 mV/V.
  - Transistor's $\frac{CV}{I}$:

~3.5 psec (N-ch)

~7 psec (P-ch)

Then, inverter delay?

- SRAM: 10.26 µm^2

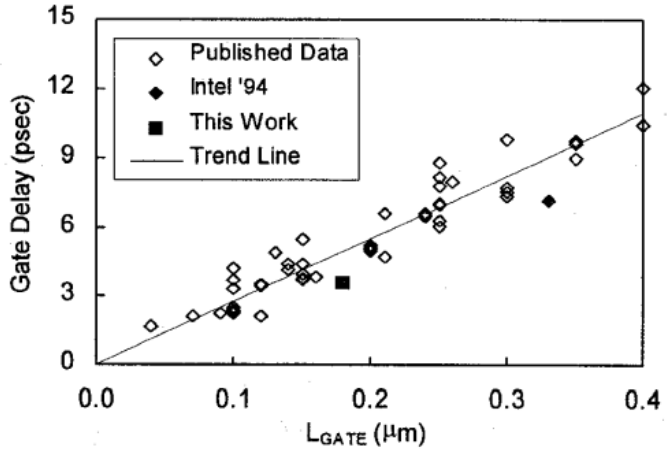


Fig. 9 N-ch CV/I gate delay vs. gate length trend

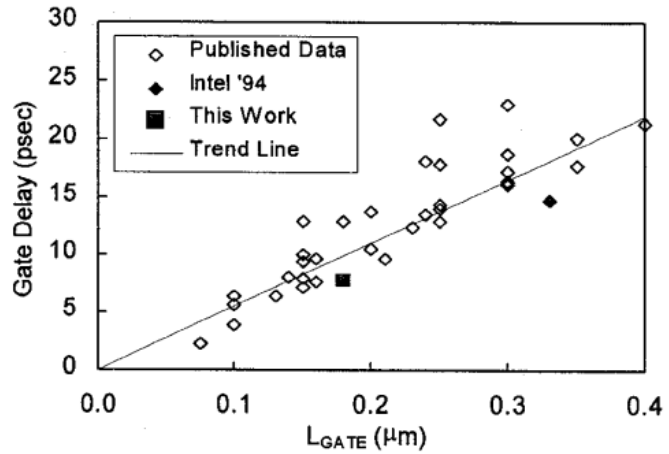


Fig. 10 P-ch CV/I gate delay vs. gate length trend

Intel 0.18 μm @ IEDM 1998

- Fact sheet (Red ones for 0.18 μm)
  - V_{DD} = 1.3 – 1.5 V (1.8 V). Actual channel length is 0.13 μm (N-ch)/0.15 μm (P-ch) (0.18 μm). Oxide thickness is 3.0 nm (4.5 nm). Saturation currents at 1.5 V are 0.94 mA/μm (0.70 mA/μm) (N-ch) and 0.42 mA/μm (0.32 mA/μm) (P-ch). Subthreshold slope is less than 90 mV/dec (85 mV/dec). N-ch/P-ch threshold voltage are 0.30/-0.24 V (0.28/-0.27 V).
  - DIBL?
  - Inverter delay (fan out = 1):

    <11 psec at 1.5 V
  - SRAM: 5.59 μm^2 (10.26 μm^2)

Inverter gate delay (Intel)

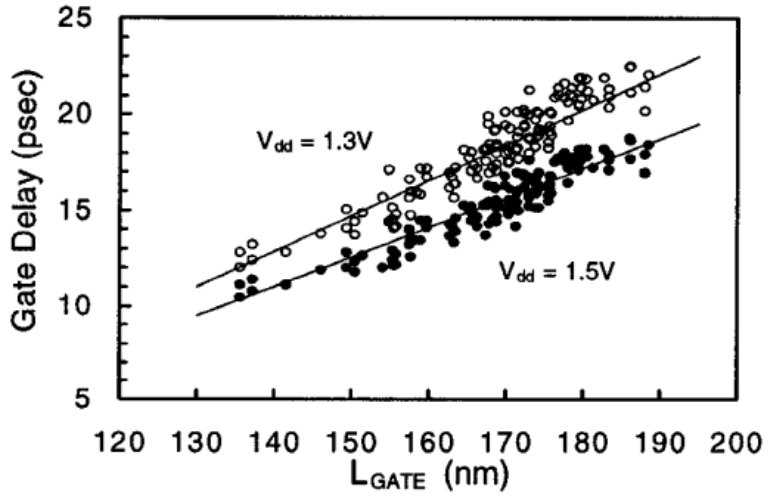
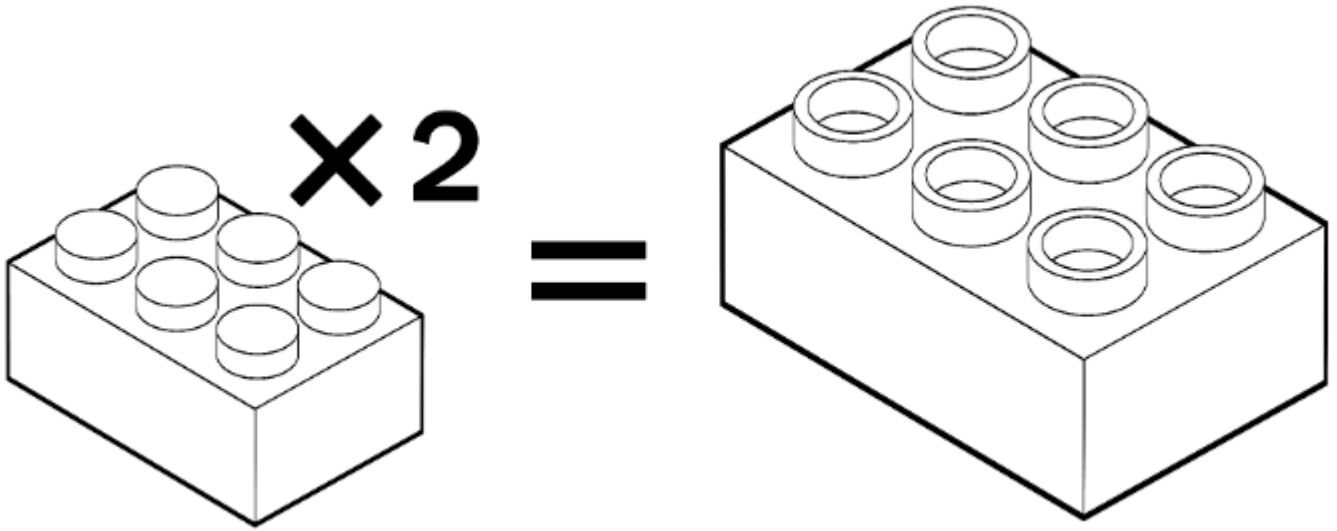


Fig. 10 Inverter gate delay per stage vs. L_{GATE}, FO=1

When you read those papers,

- You can find that:
  - The authors mainly discuss the single device performance.



Lego brick and Duplo brick (Lego)

Chronicles

- Intel and TSMC. IEDM and VLSI papers
  - 130nm: 2000 (Intel, IEDM)
  - 90nm: 2003 (Intel, IEDM)
  - 65nm: 2004 (Intel, IEDM)
  - 45nm: 2007 (Intel, IEDM)
  - 32nm: 2008 (Intel, IEDM)
  - 22nm: 2012 (Intel, VLSI)
  - 16nm: 2013 (TSMC, IEDM), 14nm: 2014 (Intel, IEDM)
  - 10nm: 2016 (TSMC, IEDM)
  - 7nm: 2016 (TSMC, IEDM)
  - 5nm: 2019 (TSMC, IEDM)
  - 3nm: 2022 (TSMC, IEDM)
  - 2nm: 2024 (TSMC, IEDM)

For your interest, watch the video, [Eng][VLSIDevices2025] L23, from 33:53.

Homework#2

- Due: 08:00 on Sep. 9
- Submit your report through GIST LMS system.
- 1) Download Intel's IEDM 1998 abstract for 0.18 μm technology.
  - See Fig. 6.
  - Calculate the DIBL for both devices.
- 2) For 0.25 μm devices,
  - Estimate C (of course, per width) for N/PMOSFETs.
  - Compare it with $\epsilon_{ox}\frac{L}{t_{ox}}$.

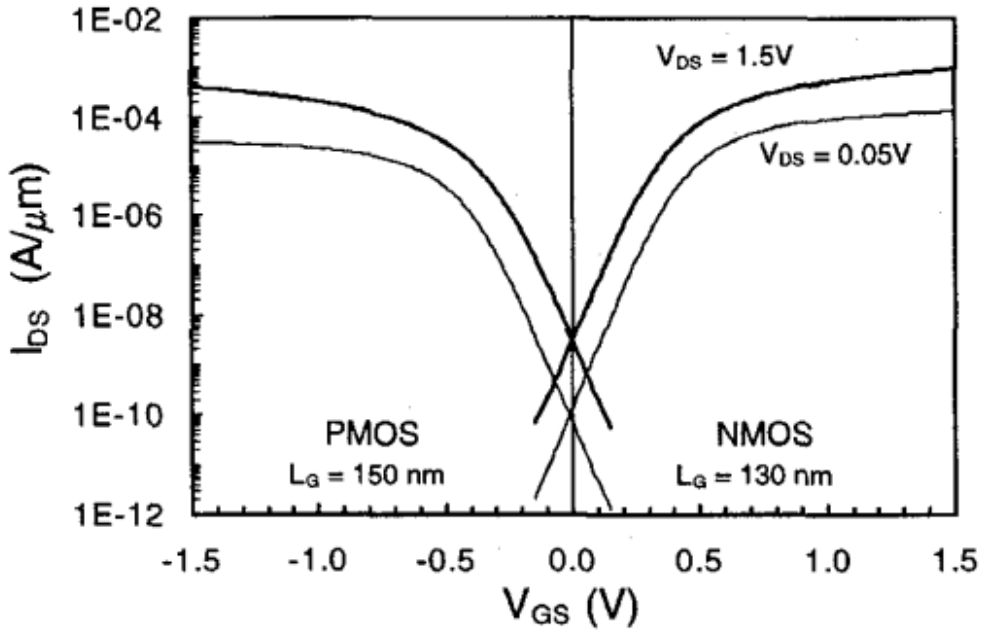


Fig. 6 MOSFET subthreshold curves

Thank you!