Lecture14: CMOS amplifier, common-source

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Electrical Engineering and Coumputer Science
Gwangju Institute of Science and Technology

GIST Lecture on April 25, 2018 (Internal use only)

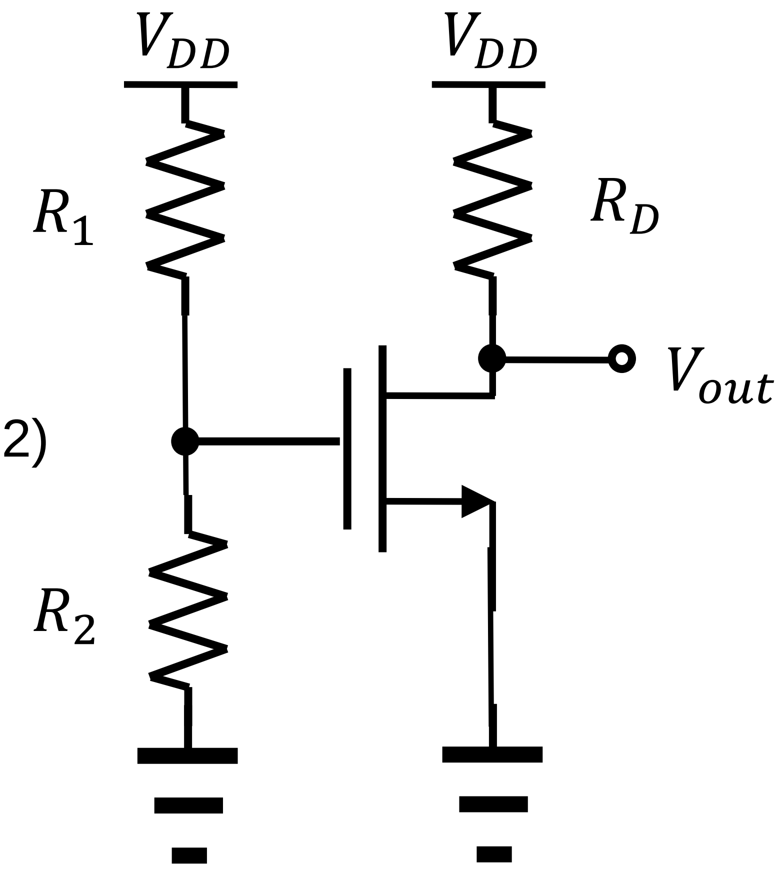
Simple biasing (1/2)

- A better way
  – The gate bias voltage is

$$V_{GS} = \frac{R_2}{R_1+R_2} V_{DD} \qquad (17.10)$$

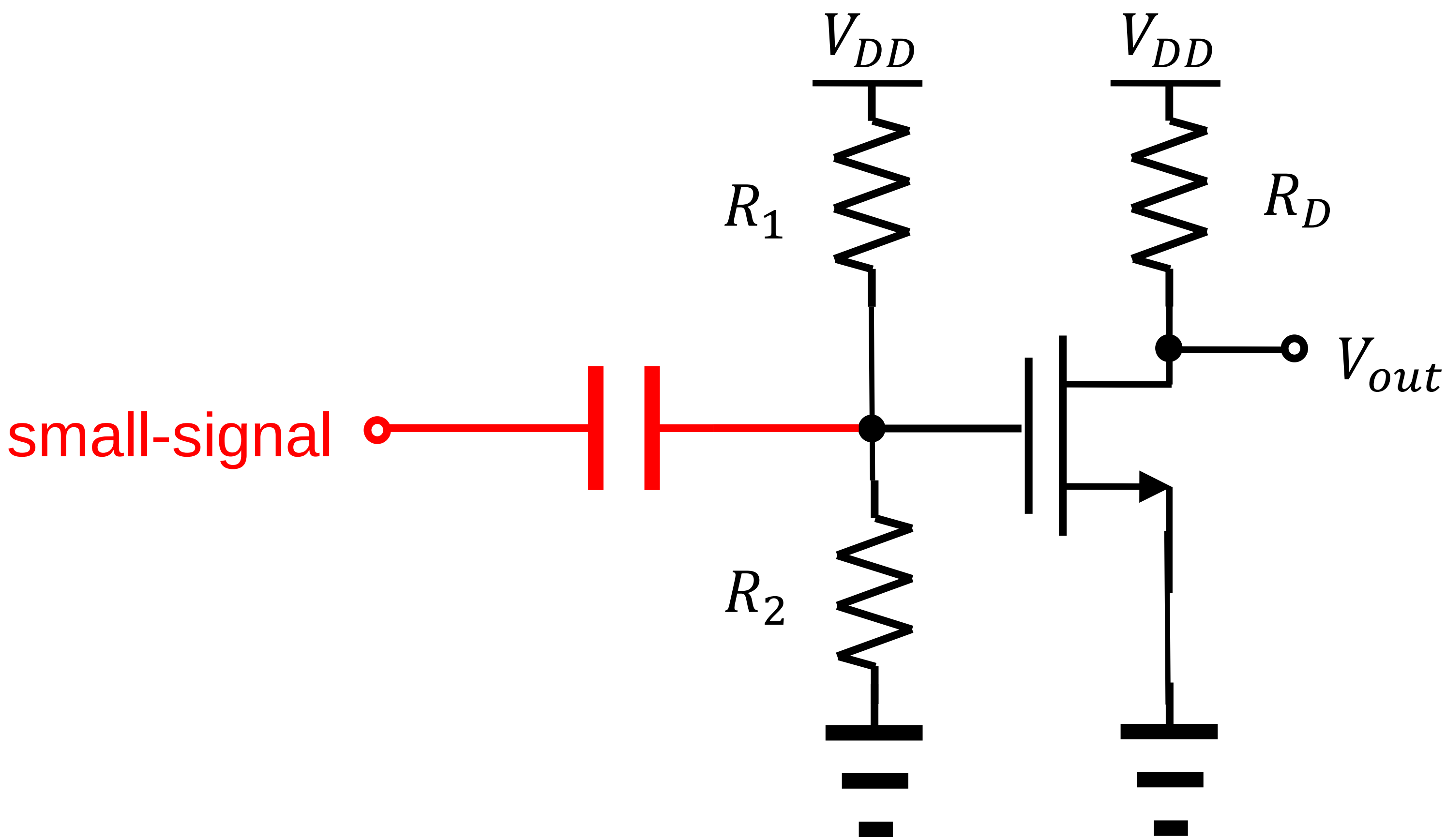
  – The drain current is

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2 \qquad (17.12)$$



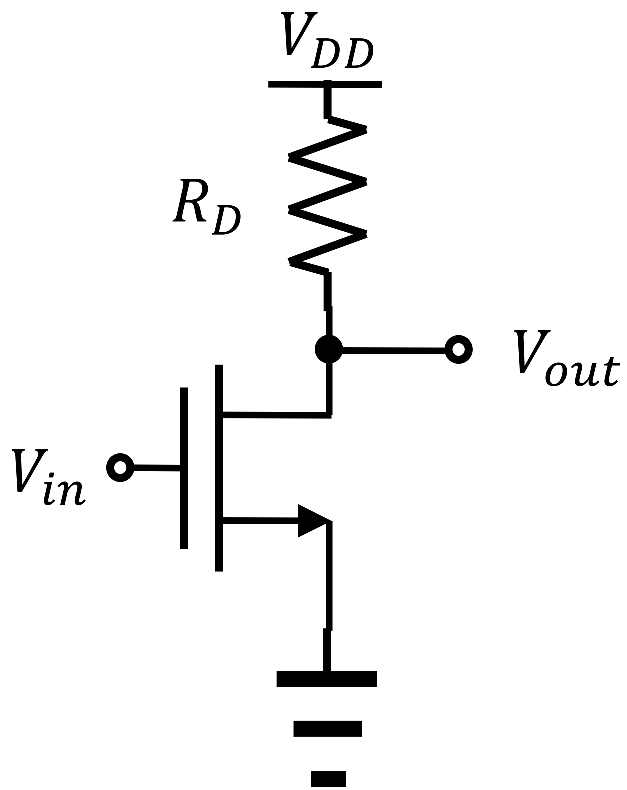
Simple biasing (2/2)

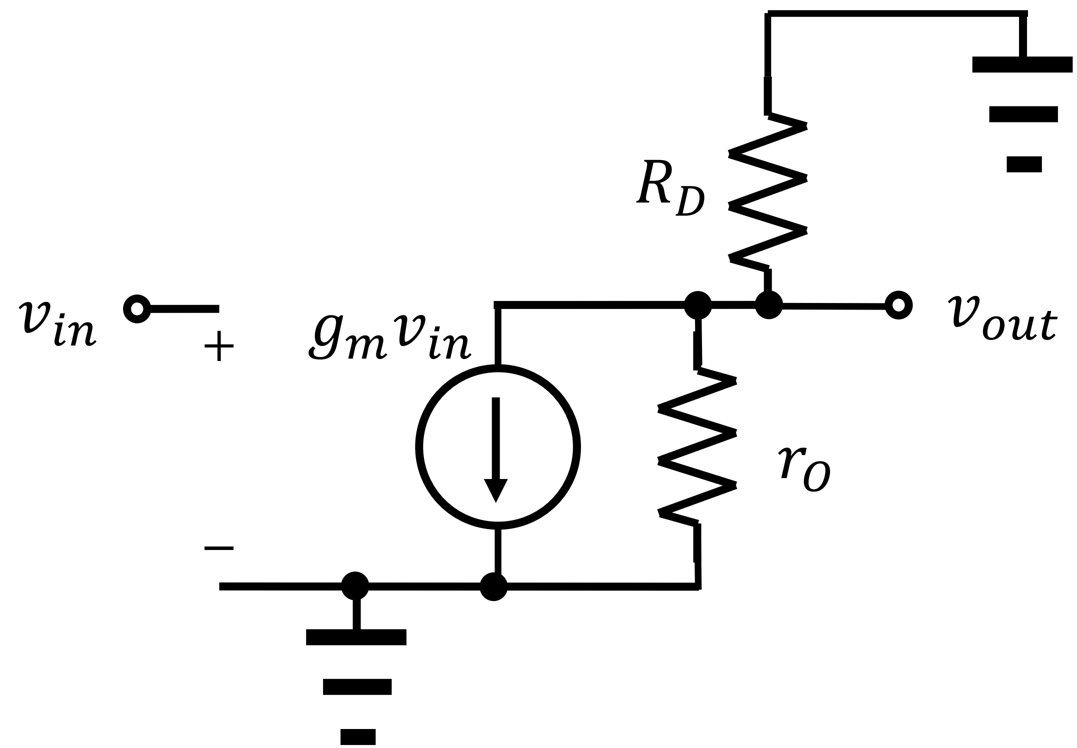
- How to apply the small-signal input
  - Use a capacitor!



Small-signal model

- Let’s draw the small-signal model together!





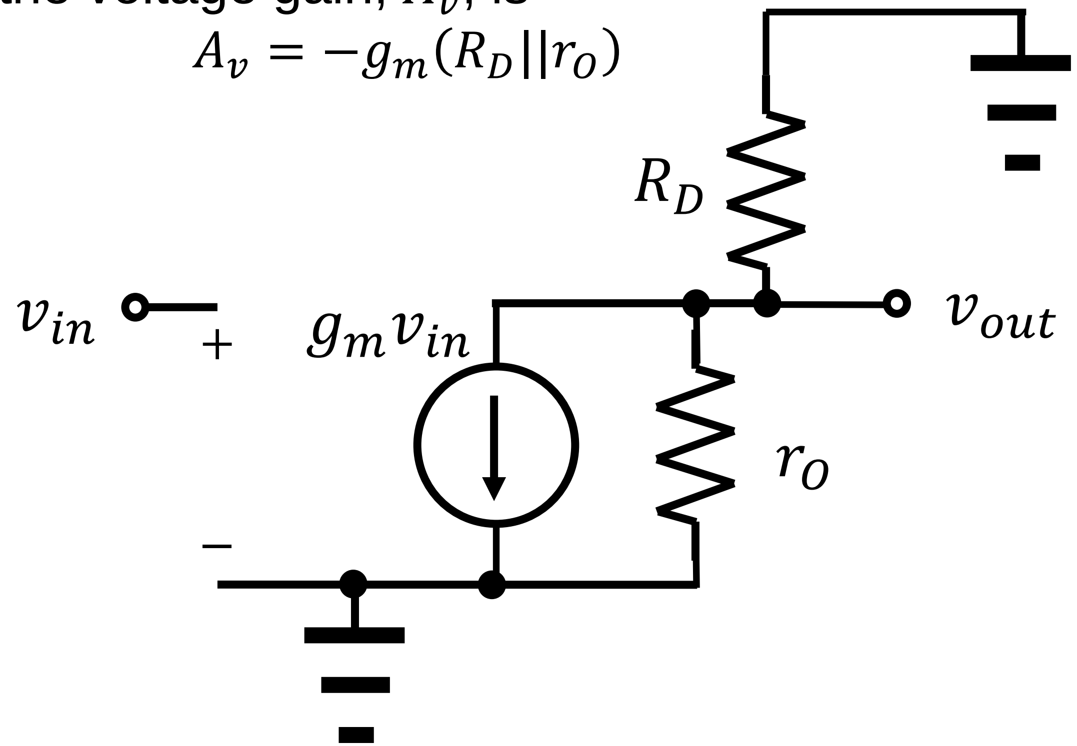
Gain

- Now, calculate the v_{out}.
  - KCL for the v_{out} node gives

$$v_{out} = -g_m(R_D||r_O)v_{in}$$

  - Therefore, the voltage gain, A_v, is

$$A_v = -g_m(R_D||r_O)$$



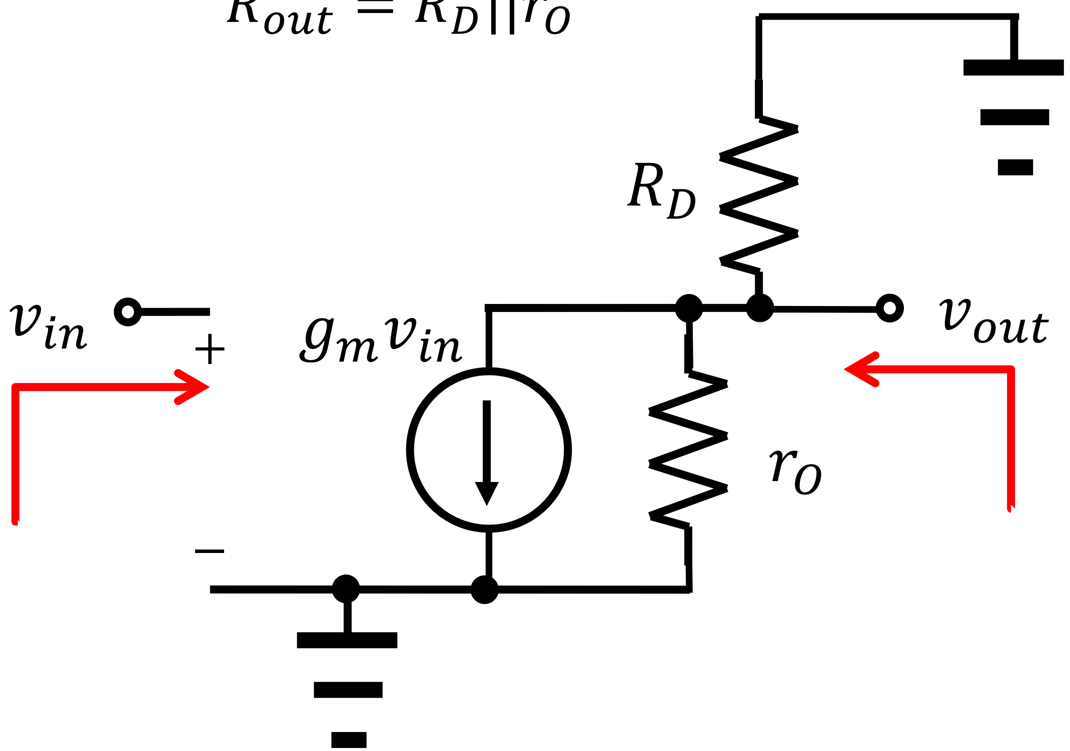
Input/output impedances

- Input impedance

$$R_{in} = \infty$$

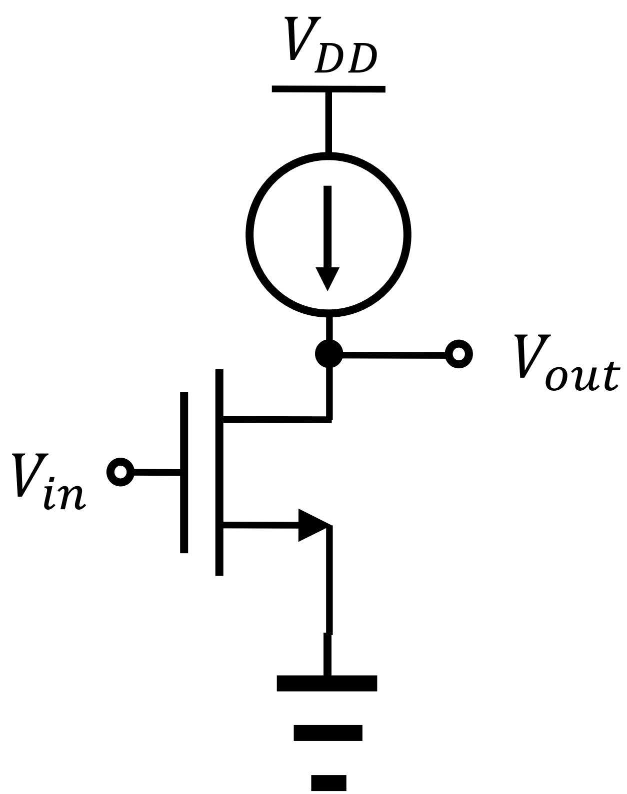
- Output impedance

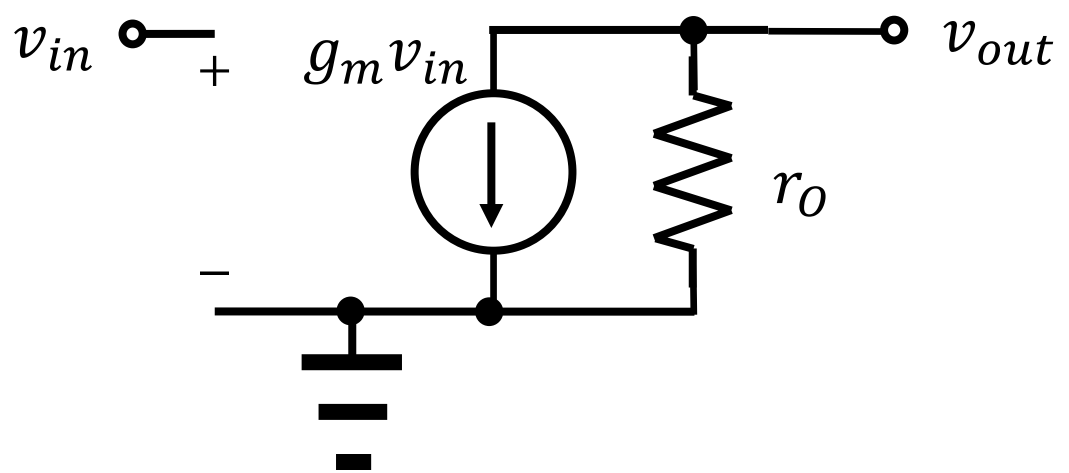
$$R_{out} = R_D || r_O$$



Current-source load

- When $R_D \rightarrow \infty$,
  - The gain can be maximized.





Diode-connected load

- Use a diode-connected load.
  - It is not an ideal current source.

$$v_{out} = -g_{m1}\left(r_{O1}||\frac{1}{g_{m2}}||r_{O2}\right)v_{in}$$

$$A_v = -g_{m1}\left(r_{O1}||\frac{1}{g_{m2}}||r_{O2}\right)$$