HW#6, Electronic Circuit, Spring semester 2020

April 27, 2020

Due: 23:55, May 1 (Friday night)

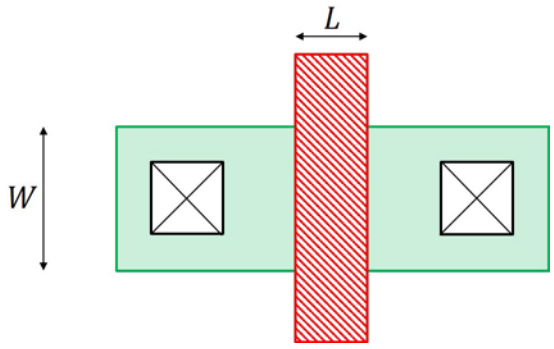
We have 8 problems.

In your answer file, specify both the **SOLUTION PROCEDURE** and the **FINAL SOLUTION**.

1. In the Lecture 10, it was stated that the patterning is done by the photolithography. In this problem, write a report on the photolithography. Clearly identify the references.

2. Visit the TSMC homepage (tsmc.com). You can find the history of the logic technology. A logic technology is specified by its minimum feature size, in our terminology, L. Write the minimum feature size of each technology and its year. (For example, 0.18 micron technology in 1999.)

3. The figure shows a layout of a MOSFET. Consider a larger MOSFET, whose length is $2L$ and width is $3W$. Draw the layouts of the original MOSFET (shown in the figure) and the larger MOSFET.



4. In a PMOSFET, the substrate is doped with N-type dopants. Its source and drain regions are P-type doped. In order to electrically isolate source/drain terminals from the substrate, what is a desirable range of the drain voltage, relative to its substrate voltage?

5. The area of a source region is 1600 nm^2. An abrupt doping profile is introduced in the source region. The dopant density is 2 X 10^{20} cm^{-3}. The depth of the source region is 50 nm. Then, how many n-type dopants are found in the source region?

6. In the lecture material of the Lecture 11, a differential equation of $V(x)$ is presented. Solve the differential equation to have analytic expression for $V(x)$. The derivation procedure should be explicitly shown.

7. The threshold voltage of a NMOSFET is 0.8 V. $\mu_n C_{ox} \frac{W}{L}$ is $4\ \mathrm{mA/V^2}$. Assuming the long-channel MOSFET, calculate the drain current at V_{GS} = 1.8 V and V_{DS} = 0.1 V.

8. The threshold voltage of a NMOSFET is 0.8 V. $\mu_n C_{ox} \frac{W}{L}$ is $4\ \mathrm{mA/V^2}$. Assuming the long-channel MOSFET, calculate the drain current at V_{GS} = 1.8 V and V_{DS} = 1.8 V.