Lecture9: Metal-Oxide-Semiconductor

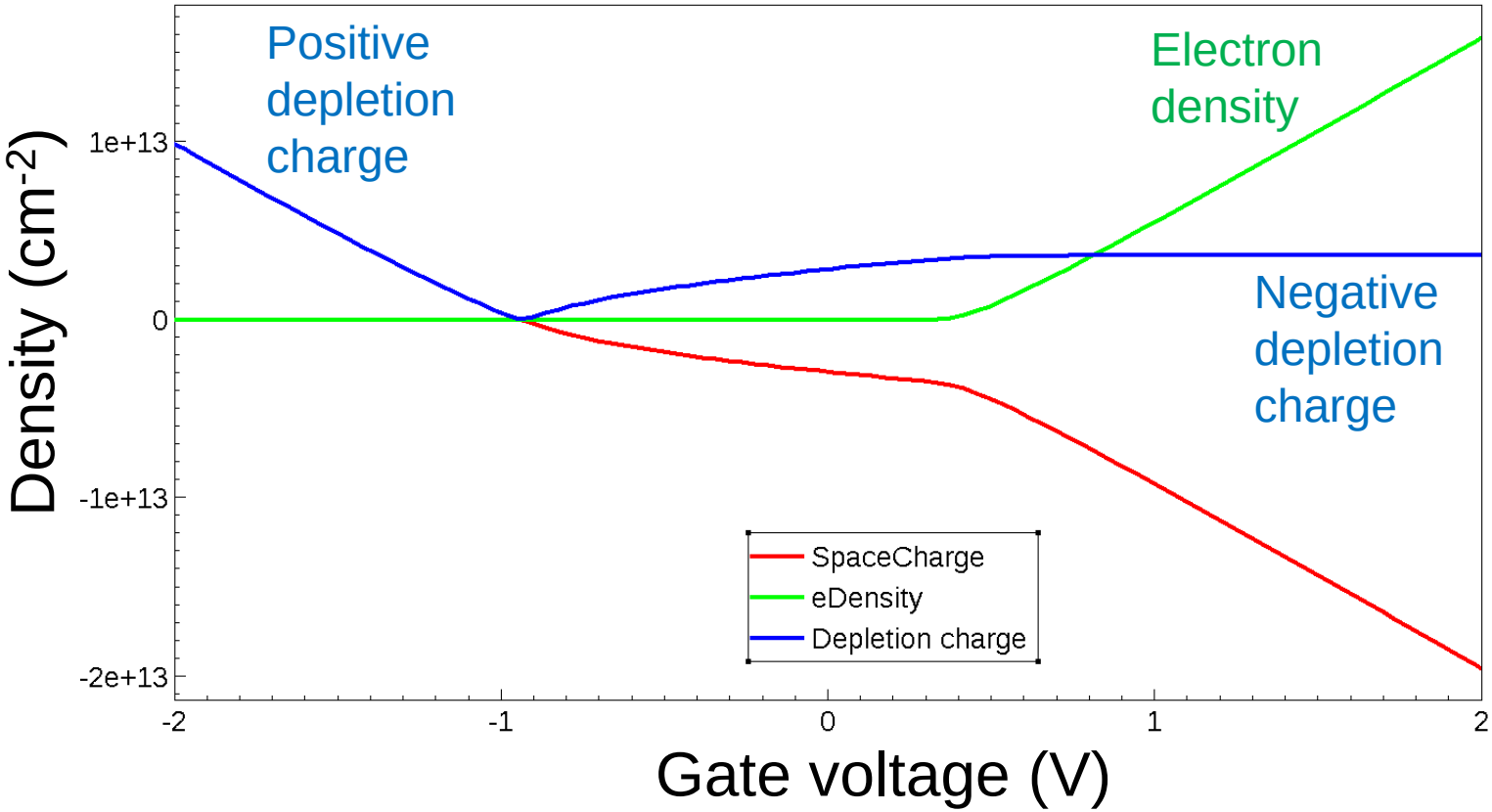
Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

GIST On-Line Lecture on April 13, 2020 (Internal use only)

TCAD simulation result

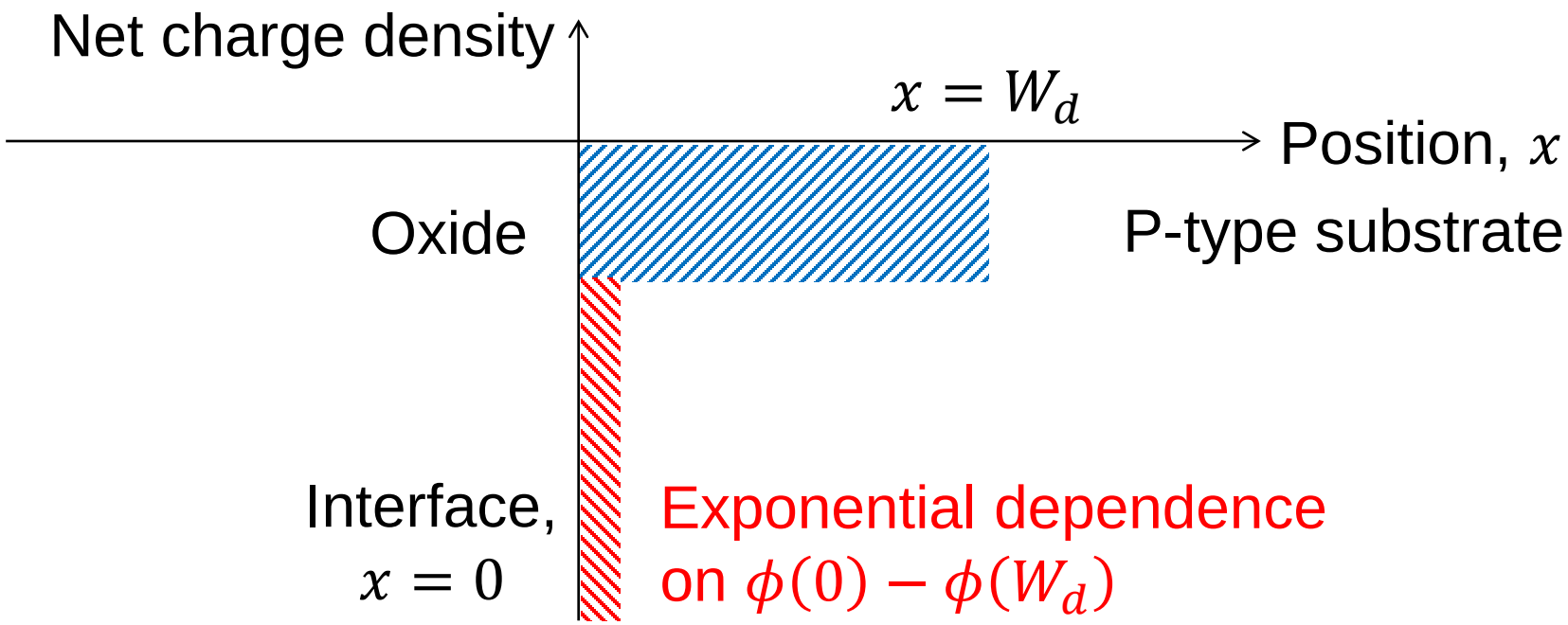
- Integrated densities
  - Oxide thickness of 2 nm
  - P-type substrate doping of $1x10^{18}$ cm^{-3}



Surface potential pinning

- Even when the gate voltage is increased above the threshold voltage, the surface potential is ***almost*** fixed.
  - (It's just like that the diode voltage is ***almost*** fixed to $V_{D,on}$.)

$$n(0) = \frac{n_i^2}{N_A} \exp \frac{\phi(0) - \phi(W_d)}{V_T}$$



Electron charge density

- Usually, we want to know

$$Q_{elec} = (-q)\int_0^{\infty} n(x)dx$$

- When $V_G > V_{TH}$,
  - The electron charge density is proportional to $V_G - V_{TH}$.

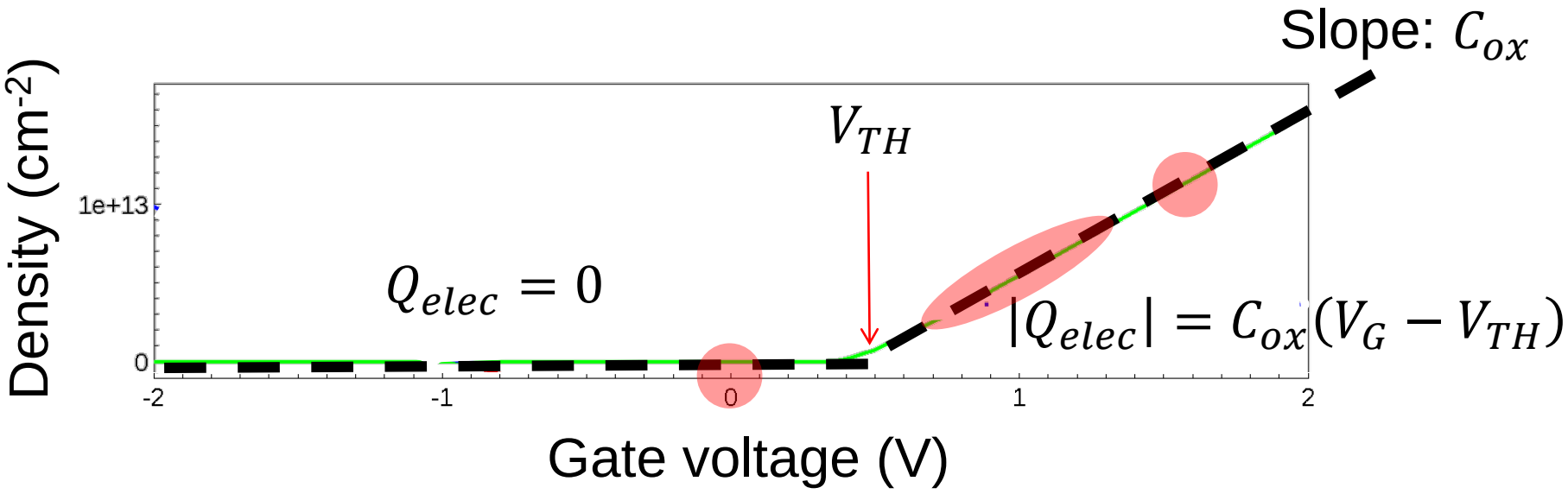
$$|Q_{elec}| = C_{ox}(V_G - V_{TH})$$

  - (Here, Q_{elec} and C_{ox} are quantities *per area*.)
- When $V_G < V_{TH}$,
  - The electron charge density vanishes.

$$Q_{elec} = 0$$

$|Q_{elec}|$ versus V_G

- It is piecewise linear. Therefore, it is nonlinear.
  - Digital application: ON ($V_G = V_{DD}$) / OFF ($V_G = 0$)
  - Analog application: Linear part



Engineering questions

- Which one is good?
  - Large C_{ox} or small C_{ox}?
  - Answer) We want to have a large C_{ox}. Therefore, a thin oxide layer is desirable.
  - High V_{TH} or low V_{TH}?
  - Answer) Depending on V_{DD}, an appropriate value of V_{TH} should be chosen. By changing the metal or the substrate doping, we can control V_{TH}.

- These parameters are determined by the manufacturer.
  - Designers select the circuit topology.
  - Designers select sizes of transistors.