Lecture8: Metal-Oxide-Semiconductor

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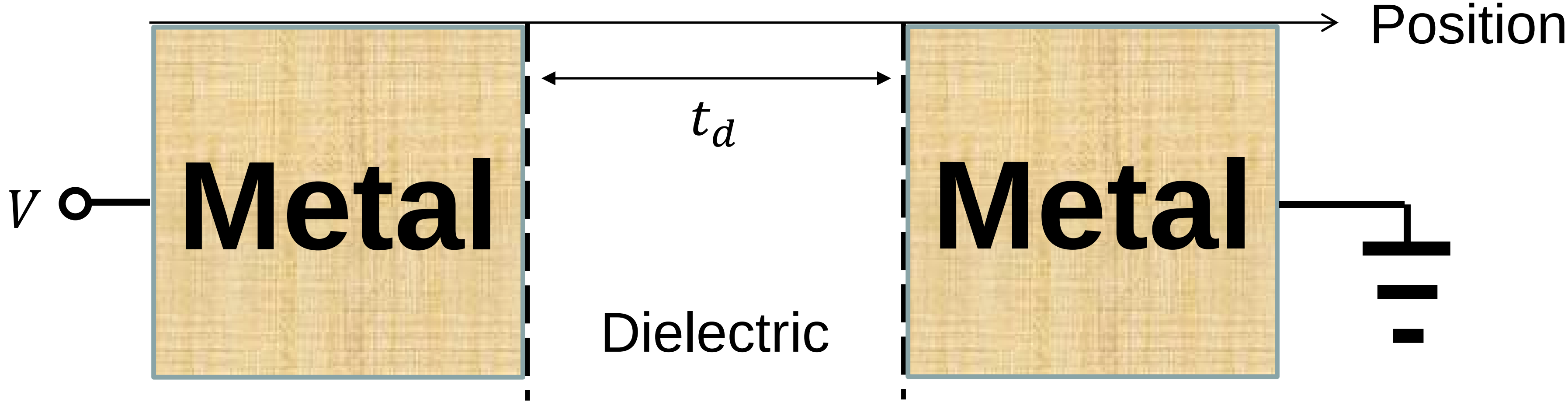
Parallel plates

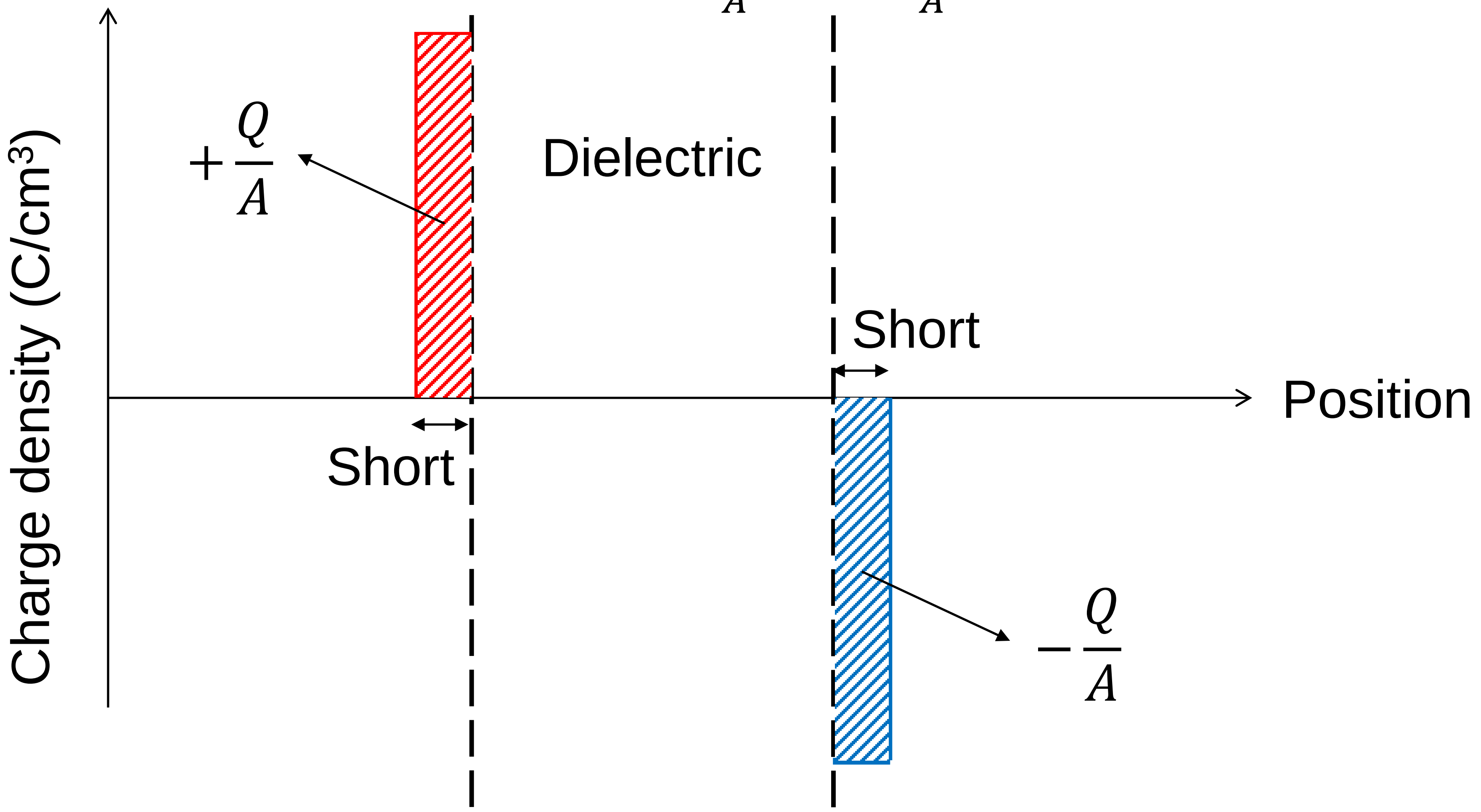
- A problem from “General Physics” course.
  - Consider a dielectric layer (whose thickness is t_d and area is A) sandwiched by two parallel metal plates. Its permittivity is ϵ_d.
  - A voltage difference, V, is applied.
  - The charges are $+Q$ and $-Q$, respectively.
  - The Gauss law in the 1D structure

$$\frac{d}{dx}(\epsilon E_x) = \rho$$



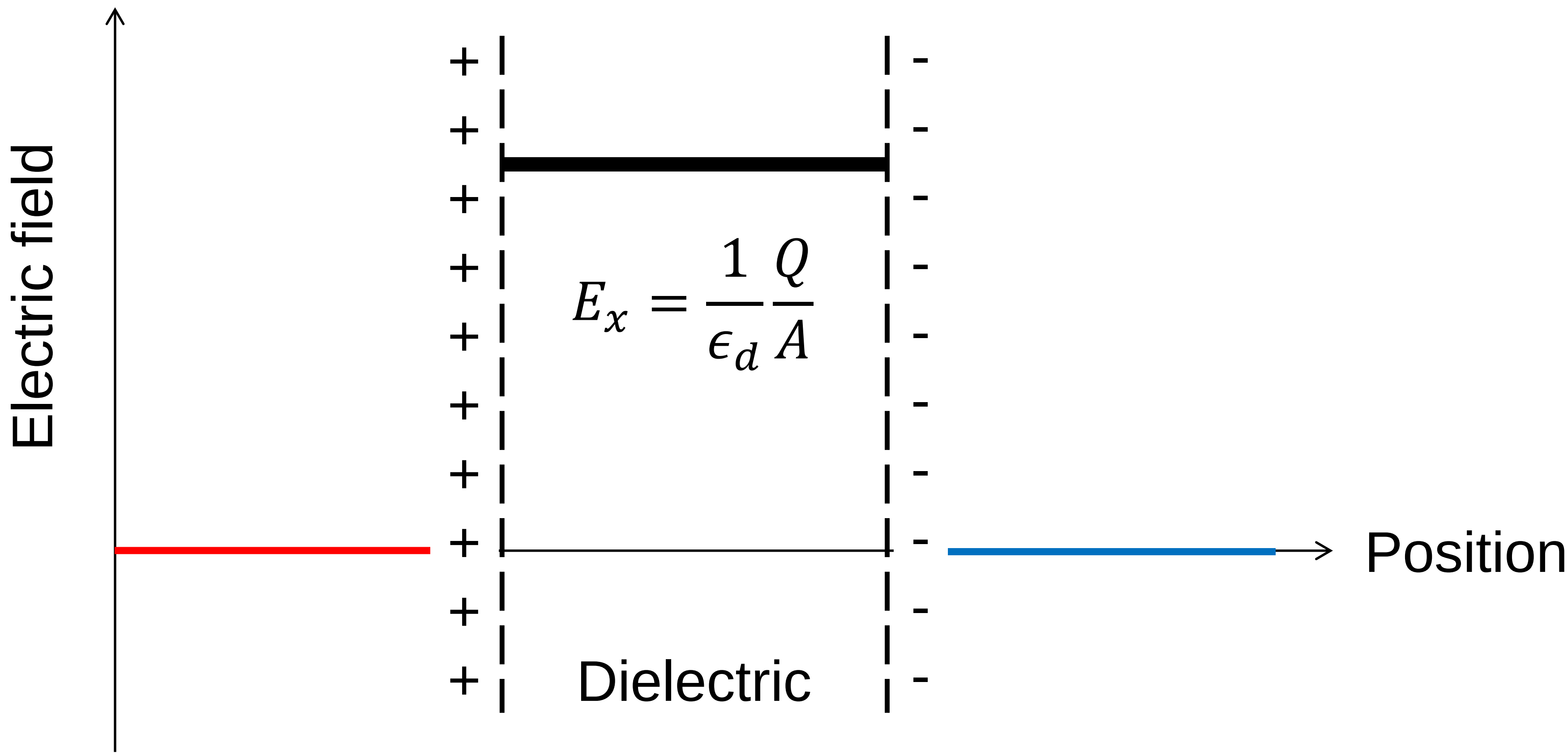
Charge density

- Areal charge densities are $+\frac{Q}{A}$ and $-\frac{Q}{A}$.



Electric field

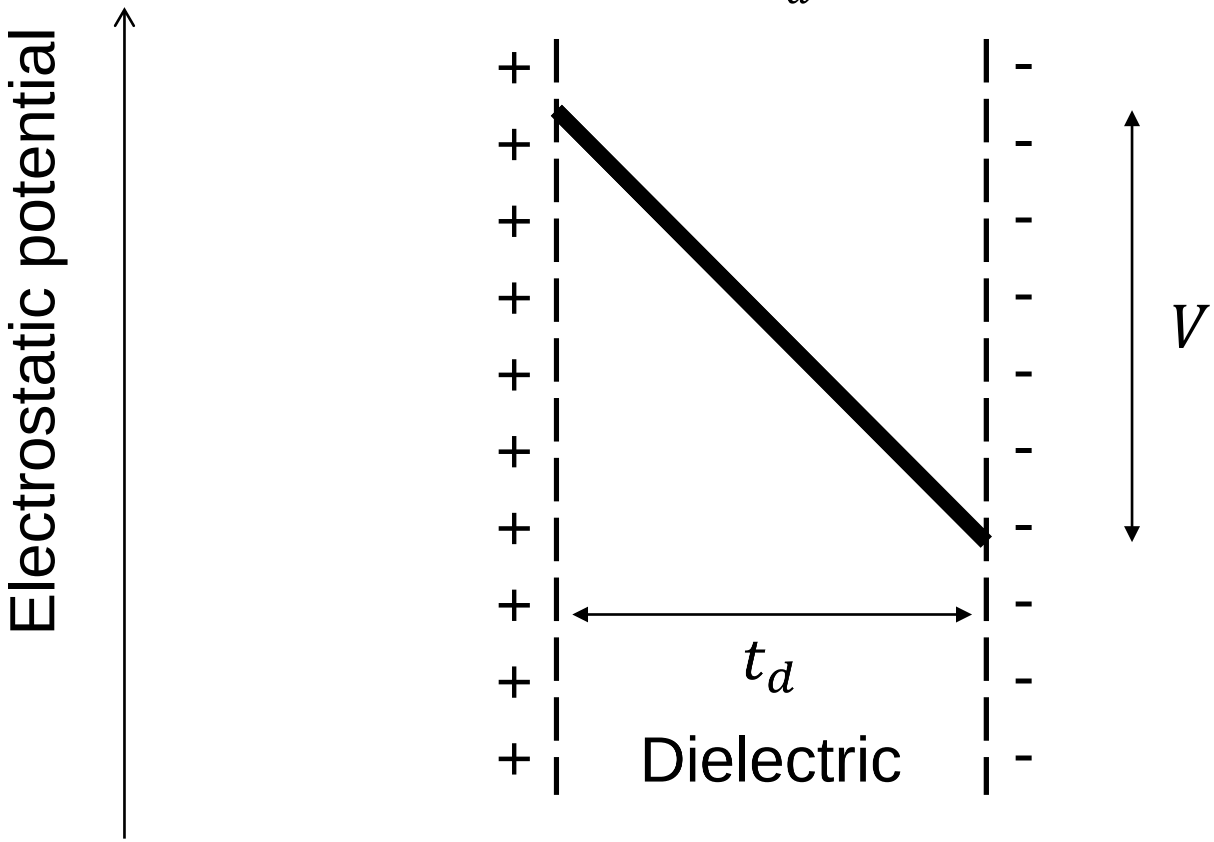
- Electric field inside the dielectric layer is $\frac{1}{\epsilon_d}\frac{Q}{A}$.
  - Constant over the dielectric layer



Electrostatic potential

- Solve $-\frac{d\phi}{dx} = E_x$.

$$V = \frac{1}{\epsilon_d}\frac{Q}{A}t_d$$



Capacitance

- The capacitance charge depends on the applied voltage.
  - From the previous equation,

$$Q = \epsilon_d \frac{V}{t_d} A$$

  - Remember that, for a capacitor,

$$Q = CV$$

  - Therefore, the capacitance becomes

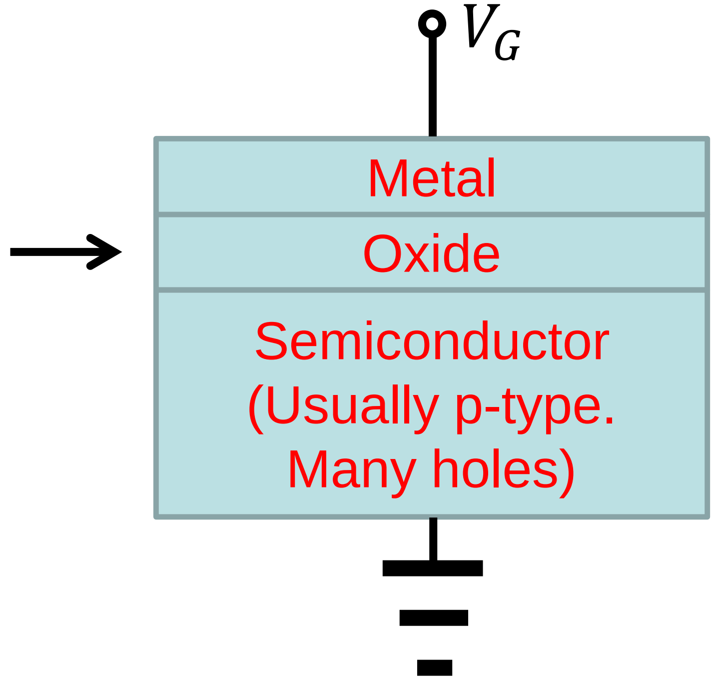
$$C = \frac{\epsilon_d}{t_d} A$$

  - (Sometimes, the capacitance *per unit area*, $\frac{\epsilon_d}{t_d}$, is also written as C. Yes, it's confusing.)

Metal-Oxide-Semiconductor

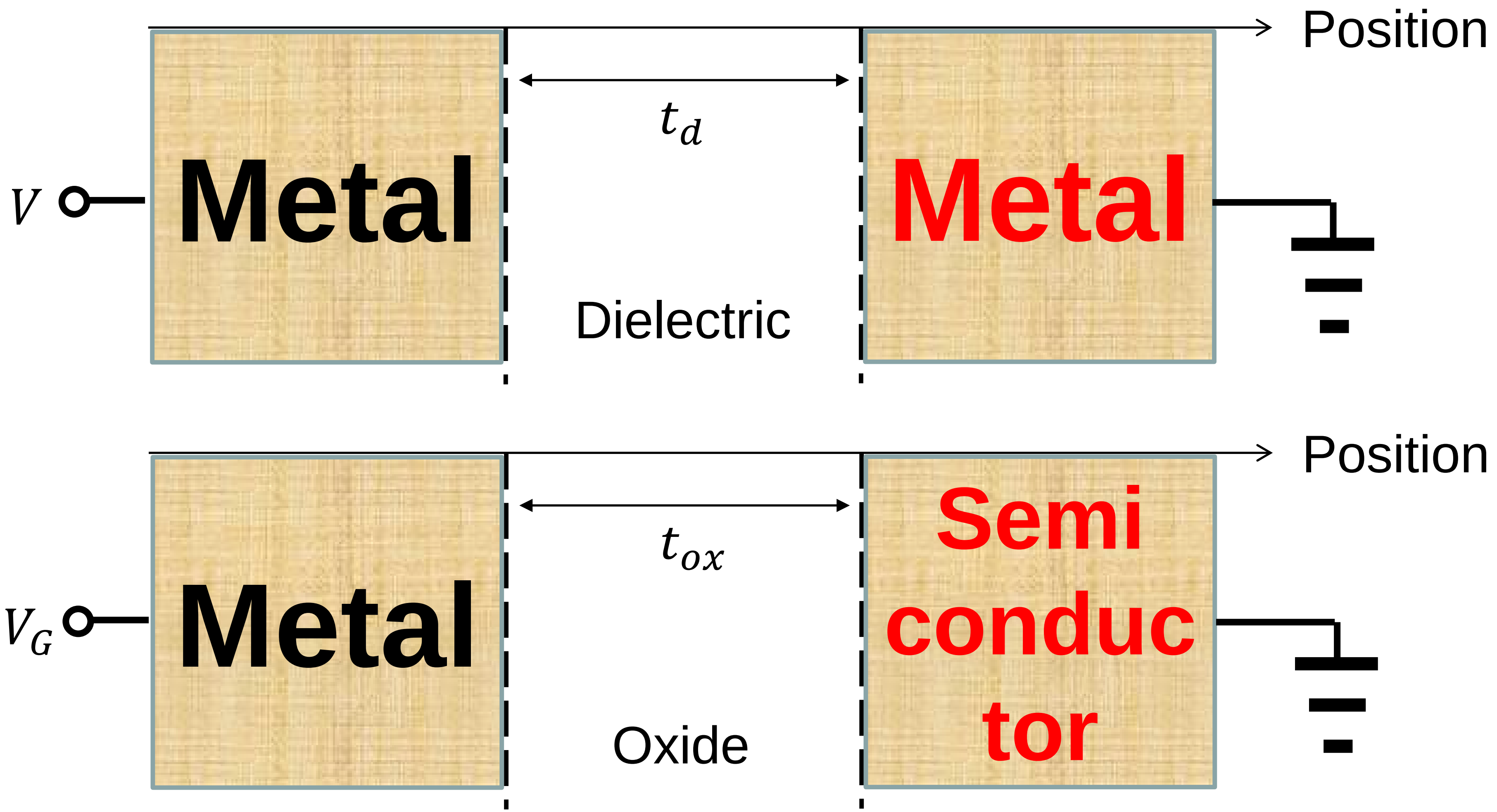
- The key structure in the microelectronics
  - Question: Is the MOS a capacitor with $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$?
  - Answer: No.

Its thickness, t_{ox}



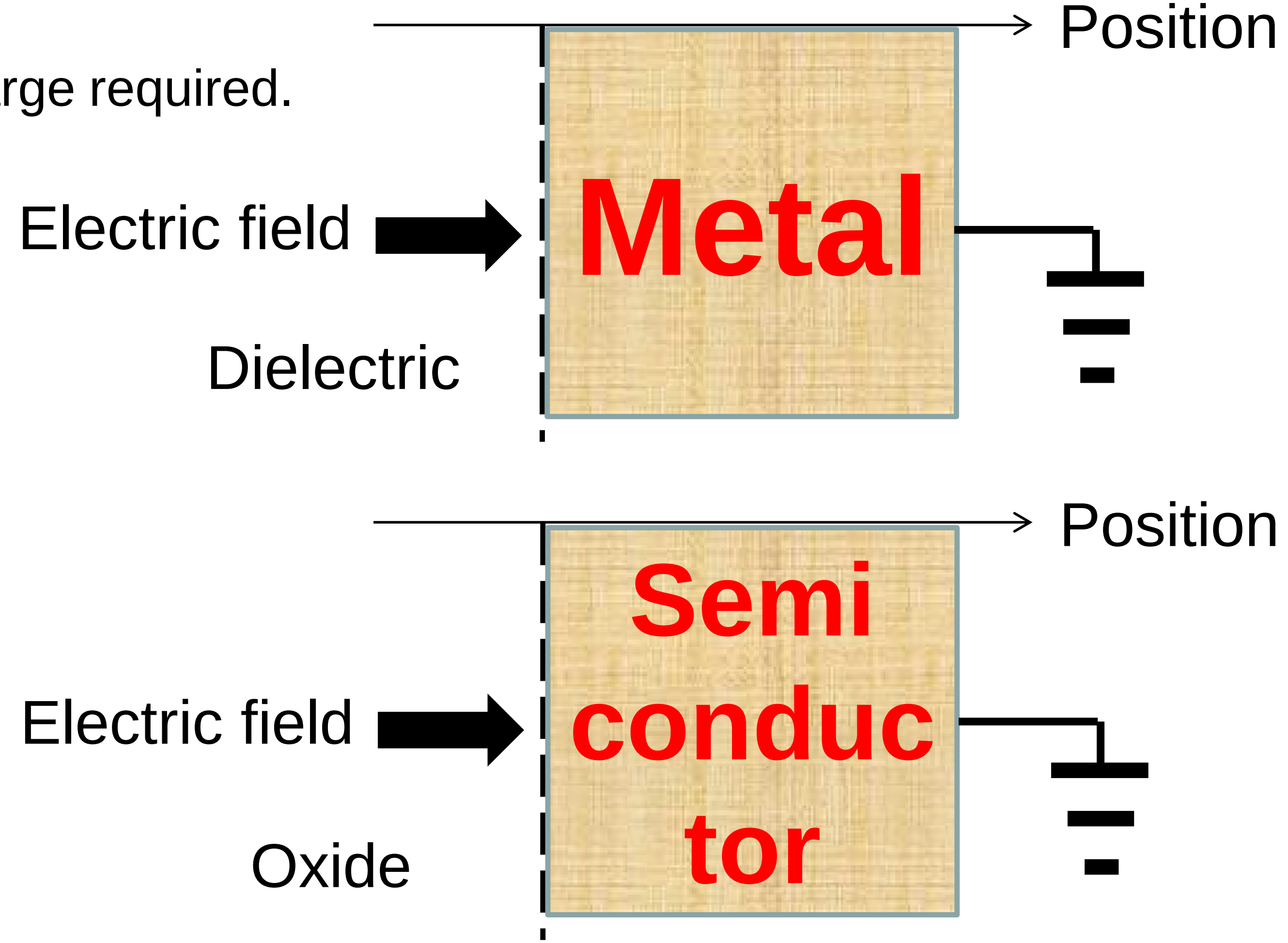
What is the difference?

- Metal versus semiconductor



The same electric field

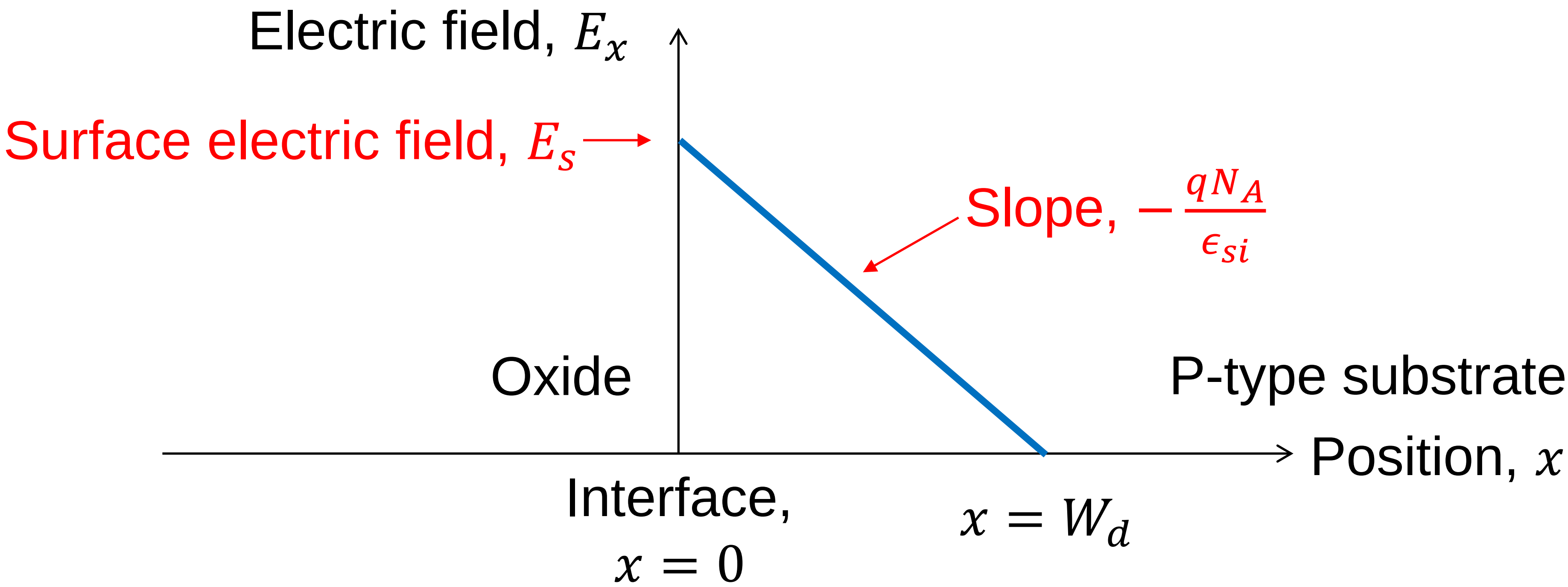
- Deep inside metal or semiconductor, we have no electric field.
  - Negative charge required.



P-type substrate

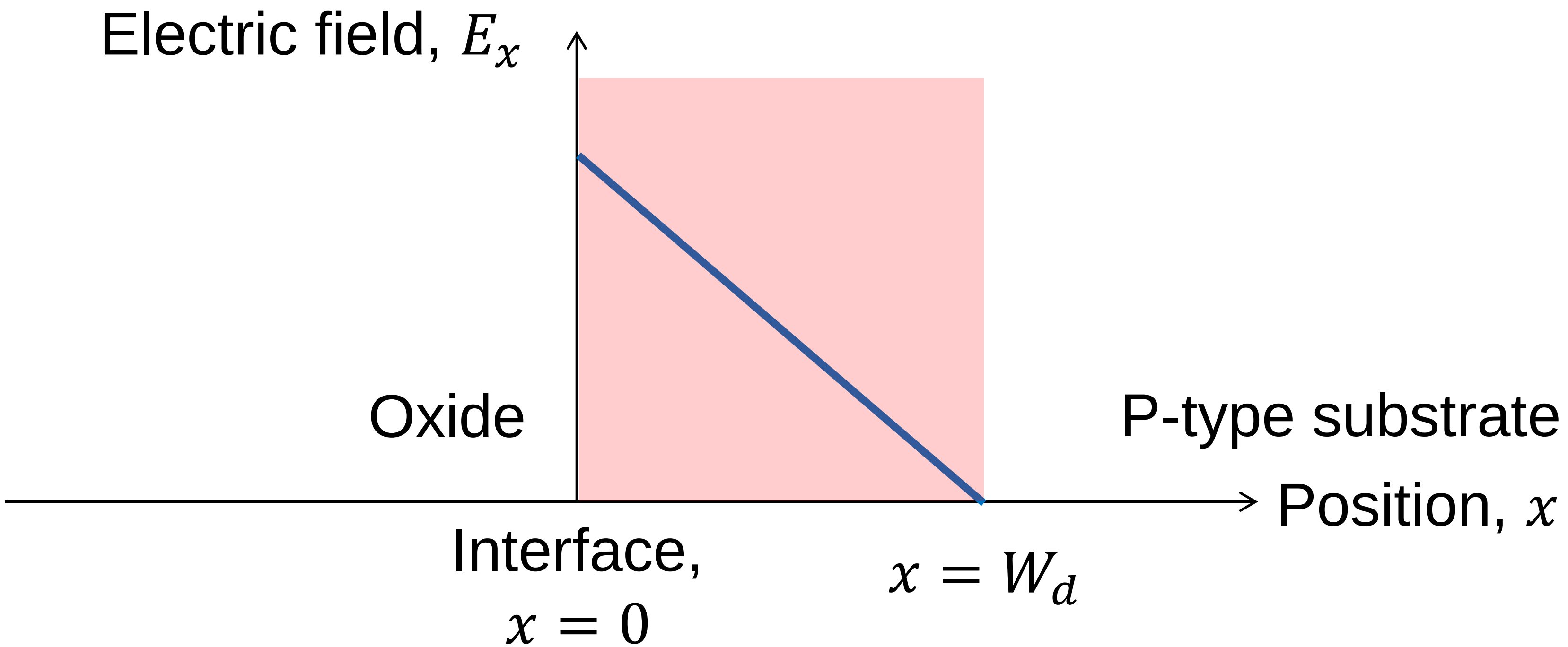
- Just like the PN junction, the P-type substrate can provide a negative charge by the depletion!

$$E_s - \frac{qN_A}{\epsilon_{si}} W_d = 0$$



Depletion

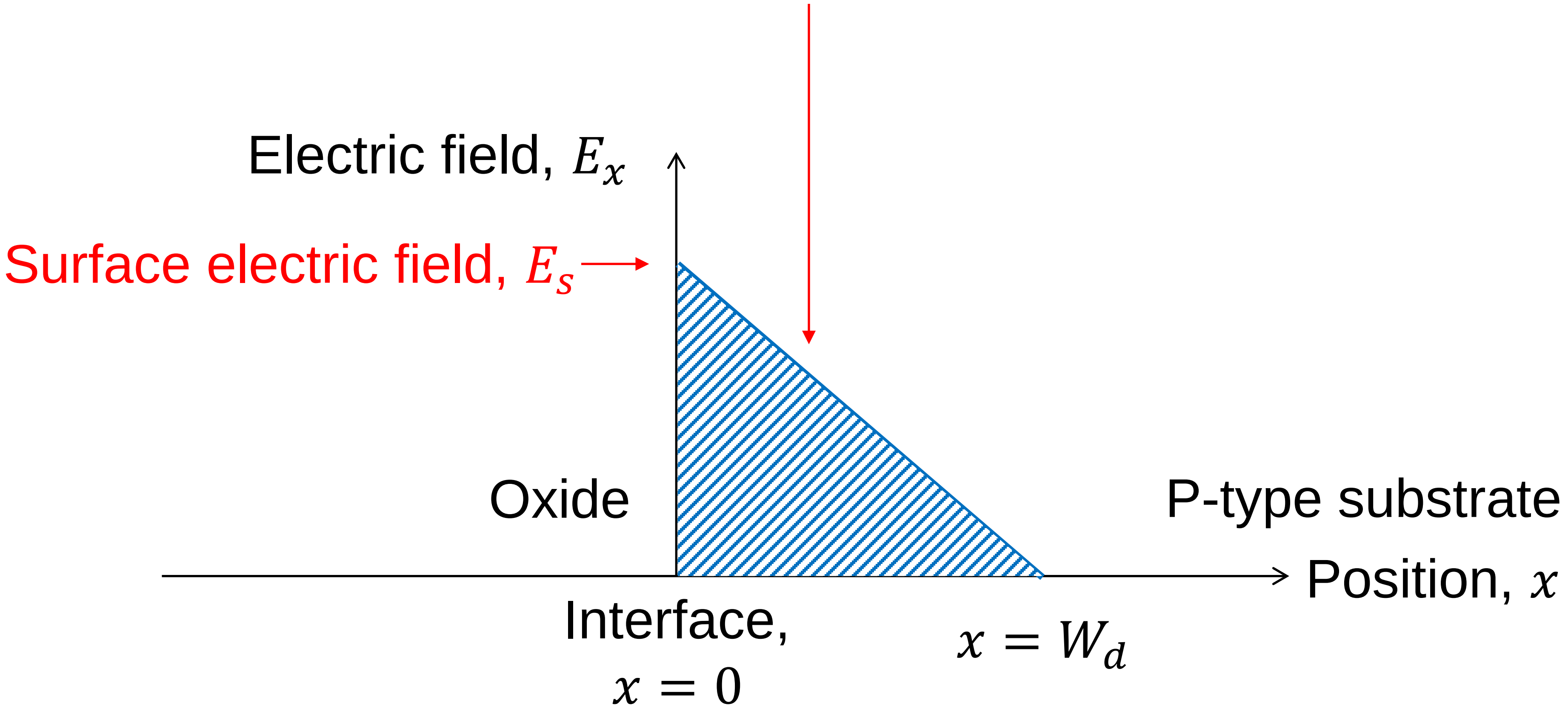
- Up to $x = W_d$, we have no hole. We have no electron.
  - MOS structures are intentionally designed to be in such a situation at $V_G = 0\ \mathrm{V}$.
  - In other words, with $V_G = 0\ \mathrm{V}$, we have no charge carrier at the semiconductor/oxide interface.



Potential difference

- By integrating the electric field,

$$\phi(0) - \phi(W_d) = \frac{1}{2} E_s W_d = \frac{\epsilon_{si}}{2qN_A} E_s^2$$



Electron density

- At equilibrium, there is a relation of (Probably you remember it.)

$$n = n_i \exp \frac{\phi}{V_T}$$

  - At $x = W_d$, we have

$$n(W_d) = n_i \exp \frac{\phi(W_d)}{V_T} = \frac{n_i^2}{N_A}$$

  - At $x = 0$, we have

$$n(0) = n_i \exp \frac{\phi(0)}{V_T} = n_i \exp \frac{\phi(W_d)}{V_T} \exp \frac{\phi(0) - \phi(W_d)}{V_T}$$

  - In other words, the electron density at the interface is

$$n(0) = \frac{n_i^2}{N_A} \exp \frac{\phi(0) - \phi(W_d)}{V_T}$$

Inversion & threshold voltage

- For a high gate voltage, E_S is also high.
  - Consider a condition of

$$n(0) = \frac{n_i^2}{N_A} \exp \frac{\phi(0) - \phi(W_d)}{V_T} = N_A$$

  - It is realized by the potential difference of

$$\phi(0) - \phi(W_d) = 2V_T \log \frac{N_A}{n_i}$$

  - The electron density at the interface is the same with the P-type doping density.
  - This phenomenon is called the ***inversion***.
  - The gate voltage which meets the above condition is called the ***threshold voltage***.

Above the threshold voltage,

- Two mechanisms for negative charges
  - 1) Depletion of the P-type substrate
  - 2) Inversion electrons