# Lecture10: MOSFET

Sung-Min Hong (smhong@gist.ac.kr)

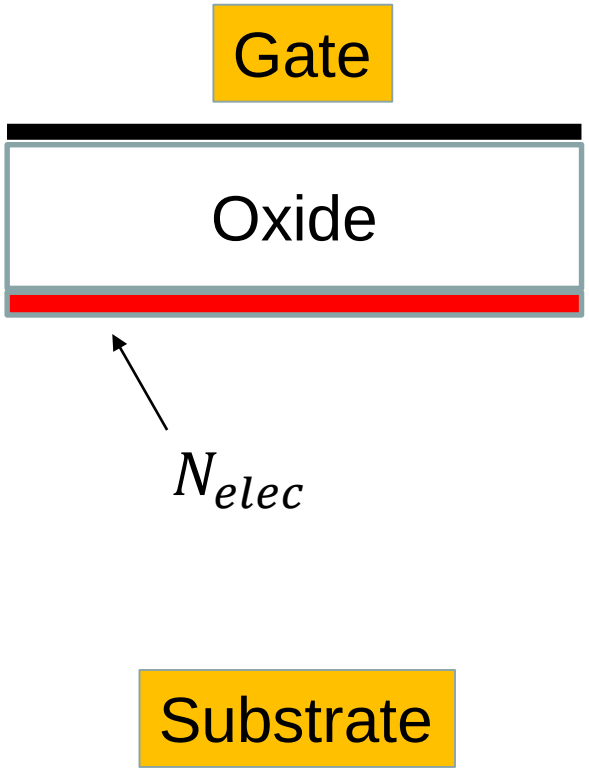
Semiconductor Device Simulation Lab.
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

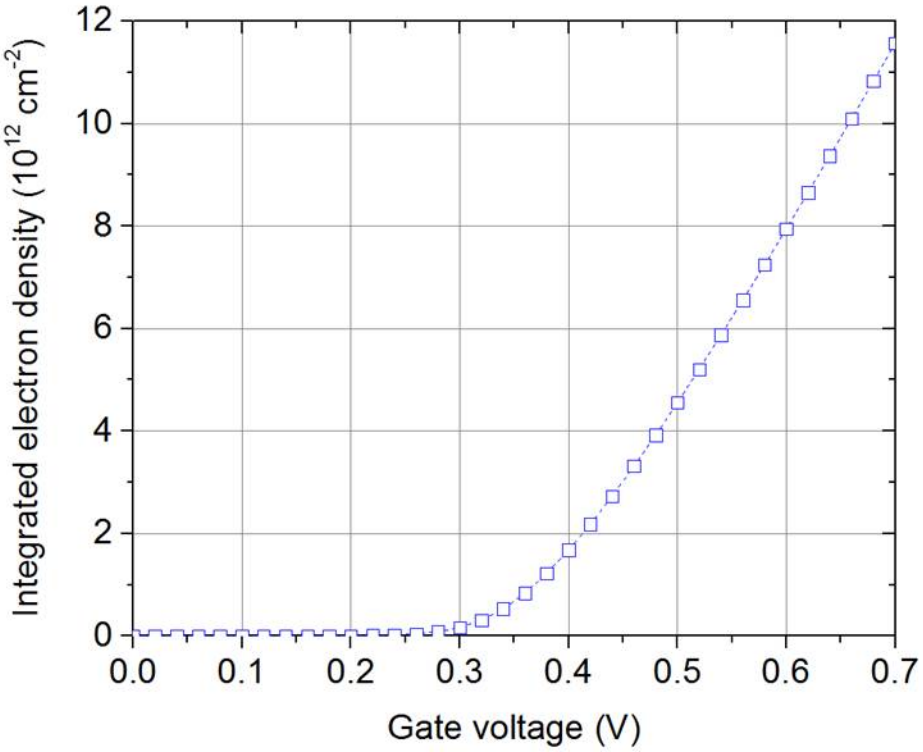
**GIST On-Line Lecture on April 20, 2020 (Internal use only)**

# MOS

- Metal-Oxide-Semiconductor
  - $V_G$ controls the total number of mobile electrons.

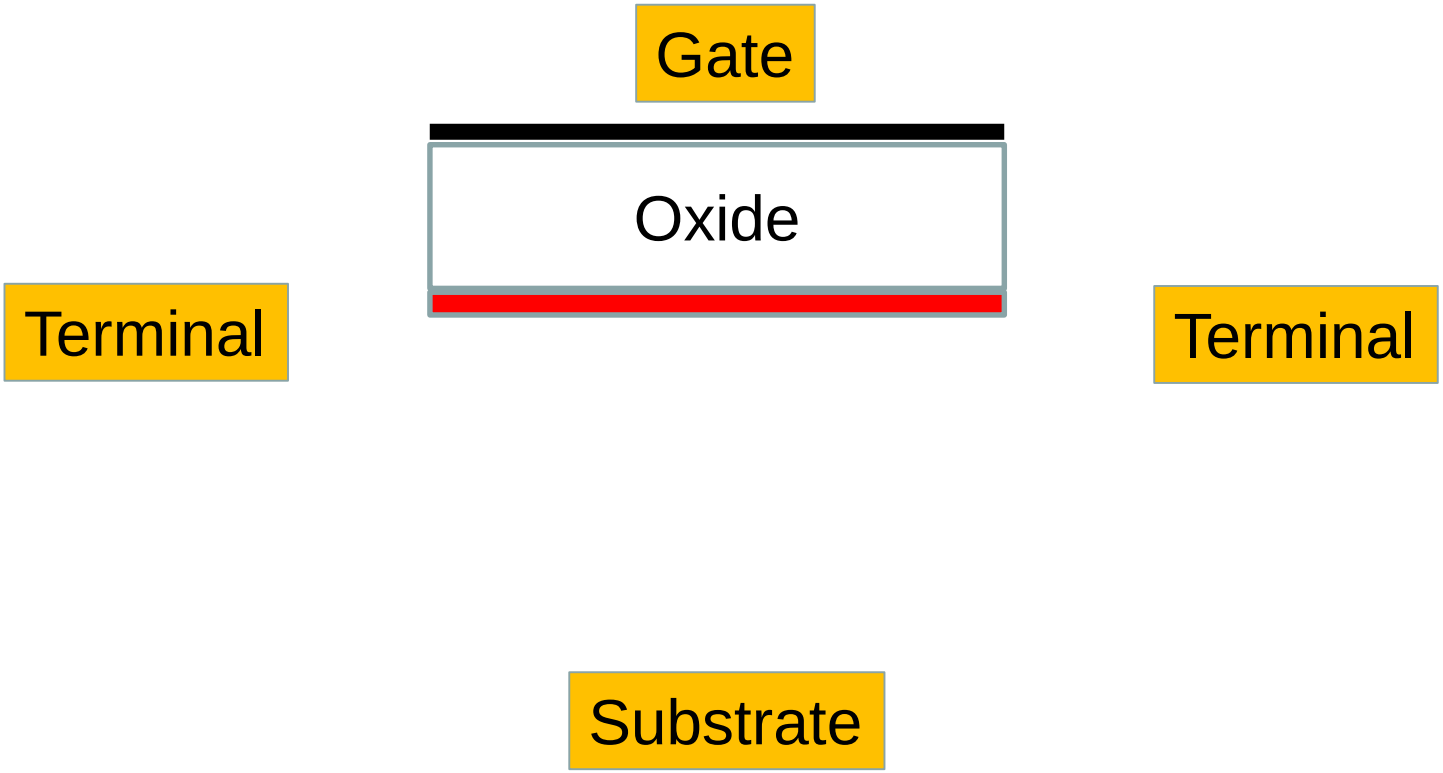
$$N_{elec} = C_{ox}(V_G - V_{TH})$$



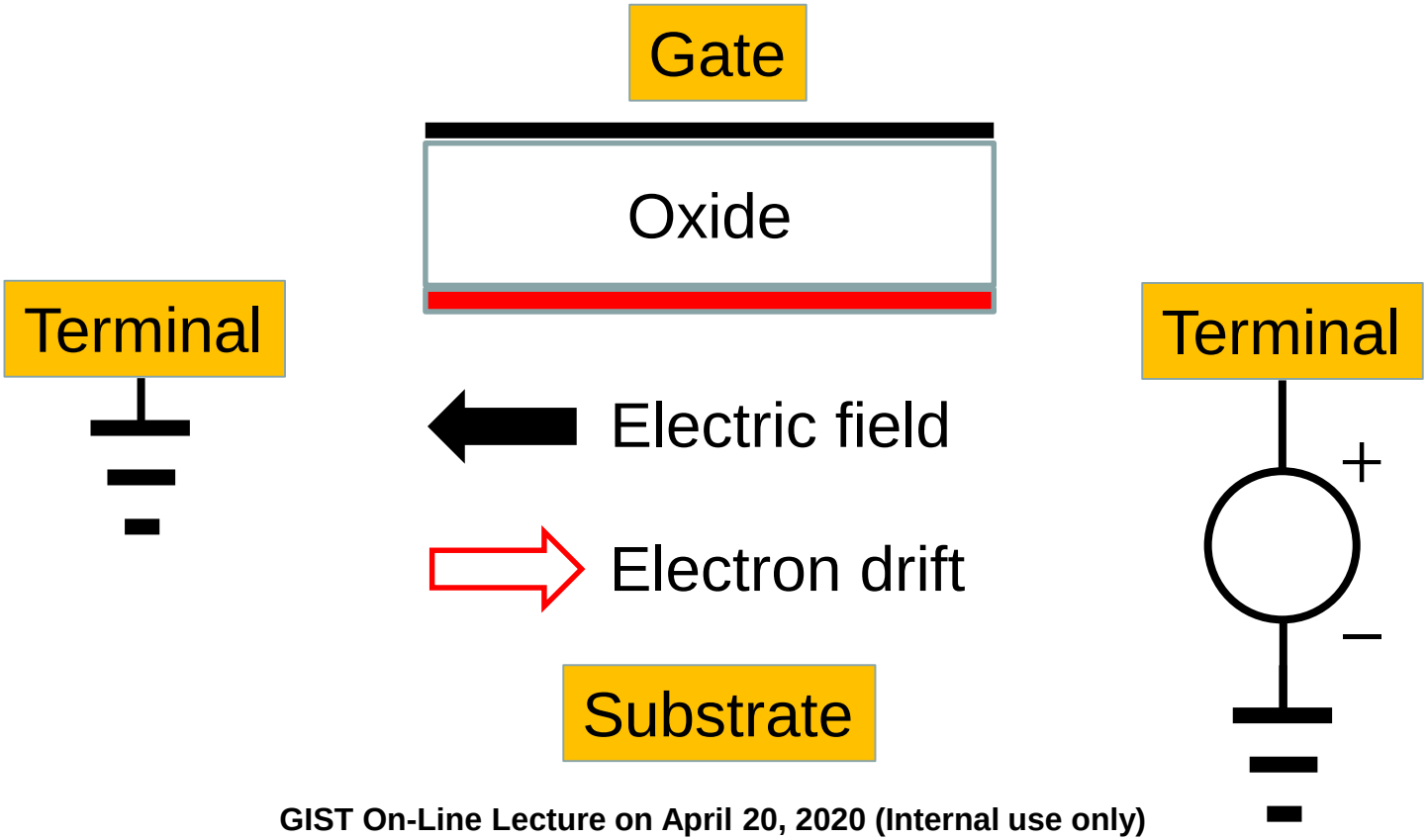
# MOSFET

- MOS + FET (Field-Effect Transistor)
  - Another electric field for the current conduction
  - We need two additional terminals.



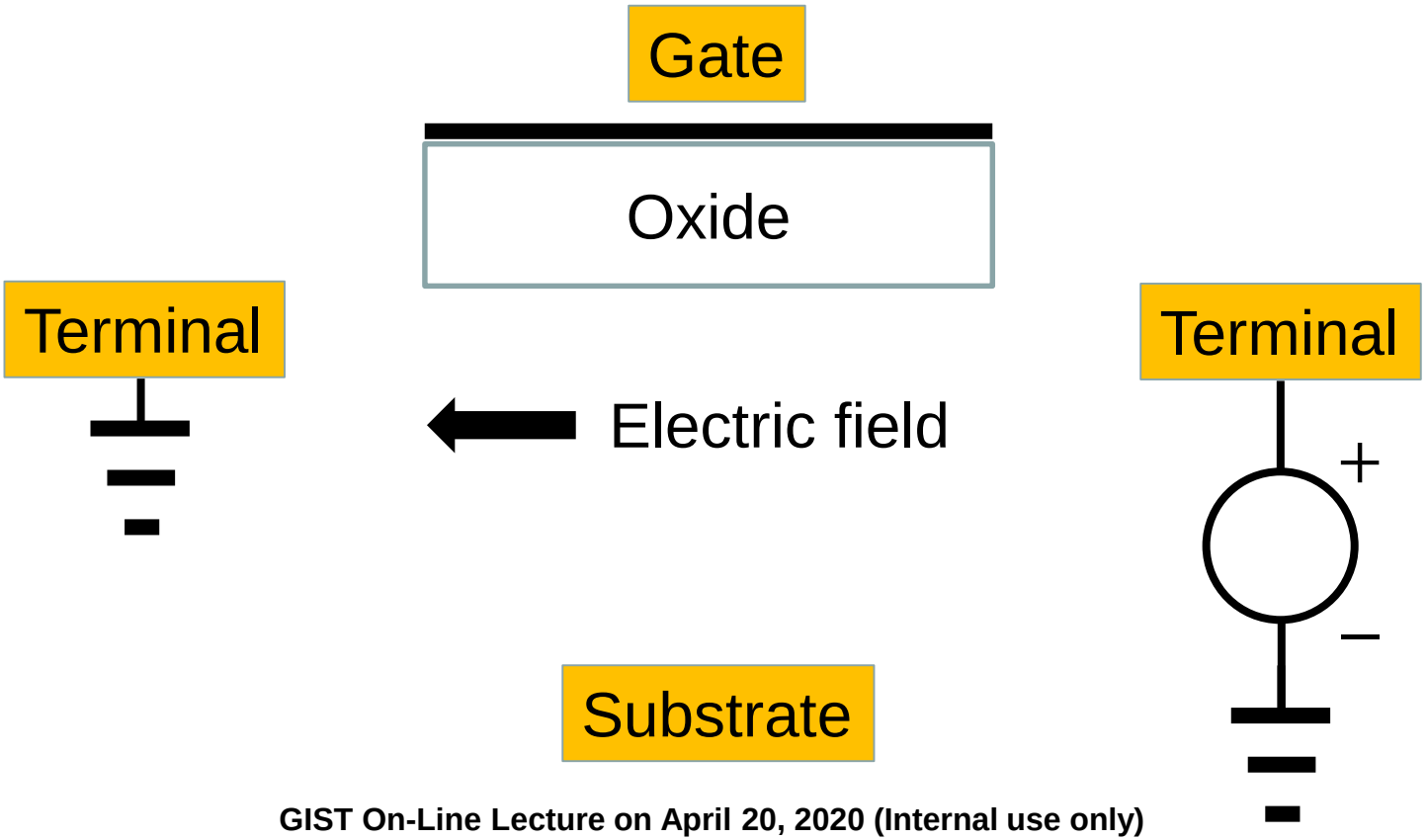
# Electron transport

- Assume that one terminal is positively biased.
  - Electron moves from the grounded terminal to the positively biased terminal.



# Of course,

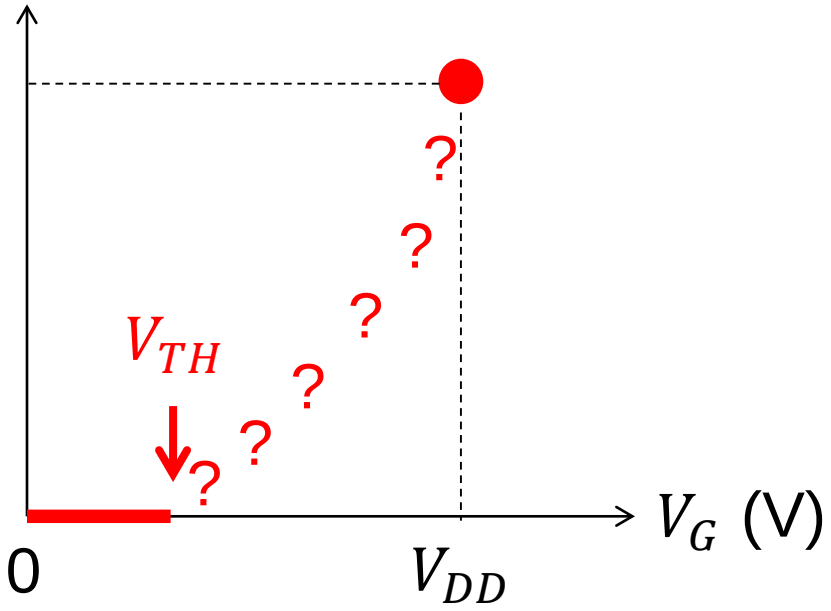
- When the gate voltage is lower than the threshold voltage,
  - There is no electric current.



# $I$ (of which one?) versus $V_G$

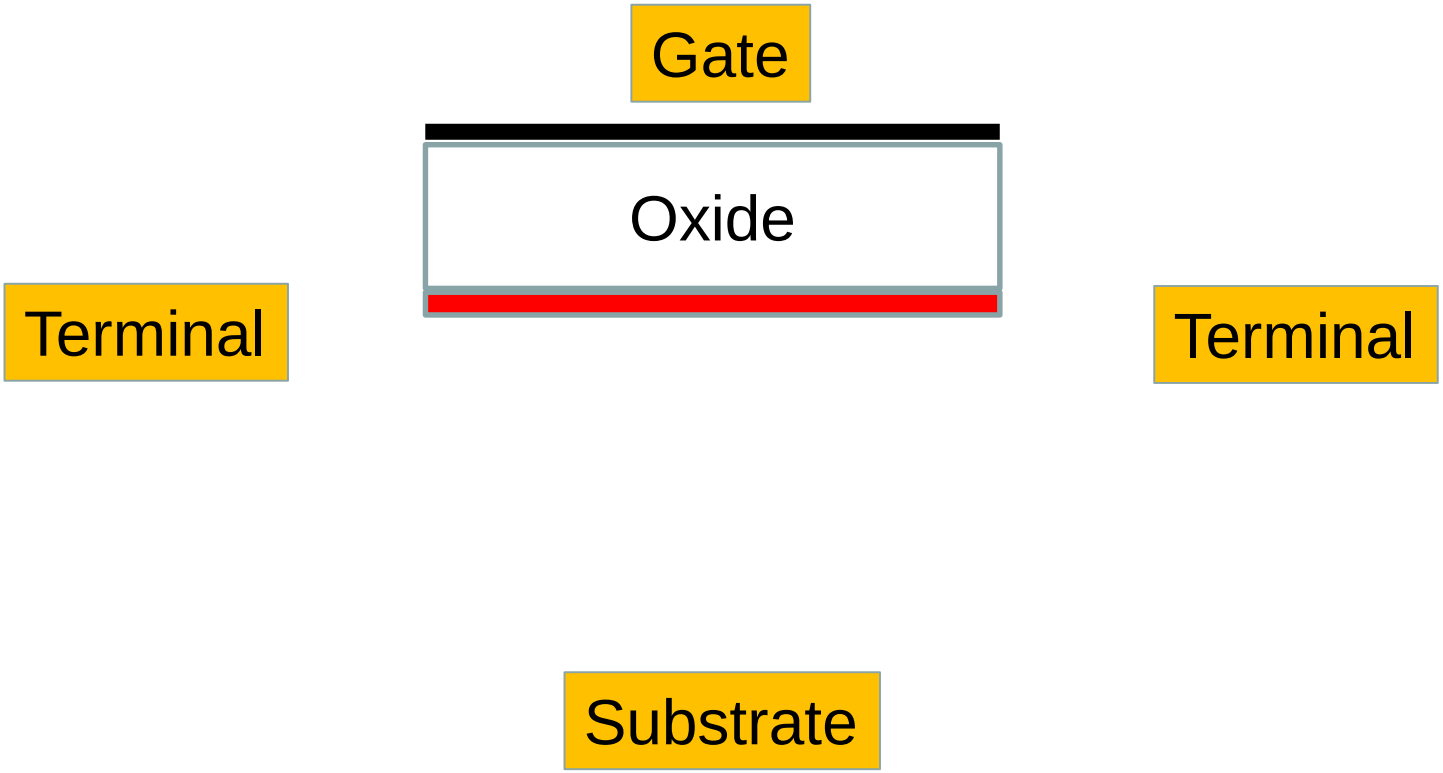
- Draw an IV curve.
  - Based upon the previous discussion, we can draw it partially.

$I$ of the positively biased terminal (A)



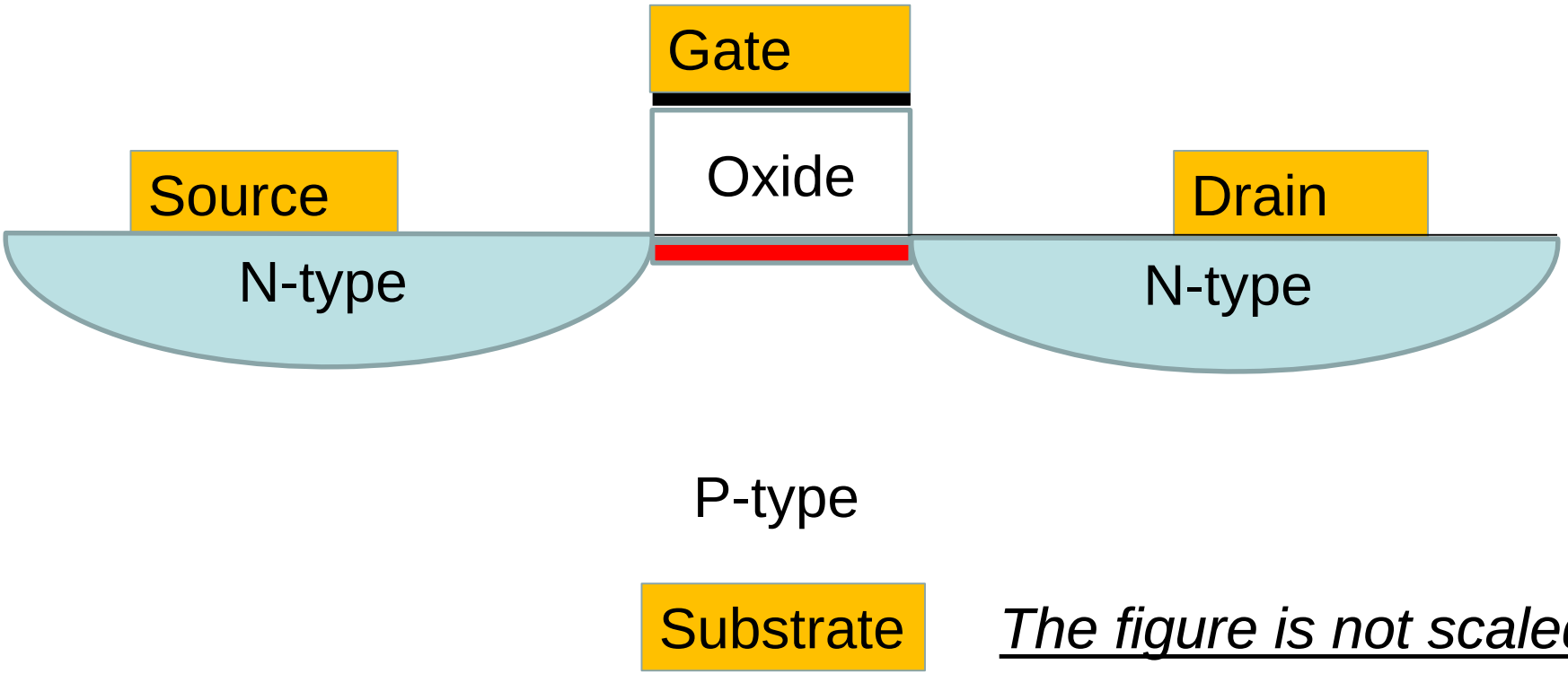
# Electric isolation

- How can we isolate terminals?
  - The gate terminal is perfectly isolated. No problem.
  - Substrate? Remember that it is P-type.



# Structure

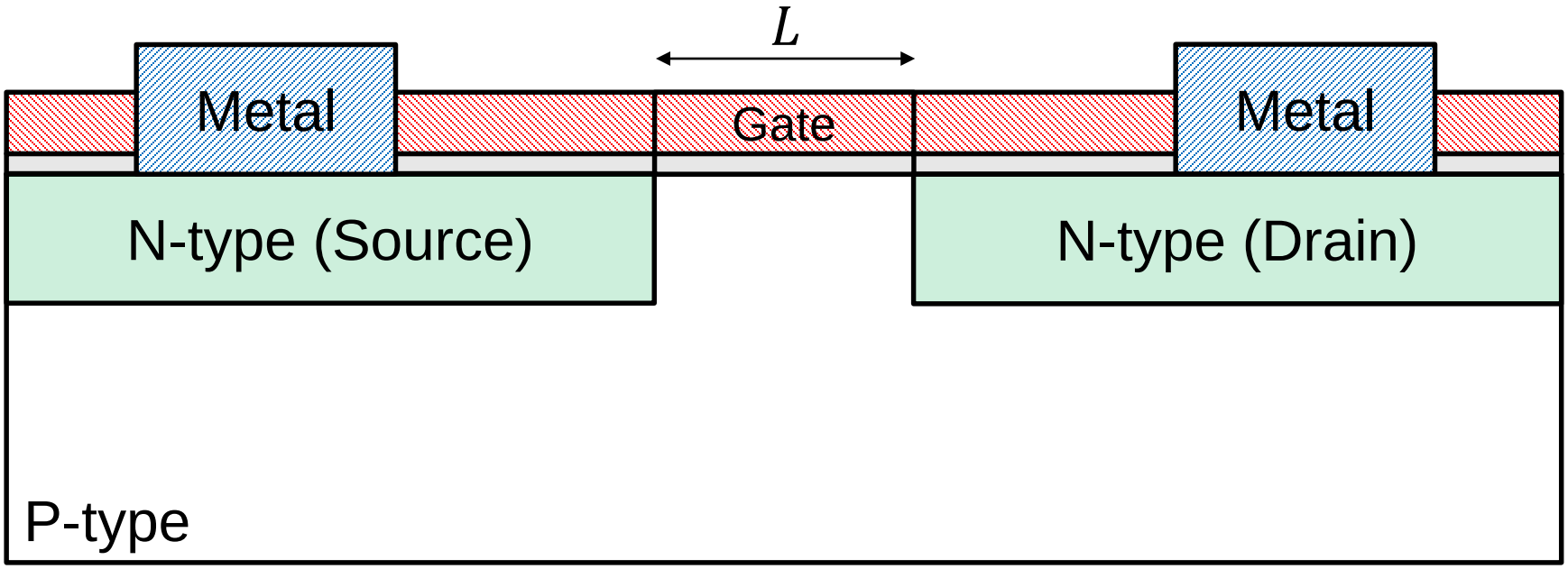
- PN junctions for the electric isolation
  - Source/Drain terminals on N-type regions
  - Substrate terminal connected to P-type substrate




*The figure is not scaled!*

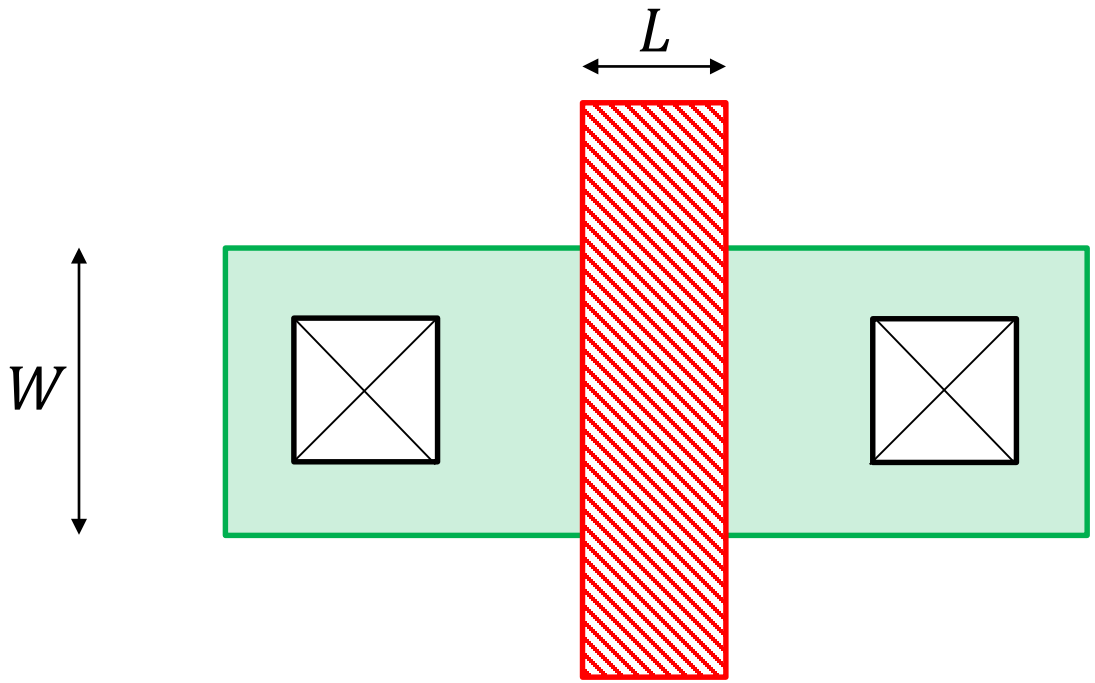
# Fabrication (Much simplified)

- Patterning by the photolithography
  - Oxide layer and gate material
  - Gate patterning
  - Source/Drain implantation
  - Metal contact formation



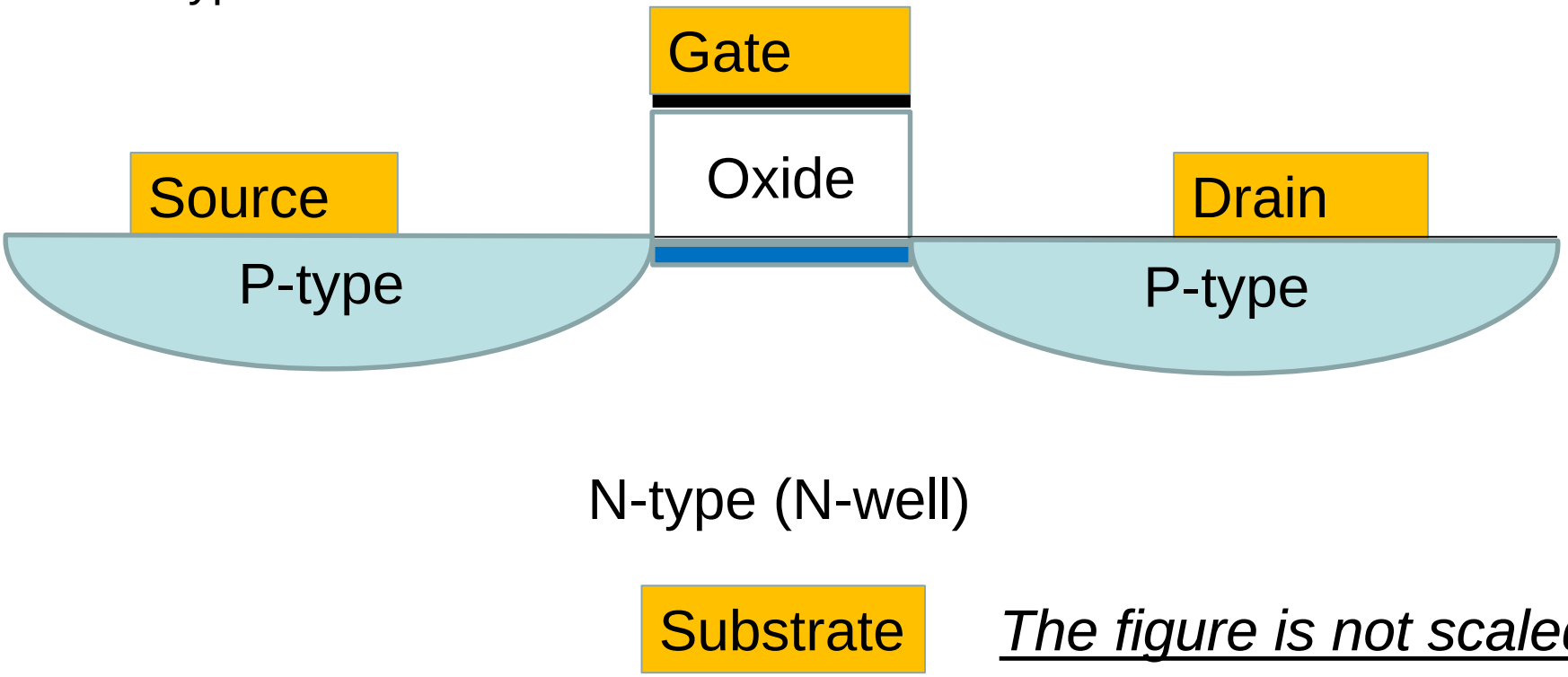
# Layout

- Layout designers draw the MOSFET with two boxes.
  - One for the diffusion region and the other for the gate material
  - Their intersection (length $L$ and width $W$) is important.



# PMOSFET

- A dual device to the NMOSFET
  - N-type substrate
  - Inversion holes for negative $V_G$ values
  - P-type source/drain




*The figure is not scaled!*