Lecture22:
NMOS inverter (2)

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After all,

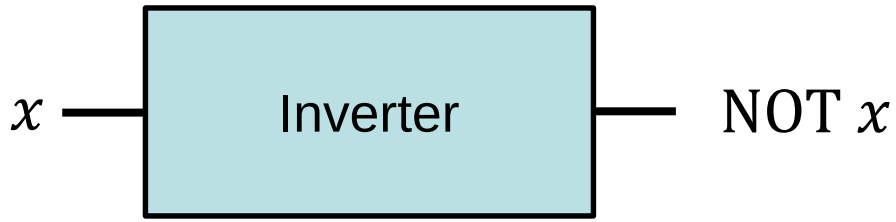
- As much as we have AND, OR, and NOT gates, we can implement any Boolean function.
  - For example,

$$x \text{ XOR } y = \big(x \text{ AND } (\text{NOT } y)\big) \text{ OR } \big((\text{NOT } x) \text{ AND } y\big)$$

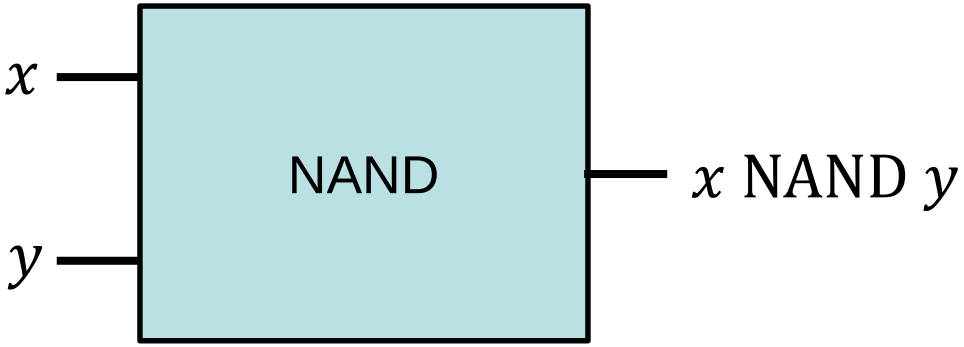
  - *With NAND, NOR, and NOT gates, we can, too.*

Inverter and NAND

- NOR can be implemented similarly.



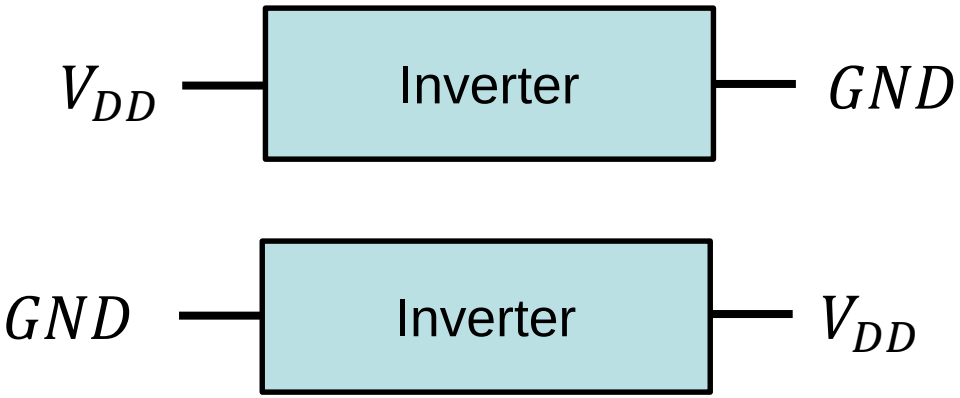
x	NOT
0	1
1	0

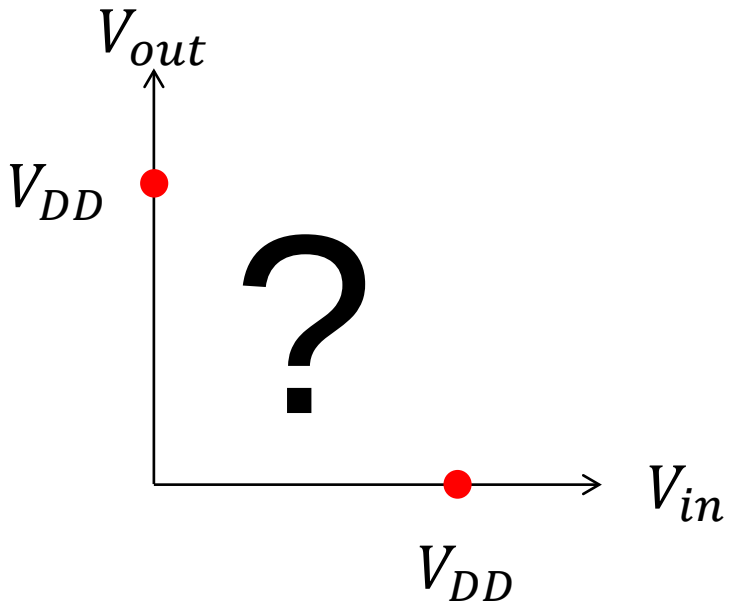


x	y	NAND
0	0	1
0	1	1
1	0	1
1	1	0

In circuit,

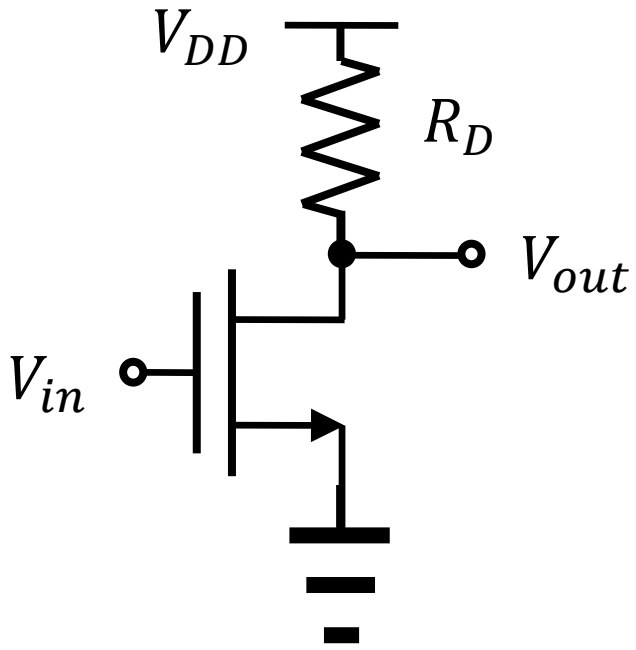
- How can we represent 0 and 1?
  - V_{DD} is assigned to the logical value, 1.
  - GND is assigned to the logical value, 0.





NMOS inverter

- How can we have an output, 0?
  - Only when the input is high. *You have seen it before!*



Vin	Vout
0	1
1	0

Voltage transfer

- When $V_{in} < V_{TH}$, trivially, $V_{out} = V_{DD}$.
- When V_{in} is slightly larger than V_{TH}, the NMOSFET is in the saturation region.

$$V_{out} = V_{DD} - I_D R_D$$

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2$$

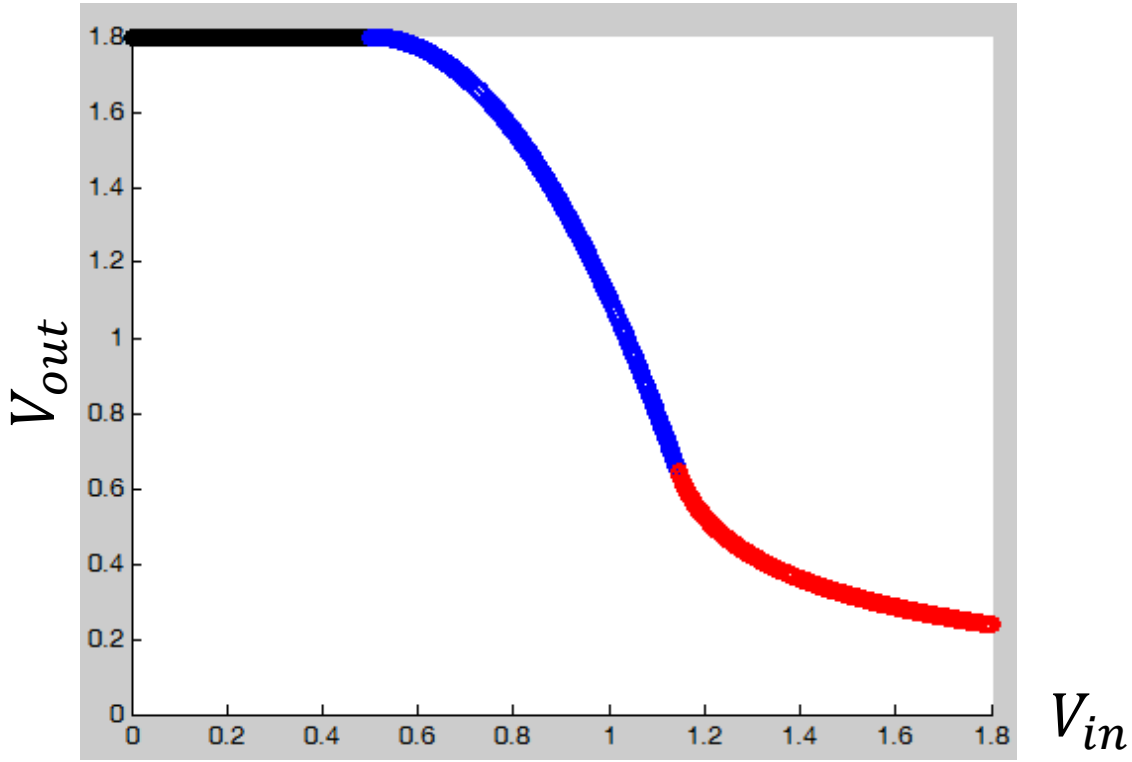
- When V_{in} is further increased, the NMOSFET is in the triode region.

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D[2(V_{in} - V_{TH})V_{out} - V_{out}^2]$$

Draw it! (1/2)

- Parameters in Example 17. 14 (Razavi) w/o modification.

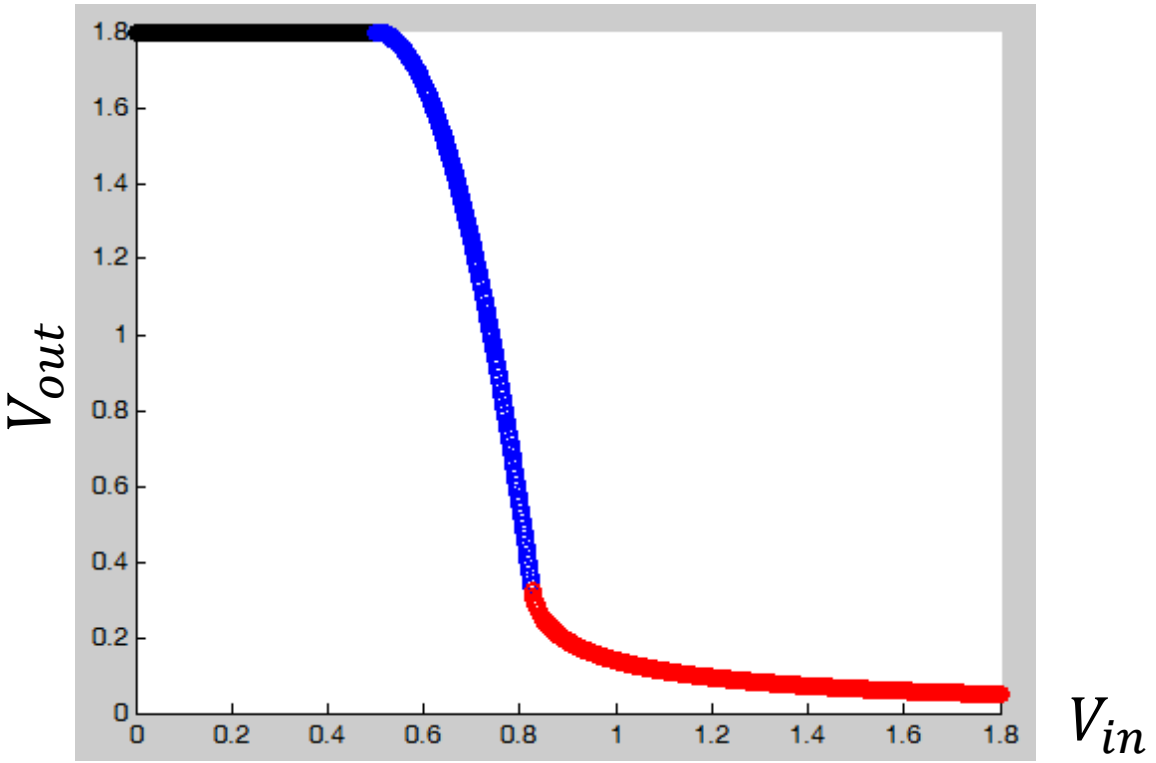
$\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $V_{TH} = 0.5\ \text{V}$, $\frac{W}{L} = \frac{10}{0.18}$, $R_D = 1k\Omega$ and $V_{DD} = 1.8\ \text{V}$



Draw it! (2/2)

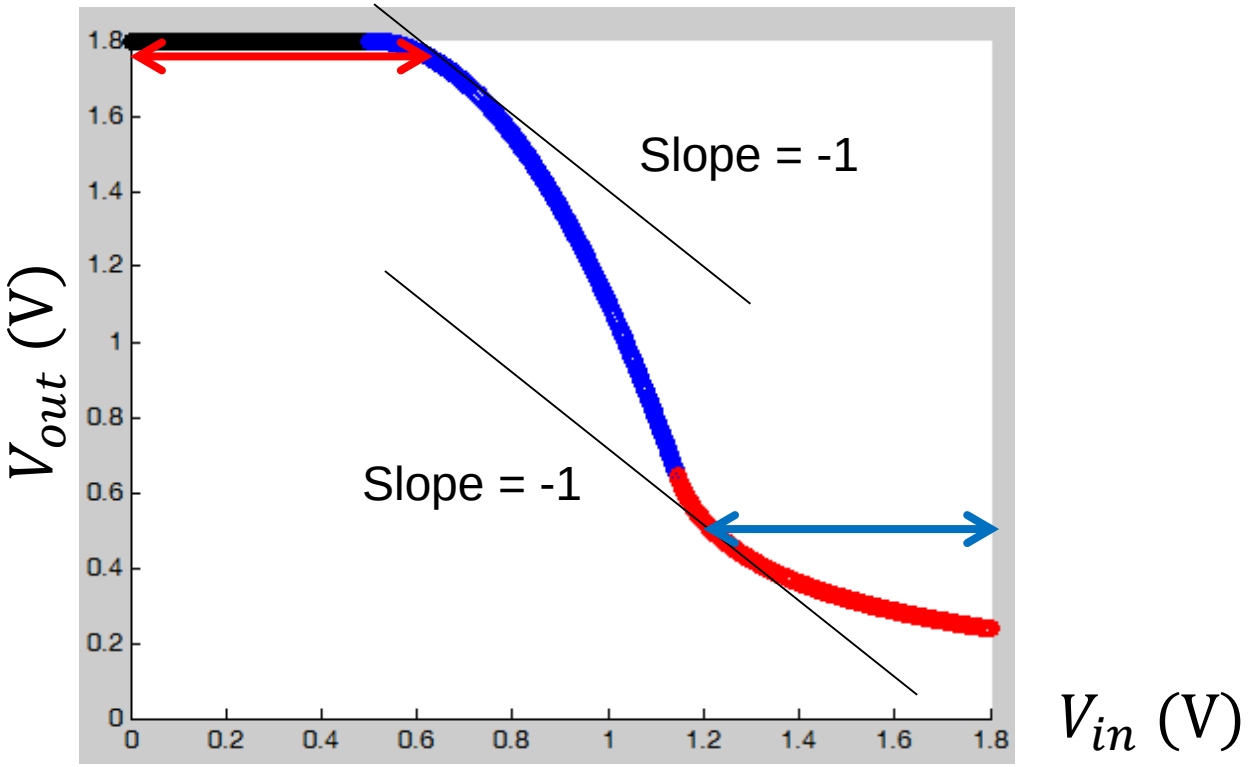
- With a wider NMOSFET

$\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $V_{TH} = 0.5\ \text{V}$, $\frac{W}{L} = \frac{50}{0.18}$, $R_D = 1k\Omega$ and $V_{DD} = 1.8\ \text{V}$



Noise margin

- Verbatim
  - “(It) is the maximum amount of degradation (noise) at the input that can be tolerated before the output is affected significantly.”



Noise margin of CS stage

- Let's calculate $NM_L = V_{IL}$.
  - In this case, (blue curve)

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2$$

  - Taking the differentiation w. r. t. V_{in},

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})$$

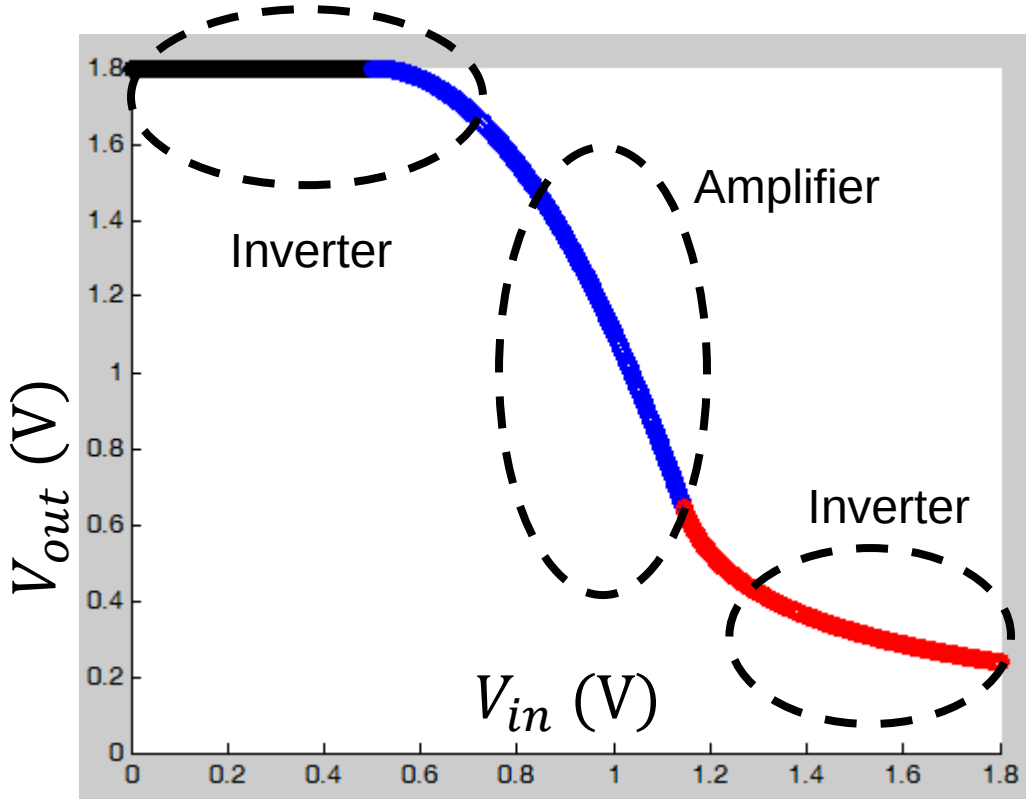
  - At $V_{in} = V_{IL}$, the slope becomes -1,

$$NM_L = V_{IL} = \frac{1}{\mu_n C_{ox}\frac{W}{L}R_D} + V_{TH}$$

  - (Stronger NMOS yields a reduces NM_L.)

Common-source

- Common-source configuration
  - It can be used as an inverter.
  - It can be used as an amplifier.
  - $\frac{dV_{out}}{dV_{in}}$ is the voltage gain.



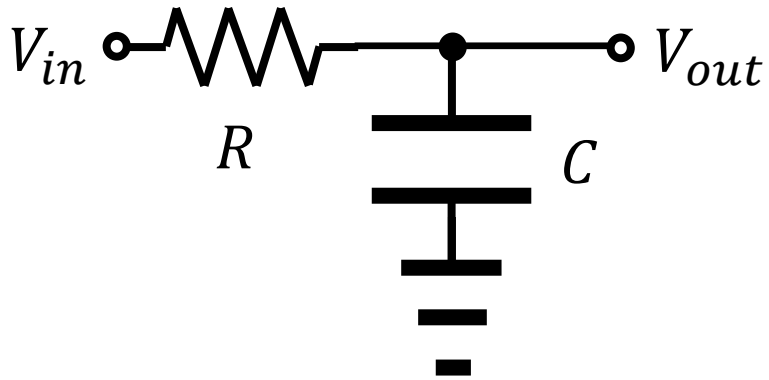
RC circuit

- Consider a serial RC circuit.
  - The KCL states

$$\frac{V_{out} - V_{in}}{R} + C\frac{dV_{out}}{dt} = 0$$

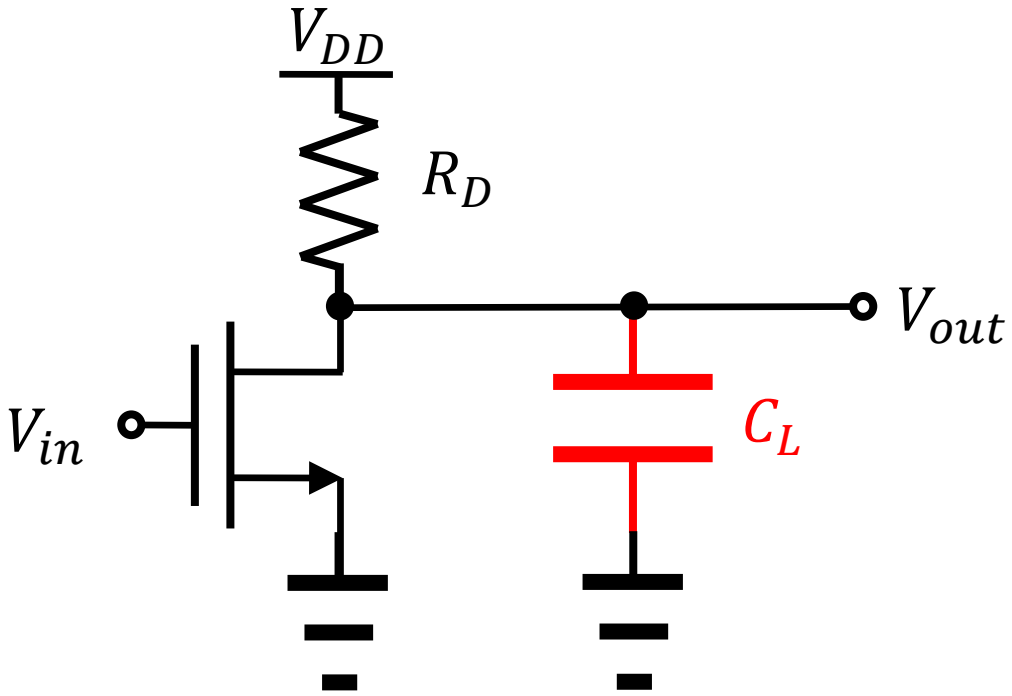
  - Assume a step-wise change of V_{in} at $t = 0$. It becomes V_{DD}.
  - Initial output voltage is V_0.
  - Its solution is given by

$$V_{out}(t) = V_{DD} + (V_0 - V_{DD})\exp\left(-\frac{t}{RC}\right)$$



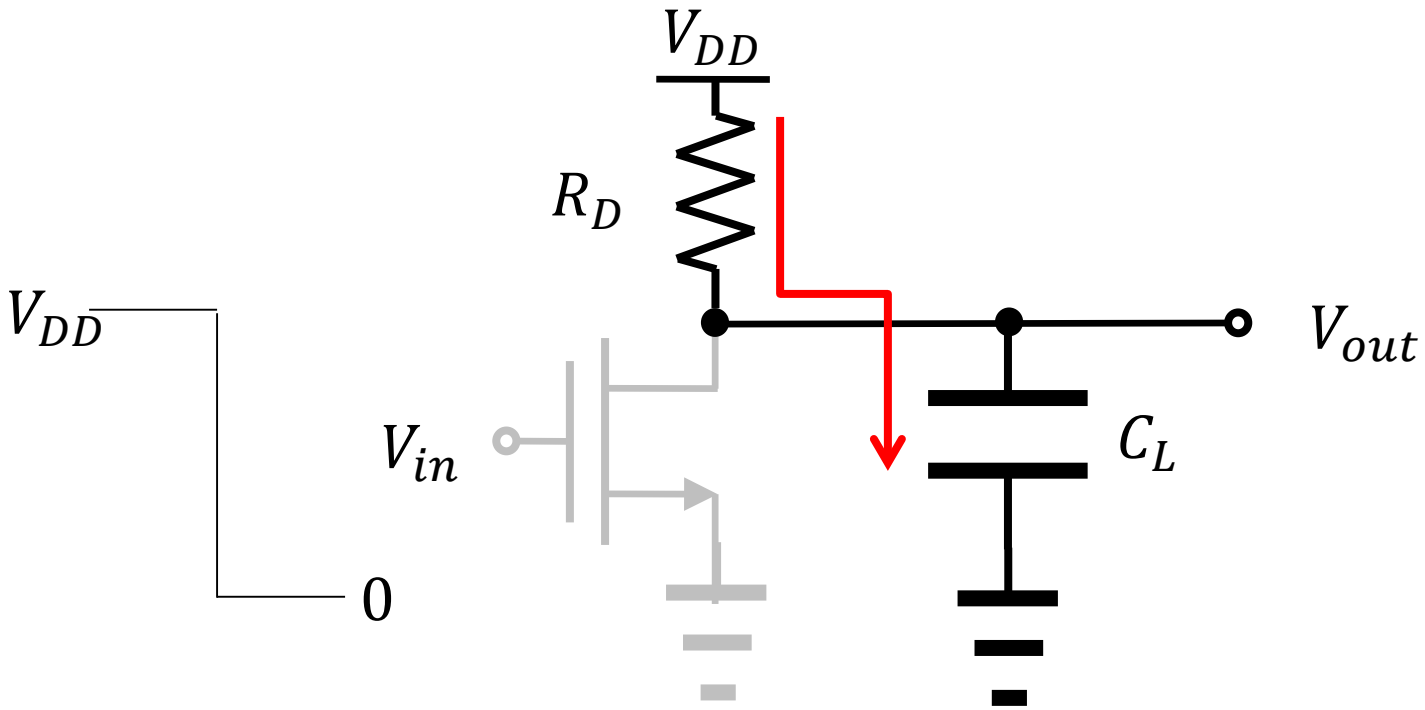
Speed of inverter (1/4)

- VTC merely describes the DC behavior.
  - Input voltages with different frequencies (1 kHz, 1 MHz, 1 GHz, …)
  - Time-dependent behavior



Speed of inverter (2/4)

- A rapid transition of V_{in} from V_{DD} to 0
  - The capacitor should be charged.



Speed of inverter (3/4)

- Simply, it is a RC circuit.
  - Then, the solution is simply

$$V_{out}(t) = V_{out}(0^-) + [V_{DD} - V_{out}(0^-)]\left(1 - \exp\frac{-t}{R_D C_L}\right)$$

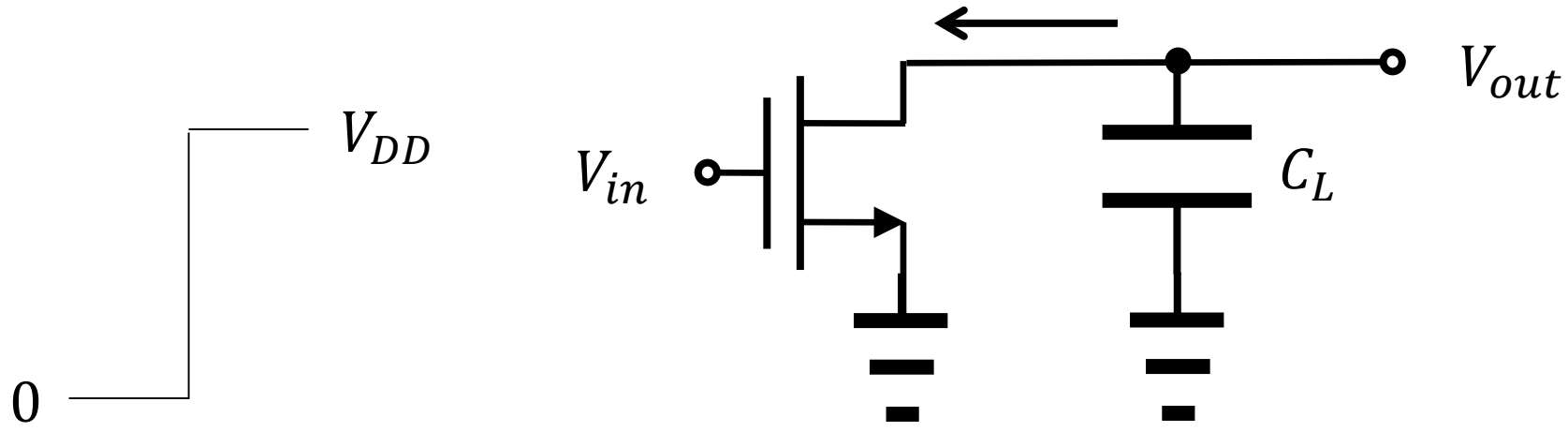
  - Since $\exp(-3) \approx 0.05$, after $3R_D C_L$, V_{out} reaches $0.95\ V_{DD}$.

  - Yes, it takes time to get the stable output voltage…
  - The delay restricts the maximum signal frequency.

Speed of inverter (4/4)

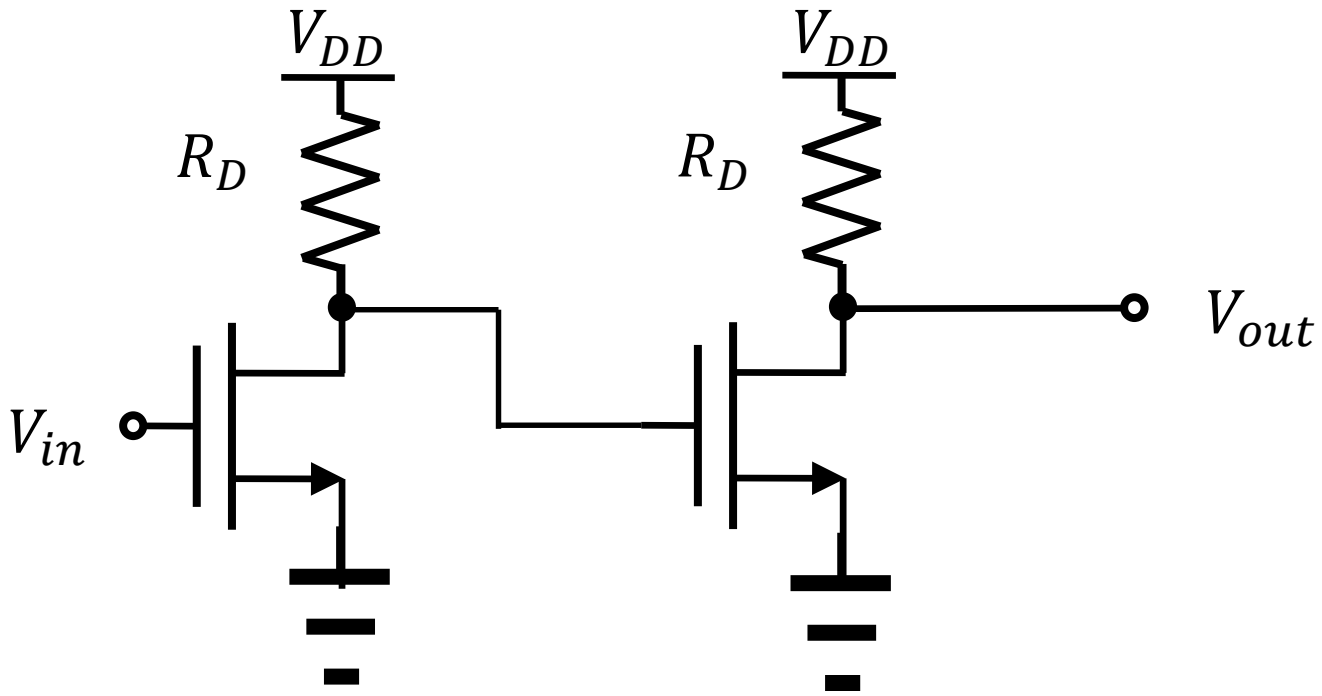
- A rapid transition of V_{in} from 0 to V_{DD} to 0
  - At the initial phase, the resistor does not conduct.
  - Also the MOSFET is operated in its saturation mode. Then,

$$I_{D,sat} + C_L \frac{dV_{out}}{dt} = 0$$



Origin of C_L?

- Consider an inverter chain.
  - Then, what is the load capacitance for the first stage?



- Interconnect