HW#10, Electronic Circuit, Spring semester 2020

June 7, 2020

Due: 23:55, June 12 (Friday night)

We have 10 problems.

In your answer file, specify both the **SOLUTION PROCEDURE** and the **FINAL SOLUTION**.

1. Calculate the small-signal voltage gain of a common-source amplifier with a correct sign. The threshold voltage of the transistor is 0.4 V. $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$. Its width is ten-times wider than its length. Neglect the channel-length modulation. Also, let $V_{DD} = 1.8\ \text{V}$, $R_D = 17.5\ k\Omega$, and $V_{GS} = 0.6\ \text{V}$.

2. Calculate the dc power dissipation of the common-source amplifier in the Problem #1.

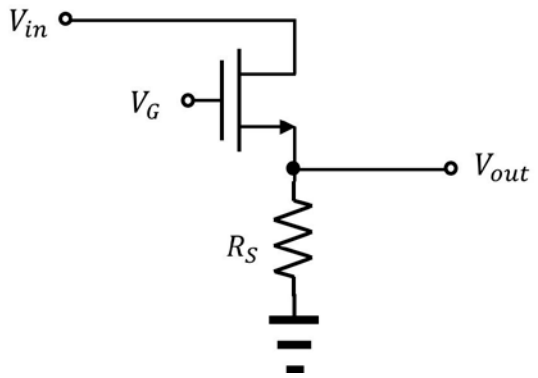
3. Consider the amplifier in the Problem #1. Estimate the maximum amplitude of a sinusoidal small-signal gate voltage to keep the MOSFET in the saturation region.

4. Calculate the (time-averaged) ac power dissipation by R_D in the Problem #1. Use the small-signal amplitude of the gate voltage, which is obtained in the Problem #3.

5. A common-gate amplifier using an NMOS transistor for which $g_m = 4\ \text{mA/V}$ has a $5\ \text{k}\Omega$ drain resistance and a $5\ \text{k}\Omega$ load resistance. (Neglect the channel-length modulation.) The amplifier is driven by a voltage source having a $500\ \Omega$ resistance. What is the overall voltage gain? Note that the input signal voltage is different from the source terminal voltage in this problem.

6. Design a source follower. The output resistance of the source follower should be $200\ \Omega$. The MOSFET has $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$ and is operated at $V_{GS} - V_{TH} = 0.25\ \text{V}$. Find the required W/L ratio. Also specify the dc bias current.

7. In the lecture, we didn't consider a circuit topology wherein the input is applied to the drain and the output is sensed at the source. In this problem, we consider such a circuit topology. V_G is constant. Assume that the MOSFET has an output resistance of r_O. Also the transconductance is denoted as g_m. Express the voltage gain in terms of g_m, r_O, and R_s.



8. Calculate the input and output impedances of the circuit in the Problem #7.

9. Design an NMOS inverter. The power supply $\mathrm{V_{DD}} = 2.5\ \mathrm{V}$. When the input voltage is V_{DD}, the output voltage is 0.1 V and the current is 50 μA. Let the transistor be specified to have V_{TH} = 0.5 V and $\mu_n C_{ox} = 125\ \mu\mathrm{A/V^2}$. Neglect the channel-length modulation. Specify the required values of *W*/*L* and R_D.

10. Consider the NMOS inverter in the Problem #9. A load capacitor is 45 fF. Initially, the input voltage is V_{DD}. At t=0, the input voltage suddenly becomes 0 V. Calculate the time required for the output voltage to be 1.3 V.