Pragmatic

Design Rules Manual

Helvellyn 2.1.0

16th March 2023

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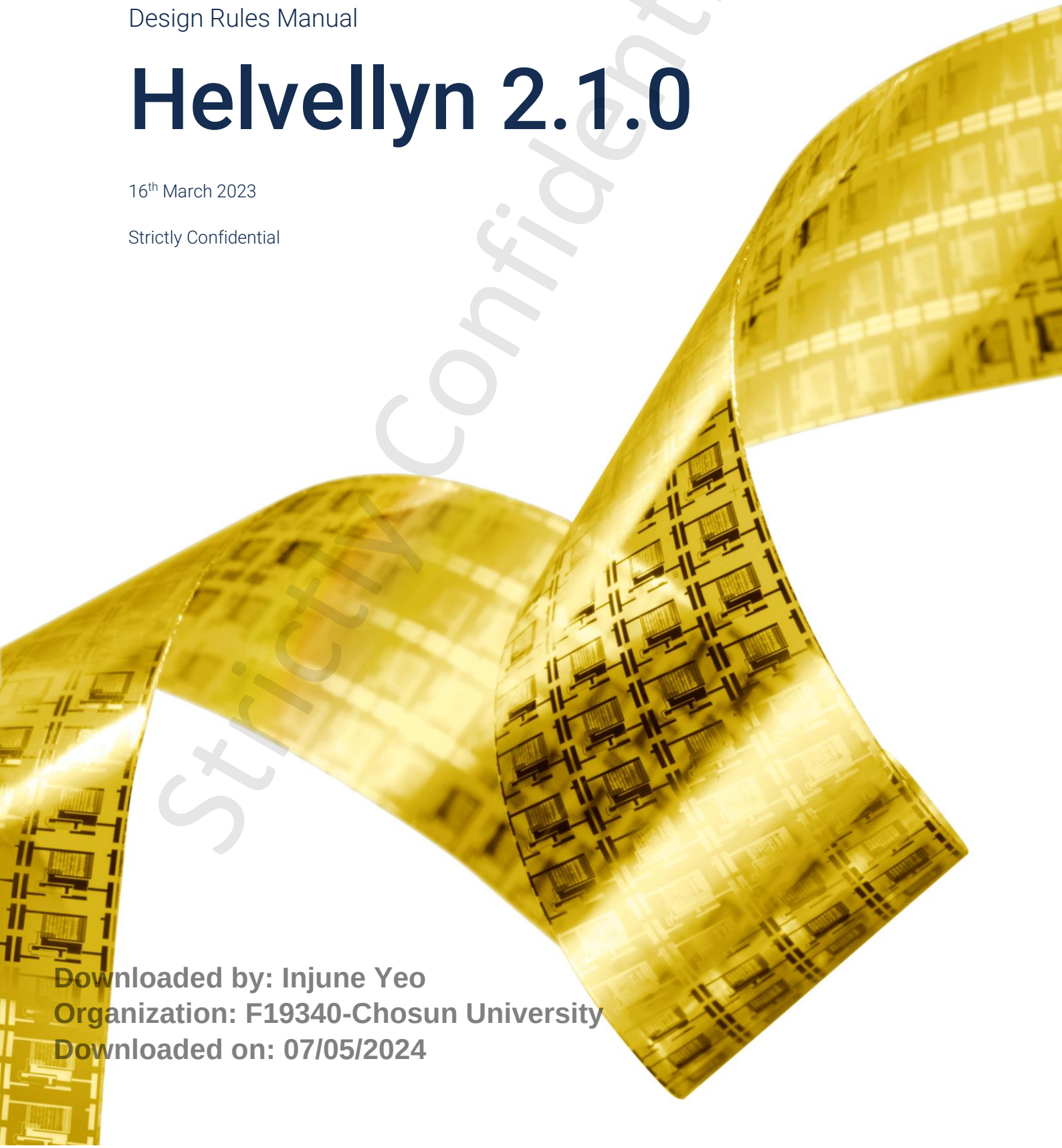

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1 Introduction

This Design Rules Manual (DRM) defines the rules and guidelines for physical design in Pragmatic's Helvellyn FlexIC Foundry process technology. This is a release of Helvellyn 2.1.0. beta.2.

1.1 Definition of terms

In this document the following terms are used to describe the guidelines, the table below defines how they are to be interpreted:

Term	Interpretation
MUST	Not following this guidance will cause the design to fail the DRC check and the circuit will not be accepted for production
RECOMMENDED (W)	The designer is recommended to follow this guidance. If these are not met, they will be flagged by the DRC check and a discussion will be needed with your Pragmatic representative.
BEST PRACTICE	This is an example of best practice, but it is not checked by the DRC

Table 1: How to interpret these guidelines

1.2 General rules

- Only orthogonal or 45° lines are allowed
- Acute angles are forbidden
- The database must utilise a resolution of 25nm

1.3 Layer names

The table below describes the FlexIC GDSII layer names. All GDSII layers are datatype=0. Note that the non-physical identification layers are not directly used for mask fabrication.

Layer/purpose	Layer name	Description	GDSII number
SD/drw	Source & drain	First metallisation layer, used to form TFT source and drain electrodes.	1
RES/drw	Resistor	Oxide semiconductor islands forming the active area for high value resistors.	802
SEMI/drw	Semiconductor	Oxide semiconductor islands forming the active area for transistors.	2
CONT/drw	Contact	Contact via formed through the gate dielectric connecting SD to GATE.	3
GATE/drw	Gate	Gate metallisation layer.	4
VIA1/drw	Via 1	Via formed through the inter-metal-dielectric-1 layer (IMD1) between GATE and MT1.	6
MT1/drw	Metal tracking 1	First interconnect layer.	7
VIA2/drw	Via 2	Via formed through the inter-metal-dielectric-2 layer (IMD2) between MT1 and MT2.	8
MT2/drw	Metal tracking 2	Second interconnect layer and probe pad formation.	9
RV/drw	Redistribution VIA	Via formed through the final passivation layer	10
RDL/drw	Redistribution	Metal layer over the FlexIC.	15
SDTEXT/drw	SD text	SD layer used only for text labels	101
RESTEXT/drw	RES text	RES layer used only for text labels	852
SEMITEXT/drw	SEMI text	SEMI layer used only for text labels	102
CONTTEXT/drw	CONT text	CONT layer used only for text labels	103
GATETEXT/drw	GATE text	GATE layer used only for text labels	104
VIA1TEXT/drw	VIA1 text	VIA1 layer used only for text labels	106
MT1TEXT/drw	MT1 text	MT1 layer used only for text labels	107

Layer/purpose	Layer name	Description	GDSII number
VIA2TEXT/drw	VIA2 text	VIA2 layer used only for text labels	108
MT2TEXT/drw	MT2 text	MT2 layer used only for text labels	109
RVTEXT/drw	RV text	RV layer used only for text labels	110
RDLTEXT/drw	RDL text	RDL layer used only for text labels	115
FILLSD/fill	SD fill	SD layer only for fill, reserved for use by Pragmatic	401
FILLRES/fill	RES fill	RES layer only for fill, reserved for use by Pragmatic	812
FILLSEMI/fill	SEMI fill	SEMI layer only for fill, reserved for use by Pragmatic	402
FILLCONT/fill	CONT fill	CONT layer only for fill, reserved for use by Pragmatic	403
FILLGATE/fill	GATE fill	GATE layer only for fill, reserved for use by Pragmatic	404
FILLVIA1/fill	VIA1 fill	VIA1 layer only for fill, reserved for use by Pragmatic	406
FILLMT1/fill	MT1 fill	MT1 layer only for fill, reserved for use by Pragmatic	407
FILLVIA2/fill	VIA2 fill	VIA2 layer only for fill, reserved for use by Pragmatic	408
FILLMT2/fill	MT2 fill	MT2 layer only for fill, reserved for use by Pragmatic	409
FILLRV/fill	RV fill	RV layer only for fill, reserved for use by Pragmatic	410
FILLRDL/fill	RDL fill	RDL layer only for fill, reserved for use by Pragmatic	415
NOFILLSD/blockage	SD fill exclusion	Non-physical identification layer that prevents Pragmatic SD fill algorithm, reserved for use by Pragmatic	441
NOFILLRES/blockage	RES fill exclusion	Non-physical identification layer that prevents Pragmatic RES fill algorithm, reserved for use by Pragmatic	842
NOFILLSEMI/blockage	SEMI fill exclusion	Non-physical identification layer that prevents Pragmatic SEMI fill algorithm, reserved for use by Pragmatic	442

Layer/purpose	Layer name	Description	GDSII number
NOFILLCONT/blockage	CONT fill exclusion	Non-physical identification layer that prevents Pragmatic CONT fill algorithm, reserved for use by Pragmatic	443
NOFILLGATE/blockage	GATE fill exclusion	Non-physical identification layer that prevents Pragmatic GATE fill algorithm, reserved for use by Pragmatic	444
NOFILLVIA1/blockage	VIA1 fill exclusion	Non-physical identification layer that prevents Pragmatic VIA1 fill algorithm, reserved for use by Pragmatic	446
NOFILLMT1/blockage	MT1 fill exclusion	Non-physical identification layer that prevents Pragmatic MT1 fill algorithm, reserved for use by Pragmatic	447
NOFILLVIA2/blockage	VIA2 fill exclusion	Non-physical identification layer that prevents Pragmatic VIA2 fill algorithm, reserved for use by Pragmatic	448
NOFILLMT2/blockage	MT2 fill exclusion	Non-physical identification layer that prevents Pragmatic MT2 fill algorithm, reserved for use by Pragmatic	449
NOFILLRV/blockage	RV fill exclusion	Non-physical identification layer that prevents Pragmatic RV fill algorithm, reserved for use by Pragmatic	450
NOFILLRDL/blockage	RDL fill exclusion	Non-physical identification layer that prevents Pragmatic RDL fill algorithm, reserved for use by Pragmatic	455
NOSD/blockage	SD exclusion	Non-physical identification layer for SD, SDTEXT exclusion. FILLSD is allowed, reserved for use by Pragmatic.	501
NOGATE/blockage	GATE exclusion	Non-physical identification layer for GATE, GATETEXT exclusion. FILLGATE is allowed, reserved for use by Pragmatic.	504
NOMT1/blockage	MT1 exclusion	Non-physical identification layer for MT1, MT1TEXT exclusion. FILLMT1 is allowed, reserved for use by Pragmatic.	507
NOMT2/blockage	MT2 exclusion	Non-physical identification layer for MT2, MT2TEXT exclusion. FILLMT2 is allowed, reserved for use by Pragmatic.	509
NORDL/blockage	RDL exclusion	Non-physical identification layer for RDL, RDLTEXT exclusion. FILLRDL is allowed, reserved for use by Pragmatic.	515

Layer/purpose	Layer name	Description	GDSII number
CAPID/drw	Capacitor	Non-physical identification layer defining SD-GATE capacitor structures.	120
CAPID2/drw	Capacitor 2	Non-physical identification layer defining metal capacitor structures except SD-GATE	128
RESIDSD/drw	SD resistor	Non-physical identification layer defining SD resistor structures.	122
RESIDGATE/drw	GATE resistor	Non-physical identification layer defining GATE resistor structures.	124
RESIDMT1/drw	MT1 resistor	Non-physical identification layer defining MT1 resistor structures.	125
RESIDMT2/drw	MT2 resistor	Non-physical identification layer defining MT2 resistor structures.	126
RESIDRDL/drw	RDL resistor	Non-physical identification layer defining RDL resistor structures.	127
DICE/drw	Dicing	Non-physical identification layer defining dice lines.	130
LFUSEID/drw	Laser fuse ID	Non-physical identification layer defining area for laser fuses	123
LFUSEALIGNID/drw	Laser fuse alignment ID	Non-physical identification layer defining area of laser alignment marks	129
LFUSEALIGNMT2/drw	Laser fuse alignment MT2	MT2 layer used for laser alignment marks	559
RBOUND/drw	Reticle boundary	Non-physical identification layer defining the limits of the reticle available for circuit design. (Pragmatic use only.)	131
BOUND/bnd	Boundary	Reserved for use by Pragmatic	0
BULK/ drw	Bulk	Reserved for use by Pragmatic	800
Reserved for customer use: 30-39, 300-399. All other layers cannot be used.			

Table 2: Layer names

1.4 Layer mapping file

The layer mapping file, that translates to or from GDSII layers, is supplied as part of the PDK. This layer mapping file, *pragLib.layermap*, is found in the PDK installation in the *cdslib/pragLib* folder.

In the default installation, the layer mapping file is automatically used. However, if not using the default set-up, ensure that the GDSII translations reference the correct layer mapping file before submitting to Pragmatic.

1.5 Pins for calibre verification

The Pragmatic Calibre Layout Versus Schematic (LVS) verification deck expects pins or ports for LVS purposes. With the Pragmatic PDK, these should be created as labels on the corresponding layer and purpose pair, i.e., SD/drw, GATE/drw, MT1/drw, MT2/drw, etc.

1.6 Layout terminology

Parameter	Meaning
Minimum width	Specifies the minimum width of all objects on the named layer
Exact size	Specifies the exact size of all shapes on the named layer
Not allowed	Specifies that no objects should exist on the named layer
Spacing	Specifies the minimum distance between pairs of objects on the same or two different layers
Surround	Specifies that objects on one layer must be completely surrounded by objects on another layer
Overlap	Specifies the minimum amount that the objects on one layer must overlap an object on another layer (inside edge to inside edge)
Extension	Specifies the minimum distance that objects on one layer must extend beyond the edge of an object on another layer (outside edge to inside edge)

Table 3: Terminology

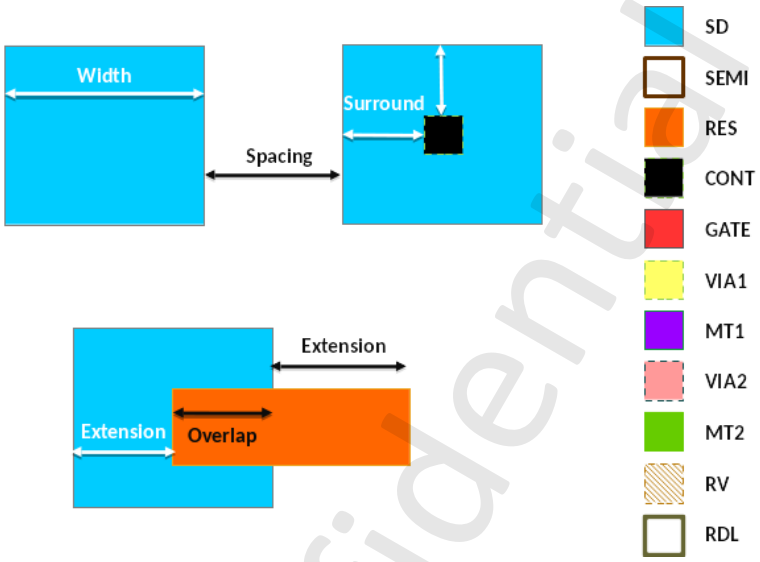

Figure 1:Terminology and layer representation

2 Layer rules

2.1 High value resistors (RES)

This set of rules is used to design high value resistors. RESTEXT is the same physical layer as RES but is used only for text and labels. FILLRES and NOFILLRES are reserved for use by Pragmatic.

Rule	Description	Value (µm)
RES.2	Minimum spacing	1.4
RES.3	Minimum SD overlap of RES	1.0
RES.4	Minimum SD extension beyond RES	1.0
RES.5	Minimum SD spacing to RES	0.5
RES.6	Minimum width	1.4
RES.7	Maximum width	75.0
RES.8	Minimum length	3.0
RES.9	Maximum length	120.0
RESTEXT.1	Minimum spacing to any layer	3.0
RESTEXT.2	RESTEXT not allowed on any layer	
FILLRES.1	Unauthorised use of FILLRES	
NOFILLRES.1	Unauthorised use of NOFILLRES	

Table 4: High value resistor rules

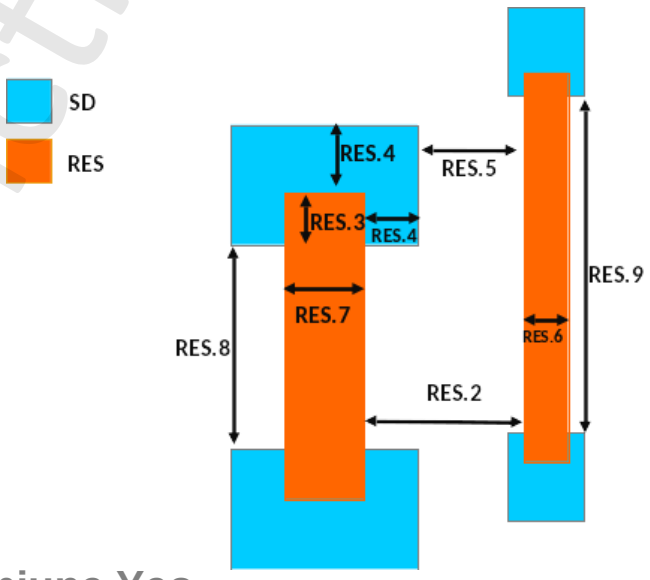

Figure 2: High value resistor rules

2.2 Semiconductor (SEMI)

This set of rules is used for isolated semiconductor islands that define the transistor width and forms the transistor channel. SEMITEXT is the same physical layer as SEMI but is used only for text and labels. FILLSEMI and NOFILLSEMI are reserved for use by Pragmatic.

Rule	Description	Value (µm)
SEMI.1	Minimum width	1.6
SEMI.2	Minimum spacing	2.0
SEMI.3	Minimum SEMI overlap of SD	0.5
SEMI.4	Minimum SD spacing to SEMI	0.5
SEMI.5	Minimum SD extension beyond SEMI in width	0.2
SEMI.6	Minimum RES spacing to SEMI	3.0
SEMI.7	Minimum transistor channel width	2.0
SEMI.8	Maximum transistor channel width	20.0
SEMI.9	Maximum transistor channel length	5.0
SEMITEXT.1	Minimum spacing to any layer	3.0
SEMITEXT.2	SEMITEXT not allowed on any layer	
FILLSEMI.1	Unauthorised use of FILLSEMI	
NOFILLSEMI.1	Unauthorised use of NOFILLSEMI	

Table 5: Semiconductor rules

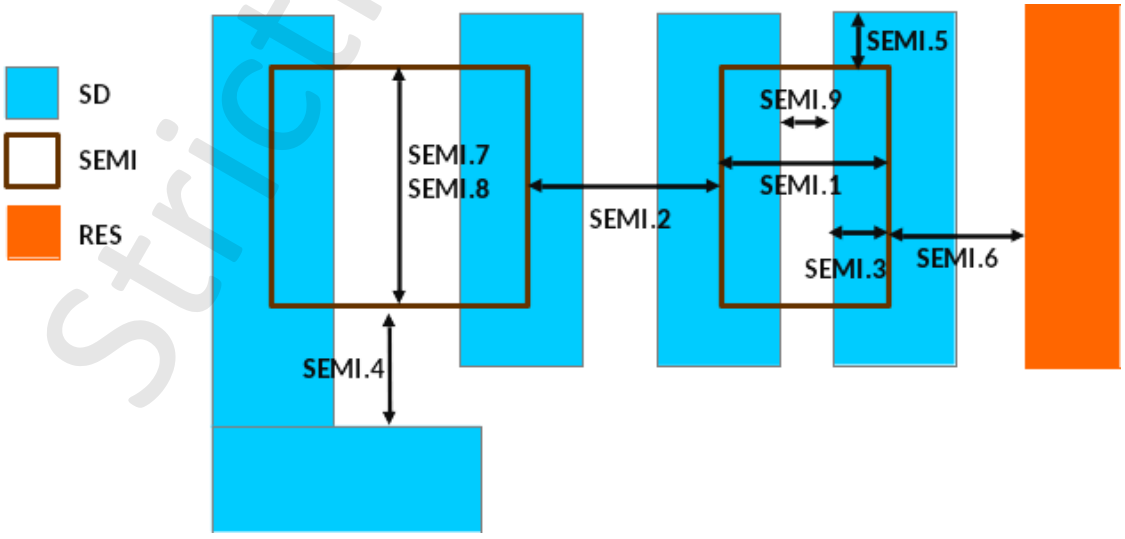

Figure 3: Semiconductor rules

2.3 Source & drain (SD)

Used for TFT source and drain, high value resistor electrodes, short interconnects, and horizontal cell power rails. SDTEXT is the same physical layer as SD but is used only for text and labels. Rules marked 'W' are related to Design for Manufacture (DfM) considerations and are more fully described in the Design Guide (DG). FILLSD, NOFILLSD and NOSD are reserved for use by Pragmatic.

Rule	Description	Value (µm)
SD.1	Minimum width	2.0
SD.2	Minimum spacing (TFT channel)	0.6
SD.3	Minimum spacing (routing)	2.0
SD.4	Maximum length of SD at minimum width	200.0
SD.5	Minimum width for long lines ≥ [SD.4]	4.0
SD.6W	Minimum spacing for width ≥ 30µm	6.0
SD.7W	Connecting to probe or bond pad at minimum width SD	Not recommended
SDTEXT.1	Minimum spacing to any layer	3.0
SDTEXT.2	SDTEXT not allowed on any layer	
FILLSD.1	Unauthorised use of FILLSD	
NOFILLSD.1	Unauthorised use of NOFILLSD	
NOFILLSD.2	FILLSD not allowed on NOFILLSD	
NOSD.1	Unauthorised use of NOSD	
NOSD.2	SD, SDTEXT not allowed on NOSD	

Table 6: Source & drain rules

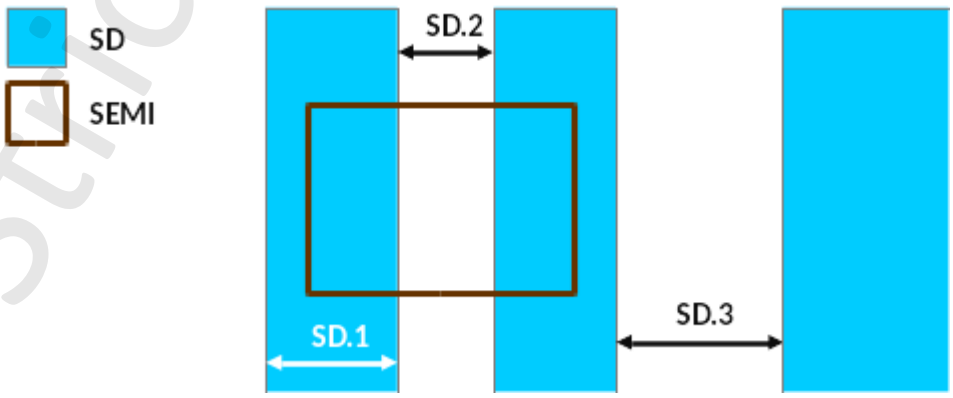

Figure 4: Source & drain rules

2.4 Contact (CONT)

Used for opening contact vias from GATE to SD in the TFT gate dielectric. CONTTEXT is the same physical layer as CONT but is used only for text and labels. FILLCONT and NOFILLCONT are reserved for use by Pragmatic.

Rule	Description	Value (µm)
CONT.1	Exact size	1.0 x 1.0
CONT.2	Minimum spacing between CONT contact vias	1.0
CONT.3	Minimum SD surrounding CONT contact via	0.5
CONT.4W	Single CONT connection. Multiple contacts are recommended.	
CONTTEXT.1	Minimum spacing to any layer	3.0
CONTTEXT.2	CONTTEXT not allowed on any layer	
FILLCONT.1	Unauthorised use of FILLCONT	
NOFILLCONT.1	Unauthorised use of NOFILLCONT	
NOFILLCONT.2	FILLCONT not allowed on NOFILLCONT	

Table 7: Contact rules

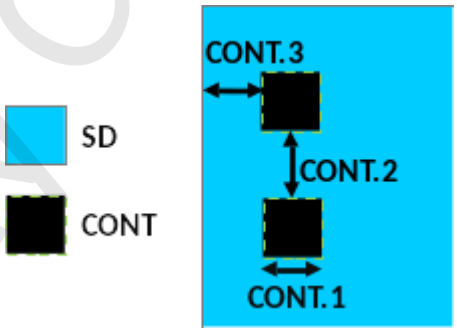

Figure 5: Contact rules

2.5 Gate (GATE)

Used for TFT gate, routing, and vertical power straps. GATETEXT is the same physical layer as GATE but is used only for text and labels. Rules marked 'W' are related to Design for Manufacture (DfM) considerations and are described further in the Design Guide (DG). FILLGATE, NOFILLGATE and NOGATE are reserved for use by Pragmatic.

Rule	Description	Value (µm)
GATE.1	Minimum width (outside transistor)	2.0
GATE.2	Minimum spacing	3.0
GATE.3	Minimum GATE extension beyond TFT channel length	0.075
GATE.4	Minimum GATE extension beyond TFT channel width	0.5
GATE.5	Minimum GATE spacing to RES	0.5
GATE.6	Minimum GATE spacing to SEMI	0.5
GATE.7	Minimum GATE surrounding CONT	0.5
GATE.8	GATE not allowed on RES	
GATE.9	Minimum width (inside transistor)	0.75
GATE.10	Maximum length of GATE at minimum width GATE.9 outside transistor SEMI region	2.0
GATE.11	Maximum length of GATE at minimum width [GATE.1]	200.0
GATE.12	Minimum width for long lines ≥[GATE.11]	4.0
GATE.16W	Minimum spacing for width ≥ 30µm	6.0
GATE.17W	Connecting to probe or bond pad at minimum width GATE [GATE.1]	Not recommended
GATE.18W	Maximum length between CONT or VIA1 pinning	750.0
GATETEXT.1	Minimum spacing to any layer	3.0
GATETEXT.2	GATETEXT not allowed on any layer	
FILLGATE.1	Unauthorised use of FILLGATE	
NOFILLGATE.1	Unauthorised use of NOFILLGATE	
NOFILLGATE.2	FILLGATE not allowed on NOFILLGATE	
NOGATE.1	Unauthorised use of NOGATE	
NOGATE.2	GATE, GATETEXT not allowed on NOGATE	

Table 8: Gate rules

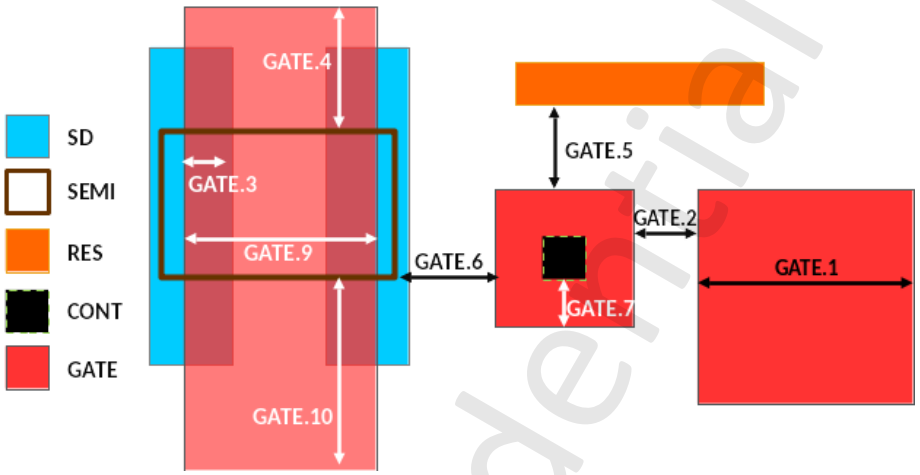

Figure 6: Gate rules

2.6 Via 1 (VIA1)

Used for the formation of vias in the IMD1 layer, allowing the connection of MT1 to GATE. VIA1TEXT is the same physical layer as VIA1 but is used only for text and labels. FILLVIA1 and NOFILLVIA1 are reserved for use by Pragmatic.

Rule	Description	Value (µm)
VIA1.1	Exact size	1.5 x 1.5
VIA1.2	Minimum spacing between VIA1 vias	1.5
VIA1.3	Minimum GATE surrounding VIA1 via	0.75
VIA1.4	Minimum spacing between VIA1 and SEMI	3.0
VIA1.5	Minimum spacing between VIA1 and RES	3.0
VIA1.7	VIA1 via not allowed on SD edge	
VIA1.8	Minimum spacing between VIA1 and SD edge	1.0
VIA1.9	Stacked CONT-VIA1 must be centred	
VIA1.10W	Single VIA1 connection. Multiple vias are recommended.	
VIA1TEXT.1	Minimum spacing to any layer	3.0
VIA1TEXT.2	VIA1TEXT not allowed on any layer	
FILLVIA1.1	Unauthorised use of FILLVIA1	
NOFILLVIA1.1	Unauthorised use of NOFILLVIA1	
NOFILLVIA1.2	FILLVIA1 not allowed on NOFILLVIA1	

Table 9: Via1 rules

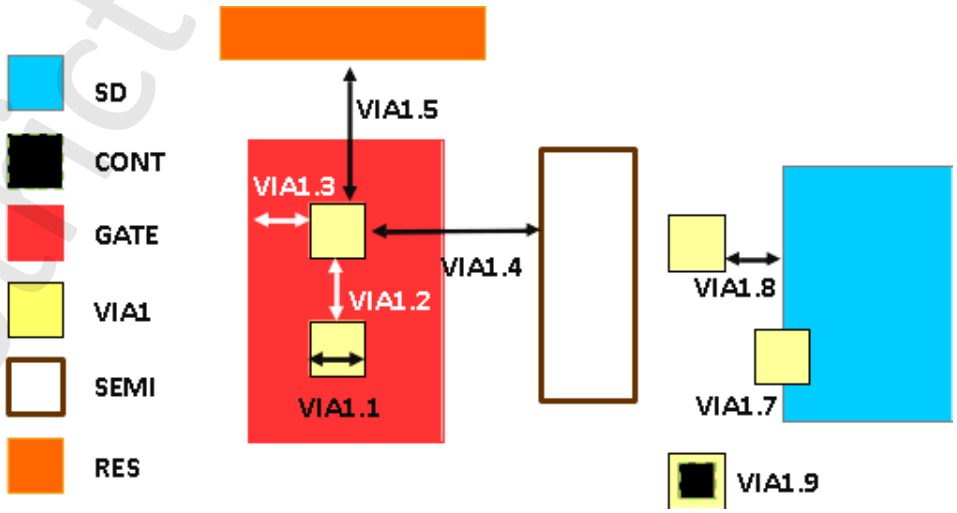

Figure 7: Via1 rules

2.7 Metal tracking 1 (MT1)

Used for routing. MT1TEXT is the same physical layer as MT1 but is used only for text and labels. Rules marked 'W' are related to Design for Manufacture (DfM) considerations and are described in detail in the Design Guide (DG). FILLMT1, NOFILLMT1 and NOMT1 are reserved for use by Pragmatic.

Rule	Description	Value (µm)
MT1.1	Minimum width	3.0
MT1.1W	Minimum preferred width	4.0
MT1.2	Minimum spacing	2.0
MT1.3	Minimum MT1 surrounding VIA1	1.0
MT1.4	Maximum length of MT1 at minimum width	100.0
MT1.5	Minimum width for long lines ≥ [MT1.4]	4.0
MT1.6W	Minimum spacing for width ≥30µm	6.0
MT1.7W	Connecting to probe or bond pad at minimum width MT1	Not recommended
MT1.8W	Maximum length between VIA1 or VIA2 pinning	750.0
MT1TEXT.1	Minimum spacing to any layer	3.0
MT1TEXT.2	MT1TEXT not allowed on any layer	
FILLMT1.1	Unauthorised use of FILLMT1	
NOFILLMT1.1	Unauthorised use of NOFILLMT1	
NOFILLMT1.2	FILLMT1 not allowed on NOFILLMT1	
NOMT1.1	Unauthorised use of NOMT1	
NOMT1.2	MT1, MT1TEXT not allowed on NOMT1	

Table 10: MT1 rules

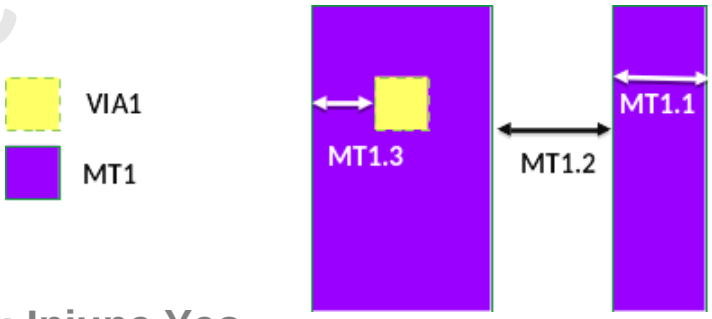

Figure 8: MT1 rules

2.8 Via 2 (VIA2)

Used for the formation of vias in the IMD2 layer, allowing the connection of MT2 to MT1. VIA2TEXT is the same physical layer as VIA2 but is used only for text and labels. FILLVIA2 and NOFILLVIA2 are reserved for use by Pragmatic.

Rule	Description	Value (µm)
VIA2.1	Exact minimum size not stacked on VIA1 Exact maximum size not stacked on VIA1	1.5 x 1.5 2.0 x 2.0
VIA2.2	Minimum spacing between VIA2 vias	1.5
VIA2.3	Minimum MT1 surrounding VIA2 via	1.0
VIA2.4	Minimum VIA2 via spacing to VIA1 via (not stacked on VIA1)	2.0
VIA2.7	Exact size stacked on VIA1	2.0 x 2.0
VIA2.9	Stacked VIA1-VIA2 must be centred	
VIA2.10W	Single VIA2 connection. Multiple vias are recommended.	
VIA2TEXT.1	Minimum spacing to any layer	3.0
VIA2TEXT.2	VIA2TEXT not allowed on any layer	
FILLVIA2.1	Unauthorised use of FILLVIA2	
NOFILLVIA2.1	Unauthorised use of NOFILLVIA2	
NOFILLVIA2.2	FILLVIA2 not allowed on NOFILLVIA2	

Table 11: Via2 rules

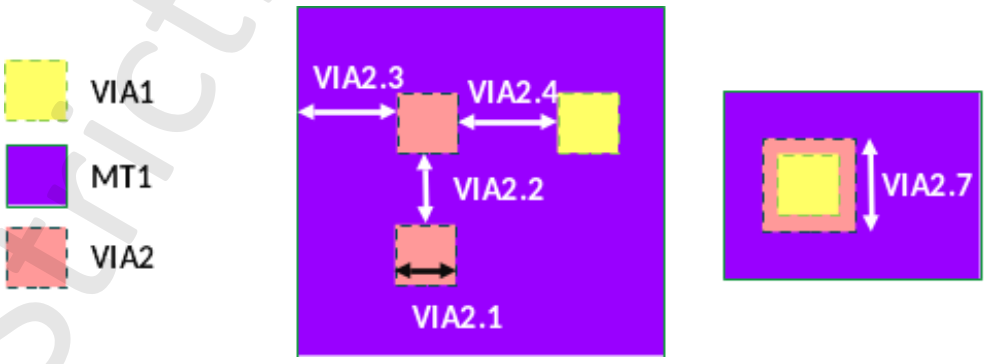

Figure 9: Via2 rules

2.9 Metal tracking 2 (MT2)

Used for routing. MT2TEXT is the same physical layer as MT2 but is used only for text and labels. Rules marked 'W' are related to Design for Manufacture (DfM) considerations and are more fully described in the Design Guide (DG). FILLMT2, NOFILLMT2 and NOMT2 are reserved for use by Pragmatic.

Rule	Description	Value (µm)
MT2.1	Minimum width	3.0
MT2.1W	Minimum preferred width	4.0
MT2.2	Minimum spacing	2.0
MT2.3	Minimum MT2 surrounding VIA2	1.0
MT2.4	Maximum length of MT2 at minimum width	100.0
MT2.5	Minimum width for long lines ≥ [MT2.4]	4.0
MT2.6W	Minimum spacing for width ≥ 30µm	6.0
MT2.7W	Connecting to probe or bond pad at minimum width MT2	Not recommended
MT2.8W	Maximum length between VIA2 or RV pinning	750.0
MT2TEXT.1	Minimum spacing to any layer	3.0
MT2TEXT.2	MT2TEXT not allowed on any layer	
FILLMT2.1	Unauthorised use of FILLMT2	
NOFILLMT2.1	Unauthorised use of NOFILLMT2	
NOFILLMT2.2	FILLMT2 not allowed on NOFILLMT2	
NOMT2.1	Unauthorised use of NOMT2	
NOMT2.2	MT2, MT2TEXT not allowed on NOMT2	

Table 12: MT2 rules

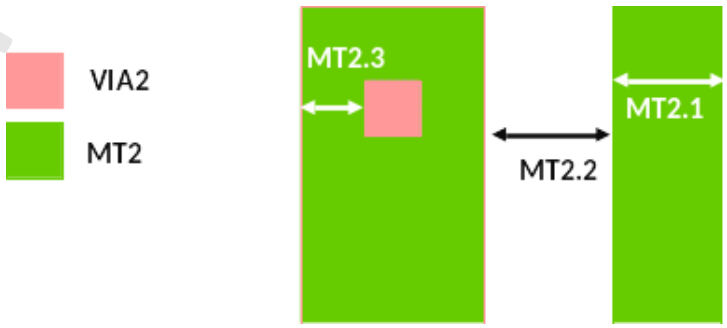

Figure 10: MT2 rules

2.10 Redistribution Via layer (RV)

The RV layer opens an aperture in the passivation layer allowing the connection of RDL to MT2. RVTEXT is the same physical layer as RV but is used only for text and labels. FILLRV and NOFILLRV are reserved for use by Pragmatic.

Rule	Description	Value (µm)
RV.1	Minimum size of RV	20.0 x 20.0
RV.2	Minimum spacing between RV	20.0
RV.3	Minimum MT2 surrounding RV	6.0
RVTEXT.1	Minimum spacing to any layer	3.0
RVTEXT.2	RVTEXT not allowed on any layer	
FILLRV.1	Unauthorised use of FILLRV	
NOFILLRV.1	Unauthorised use of NOFILLRV	
NOFILLRV.2	FILLRV not allowed on NOFILLRV	

Table 13: RV rules

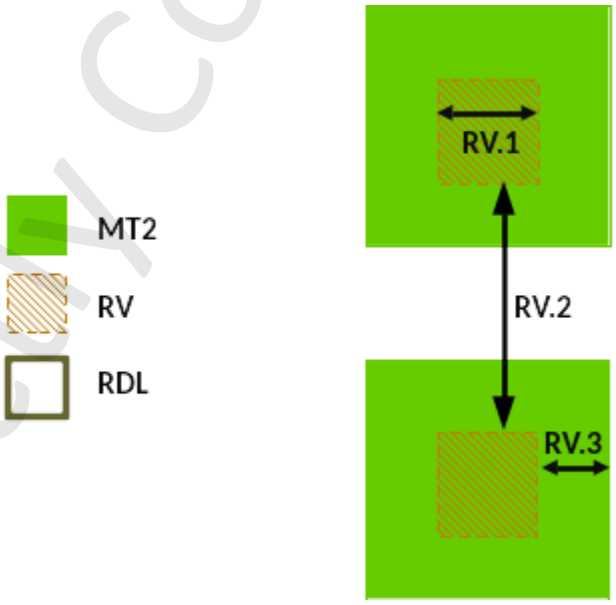

Figure 11: RV rules

2.11 Redistribution layer (RDL)

The RDL layer is an additional metal layer on the surface of the chip over the passivation whose primary use is in the formation of pads. RDLTEXT is the same physical layer as RDL but is used only for text and labels.

Rules marked 'W' are related to Design For Manufacture (DfM) considerations and are more fully described in the Design Guide (DG). FILLRDL and NOFILLRDL are reserved for use by Pragmatic.

Rule	Description	Value (µm)
RDL.1	Minimum width of RDL	30.0
RDL.2	Minimum spacing between RDL	6.0
RDL.3	Minimum RDL surrounding RV	12.0
RDL.4W	Maximum length between RV pinning	750.0
RDL.5	RDL not allowed on LFUSEID	
RDLTEXT.1	Minimum spacing to any layer	6.0
RDLTEXT.2	RDLTEXT not allowed on any layer	
FILLRDL.1	Unauthorised use of FILLRDL	
NOFILLRDL.1	Unauthorised use of NOFILLRDL	
NOFILLRDL.2	FILLRDL not allowed on NOFILLRDL	
NORDL.1	Unauthorised use of NORDL	
NORDL.2	RDL, RDLTEXT not allowed on NORDL	

Table 14: RDL rules

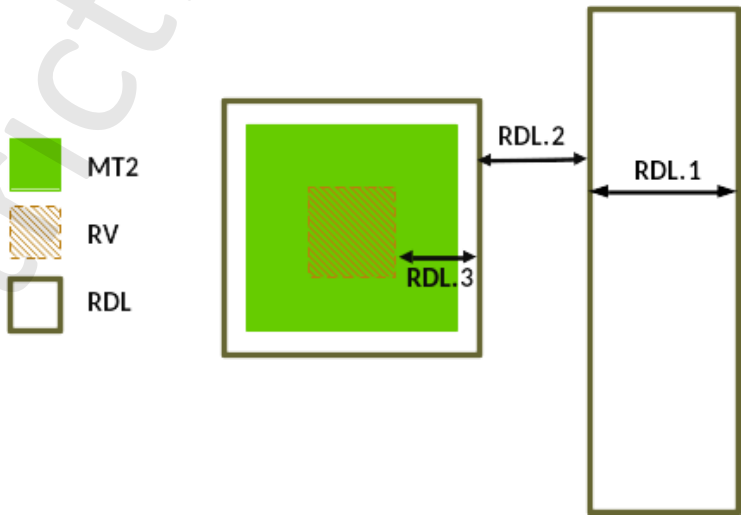

Figure 12: RDL rules

2.12 Dice layer (DICE)

This is an optional step if requesting Pragmatic wafer laser dicing. Other drawn layers are not allowed on the DICE layer due to potential damage from the laser itself.

For the use of other custom dicing solutions, please discuss with your Pragmatic technical representative.

Rule	Description	Value (µm)
DICE.1	Width of DICE line	100.0
DICE.2	Minimum DICE spacing to RV or layers touching RV	0.0
DICE.3	Minimum DICE spacing to layers not touching RV	50.0

Table 15: DICE rules

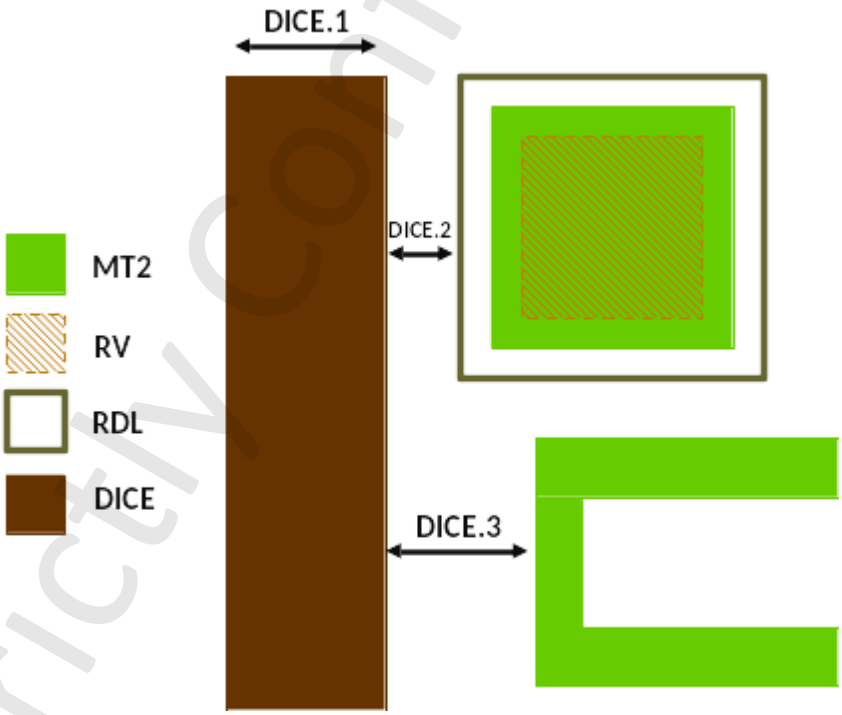

Figure 13: DICE rules

2.13 Metal resistor identification layers

RESIDSD, RESIDGATE, RESIDMT1, RESIDMT2, RESIDRD are non-physical identification layers to identify deliberate resistors in the metal layers SD, GATE, MT1, MT2, RDL respectively. The extracted metal resistor is the area within the relevant resistor ID layer. The intended use of these layers is covered in detail in the Design Guide.

Rule	Description
RESIDSD.1	RESIDSD must be inside SD
RESIDGATE.1	RESIDGATE must be inside GATE
RESIDMT1.1	RESIDMT1 must be inside MT1
RESIDMT2.1	RESIDMT2 must be inside MT2
RESIDRDL.1	RESIDRDL must be inside RDL

Table 16: Metal resistor ID

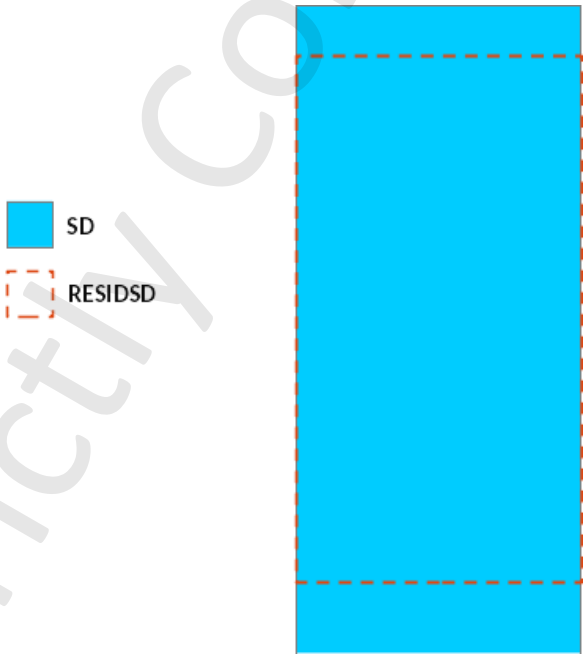

Figure 14: Metal resistor ID rules

2.14 Capacitor identification layers

CAPID and CAPID2 are non-physical identification layers to identify deliberate capacitors formed by the intersection of metal layers. CAPID is used to identify SD-GATE capacitors. CAPID2 will identify all other SD, GATE, MT1, MT2, RDL metal-metal capacitors. The CAPID and CAPID2 layers should completely surround all constituent parts of the capacitor including any routing.

Rule	Description	Value (µm)
CAPID.1	Minimum CAPID surrounding GATE	0.0
CAPID.2	Minimum SD surrounding GATE in CAPID	0.5

Table 17: CAPID rules

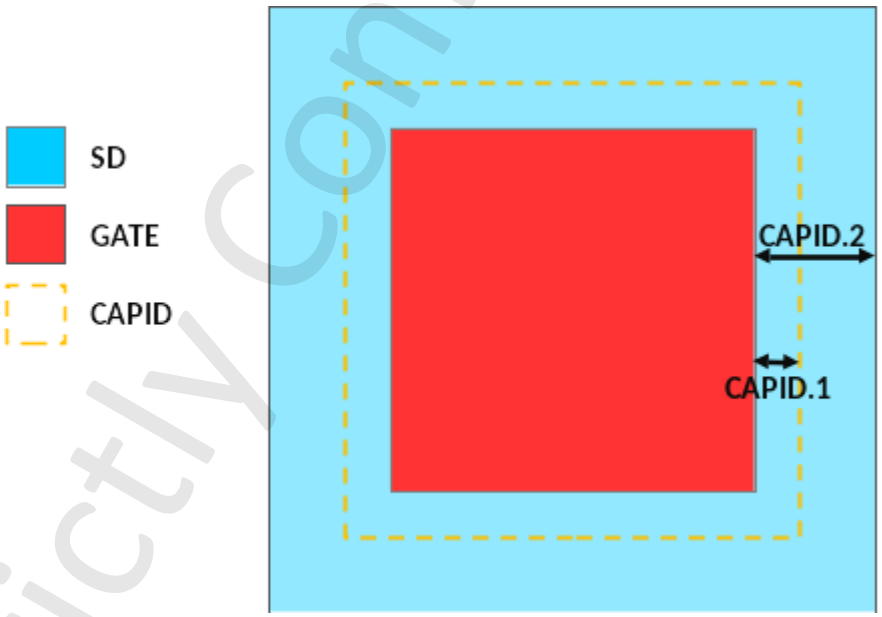

Figure 15: CAPID rules

2.15 Laser fuses (LFUSEID)

IMPORTANT NOTE: The following section is for informational purposes only. Use of the LFUSEID layer is not permitted unless discussed and agreed in advance with your Pragmatic representative. Access to LFUSE p-cells must be arranged through your Pragmatic representative.

This is an optional process step and available by request only in advance of use.

LFUSEID is a non-physical identification layer used to identify the location of MT2 laser fuses, typically used in programmable read-only memory, and the exclusion zone around the laser fuse. The LFUSEID area itself identifies the extent of the zone affected by the heat of the laser and therefore any structures within LFUSEID may be damaged by the programming laser.

In order to allow the laser system to locate the laser fuse, there must be an instance of *laser_fuse_1* p-cell from pragLib in the PDK. The origin of the *laser_fuse_1* p-cell is the target for the laser system (Figure 17). Also, the laser alignment p-cell must be placed near the laser fuses (Figure 18). The laser fuse alignment is available as *laser_fuse_alignment* from pragLib in the PDK.

Rule	Description	Value (µm)
LFUSEID.1	Exact length of MT2 laser fuse within LFUSEID area	16
LFUSEID.2	Exact width of MT2 laser fuse within LFUSEID area	2
LFUSEID.3	Exact size of LFUSEID parallel to laser travel, perpendicular to fuse	13
LFUSEID.4	Exact size of LFUSEID perpendicular to laser travel, parallel to fuse	16
LFUSEID.5	Minimum LFUSEID extension beyond MT2 laser fuse width	5.5
LFUSEID.6W	Only MT2 laser fuse is allowed in LFUSEID area	
LT.1	Laser alignment target LFUSEALIGNMT2 short dimension	6
LT.2	Laser alignment target LFUSEALIGNMT2 long dimension	22
LT.3	LFUSEALIGNID extension beyond LFUSEALIGNMT2 long-edge	27
LT.4	LFUSEALIGNID extension beyond LFUSEALIGNMT2 short-edge	0
LT.5	Maximum rectilinear distance of LFUSEALIGNMT2 to MT2 laser fuse	2000
LT.6	Only LFUSEALIGNMT2 is allowed in LFUSEALIGNID laser alignment target area.	
LT.7	Minimum LFUSEALIGNID spacing to any layer	3

Table 18: Laser fuse rules

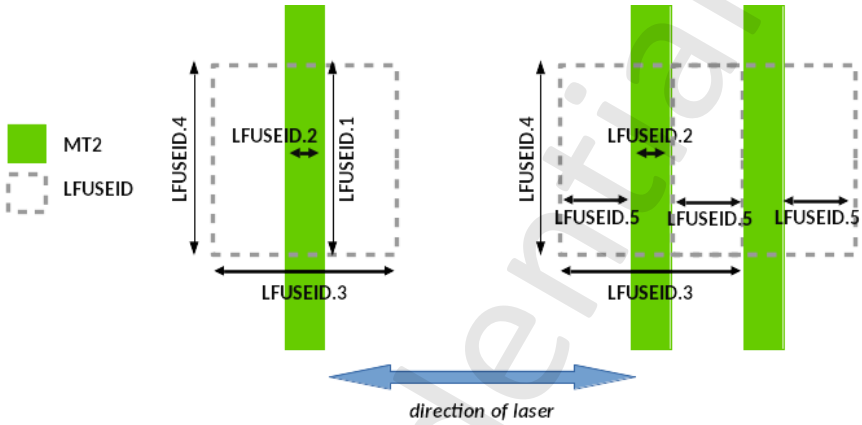

Figure 16: Laser fuses

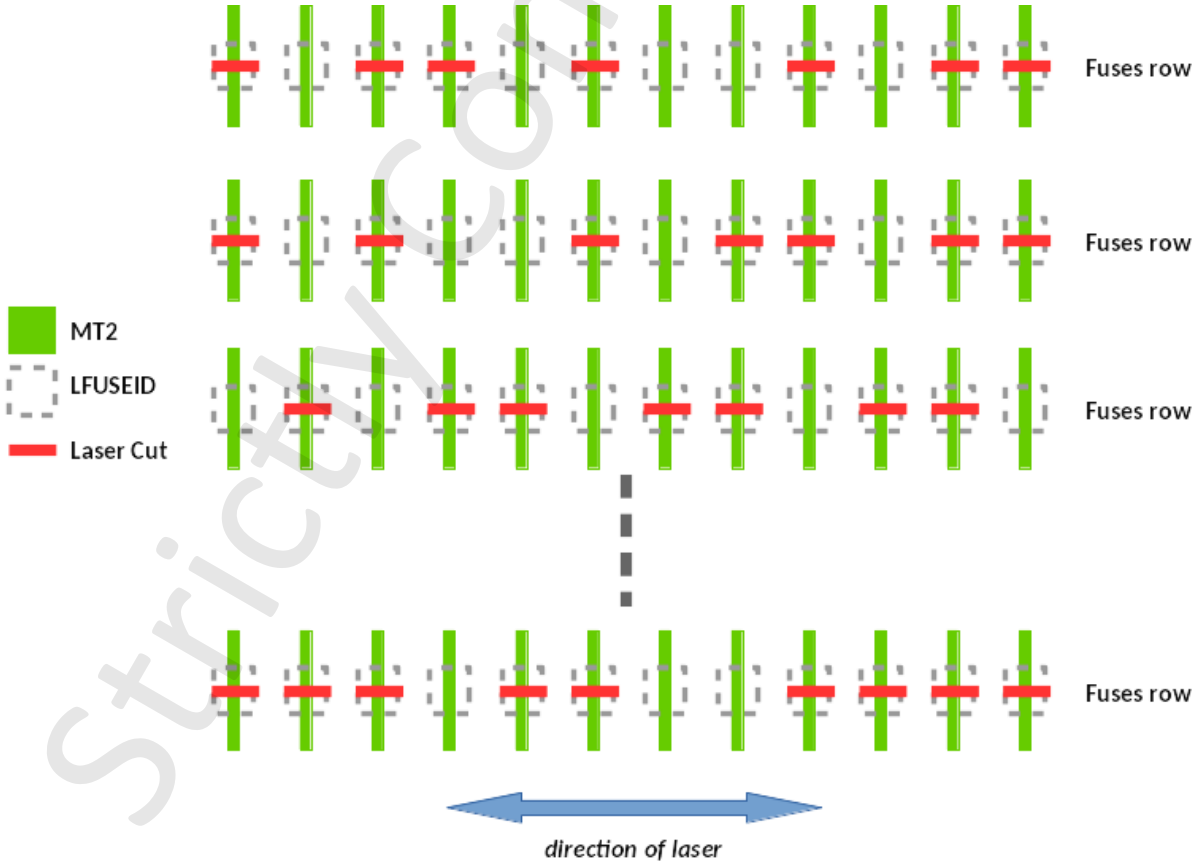

Figure 17: Laser fuse rows

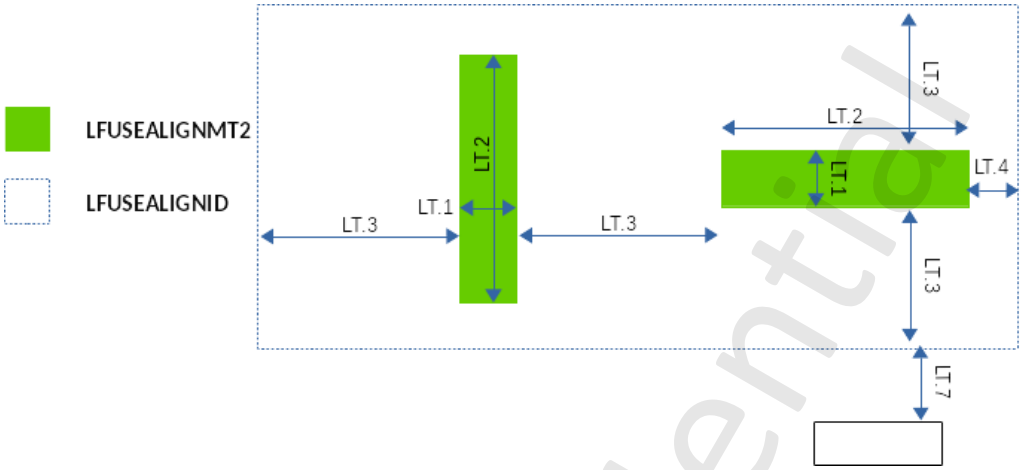

Figure 18 : Laser target alignment mark

2.16 Reticle Boundary (RBOUND)

The RBOUND layer defines the limits for drawn data when designing a reticle and is 100µm wide around the perimeter of the reticle

The cell *Core_Outline_22x21* is provided in the *lib_common* library as a suitable template for designers to use.

Rule	Description	Value (µm)
RBOUND.1	Other layers (except DICE) are not allowed in RBOUND	

Table 19: Reticle boundary

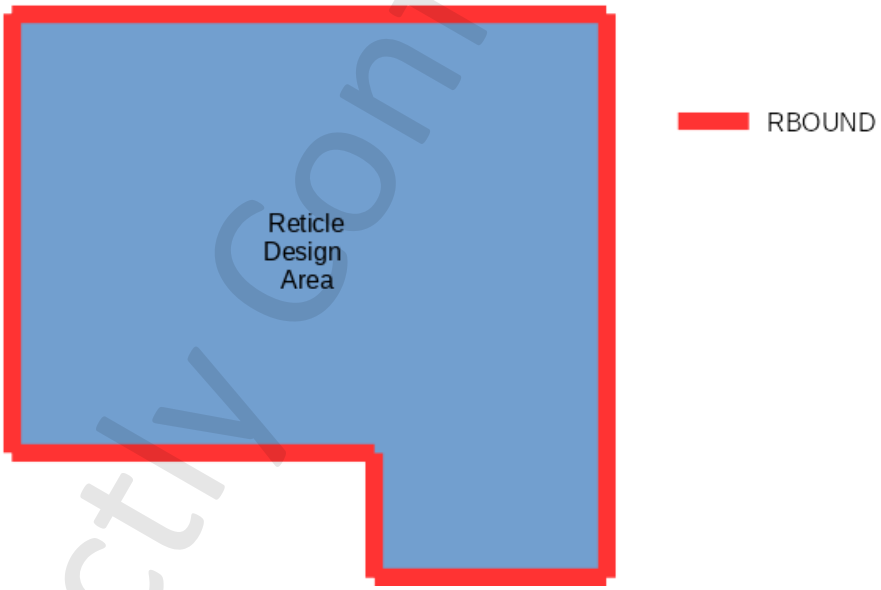

Figure 19: Reticle boundary

2.17 Layer Density Rules

The target densities specified in Table 20 must not be exceeded. Designs with significantly lower density will have dummy fill shapes added by Pragmatic data preparation as described in the Design Guide. The first rule (DENS.1) applies to each layer but the second and third rule are specific to the metal layers within the transistor.

Rule	Description	Value
DENS.1	Maximum global metal density in each metal layer	50%
DENSSD.1	Maximum local density (window size = 12µmx12µm, step 6µm) of SD when width >=25µm (except for capacitors with CAPID)	75%
DENSGATE.1	Maximum local density (window size = 12µmx12µm, step 6µm) of GATE when width >=25µm (except for capacitors with CAPID)	75%

Table 20: Layer densities

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Appendix 2: List of acronyms

Acronym	Meaning
DfM	Design for Manufacture
DG	Design Guide
DRM	Design Rule Manual
EDA	Electronic Design Automation
FlexICs	Flexible Integrated Circuits
GDSII	Graphic Design System II
IGZO	Indium Gallium Zinc Oxide
LVS	Layout Versus Schematic
NRE	Non-Recurring Engineering
PDK	Process Design Kit
LFUSE	Laser Fuse
TFT	Thin Film Transistor

Table 21: List of acronyms

Appendix 3: Document version control

Version	Description of changes	Date
1.0	First PDK release for Helvellyn 2.1.0 beta	1st February 2023
2.0	First revision for Helvellyn 2.1.0.beta.2	8th March 2023
2.1	Section on CAPID layers updated	16th March 2023

Table 22: Document version control

Appendix 4: Index