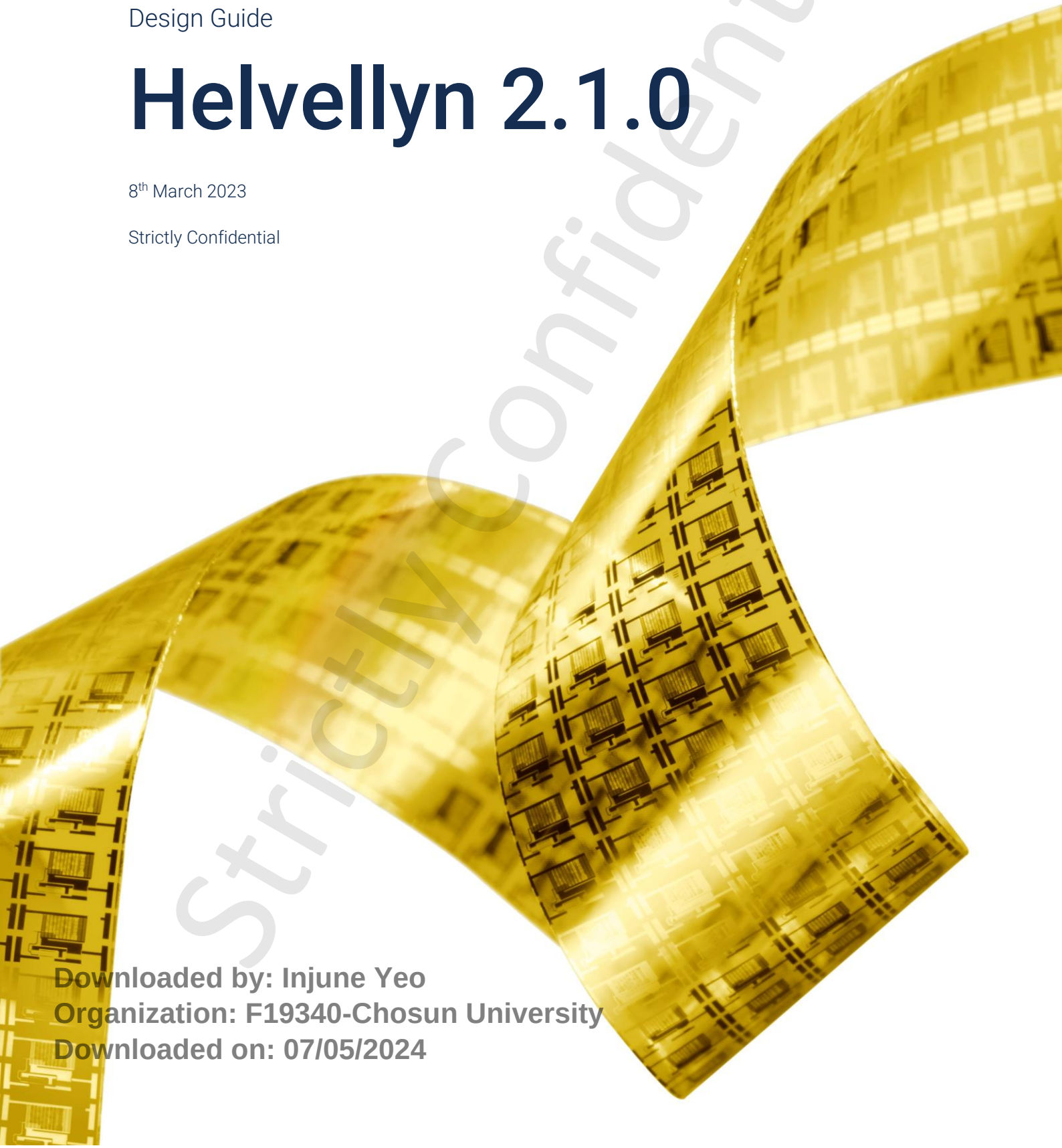
Pragmatic

Design Guide

Helvellyn 2.1.0

8th March 2023

Strictly Confidential



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1 Introduction

This Design Guide (DG) provides guidance for engineers who wish to build circuits based on the Helvellyn FlexIC Foundry process technology. It includes design, simulation and electrical specifications and links to additional guidance material relevant to this technology node. This is a Helvellyn 2.1.0. beta.2 release.

1.1 Process description

Pragmatic's Helvellyn technology is based on Indium Gallium Zinc Oxide (IGZO), an amorphous metal-oxide n-type semiconductor. Flexible integrated circuits (FlexICs) manufactured by Pragmatic are built on an insulating polyimide substrate and therefore there is no conductivity within the bulk and no parasitic capacitance between devices and the substrate. Equivalent field effect mobility within the transistors is roughly 10cm^2/Vs.

High-k capacitors and a dedicated high value resistor layer are available. The process has four routable metal layers which include the metal layers utilised within the TFT device to form the gate and source-drain regions.

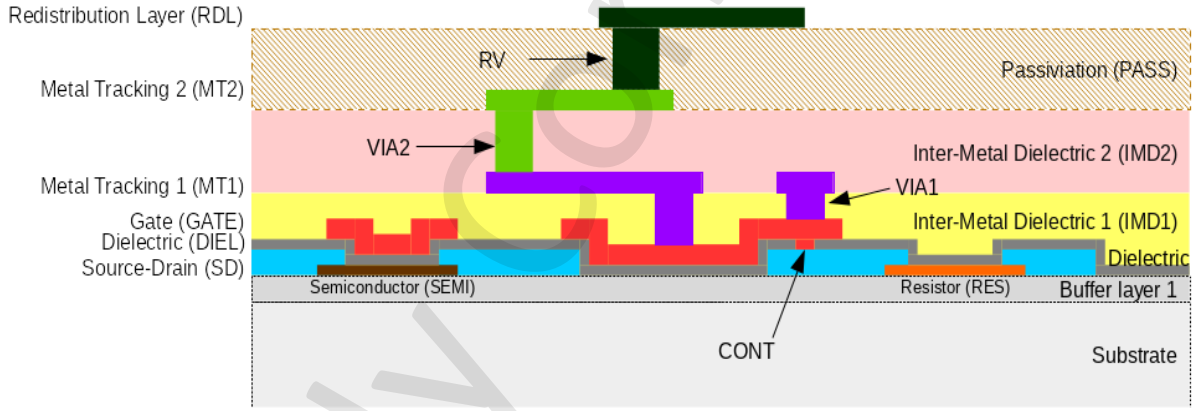

Figure 1: Technology cross section (not to scale)

The full list of the drawn layers is given in the Helvellyn Design Rules Manual (DRM), which should be used in conjunction with this document. Reference to rules from the DRM and Reticle Design Manual (RDM) and are highlighted in this way in this document: **[RULE.X].**

The DG, DRM and RDM list the rules that must be followed by designers when building circuits for production using the Helvellyn process technology. There are some rules that are mandatory, failure to meet these rules will cause the design to fail DRC and LVS checks. Other rules are recommendations, these have a W in the rule name and are related to Design for Manufacture (DfM) considerations for improved manufacturing yield. These rules will be flagged if they fail the DRS and LVS. When this happens

the designer and Pragmatic will discuss the violations and whether to proceed. Pragmatic reserve the right to refuse to tape out a design.

Test chips are recommended for all circuits, particularly analogue designs, to ensure that they meet the requirements of the design. There are other rules that are simply best practice and are not checked. This document will explain some of best practice rules and give guidelines on how they should be interpreted.

1.2 Digital considerations

To design digital logic cells in a unipolar transistor technology requires a different approach compared to complementary technologies, for example using an n-type transistor under different bias conditions (e.g. diode load) or utilising a fixed high value resistor. Each of these options creates different trade-offs between area, power, speed, and robustness (noise margin). Mitigation measures for one parameter may have a negative impact on others, such as utilizing buffer stages to recover noise margin ("pseudo-CMOS logic") where circuit robustness is improved at the cost of other parameters.

In all design types, using the Helvellyn process technology, there is a significant static power draw through the load in addition to the dynamic power consumption. This additional power draw needs to be considered with particular attention to heat generation and dissipation given the insulating nature of the flexible substrate.

The lack of a complementary load, or the use of a passive load, will also create a significant asymmetry in transient behaviour that must be taken into account. If a passive load is used, then rising edges at internal nodes will typically be slower than falling edges as they are limited by the charging of node capacitance through a relatively large load resistance. In such cases, falling edge triggered logic may be considered instead of rising edge logic to reduce any jitter associated with the slower rising edges. The asymmetric behaviour may also lead to unwanted lengthening or shortening of pulses or clocks as they pass through multiple stages of buffers.

1.3 Analogue considerations

The design of analogue blocks should take note of the following considerations:

- The overlap capacitance between SD and GATE regions is significant so the routing of GATE over SD should be avoided. It is recommended that GATE routing over SD be limited to short connection, for example, within a cell layout or between adjacent blocks. Even in such cases, any SD-GATE overlaps should be kept to a minimum. Long signal or clock tracks should be routed in MT1 or MT2.
- The parasitic effects of metal-metal overlaps must be considered. As noted above, SD-GATE overlaps are particularly high but even the capacitances associated with the higher metal layers of MT1, MT2 and RDL can be quite significant compared to the intrinsic transistor capacitances. Simulations using parasitic extracted netlists are recommended.

2 Layout guidelines

The following section outlines the design recommendations to achieve an optimised layout that should result in the best manufacturing outcome.

2.1 Transistors

Transistors must consist of a single straight channel segment. A single channel segment is defined as an isolated SEMI island where the channel length connects between two parallel electrodes defined in SD, extending beyond the edge of SEMI in the width (W) direction. Channel length is defined as the distance between these two parallel SD structures. The entirety of the region defined by the transistor width (W) and length (L) dimensions should be covered with an associated structure in GATE, with the required rules considered. SEMI should not be continuous between neighbouring transistor elements but confined around the channel region. An example is shown below:

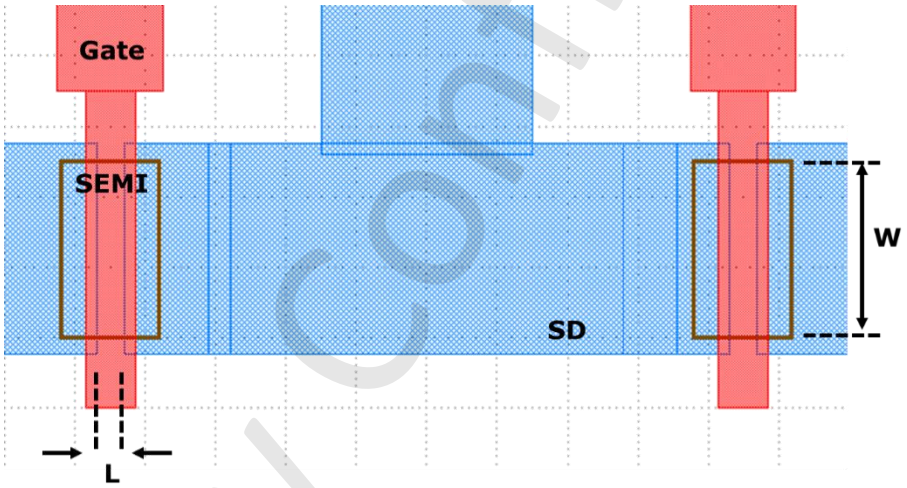

Figure 2: An example of two small transistors

Note that the spacing between transistor channels as well as the density of local metallisation may be increased to improve heat dissipation, as long as **[DENSSD.1]** and **[DENSGATE.1]** are not violated.

Additional measures that can be taken include increasing notch width, decreasing the individual transistor width (W), or adding a metal heat distributing shield in upper metals (MT1 and/or MT2) above the TFT.

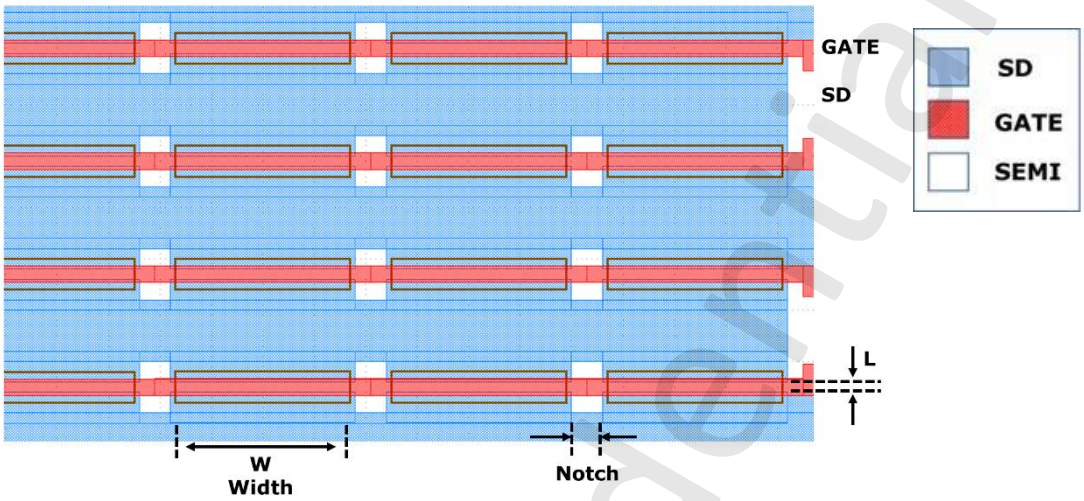

Figure 3: An example of transistors connected in parallel

2.2 High value resistors

High value resistors can be adapted in layout to optimise their footprint within the circuit, including serpentine shapes. However, the path of current through a serpentine device is not the same as through a straight resistor with the same number of squares. The sheet resistance values listed in Table 6 are based on straight resistors.

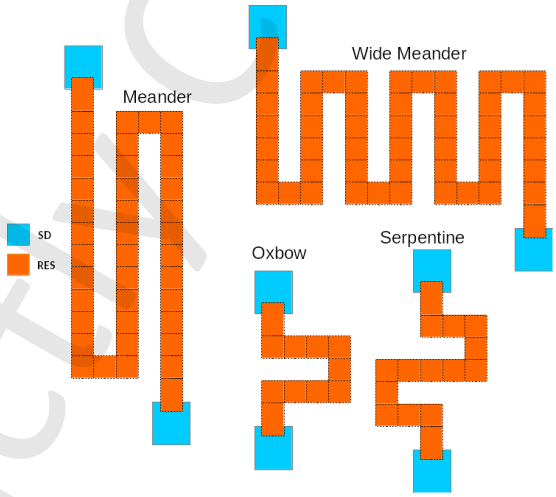

Figure 4: Examples of high value resistor structures

The resistance of non-straight resistors can be calculated using the following equation and Figure 5

$$R_{sh} = 200\ (1\text{-}0.98c)$$

where R_{sh} = effective sheet resistance [kΩ/square], c = number of corners per micron length of resistor.

This calculation is performed automatically by the res p-cell in the pragLib library and by the parasitic extraction decks. Note that the sheet resistance calculation for non-straight resistors has been validated for structures with only up to 16 corners.

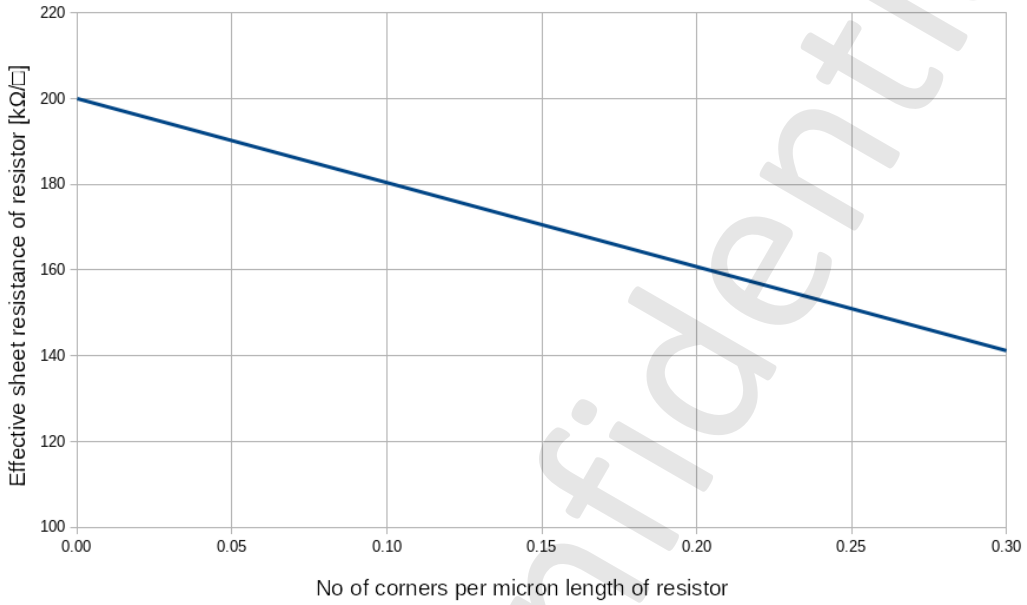

Figure 5: Relationship between effective sheet resistance and number of corners

2.3 Metal resistors

All metal paths have some parasitic resistance. (See section 3.4.) These are not seen during LVS or schematic simulations although they are seen during a parasitic-resistance extracted simulation. However, if a metal resistor from layers SD, GATE, MT1, MT2 or RDL is needed for a functional purpose, then a corresponding metal resistor ID layer may be used to identify the metal resistor. These metal resistor ID layers are RESIDSD, RESIDGATE, RESIDMT1, RESIDMT2, RESIDRDL for SD, GATE, MT1, MT2, RDL respectively.

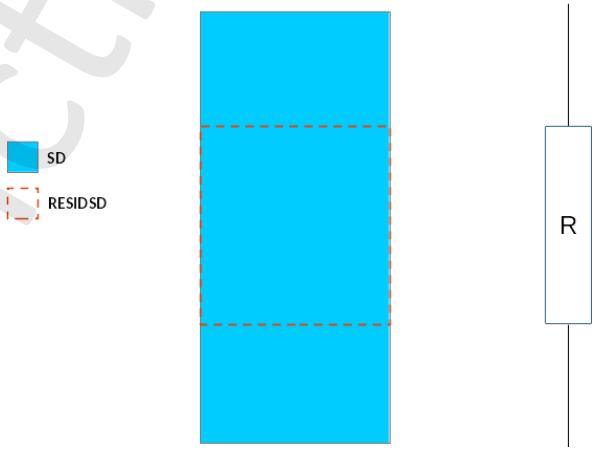

Figure 6: Metal resistor

Figure 6 shows an example of an SD metal resistor. Only the SD layer that is directly underneath the RESIDSD layer is identified as a functional metal resistor for LVS and schematic simulation purposes.

2.4 Capacitors

All metal -metal overlaps have some parasitic capacitance. (See section 3.4.) These are not seen during LVS or schematic simulations although they are seen during a parasitic-capacitance extracted simulation. However, if a metal-metal capacitor from layers SD, GATE, MT1, MT2 or RDL is needed for a functional purpose, then a corresponding capacitor ID layer may be used to identify the metal-metal capacitor. These capacitor ID layers are CAPID for SD-GATE capacitors, and CAPID2 for all other metal-metal capacitors.

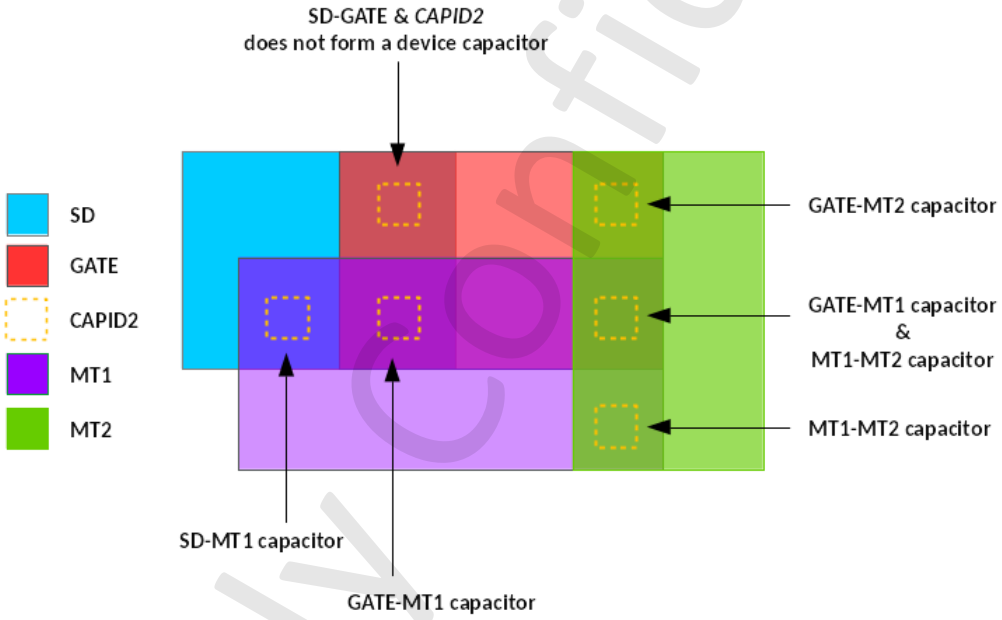

Figure 7: CAPID2 examples

2.5 Optimising current density

The integrated circuit is mainly constructed of polymer layers, including the substrate, intermetal dielectrics and passivation. This means that heat generated within the circuit remains localised near the point at which it is generated. In designs that require large current densities, care should be taken to reduce hotspots within the device layout. For example, 90° angles will result in high current densities at the inner corner. Two 45° angles can be used to better distribute the current and hence the heat generated.

Figure 8: Design optimisation for current density with corners

Similarly, a diamond shaped array of vias can be used to distribute heat as shown below.

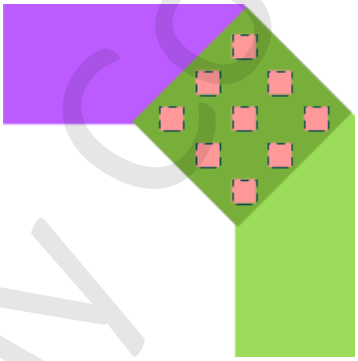

Figure 9: Design optimisation for current density with vias

When connecting features with different widths, tapering the link is advised:

Figure 10: Connecting features of different widths

Bowtie connections should be used to reduce current hotspots:

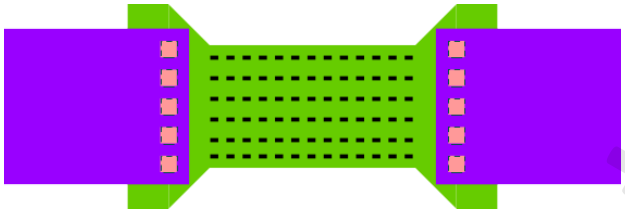

Figure 11: Bowtie connections

Designers must consider compound effects of power lines, for example when routing to I/O pads, and ensure the current density does not exceed that specified in Table 3. **[SD.7W], [GATE.17W], [MT1.7W], [MT2.7W].**

2.6 ESD guidelines

The Helvellyn process technology does not include diodes, so groupings of passive components and transistors must be used to manage ESD protection. There are multiple approaches to accomplish this, focusing on reducing the peak voltage seen at an input or output (I/O). For example, additional capacitance can be used to reduce the voltage created by a set amount of charge and combined with the provision of a discharge path. Also, resistance can help to create a resistor/capacitor (RC) delay along the charging path to provide time for the discharge path to turn on and further reduce peak current values. The capacitor should also be designed such that the GATE layer is smaller than the SD layer. This is to avoid the vertical perimeters which may present an ESD risk. A possible circuit is shown below.

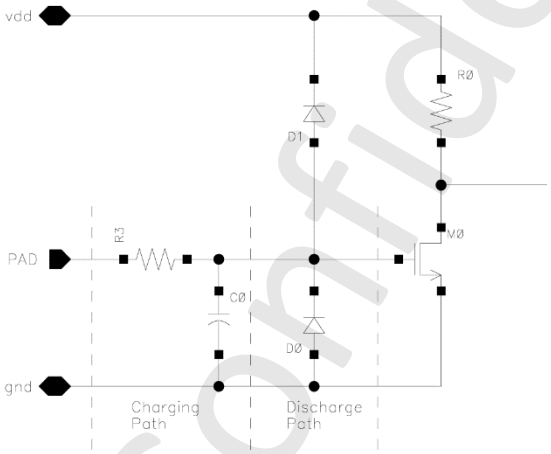

Figure 12: Example of ESD protection circuit on IO buffer where the diodes may be a series of diode-connected transistors

The use of transistors in a diode configuration, i.e., gate connected to drain, can help provide additional ESD mitigation with a unidirectional current path that provides an improved discharge path.

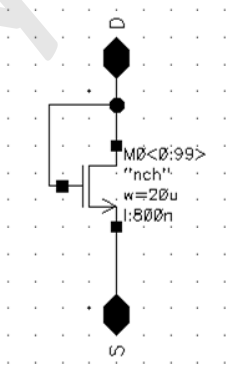

Figure 13: Example ESD protection diode circuit

2.7 Metal density

For all layers, designers must remain within the limits given **[DENS.1], [DENSSD.1]** and **[DENSGATE.1].** The density of the SD layer is particularly critical. Pragmatic applies fill algorithms to control layer densities, improving reliability and providing consistent device performance independent of design. Designers should not apply their own metal fill patterns to increase layer density.

Where there are large areas of SD-GATE capacitance, for example for VDD-VSS decoupling, care should be taken to not have very large unbroken areas of SD. Figure 14 shows an example of how openings within a large area of metal can be patterned to reduce the metal density.

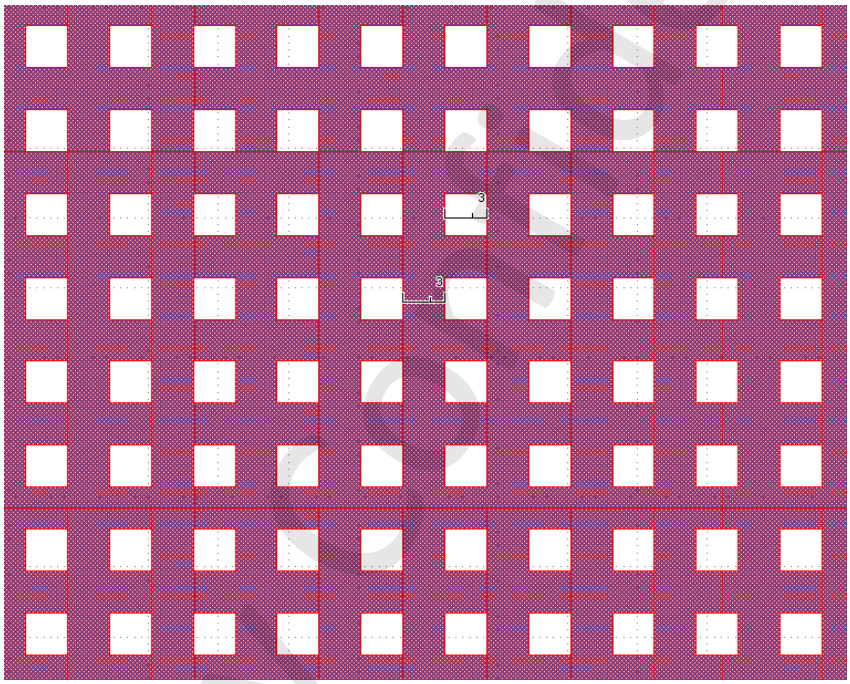

Figure 14: Example of openings within a large SD-GATE capacitor structure.

2.8 Bus routing

When routing parallel metal tracks in any metal layer, for example in a bus, these should be separated by a spacing greater than the appropriate design rule minimum **[SD.3], [GATE.2], [MT1.2],** or **[MT2.2]** as described in **[SD.6W]. [GATE.16W], [MT1.6W] and [MT2.6W]**.

For very long lines, the designer should consider if the operating frequency and the length of line might cause some transmission line effects. The dielectric constant (or relative permittivity) of the IMD1 and IMD2 layers are 3.0 @ 1kHz to 10kHz, up to 4.1 @ 1GHz.

Figure 15: Parallel metal track spacing example

To increase the mechanical integrity of the circuit the designer should consider pinning metal tracks at intervals as described in **[GATE.18W], [MT1.8W], [MT2.8W] and [RDL.4W].**

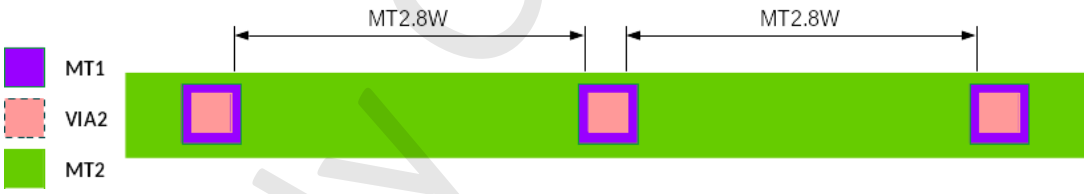

Figure 16: Example of pinning long MT2 metal track with VIA2

2.9 Vias

In order to improve yield (CONT, VIA1, VIA2, RV), it is recommended that 2 or more vias are used to make a connection between layers.

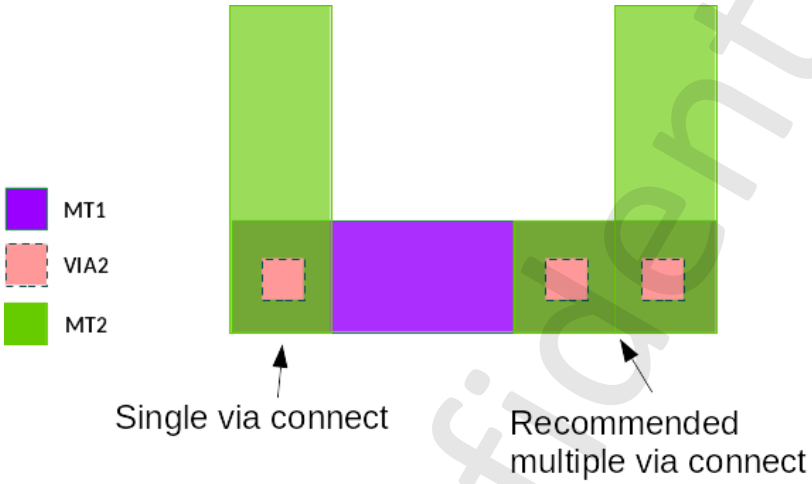

Figure 17: VIA2 connections

2.10 Devices under external connection pads

It is recommended that transistors, high value resistors and capacitors are not placed under probe or bond pads. It is possible for damage to occur to such devices when the pad area is probed for testing or during bonding operations involving the pad. Devices placed under probe or bond pads are also at risk of changes in performance due to the possibility of localised changes in temperature or pressure.

3 Electrical rules

3.1 Voltage limits

V_{PEAK} is the maximum voltage that can be applied to a dielectric before permanent damage may be caused.

Parameter	V_{PEAK} (V)
DIEL gate dielectric breakdown voltage	12
IMD1 inter-metal dielectric-1 breakdown voltage	20
IMD2 inter-metal dielectric-2 breakdown voltage	20
PASS passivation breakdown voltage	20

Table 1: Maximum allowed voltages

3.2 DC Power and DC current limits

As described earlier in Section 2.1, care must be taken to not generate excessive heat in any part of the circuit. This can be achieved by limiting the current, and therefore power dissipation, in a localised area when considering the total, not individual, transistor width. The following tables provide the safe operating limits.

Sum of transistor widths (µm)	Power density (µW/µm)
≤120	10.0
>120	1.0

Table 2: Maximum power density for transistors per µm of width (for sub-width = 20µm and notch width = 3µm, where total channel width >20µm)

Layer	Current density (mA/µm)
SD	0.1
GATE	0.1
MT1	0.1
MT2	0.1
RDL	0.25

Table 3: Maximum current density for metal routing per µm of width

Layer	Size (µm)	Current (mA)
CONT	1.0 x 1.0	0.075
VIA1	1.5 x 1.5	0.075
VIA2	1.5 x 1.5	0.075
RV	20 x 20	0.5

Table 4: Maximum current through vias

3.3 Transistor parasitic capacitance

Within a transistor, there are regions of overlap between SD and GATE. The simulation model and the parasitic extraction deck assume that a transistor has been drawn with the minimum dimensions as detailed in the DRM **[GATE.3] [GATE.4].** The p-cell provided in the PDK uses these minimum dimensions. Therefore, if a transistor has been drawn with different SD and GATE extension dimensions, both the simulation model and parasitic extraction will be incorrect.

3.4 Device and parasitic routing capacitance

High value capacitors are formed by the intentional overlap of the SD and GATE layers. A p-cell is provided for this. The other layer-layer capacitors should not be used for devices, and the values given in Table 5 are a guide for parasitic effects only. These are the maximum capacitances expected between the layers.

There is a significant capacitance between the two lowest metal tracking layers (SD and GATE) due to the thin, high-k insulating material being used as the dielectric layer (DIEL). Routing in these lower metal levels will cause large parasitic capacitances at metal track crossovers between these layers. This routing is recommended to be confined within a standard cell, with routing between cells completed in the upper metal layers (MT1 and MT2).

The capacitance of parasitic capacitors containing IMD1, IMD2, or PASS layers will vary because the thickness of these layers is not constant, since it will depend on the amount and size of the patterning below. Typically, larger planar structures will have less capacitance per unit area than structures where the lower level is made up of narrow lines. Narrow lines result in higher capacitance.

Table 5 shows the maximum parasitic capacitance when metal is patterned at minimum widths. Minimum and typical values are not provided because they are highly dependent on layout. There is no capacitance from any metal track to the non-conducting substrate.

Parameter	Value			Units
	Min	Typ	Max	
SD-GATE overlap	2.6	2.7	2.8	fF/μm^2
SD-MT1 overlap			0.15	fF/μm^2
SD-MT2 overlap			0.08	fF/μm^2
SD-RDL overlap			0.04	fF/μm^2
GATE-MT1 overlap			0.15	fF/μm^2
GATE-MT2 overlap			0.08	fF/μm^2
GATE-RDL overlap			0.04	fF/μm^2
MT1-MT2 overlap			0.18	fF/μm^2
MT1-RDL overlap			0.05	fF/μm^2
MT2-RDL overlap			0.06	fF/μm^2

Table 5: Layer to layer capacitance values

3.5 Device and wire resistance

Parameter	Value			Units
	Min	Typ	Max	
SD sheet resistance	0.200	0.325	0.450	Ω/☐
GATE sheet resistance	0.200	0.325	0.450	Ω/☐
MT1 sheet resistance	0.200	0.325	0.450	Ω/☐
MT2 sheet resistance	0.200	0.325	0.450	Ω/☐
RDL sheet resistance			0.100	Ω/☐
RES sheet resistance	0.150	0.200	0.250	MΩ/☐
CONT resistance			2.000	Ω
VIA1 resistance			2.000	Ω
Stacked CONT-VIA1 resistance			2.000	Ω
VIA2 resistance			2.000	Ω
RV resistance			2.000	Ω

Table 6: Interconnect resistance values

4 Simulation information

This section describes the SPICE simulation compact models and the conditions for simulations. Maximum operating voltage is defined in Table 1.

4.1 Transistor model

The n-channel transistor model is an amorphous silicon 3-terminal model. Simulation models are provided in the Cadence Spectre format for fast, typical and slow corners. As Pragmatic's n-TFT technology is based on a metal-oxide semiconductor, this will lead to an imperfect model fit.

4.2 Transistor model performance

The result of the simulation model for the typical corner compared with measured data for normalised widths is shown in Figure 18 and Figure 19 and measured data normalised for length is shown in Figure 20 and Figure 21. The simulation models are only accurate at low I_{DS} current down to approximately 10pA. This is a limitation of the measuring equipment.

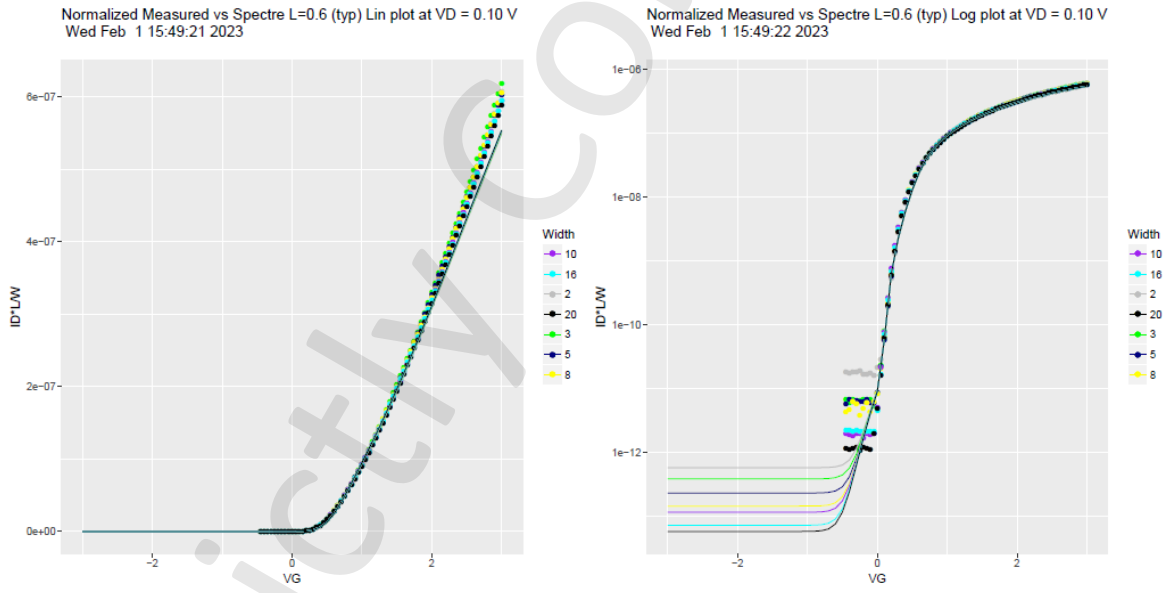

Figure 18: TFT measured performance (normalised width) vs simulated model at 25°C and V_D=0.1V

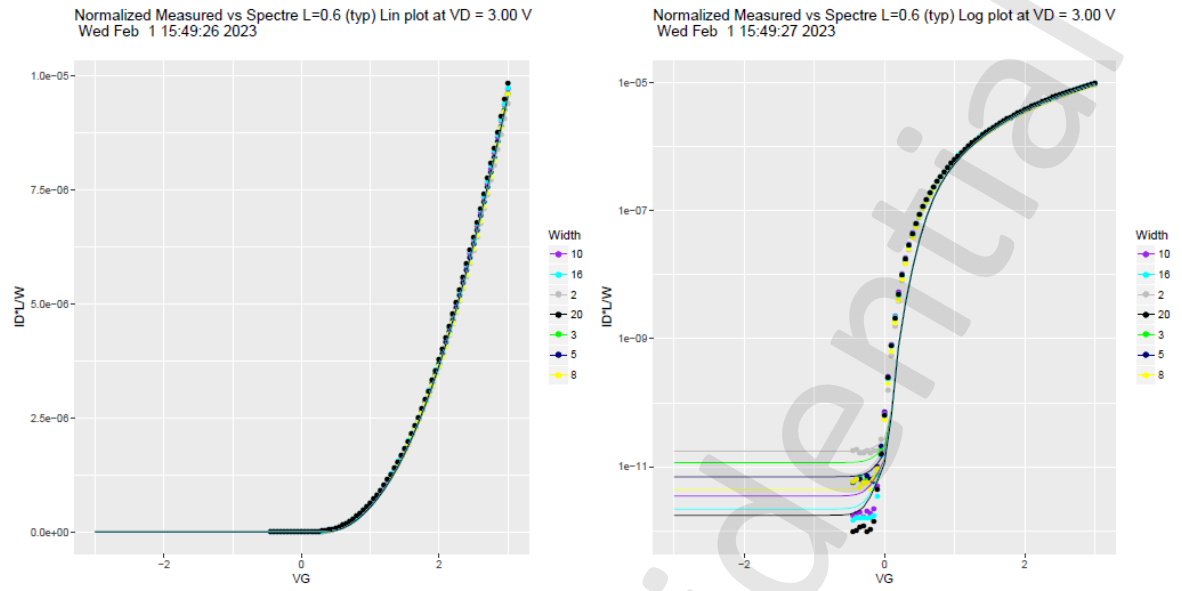

Figure 19: TFT measured performance (normalised width) vs simulation model at 25°C and V_D=3V

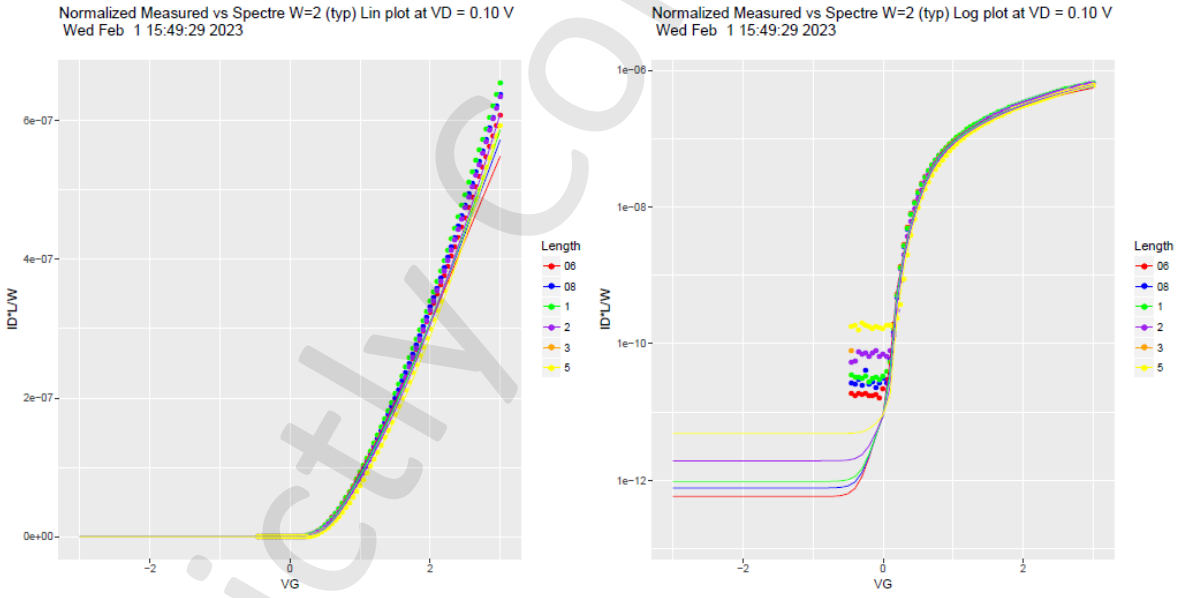

Figure 20: TFT measured performance (normalised length) vs simulation model at 25°C and V_D=0.1V

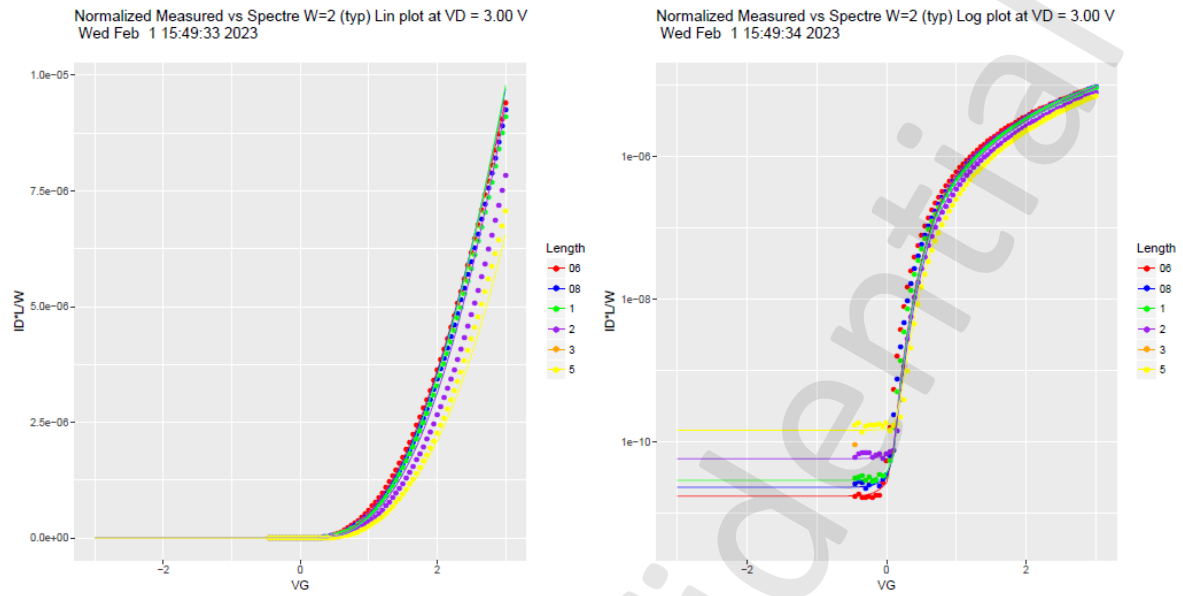

Figure 21: TFT measured performance (normalised length) vs simulation model at 25°C and V_D=3V

It should be noted that the simulation model is accurate at L=5µm and between L=0.6µm to L=1µm but is less accurate at intermediate length values. Please speak to your Pragmatic representative for more details.

The graphs in this section show the voltage limits with which the model has been characterised. Simulation beyond these limits may be unpredictable. The voltage limits are listed in Table 7.

Parameter	Description	Min voltage (V)	Max voltage (V)
V_G	Gate-Source voltage	-0.5	3.0
V_D	Drain-Source voltage	0	3.0

Table 7: Simulation model voltage limits

The results of the simulation model for the typical, fast and slow corners compared with measured data for 2x0.6 µm and 2x5 µm are shown in Figure 22 to Figure 29.

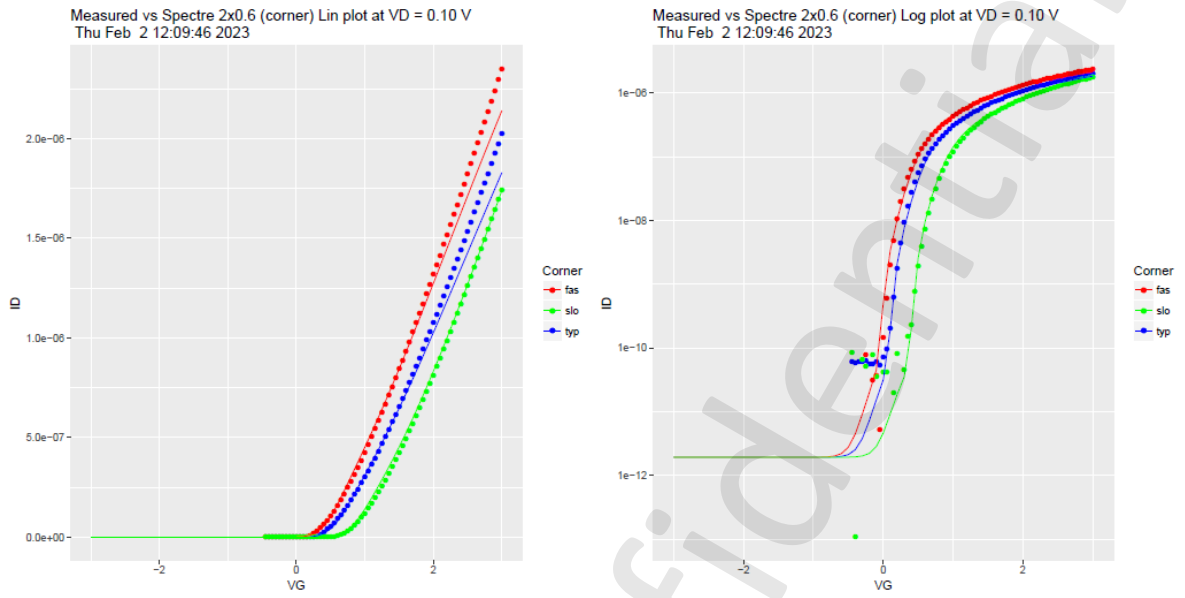

Figure 22: 2x0.6 µm TFT corners measured performance vs simulation model at 25°C and V_D=0.1V

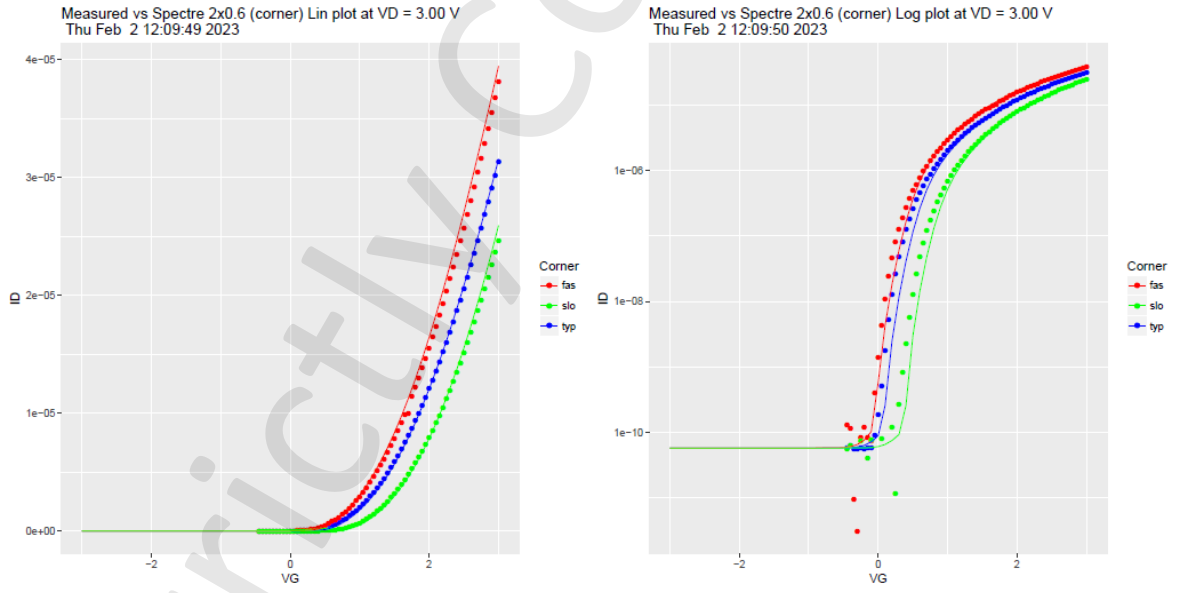

Figure 23: 2x0.6 µm TFT corners measured performance vs simulation model at 25°C and V_D=3V

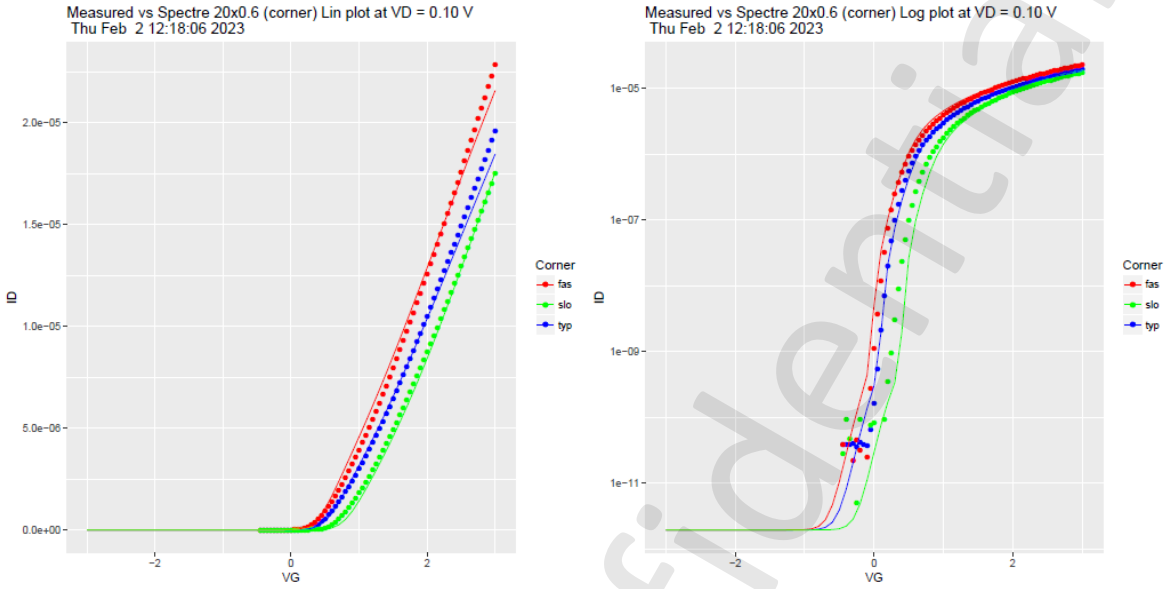

Figure 24: 20x0.6 µm TFT corners measured performance vs simulation model at 25°C and V_D=0.1V

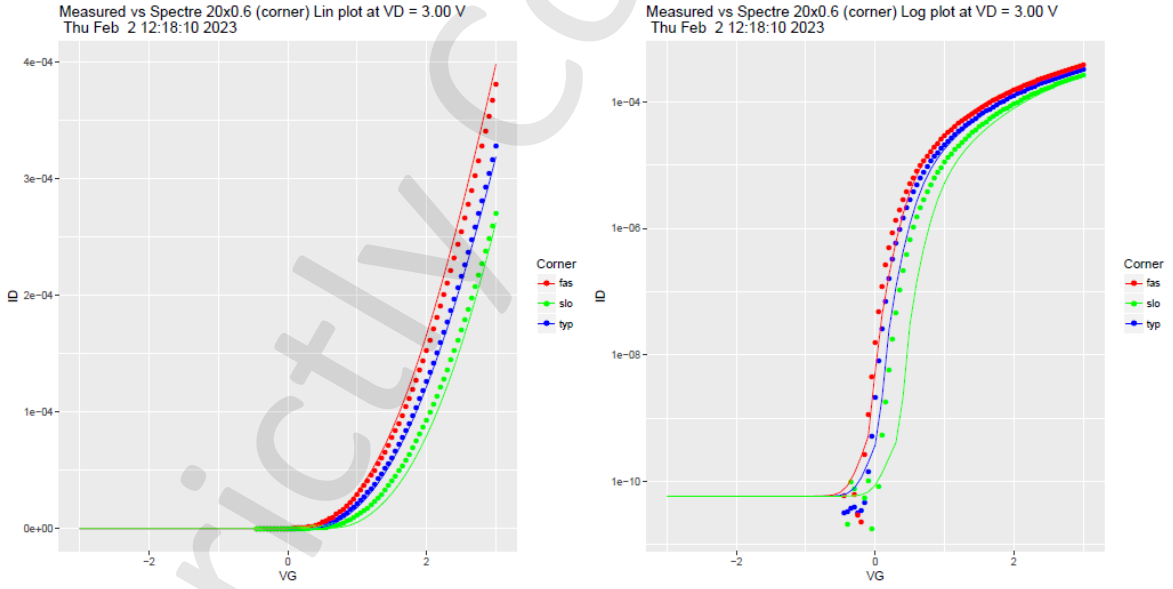

Figure 25: 20x0.6 µm TFT corners measured performance vs simulation model at 25°C and V_D=3V

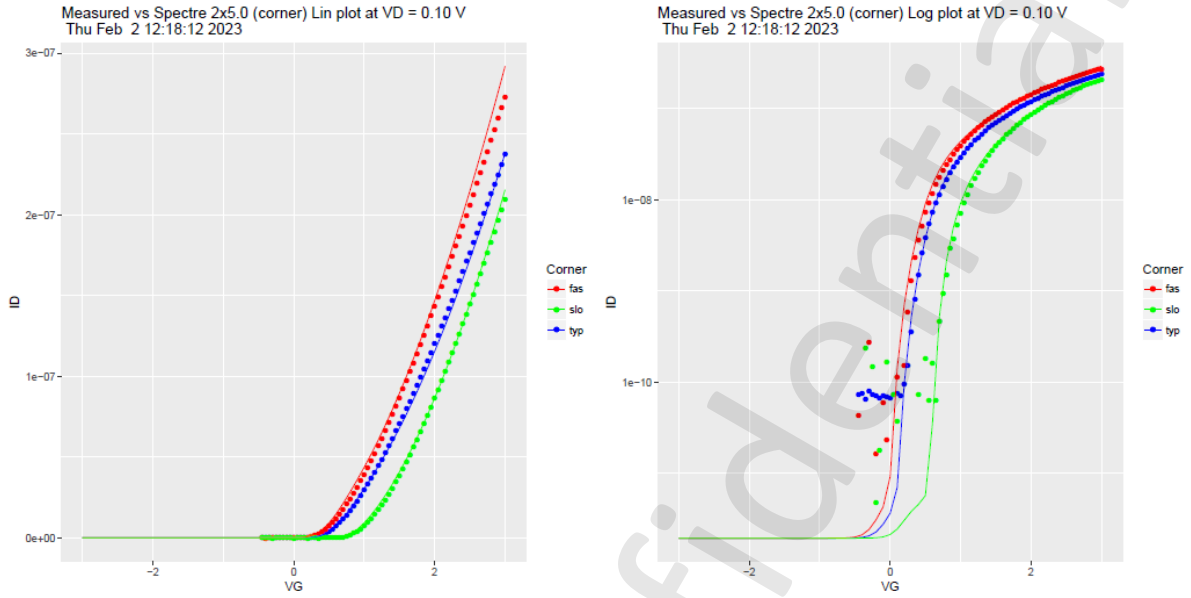

Figure 26: 2x5 µm TFT corners measured performance vs simulation model at 25°C and V_D=0.1V

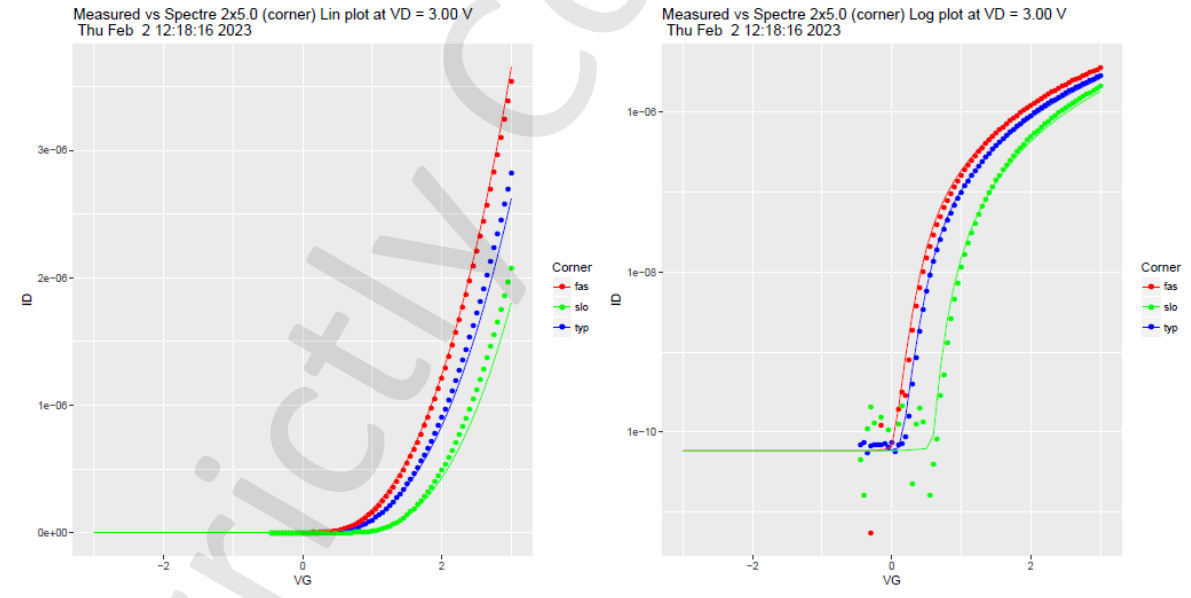

Figure 27: 20x0.6 µm TFT corners measured performance vs simulation model at 25°C and V_D=3V

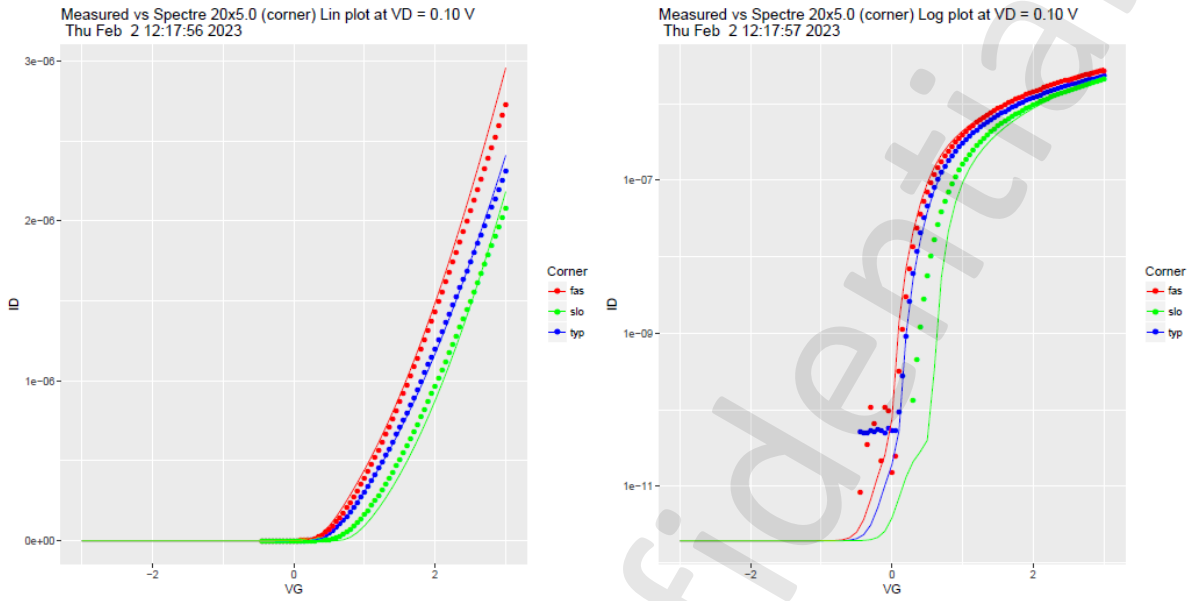

Figure 28: 20x5 µm TFT corners measured performance vs simulation model at 25°C and V_D=0.1V

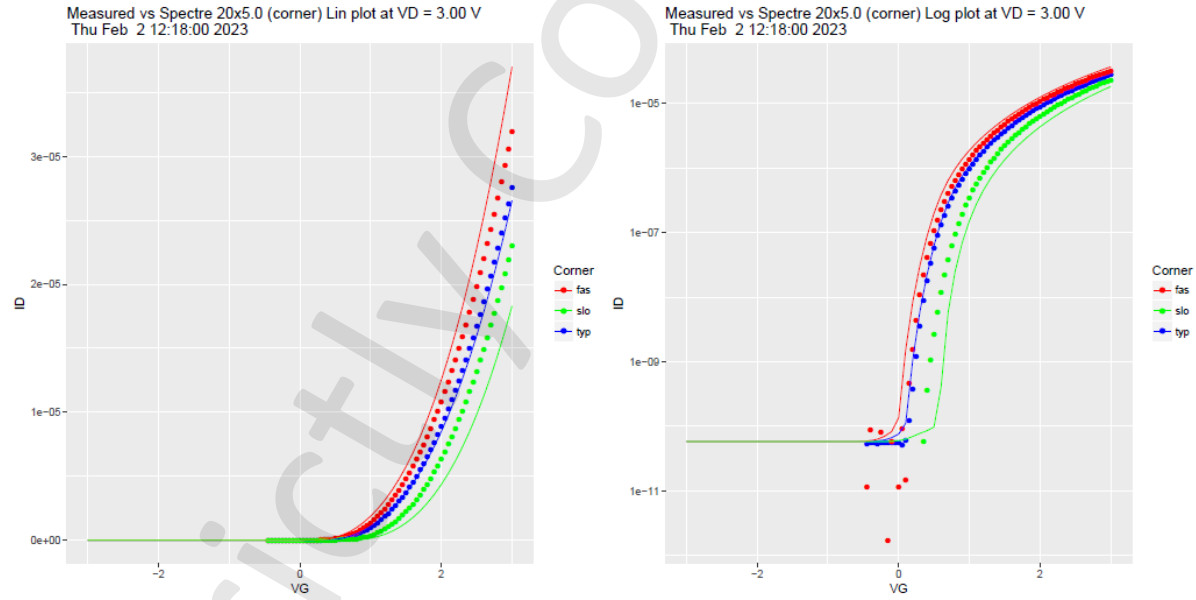

Figure 29: 20x5 µm TFT corners measured performance vs simulation model at 25°C and V_D=3V

The following table shows the measured vs simulated transistor current (I_{ON}), under the following conditions V_D = 3.0V, V_G = 3.0V and V_S = 0V at 25ºC.

Geometry (µm x µm)	Condition	I_{ON} measured (µA)	Simulated (µA)	Error (%)
2.0 x 0.6	Fast	38.11	39.46	3.55
2.0 x 0.6	Slow	24.63	25.94	5.31
2.0 x 0.6	Typical	31.31	31.57	0.83

Table 8: TFT measured vs simulated I_{ON}

The amorphous semiconductor material used for the transistors exhibits a small mobility increase with increasing temperature. This temperature behaviour is not currently captured in the transistor simulation model. The transistor models are simplified and are invariant to temperature in this range. Please contact your Pragmatic representative for more details.

4.3 Transistor Monte-Carlo models

Monte-Carlo models will be provided in a future release.

4.4 Transistor model leakage currents

Leakage currents in the amorphous silicon model have the following observed behaviour which must be considered:

- The measured SD channel leakage currents, I_{DSLEAK}, are at the noise floor of measuring equipment. Therefore, the corresponding leakage current values in the model may be inaccurate, consequently the leakage may be over-estimated.
- GATE leakage is not included in the model.

4.5 High value resistor model

The conductivity of high value resistors increases with temperature, resulting in a change in sheet resistance at the rate of -0.6% per degree centigrade (°C). The high value resistor model has temperature coefficients. Monte-Carlo models are not provided. The table below shows the modelled sheet resistance.

Process	Sheet resistance (MΩ/□)
Minimum	0.15
Maximum	0.25
Nominal	0.20

Table 9: Modelled sheet resistance for a straight high value resistor at 25 °C and 3 V.

4.6 Capacitor model

The capacitor model includes no temperature coefficients. Monte-Carlo models are not provided. The table below shows the modelled capacitance of a capacitor designed to be 27pF:

Process corner	Cap (pF)
Minimum	26.0
Maximum	28.0
Nominal	27.0

Table 10: Modelled device capacitance

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Appendix 2: List of acronyms

Acronym	Meaning
DfM	Design for Manufacture
DG	Design Guide
DRM	Design Rule Manual
EDA	Electronic Design Automation
FlexICs	Flexible Integrated Circuits
IGZO	Indium Gallium Zinc Oxide
LFUSE	Laser Fuse
LVS	Layout Versus Schematic
NRE	Non-Recurring Engineering
PDK	Process Design Kit
RDM	Reticle Design Manual
TFT	Thin Film Transistor

Table 11: List of acronyms

Appendix 3: Document version control

Version	Description of changes	Date
1.0	First release of Helvellyn 2.1.0.beta.1	1st February 2023
2.0	First major revision Helvellyn 2.1.0.beta.2	8th March 2023
2.1	Section on capacitors added	16th March 2023

Table 12: Document version control

Appendix 4: Index