Pragmatic

Reticle Design Manual

Helvellyn 2.1.0

8th March 2023

Strictly Confidential

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1 Introduction

The Reticle Design Manual (RDM) provides guidance for engineers who wish to design their own reticles incorporating their electronic circuits based on the Helvellyn FlexIC Foundry process technology. This is a release of Helvellyn 2.1.0 beta.2.

2 Tape-out and reticle information

2.1 Transmission protocol and data format

Data for fabrication must be delivered in GDSII format using the GDS/layer mapping of the Pragmatic PDK. It is mandatory for customers to run a DRC check before sending the GDSII to Pragmatic, we recommend running an LVS check alongside to ensure there are no errors.

After the GDSII is delivered to Pragmatic, Pragmatic will perform DRC checks before confirming acceptance of the GDSII. Pragmatic retains the right to reject a design that fails DRC checks and will provide reasons for the decision.

Below is the recommended flow to use for tapeout on Helvellyn 2.1.0:

- Dry-run database > 7 days before tapeout
- Provide DRC clean full reticle GDSII on Pragmatic FTP server (*.gds, *.gds.tar.gz format required)
- Provide .drc results
- Announce delivery to Pragmatic
- Pragmatic will process the GDSII
- Final GDSII is sent back to the customer for confirmation before reticle generation

2.2 Reticle information

The usable reticle area is the total reticle area **[RET.1]** minus the reserved area **[RET.2]** as given in the table below and shown diagrammatically. It should be noted that the usable reticle area is slightly smaller than the reticle repeat distance.

These rules will not be checked by DRC and need to be verified by the customer independently. The customer can use the Reticle Outline Frame (Core_Outline_22x21) provided in the PDK to carry out this verification.

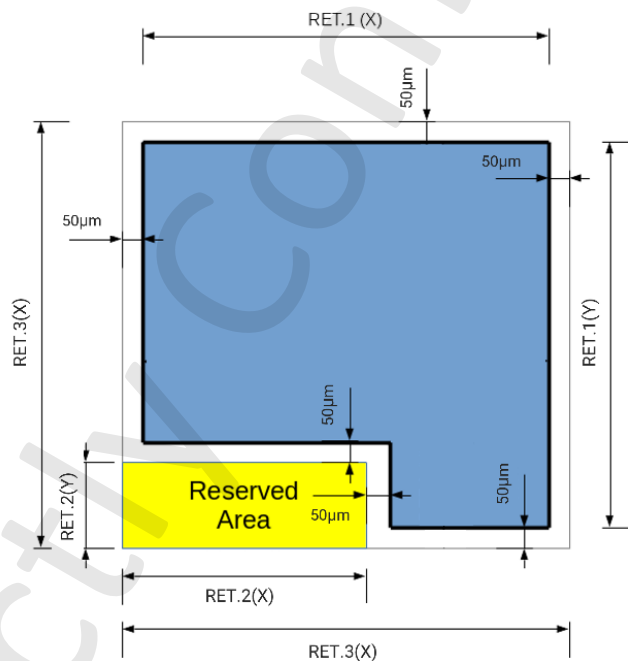| Rule	Description	Area (mm)
RET.1	Total reticle area	21.9 x 20.9
RET.2	Reserved area	9 x 3
RET.3	Reticle repeat distance	22 x 21

Table 1 Reticle area rules

Figure 1: Reticle layout

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Appendix 2: List of acronyms

Acronym	Meaning
DRC	Design Rule Check
DRM	Design Rule Manual
ESD	Electrostatic Discharge
FlexICs	Flexible Integrated Circuits
GDSII	Graphic Design System II
IGZO	Indium Gallium Zinc Oxide
LVS	Layout Versus Schematic
PDK	Process Design Kit
TFT	Thin Film Transistor

Table 2: List of acronyms

Appendix 3: Document version control

Version	Description of changes	Date
1.0	First release for Helvellyn 2.1.0.beta.1	1st February 2023
2.0	First revision for Helvellyn 2.1.0.beta.2	8th March 2023

Table 3: Document version control

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