Helvellyn 2.1.0 beta.2 Datasheet

Overview

Pragmatic's FlexIC Foundry® service is a platform for designing flexible integrated circuits that can then be manufactured using the FlexLogIC® fab-in-a-box production system. The FlexIC Foundry service is the first in the world to allow innovators to design custom flexible integrated circuits (FlexICs) that are thinner than a human hair. Its unique technology enables the rapid turnaround of new designs and prototypes at a low fixed cost. This combination allows designers to iterate and test their creations within weeks, accelerating the development cycle.

The remarkable short cycle time of this novel foundry offering empowers system architects to optimise designs for the task at hand, since variants or derivatives can be quickly and cost effectively re-spun. This further reduces the solution cost, as there is no need to design-in overhead to accommodate multiple applications.

The core offering of the FlexIC Foundry is a Thin Film Transistor (TFT) process developed from the beginning to target the unique challenges of flexible integrated circuits. Particularly suited to applications where form factor and cost outweigh speed and performance criteria, FlexICs fabricated using this process excel in areas such as unique identification, multiplexing, driver circuitry, and basic computation.

The second generation Helvellyn 2.1.0 technology node offers four metal layers over a 600nm minimum channel dimension n-type FET process. The process also includes a dedicated resistor layer and metal-insulator-metal capacitors. With an operating voltage of 3 V_{DC}, the technology is ideal for applications including Radio Frequency Identification (RFID), sensing and other applications, thereby enabling the Internet of Everything.

Main benefits

- Low NREs
- Ultra-short tape-out to customer delivery (< 3 weeks)
- Ultra-short manufacturing cycle time (< 5 days)

Main features

- Flexible ICs with ~30µm thickness
- PDK (Process Design Kit) compatible with industry standard EDA tools
- Device library including transistors, resistors and capacitors
- Four metal layer stack for efficient interconnects

Specifications

TRANSISTORS	Metal oxide thin film transistor	n-type FET
	Minimum channel dimension	L= 600 nm, W = 2 µm
	Field effect mobility	~10 cm^2/Vs
	R_{DSOFF} (L=600nm, V_G = 0V, V_D = 0.1V)	> $4x10^8$ Ω.µm
	R_{DSON} (L=600nm, V_G = 3V, V_D = 0.1V)	< $1.6x10^5$ Ω.µm
RESISTORS	Dedicated resistor layer	200 kΩ/sq.
	Minimum line width / space	1.4 µm / 1.4 µm
	Temperature performance	Linear -0.6% per °C
MIMCAPS	Unit capacitance	2.7 $fF/µm^2$
	Leakage at 3.3V	$1x10^{-16}$ $A/µm^{2`}$
INTERCONNECTS	Independent metal routing	4 layers (2 dedicated)
	Routing pitch	6 µm
LASER FUSE	Fuse width	2 µm
	Heat affected zone	~60 $µm^2$
PHYSICAL	Total thickness	~30 µm
	Minimum bend radius	5 mm
PASSIVATION	Top passivation thickness	1.3 µm
	Aluminium RDL	0.5 µm

Table 1: Product specification

EDA Environments

Designers can take advantage of FlexIC Foundry technologies using industry-standard electronic design automation (EDA) tools.

	Simulation	Analog design	Digital design	Place & route	Verification
Cadence	SPECTRE	VIRTUOSO	GENUS	INNOVUS	
Siemens EDA			Oasys-RTL	Nitro-SoC	Calibre

Figure 1: EDA environments

Technology Stack

An aluminium RDL (ReDistribution Layer) final metallisation layer is provided for attachment methods compatible with Aluminium Oxide surface layers.

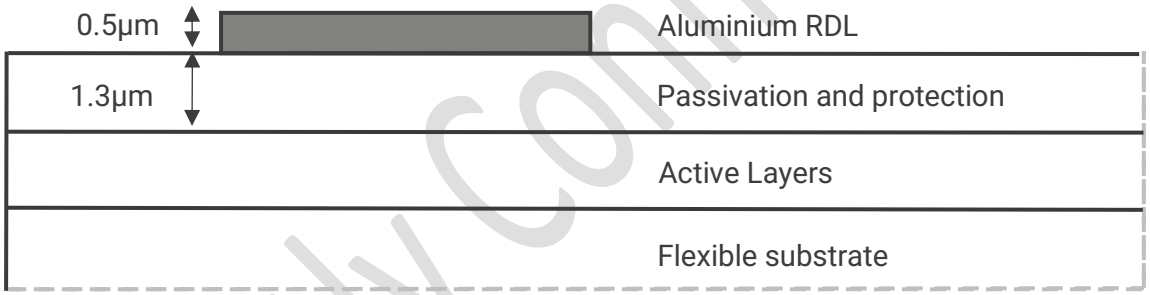

Figure 2: Technology stack

Delivery formats

PragmatIC FlexICs are available in the following formats:

SAMPLES	Chip in Gel Pak Diced on tape and frame
PRODUCTION AND SAMPLES	On glass carrier

Table 2: Delivery formats

Appendix: Legal information

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