Process and Device Simulation of Two-Dimensional β-Ga_2O_3 MOSFETs

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Abstract

In this work, a two-dimensional silicon implanted β-Ga_2O_3 metal-oxide-semiconductor field-effect-transistor (MOSFET) is numerically investigated with our in-house process (G-Process) and device (G-Device) simulation programs. The doping profile and device structure are generated in the G-process and the electrical properties of the resultant structure are simulated with the G-Device. In the process simulation, the impact of the ambient condition on the diffusion profile is investigated. Moreover, the device simulation can be robustly performed up to high bias voltages without any convergence problem. It is expected that these simulation programs can be employed in simulating various Ga_2O_3 devices.

Introduction

Recently, β-Ga_2O_3 has gained much interest, because it is a promising ultra-wide bandgap material. The planar MOSFETs based on β-Ga_2O_3 has been implemented with the ion-implantation and the diffusion process to form selective and high doping region for ohmic contact of access region [1-3]. For an accurate device simulation of the β-Ga_2O_3 MOSFETs, the realistic doping profile and device structure should be generated by the process simulation.

In this work, the process and device simulation of a two-dimensional (2D) β-Ga_2O_3 planar MOSFET is conducted with our in-house simulation programs (G-Process and G-Device [4]).

Process Simulation

First, 2D process simulation is conducted with relevant β-Ga_2O_3 MOSFET process flow [3] shown in Fig. 1. Ion implantation profiles of Si-dopant and damage are calculated from Stopping and Range of Ions in Matter (SRIM) simulation in 1.2 μm unintentionally doped (UID) Ga_2O_3 layer (4×10^{14} cm^{-3} carrier density). Implantation condition reported from [5] is applied to achieve a uniform profile whose depth is 150 nm. And 2D implantation profile is calculated for an open window from -15 μm to -2 μm. Subsequently, the diffusion process simulation is conducted at 1100 ℃ for 60 s in the N_2 or O_2 ambient. In the diffusion process simulation, an experimentally fitted transport model of diffusion process in [6] is adopted:

$$\frac{\partial \mathrm{Si}}{\partial \mathrm{t}} - \mathrm{D_{Si}}\left(\frac{\partial^2 \mathrm{Si}}{\partial \mathrm{x}^2} + \frac{\partial^2 \mathrm{Si}}{\partial \mathrm{y}^2}\right) - \mathrm{R} = 0, \quad (1)$$

$$\frac{\partial \mathrm{V}}{\partial \mathrm{t}} - \mathrm{D_v}\left(\frac{\partial^2 \mathrm{V}}{\partial \mathrm{x}^2} + \frac{\partial^2 \mathrm{V}}{\partial \mathrm{y}^2}\right) + \mathrm{R} + \mathrm{K_{DA}}(\mathrm{V} - \mathrm{E_v})(\mathrm{I} - \mathrm{E_v}) = 0, \quad (2)$$

$$\frac{\partial \mathrm{I}}{\partial \mathrm{t}} - \mathrm{D_I}\left(\frac{\partial^2 \mathrm{I}}{\partial \mathrm{x}^2} + \frac{\partial^2 \mathrm{I}}{\partial \mathrm{y}^2}\right) + \mathrm{K_{DA}}(\mathrm{V} - \mathrm{E_v})(\mathrm{I} - \mathrm{E_v}) = 0, \quad (3)$$

$$\frac{\partial \mathrm{T}}{\partial \mathrm{t}} - \mathrm{R} = 0, \quad (4)$$

$$\mathrm{R} = (\mathrm{K_T} \cdot \mathrm{Si} \cdot \mathrm{V}) - (\mathrm{K_R} \cdot \mathrm{T}), \quad (5)$$

where Si, V, I, and T are densities of silicon, vacancy, interstitial, and trapped silicon, respectively. And R is the reaction rate representing the trapping on damage site. The Si-dopant diffusion is significantly suppressed in the N_2 ambient condition as shown in Fig. 2 and 3. Therefore, N_2 ambient condition is employed to minimize the redistribution of dopant in this work. In order to decrease the contact resistance by forming a contact at the peak doping position, anisotropic 70nm shallow etch is selectively conducted in the S/D access region (from -15 μm to -12 μm in the lateral position). And a 50-nm-thick Al_2O_3 layer is deposited to form the gate dielectric layer. Later, it is selectively etched for S/D contact opening. It is noted that deposition and etching processes are treated as purely geometric operations in this work.

Fig. 4 shows the final doping profile and device structure of the planar β-Ga_2O_3 MOSFET. The device has box-like doping profiles in S/D regions, which are enabled with N_2 ambient condition. The channel length is designed as 4 μm. Magenta lines represent contact surfaces. The doping density along the channel direction is shown in Fig. 5.

Device Simulation

The electrical characteristics of the β-Ga_2O_3 MOSFET are numerically simulated. A mesh suitable for the device simulation is generated, as shown in Fig. 6. The drift-diffusion simulation is performed. The doping dependent mobility model and the high-field saturation are considered. The model parameters are modified to have a maximum electron mobility of 130 cm^2/Vs [7]. In the semi-insulating substrate, an acceptor-like trap, whose energy level is 0.8eV away from the conduction band minimum [8], is introduced. The input and output characteristics are shown in Figs. 7 and 8, respectively. Contact resistance of 0.25 Ω · mm is applied to both sides of source and drain contacts. The simulated electron density profiles are shown in Fig 9 (a) and (b) at V_{GS} = 5 V, V_{DS} = 10 V and V_{GS} = 20V, V_{DS} = 10 V, respectively. It is noted that the device simulation can be robustly performed up to high bias voltages without any convergence problem.

Conclusions

In conclusion, the 2D β-Ga_2O_3 planar MOSFET has been successfully simulated with our in-house simulators. The developed simulation programs are applicable to optimize the process conditions and device structure of β-Ga_2O_3 power electronic devices.

References

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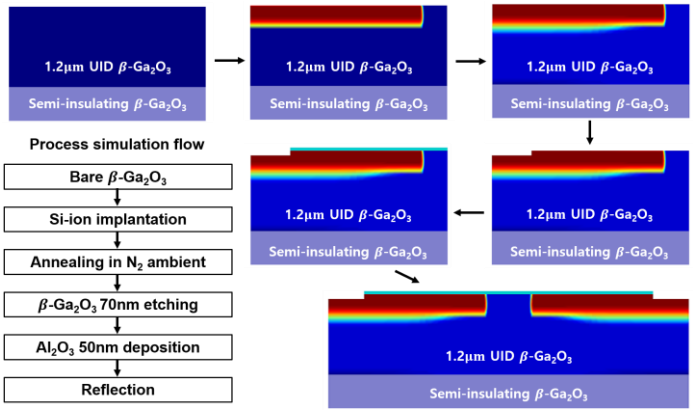

Fig. 1. 2D process simulation flow of planar β-Ga_2O_3 MOSFETs. The snapshot of doping profile and device structure is shown at each process step.

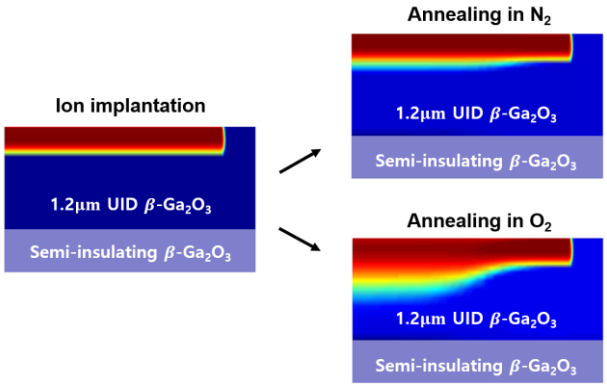

Fig. 2. 2D doping profile after ion implantation, annealing in each ambient N_2, O_2 for 60 s at 1100 ℃.

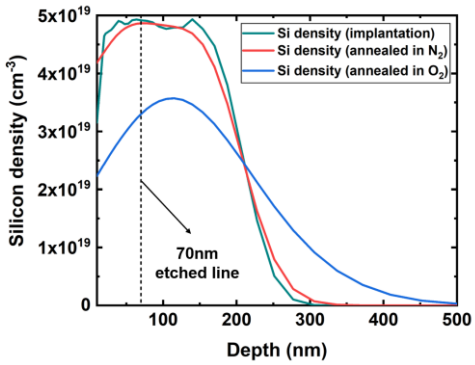

Fig. 3. Si dopant profile along the depth direction. The as-implanted profile and the profiles after diffusion under different ambient conditions are shown.

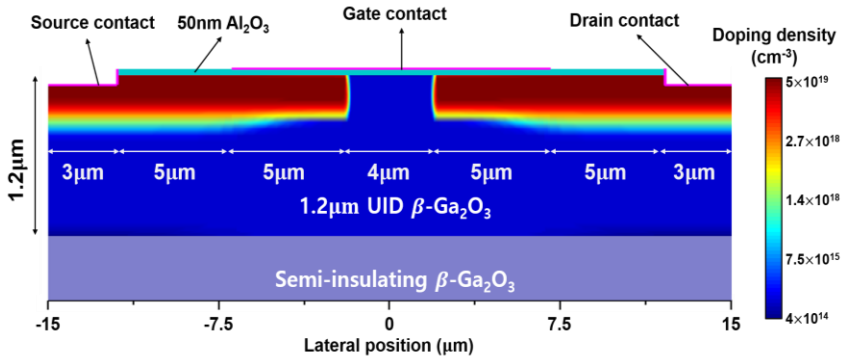

Fig. 4. Final 2D doping profile and device structure of the N_2-annealed β-Ga_2O_3 planar MOSFET generated by the process simulation program.

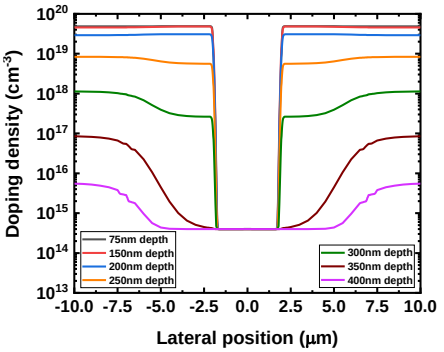

Fig. 5. Doping density along the lateral (channel) direction in the N_2-annealed β-Ga_2O_3 MOSFET. Various positions along the vertical direction are considered.

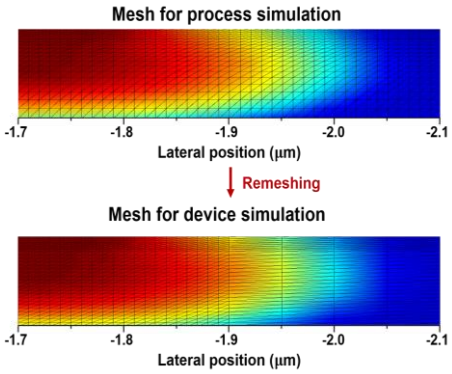

Fig. 6. Mesh refinement to generate mesh suitable for device simulation.

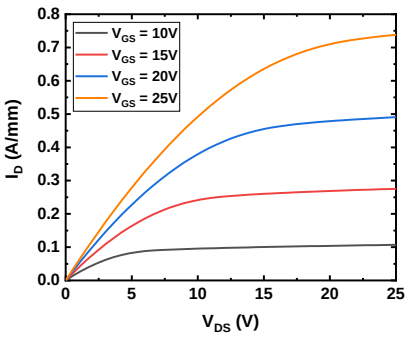

Fig. 7. DC output characteristics (I_D - V_{DS}) of the planar β-Ga_2O_3 MOSFET. V_{GS} varies from 10 V to 25 V with 5 V step.

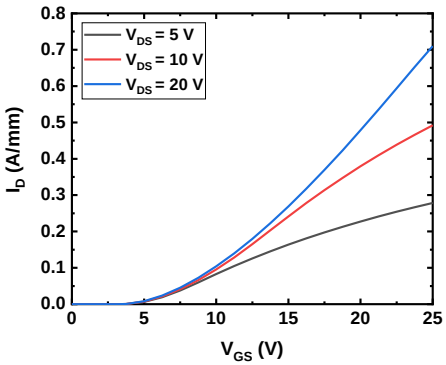

Fig. 8. DC input characteristics (I_D – V_{GS}) of the planar β-Ga_2O_3 MOSFET. V_{DS} varies from 5 V to 20 V.

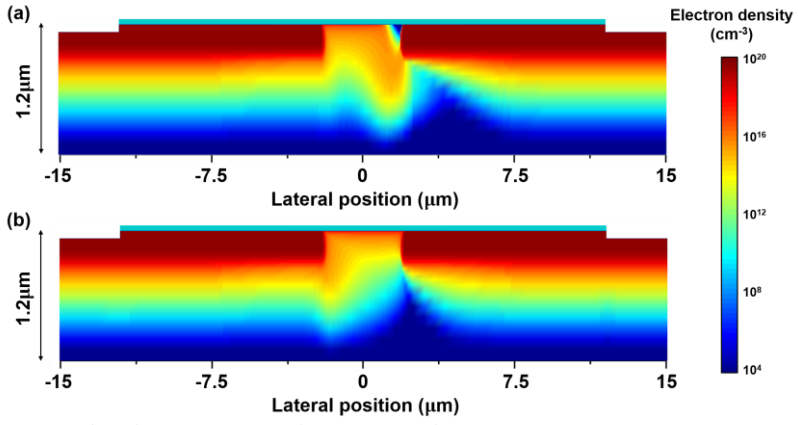

Fig. 9. 2D profile of electron density of the simulated β-Ga_2O_3 MOSFET. (a) V_{DS} = 10 V and V_{GS} = 5 V (b) V_{DS} = 10 V and V_{GS} = 20 V