VLSI Devices
Lecture 20

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Coverage

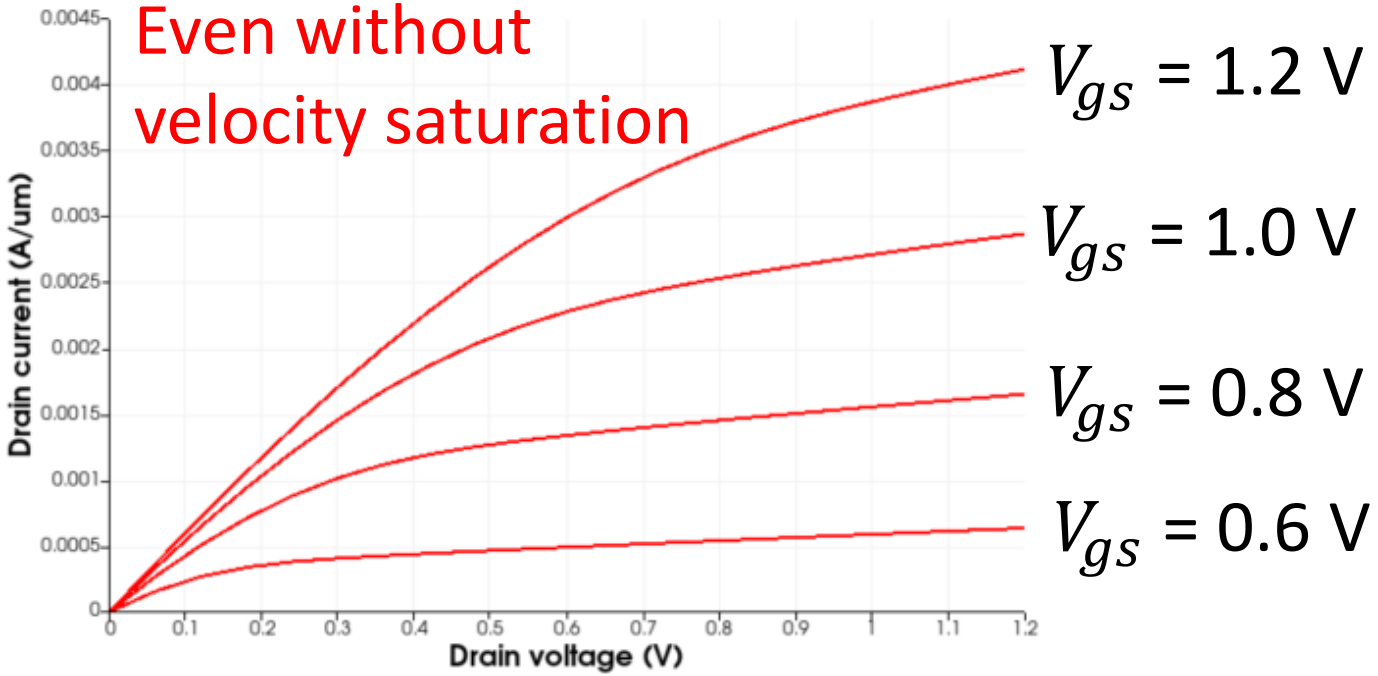
- Two YouTube lectures reserved for advanced topics
  - L14: ~~Substrate bias~~, ~~channel mobility~~
  - L15: ~~3.2.1~~
  - L16: ~~3.2.1 (Continued)~~
  - L17: ~~Velocity saturation (3.2.2)~~
  - L18: Channel length modulation and so on (3.2.3, 3.2.4, 3.2.5)
  - L19: MOSFET scaling
  - L20: MOSFET scaling (Continued)
  - L21: Quantum effect (4.2.4)
  - L22: Double-gate MOSFETs (10.3)
  - L23: FinFETs
  - L24: CFETs

Channel length modulation

- Gradual-channel approximation fails at the saturation point.
  - Distance between the saturation point and the drain, ΔL.
  - Drain current increases as

$$I_d = \frac{I_{dsat}}{1 - (\Delta L / L)}$$

Taur, Eq. (3.101)



Short-channel devices: TSMC 3 nm node

- IEDM 2022 (27.1)
  - DIBL versus L

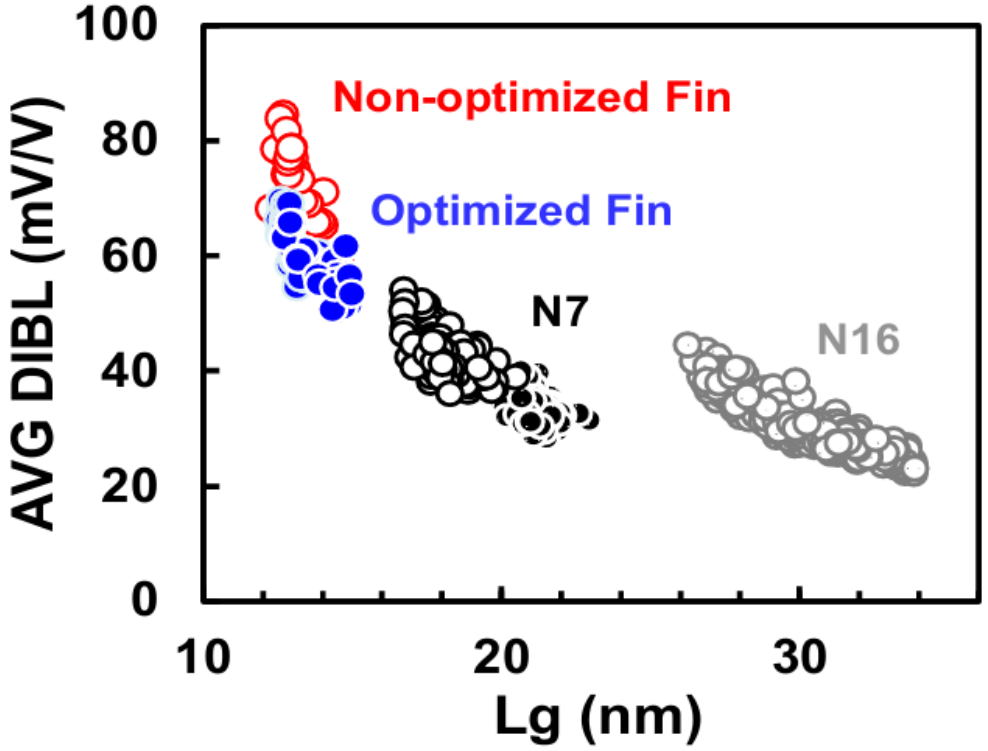


Fig.1 FinFET Lg scaling trend vs DIBL. Fin profile optimization is critical but is at the limit for further Lg scaling.

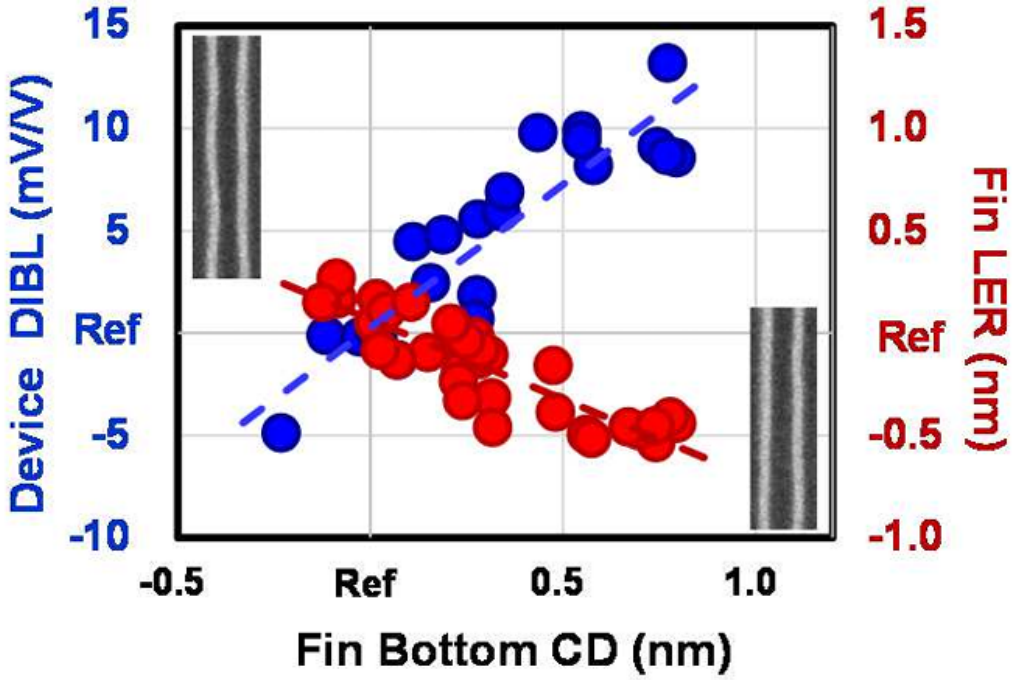


Fig.2 Smaller fin bottom CD reduces DIBL but degrades LER, which is an indicator of fin structural robustness and potential yield impact.

Source-drain series resistance

- Finite silicon resistivity + metal contact resistance
  - MOSFET channel resistance in the linear region

$$R_{ch} = \frac{V_{ds}}{I_d} = \frac{L}{\mu_{eff} C_{inv} W \left(V_{gs} - V_{on}\right)}$$

Taur, Eq. (3.102)

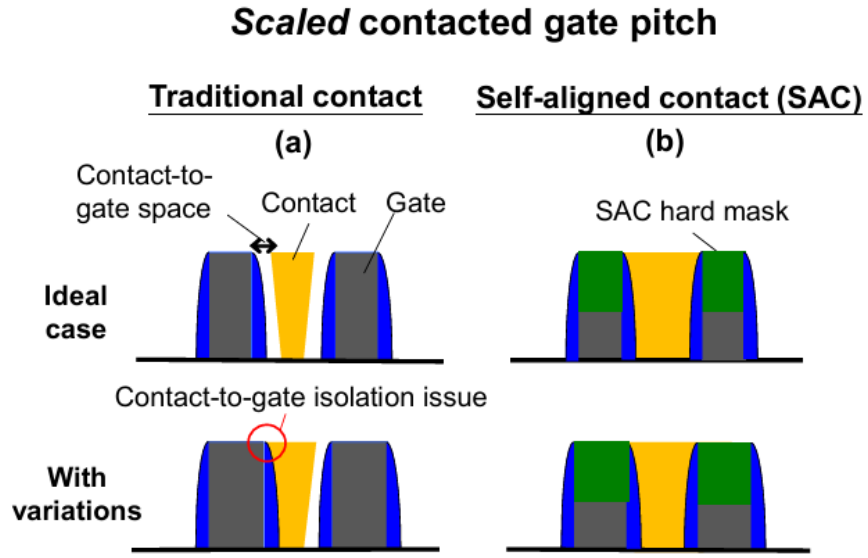
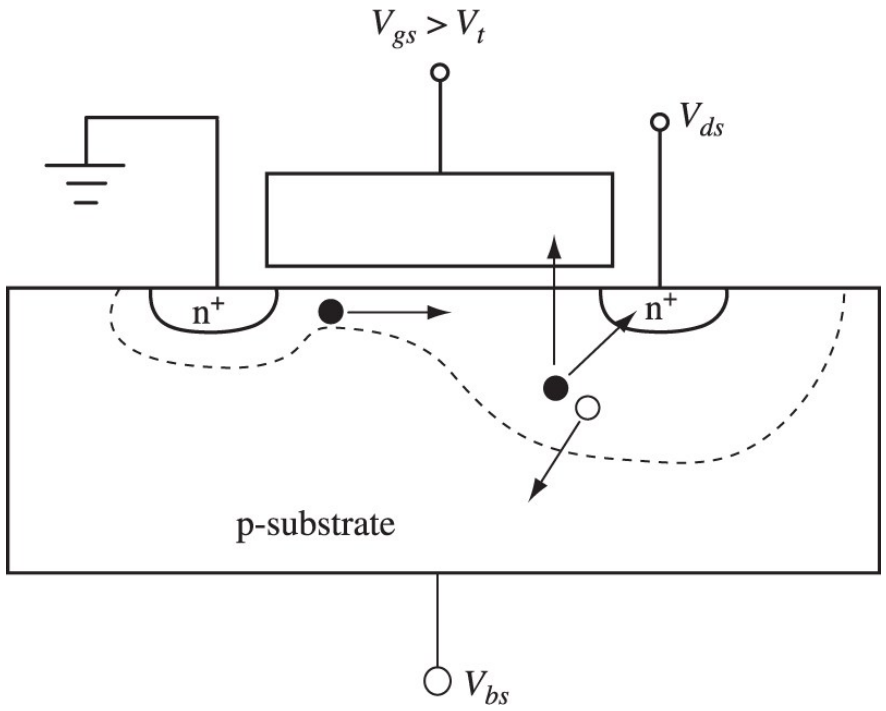


Fig.3 Contact schematics. Traditional contact (a) is vulnerable to variations induced contact-to-gate isolation issues compared to SAC (b).

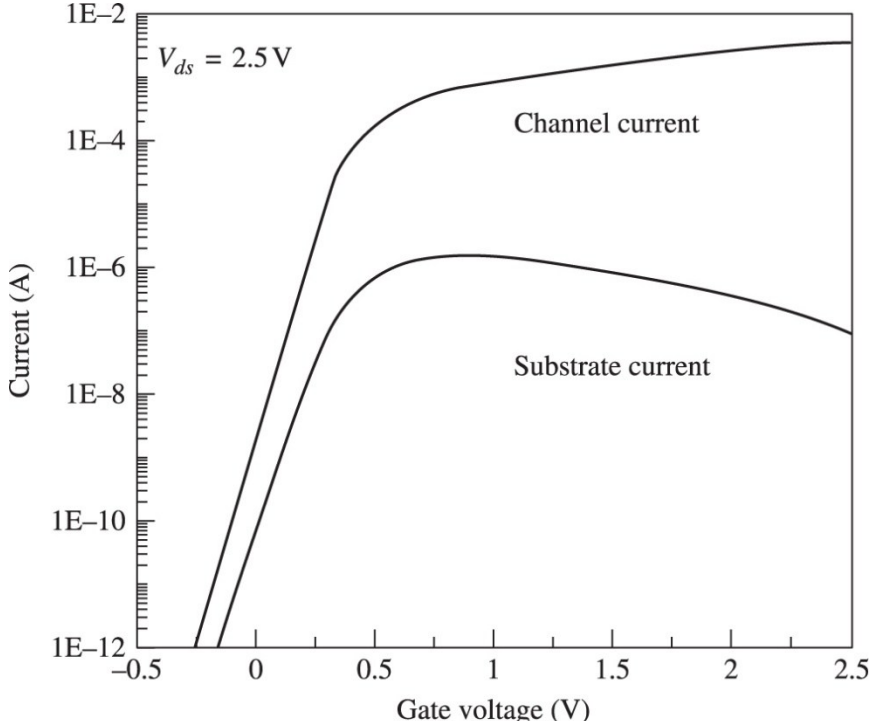
Self-aligned contact (TSMC, IEDM 2022)

Hot carrier effects

- Electrons gain energy from the electric field.
  - Injection into the SiO2 layer. Secondary electron/hole pair.
  - $V_{ds} - V_{dsat}$ is the voltage drop in the space-charge region.



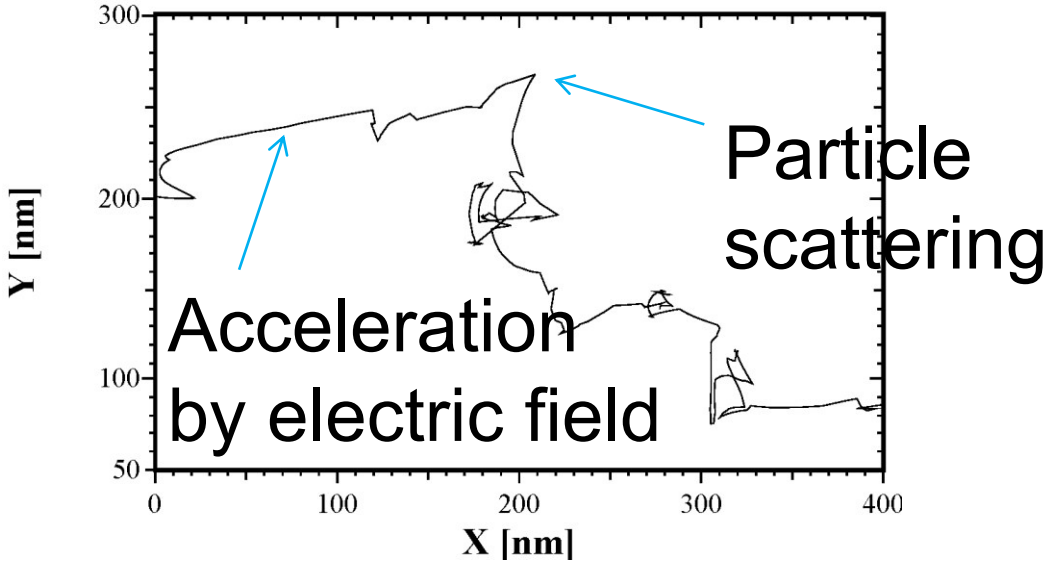
Channel hot-electron (Taur, Fig. 3.33)



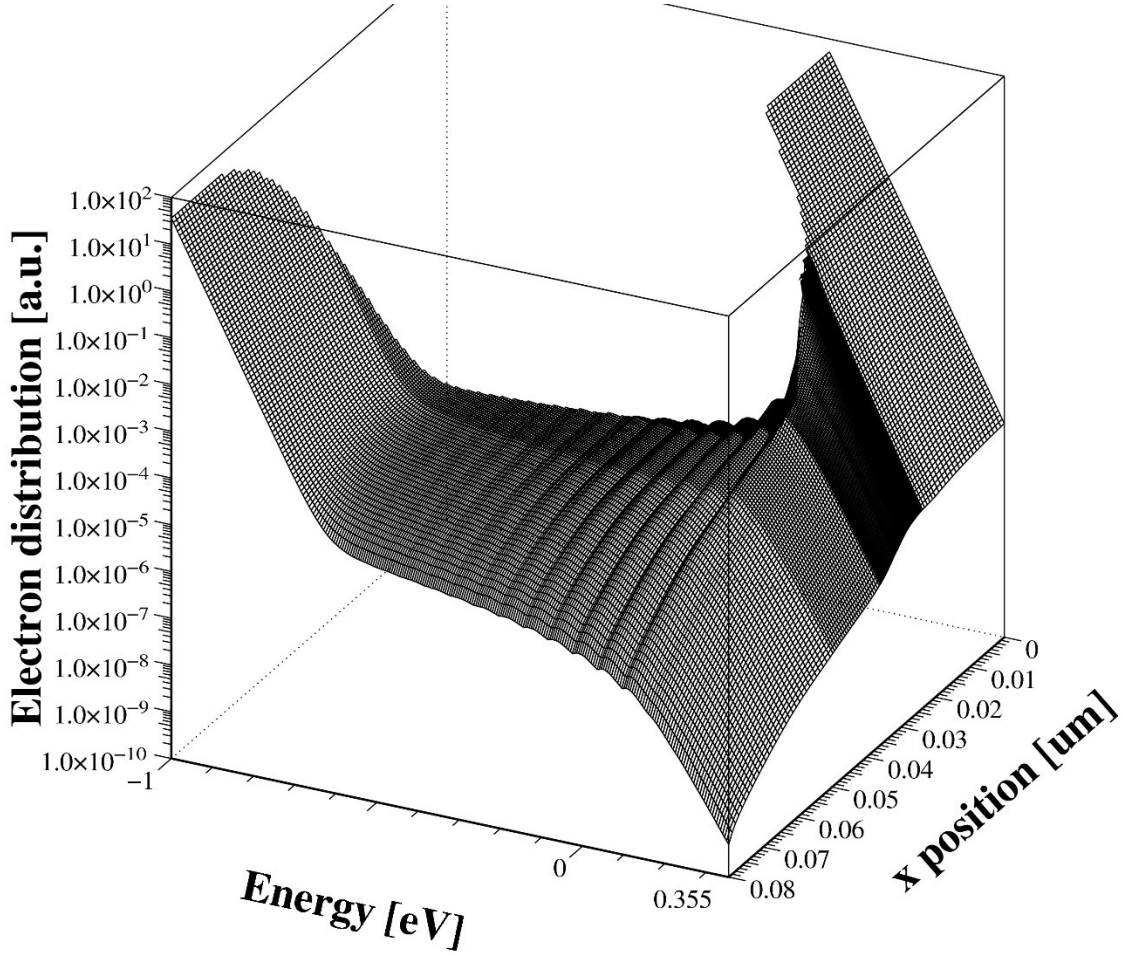
Substrate current (Taur, Fig. 3.34)

Energy distribution, $f(\mathbf{r}, E)$

- Key quantity to understand various effects
  - Various ways to model it
  - Boltzmann transport equation



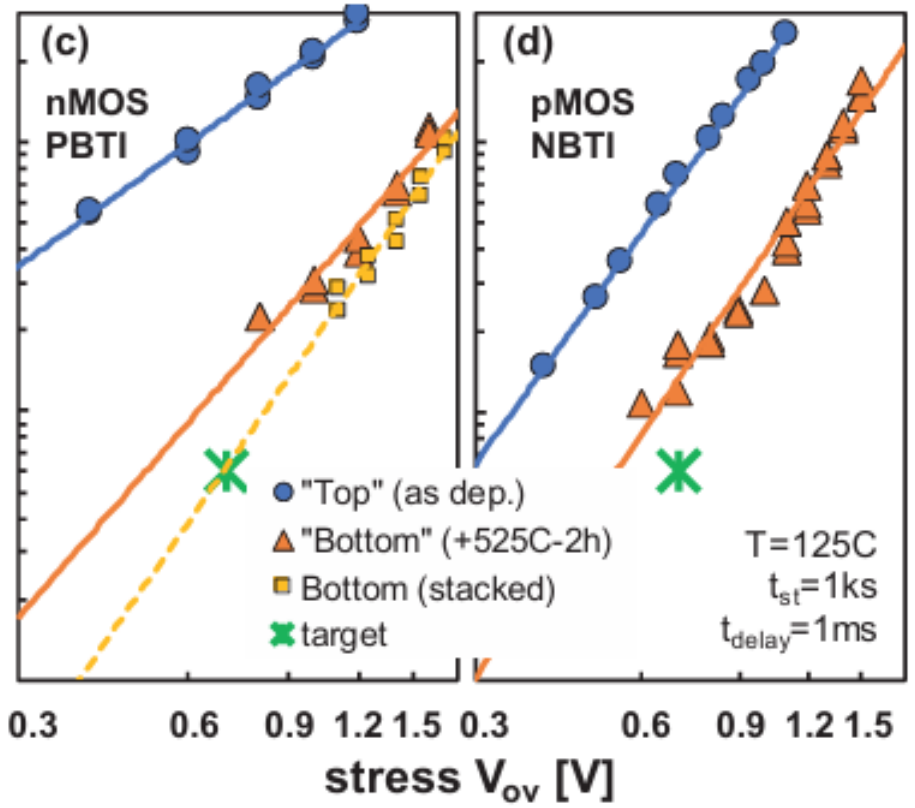
Stochastic electron motion simulated by Monte Carlo



Distribution function

BTI (Bias-Temperature Instability)

- Reliability issue (NBTI in PMOSFETs, PBTI in NMOSFETS)
  - Interface trap generation & $|V_t|$ shift

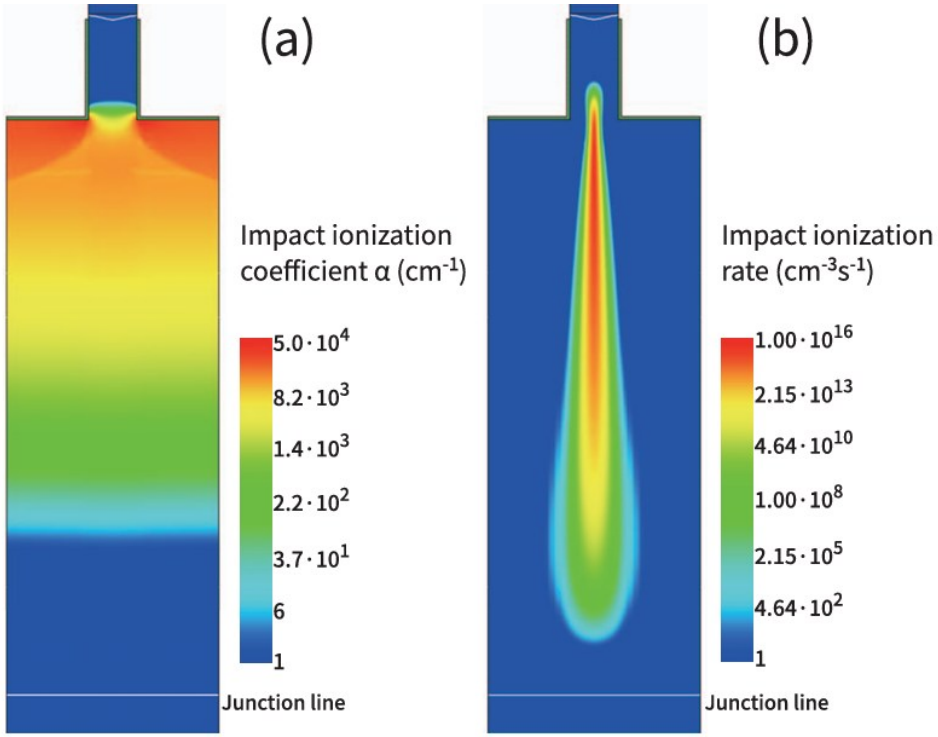


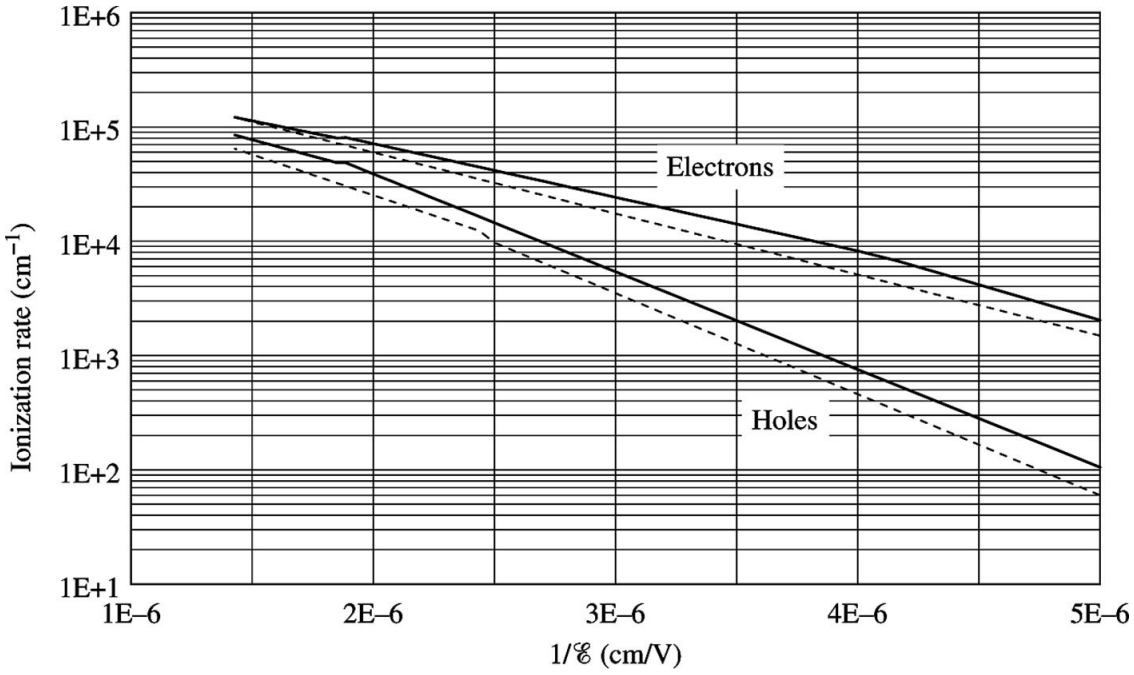
BTI characteristics of gate stacks (IMEC, IEDM 2018)

MOSFET breakdown

- Impact ionization
  - Strong dependence on $\mathcal{E}$

$$\alpha = A \exp\left(-\frac{b}{\mathcal{E}}\right)$$ Taur, Eq. (2.258)

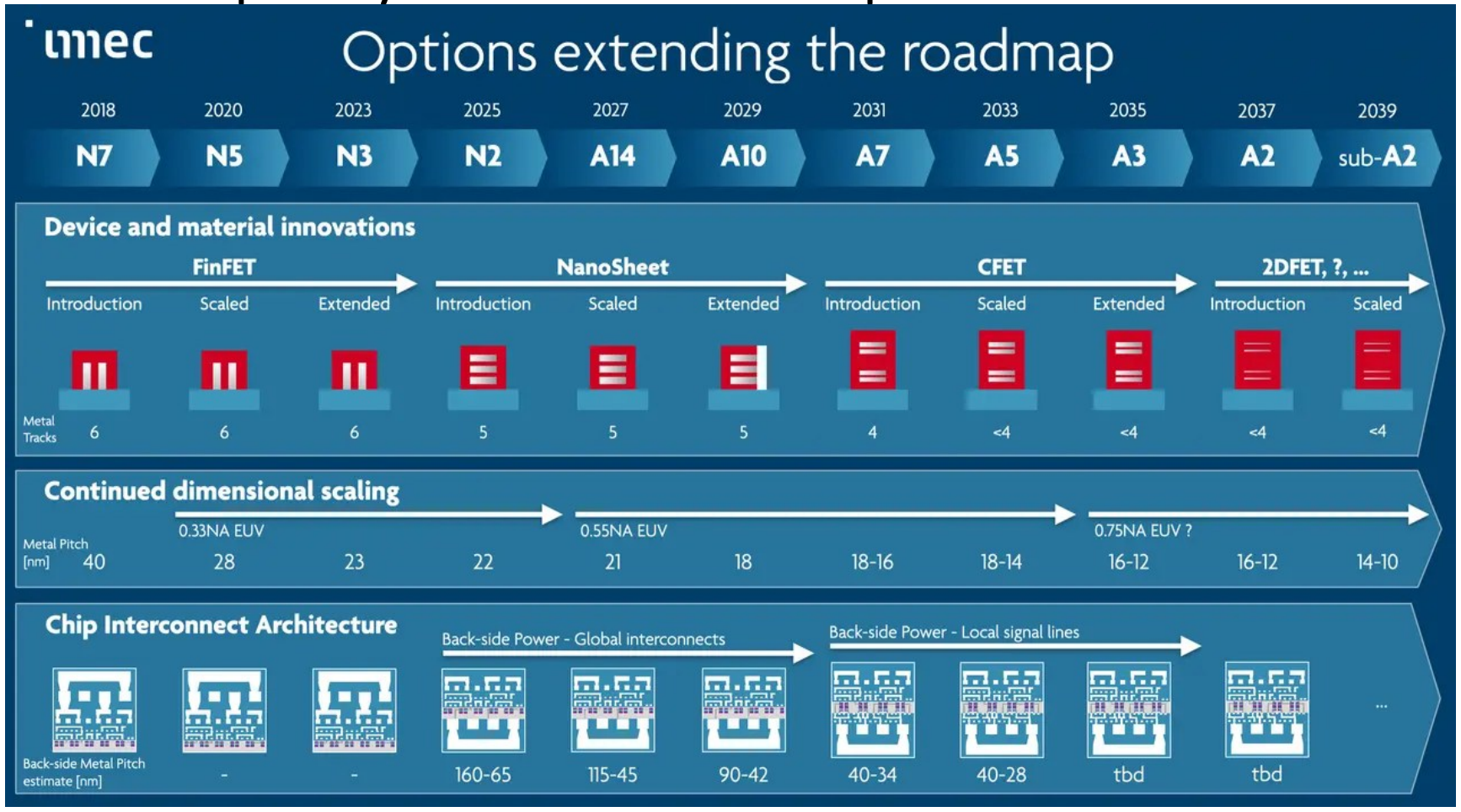




Impact ionization rates in silicon (Taur, Fig. 2.59)

MOSFET scaling

- First of all, we must understand the history. (~ 2011)
  - Comtemporary MOSFETs are not planar.



IMEC roadmap

Thank you!