VLSI Devices
Lecture 21

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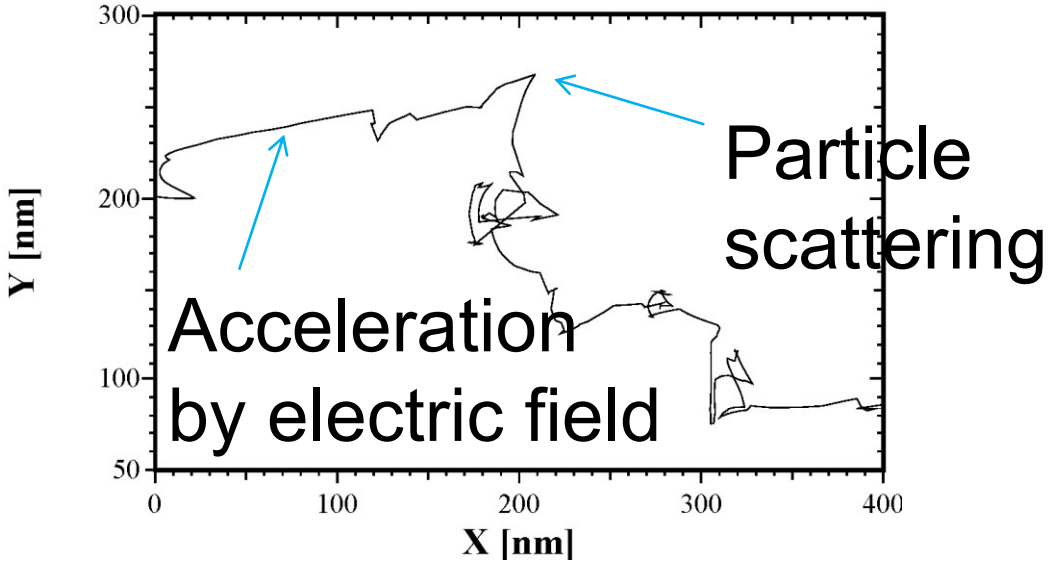
Coverage

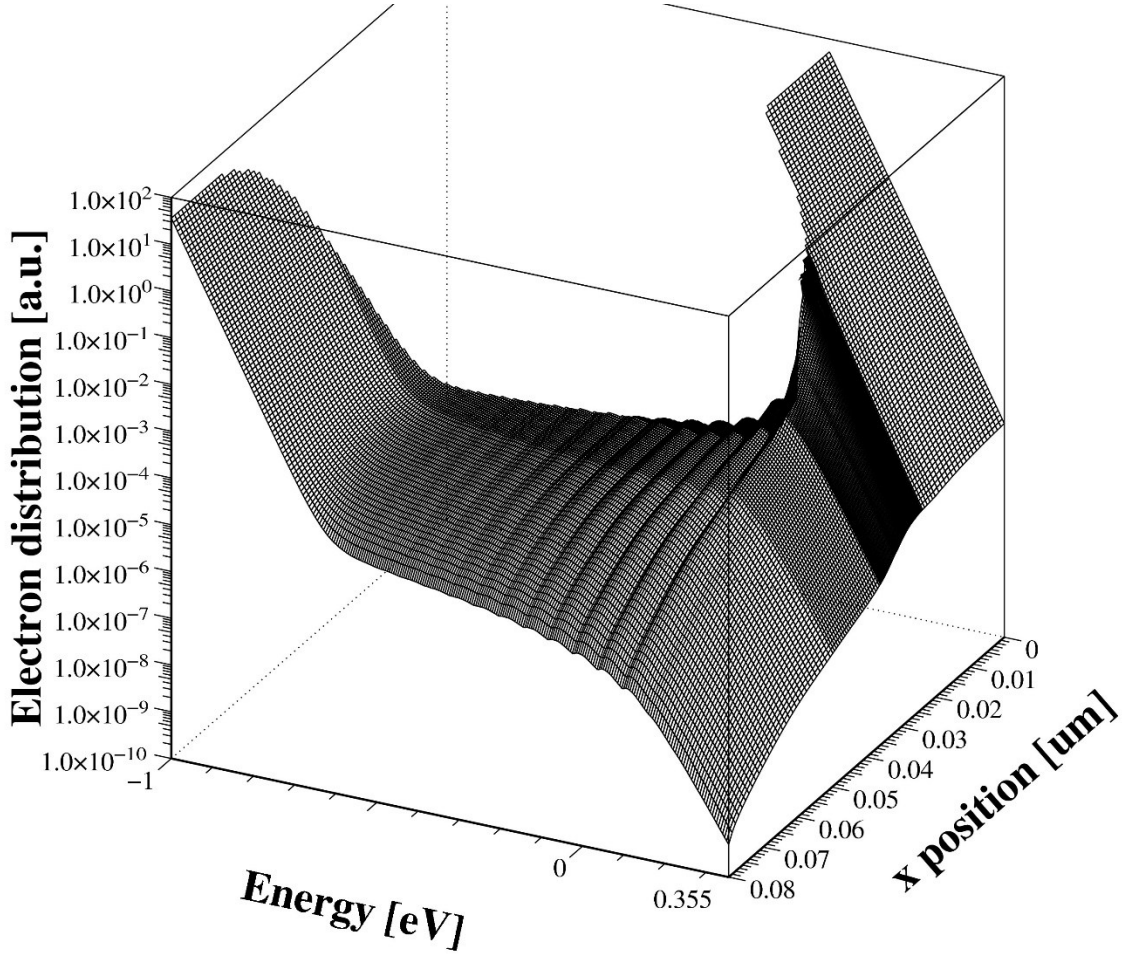
- Two YouTube lectures reserved for advanced topics
  - L14: ~~Substrate bias~~, ~~channel mobility~~
  - L15: ~~3.2.1~~
  - L16: ~~3.2.1 (Continued)~~
  - L17: ~~Velocity saturation (3.2.2)~~
  - L18: ~~Channel length modulation and so on (3.2.3, 3.2.4, 3.2.5)~~
  - L19: MOSFET scaling
  - L20: MOSFET scaling (Continued)
  - L21: Quantum effect (4.2.4)
  - L22: Double-gate MOSFETs (10.3)
  - L23: FinFETs
  - L24: CFETs

Energy distribution, $f(\mathbf{r}, E)$

- Key quantity to understand various effects
  - Various ways to model it
  - Boltzmann transport equation



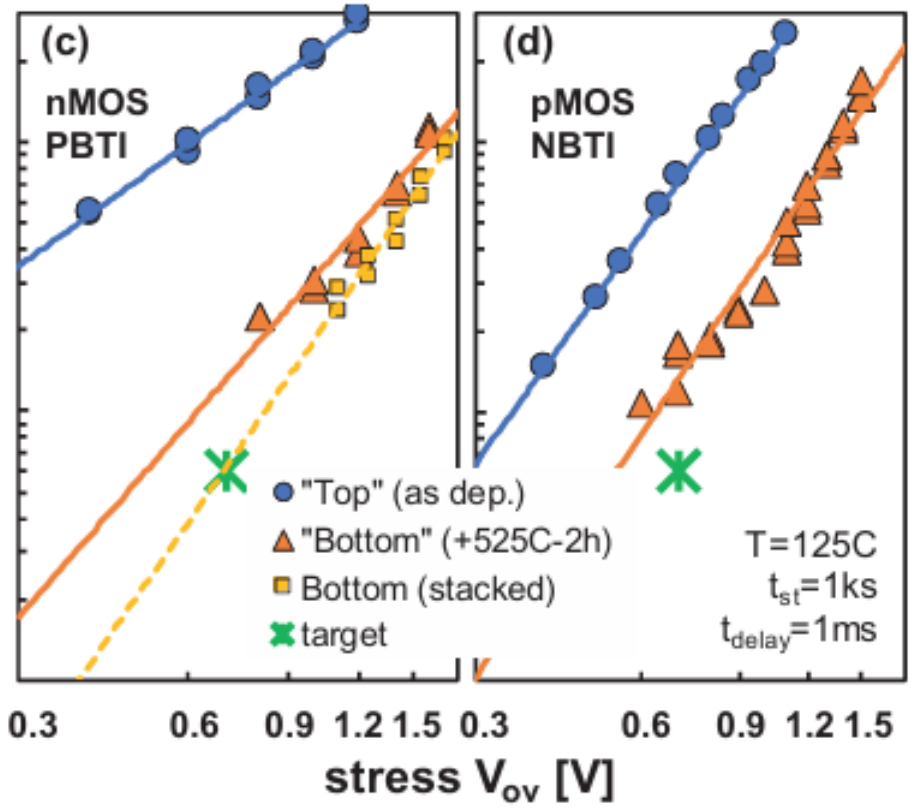
Stochastic electron motion simulated by Monte Carlo



Distribution function

BTI (Bias-Temperature Instability)

- Reliability issue (NBTI in PMOSFETs, PBTI in NMOSFETS)
  - Interface trap generation & $|V_t|$ shift

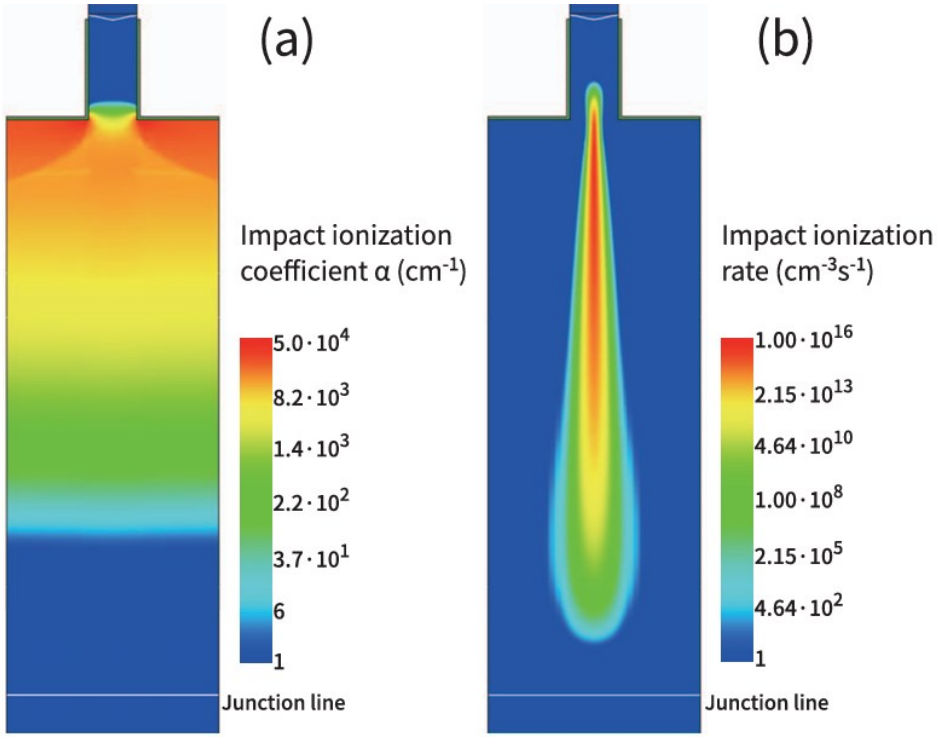


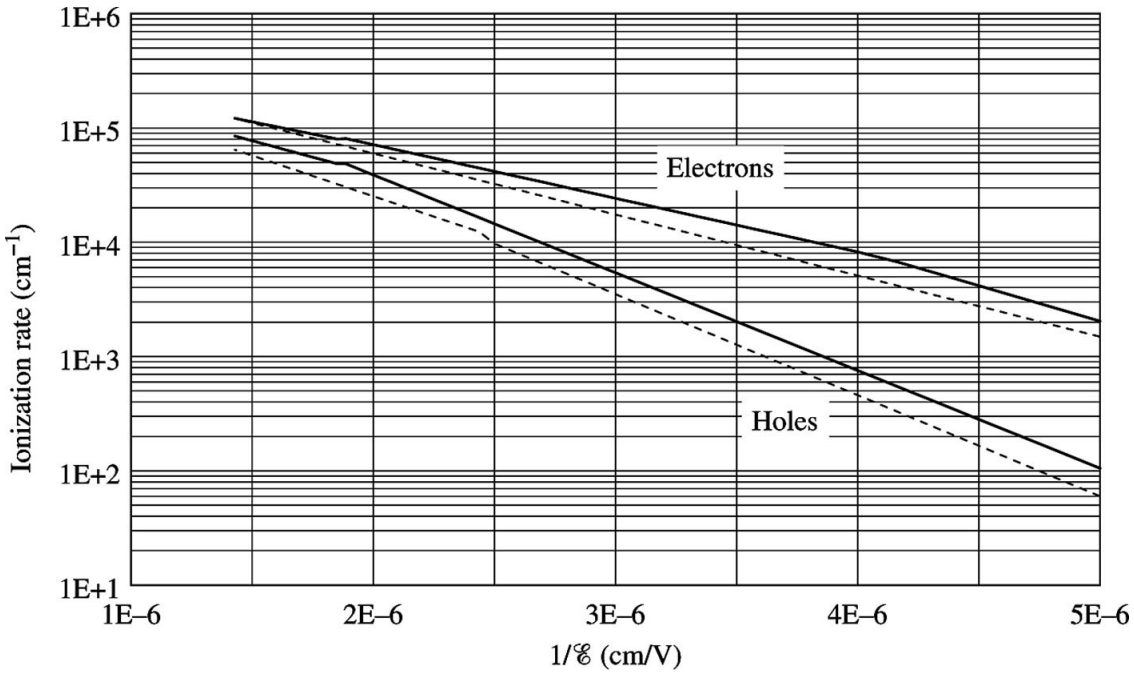
BTI characteristics of gate stacks (IMEC, IEDM 2018)

MOSFET breakdown

- Impact ionization
  - Strong dependence on $\mathcal{E}$

$$\alpha = A \exp\left(-\frac{b}{\mathcal{E}}\right)$$ Taur, Eq. (2.258)

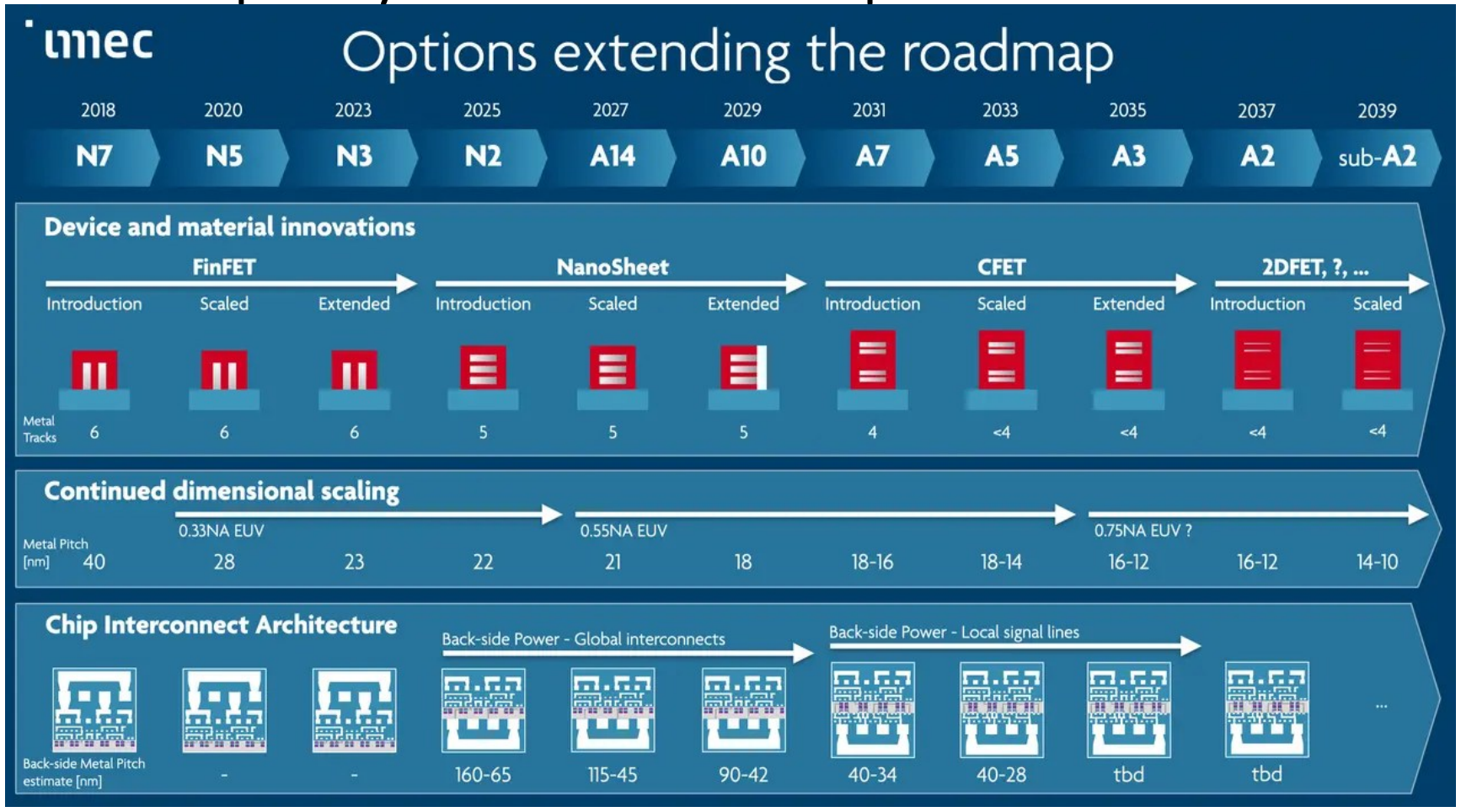




Impact ionization rates in silicon (Taur, Fig. 2.59)

MOSFET scaling

- First of all, we must understand the history. (~ 2011)
  - Comtemporary MOSFETs are not planar.



IMEC roadmap

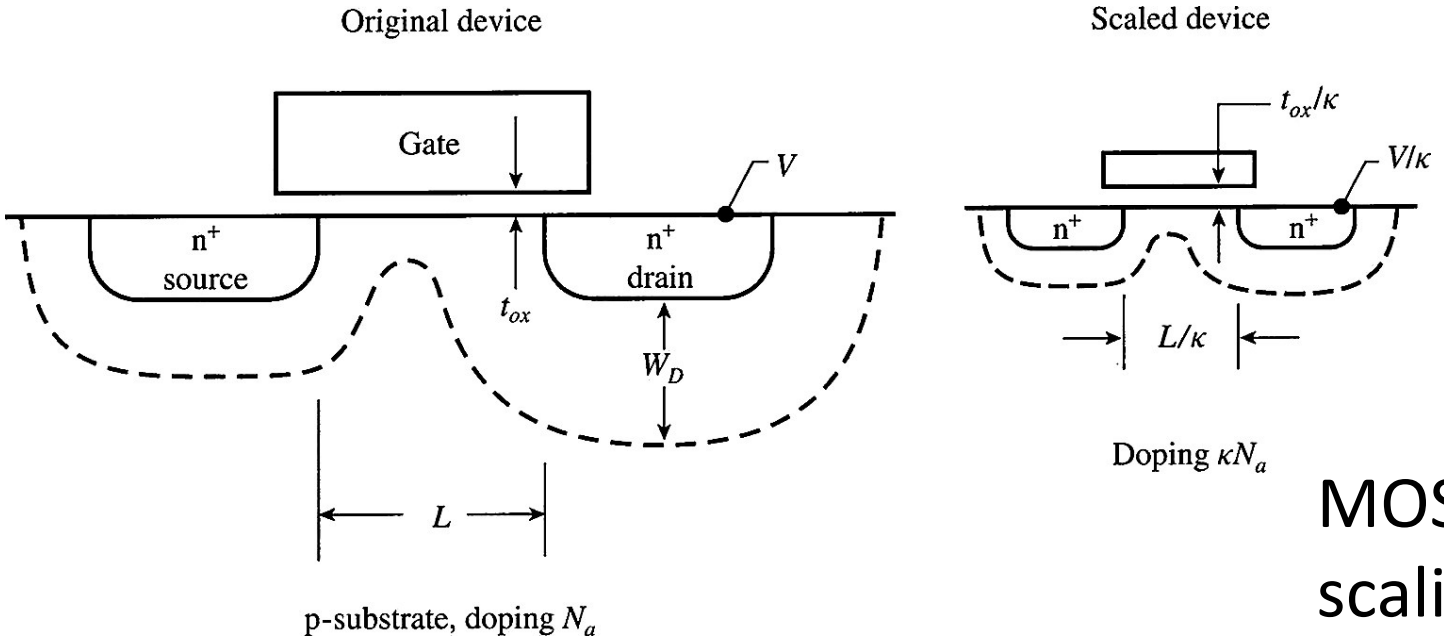
Basic assumptions

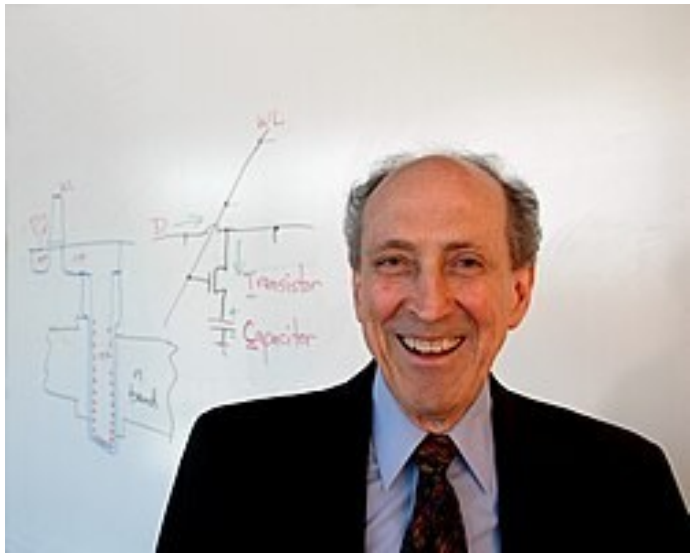
- High-resolution lithographic techniques (Minimum L)
- Technological advancement in ion implantation (Shallow junction)

An architect and a construction worker (Image generated by ChatGPT)

Constant-field scaling (Dennard scaling)

- Keep short-channel effects under control,
  - By scaling down the vertical dimensions along with the horizontal dimensions.
  - Decrease the applied voltage.
  - Increase the substrate doping concentration.





R. H. Dennard
(Inventor of DRAM)

MOSFET constant-electric-field scaling (Taur, Fig. 4.1)

Rules for constant-field scaling (1)

- Scaling assumption (κ>1)
  - Device dimensions (t_{ox}, L, W, and x_j): $1/\kappa$
  - Doping concentration (N_a and N_d): κ
  - Voltage (V): $1/\kappa$
- Maximum drain depletion width

$$W_D = \sqrt{\frac{2\epsilon_{si}(\phi_{bi}+V_{dd})}{qN_a}} \rightarrow \sqrt{\frac{2\epsilon_{si}\left(\phi_{bi}+\frac{1}{\kappa}V_{dd}\right)}{q\kappa N_a}} \qquad \text{Taur, Eq. (4.1)}$$

$$\approx \frac{1}{\kappa}\sqrt{\frac{2\epsilon_{si}(\phi_{bi}+V_{dd})}{qN_a}} = \frac{1}{\kappa}W_D$$

Rules for constant-field scaling (2)

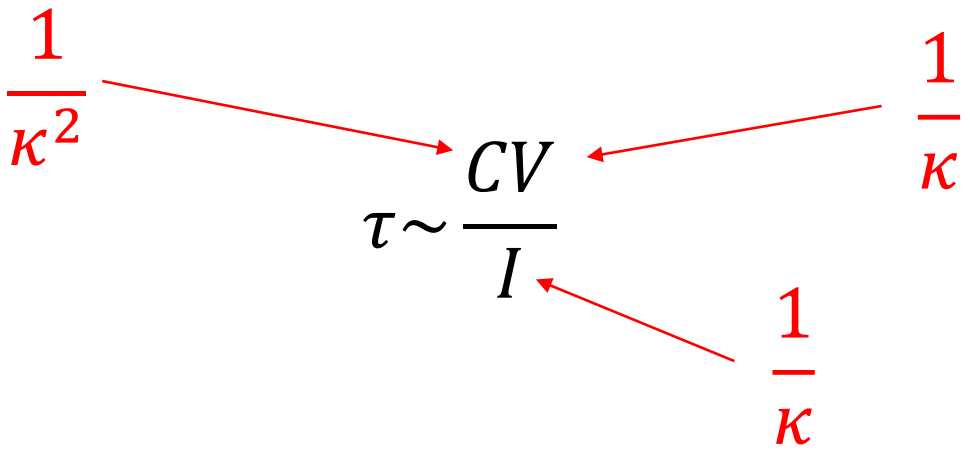
- Capacitances
  - They scale down by κ.
- Charge per device ($\sim C \times V$)
  - It scaled down by κ^2.
- Drain current
  - The original one

$$I_d = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_t)V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

$$\mu_n \kappa C_{ox} \frac{\frac{1}{\kappa}W}{\frac{1}{\kappa}L}\left[\left(\frac{1}{\kappa}V_{gs} - \boldsymbol{V_{t,scaled}}\right)\frac{1}{\kappa}V_{ds} - \frac{1}{2}\frac{1}{\kappa^2}V_{ds}^2\right] \approx \frac{1}{\kappa}I_d$$

Effect of scaling on circuit parameters

- Important colcusion of constant-field scaling:
  - Once the device dimensions and the power-supply voltage are scaled down, the circuit speeds up by the same factor.



  - Moreover, power dissipation per circuit, which is proportional to VI, is reduced by κ^2.

Thank you!