VLSI Devices
Lecture 15

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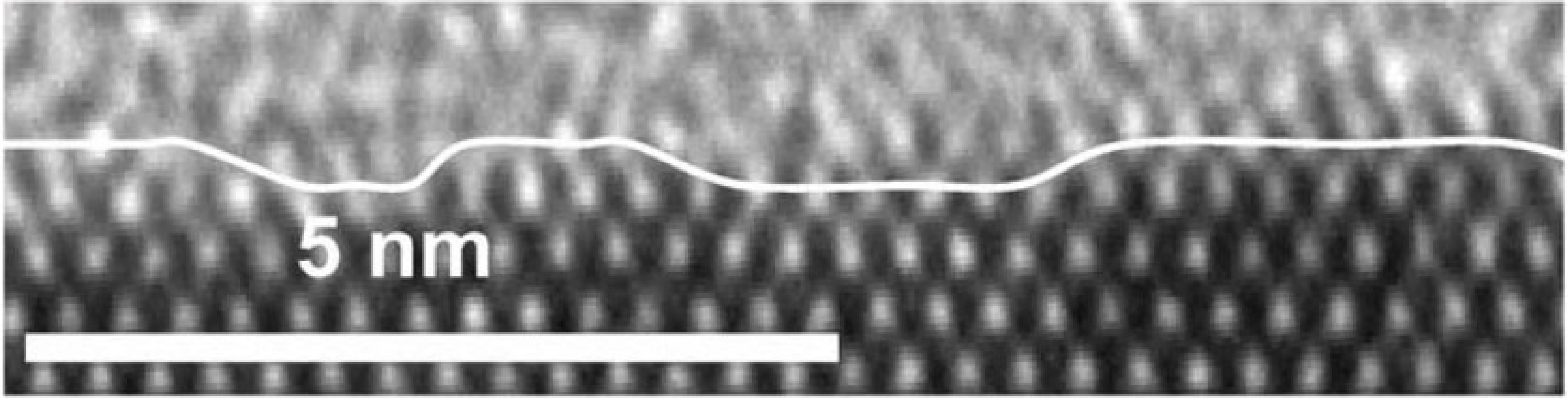
Coverage

- Two YouTube lectures reserved for advanced topics
  - L14: ~~Substrate bias~~, channel mobility
  - L15: 3.2.1
  - L16: 3.2.1 (Continued)
  - L17: Velocity saturation (3.2.2)
  - L18: Channel length modulation and so on (3.2.3, 3.2.4, 3.2.5)
  - L19: MOSFET scaling
  - L20: MOSFET scaling (Continued)
  - L21: Quantum effect (4.2.4)
  - L22: Double-gate MOSFETs (10.3)
  - L23: FinFETs
  - L24: CFETs

Rough surface

- High-resolution TEM image of SiO_2/Si interface
  - How can we characterize the roughness? Autocorrleation function, $\Delta(r)$. Usually, $\Delta^2 \exp\left(-\frac{r^2}{\Lambda^2}\right)$ or $\Delta^2 \exp\left(-\frac{r}{\Lambda}\right)$



HRTEM image (Prof. Shinichi Takagi's group, IEEE TED, 2010)

Effective mobility against effective field

- Effective field
  - Average electric field perpendicular to the Si-SiO$_2$ interface experienced by the carriers in the channel

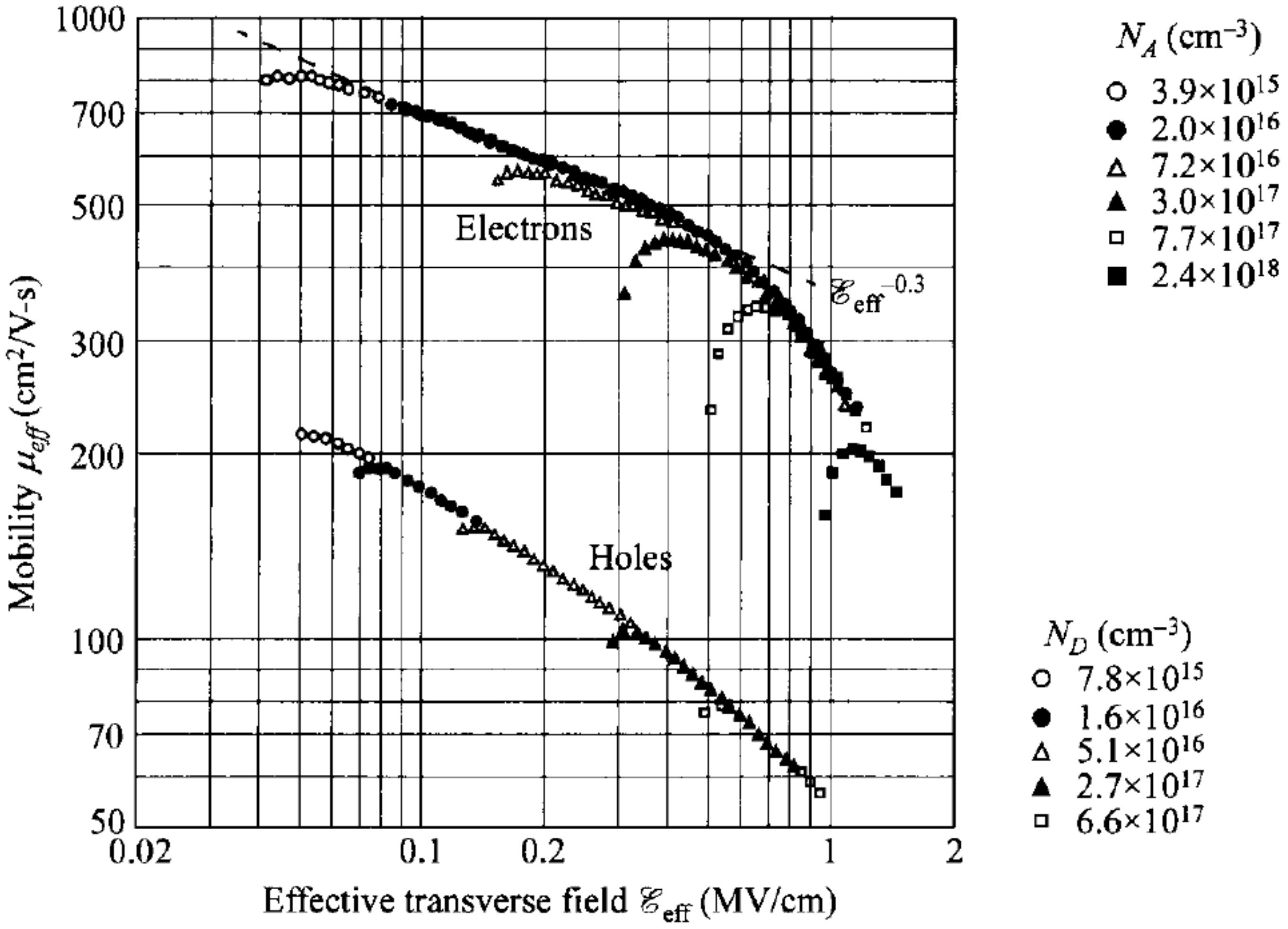
$$\mathcal{E}_{eff} = \frac{1}{\epsilon_{si}}\left(|Q_d| + \frac{1}{2}|Q_i|\right) \qquad \text{Taur, Eq. (3.51)}$$

  - Using $|Q_d| \approx C_{ox}(V_t - V_{fb} - 2\phi_B)$ and $|Q_i| \approx C_{ox}(V_{gs} - V_t)$,

$$\mathcal{E}_{eff} = \frac{V_t - V_{fb} - 2\phi_B}{3t_{ox}} + \frac{V_{gs} - V_t}{6t_{ox}} \qquad \text{Taur, Eq. (3.53)}$$

Mobility variation

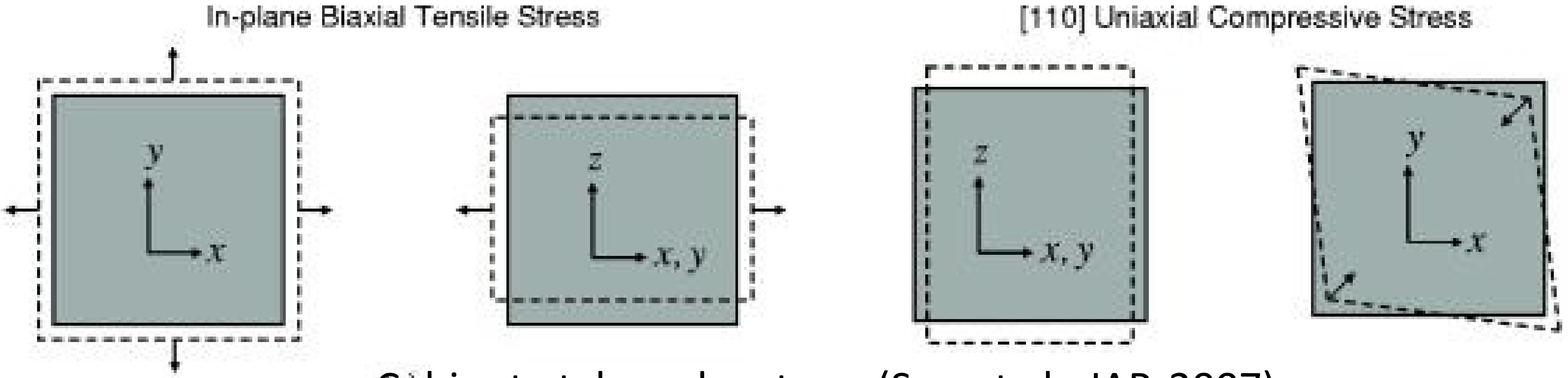
- Mobility variation (Vertical field dependence)



Inversion-layer mobility (Sze's book)

Strain effect on mobility

- Default wafer orientation is in the (001) plane.
  - In-plane biaxial tensile stress: NMOSFET
  - [110] uniaxial compressive stress: PMOSFET
  - Overall, the VLSI industry has utilized strain to gain about 10~25 % on the drive current of NMOSFET and 50 % or more on the drive current of PMOSFET.

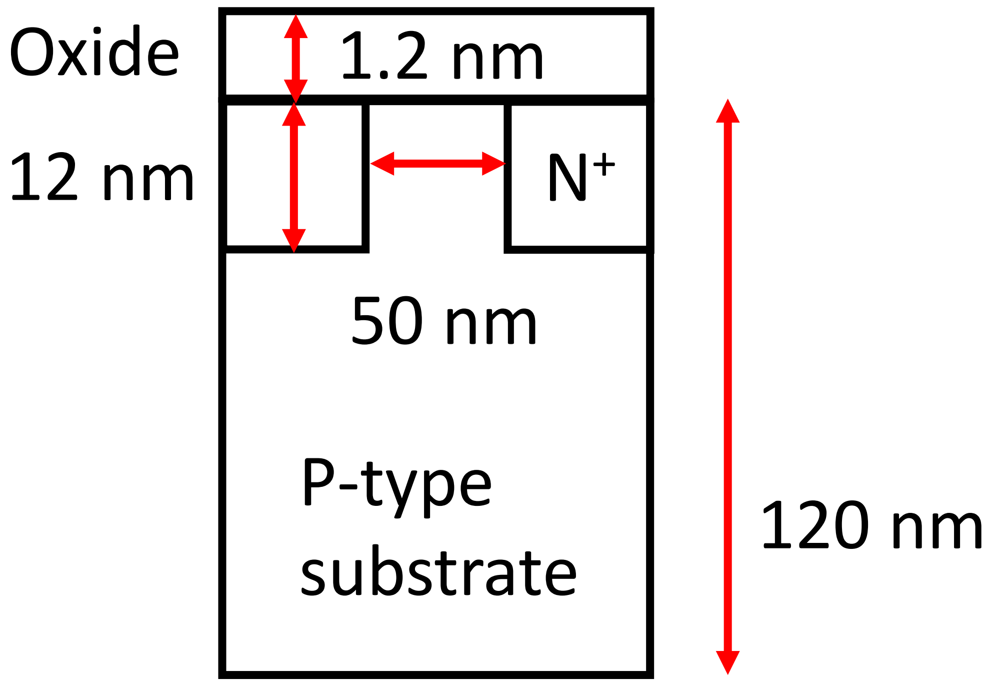


Cubic ctrstals under stress (Sun et al., JAP, 2007)

Model planar MOSFET

- Effective oxide thickness of 1.2 nm
  - Gate workfunction of 4.3 eV
  - Substrate doping of 1.5X10^{18} cm^{-3}
  - V_{DD} of 1.2 V

- Channel length of 50 nm
  - Comparison with 1 μm device

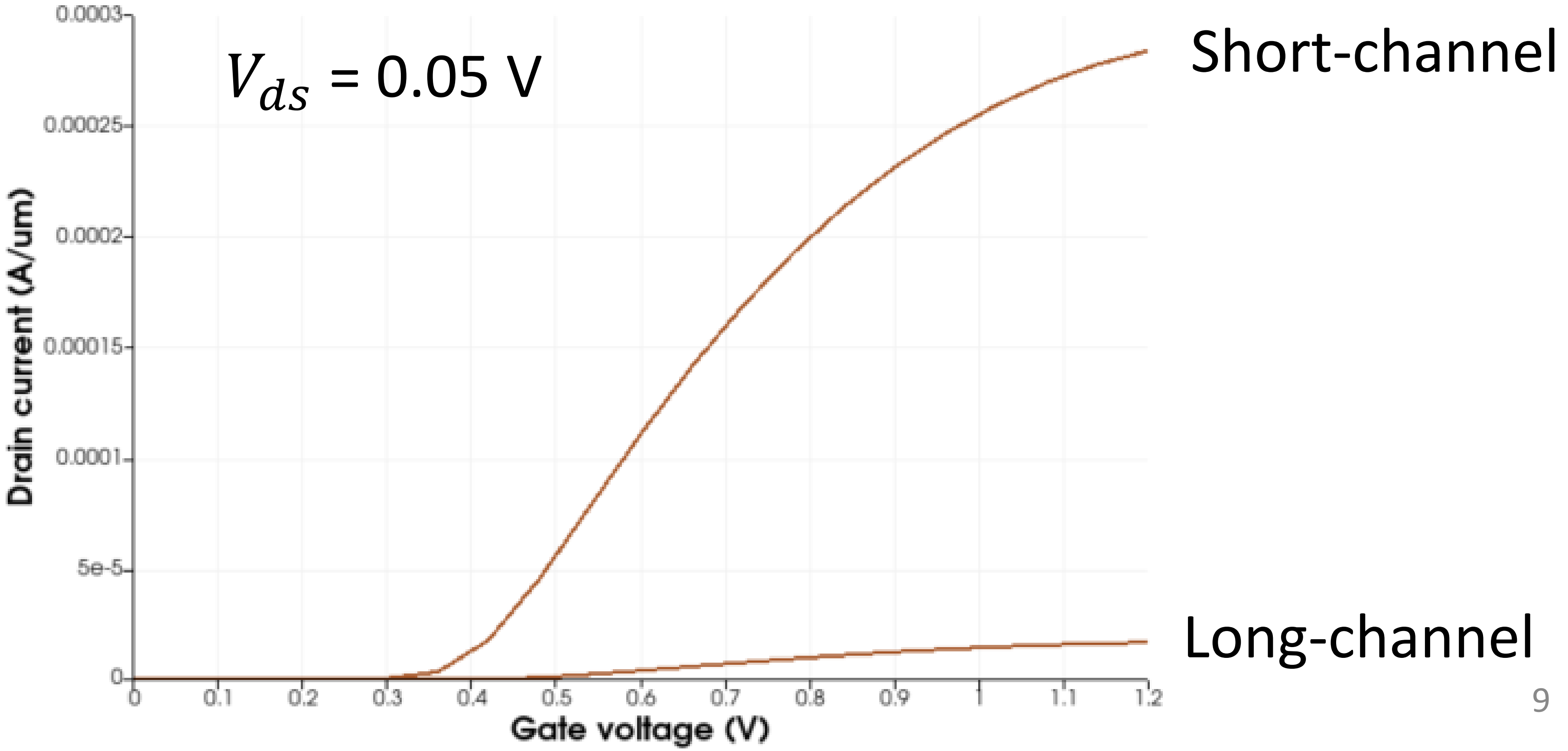


Short and long structures

- Drawn in the same scale

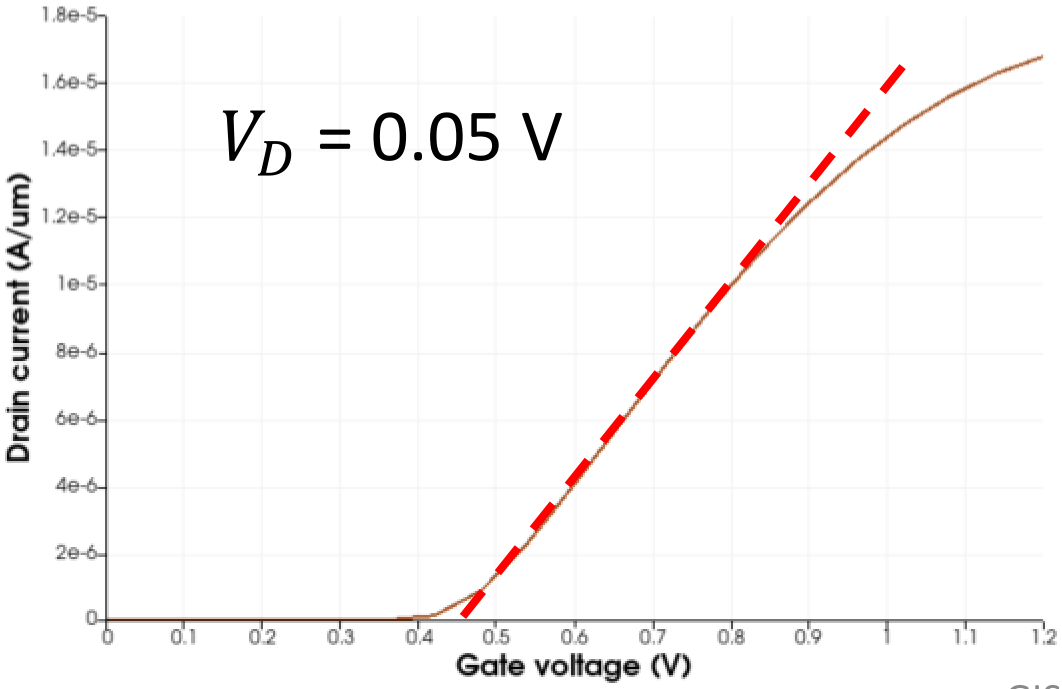
Input characteristics

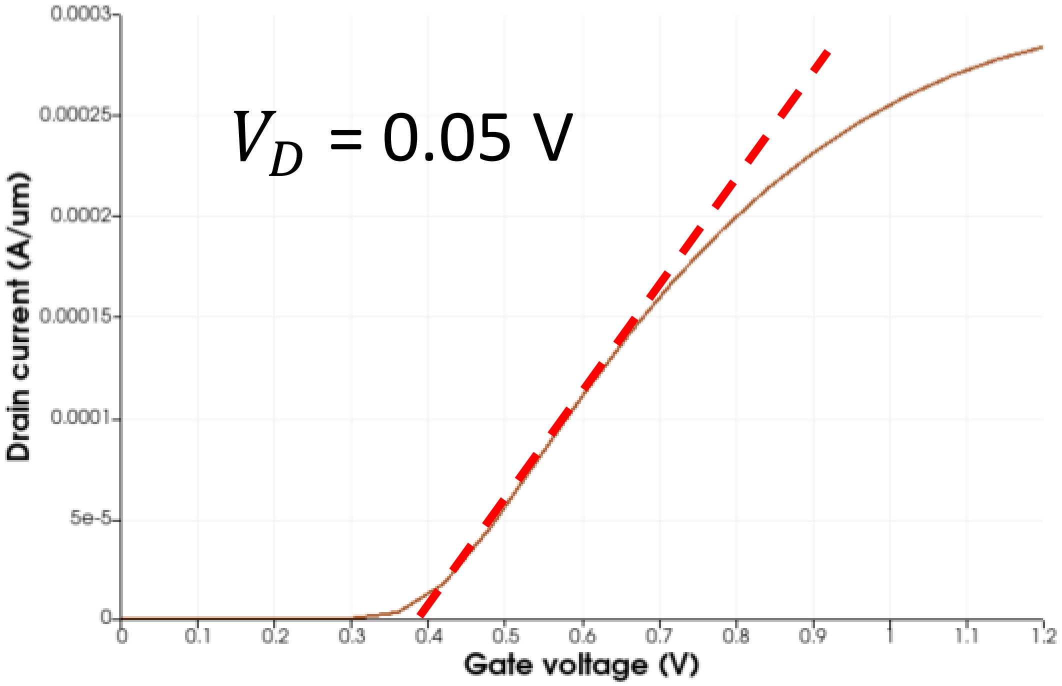
- Physical models included
  - Note that $I_D \propto \frac{1}{L}$.



Reduction of V_t, even at a low V_{ds}

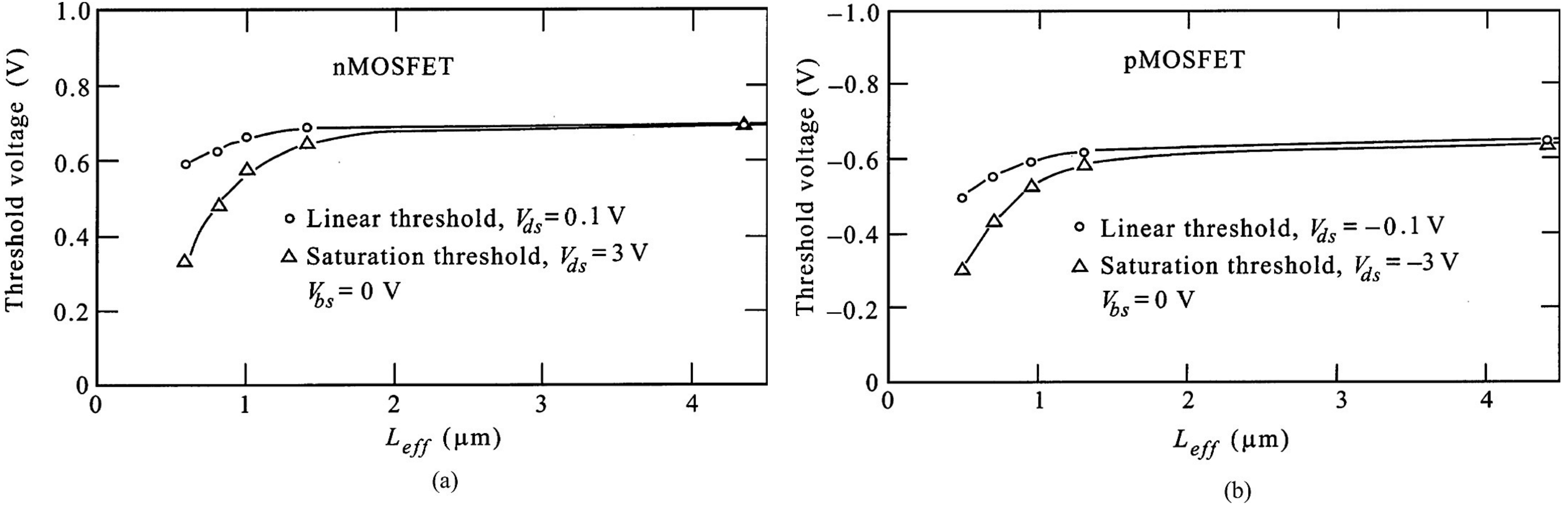
- For a short-channel device, the threshold voltage decreases.
  - ~ 0.45 V (Long-channel)
  - ~ 0.4 V (Short-channel)
  - Why?





V_t as a function of L

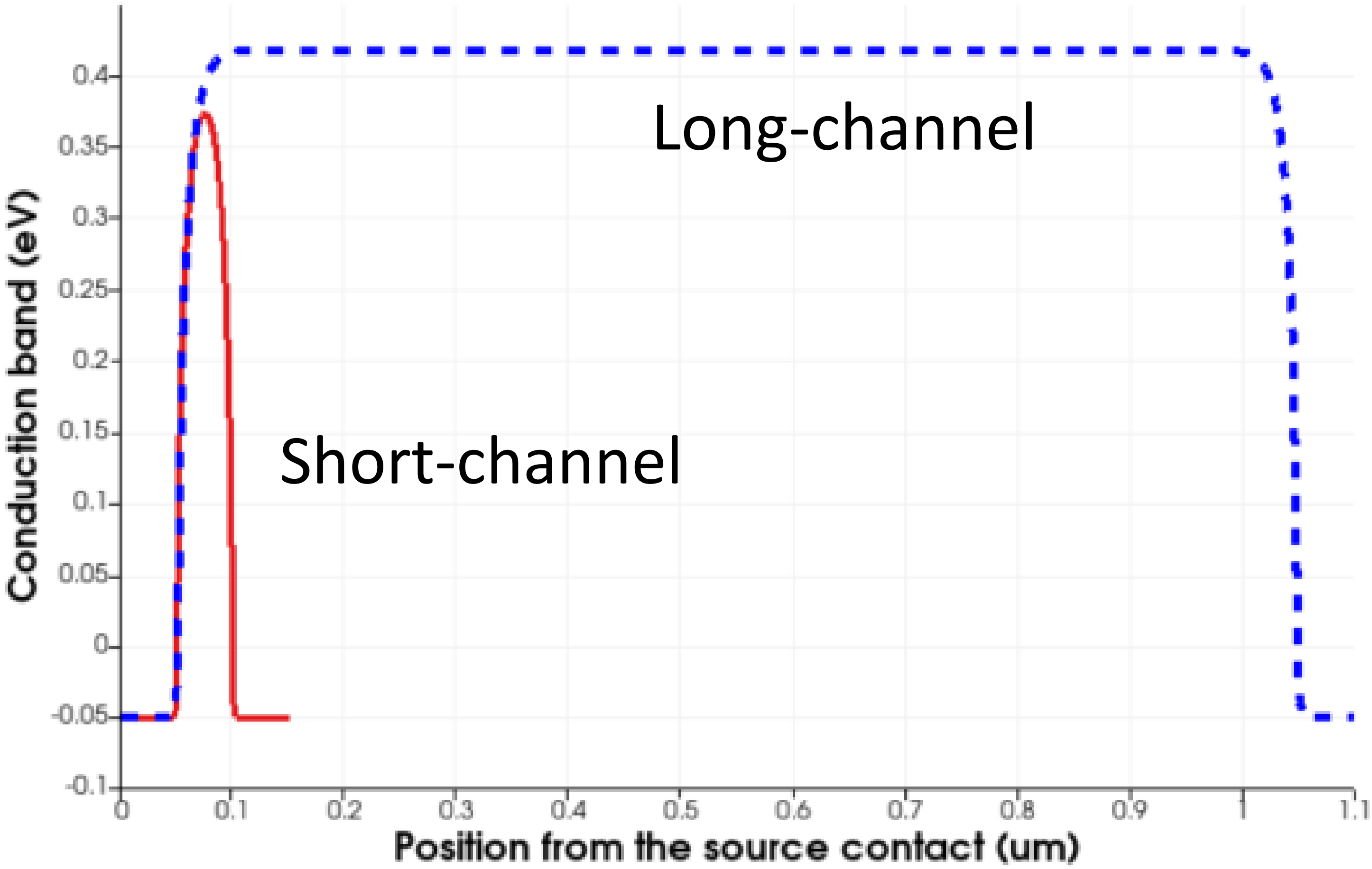
- Short-Channel Effect (SCE) = Decrease of V_t as the channel length is reduced



Short-channel threshold rolloff (Taur, Fig. 3.19)

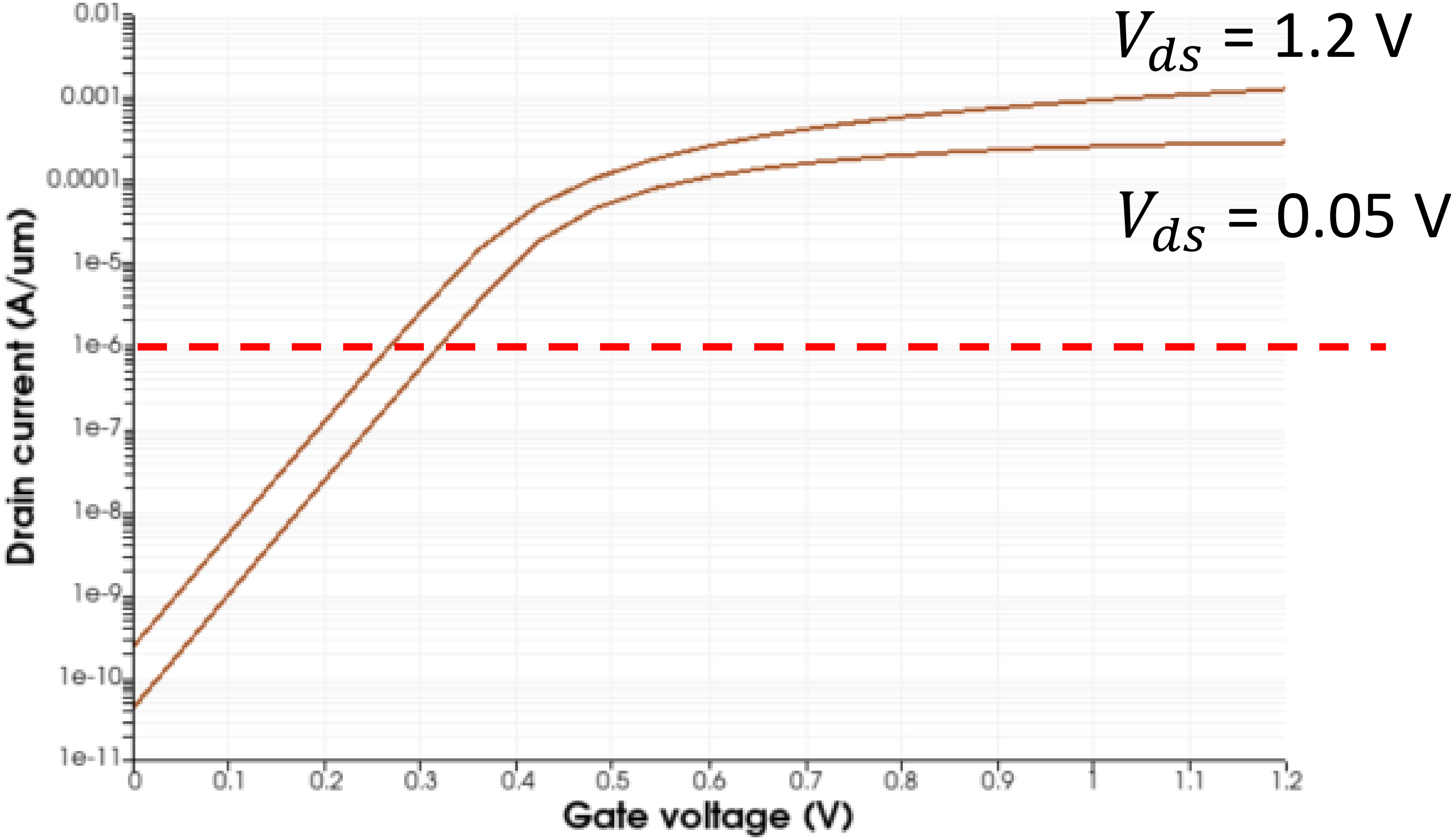
Charge sharing

- Even at V_{gs} = V_{ds} = 0 V, the conduction band profiles are different.



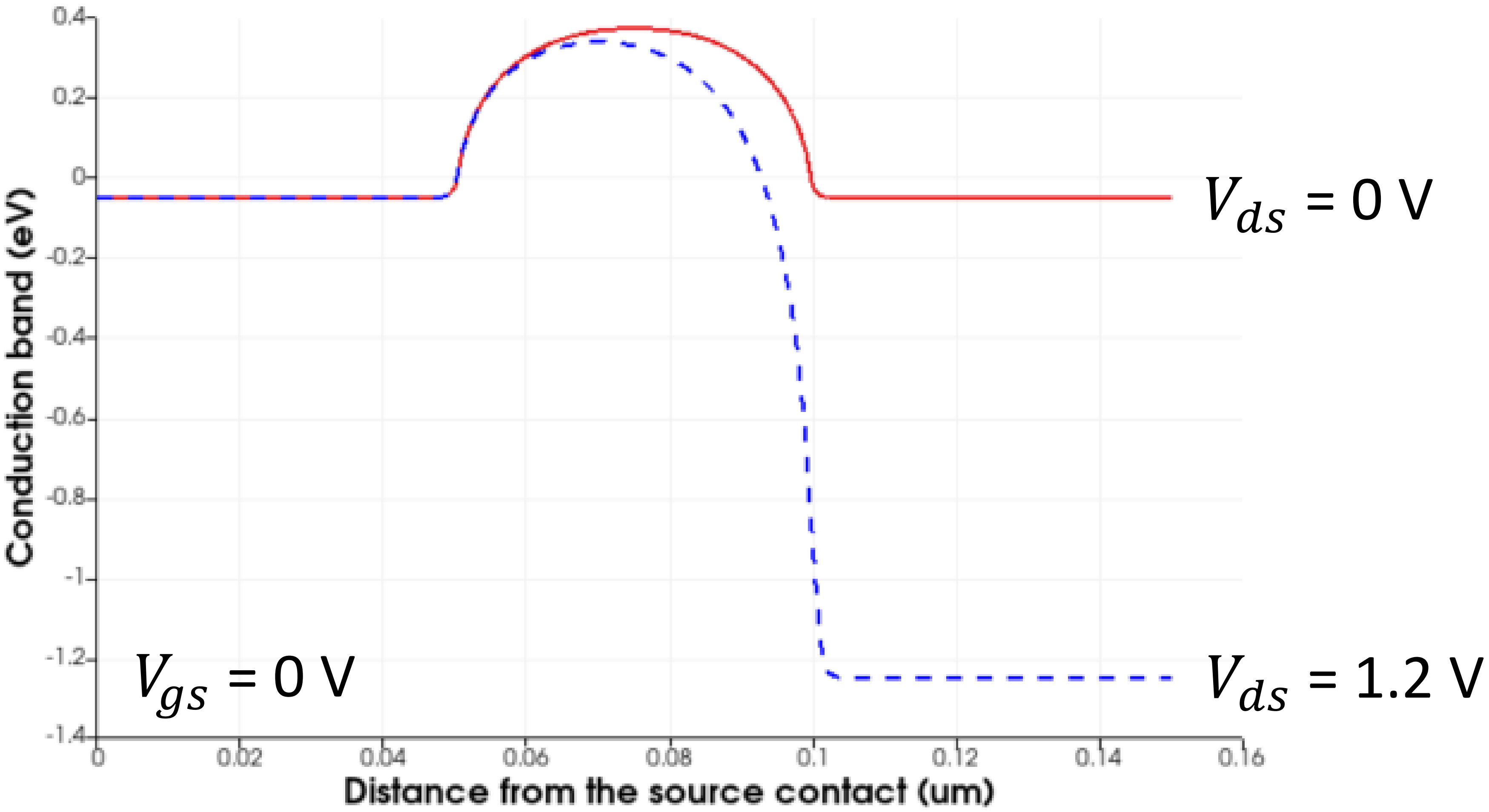
Drain-induced barrier lowering (DIBL)

- Much worse than the long-channel device
  - 45 mV/V @ I_D = 10^{-6} A/μm



Conduction band, again

- At a high V_{ds}, the energy barrier is further reduced.



Simplified geometry for an analytic solution

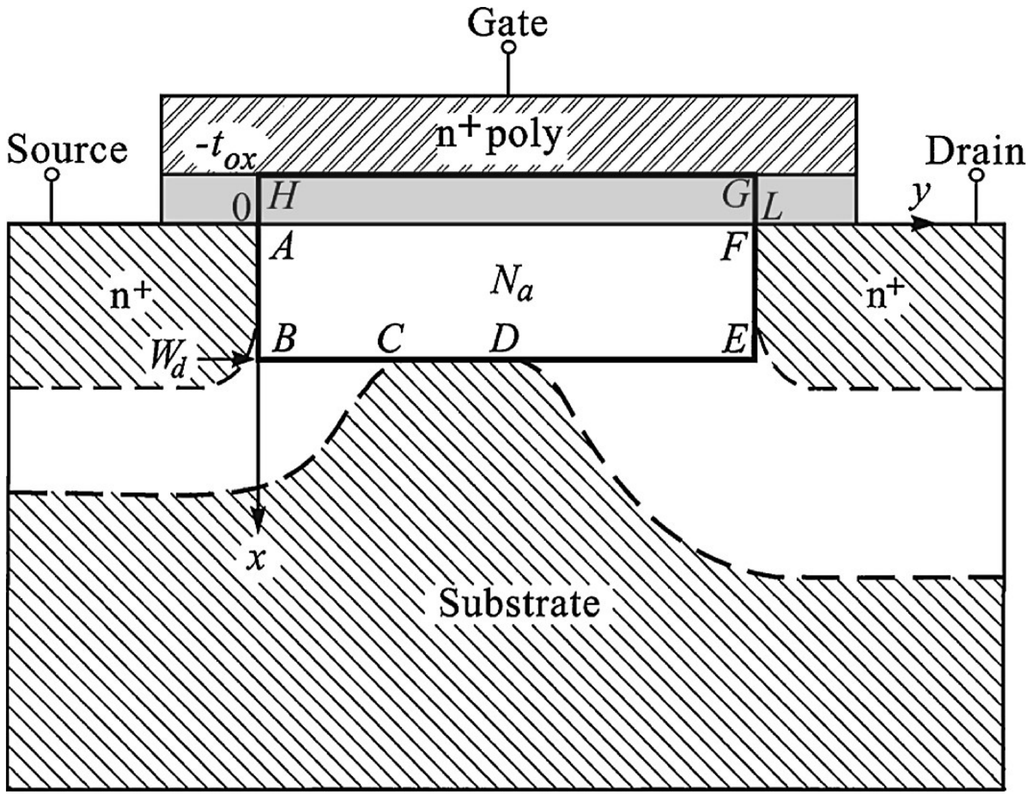
- Poisson equation
  - For AFGH

$$\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2}=0 \quad \text{Taur, Eq. (A9.1)}$$

  - For ABEF

$$\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2}=\frac{qN_a}{\epsilon_{si}}$$

Taur, Eq. (A9.2)



Simplified geometry (Taur, Fig. A9.1)

Thank you!