VLSI Devices

Lecture 1

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Course

- Course number: EC4313 (SE3101)
- Credits: 3
- Schedule: 09:00~10:15 every Monday/Wednesday
- Instructor: Sung-Min Hong

Prerequiste and references

- Semiconductor Materials and Devices (EC3206) *or an equivalent course*
- Textbook
  - Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices
  - 2nd edition (and 3rd edition)

Prof. Yuan Taur
(UCSD)

Resources

- Presentation materials
  https://github.com/hi2ska2/vlsidevices2025s

- Homework submission and notice
  - GIST LMS system

- YouTube channel
  https://www.youtube.com/@TCADHong

Grading and policies

- Attendance: 10 %
- Mid-term examination: 40 %
- Final examination: 50 %

- Homework
  - Some assignements may be given. However, they will not contribute to the total score.

Recorded lectures

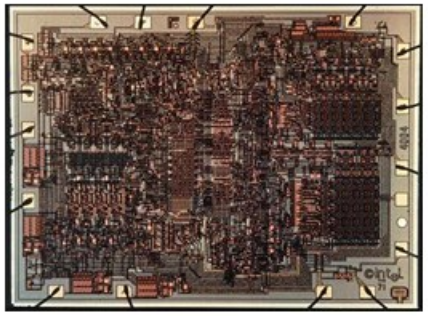
- Week 2 (Mar. 10 and Mar. 12)
  - Business trip to Hong Kong
  - Lecture 2: Recorded video, available at 09:00 on Mar. 10 (on my YouTube channel)
  - Lecture 3: Recorded video, available at 09:00 on Mar. 12 (on my YouTube channel)
  - Attendance: Leave a comment under the video.
- Additionally, Week 15 (Jun. 9 and Jun. 11)
  - Business trip to Kyoto
  - Additional recorded videos? *(To be decided)*

My own lecture material in 2014

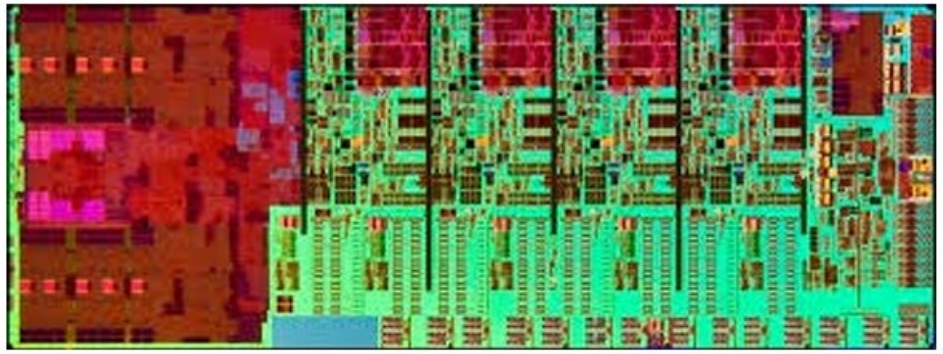
- “Digital design” course

Die shot

- More than 40 years between them



Die size: 12 sq mm
Min. feature size: 10 micron
Max. clock speed: 740 kHz



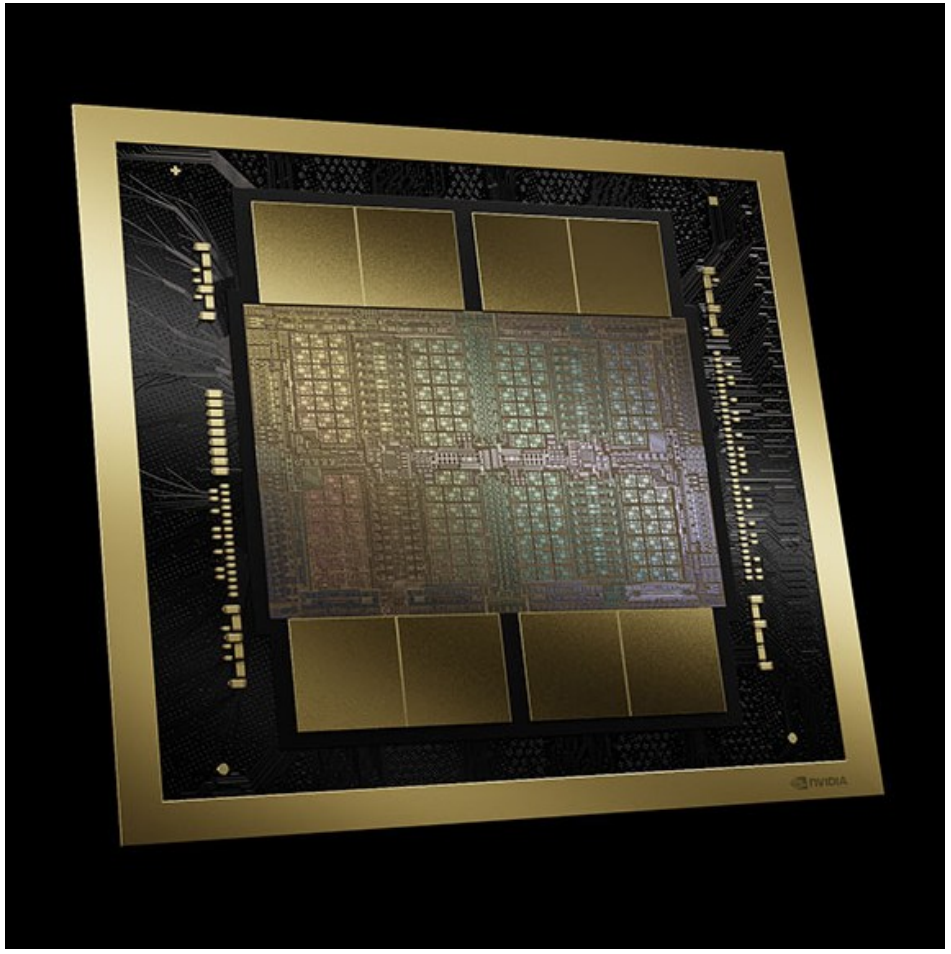
Die size: 177 sq mm
Min. feature size: 22 nm

Intel 4004, 1971, 2.3k transistors

Intel Core i7 4770K, 2013, 1.4B transistors

As of 2025,

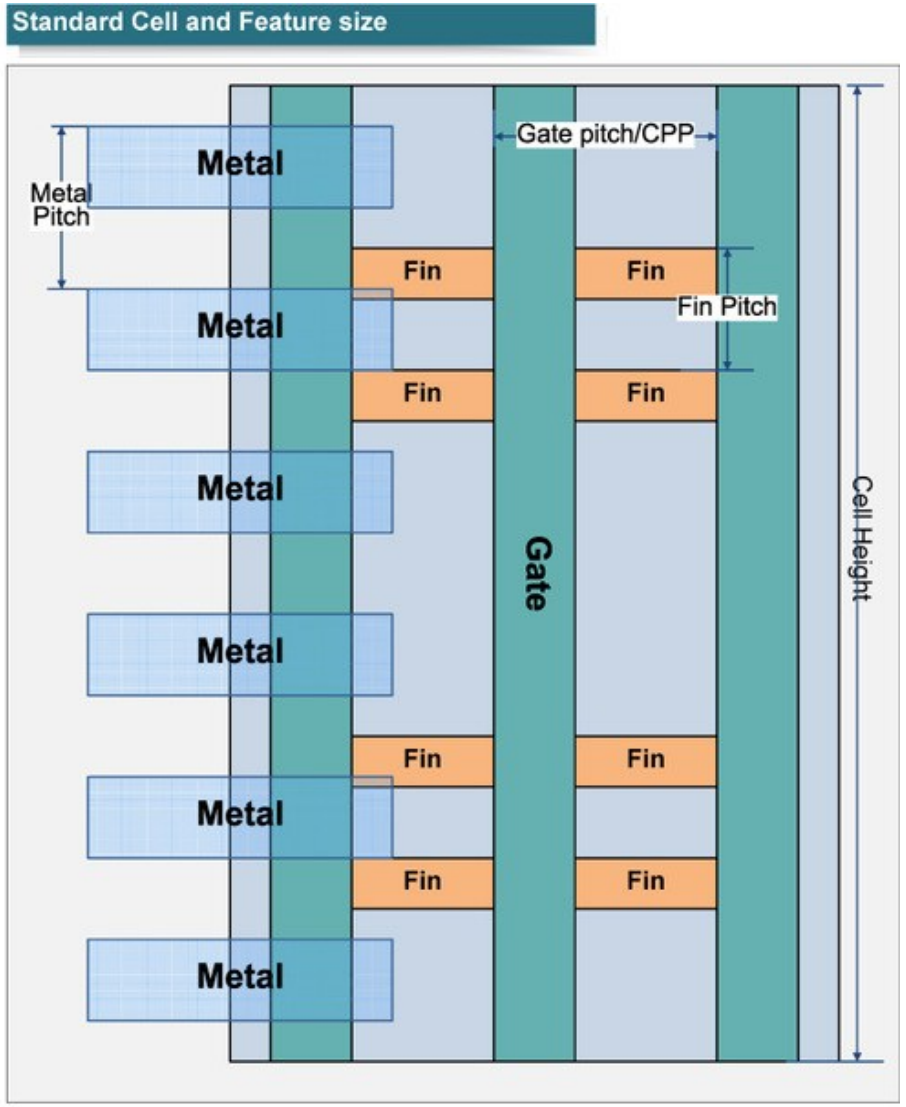
- What is the state-of-the-art?
  - It is no longer a CPU. It is no longer an Intel chip.



Nvidia B200, 2024,
208B transistors

What is the magic behind it?

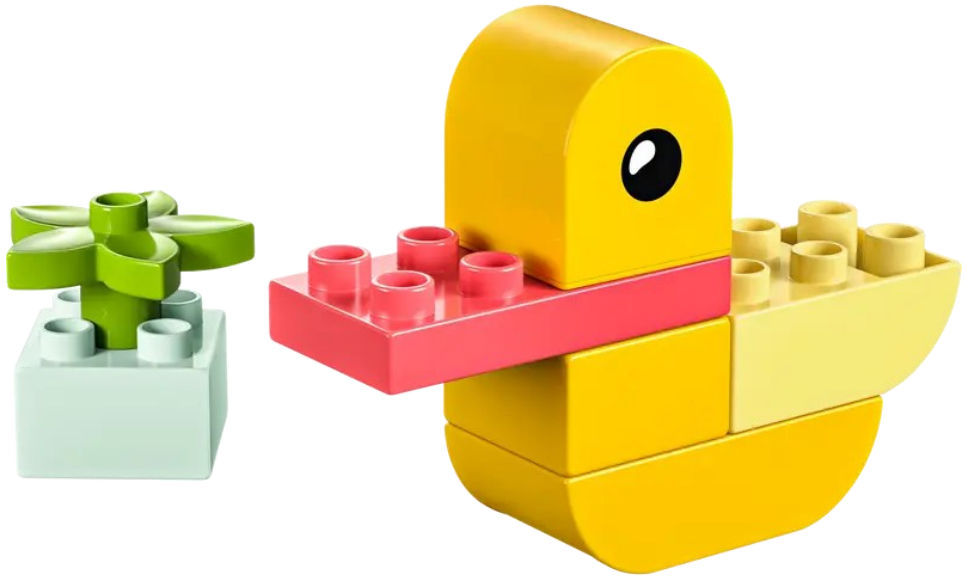
- Increasing the die size helps a lot.
  - Still, the main driver is the transistor scaling.
  - Intel 22nm: 16.5M transistors/mm^2
  (Wikipedia, “22 nm process”)
  - TSMC N5: 138.2M transistors/mm^2
  (Wikipedia, “5 nm process”)



Standard cell and feature size
(H. Goto, PC Watch article, 2017)

Lego

- Fantastic Lego creation
  - Numerous Lego bricks
  - Creative ideas

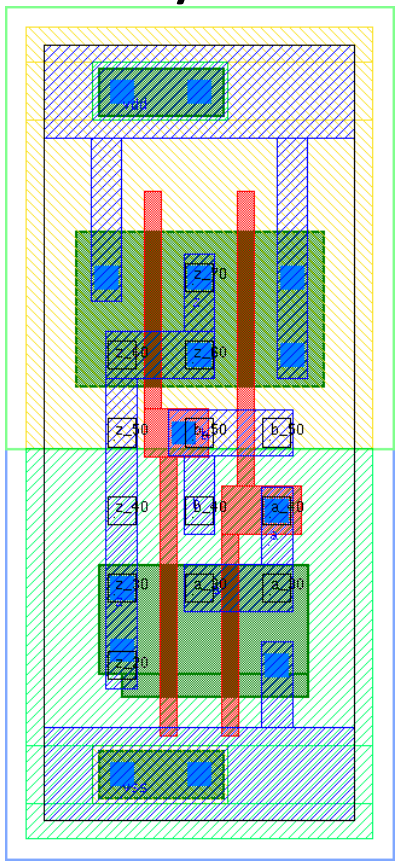


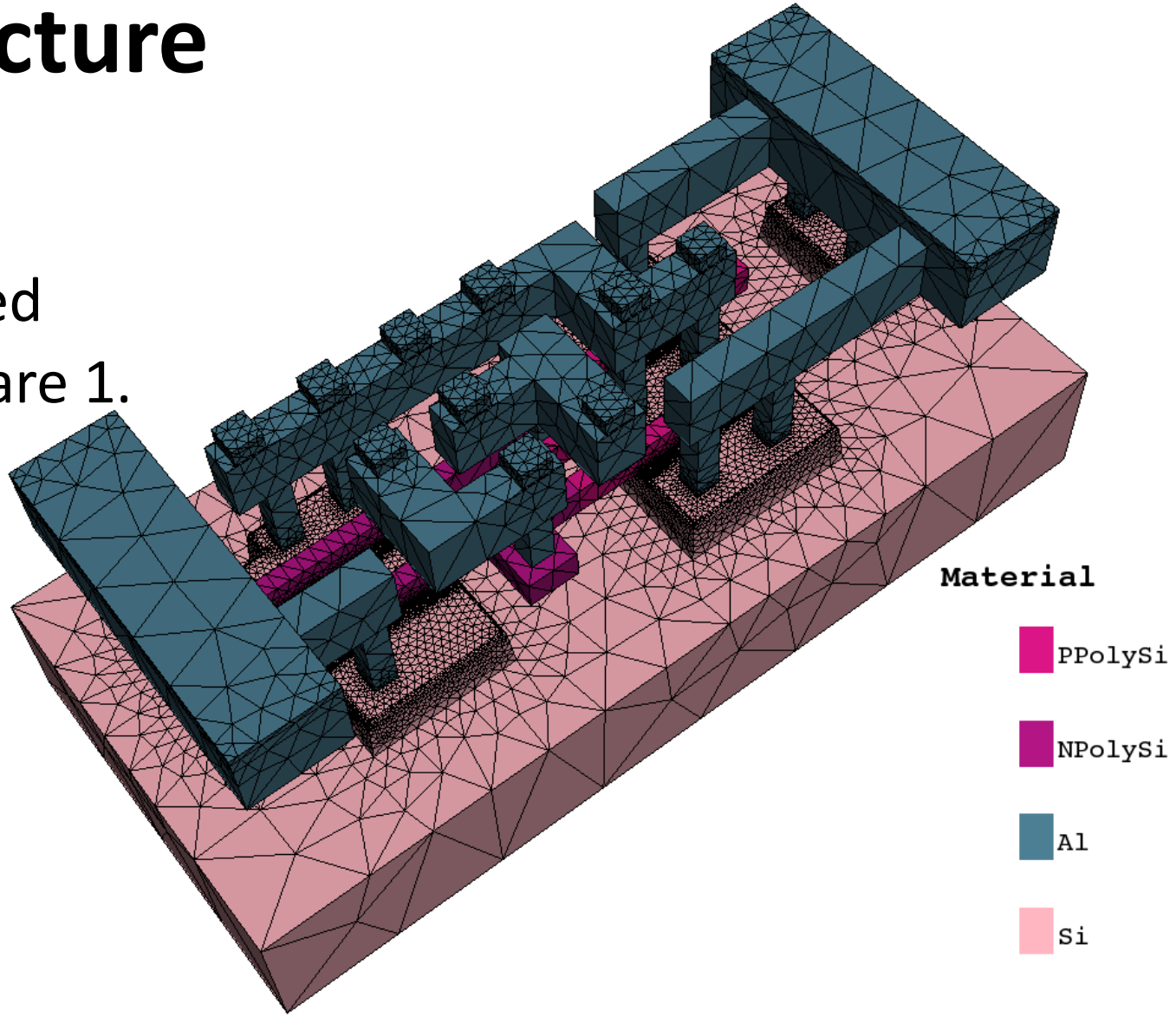
My first duck (Lego homepage)

Hogwarts castle (Lego homepage)

Layout versus 3D structure

- Example) NAND gate
  - Output is electrically connected to GND only when both inputs are 1.

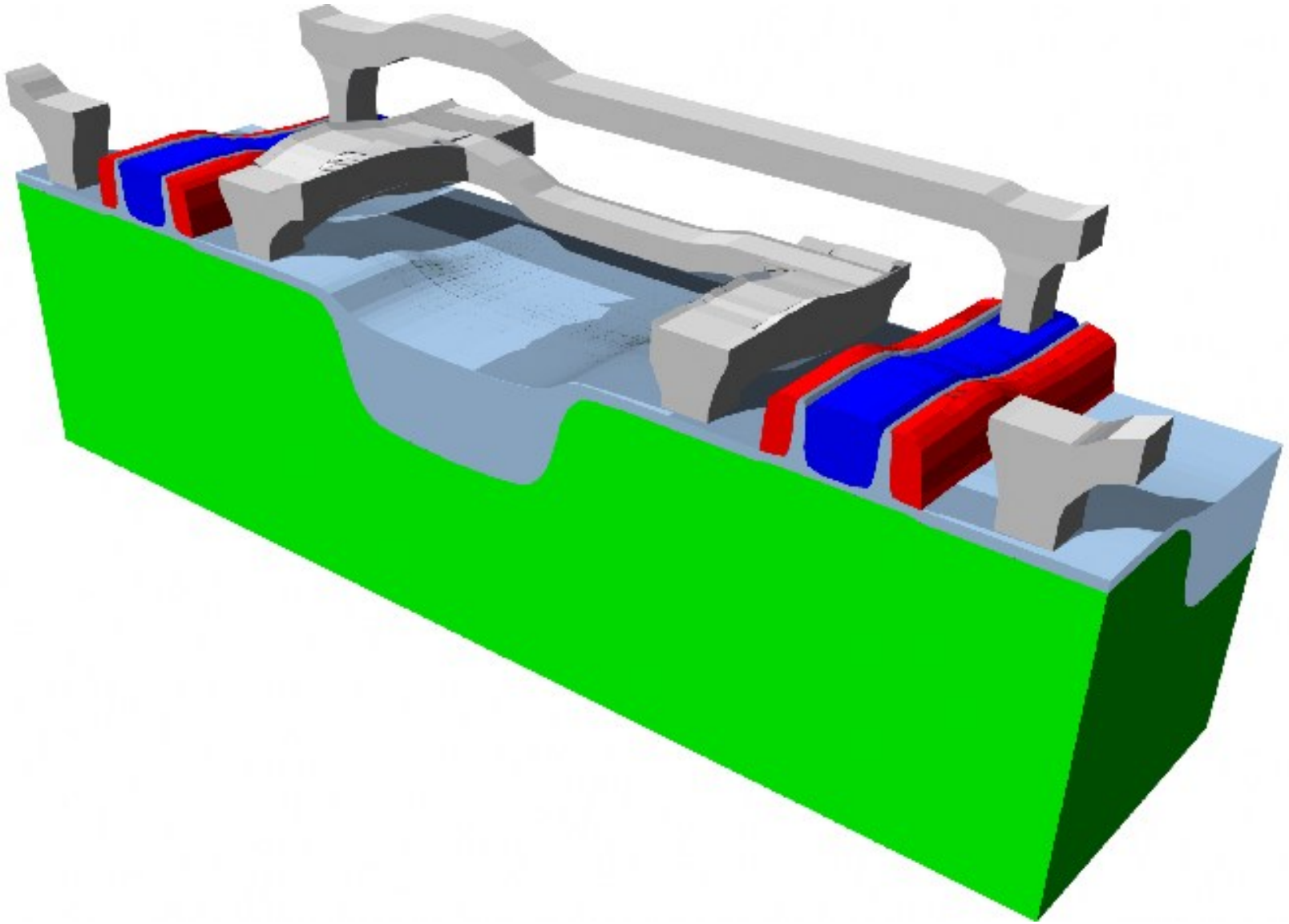




Layout and 3D structure of a CMOS NAND gate (Cogenda)

Transistors

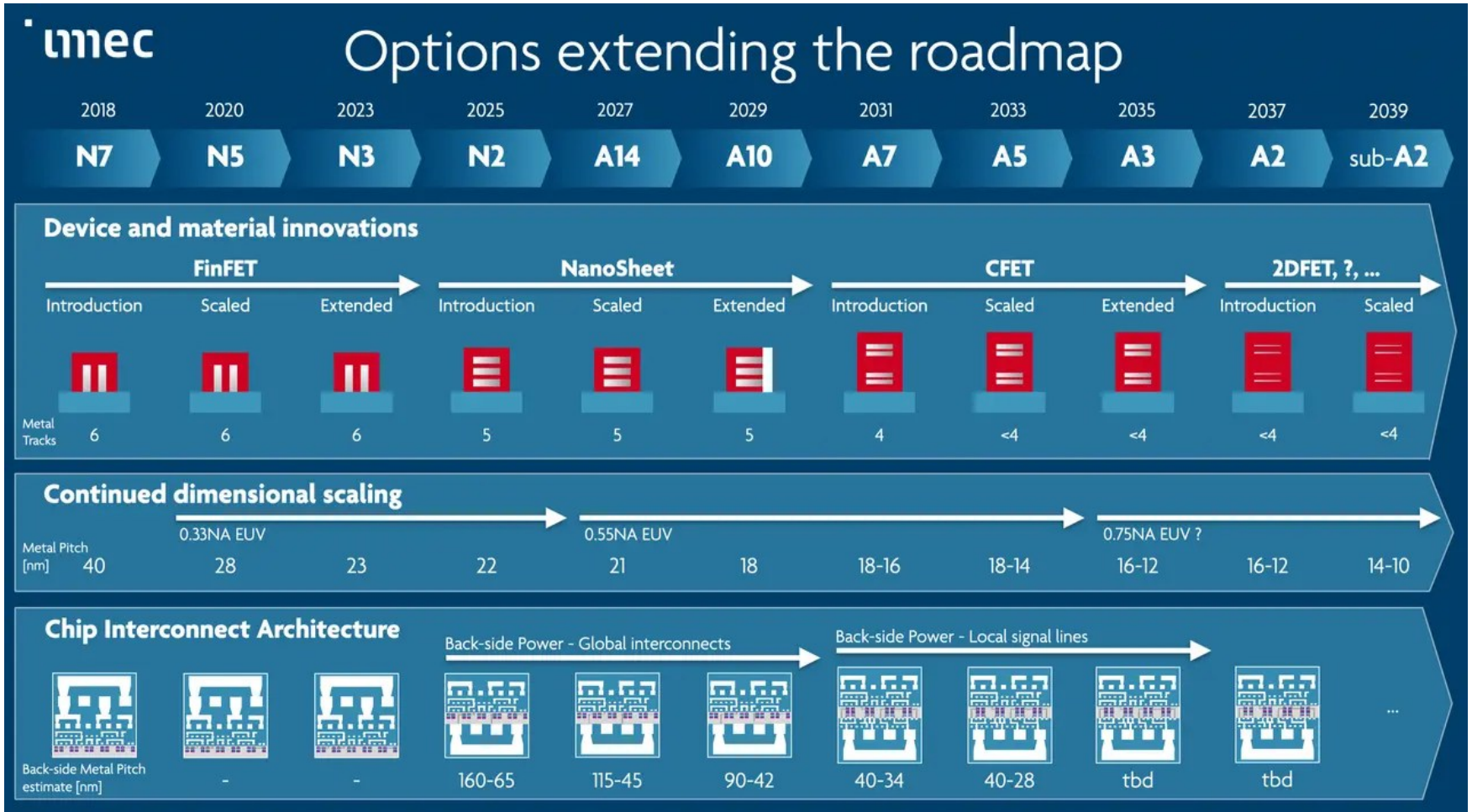
- Inverter example
  - Electrical conduction determined by silicon regions
  - Controlled by input signal (Switch)



3D structure of a CMOS inverter (P. Fleischmann, Ph. D. dissertation, 1999)

Scaling roadmap

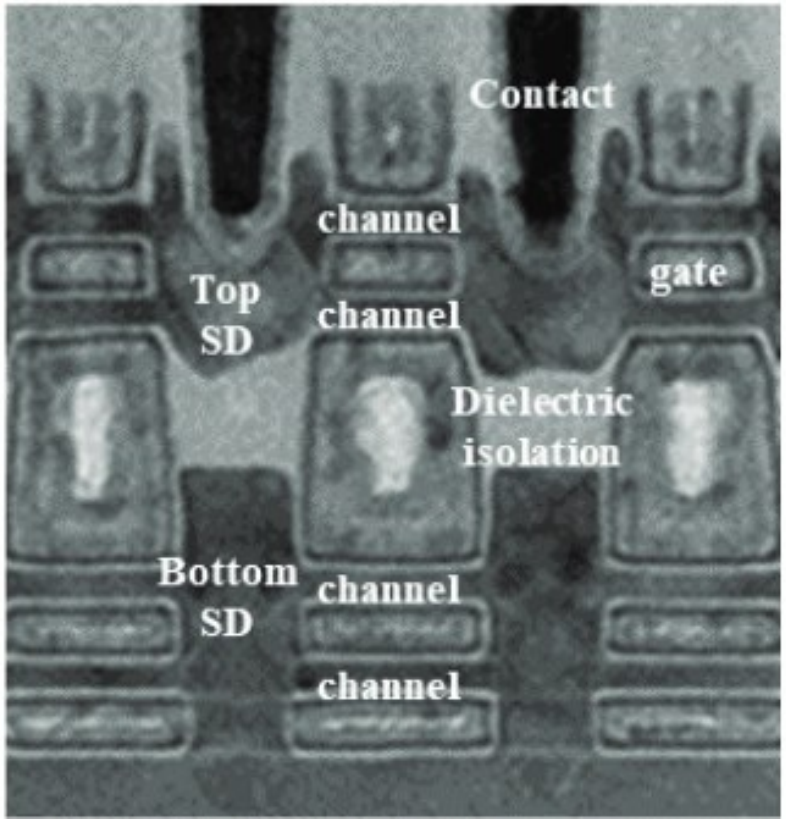
- Transistor scaling is extremely difficult.
  - *"It ain't over till it's over."*



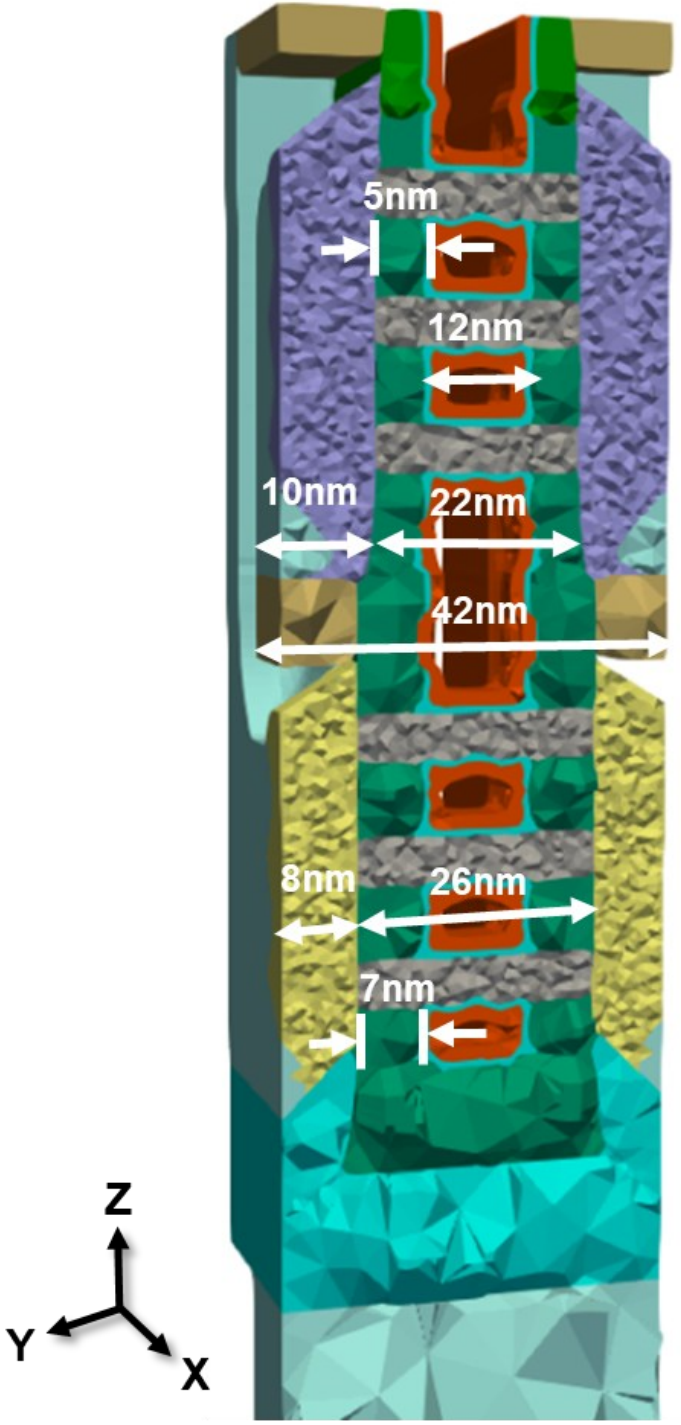
IMEC's roadmap

CFET

- Stacking NMOSFET and PMOSFET
  - Actively under development

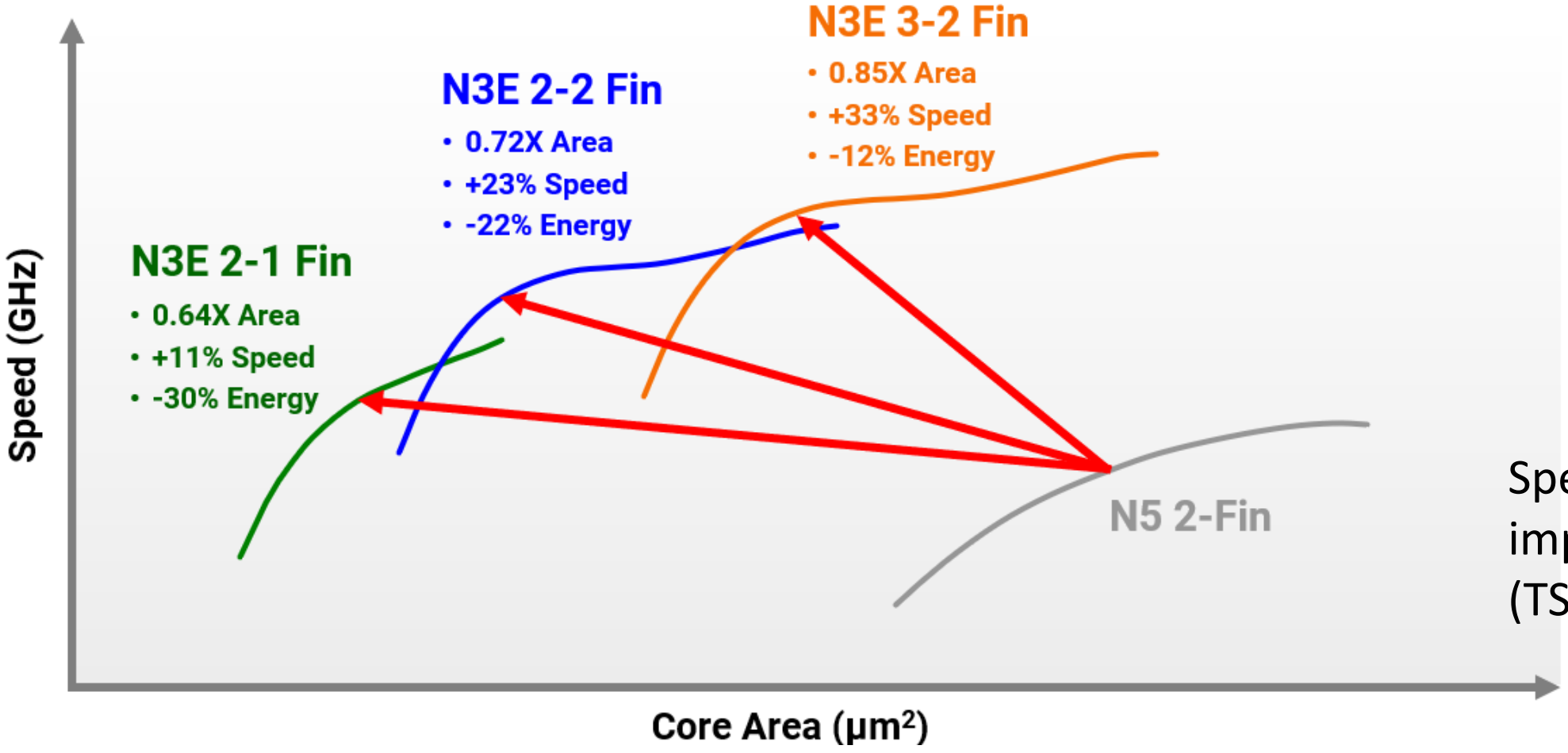


TEM image of a CFET (Samsung, IEDM 2023)



In addition to transistor area,

- We must consider other two factors, power & performance.
  - PPA



Speed and area improvement (TSMC blog)

Device engineers

- How can they develop the next-generation technology?
  - They know various ways to improve the technology.

Alchemist
(Image generated by ChatGPT)

Thank you!