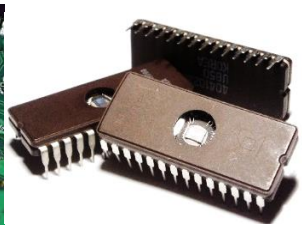
5. WAFER TECHNOLOGY

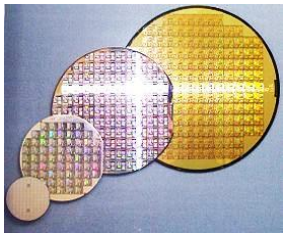
Syllabus: Introduction: physical and chemical properties of silicon, purification of silicon: chemical vapor deposition (CVD) process, zone refining process, crystal growth; preparation of single crystal silicon by Czhochralski crystal pulling technique, numerical problems; crystal slicing and wafer preparation. Fabrication processes: thermal oxidation, diffusion, ion implantation, numerical problems, epitaxial growth, masking, photolithography, wet etching and dry etching.

INTRODUCTION

Wafer technology is a technique used to produce wafers required for the manufacturing of integrated circuit chips and micro devices which have important role in electronic industry.

In electronics, **a wafer (the raw material) is a thin piece of a semiconductor material such as a silicon crystal**.



Silicon is a semiconductor material used as a substrate in the manufacturing of integrated circuit chips and micro devices. The silicon has to be subjected to many microfabrication process steps such as doping or ion implantation, etching, deposition of various materials, and photolithographic patterning. Finally, the individual microcircuits are separated and packed. Therefore, we should know the physical and chemical properties of silicon.

PHYSICAL PROPERTIES OF SILICON:

1. Silicon is a semiconductor having the band gap of 1.125 eV at 25 ◦C.
2. Si exists in two allotropic forms (amorphous and crystalline).
3. Silicon is a metalloid (properties that are intermediate between those of metals and nonmetals).
4. The melting point of silicon is 1410 ^{o}C, and the boiling point is 2355 ^{o}C.

5. Si density is 2.33 gram/cm^3.
6. Si is hard, dark grey solid. The hardness is about 7 on the Mohs scale.
7. Si crystallizes into a diamond cubic structure at atmospheric pressure.
8. Si contracts on melting (heating) and expands on solidification (cooling), which facilitates doping or incorporation of impurities.
9. Impurities incorporated in the Si lattice, provides either free electrons (-ve charge) or holes (+ve charge).

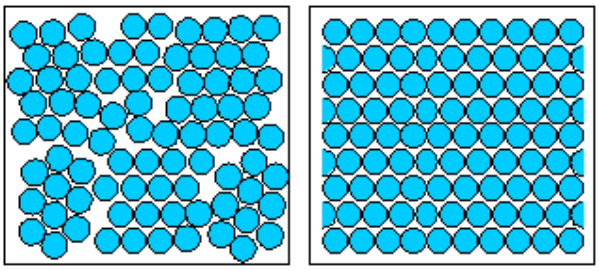
CHEMICAL PROPERTIES OF SILICON:

1. Silicon is a relatively inactive element at room temperature.
2. Si has +2 and +4 oxidation states, but +4 (tetravalent) is stable.
3. Si does not combine with oxygen or other elements at normal temperatures.
4. At higher temperatures, silicon becomes much more reactive.
5. In the molten state, it can combine with O, N, S, P and other elements.
6. It also forms several alloys very easily in the molten state.
7. Si can combine with carbon (another tetravalent element) and forms Si-C strong covalent bonds and a stable product.
8. Si is reactive towards halogens and forms chlorosilanes such as H_2SiCl_2, $HSiCl_3$ and $SiCl_4$. These are highly volatile and can be decomposed to elemental Si at low temperatures, which are used in the purification of Si).
9. Si readily combines with H_2 to form hydrides or silanes. (The silane i.e., SiH_4 is used in the further purification and preparation of electron grade silicon).

TYPES OF SILICON

Silicon is classified according to the size of the grain/particle (which refers to the **size** of a single crystal inside a **particle** or **grain),** making up the materials.

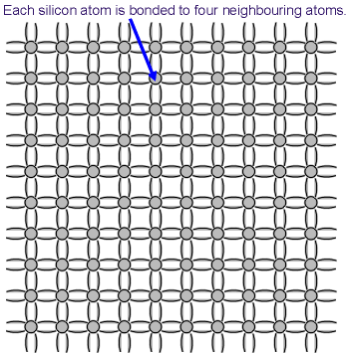
	Grain /Particle size
1) Single-crystal	> 10cm
2) Multicrystalline	1mm - 10cm
3) Polycrystalline	1µm - 1mm
4) Microcrystalline	<1µm



Polycrystal Single crystal

SINGLE CRYSTAL

In single-crystal silicon, the arrangement of atoms in the material is uniform as the entire structure is grown from the same crystal. This uniformity helps in transferring electrons efficiently through the material. To make an effective wafer, silicon has to be “doped” with other elements to make n-type and p- type layers.



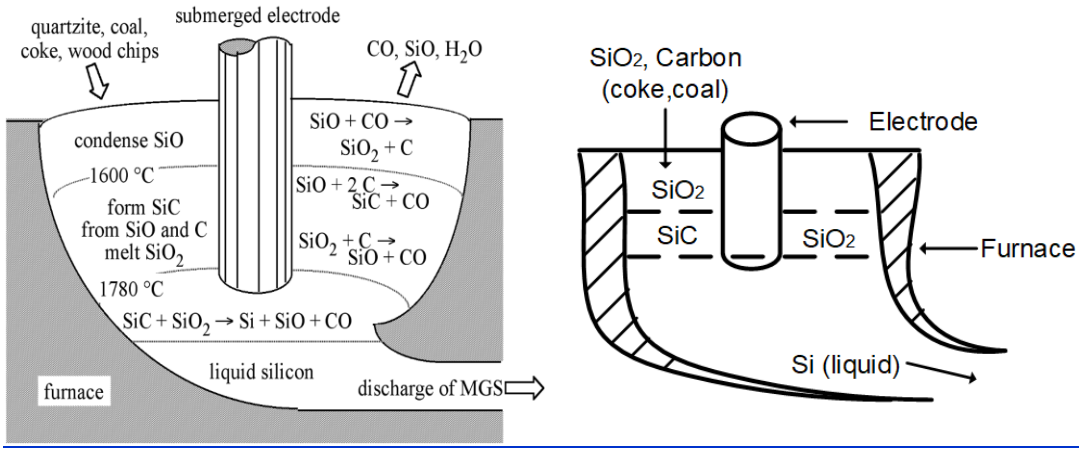
Single crystal silicon can be obtained from sand or quartz. The process of obtaining single crystal silicon involves three steps.

1. Production of metallurgical grade silicon – MGS
2. Production of electron grade silicon - EGS
3. Preparation of single crystal silicon.

PREPARATION OF METALLURGICAL GRADE SILICON (MGS) USING SAND (QUARTZINE)

Sand from Australian beaches is generally preferred as a source of silica (SiO_2) due to its high purity. Such sand is called Quartzine. Quartzine is mixed with sources of carbon like coke, coal or wood chips and then heated in a furnace using submerged electric arc at 2000^{o}C to obtain MGS of

98% – 99% purity. In electronic applications, electronic grade silicon (EGS) needed should be 99.99999999% pure. This purity can be done by chemical vapour deposition method.



$$\underset{\text{Raw material}}{SiO_2} + \underset{\substack{\text{Coal/coke}\\\text{reducing agent}}}{2C} \xrightarrow{2000^oC} \underset{\substack{\text{Metallurgical}\\\text{grade silicon}}}{Si} + 2CO$$

PREPARATION OF ELECTRONIC-GRADE SILICON FROM MGS BY THE CVD PROCESS

Electronic grade silicon (EGS) is one of the purest forms of silicon. It is approximately 99.99999999% pure form of silicon.

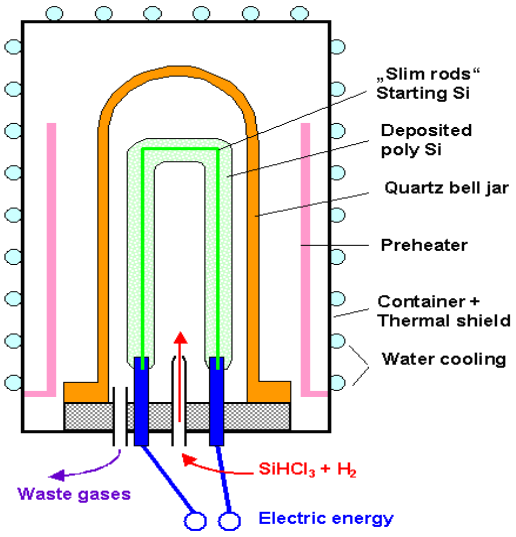
The metallurgical grade silicon (MGS) is solidified and pulverized (reduce particle size) to a fine powder. This powdered silicon is treated with anhydrous/dry HCl to obtain trichlorosilane and hydrogen as the products. The product mixture is subjected to fractional distillation to obtain pure trichlorosilane ($SiHCl_3$).

$$Si + 3HCl \longrightarrow SiHCl_3 + H_2\uparrow + Heat$$

This $SiHCl_3$ is to be passed through a chamber of Chemical Vapor Deposition (CVD) to obtain EGS.

Construction:

This technique is used for the production of polycrystalline silicon (grain size is 1 µm-1 mm).



In a quartz bell jar, thin rods of silicon of 4 mm diameter are fixed to rod holders. The quartz bell has an inlet through which reactants $SiHCl_3$ and H_2 to be supplied into the chamber. There is an outlet through which residual gases are taken out.

Working:

Reduction Reaction:

- The Si rods are heated from an external heating source to about 1000°C. By this sufficient conductivity is supplied through graphite electrodes and the vessel gets evacuated.
- At this stage, when the slim Si rods are at the reaction temperature, an optimized mixture of $SiHCl_3$ and H_2 is to be introduced into the chamber.
- To maintain the constant pressure, the reaction products are pumped out through outlet.
- At the elevated temperature, The $SiHCl_3$ undergoes reduction to produce silicon and HCl. The silicon (polycrystalline) deposits over the T-shaped slim Si rod of 4mm diameter.

$$SiHCl_3 + H_2 \xrightarrow{1000^oC} Si + 3HCl$$

- The rods are cut and taken out from the CVD chamber. They have purity of 99.99999999% and are called EGS. The residual gas HCL is taken out through the outlet.

Pyrolysis:

- Polycrystalline EGS can also be prepared by Pyrolysis of Silane at 900°C in the CVD reactor.

$$SiH_4 \rightarrow Si + 2H_{2(g)}$$

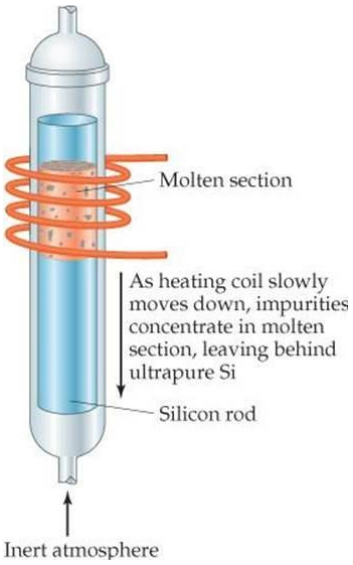
- This process helps in the production of low cost EGS and less harmful reaction products.
- Worldwide consumption of EGS is around 5000 tons per year

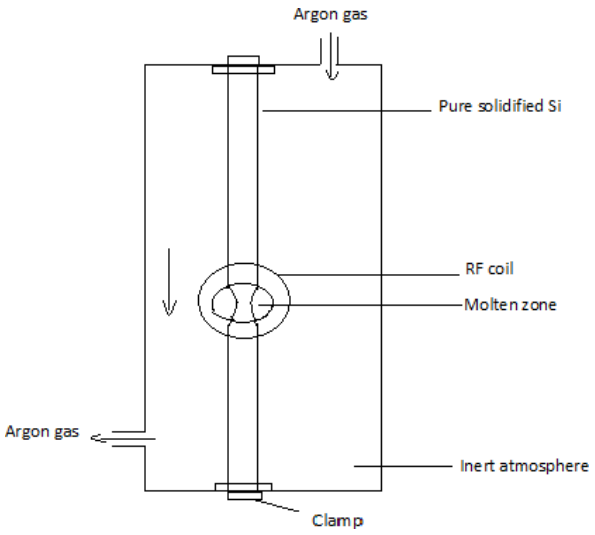
PURIFICATION OF SILICON BY ZONE REFINING

Electronic grade silicon (EGS) obtained from CVD is to be subjected to zone refining to make sure that no solid impurities are carried on to the next process of making wafers.

Zone Refining is the unique method of obtaining 99.99999999% pure polycrystalline Electronic Grade Silicon with perfect and rigorous recrystallization.

Principle: When a solid is melted, the impurities tend to concentrate in the molten zone.





Procedure:

- A vertical zone refiner is used for the purification of EGS.
- The silicon rod is clamped vertically in an inert atmosphere of Ar.
- The Si rod is heated by a radio frequency (RF) coil at about 1000^{o}C -1200^{o}C.
- At this temperature, molten zone is created at the specific portion of Si rod where RF coil is held.
- The RF coil is slowly moved from top to bottom. As a result, the impurities are swept down with molten material due to gravity, while pure Si solidifies at the upper portion with perfect recrystallization. This is said to be one zone pass.
- Once RF coil is moved from top to bottom, it brings down most of the impurities to the lower part of the rod.
- This movement is repeated several times to ensure high purity. Once the process is done, we get two parts: purified upper part and unpurified lower part.

- The lower portion of the rod is cut and separated as it contains high concentration of impurities.
- The upper portion of the silicon rod is pure and polycrystalline which can be converted into monocrystalline silicon.
- From this technique, the impurity level can be reduced to 1 atom in every 10^{12} atoms of silicon in parts per trillion ranges.

PRODUCTION OF SINGLE CRYSTAL SILICON

Electron grade silicon (EGS) is the raw material that is used for the preparation of single crystal silicon. EGS is actually a polycrystalline silicon material of high purity. EGS has some major impurities like boron, carbon and residual donors. The pure EGS will have doping elements in the parts per billion (ppb) range, and carbon less than 2 parts per million.

Crystal Growth

This process is done to convert polycrystalline silicon to single crystalline silicon. Crystallization takes place if molten silicon is allowed to solidify to a seed crystal (Seed crystal is highly pure single crystalline silicon which is used as the starting material for crystal growth). Two processes are used for single crystal silicon production from polysilicon

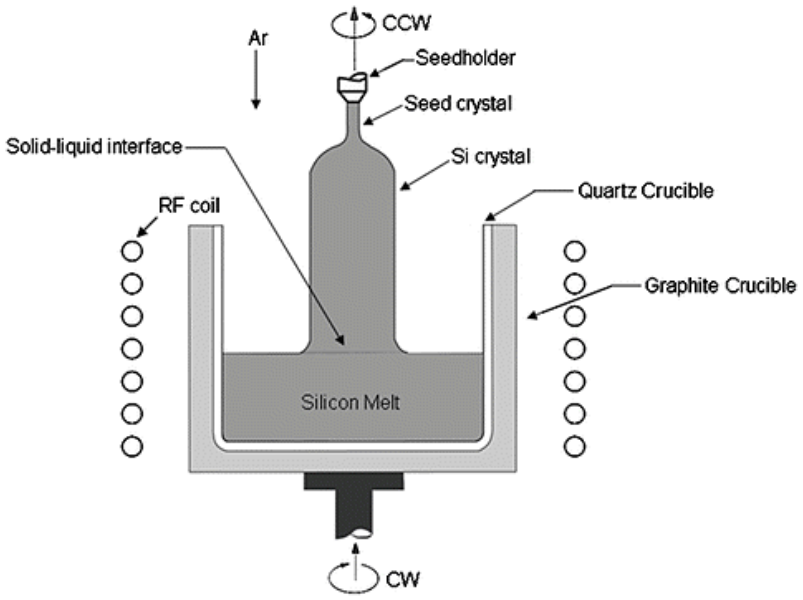
1) Czhochralski crystal pulling technique
2) Float zone process (FZ process)

CZOCHRALSKI CRYSTAL PULLING TECHNIQUE TO PRODUCE SINGLE CRYSTAL SILICON

Fabrication of most of the semiconductor devices requires single crystalline electronic grade silicon. **Czhochralski crystal pulling technique** is a method used for the production of **single crystal EGS** from **polycrystalline EGS**.

Principle:

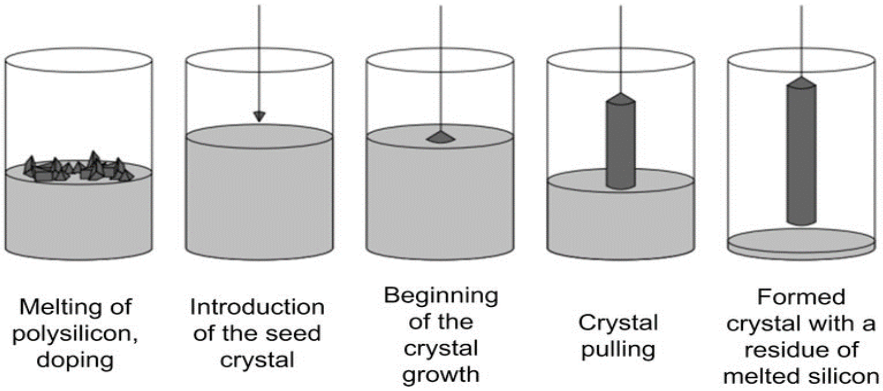
In this technique single crystalline EGS is used as a seed to grow single crystal silicon from polycrystalline silicon. When the silicon melt is pulled out, the atoms of polycrystalline silicon solidifies. It reproduces the same orientation and crystal structure as that of the used single crystalline EGS seed.



Procedure:

- A quartz crucible is placed on a crucible holder fixed with RF heating coil.
- Polycrystalline silicon material is taken into a quartz crucible.
- The crucible is heated using a RF power source in an inert atmosphere of krypton.
- When the silicon material melts, the temperature is lowered so that it is kept at the M.P. of the material (1500 ^{o}C).
- A single crystal of silicon is attached to the tip of a puller rod (seed holder) and is brought down into the molten silicon so that it just reaches the surface of the material.
- At the same time, the rod is rotated at the speed of 100 rpm and slowly lowered such that 25% of seed is immersed in the melt.
- The crucible is rotated in the opposite direction and simultaneously pulled out at the rate of 15 to 30 cm per minute.
- Initial pulling forms narrow neck of monocrystalline silicon rod. Once the neck is formed, the pulling rate is maintained at 1.5 – 5 cm per hour and the rotation at 100 rpm.
- As the melt is pulled out, it solidifies and has the same orientation and crystal structure as that of the seed.
- The process should be stopped when small amount of silicon melt is still remaining in the crucible as it contains high concentration of impurities.
- Finally, an intrinsic crystal of silicon of 5 cm diameter and 25 cm length is obtained. Such rod is called as **Ingot**. This crystal is then tested for its conductivity and cut into wafers of 0.25 mm thickness with the help of a diamond tipped saw.

This technique is also used for the production of n or p-type of single-crystal silicon by doping with boron (p-type semiconductor) or phosphorous (n-type semiconductor) in the melt. Calculated amount of selected dopant must be added into the crucible so that dopant atom gets into silicon rod while it is being developed.



The concentration of impurity in the melt (liquid state) is usually less than that in the grown crystal (solid state). The maximum concentration of impurities that can be introduced into a semiconductor at a given temperature T is known as solid solubility. Solid solubility increases with increase in temperature. The oxygen content in crystal grown by CZ process is high ($5x10^{17}$ to $2x10^{18}cm^{-3}$). This is due to the reaction of silicon in the melt with the quartz lining of crucible. This oxygen may become electrically active during subsequent process. Czochralski process is not used when material with resistivity more than 10 ohm-cm is required.

Segregation Constant: Segregation constant (K_o) plays an important role in determining the amounts of dopants to be added. The K_o is defined as the ratio of concentration of impurities in the solid (C_s) to the concentration of impurities in liquid state(C_l) at equilibrium.

$$K_o = \frac{C_s}{C_l}$$

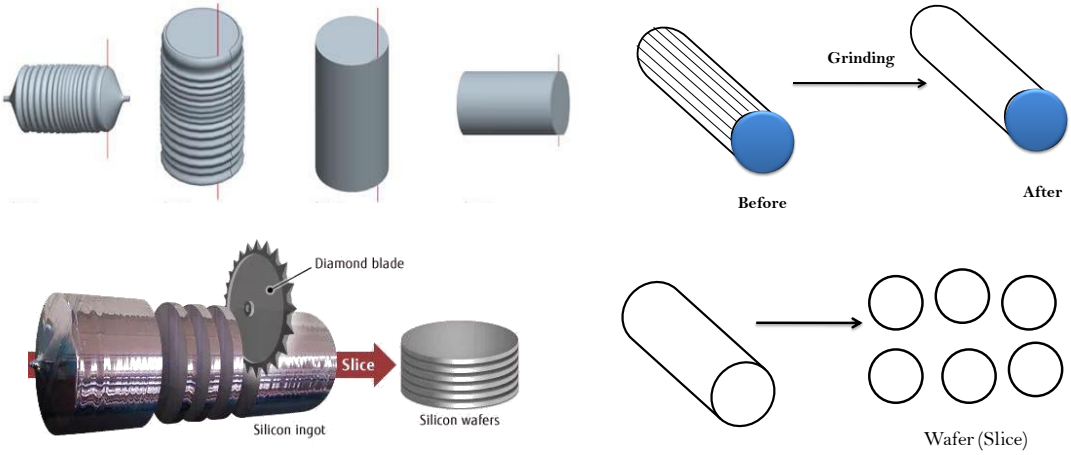
Solid solubility: The maximum concentration of impurities that can be introduced into a semiconductor at a given temperature is known as solid solubility. Solid solubility increases with increase in temperature. Following are the formulas used for the calculation of dopants in the silicon wafer.

PREPARATION OF WAFERS

The wafer formation process converts the large silicon crystals into individual wafers. The first step is to check the silicon ingot for its crystal orientation and electrical conductivity.

Crystal Slicing

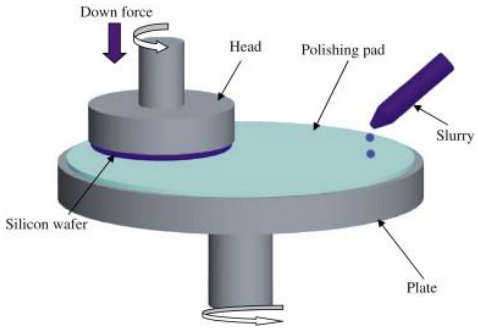
- It is a mechanical process of cutting ingots into more pieces.
- The ingot obtained by Czochralski process is to be cut on both ends to get flat surfaces.
- Crystal ingot has a diameter of 20 cm and a length of 100 cm; this ingot surface is ground well to get an exact cylindrical shape with flat ends.
- Before slicing, a piece of silicon is taken out using a saw blade, and then crystal orientation is determined using X-ray diffraction method. This process is continued until the wanted orientation of the crystal at the surface is obtained. Then the crystal is cut into slices (wafers) at the selected angles.



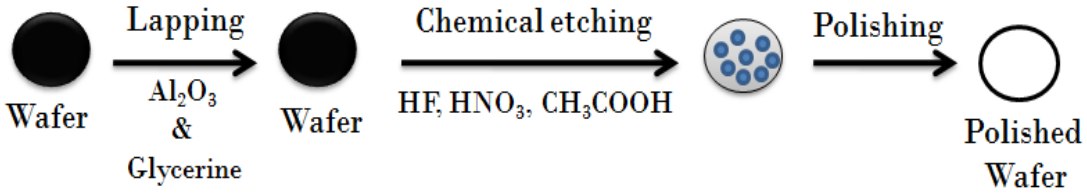
- The thickness of wafers varies from 0.4 mm to 1.0 mm. The slicing is done by a ring-shaped saw blade made of stainless steel containing diamond cutting. The process is carried out in the water as coolant.
- About one-third (1/3) of the material is lost as sawdust.

Wafer Preparation

- The sliced crystal has to be subjected to lapping on both the sides.
- **Lapping** involves the polishing of silicon slice under pressure to remove any cracked surface on silicon wafer, saw marks and damaged surface caused by the slicing process. Lapping is done using a mixture of Al_2O_3 and glycerine.



- The lapped wafers are subjected to **chemical etching** i.e., treating with the mixture of HF, HNO_3 and CH_3COOH to remove any further damages from the surface of silicon wafers.
- **Lapping and chemical etching** processes produce flat surface on silicon wafers. Later based on their thickness, the wafers are separated on a machine-controlled basis.
- Finally, the Si wafer should be made ready for manufacturing. In order to distinguish both surfaces of wafer, one side of the wafer is polished to mirror finish. Fabrication process is carried out on the polished surface.



FABRICATION PROCESS

- **Fabrication:** It is the process of making or manufacturing something from raw or semi-finished materials.
- For many electrical and electronic applications, the quality of polished wafer is not sufficient due to some defects generated during crystal growth of the wafer.
- The defects in few microns at the surface can reduce the performance of devices built on it.
- This problem can be overcome by depositing an additional layer of high purity Si on the top of the polished wafer substrate.

The following are the processes involved in the fabrication are:

1) Thermal oxidation

2) Diffusion

3) Ion implantation

4) Epitaxial growth

5) Masking

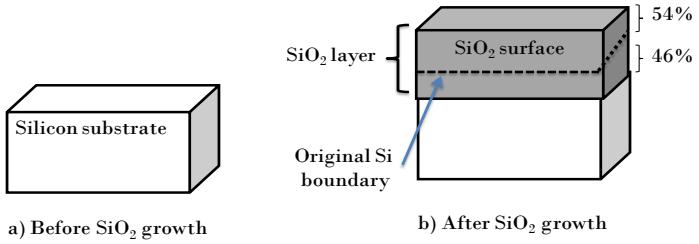
6) Photo Lithography

7) Etching

- The basic integrated circuit manufacturing process is known as 'planar process' in which introduction of dopants and metallic connections are carried out from the top surface of the wafer.
- In planar process, several wafers can be processed simultaneously. Precise control of temperature; humidity and clean environment are required for fabrication of devices.

THERMAL OXIDATION

Thermal Oxidation is a method of growing a SiO_2 layer from a single crystal silicon wafer.



Thermal oxidation is required for, (1) masking the material 2) surface modification 3) biocompatibility 4) to act as a sacrificial layer.

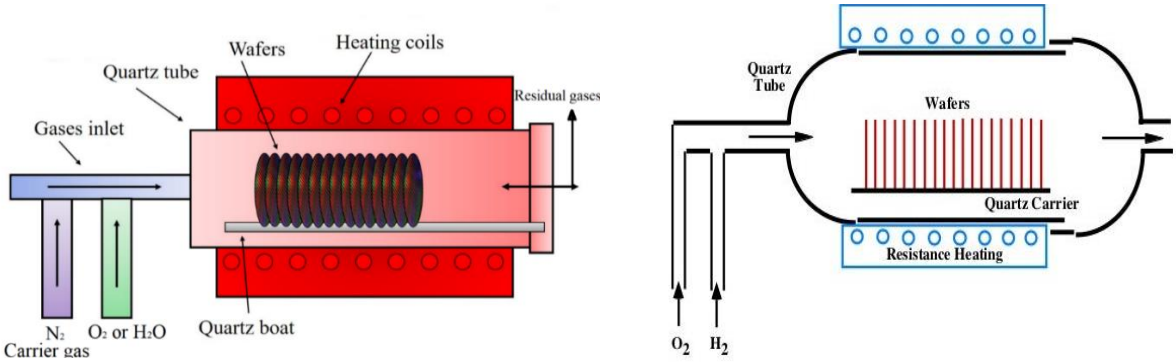


Fig. Thermal Oxidation System

Procedure:

- Thermal oxidation is carried out in a thermal oxidation furnace system.
- It consists of a quartz furnace tube. Si wafers are placed vertically on quartz boat inside the quartz furnace tube in such a way that polished side of wafer is facing the inlet of quartz tube.
- One end of the quartz furnace tube is provided with an outlet to remove residual gases.

- The other end of the tube is provided with 2 inlets for sending in oxidizing agents i.e., oxygen (for dry oxidation) or water vapour (for wet oxidation) required for oxidation reaction.
- The quartz furnace tube is heated to a temperature of 900^{o}C to 1200^{o}C using resistance heaters/heating coils.
- Thermal oxidation proceeds in two ways depending on the nature of oxidizing agent used.

Dry Oxidation:

- Dry oxidation takes place when dry O_2 is used as an oxidizing agent.
- The dry oxygen in its molecular form is diffused into the wafer at high temp of 900 ^{o}C to 1200^{o}C and is made to react with it.
- The chemical reaction at the Si surface is,

$$Si + O_2 \rightarrow SiO_2$$

- One molecule of oxygen results in the formation of one molecule of SiO_2.
- As reaction proceeds, the thickness of SiO_2 increase. Decrease in the rate of reaction, decreases the rate of increase of thickness of SiO_2.
- In dry oxidation, the rate pf oxide layer growth is very low. But its electrical properties are excellent. Dry oxidation results in SiO_2 layer of thickness less than 1.0 μm.

Wet Oxidation:

- Here water vapour/steam is used as an oxidizing agent.
- This process takes place at a temp of 900^{o}C to1000^{o}C.
- The steam is allowed through an inlet so that it reaches preheated silicon wafers. At high temperature, steam reacts with surface silicon atoms to form SiO_2 and hydrogen.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

- Here, two molecules of water vapour are used to for one molecule of SiO_2.
- As reaction proceeds, thickness of SiO_2 keeps increasing which decreases the rate of reaction and hence the rate of increased thickness of SiO_2 decreases.
- H_2 produced by this reaction diffuses rapidly through the growing oxide and leaves the system at the gas oxide interface.
- Wet oxidation is much faster than dry oxidation. It is suitable for making thick oxide greater than 1μM. But it suffers from more structural defects.

- Due to more quantity of SiO_2 produced which results in further increased thickness of SiO_2 layer. This is because,
- When SiO_2 is grown on Si wafer, thickness of Si decreases as Si is consumed during oxidation.
- In the beginning, O_2 & Si react to form SiO_2. Once oxide layer is formed, further oxidation occurs at Si- SiO_2 interface, but not on top of oxide.
- Oxide growth rate slows down with increase in oxide thickness because the oxidizing agent should move through the growing oxide layer in order to reach the Si surface.
- The interface produced by thermal oxidation is not exposed to atmosphere, minimizing the impurities. The oxide films thus formed are used in making both simple and complex semiconductor devices, in integrated circuits etc.

DIFFUSION

Principle

- **Diffusion** is a process of selective doping of 'B' or 'P' atoms into semiconductor Si wafer.
- **Doping** means the introduction of impurities into the semiconductor wafer to change its conductivity.
- The specific area of silicon where dopants are to be introduced is precisely marked and SiO_2 is etched from that area because impurities like B, P etc. do not diffuse through SiO_2.

The Si wafer ready for diffusion process is carried out in two steps. 1) Pre-deposition and 2) Drive in.

Pre-Deposition

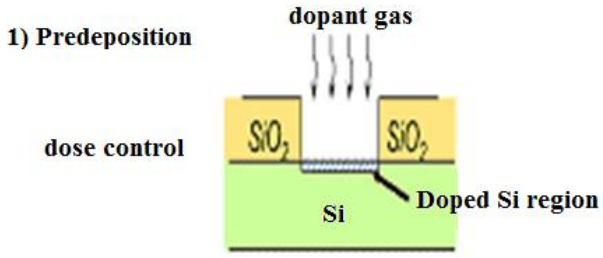
i) In Pre-deposition, a high concentration of dopant atoms in vapour form is introduced on the Si surface at 1000^oC.

ii) At 1000^oC, the dopant atoms penetrate through the silicon surface and get concentrated near the surface. This occurs due to the loss of energy at given temperature.

iii) This process of dopant atom concentrating near the surface of wafer is also called as "Constant source deposition".

iv) At this high temperature, the bonds in Si are broken and impurity atoms diffuse into the Si wafer because of the concentration gradient and replaces Si atoms in the bond.

v) This process produces a shallow, heavily doped layer. This is also known as **constant source diffusion.**



Drive-In

i) After the desired amount of dopant is deposited on Si wafer during pre-deposition, the dopant source is removed during drive in process.

ii) During drive-in process, the impurities are diffused deeply into the Si wafer.

iii) For drive-in process the supply of impurity is stopped and the temperature raised to 1250^{o}C.

iv) As the dopant source is removed after pre-deposition, the total amount of impurities in the wafer remains constant during drive-in process.

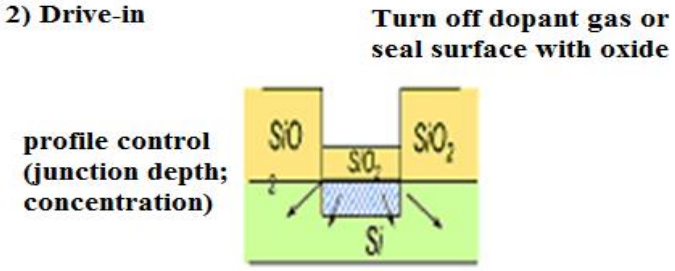
v) This reduces the surface concentration and increases the junction depth.

vi) This process is done at higher temperature of 1100^{o}C to 1250^{o}C.

vii) At high temperature of 1100^{o}C, these impurities diffuse into Si wafer and their concentration reduce at the surface.

viii) The diffusion depth is decided by the precise control of temperature and time of diffusion.

ix) In drive-in, the dopant atoms are rich inside the silicon wafer. This is also called as **constant dose diffusion**.



After the doping is done only nitrogen gas is supplied to flush out any impurities left in the quartz tube and also to bring down the temperature so that silicon wafers can be taken out.

Process

Diffusion process is carried out in an open tube diffusion reactor/furnace.

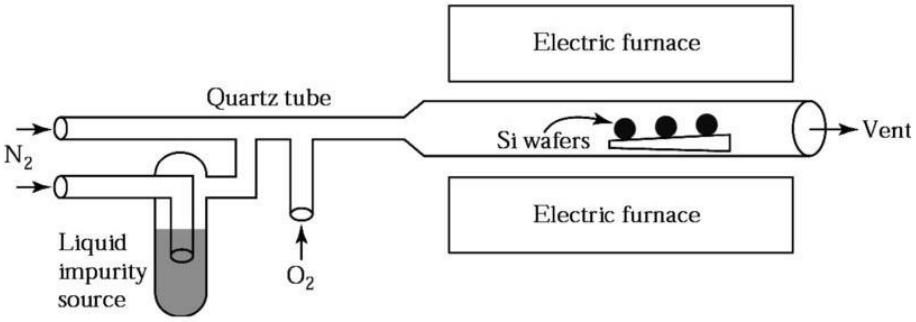


Fig. Open tube diffusion system

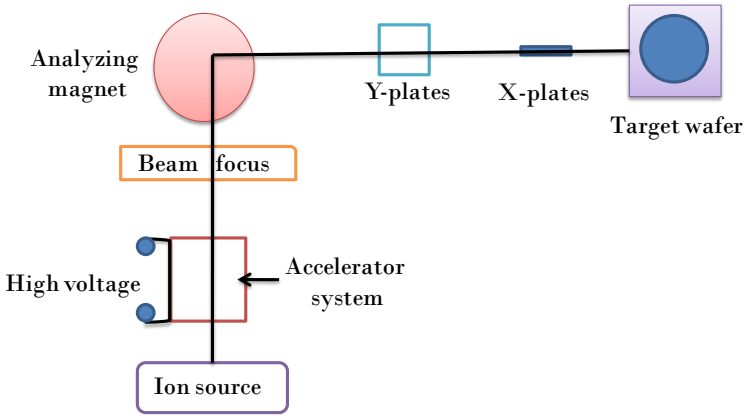
- It consists of a quartz tube inside of which movable quartz boat is present which acts as a carrier.
- Wafers are arranged on the quartz boat in series in order to have uniform doping on all wafers.
- Impurities are introduced into the furnace in vapour form using nitrogen & oxygen as carrier gases.
- Oxygen gas is introduced first to restore SiO_2 (the place where it was over etched) and to oxidize any of the impurities which are carried away by nitrogen.
- After O_2, nitrogen gas is passed through dopant solution (diborane or phosphine) which will carry the dopant atoms to the surface of silicon wafer.
- Boron (acceptor impurity), & phosphorous (donor impurity) are two common sources of dopants/impurities for diffusion in silicon wafer. They have high diffusion rate in silicon, low diffusion rate in SiO_2.
- Quartz boat furnace is heated by means of electric furnace to a temperature of 1000^{o} C when pre-deposition takes place. After pre-deposition, the supply of impurity is stopped by stopping nitrogen in liquid dopant and the temperature is increased to 1100^{o}C to 1250^{o} C and the drive-in process begins and driving the impurities deeply into the Si semiconductor.
- The diffusion depth is decided by the precise control of the temperature and time of diffusion.

ION IMPLANTATION

- It is an alternate method of doping in which selected area of the wafer surface is bombarded with high energy (10,000 ev) impurity ions. For this selective doping technique, it is not mandatory to have any masking layer on the silicon surface.
- The dopant atoms are converted into highly concentrated tiny beam. These high energy ions can penetrate into the Si semiconductor.

- The faster the ions 'shot' at the wafer, the deeper they penetrate. On entering the wafer, due to collision with electrons and nuclei of silicon atoms, they lose their energy and stops penetration.

A simplified setup for ion implantation process is shown in the figure.



Procedure

• Ion source consists of the dopant 'B' or 'P' material within a strong electric field.

• The strong electric field separates the dopant atoms into respective ions forming charged gaseous plasma.

• These charged ions are then induced to wanted velocity by controlling of high voltage in the accelerator system.

• Later, these charged high velocity ions are focused into a narrow beam of high velocity ions having current of the order of 1 mA.

• The beam is turned through 90^{o} by using an analyzing magnet. The unwanted impurities in the beam are removed in analyzing magnet.

• The magnetic field in the analyzing magnet is set up in such a way that only the desired dopant turns through right angle (90^{o}) and the unwanted impurities having different mass from that of the desired material are turned by different angle and are screened out by 'Y' plates.

• The focused beam of dopant ions is then passed through 'X' scanning plates which helps in proper implantation of ion beam over the target silicon wafer.

• The ion beam is moved over the target wafer up and down, as the implantation has to be done bit by bit.

• The depth of penetration of any particular type of ion will increase with increasing accelerating voltage.

• After the ion implantation process, the silicon wafer is subjected to annealing process at a temperature of 800-1000^{o}C for period of 20 to 30 minutes to restore any mechanical damage on silicon wafer.

Annealing is done mainly to achieve the following:

- The semi-conductor Si wafer can regain its crystal structure back to single crystal which is important for efficient device operation.
- It allows the dopant material to fit well into the silicon crystal lattice.

Though ion implantation is more expensive process than conventional diffusion, it offers the following **advantages**.

- The depth of the doping levels can be precisely controlled, because both the accelerating voltage and the ion beam current are electrically controlled outside the apparatus.
- Highly pure dopants can be added.
- Uniform doping over the silicon surface is possible.
- Doping area can be precisely defined since the spread of the directed ion beam is very little.
- As it is a low temperature process, the movement of impurities is less within the Si wafer.

EPITAXIAL GROWTH

Introduction

Once a crystal ingot is grown, it is cut into slices by a diamond saw. These slices are first polished with an abrasive grit, and then are mechanically polished to remove surface damages. These are the starting materials used for the fabrication of semiconductor devices and microcircuits. For many applications, these slice helps just as mechanical support, on which layers of materials of appropriate resistivity and conductivity are developed suitable for the fabrication of microcircuits. The term epitaxy is derived from two Greek words, ‘epi’ means upon and ‘taxis’ means ordered.

- **Epitaxy** is the process growing a crystalline layer over a crystalline substrate. In the epitaxial process, the substrate wafer acts as a seed crystal, thus preserving the overall single crystal structure. Hence, epitaxial grown layer has same crystal structure as that of the substrate.
- **Homoepitaxy**: When the grown layer and the substrate are of same material, then the process is known as homoepitaxy or autoepitaxy. Example - Si grown on Si and GaAs grown on GaAs.

In homoepitaxy, no problems of compatibility occur because of similarity in orientation, chemical properties, lattice parameters and crystal structure of the epitaxial layer and the substrate on which it is grown.

- **Heteroepitaxy**: When the grown layer and the substrate are of different material, then the process is known as heteroepitaxy. Example - Si (diamond lattice) grown on sapphire (hexagonal) and GaAs on Si.

  In heteroepitaxy, the crystal structures of the layer and the substrate should be similar if crystalline growth is to be obtained. The substrate must be chemically and physically inert to the growth environment. There must be chemical characteristics between the materials.

- By diffusion or ion-implantation process, impurities such as 'B' or 'P' are driven into the silicon semiconductor wafer. But **in epitaxial growth, a layer of doped semiconductor is grown over the existing semiconductor which may be of any doping**.

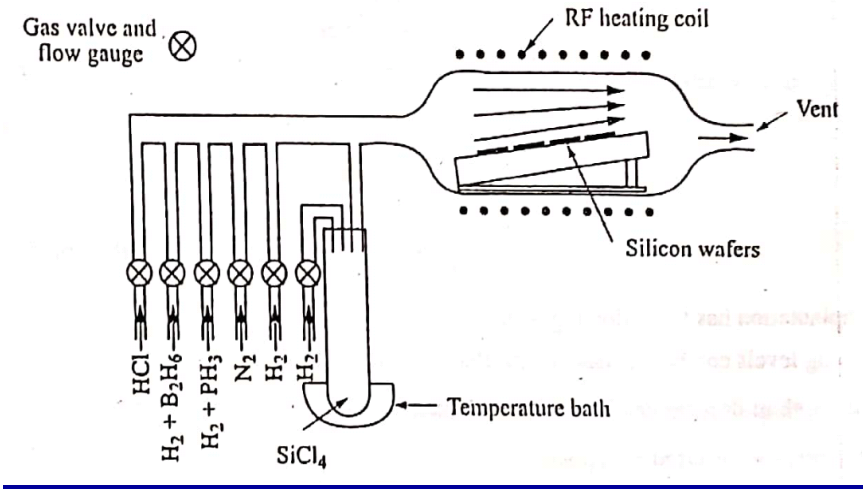


Fig. Epitaxial Growth System

Procedure:

- The silicon wafers are placed in a boat shaped graphite crucible and kept in a long cylindrical quartz tube with inlet and outlet for gases.
- The reactive gases are introduced into the reaction chamber based on the selection of semiconductor material and the dopant atoms.
- The system is heated by RF coil to a temperature of 1200^{o}C. At this temperature, semiconductor formation takes place and grows on the silicon semiconductor substrate.
- The byproduct gases like H_2 and HCl are vented away from the quartz tube.

- The thickness of the layer varies from 3 to 30 microns. This type of epitaxial growth is called as vapour phase epitaxial growth.

Steps involved in vapour phase epitaxial growth:

- Hydrogen gas is passed to purify the reactor of any impurities.
- HCl gas is passed for vapour phase etching of silicon semiconductor wafer surface at a temperature of 1150^{o}C to 1250^{o}C for 3 minutes. Thin region of damaged Si is removed from the silicon wafer surface by means of HCl etching.

$$Si_{(S)} + 4HCl_{(g)} \rightarrow SiCl_{4(g)} + 2H_{2(g)}$$

- Vapours of H_2 and $SiCl_4$ are passed into the reaction chamber for producing **silicon on silicon** epitaxial layer. This process of epitaxial growth is known as **chemical vapour deposition** as all the chemicals introduced and that take part in the reactions are in the form of gaseous state.

$$SiCl_{4(g)} + 2H_{2(g)} \rightarrow Si_{(S)} + 4HCl_{(g)}$$

- H_2 and Diborane (B_2H_6) are supplied for p-type epitaxial layer growth on silicon wafer.
- H_2 and Phosphene (PH_3) are supplied for n-type epitaxial layer growth on silicon wafer.
- Once the growth is completed, the dopant atoms and silicon flows are eliminated and temperature is reduced by shutting the power off.
- H_2 gas is passed to purify the reactor of any impurities left out in the reactor.
- As the reactor cools down to ambient temperature, the H_2 flow is replaced by N_2 flow so that the reactor may be opened up safely.

Advantages of using $SiCl_4$ as source

- $SiCl_4$ is non-toxic, inexpensive and easy to purify.
- The reaction of $SiCl_4$ and the formation of Si takes place only on the Si surface and not on boat or reaction chamber walls.

MASKING

In the manufacture of semiconductor devices, selective doping is often necessary. During this certain regions of the wafer have to be protected against doping. This is usually done by covering the entire wafer by a protective layer, and then removing this layer at selected regions of the wafer. This is called **masking**.

PHOTOLITHOGRAPHY

Introduction

Photolithography or optical lithography is a kind of lithography (printing).

- **Photolithography** is a process of transferring geometric shapes or images on a mask to the surface of a silicon wafer by the use of UV light and a photo resist.

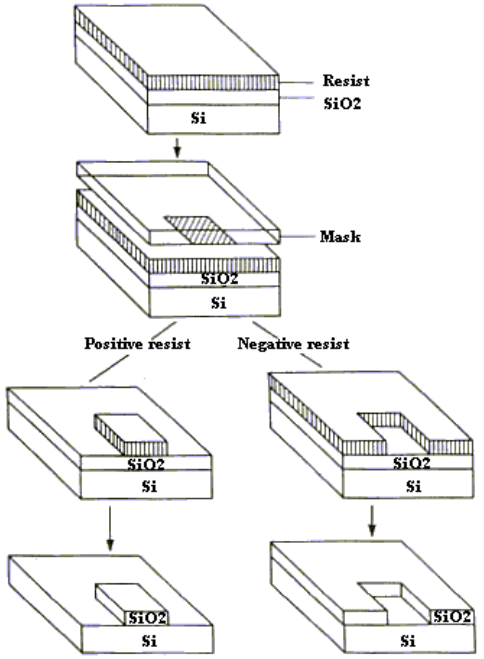
The steps involved in the photolithographic process are as follows:

1) Wafer Cleaning and Barrier Formation

In the first step, the wafers are chemically cleaned to remove any traces of organic, ionic, and metallic impurities. After cleaning, silicon dioxide, which serves as a barrier layer, is deposited on the surface of the wafer.

2) Photo resist Application (Spinning)

A drop of **light-sensitive liquid** called photoresist is applied on the surface of the oxidized silicon wafer. The wafer is then accelerated rapidly to a rotational velocity in the range **3000 to 7000 RPM for 30-60 seconds.** The spinning spreads the solution in a thin, nearly uniform coat and spins out the excess liquid. The thickness of the coat so obtained is in the range **5000 to 10000** Å**.**



3) **Prebake**

The silicon wafers coated with photo resist are now put into an oven at about 80°C for about 30-60 minutes to remove solvents in the photo resist and to harden it into a semisolid film.

4) Mask Alignment and Exposure

A mask or "photomask" is a square glass plate with a patterned emulsion of metal film on one side. The mask is aligned with the wafer, so that the pattern can be transferred onto the wafer surface.

Once the mask has been accurately aligned with the pattern on the wafer's surface, the photoresist is exposed through the pattern on the mask with a high intensity UV light. The exposure time is generally in the range 3-10 seconds and is carefully controlled such that the total UV radiation, and then developed in a developer.

5) Post bake

After development and rinsing, the wafers are postbake in an oven at a temperature of about 150°C for about 30-60 minutes to further strengthen the remaining resist on the wafer. The photo resist adheres better to the wafer and make it more resistant to the hydrofluoric acid (HF) solution used for etching of the silicon dioxide.

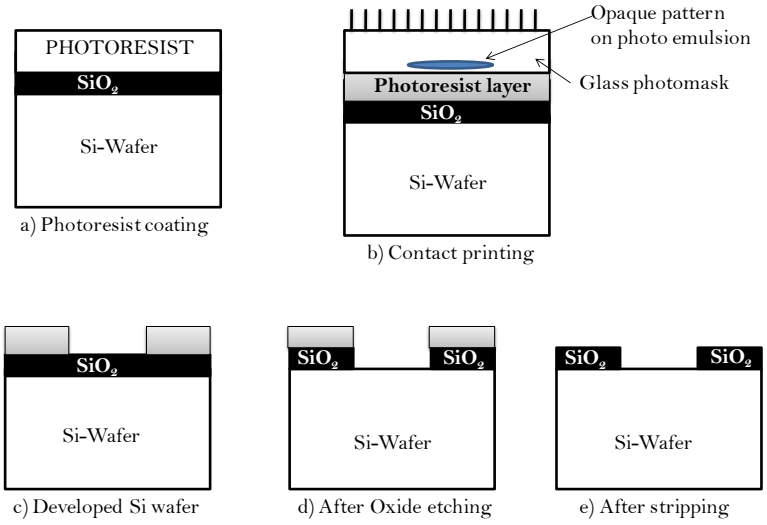
6) Oxide Etching

The remaining resist is hardened and acts as a convenient mask through which the oxide layer can be etched away to expose areas of semiconductor underneath. These exposed areas are ready for impurity diffusion.

For etching of oxide, the wafers are immersed in or sprayed with a hydrofluoric acid solution. This solution is usually a diluted solution of typically 10:1, H_2O: HF, or more often a 10:1 NH_4F: HF solution. The HF solutions will etch the SiO_2 but will not attack the underlying silicon, nor it will attack the photo resist layer to any considerable degree. The wafers are exposed to the etching solution to remove the SiO_2 completely in the areas of the wafer that are not covered by the photo resist.

7) Photoresist Stripping

Following oxide etching, the remaining resist is finally removed with a mixture of H_2SO_4 and H_2O_2 and with the help of scratch process. Finally washing and drying completes the required window in the oxide layer. The figure below shows the silicon wafer ready for next diffusion.



Photolithographic Process Steps

Negative photoresists are more difficult to remove. Positive photoresists can usually be easily removed in organic solvents such as acetone.

ETCHING

- After a photo resist image has been formed on the surface of the wafer, the next process involves transferring that image into a layer under the resist. This is done by selective removal of material from the unmasked regions. The technique by which material can be uniformly or selectively removed is called **etching**.
- Some of the etching techniques used are wet chemical etching and plasma etching.

Wet Chemical Etching

- In this process, the wafer is immersed in the etching solution at required temperature and the etching solution reacts with the exposed film to form soluble byproducts.
- A number of chemical reagents and their mixtures are used for etching purposes. Water is an intrinsic component of all these reagents.
- A common Al etchant is 20% acetic acid, 77% phosphoric acid and 3% nitric acid.
- The main problems with wet chemical etching are
  1) Wet etching is undercutting
  2) It is difficult to control
  3) It produces high defect levels due to solute particle contamination.
  4) Cannot be used for small features

5) Produces large volumes of chemical waste.

Plasma Etching

- Plasma etching is a dry etching process in which reactive gases are fed into the reaction chamber. This is excited by high strength RF field to form plasma of charged ions. These ions react with the material to be etched which evaporates off from the wafer. CF_4 is the commonly used compound for etching Si, SiO_2 and Si_3N_4.
- When these interactions are used to form volatile products so that material is removed or etched from surfaces that are not masked by lithographic patterns, the technique is known as **reactive plasma etching**.
- Plasma etching process proceeds in the following steps

1) A feed gas introduced into the chamber must be broken down into chemically reactive species by the plasma.
2) These species must diffuse to the surface of the wafer and be adsorbed.
3) The reaction product must be desorbed and should be diffused away from the wafer.
4) Finally, the reaction product should be transported by the gas flow out of the etch chamber.

Advantages of plasma etching

1) Plasmas are much easier to start and stop than wet etching.
2) Plasma etch processes are much less sensitive to small changes in the temperature of wafer.
3) There is less undercutting in plasma etching.
4) This process produces less chemical waste than wet etching.