



# On the Interconnection Complexity vs Size Trade-off in Circuit Graphs

Marieke Louage

UGent

Ghent, Belgium 0009-0002-2569-0944

Muhammad Mazher Iqbal

UGent

Ghent, Belgium 0000-0002-2421-8456

Dirk Stroobandt

UGent

Gent, Belgium 0000-0002-4477-5313

## ABSTRACT

Electronic Design Automation (EDA) for Field Programmable Gate Arrays (FPGAs) strives to optimize the timing properties of physical circuits on FPGAs. The process involves logic synthesis and packing in physical synthesis, which generates a circuit graph. This graph is subsequently placed and routed onto the FPGA architecture to create a physical circuit. Researchers have demonstrated that merely minimizing circuit size does not necessarily lead to an optimal wirelength. Namely, as circuit size decreases the interconnection complexity can (and normally does) increase. This work focuses on gaining a better understanding of this phenomenon. We investigate the trade-off between size and interconnection complexity by examining ideal circuit graphs which are an abstraction of real circuits graphs based on Rent's rule. An ideal circuit is reduced to only three parameters: size  $B_c$ , interconnection complexity  $r$  and terminals per block  $K$ . First we study the effect of size  $B_c$  and interconnection complexity  $r$  on wirelength by making a visual representation with Donath's wirelength prediction method. The created visual clearly exposes and provides insight in the trade-off between size and interconnection complexity. Furthermore, it shows that interconnection complexity is limited subject to circuit size. Second, we derive the shape of ideal circuit graphs based on its three parameters. We use the hypervolume-hyperarea interpretation of Rent's rule as a basis for constructing ideal circuit graphs. In understanding the structure of ideal circuit graphs it becomes clear why complexity is bound by size. We find that the complexity  $r$  of an ideal circuit is lower than  $\frac{\log_2(B_c)-1}{\log_3(B_c)}$ . The model for building ideal circuit graphs enhances our intuitive understanding of interconnection structure in FPGA circuits and might be the basis for a new synthetic benchmark generation technique.

## KEYWORDS

Electronic Design Automation, Interconnection Structure, Rent's Rule, Wirelength Estimation, Circuit Dimensionality, Synthetic Benchmark Design, FPGA

## ACM Reference Format:

Marieke Louage, Muhammad Mazher Iqbal, and Dirk Stroobandt. 2023. On the Interconnection Complexity vs Size Trade-off in Circuit Graphs. In *2023 ACM International Workshop on System-Level Interconnect Pathfinding (SLIP '23)*, November 2, 2023, San Francisco, CA, USA

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*SLIP '23, November 2, 2023, San Francisco, CA, USA*

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ACM ISBN 979-8-4007-0474-1/23/11...\$15.00

<https://doi.org/10.1145/3632409.3632838>

'23), November 2, 2023, San Francisco, CA, USA. ACM, New York, NY, USA, 7 pages. <https://doi.org/10.1145/3632409.3632838>

## 1 INTRODUCTION

In Electronic Design Automation (EDA) for Field-Programmable Gate Arrays (FPGAs), the objective is to create circuits with low total wirelength and low critical path wirelength. A circuit is represented by a netlist, which is a directed graph consisting of blocks as nodes that perform logic functions, and interconnections as edges that connect the input and outputs of these blocks. At different stages along the EDA pipeline, it was found that minimizing the number of blocks of a netlist does not minimize wirelength of the physical circuit. In [1] Kutzschebauch and Stok proposed to use congestion aware algorithms in logic synthesis. In [2] Dehon found that maximum LUT utilization does not optimize wirelength because of the increase in interconnection complexity. In [3] Murray et al. also found that dense packing has a negative effect on total wirelength and critical path wirelength. In [4] Hyun et al. proposed a machine learning based method for placement-aware synthesis, logic synthesis optimized for predicted wirelength. In [5] Liu and Marek-Sadowska conducted an experimental study on the relation between netlist structure and placement efficiency, they found that different placers favour different netlist characteristics and that interconnection complexity correlates with the total wirelength.

In this paper we seek to characterize the relationship of circuit graph structure on wirelength. We do this by studying abstractions of real circuits based on Rent's rule. Namely, real circuit graphs approximate a self-similar relationship between the terminals and blocks of its subcircuits that is called Rent's rule. Our ideal circuit graphs are a perfect manifestation of Rent's rule and are only dependent on three parameters: interconnection complexity  $r$ , number of blocks or size  $B_c$  and terminals per block  $K$ .

In the first part of the paper, we investigate the effect of  $r$  and  $B_c$  on wirelength by using Donath's wirelength estimation technique [9]. His method enables us to visualize the relationship between wirelength, interconnection complexity  $r$  and size  $B_c$ . This provides us with a interconnection complexity vs size trade-off that illustrates that minimizing netlist size is not always the optimal strategy. Moreover, it shows that interconnection complexity is bound subject to circuit size. Then, we continue with evaluating the obtained trade-off for ideal circuit graphs on realistic circuit graphs. For this purpose we use two distinct sets of benchmarks: one comprising synthetic benchmarks that are designed to be similar and another featuring realistic benchmarks unrelated to another.

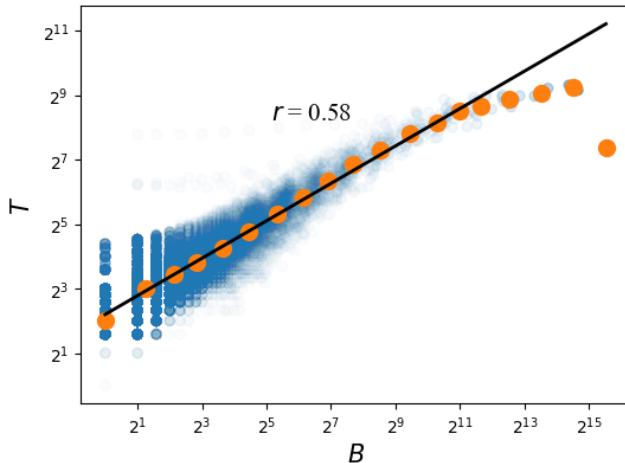
The second part of the paper works towards understanding the ideal circuit graph structure itself. We give a method to construct ideal circuit graphs subject to its three parameters  $r$ ,  $B_c$  and  $K$ .

This provides the reader with an intuitive understanding of interconnection complexity. With this method, it becomes evident why interconnection complexity is bound by a finite circuit size, illuminating the observation made in the wirelength characteristic.

The rest of the paper is organized as follows. In Section 2 we introduce Rent's rule, Donath's wirelength estimation method and explain how the synthetic benchmarks used for evaluation are created. In Section 3 we present a wirelength characteristic, that gives a visual relationship between total wirelength, size and interconnection complexity. In the same section, we evaluate the obtained wirelength characteristic with both a synthetic benchmarks set with similar circuits and a real benchmark set with unrelated circuits. In Section 4 we present a model for generating circuits of a certain Rent exponent and derive an upper bound on circuit complexity for a given circuit size. We conclude the paper in Section 5 and describe future work in Section 6.

## 2 METHODS

### 2.1 Rent's rule



**Figure 1:** A typical Rent characteristic. The blue dots represent partitioned subcircuits and the orange dots represent the binned averages.

In [6] Landman and Russo found that logic graphs have a self-similar structure characterized by a fixed relationship between  $T$ , the average number of terminals and  $B$ , the average number of blocks of optimal circuit partitions. This relationship is called Rent's rule:

$$T = KB^r \quad (1)$$

Here,  $K$  is the average number of terminals per block and  $r$  is the Rent exponent. Rent's rule shows that the number of terminals is a power of the number of blocks at different hierarchical partitions of the circuit. The Rent exponent  $r$  is a measure of interconnection complexity of the circuit. Circuits with a higher  $r$  are more connected and are generally harder to place and route. Theoretically,

$r$  can be any number between 0 and 1, in reality  $r$  typically lies between 0.5 and 0.75.

Figure 1 shows Rent's rule for a realistic circuit. The circuit is recursively partitioned in two parts, with the objective of minimizing the number of terminals of the sub-circuits. Each sub-circuit is represented by a blue data point on the graph. On a log-log plot, the Rent's rule power law is transformed to a linear relationship and the slope of the line is the Rent exponent  $r$ . The self-similar structure breaks at higher blocks counts, as can be seen by the samples deviating from the line. This behaviour is designated Rent region II and occurs because the number of input and output terminals of a chip is (artificially) bounded by physical restrictions.

In [7] Ozaktas described a multidimensional interpretation of Rent's rule: the terminal-block relationship can be seen as a hyperarea-hypervolume relationship. The (fractal) hypervolume dimension  $D_v$  of a circuit is:

$$D_v = \frac{1}{1-r} \quad (2)$$

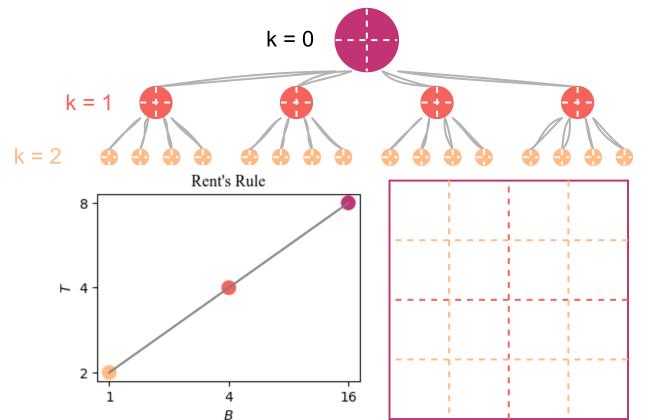
The hypersurface dimension  $D_s$  is :

$$D_s = D_v - 1 \quad (3)$$

A Rent exponent  $r$  of 0.5 has a  $D_s$  of 1 and a  $D_v$  of 2, this corresponds with a shape in 2D: the perimeter scales linearly and the area scales quadratically. Similarly, a Rent exponent of 0.67 has a  $D_s$  of 2 and a  $D_v$  of 3, this corresponds with a shape in 3D: the area scales quadratically, while the volume scales cubically.

In [8] Stroobandt also found this relationship and described that regular meshes, such as the one for Rent exponent 0.5 displayed in Figure ??, obey Rent's Rule.

### 2.2 Donath's Wirelength Estimation Method



**Figure 2:** Donath's wirelength estimation method. A circuit is recursively partitioned in 4 subcircuits which yields the Rent characteristic. The circuit is placed on an equally sized recursively partitioned architecture.

In [9] Donath proposed a technique for estimating the total wirelength of a circuit based on the terminal-block relationship

described by Rent's rule. The method simulates a recursive partitioning optimized placement algorithm and extracts a stochastic wirelength estimation at each stage.

Figure 2 shows the idea. First, a circuit with size  $B_c = 4^n$  is recursively partitioned in four parts such that the number of cut interconnects is minimized at each level  $k$ . The obtained  $(B_k, T_k)$  pairs form a Rent characteristic of the circuit, and expose the interconnection complexity  $r$  of the circuit. Then, the partitioned circuit is virtually placed on a square architecture of size  $4^n$  also recursively partitioned in four smaller squares as shown in the figure.

This virtual placement consists of a recursive assignment of the circuit partitions to the architecture partitions. At each level  $k$ , the estimated average wirelength of the cut wires  $L_k$  is directly proportional to the length of the sides of the architecture partition

$$L_k \propto \sqrt{B_k} \quad (4)$$

The number of cut wires on level  $k$  is

$$W_k = \frac{4 \times T_k - 1 \times T_{k-1}}{2} \quad (5)$$

The total estimated wirelength is

$$L_c = \sum_{k=1}^n W_k \times L_k \quad (6)$$

The estimation gives the sum of all internal wires, wires connecting to IOs are ignored.

### 2.3 Ideal circuit graphs

In this paper we study ideal models of circuit graphs that perfectly obey Rent's rule. These ideal circuit graphs are largely constrained by Rent's rule and are reduced to three parameters:

- Interconnection complexity  $r$
- Circuit size  $B_c$
- Terminals per block  $K$

### 2.4 Realistic circuit graphs

Although this is not the main focus of the paper, we also briefly look at realistic circuit graphs. We evaluate how the theoretical claims about ideal circuit graphs with regard to wirelength hold when working with real circuit graphs. To this end we use version 8 of the Versatile Place and Route (VPR) tool for physical design and two sets of benchmarks for the stratixiv\_arch.timing.xml architecture.

The first benchmark set is the publicly available Titan benchmark suite [3]. The second is a synthetic benchmark set custom-made for the stratixiv\_arch.timing.xml architecture, the synthetic benchmarks are clones of a Titan benchmark that vary in  $r$  and  $B_c$ . Here we describe how we extended the synthetic benchmark generation tool Generate Netlist (GNL) [11] developed by Stroobandt et al. to generate circuits for the the stratixiv\_arch.timing.xml based on an existing benchmark. GNL generates an interconnection structure given a set of blocks and an  $r$  according to Rent's Rule. There is no interpretation of signals, but to make a benchmark for a we need specific control signals for various circuit elements. The architecture has Complex Logic Blocks (CLBs), Block Random Access Memory

(BRAM) and Digital Signal Processing Logic element (DSPs). In addition, CLBs can be assigned to work together in a carry chain. The control paths of these elements cannot be generated with GNL. Therefore we proceed as follows: the data path, which forms the bulk of interconnections, can be random and is generated with GNL. The control path is added afterwards with regard to some constraints.

To produce synthetic benchmarks of size  $B_c$  and Rent exponent  $r$ , the following steps are taken:

- (1) The block distribution is collected from the reference Titan benchmark. This consists of the number of occurrences of each unique block and its properties (block type, I/O counts, the sequential or combinational property).
- (2) The block distribution, including IO blocks, is scaled to obtain the desired circuit size.
- (3) The interconnections are added in two steps.
  - GNL generates the datapath interconnections.
  - The control ports are copied from the original benchmark and adjusted to fit the new size. The carry chains need special care: we randomly distribute CLBs in groups of similar size as in the original benchmark. We wire the carry chains control ports and decouple the data ports with flip flops so that two carry chains are never combinationally connected.

The extended GNL tool is used to generate a synthetic benchmark set of 55 circuits. The sparcT1\_core\_stratixiv\_arch\_timing Titan benchmark is used as the base benchmark. Circuits for every combination of Rent exponents  $[0.4, 0.45, 0.5, 0.55, 0.6]$  with scale factors for scaling the circuit size  $[\frac{1}{2}, \frac{1}{\sqrt{2}}, 1, \sqrt{2}, 2]$  plus every combination of Rent exponents  $[0.65, 0.7, 0.75, 0.8, 0.85, 0.9]$  with scale factors  $[\frac{1}{4\sqrt{2}}, \frac{1}{4}, \frac{1}{2\sqrt{2}}, \frac{1}{2}, \frac{\sqrt{2}}{2}]$  are generated.

GNL has no mechanism to control logic depth, consequently the generated benchmarks do not have a reliable logic depth distribution and critical path. Therefore, these synthetic benchmarks are packed, placed and routed with VPR with all timing optimized options turned off. The Titan Benchmarks suite is run twice, once with timing optimized options turned on and once with timing optimized options turned off.

## 3 WIRELENGTH OF CIRCUIT GRAPHS

How do the parameters interconnection complexity  $r$  and size  $B_c$  influence the wirelength  $L_c$  of a circuit? What is the maximum wirelength that can be obtained for a circuit size  $B_c$  and at what interconnection complexity  $r$  is it found? In what follows, we will use ideal circuit graphs and Donath's wirelength estimation method to show that there is clearly a trade-off between  $r$  and  $B_c$ . We also briefly discuss the results for realistic circuit graphs with Donath's method but do not go into detail in this paper.

### 3.1 Ideal circuit graphs

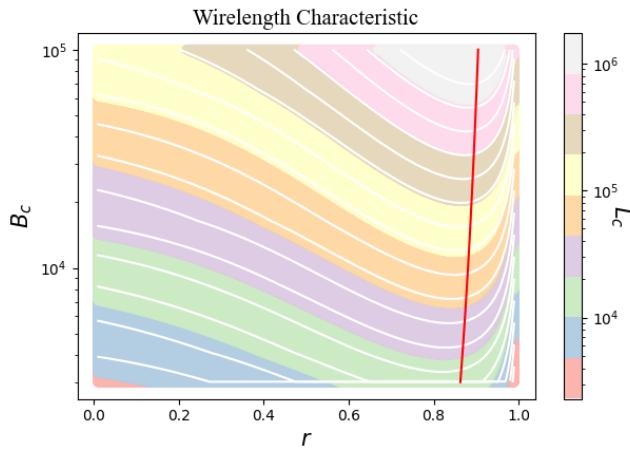
Ideal circuit graphs are summarized by  $r$ ,  $B_c$  and  $K$ . These parameters carry enough information to make a wirelength prediction with Donath's wirelength estimation method. We estimate the wirelength over a range of  $r$  and  $B_c$  values. To work with circuit sizes  $B_c | \#n \in \mathbb{N} : B_c = 4^n$ , we do the following.

Again, the circuit is recursively partitioned in four. But there can only be clusters containing a natural number of blocks. Consequently, if  $B_k$ , the number of blocks per partition at level  $k$ , is not a natural number, the partitions are regrouped in  $i$  clusters of size  $\lfloor B_k \rfloor$  and  $j$  clusters of size  $\lceil B_k \rceil$  such that:

$$i \times \lfloor B_k \rfloor + j \times \lceil B_k \rceil = B_k \quad (7)$$

The number of wires is directly derived from the number of terminals of the clusters which can be found with equation 1. The used FPGA architectures are rectangular instead of square. This is not a problem when comparing estimated wirelength between different circuits as long as the architectures have a fixed  $b \times h$  ratio. The average wirelength scales the same way as on a square architecture, wirelength( $k$ ) is half of wirelength( $k-1$ ). We execute Donath's method with the proposed interpolation method over a range of Rent exponents  $r$  and sizes  $B_c$  and obtain the graph shown in Figure 3. This graph, further called the wirelength characteristic, shows the relationship between total wirelength, circuit size and Rent exponent. The size axis and wirelength axis have a logarithmic scale and the Rent exponent axis has a linear scale. The white lines connect points of equal wirelength, two adjacent lines differ by a factor of two.

The wirelength characteristic clearly shows that there is a trade-off between size and interconnection complexity. For typical Rent exponents  $r | r \in [0.5, 0.75]$  decreasing the circuit size  $B_c$  lowers the total wirelength, only if  $r$  does not increase too much. This aligns with the findings of Murray et al. on packing [3]: packing LUTs too dense has negative effects on the wirelength.



**Figure 3: The wirelength characteristic shows the relationship between circuit size  $B_c$ , interconnection complexity  $r$  and wirelength  $L_c$ .**

### 3.2 Bound on wirelength

The wirelength characteristic shows that there is a maximum wirelength that ideal circuit graphs with a certain circuit size  $B_c$  can have. The maximum wirelength  $L_{c,max}(B_c)$  occurs at a certain

interconnection complexity which we will call:

$$r_{mw}(B_c)$$

A higher interconnection complexity results in a lower wirelength estimation. In Section 4 we will explain this by focusing on the interconnection structure itself.

### 3.3 Realistic circuit graphs

Realistic circuit graphs differ from ideal ones in that they only approximate Rent's rule and are not fully captured in the three parameters  $r$ ,  $B_c$  and  $K$ . However, there is certainly a trade-off between size and interconnection complexity to be found in realistic circuit graphs.

To this end, we abstract the benchmarks with  $r$ ,  $B_c$ ,  $K$  and an estimated wirelength  $L_{c,estimated}$  using Donath's method. Next we obtain the real wirelength  $L_{c,real}$  by running the benchmarks through physical synthesis with VPR. And in the end, we compare  $L_{c,real}$  against  $L_{c,estimated}$ .

We wish to find the same scaling factor in estimated wirelength and routing wirelength. If the estimated wirelength of circuit1 is two times the estimated wirelength of circuit2, we want the routing wirelength of circuit1 to be two times the routing wirelength of circuit2.

Figure ?? and ?? show a log-log plot of  $L_{c,real}$  against  $L_{c,estimated}$  for the GNL clones benchmarks and the Titan benchmarks respectively. The synthetic benchmark suite, a change in estimated wirelength is well reflected in a change in real wirelength. The Titan benchmark suite on the other hand, shows the right overall trend, but there are cases where estimated wirelength doubles while the routing wirelength decreases.

The synthetic benchmark suite is designed to contain realistic circuits (not ideal circuits) that vary in  $r$  and  $B_c$  but are otherwise highly similar. This is done with the underlying thought that this best reflects instances of a circuit under transformation. Where by minimization operations,  $B_c$  and  $r$  change, but otherwise remain fairly similar. This is not confirmed and needs further research.

## 4 STRUCTURE OF CIRCUIT GRAPHS

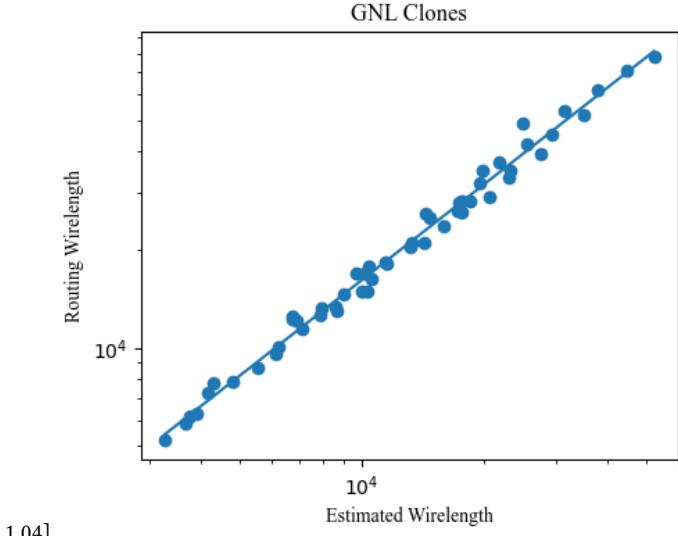
Knowing that ideal circuit graphs have three parameter constraints  $r$ ,  $B_c$  and  $K$ , can we imagine what these graphs look like? Here we display a method for generating ideal circuit graphs. From this analysis a relationship between  $r$  and  $B_c$  rises: namely  $B_c$  limits  $r$ .

### 4.1 Model for building infinite ideal circuit graphs

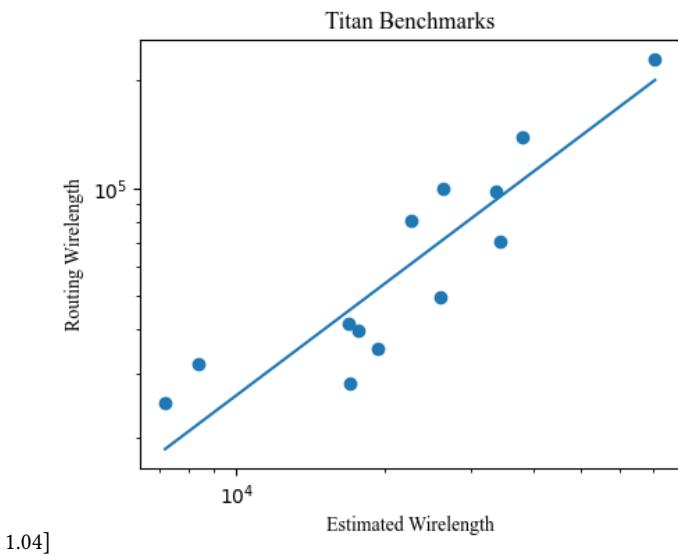
First, we will describe a method for building infinite ideal circuit graphs. These are only subject to the parameters  $r$  and  $K$ , and not bound by a size  $B_c$ .

First we make circuits of Rent exponent  $r = 0.5$  and then generalize for other values. Circuits of  $r = 0.5$  have a dimensionality  $D_v$  of 2 and  $D_s$  of 1. Consequently, the terminal-block relationship is like the perimeter-area relationship of a 2D shape. To achieve that the blocks relate to area, they are evenly distributed over a plane. Similarly, to achieve that terminals relate to the perimeter, we require a uniform interconnection structure such that the number

[Synthetic benchmark set. Pearson correlation coefficient: 0.99  
Slope:



[Titan benchmark suite. Pearson correlation coefficient: 0.95  
Slope



**Figure 4: Predicted wirelength versus routed wirelength. Ideally the slope between every two points is 1.**

of interconnections cut is (approximately) linear with the length of the cut.

This leads to Figures ?? and ???. The first image shows a circuit where each block has eight terminals ( $K = 8$ ) and is connected to all its neighbours. The second image shows a circuit where  $K = 24$  and the blocks are also connected to second neighbours. In these two circuits, the terminal-block relationship of partitions is a perimeter-area relationship. This is visualized with the red selection boxes. The

number of blocks is directly proportional to the area of the square and the number of terminals with the perimeter of the square.

Next to these perfect cases, we can make circuits of any  $K$  that also obey Rent's rule. For example, if we randomly remove about half of the wires from Figure ??, the average number of terminals per block  $K$  becomes 4. An example is shown in Figure ???. On average halve of the tracks on the perimeter will be erased on random places. For a large enough cut or sample, the linear scaling property remains. Another, (very specific) example is the regular shaped grid shown in Figure ??, .

In general, a method for generating ideal circuit graphs with Rent exponent  $r$  and terminals per block  $K$  is:

- (1) Arrange the desired number of blocks in the related  $D_v$  dimensional space. The number of neighbours each block has in  $D_v$  space is  $3^{D_v} - 1$ .
- (2) Randomly assign  $K$  interconnections between each block and its neighbours. Neighbours at an equal distance have the same probability. First line of neighbours have the highest probability, second neighbours lower, etc.

This results in a unbound homogeneous circuit graph.

## 4.2 Model for building finite ideal circuit graphs

Starting from an infinite ideal circuit graph, we can transition to an ideal circuit graph with a finite circuit size  $B_c$ . We select  $B_c$  blocks that become part of the circuit, the other blocks become virtual blocks. The interconnection from circuit blocks to virtual blocks become I/O terminals of the circuit. This is shown in Figure 6.

## 4.3 Bound on interconnection complexity for finite circuit graphs

The number of neighbours one block has in a  $D_v$  space is given by:

$$B_{\text{neighbours}} = 3^{D_v} - 1 \quad (8)$$

This is visualized for  $D_v = 2$  and  $D_v = 3$  in Figure 7. Each connection between the block and its neighbours is equally likely. If the circuit size  $B_c$  is equal to  $3^{D_v}$  then there can only be one block that is connected to all other blocks in the circuit. The other blocks have (a) virtual neighbour(s) that generate I/O when connected.

Now, if the circuit size  $B_c$  is smaller than  $3^{D_v}$ , there can be more than one block that is connected to all other blocks in the circuit, but each block has virtual neighbours that give rise to I/O. More connections will fall outside of the chip.

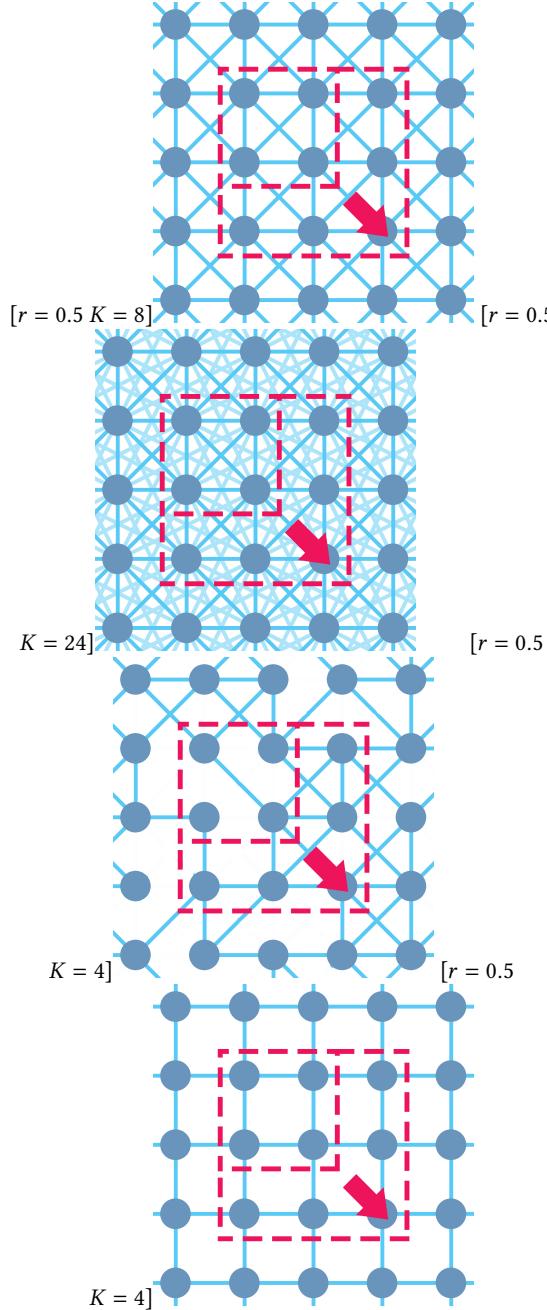
An upper bound on dimensionality with respect to the number of blocks  $B_c$  is therefore:

$$D_{m, B_c} = \log_3(B_c) \quad (9)$$

The corresponding Rent exponent is:

$$r_{mc, B_c} = \frac{\log_3(B_c) - 1}{\log_3(B_c)} \quad (10)$$

This maximum complexity Rent exponent  $r_{mc, B_c}$  marks an upper bound on the maximum wirelength Rent exponent  $r_{mw}(B_c)$ . Namely, each block is already connected with all other blocks by a at least a distance of two. A further increase in dimensionality



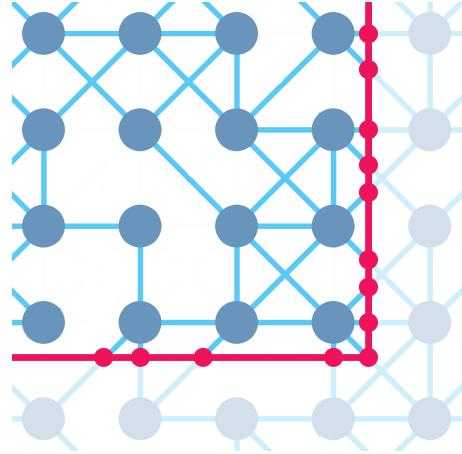
**Figure 5:** These are 2 dimensional circuits with a terminal-block relationship equal to a perimeter-area relationship.

cannot result in more connected blocks, but will instead create more external interconnections. Therefore:

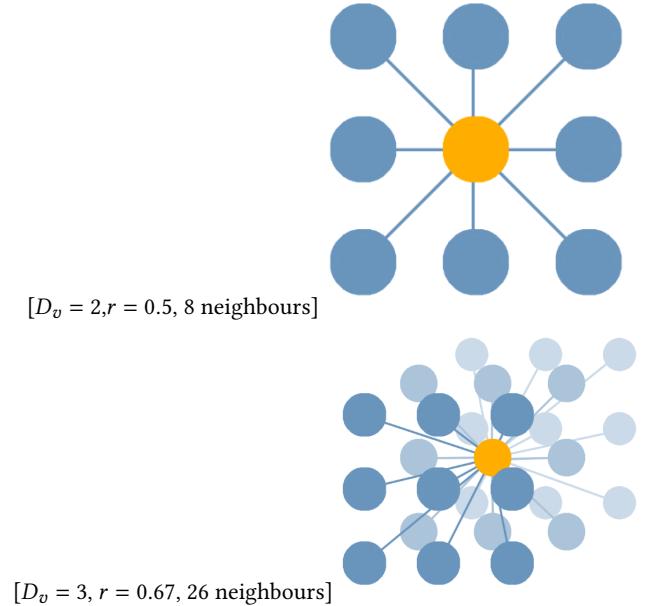
$$r_{mc}(B_c) < r_{mc}(B_c) \quad (11)$$

$r_{mc,B_c}$  is plotted in red in Figure 3 and correlates well with the maximum wirelength Rent exponent  $r_{mw}(B_c)$ .

From  $r_{mc,B_c}$  on the circuit size is too small to accommodate the level of interconnection complexity asked by the Rent exponent. A



**Figure 6:** Connections from circuit blocks to virtual blocks give rise to I/O terminals visualised by the red dots.



**Figure 7:** A block and its neighbours in  $D_v$  space.

further increase in complexity, introduces more virtual neighbours which results in more external interconnections. When the Rent exponent is 1, the dimension and the number of neighbours are infinite. There are infinitely many virtual neighbours and the chance of interconnecting with a neighbour falling inside the chip bounds is zero. Every interconnection falls outside the chip consequently the wirelength inside the chip is zero. This can be seen in Figure 3 by the asymptotic behaviour of the equal wirelength lines as they approach 1.

#### 4.4 Difference with realistic circuit graphs

Where ideal circuits have a constant interconnection complexity  $r$  throughout the entire circuit, real circuits have local variations in interconnection complexity. This is described by Marek et al. as local Rent exponents [12]. This might be taken care of by arranging blocks in a grid with varying dimensions provided this is possible. Though it is easy to imagine a 2D arrangement with locally thickened spots of 3D space.

### 5 CONCLUSION

In this paper we studied ideal circuit graphs to better understand the relationship between interconnection complexity and size in circuit graphs. First, we presented a wirelength characteristic that visually shows how wirelength, circuit size and Rent exponent interact for ideal circuit graphs. This wirelength characteristic shows a clear trade-off between size and interconnection complexity. The predicted change in wirelength of ideal circuit graphs was evaluated for real circuit graphs. A synthetic benchmark suite made of highly similar circuits, reflected the trade-off well. The trade-off is less visible in the more heterogeneous Titan benchmark suite. In addition, the wirelength characteristic shows that the interconnection complexity is limited subject to the circuit size. Second, we described a model for generating circuits of a certain Rent exponent. Based on the analysis, we defined a formula for an upper bound on interconnection complexity. The method provides an intuitive way of imagining circuits in terms of their interconnection complexity.

### 6 FUTURE WORK

In future work we will further explore the wirelength characteristic. It gives valuable information on the size vs interconnection complexity trade-off and we will use it to evaluate dense packing. On another path we will explore the possibilities for a synthetic benchmark generation tool. The multi-dimensional interconnection structure analysis provides a basic strategy for a benchmark generation technique: first arrange blocks in D space, then randomly assign neighbours by a cost function. However, it remains to be explored how grids in fractal dimensions can be assembled. And, how to mimic variations in interconnection complexity described by local rent exponents.

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