# Cryo-CMOS Electronic Control for Scalable Quantum Computing: Invited

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# INVITED Cryo-CMOS Electronic Control for Scalable Quantum Computing

Fabio Sebastiano[1], Harald Homulle[1], Bishnu Patra[1], Rosario Incandela[1], Jeroen van Dijk[1], Lin Song[1,2], Masoud Babaie[1], Andrei Vladimirescu[1,3], Edoardo Charbon[1,4,5]
[1]Delft University of Technology, Delft, The Netherlands,[2]Tsinghua Univ., Beijing, P.R. China, [3]U.C. Berkeley, Berkeley, CA, U.S.A. [4]Intel Corp., Hillsboro, OR, U.S.A., [5]EPFL, Neuchâtel, Switzerland
f.sebastiano@tudelft.nl

## ABSTRACT

Quantum computers[1] could revolutionize computing in a profound way due to the massive speedup they promise. A quantum computer comprises a cryogenic quantum processor and a classical electronic controller. When scaling up the cryogenic quantum processor to at least a few thousands, and possibly millions, of qubits required for any practical quantum algorithm, cryogenic CMOS (cryo-CMOS) electronics is required to allow feasible and compact interconnections between the controller and the quantum processor. Cryo-CMOS leverages the CMOS fabrication infrastructure while exploiting the continuous improvement of performance and miniaturization guaranteed by Moore's law, in order to enable the fabrication of a cost-effective practical quantum computer. However, designing cryo-CMOS integrated circuits requires a new set of CMOS device models, their embedding in design and verification tools, and the possibility to co-simulate the cryo-CMOS/quantum-processor architecture for full-system optimization. In this paper, we address these challenges by focusing on their impact on the design of complex cryo-CMOS systems.

## CCS CONCEPTS

**Hardware → Quantum computation**; **Electronic design automation**; Analog and mixed-signal circuits; Application specific integrated circuits.

## KEYWORDS

Cryo-CMOS, cryogenics, quantum computation, qubit, error-correcting loop, device models.

## 1 INTRODUCTION

Quantum computers hold the promise to successfully address computational problems that are intractable by standard computing paradigms. These problems include efficient search in extremely large datasets, factorization of large integers in their prime factors and simulations of quantum systems for the optimization of drug synthesis, materials and industrial chemical processes [1]. In a quantum computer, standard logic bits are replaced by quantum bits (qubits), which can be represented as a point on the surface of a three-dimensional sphere, the so-called Bloch sphere, shown in Figure 1. In this construct, standard logic '1' and '0' are replaced by quantum states $|0\rangle$ and $|1\rangle$, and are manipulated, so as to exploit the fundamental phenomena of quantum mechanics for computation, i.e. superposition and entanglement [2]. Qubits can exist in a superposition of both state $|0\rangle$ and $|1\rangle$ simultaneously, which results in a computing power that doubles with every additional qubit, thus resulting in a massive speedup with respect to traditional computers. For example, it has been estimated that the state of a 50-qubit system cannot be stored in the memory of the world's most powerful computers today [3].

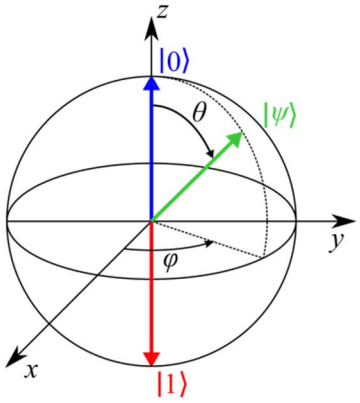


**Figure 1. Bloch sphere representation of a qubit.**

In addition to a quantum processor comprising several qubits, a quantum computer also requires a classical controller to manipulate and read out qubit states (Figure 2). Classical controller and quantum processor must be placed in close proximity, because of the need for physical interconnections between them. This requirement will be especially stringent when the number of qubits, and hence the wires connecting them, will grow to very large numbers. Since most quantum processors nowadays require operation at deep-cryogenic temperature well below 1 K, such as in the examples shown in Figure 2, the


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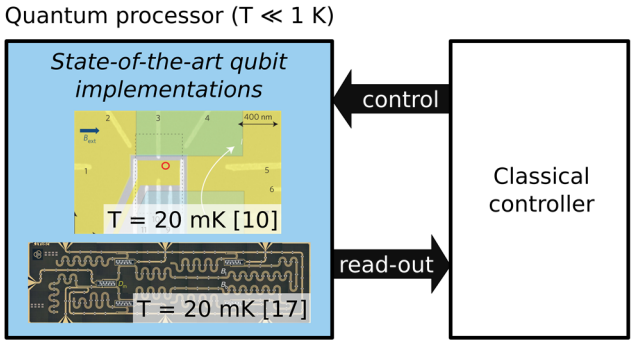


**Figure 2. Quantum-classical interface.**

classical controller must also operate at cryogenic temperature. To address this issue, a cryogenic CMOS (cryo-CMOS) electronic controller has been proposed [4]-[7]. The controller must satisfy stringent requirements on noise, accuracy, and bandwidth, in order not to reduce qubit performance, and to comply with power dissipation limits imposed by the cooling technology. Meeting those demands requires effort and innovations both in the development of new system and circuit architectures and in the creation of novel design and verification strategies and tools. In regard to design tools, few topics require specific attention: the co-simulation of the electronic interface with the quantum processor for a full system optimization; the need for models of CMOS devices operating at cryogenic temperature and their embedding in commercial EDA tools to enable the design of complex circuits and systems.

In this paper, we focus on those challenges and their impact on the design of complex cryo-CMOS circuits. The paper is organized as follows. The motivations and the requirements for the cryo-CMOS controller are presented in section 2. Section 3 and 4 discuss the challenges for the development of the quantum-processor/controller co-simulations and cryo-CMOS device models, respectively, while remarks on cryo-CMOS design automation occupy section 5. Conclusions are drawn in section 6.

## 2 THE NEED FOR CRYO-CMOS CONTROL

Several physical implementations have been proposed for qubits, however solid-state alternatives are currently the most promising in terms of scalability to a large number of qubits, although no more than a dozen qubits have been demonstrated in such platforms so far [8]. Solid-state qubits come in several variants, such as electron spins in quantum dots, superconducting circuits, and nitrogen-vacancies in diamond lattices [9]-[20]. A common feature of most of those technologies is the required operation at deep-cryogenic temperatures, typically below 100 mK. This is required both to expose their quantum behavior and to increase the coherence time of their quantum state. The coherence time is usually far below a second, that is a time frame much shorter than what is required for the execution of any practical quantum algorithms. Consequently, to counteract the loss of the quantum state, quantum error-correction techniques have been developed to exploit information redundancy by encoding the quantum information on a large number of qubits, thus trading off simplicity for fidelity in execution of the quantum algorithm [21]. Thus, although a quantum computer with 50 *logical* qubits can already exceed the memory capabilities of today's supercomputers and non-trivial quantum chemistry problems can be solved with the availability of just 100 *logical* qubits [22], thousands, or even millions, of *physical* qubits, i.e. the real physical devices, are required to enable practical quantum computation.

The classical controller in Figure 2 must serve this large number of qubits by taking care of the execution of the quantum algorithm and, in parallel, by implementing an error-correction loop intended to maintain the fidelity of the computation beyond coherence times. Interfacing solid-state qubits usually involves the generation and acquisition of purely electrical signals, such as microwave bursts with frequencies ranging from a few GHz to tens of GHz and voltage and current pulses with a bandwidth of tens of MHz.

Since existing state-of-the-art quantum processors comprise only a few qubits, most of the electronics making up the classical controller operate at room temperature and it is wired to the qubits in the cryogenic chamber. Only a few functionalities, such as low-noise amplification of read-out signals and attenuation of control signals, are implemented at cryogenic temperature in close proximity to the quantum processors. However, when scaling up the number of qubits to the large number required for any practical computation, this approach may incur a number of limitations, including the thermal load of the large number of cables, or the latency of the error-correction loop [23]. Although there is not yet a general consensus about whether those limitations are critical or may be circumvented in the near future, it is clear that wiring thousands of low-frequency and high-frequency wires from room temperature to the cryogenic quantum processor would lead to an extremely expensive, bulky, unreliable and, hence, unpractical quantum computer.

As an alternative, a cryogenic controller may be employed, in order to relieve the requirements on interconnections, system size and reliability. Several technologies have demonstrated functionality at cryogenic temperature, such as junction field-effect transistors (JFET), high-electron-mobility transistors (HEMT), superconducting devices based on Josephson junctions, compound semiconductors (e.g. GaAs) and CMOS transistors [24][25]. However, by relying on the progress of the semiconductor industry, only CMOS technology can ensure low power consumption and functionality down to 30 mK [7][26], while offering the integration of billions of transistors on a single chip, as it will be required to handle the complexity of future quantum processors. Moreover, CMOS is preferred also because the design automation infrastructure is very mature for the standard industrial and military temperature ranges, i.e. down to -55 °C.

Figure 3 shows a generic platform for control and read-out of a quantum processor. It comprises a frontend for (de)multiplexing, amplification, analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC) for the analog signals coming from and

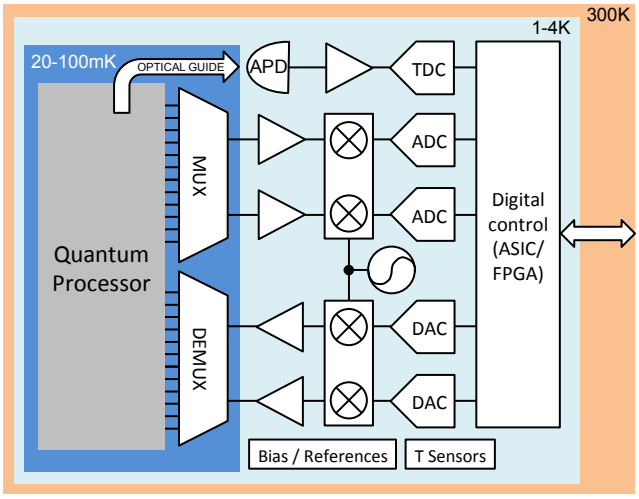


**Figure 3. Generic electronic platform for the control and read-out of quantum processors.**

feeding to all qubits. Ideally, quantum processors and electronics should operate at the same temperature, if not even on the same chip, to eliminate the need for any off-chip interconnect. However, currently available refrigeration technologies limit the available cooling power to less than ~1 mW at temperature below 100 mK [28], and it is unlikely that the full electronic controller can operate with such power budget in the near future. On the contrary, a cooling power exceeding 1 W is usually available at the 4-K stage, thus allowing the majority of the electronics to operate there. A limited amount of low-power electronics, including (de)multiplexers to reduce the number of connections to the 4-K stage, is envisioned to operate at the same temperature as the quantum processor, as shown in Figure 3.

The specifications for the cryo-CMOS electronic controller are extremely challenging. To ensure the target performance in the quantum processor, electronic signals driving the qubits must be highly accurate (in terms of amplitude, timing, frequency and phase) and contribute a negligible amount of noise. As a comparison, the control of state-of-the-art quantum processors is achieved by using the most accurate (and expensive) bench-top electronic instrumentation available on the market [9]-[20]. The read-out must be very sensitive to detect the weak signals from the quantum processor [6], and to ensure a low kickback, so as to avoid altering qubit states. These specifications must be granted while keeping the latency of the error-correction loop much lower than the qubit coherence time. Moreover, while ensuring the above-mentioned functionalities and specifications, the controller must dissipate very low power. Although more than 1-W cooling power is available at 4 K, a processor with only 1000 qubits would limit the power budget to 1 mW/qubit, which is already very challenging, as shown in [6]. Thus, while targeting for a power budget of 1 mW/qubit is ambitious, but probably achievable in the short and medium term, it becomes clear that the development of advanced cryo-CMOS systems must go hand in hand with the development of more advanced and powerful refrigeration systems.

**Table 1. Error sources for a microwave pulse for single-qubit operation (assuming a square pulse).**

| | |
|---|---|
| Microwave frequency | Accuracy |
| | Noise |
| Microwave amplitude | Accuracy |
| | Noise |
| Microwave duration | Accuracy |
| | Noise |
| Microwave phase | Accuracy |
| | Noise |

In addition to the above-mentioned challenges, proper design tools and design flows are required to support the development of a complex system as the one in Figure 3. Cryo-CMOS can already exploit the design automation infrastructure already in place for standard CMOS. However, specific issues related both to the operation at cryogenic temperature and the interfacing with a quantum system must be addressed, as elaborated in the following sections.

## 3 CO-SIMULATING THE ELECTRONIC CONTROLLER AND THE QUANTUM PROCESSOR

The tight power budget coupled with very demanding specifications calls for a careful system optimization. While electronic controllers operating at room temperature can be overdesigned to make the performance of the full quantum computer limited by the qubits by a wide margin, this cannot be allowed in a cryogenic implementation. It is then necessary to understand clearly the effect of any non-ideality of the electronic controller on the system performance.

For example, in the case of spin qubits and transmons [10][17], single-qubit operations, i.e. rotations of the qubit state $|\psi\rangle$ in the Bloch sphere in Figure 1, can be executed by exciting the qubit with a microwave pulse with a specific carrier frequency and phase and specific pulse shape, amplitude and duration, which all together determine the axis of rotation and the angle of rotation in the coordinate system in Figure 1. The possible error sources for this example are listed in Table 1. Any error or any additional noise on the pulse parameters would cause an error in the operation that can be quantified by the *fidelity* of the quantum operation [27]. The fidelity, which should be as close as possible to 100%, is a measure of the reliability of the quantum operation, similar to the Bit Error Rate (BER) for classical communication systems. Knowing how much each single source of error contributes to the final fidelity enables a better optimization of the design, since, for example, providing accuracy/noise in the pulse amplitude may be more expensive in terms of power consumption than ensuring accuracy/noise in the pulse duration. Error budgeting for a minimum power consumption would then become possible.

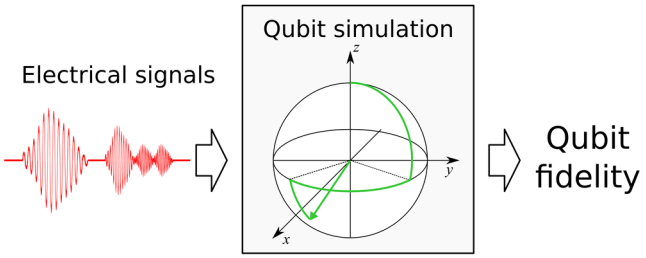


**Figure 4: Process for the co-simulation of the electronic controller and the quantum processor.**

For this purpose, we have developed a MATLAB simulation tool that receives as input a description of the required electrical signals and simulates the quantum system with those excitations by numerically solving the Schrödinger equation (Figure 4). As a result, the fidelity of the operation is computed. Since the simulation is computationally intensive, we are currently only able to simulate two spin qubits. However, since this allows the simulation of single- and two-qubit operations and qubit read-out (which are sufficient building blocks for most quantum computer implementations), it is sufficient, together with a theoretical model, to derive an accurate error budget for the general electronic platform of Figure 3. Moreover, the MATLAB model of the quantum processor can be used for verification of the developed cryo-CMOS circuit during the design phase (or during experimental validation before connection to the quantum processor): the simulated (or measured) output waveforms could be fed to the qubit simulator while the electrical signals generated for the read-out can be passed to the circuit simulator.

This represents the first step towards a fully integrated environment for the design and verification of the controller/quantum-processor system, although several challenges are already in sight. First, it is well known that quantum systems cannot be efficiently simulated with traditional computers, and it is unclear how the simulations can be extended to a larger number of qubits that can better represent a real scenario. Furthermore, it would be convenient to embed the qubit simulation in commercial EDA design/verification flows and tools. Finally, it will be necessary to fully or partially integrate the physical simulation of qubit into the full design/validation stack of the quantum system [29], which includes the infrastructure for the quantum microcode execution and for the quantum compiler on top of the above-discussed physical layer.

## 4 CRYO-CMOS DEVICE MODELING

Accurate device models are required to reliably design and simulate complex cryo-CMOS circuits. At deep-cryogenic temperature, many physical parameters that determine transistor behavior, such as carrier mobility, show a strong deviation from room temperature. This results, for example, in a larger drain current and higher threshold voltage at 4 K. In addition, several non-idealities that are specific to the cryogenic operation appear, such as the a so-called 'kink', i.e. a sudden increase in drain current at high drain-source voltage, and hysteresis in the drain

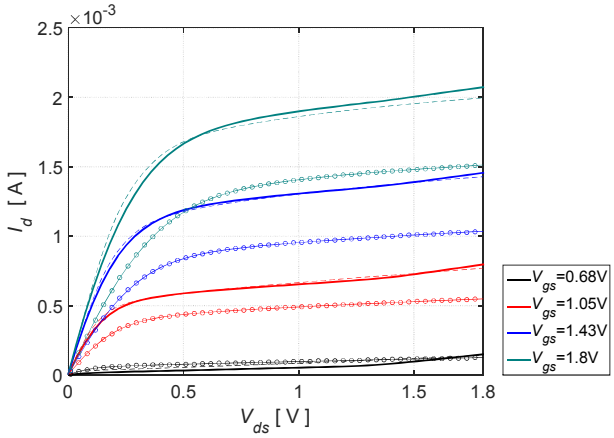


**Figure 5: I-V characteristics of a 2320 nm/160 nm NMOS fabricated in 160-nm CMOS: measurements at 300 K (dotted lines) and 4 K (solid lines); SPICE-compatible model (dashed lines).**

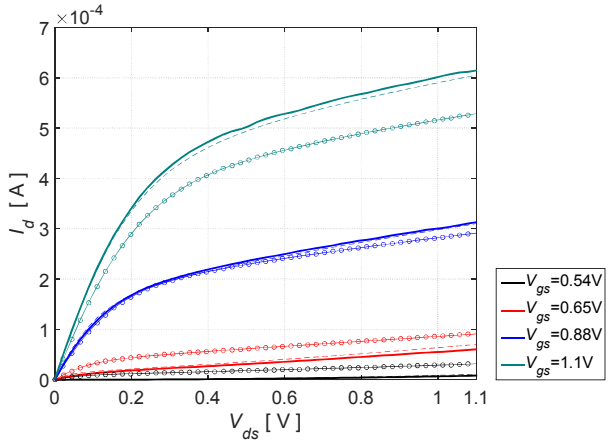


**Figure 6. I-V characteristics of a 1200 nm/40 nm NMOS in 40-nm CMOS: measurements at 300 K (dotted lines) and 4 K (solid lines); SPICE-compatible model (dashed lines).**

current when sweeping the drain-source voltage upwards or downwards.

Although the physics of cryo-CMOS is generally understood [30] and a few nanometer technologies have been cryogenically characterized (65 nm at 78 K [31], 32 nm at 6 K [32], 14 nm at 77 K [33]), there is not yet a general consensus on a standard cryogenic model for modern technologies, since prior models were limited to mature technologies (feature size ≥ 160 nm) and moderate cryogenic temperatures (>20 K) [34]-[38]. Characterization and modelling of nanometer CMOS technologies is specifically relevant for implementing low-power circuits for the platform in Figure 3, where handling of large-bandwidth high-frequency signals is required.

As a step in that direction, we have characterized a large number of active and passive components in standard 160-nm and 40-nm CMOS technologies [6][7][39]. As an illustration, Figure 5 and Figure 6 shows the output characteristics of NMOS transistors in both technologies. Despite a non-negligible shift of the transistor parameters, such as threshold voltage and current gain,

those characteristics are not dissimilar to the ones of a standard NMOS transistor, thus leading us to believe that standard SPICE models may be applicable also at cryogenic temperature. However, although it seems that a SPICE-compatible model for the DC behavior of cryo-CMOS devices may be feasible, much work must still be devoted to develop a full cryo-CMOS device model with the same reliability and accuracy of the models available for commercial technologies at room temperature, thus allowing the design of the complex RF, analog, mixed-signal and digital circuits of Figure 3.

The challenges to be addressed include the modelling and characterization of dynamic and RF behavior, of noise at low and high frequency, both for active devices and passives. Moreover, some preliminary investigations have suggested that transistor mismatch at 4 K is largely uncorrelated to that at 300 K and that standard design techniques to mitigate the effect of mismatch may need to be modified [40]. The large impact of mismatch on the performance and, hence, the design of analog and mixed-signal circuits asks for further investigations, and both additional experimental data and theoretical analysis will be required before the correct cryogenic mismatch model can be included in design tools. Finally, self-heating may give a non-negligible effect, since even a temperature raise of only a few degrees represents a relatively large increase in absolute temperature that can result in a large variation of the electrical properties of the devices. Because of this high sensitivity, it may be necessary to model the self-heating for each individual device. This would require strong efforts in properly updating the EDA tools, since self-heating of single devices or circuit sub-blocks can be highly dependent both on their physical placement on the die and their surroundings (including metal interconnections), not to mention the effect of thermal transients. At the moment, those issues are left largely unexplored for cryo-CMOS to the best of the author's knowledge.

# 5 DESIGN AUTOMATION FOR CRYOGENIC DESIGNS

Although the characteristic of CMOS transistors show a very wide alteration at cryogenic temperature, it has been shown that even complex commercial components not designed or specified outside the commercial temperature range, such as FPGAs, can reliably operate at cryogenic temperature [41]-[43]. Extensive characterization showed not only that all major components of a standard Xilinx Artix 7 FPGA, including look-up tables (LUT), phase-locked loops (PLL) and IOs, operate correctly down to 4 K but also that their logic speed is very stable over temperature [43]. An ADC based on a time-to-digital converter (TDC) has also been implemented in the same FPGA platform and its continuous operation from 300 K down to 15 K has been demonstrated, although specific care had to be taken in designing the firmware to minimize the temperature sensitivity, and calibration was extensively used to compensate for temperature effects [42].

Apart from showing the functionality of standard CMOS components at cryogenic temperature, FPGAs can also have a practical application for the implementation of the system in Figure 3, which at least in the first instance will not be necessarily limited to application-specific integrated circuits (ASIC). FPGAs could be beneficial thanks to their reconfigurability, which could prevent expensive and time-consuming cool-down-warm-up cycles. In addition, FPGA design tools leverage a mature synthesis and place-and-route technology, with advanced verification tools that could be used to emulate the operation of the circuit at cryogenic temperatures.

For the design and verification of the cryogenic FPGA, standard tools for firmware design were employed. The characterization of a standard FPGA library was an important step in creating the firmware, thus enabling correct operation at deep-cryogenic temperature. Similar efforts are needed in ASIC digital libraries, where transistor models are part of this characterization and could enable fast library certification. Ultimately, logic gate farms will be required to verify simulations and to validate the proposed models. In this context, the process of digital library characterization is not unlike a conventional one, with the difference that it requires care in measuring the circuits at various temperatures with a well-controlled measurement setup and particular attention to self-heating. The library characterization will also yield non-functional library elements, depending on temperature, thus requiring that synthesis and place-and-route tools be temperature-driven and/or temperature-aware.

A less trivial task would be the design of digital circuits that exploit the specific features of cryo-CMOS. The main challenge of operating large CMOS circuits and systems at cryogenic temperatures is power dissipation. In order to minimize power dissipation, the supply voltage could be reduced even down to a few tens of millivolt by exploiting the relaxed requirement on noise margins due to the low thermal-noise level at cryogenic temperature. Operation in sub-threshold regime can also be heavily exploited thanks to the improved subthreshold slope at low temperature and to the resulting large on/off-current ratio ($I_{on}/I_{off}$) ratio. Furthermore, the expected extremely low leakage current in cryo-CMOS may lead to power-efficient use of existing dynamic logic, or even bring in the possibility of new dynamic logic families. This can pose problems in the synthesis and verification of logic circuits, prompting the EDA industry to rethink models and perhaps even simulators, so as to achieve the necessary accuracy in the simulation of these regimes.

Finally, the operating temperature can be exploited as a new design parameter. Since the cooling power in a cryogenic refrigerator is larger at higher temperature, higher computational power could be placed at a higher temperature. However, particular care should then be devoted to the interconnections that, apart from becoming unpractical, could also occupy a relevant fraction of the cooling power budget due to their thermal conduction. The full digital back-end of a quantum computer would then spread over several temperature stages, eventually with a lower inter-stage data communication rate for circuits at lower temperatures. Although conceptually interesting, such approach would require an ad-hoc EDA infrastructure covering several multidisciplinary domains, including device modelling and library characterization over a very wide temperature range,

thermal modelling, interconnect optimization and novel synthesis tools.

# 6 CONCLUSIONS

The design of cryo-CMOS controllers for quantum computers presents several challenges for the design automation industry. First steps have already been taken, especially for device modelling and simulation/optimization of the quantum/classical interface. However, we are still far from the EDA infrastructure that will enable the design of the classical controller satisfying both the demanding electrical specifications and its very tight power budget. With the growing academic and industrial interest in the field of quantum computation, we foresee that several of the presented challenges will be soon picked up by the research community. This would result in an accelerating virtuous cycle including the design of cryo-CMOS circuits and systems with ever increasing complexity on one hand and more performant EDA tools on the other hand, thus facilitating the fabrication of practical quantum computers.

# ACKNOWLEDGMENTS

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