Deep-Cryogenic Voltage References in 40-nm CMOS

Harald Homulle, Fabio Sebastiano, and Edoardo Charbon

***Abstract*—The increasing interest in electronics specifically designed to control quantum processors is currently driven by the quest for large-scale quantum computing. A promising approach is emerging based on the use of CMOS devices operating at deep-cryogenic temperatures, and several essential components have been demonstrated to operate at such temperatures, from basic MOSFETs to field-programmable gate arrays. In this letter, we show, for the first time, a voltage reference in a standard CMOS technology that can guarantee a stable voltage over a wide range of temperatures from 300 K down to deep-cryogenic temperatures. By exploiting CMOS transistors in dynamic-threshold MOS configuration, the proposed reference occupies only 445 μm^2 in a standard 40-nm CMOS process, while showing a temperature coefficient below 0.8 mV/K over the temperature range from 4 to 300 K. These results demonstrate the feasibility of wide-range cryogenic voltage references to enable future cryogenic applications.**

***Index Terms*—Bandgap, cryogenic, MOS, voltage reference.**

I. Introduction

Quantum computers promise an exponential speed-up over classical computers, thanks to the exploitation of fundamental properties of quantum systems, such as superposition and entanglement [1]. They require large-scale control electronics to properly operate, but, since the quantum processor typically operates at deep-cryogenic temperatures, several researchers have proposed to operate this electronic control interface also at cryogenic temperatures [2]–[4]. CMOS technology offers several advantages over other viable electronic technologies for the implementation of this interface, such as the integration of billions of transistors on a single chip, low power, and sub-Kelvin functionality [5], [6]. In addition, MOS transistors operating at cryogenic temperatures exhibit a higher mobility, a steeper subthreshold slope, but also a higher threshold voltage [6], [7].

CMOS systems, especially analog circuits, often require an accurate reference voltage, which must be preferably integrated on chip. Traditionally, bandgap references in CMOS technology have employed parasitic bipolar transistors, since they are preferred for their lower process spread [8]. However, silicon bipolar transistors are not well behaved below roughly 90 K, since a significant decrease in current gain and increase in base resistance limit the operation of these devices at lower temperatures [9], [10]. Commercial bandgap references were found to be unstable at 130 K and below [11], and only bandgap references relying on alternative technologies, such as SiGe BiCMOS, have been demonstrated to work at 4 K, and even down to 700 mK [12].

As an alternative to bipolar-based topologies, a reference-based only on MOS transistors is very attractive, since the feasibility of MOS-based references operating down to 4 K has been demonstrated [10]. However, prior fully-MOS reference circuits operated only above 77 K [13], [14].

In this letter, we extend the operating temperature range of voltage references well beyond the state-of-the-art, by demonstrating the first cryogenic CMOS voltage reference operating down to 4 K. First, by adopting the approach proposed in [10] for a 0.16-μm CMOS process, we analyze the behavior of the core devices implemented in a standard 40-nm CMOS technology, and identify the optimal biasing conditions to create a stable reference voltage in Section II. To validate these findings, a complete reference circuit, including the core devices and biasing electronics, has been designed and characterized down to 4 K (Section III), unlike our prior work [10] focusing only on the core devices and not demonstrating a full circuit. Conclusions are drawn in Section IV.

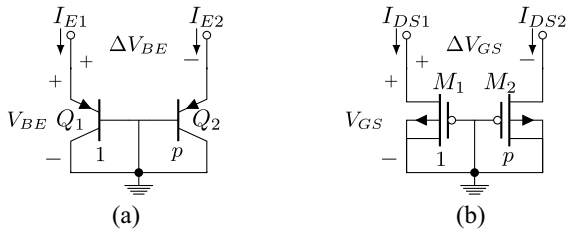

Fig. 1. Schematic of the bandgap core devices placed in a 1:p ratio, employing either (a) BJTs or (b) DTMOS. The devices are biased with equal currents, i.e., $I_{\mathrm{E1}} = I_{\mathrm{E2}} \equiv I_{\mathrm{DS1}} = I_{\mathrm{DS2}}$.

II. Bandgap Cores

A typical bandgap circuit exploits the exponential current–voltage relation of diode-connected devices, such as bipolar transistors [Fig. 1(a)], which can be expressed as

$$I = I_s\left(\mathrm{e}^{\frac{Vq}{nkT}} - 1\right) \tag{1}$$

where I and V are the device current and voltage drop, respectively, k is the Boltzmann constant, q the electron charge, T the absolute temperature and, for a BJT, I_s is the saturation current, $I = I_C$, $V = V_{\mathrm{BE}}$, and $n = n_{\mathrm{BJT}}$ is the effective emission coefficient. Since the voltage drop on such device is approximately complementary-to-absolute-temperature (CTAT), a reference voltage can be obtained by combining it with a proportional-to-absolute-temperature (PTAT) voltage that can be generated as the voltage difference between two diode-connected devices biased at different current densities

$$\Delta V = n\frac{kT}{q}\ln(p) \tag{2}$$

where, for BJTs, $\Delta V = \Delta V_{\mathrm{BE}}$, $n = n_{\mathrm{BJT}}$, and p is the emitter-area ratio of the two diodes in Fig. 1(a), biased with the same current. The reference voltage is then constructed as

$$V_{\mathrm{REF}} = V + \alpha\Delta V \tag{3}$$

where α is a constant chosen to ensure a minimum temperature coefficient for V_{REF}.

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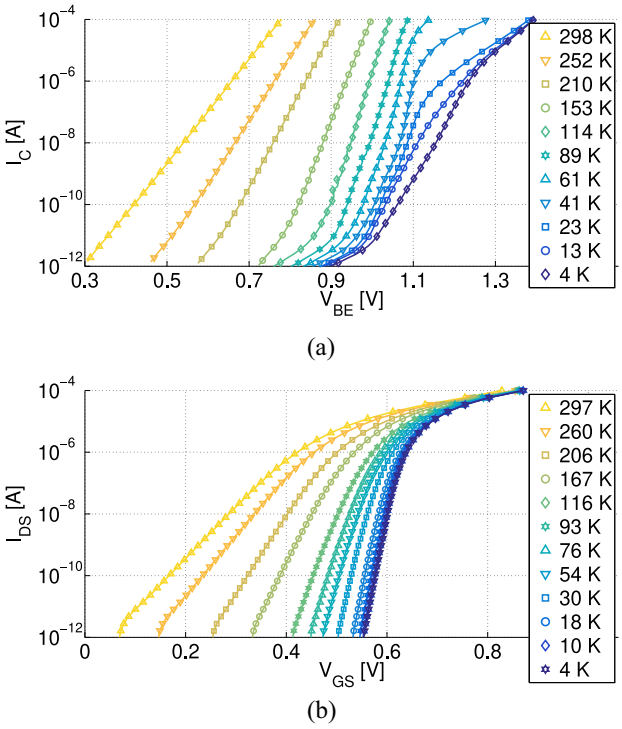

Fig. 2. (a) I_C–V_{BE} for a BJT with 5×5 μm^2 emitter area. (b) I_{DS}–V_{GS} for a DTMOS with W / L = 4 μm / 0.5 μm.

MOS in dynamic-threshold MOS (DTMOS) configuration [Fig. 1(b)], i.e., MOS with short-circuited gate and body terminals, can replace BJTs in bandgap cores, and are preferred over conventional MOS for their lower spread, better matching, steeper subthreshold slope, and operation at lower supply voltage [10]. For DTMOS in weak inversion, (1)–(3) hold with $I = I_{DS}$, $V = V_{GS}$, p being the ratio between the aspect ratio of the two diodes and $n = n_{MOS}$ being the nonideality factor.

We implemented all structures, including the pairs shown in Fig. 1 and the circuits discussed in Section III, in a 1P6M TSMC 40-nm process. After bonding on a PCB, the devices were tested in a dip-stick immersed in liquid helium or helium vapors over the temperature range from 4 to 300 K. A reference temperature diode (LakeShore DT-670) was mounted in close proximity to the sample for accurate temperature measurements, and the electrical characterization was performed using Keithley 2636B sourcemeter units.

The BJTs are composed of unit elements with a 5×5 μm^2 emitter area (comparable to those used in state-of-the-art temperature sensors and bandgap references), and $p = 12$. For the DTMOSs, thick-oxide transistors were used with a W / L = 4 μm / 0.5 μm as unit element (since larger transistors were shown to have a lower current dependency on ΔV_{GS} [10]), and $p = 36$.

For the bipolar device, I_C [Fig. 2(a)] follows the expected exponential relation [following (1)] over a wide range of currents, but only above roughly 100 K, as expected due to increasing base resistance and reduced current gain at lower temperatures [10]. On the contrary, the I_{DS} [Fig. 2(b)] in the DTMOS follows an exponential relation over the complete range down to 4 K, but only up to 1 μA, since it enters moderate inversion at higher current levels. Although following an exponential trend, the V–ln(I) slope of both devices deviates from an ideal diode behavior, as indicated by n_{BJT} and n_{MOS} deviating from unity and being temperature dependent (Fig. 3), especially for lower temperatures.

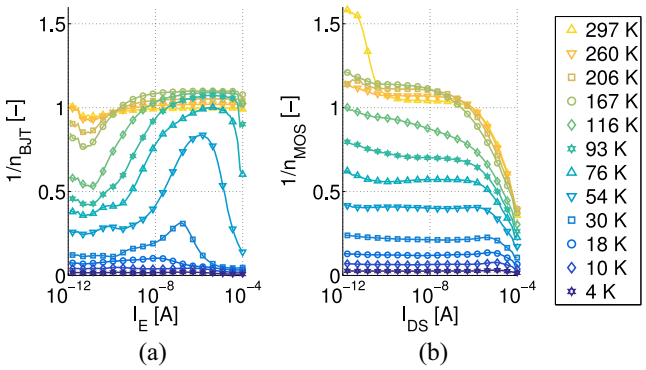

Fig. 3. Emission coefficient and nonideality factor represented as (a) $1/n_{BJT}$ and (b) $1/n_{MOS}$ versus biasing current.

When biasing the BJTs with a constant current, V_{BE} is approximately CTAT down to 100 K over a wide range of currents (10 pA–100 μA), as shown in Fig. 4(a). Below this temperature, both V_{BE} and ΔV_{BE} [Fig. 4(b)] show an abrupt change in temperature coefficient. The BJT bandgap voltage V_{REF} is composed according to (3) by numerically combining V_{BE} and ΔV_{BE} with the optimal α, achieving the lowest variation over the 100–300 K temperature range [Fig. 4(c)]. The reference voltage is close to the theoretical silicon bandgap of 1.22 V and exhibits a low temperature coefficient above 100 K (± 40 ppm/K), but is unsuitable for cryogenic applications.

Using the same approach as for the BJTs, the V_{REF} for the DTMOS has been generated in Fig. 5. With respect to the BJT's case, the reference voltage shows a better stability down to 4 K, but a much larger temperature coefficient (up to ± 830 ppm/K on the 4–300 K range). This is due to the drastic increase of n_{MOS} and the consequent flattening of ΔV_{GS} at lower temperatures. However, the analysis shows that a much flatter reference is obtained when biasing the transistors in strong inversion, i.e., for currents above approximately 1 μA. In this case, the generated reference voltage depends also on the threshold voltage of the devices. The combination of the temperature dependence of several parameters, including the hole mobility and the threshold voltage, cancel out to first order, as in typical MOS-based references, thus achieving a temperature coefficient as low as ± 20 ppm/K (Fig. 5). Contrary to intuition, this points to strong inversion references as better candidates for cryogenic operation.

In this analysis, we assumed the current to be constant over temperature. Since in a practical circuit the current is typically PTAT and the temperature coefficients of integrated resistors may be relevant, full voltage references with BJTs and with DTMOS in strong inversion have been implemented and experimentally characterized, as shown in the next section.

III. Voltage-Reference Circuits

The complete bandgap circuits are shown in Fig. 6, and the chip micrograph with superimposed layouts is shown in Fig. 7. The simplest topology for a bandgap reference has been adopted so as to minimize the circuit complexity and prevent unexpected behavior at cryogenic temperatures. A current–voltage mirror using nMOS ($M_{4,5}$) and pMOS ($M_{6,7}$), all thick-oxide with a W / L ratio of 3 / 0.4 μm and 2 / 0.4 μm, respectively, sets the voltage across R_1 to ΔV, so that the same current $\Delta V / R_1$ flows through the two core devices ($M_{1,2}$ or $Q_{1,2}$). A third branch (M_8, R_2, M_3, or Q_3) is used to sum V and ΔV using $\alpha = (R_2/R_1)$. The resistor values have been chosen large enough for a low power consumption and small enough to ensure a bias current much larger than the sources of inaccuracy, such as noise and leakage currents. We employed polysilicon

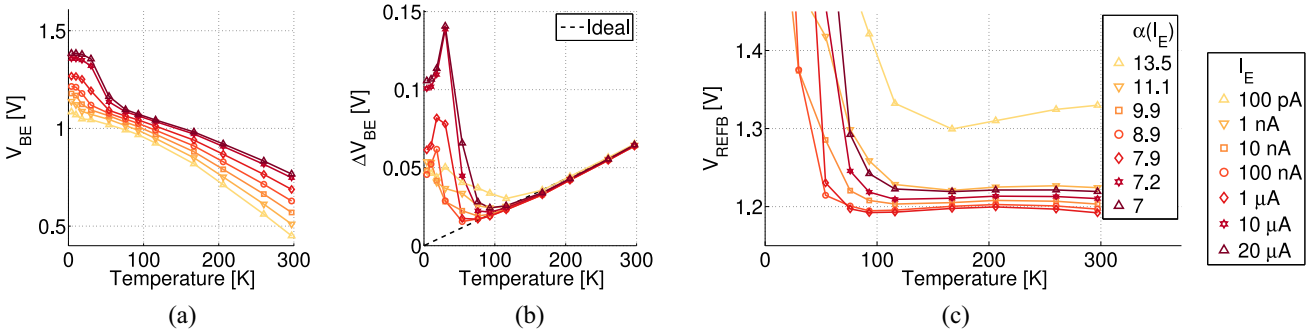

Fig. 4. Generating a reference voltage with BJTs: combining the (a) CTAT component V_{BE} with (b) PTAT component ΔV_{BE} following (3) with the (c) optimal α per each bias current to minimize the variations over the temperature range from 100 to 300 K.

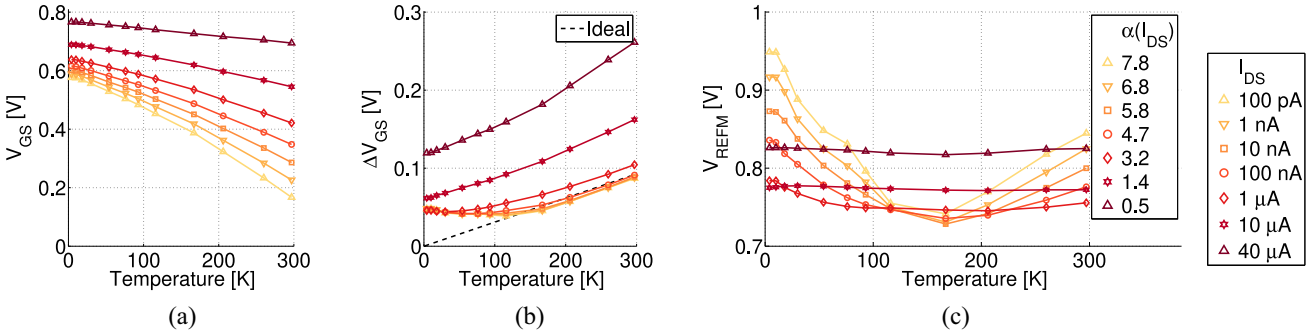

Fig. 5. Generating a reference voltage with DTMOS: combining the (a) CTAT component V_{GS} with (b) PTAT component ΔV_{GS} following (3) with the (c) optimal α per each bias current to minimize the variations over the temperature range from 4 to 300 K.

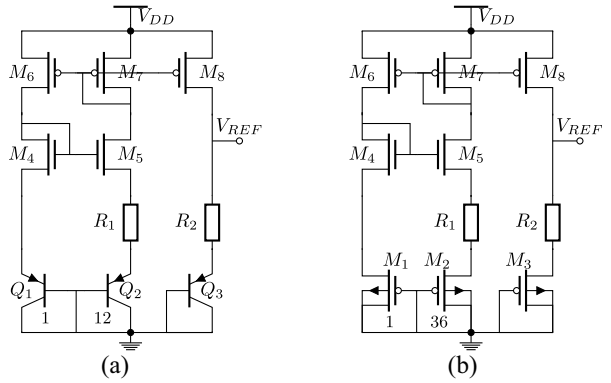

Fig. 6. Schematic of the cryogenic bandgap voltage reference employing either (a) BJTs or (b) DTMOS.

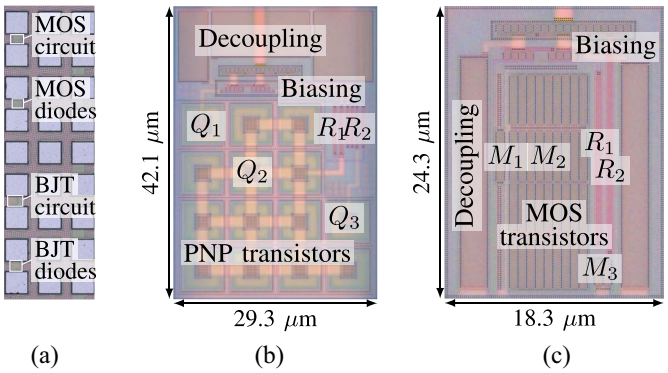

Fig. 7. (a) Chip micrograph of all devices. (b) and (c) Zoomed-in view with superimposed layout of the voltage references employing either (b) BJTs or (c) DTMOS (including decoupling capacitors).

resistors, since they show the least spread over temperature; we measured less than 10% resistance variation from 300 to 4 K for an n-poly resistor in the adopted 40-nm process with a nominal value of 4.5 kΩ at 300 K. Although this variation will affect the biasing current, and hence V_{REF}, this effect is negligible with respect to the steep variation in slope for the core devices at lower temperatures.

For the BJT-based implementation, $R_1 = 3$ kΩ and $R_2 = 7.6$ kΩ, resulting in an $\alpha = 2.53$. Since $\Delta V_{BE} = n_{BJT} kT/q \ln(p) \approx 64$ mV at 300 K, the current in each branch is roughly 21 μA, reducing to 7 μA at 100 K. The measured reference voltage is relatively flat above 100 K as shown in Fig. 8(a). Since cryogenic device models were not available at design time, the chosen α is lower than the optimal $\alpha \approx 7$ from Fig. 4(c), thus leading to a negative temperature coefficient above 100 K. Behavior over several devices is presented in Fig. 8(c) and (d). The measured power-supply rejection ratio (PSRR, Fig. 9) is 26 dB at 300 K, and reduces to 22 dB at 100 K.

In the DTMOS case, $R_1 = 6.6$ kΩ, $R_2 = 8$ kΩ, and thus $\alpha = 1.2$. By comparing V_{REF} in Fig. 4(c) with the measurements, we estimate $I_{DS} \approx 40$ μA and $\Delta V_{GS} \approx 260$ mV at 300 K, and $I_{DS} \approx 13$ μA and $\Delta V_{GS} \approx 86$ mV at 4 K. This circuit [Fig. 8(b)] properly operates down to 4 K, albeit V_{REF} still drops by 200 mV from 300 to 4 K due to α being larger than the optimum value. However, V_{REF} changes by only 10 mV (for a 3 V supply) at cryogenic temperatures between 4 and 100 K, with the temperature coefficient improving from 1.6 mV/K at 300 K to 0.1 mV/K at 4 K. This behavior is fairly flat over several devices [Fig. 8(c) and (d)]; the spread in V_{REF} improves from 32 mV (1σ) at 300 K to 22 mV (1σ) at 4 K. The PSRR (Fig. 9) is 23 dB and fairly stable over temperature. These results have been achieved thanks to core devices operating in strong inversion, while operation in weak inversion would have suffered

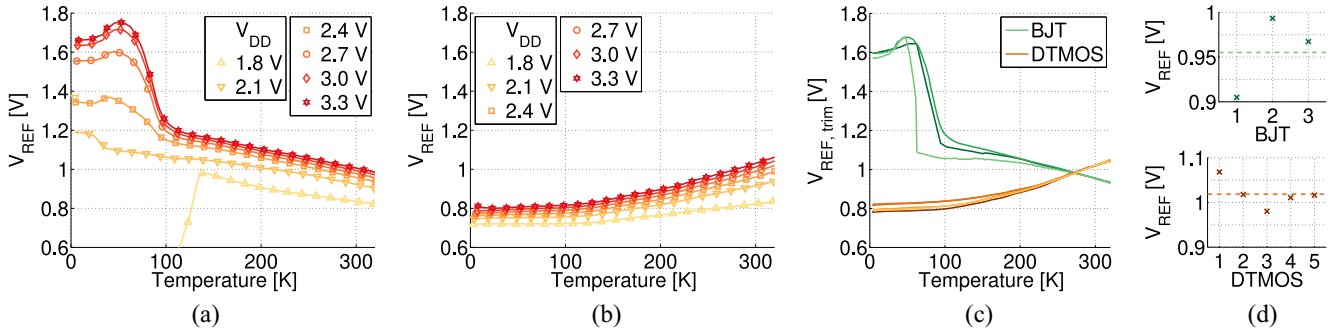

Fig. 8. Measured reference voltage V_{REF} versus temperature for the (a) BJT and (b) DTMOS implementations. (c) V_{REF} over temperature for several devices trimmed in post-processing by subtracting the offset to the average reference voltage at 300 K, i.e., the dashed lines in (d) ($V_{\mathrm{DD}} = 3$ V). (d) Untrimmed V_{REF} at 300 K ($V_{\mathrm{DD}} = 3$ V).

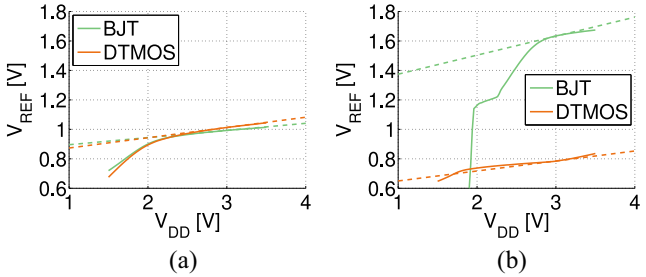

Fig. 9. Measured reference voltage V_{REF} versus supply voltage V_{DD} for both implementations at (a) 300 K and (b) 4 K. The dashed lines indicate the slope at the optimal supply voltage of 3 V.

TABLE I
SUMMARY OF THE MEASURED PERFORMANCE AT 300, 100, AND 4 K FOR BOTH VOLTAGE REFERENCES AT $V_{\mathrm{DD}} = 3$ V

		BJT			MOS		
Temperature		4 K	100 K	300 K	4 K	100 K	300 K
V_{REF} (avg.)	[V]	-	1.18	0.96	0.81	0.82	1.02
V_{REF} (1σ)	[mV]	-	97	45	22	21	32
$V_{REF,\mathrm{trim}}$ (1σ)	[mV]	-	68	0	17	18	0
P_{DD}	[μW]	-	47	189	132	153	368
$\Delta V/\Delta T$ (avg.)	[mV/K]	-	-5.5	-1.1	0.1	0.3	1.5
PSRR	[dB]	-	21.9	26.2	23.4	27.8	23.1
T range	[K]	100–320			4–320		
$\Delta V/\Delta T^{*}$	[mV/K]	-1.15			0.85		

* $\Delta V/\Delta T$ is computed using the box method over the entire temperature range and over all samples.

from the roll-off in ΔV_{GS} shown in Fig. 5(b). The performance is summarized in Table I.

IV. CONCLUSION

In this letter, we advocate the use of DTMOS for the implementation of voltage references optimized for deep-cryogenic temperatures. We showed, to the best of our knowledge, the first standard CMOS deep-cryogenic voltage reference circuit operating down to 4 K. The reference voltage varies by only 1.2% from 4 to 100 K, and achieves a temperature coefficient below 0.1%/K over the whole range from 4 to 300 K. This shows the feasibility of voltage reference circuits in standard CMOS operating more than 200 K below the standard temperature range, thus enabling cryogenic electronics for space, quantum, and high-energy physics applications.

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