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A fast and accurate delay dependent method for switching estimation of large combinational circuits

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Abstract

Assuming inertial gate delay model, the first-order temporal correlation and the structural dependencies, a probabilistic method to estimate the switching activity of a combinational circuit, is introduced. To capture the first temporal correlation a novel mathematical model and the associated new formulas are derived. Also, a modified boolean function, which describes the logic and timing behavior of each signal, is introduced. To capture the structural dependencies an efficient new method to partition a large circuit into small independent sub-circuits is proposed. Finally, an algorithm that evaluates the switching activity of any circuit node is presented.

Keywords: Gate level; Power estimation; CMOS circuit; Low power design; Computer aided design

1. Introduction

The rapid development of competitive market sectors such as wireless applications, laptops and portable medical devices, makes the power dissipation the most important parameter in the modern VLSI design. Time-to-market requirements can be achieved by the use of efficient low power design techniques and power estimation methodologies, which have been developed to solve certain design issues of all design levels [1]. The largest portion of the consumed power of a digital circuit is the dynamic power dissipation arising from the charging and discharging of the circuit nodes. Therefore, the average power dissipation of a circuit can be estimated by evaluating the average number of the transitions of the circuit nodes.

In recent years, a variety of probabilistic methods have been developed to estimate the average switching activity of the combinational circuits [2–10]. In these methods, the probabilistic properties, such as the steady state probability and the average transition probability of the input signals, were used. According to assumed gate delay model, the above methods can be classified as: (i) zero gate delay methods [3–7], where only the functional transitions are considered and (ii) non-zero gate delay methods [8–10], where both the functional and spurious transitions are taken into account.

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Accurate power estimation requires both the temporal correlation and the spatial or the structural dependencies. By temporal correlation we imply the dependency between the current signal value and its previous values, while the structural correlation is due to the reconvergent fanout regions.

In [8], the concept of the probability waveforms to estimate the average power dissipation of a combinational circuit was introduced. Given the probability waveforms of the primary inputs, an algorithm to propagate the transition waveforms through the circuit levels was developed. However, both the structural and input dependencies were not taken into consideration. Additionally, the efficiency of the algorithm for large circuits is not proved by the presented experimental results.

In [9], a symbolic simulation algorithm has been proposed. Given the switching activities of the primary inputs and using global ordered binary decisions diagrams (OBDDs) [13], where each node is expressed by the primary input signals, the transition probability of a node at time t is evaluated by calculating the probability of a novel boolean function. The new boolean function is derived by XORing the boolean functions, which correspond to the two successive switching time instances, i.e. t and $t+1$. Although the structural and the first-order temporal correlations were handled by this method, it was inefficient for large circuits since the global OBDDs require huge memory size.

A new method for calculating the transition probabilities has been presented in [10]. Based on the signal probability evaluation method of [15] and using symbolic simulation, the transition probability of the circuit was evaluated considering the first-order temporal correlation and structural dependencies. Particularly, using the first-order transition probabilities to evaluate the transition activity of the circuit nodes, the temporal correlation was captured. Also, expressing the signals in a symbolic form in terms of structural independent signals, the dependencies in the reconvergent regions were captured. To reduce the size and the complexity of the symbolic form of large reconvergent regions, the method was parameterised in terms of the depth of the considered circuit levels. By this way the propagation and the efficiently manipulation of the symbolic forms was taken place. On the other hand, an inaccuracy was occurred, since a node may be expressed symbolically in terms of not independent signals due to the circuit level depth parameter.

A method, based on the Markov chain theory and the notion of correlation coefficient, TC [6], that takes into account both spatial/temporal correlations and real-delay information, was presented in [12].

In this paper, considering inertial gate delay model, a novel probabilistic method to estimate the average switching activity of large combinational circuits is introduced. The first-order temporal correlation, the structural dependencies as well as the multiple-input transitions are taken into account, while the primary input signals are assumed mutually independent. Considering the influence of time in glitch generation, the switching activity computation problem under inertial delay model is reduced to a series of switching activity computations at specific time instances. To capture the first-order temporal correlation a novel mathematical model and new formulas are provided.

Since we are dealing with non-zero gate delay model, the time parameter influences the logic behavior of a circuit node and must be considered. To describe the logic behavior of a circuit node in terms of time, a modified Boolean function called *Real Delay Boolean Function* (RDBF) is introduced. Additionally, a new heuristic, which has twofold goal is proposed: (i) the circuit partitioning to handle large combinational circuits efficiently (ii) the calculation of the switching activity of any circuit node at any time instance. The proposed method is compared in terms of accuracy with a switch level simulator and in terms of efficiency to handle large combinational circuits with the method reported in [10]. Employing a set of benchmark circuits, the comparison results prove the efficiency of the proposed method.

The rest of the paper is organized as follows: In Section 2 the logic level power estimation problem is formulated, while its mathematical model is presented in Section 3. The switching activity

evaluation is described in Section 4, while the experimental results are presented and discussed in Section 5. Finally, the conclusions and future work are discussed in Section 6.

2. Problem formulation

It is assumed that a combinational circuit is a part of a synchronous sequential circuit, which implies that its inputs can switch synchronously with the clock, performing at most one transition at time $t = 0$ during the clock period $[0, T)$. Moreover, an applied input signal is considered as ideal step pulse, while all transitions are considered as full transitions. An inertial gate delay model is assumed, which means that any pulse whose the width is smaller than the gate delay, is filtered and does not appear in the gate output.

The power estimation problem of a combinational logic circuit can be formulated as follows: "*Given the gate level description of a combinational circuit with n inputs and m outputs and the inertial delays of its gates, and, assuming that the period of the applied input vectors is greater or equal to the settling time of the circuit, estimate the average power consumption of the circuit for an input vector stream through the calculation of its average switching activity*".

A glitch is generated at the output of a gate, if the following conditions are met: (i) the *necessary condition*, which requires the difference of the arrival times of the input signals to be greater than the inertial delay of the gate and (ii) the *sufficient condition*, which requires the appropriate transitions of the input signal(s) to switch the gate output.

Consequently, the time parameter plays a critical role in the power consumption estimation. Hence, the exact description of a logic circuit should include not only its logic behavior, but also the time dependency among the logic signals. Furthermore, since the glitch generation is strongly dependent on time, a modified Boolean function, which describes the logic and timing behavior of each signal, is needed. We call this modified Boolean function as *real delay Boolean function* (*RDBF*).

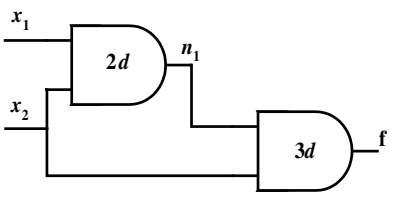

Fig. 1. The logic circuit with Unit Delay AND gates.

Example. We assume the logic circuit of Fig. 1, where the gate delays are multiples of a reference delay unit d.

The logic behavior of the node f can be described in time domain by the following RDBF:

$$f = F(x_1, x_2, t) = x_1(t - 5d)x_2(t - 5d)x_2(t - 3d) \quad (1)$$

The signal f may switch at two time instances, i.e. $t_1^f = 3d$ and $t_2^f = 5d$. More specifically, the transition of the signal f at t_1, $t_1^f = 3d$, depends on the transitions of the primary inputs x_1 and x_2 at time points $t_1^{x_1} = -2d$, $t_1^{x_2} = -2d$, and $t_1^{x_2} = 0$. The corresponding Boolean function is $f_1 = x_1(-2d)x_2 \times (-2d)x_2(0)$. The transition of f at $t_2^f = 5d$ depends on the transitions of the signals x_1 and x_2 at $t_2^{x_1} = 0$, $t_2^{x_2} = 0$, and $t_2^{x_2} = 2d$, while the corresponding Boolean function is $f_2 = x_1(0)x_2(0)x_2(2d)$. Thus, the behavior of the signal f is described in time domain by the corresponding RDBF. Moreover, the RBDF of f is reduced to ordinary Boolean functions f_1 and f_2, whose variables are the logic values of the input signals at specific time instances. Also, since node f may perform transitions at $t_1^f = 3d$ and $t_2^f = 5d$, evaluating the transition activity of the functions f_1, f_2 the transition activity of the RBDF is also evaluated.

Having the above example and Eq. (1) as starting point, a novel mathematical model, which describes the behavior of a logic signal in terms of time, should be introduced. We aim at the development of a new method, which transforms the switching activity estimation problem, considering inertial delay model, to a series of switching activity calculations at certain switching time points. For that purpose, we introduce new concepts and formulas to capture the first order temporal correlation.

3. Mathematical model

The behaviour of a binary signal, x, at a time point, t, i.e. $x(t)$, can be modelled as a random variable of a time homogeneous, strict sense stationary (SSS), lag-one Markov stochastic process having two states, s, with $s \in S = \{0, 1\}$. Also, it is assumed that the Markov process is finite, aperiodic, and irreducible with all states recurrent non-null [16].

The *transition probability*, $p^x_{kl}(t)$, expresses the probability of a signal x to perform a transition from the state k to the state l within two successive transition time points t' and t. That is:

$$p^x_{kl}(t) = p(x(t') = k \wedge x(t) = l) \quad \forall k, l \in S \tag{2}$$

The *switching activity*, $E^x(t)$, of a signal x at time instance t is given by:

$$E^x(t) = p^x_{01}(t) + p^x_{10}(t) \tag{3}$$

where $p^x_{01}(t)$ (or $p^x_{10}(t)$) is the transition probability of the signal x to perform the transition from state 0 to 1 (or 1 to 0) at time instance t.

Definition 1. A *signal transition probability vector*, $\boldsymbol{P}^x(t)$, of a signal x at a time instance t, is defined as the vector of all transition probabilities $p^x_{kl}(t)$, with $k, l \in S$:

$$\boldsymbol{P}^x(t) = [p^x_{00}(t), p^x_{01}(t), p^x_{10}(t), p^x_{11}(t)] \tag{4}$$

Definition 2. We define as *valid time points set*, $\boldsymbol{T}^x = \{t^x_1, \ldots, t^x_r\}$, the transition time points for a signal, x, i.e. the time points that a transition of signal x may occur.

For a primary input signal x holds that $\boldsymbol{T}^x = \{0\}$. The switching activity estimation problem is reduced to the estimation of $\boldsymbol{P}^x(t^x_i)\ \forall t^x_i \in T^x$. For example, the signal f shown in Fig. 1 has as *valid time points set* $\boldsymbol{T}^f = \{3, 5\}$.

We introduce the transition probability of a signal x in the time intervals (t^x_{i-1}, t^x_i) and (t^x_i, t^x_{i+1}) as $\boldsymbol{P}^x(t^{x^-}_i)$ and $\boldsymbol{P}^x(t^{x^+}_i)$, respectively. The transition probability of a signal, x, at a time point $t' \in \{t^{x^-}_i, t^{x^+}_i\}$ is expressed in terms of the transition probability at time point t^x_i, $\boldsymbol{P}^x(t') = f(\boldsymbol{P}^x(t^x_i))$, and are computed by the following formulas:

$$p^x_{kk}(t^{x^-}_i) = p^x_{kk}(t^x_i) + p^x_{k\bar{k}}(t^x_i) \quad \forall k \in S \tag{5}$$

$$p^x_{ll}(t^{x^+}_i) = p^x_{ll}(t^x_i) + p^x_{l\bar{l}}(t^x_i) \quad \forall l \in S \tag{6}$$

$$p^x_{kl}(t^{x^-}_i) = p^x_{kl}(t^{x^+}_i) = 0 \quad \forall k, l \in S \wedge k \neq l \tag{7}$$

4. Switching activity computation

Generally, a signal x of the logic circuit is a RDBF of a subset of v signals, i.e. $x(t) = f(x_1(t), \ldots, x_v(t))$. The v variables that the signal x depends on, at any time point t, are called the *support set* of signal x. For any RDBF, we can efficiently construct the corresponding OBDD using the BDD package [14]. Manipulating these OBDDs, the switching activity at the corresponding time instances can be evaluated.

To capture the structural dependencies, the support set of each internal node should consist of independent signals. It can be achieved by expressing every node in terms of primary inputs. However, the size of the support sets is increased, as we are moving to the primary inputs (i.e. depth levels of the circuit). Hence, the size of the OBDDs is also increased resulting in a large amount of occupied memory. Moreover, the computational complexity to manipulate the OBDDs is also increased. Thus, an efficient heuristic is required to reduce the size of the support sets by partitioning the circuit in independent subcircuits.

4.1. Circuit partitioning

In Fig. 2, a partitioning example is given. The support set of node y_1 can be easily found, because there is no reconvergent region. The support set of this node is: $\mathrm{Sup}(y_1) = \{x_1, x_2, x_3\}$ with three variables. For node y, there are three equivalent support sets: $\mathrm{Sup}_1(y) = \{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$ with seven variables, $\mathrm{Sup}_2(y) = \{y_1, x_4, x_5, x_6, x_7\}$ with five variables and $\mathrm{Sup}_3(y) = \{y_1, x_4, w, x_7\}$ with four variables. In order to reduce the complexity of the

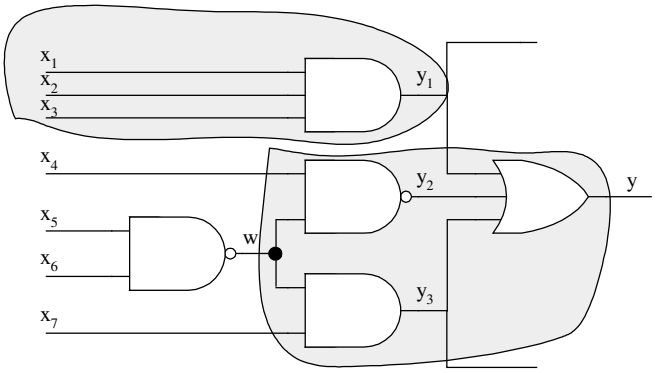

Fig. 2. A partitioning example.

constructed OBDD, we have to use the support set with the minimum number of variables.

To determine the support sets of all circuit nodes, a limited reconvergent path analysis is performed. This analysis results into a *new* heuristic, which is based on the limited depth structural correlation. More specifically, the notion of *active nodes* presented in [10] is used in order to perform an initial partitioning for any circuit signal according to a user-specified parameter, called *Depth*. This parameter specifies the number of circuit levels that are considered at the reconvergent analysis for each circuit node. If two or more paths start at a node, x, and reconverge in a node y within *Depth* circuit levels, then the node x is included in the support set of y. If the paths reconverge after *Depth* circuit levels the signals that correspond to these paths are assumed independent. Thus the circuit is partitioned in structurally independent regions.

Moreover, another user-defined parameter, called *N_vars*, is used to reduce the number of variables, v, (i.e. $v \leqslant N\_vars$) of the RDBF of any circuit node. The proposed algorithm is a modification of the algorithm reported in [8]. More specifically, after the circuit partition based on the parameter *Depth*, if the number of variables, v, of circuit node x is $v > N\_vars$, a new local partition is performed for the signal x considering *Depth*-1 logic levels. This procedure is repeated until $v \leqslant N\_vars$. The proposed heuristic is described in pseudo-code form by the function *Find_Support_Set* is shown in Fig. 4.

After the circuit partitioning, using the previous described heuristic, the next step of the proposed method is the estimation of the switching activity at the specific time points. For that purpose, another heuristic algorithm is developed.

4.2. Switching activity evaluation

Using the previously described heuristic the circuit can be partitioned, an efficient algorithm to estimate the switching activity at the specific time points is needed. A circuit node, x, switches at time $t = t_i^x$, if the derivative with respect to time of its RDBF is equal to 1. Thus, the average switching activity, $E^x(t_i^x)$, in probabilistic domain can be described by:

$$E^x(t_i^x) = p\left(\frac{\partial x(t)}{\partial t}\Big|_{t=t_i^x} = 1\right) = p\left(\lim_{\varepsilon\to 0}\{x(t_i^x-\varepsilon)\oplus x(t_i^x+\varepsilon)\} = 1\right) \quad (8)$$

Instead of performing the XORing between the Boolean functions corresponding to the time intervals (t_{i-1}^x, t_i^x) and (t_i^x, t_{i+1}^x) we can manipulate efficiently the OBDD, which corresponds to each time point t_i, in order to evaluate the switching probability at this time point. Considering the representation of an ordinary boolean function by its corresponding OBDD, the evaluation of the transition $k \to l$ with $k, l \in \{0, 1\}$ at time instance t_i can be done by the following steps shown in Fig. 3:

i) Find the set of paths to state k, $\Pi_x^k(t = t_i^x)$, of the OBDD of the Boolean function corresponding to the timed Boolean function on time point t_i^x,

ii) Find the set of paths to state l, $\Pi_x^l(t = t_i^x)$, of the OBDD of the Boolean function corresponding to the timed Boolean function on time point t_i^x,

iii) Combine each path of $\Pi_x^k(t = t_i^x)$ with all paths of $\Pi_x^l(t = t_i^x)$ and extract the switching behaviour taking into account the temporal compatibility of each signal using the following equation:

$$p_{kl}^{x}\left(t_i^x\right) = \sum_{\pi \in \Pi_x^k} \sum_{\pi' \in \Pi_x^l} \prod_{j=1}^{v} p_{k_j l_j}^{x_j}\left(t_j^{x_j}\right) \tag{9}$$

Fig. 3. The heuristic algorithm for calculating the switching activity.

Example. To make clear the above procedure, we calculate the switching activity of signal f of Fig. 1. Assuming that we are interested for the switching transition $1 \to 0$ of signal f at $t_i^f = 5$, the associated RDBF becomes: $f(2) = x_1(0)x_2(0)x_2(0^+)$.

From the previously mentioned procedure (Fig. 3) for the switching activity computation, the corresponding sets of paths are:

$$\Pi_f^1(t_i^f = 2) = \{(x_1(0), x_2(0), x_2(0^+)) = (1,1,1)\}$$

$$\Pi_f^0(t_i^f = 2) = \left\{ \begin{array}{l} (x_1(0), x_2(0), x_2(0^+)) = (0,2,2) \\ (x_1(0), x_2(0), x_2(0^+)) = (1,0,2) \\ (x_1(0), x_2(0), x_2(0^+)) = (1,1,0) \end{array} \right\}$$

where the value 2 stands for the *don't care* logic value.

If we combine each path $\pi \in \Pi_f^1(t_i^f = 2)$ with each path $\pi' \in \Pi_f^0(t_i^f = 2)$, the $p_{10}^f(2)$ can be expressed as:

$$\begin{aligned} p_{10}^f(2) &= p_{10}^{x_1}(0)\, p_{12}^{x_2}(0)\, p_{12}^{x_2}(0^+) + p_{11}^{x_1}(0)\, p_{10}^{x_2}(0)\, p_{12}^{x_2}(0^+) + p_{11}^{x_1}(0)\, p_{11}^{x_2}(0)\, p_{10}^{x_2}(0^+) \\ &= p_{10}^{x_1}(0)\left(p_{10}^{x_2}(0) + p_{11}^{x_2}(0)\right)\left(p_{10}^{x_2}(0^+) + p_{11}^{x_2}(0^+)\right) + p_{11}^{x_1}(0)\, p_{10}^{x_2}(0)\left(p_{10}^{x_2}(0^+) + p_{11}^{x_2}(0^+)\right) \\ &\quad + p_{11}^{x_1}(0)\, p_{11}^{x_2}(0)\, p_{10}^{x_2}(0^+) = p_{10}^{x_1}(0)\, p_{11}^{x_2}(0) \end{aligned}$$

because $p_{10}^{x_2}(0^+) = 0$ and, $p_{11}^{x_2}(0^+)$ and $p_{10}^{x_2}(0)$ are temporal incompatible transitions.

The pseudo-code of the proposed switching activity estimation method is shown in Fig. 4.

The inputs of the proposed algorithm are: (i) the gate level description, *Network*, (ii) the input vector set, *Vector*, and (iii) the user-defined parameters *Depth* and *N_vars*. In the beginning, the logic gates of the combinatorial circuit are sorted according to their circuit level. A limited depth reconvergent analysis is performed to find out the active nodes. Afterwards, the possible transition time instances for every signal are determined; the transition time points of the input signals are derived by analysing the input vector stream, while the transition time instances of the internal nodes are extracted by traversing the circuit from the primary input to primary outputs, taking the gate delays into account. After that, the switching activity of each node is calculated. To find out independent sub-circuits, the proposed heuristic of Section 4.1 is taken place by applying the function *Find_Support_Set*, while the heuristic of the switching activity evaluation, which has been described in Section 4.2, is taken place by applying the function *Combine_Paths*.

```
Switching_Activity_Estimation (Network, Vector, Depth, N_vars){
    Gates = Topological_Sort ( Network ) ;
    -- (1) : Perform a limited depth reconrvergent analysis
    Find_Active_Nodes ( Gates , Depth ) ;
    -- (2) : Find out the valid time points of each circuit signal.
    For each primary input signal x_i {
        T^{x_i} = {0} ;
        P^{x_i}(0) = Analyze_Input_Vector ( Vector , i ) ;
    }
    for each gate g in Gates {
        Δ = delay of g ;
        T^g = {0} ;
        for each input g_i of g {
            for each time point k ∈ ∪T^{g_i} {
                T^g = T^g ∪ {k + Δ} if k + Δ satisfies the necessary condition ;
            }
        }
    }
    -- (3) : Calculate the switching activity of any circuit node at any valid time point.
    For each gate g in Gates {
        for each time point k of T^g {
            Sup(g(k)) = Find_Support_Set ( g , k , Depth , N_vars ) ;
            OBDD(g(k)) = Construct_OBDD ( Sup (g(k)) ) ;
            P^g(k) = Combine_Paths( OBDD(g(k)) ) ;
        }
    }
}
    -- (4) : Circuit partitioning.
Find_Support_Set ( g , k , Depth , N_vars ) {
    Sup(g(k)) = Construct_Support_Set ( g, k , g.active_nodes ) ;
    Depth' = Depth ;
    While | Sup(g(k)) | > N_vars {
        Depth' = Depth' – 1 ;
        Find_Active_Nodes ( g , Depth' ) ;
        Sup(g(k)) = Construct_Support_Set ( g , k, g.active_nodes' ) ;
    }
return(Sup(g(k)) ;
}
```

Fig. 4. Pseudo-code of the proposed method.

5. Experimental results

The proposed power estimation method is implemented by ANSI C language, while its efficiency is proved by a number of ISCAS'91 benchmark multilevel circuits. For technology mapping, a library of primitive gates (i.e. NOT, BUFF, AND, NAND, OR, NOR, XOR, XNOR) of up to four primary inputs is used. All power estimations are measured in μW with 20 MHz clock frequency and 5 V power supply. For a circuit node n_i (either primary input or internal node), we define as *Node Error* the quantity $\mathrm{Err}(n_i) = |E(n_i) - E'(n_i)|/E(n_i)$ where $E(n_i)$ is the real switching activity of node n_i and $E'(n_i)$ is the estimated switching activity of this node. If the $E'(n_i)$ quantity is less than a small positive number (i.e. in our experiments 0.05), then the corresponding relative error $\mathrm{Err}(n_i)$ is not considered. For a combinational circuit with N gates and a specific input vector set V_j, we define as *Total Power Consumption* the quantity:

$$\text{Total Power}(V_j) = \frac{1}{2} \cdot V_{\mathrm{dd}}^2 \cdot f \cdot \sum_{i=1}^{N} E_{\mathrm{Eff}}(n_i). \qquad (10)$$

The effective switched capacitance, $E_{\mathrm{Eff}}(n_i)$, is defined by the product of the switching activity $E(n_i)$ and the total capacitance load of node n_i, $C_{n_i} = F_{n_i} C_{\mathrm{g}}$ where F_{n_i} is the fanout of this node and $C_{\mathrm{g}} = 0.05$ pF is a typical input capacitance (input gate + the wire load capacitance). We define as *Total Error* the quantity:

$$\text{Total Error}(V_j) = \frac{|\text{Total Power}(V_j) - \text{Total Power}(V_j)'|}{\text{Total Power}(V_j)}, \qquad (11)$$

and as *Mean Error* the quantity:

$$\text{Mean Error}(V_j) = \frac{1}{N} \sum_{i=1}^{N} \mathrm{Err}(n_i). \qquad (12)$$

Table 1 illustrates various characteristics of the selected benchmark circuits in terms of primary inputs, primary outputs, number of gates and number of logic levels.

To prove the accuracy of the proposed method, we apply an input stream of 500,000 vectors to each circuit and compare the estimated transitions of the proposed method with the transitions derived by using the QuickSim II switch level simulator of Mentor Graphics. The vectors of the input stream are pseudo-random temporal vectors, whose each input signal x_i has a static probability $p_i^{x_i} \in [0,1]$, and a transition probability $E^{x_i} \in [0,1]$, where $E^{x_i} \neq 2p_1^{x_i}(1 - p_1^{x_i})$. Three different gate delay models were considered; the zero-, unit- and inertial-gate delay model.

Table 1
Circuits characteristics

Circuit	# Inputs	# Outputs	# Gates	# Levels
C1355	41	32	180	15
C1908	33	25	205	21
C2670	233	64	422	20
C3540	50	22	817	34
C499	41	32	176	17
C6288	32	32	1491	73
C7552	207	107	1154	21
C880	60	26	221	22
alu4	14	8	543	35
cu	14	11	104	14
des	256	245	2437	17
F51m	8	8	83	10
vda	17	39	391	16

Table 2 presents the real error (%) in power estimation of the proposed method, under the assumed gate delay models (i.e. zero, unit and real), if $Depth = 3$ and $N\_vars = 8$ are chosen. More specifically, the column Total represents the *Total Error* of the estimated power dissipation, while the column Mean represents the *Mean Error* quantity. The calculated average errors are 7.5%, 8%, and 19% under zero-, unit- and inertial-gate delay model, respectively.

In order to prove the efficiency of the proposed method, we perform the same experimental procedure using the method of [10], which is the best to our knowledge method to estimate the switching activity of large circuit using probabilistic techniques. The corresponding results are given in Table 3. It can be seen that the method of [10] is not applicable for the majority of the circuits, because these circuits have large reconvergent regions, which require extremely high memory size to manipulate the corresponding large symbolic expressions. On the other hand, the proposed method manipulates efficiently these circuits due to

Table 2
Power estimation errors for *Temporal* inputs with *Depth* = 3,*N_vars* = 8

Circuit	ZERO		UNIT		INERTIAL	
	Total	Mean	Total	Mean	Total	Mean
C1355	0.610	2.774	2.853	3.948	7.201	25.757
C1908	1.029	3.757	1.025	16.236	8.195	29.653
C2670	0.516	6.756	4.220	8.441	12.397	16.887
C3540	0.609	14.498	10.573	11.238	9.672	19.502
C499	0.270	1.516	1.101	4.719	0.658	25.908
C6288	3.858	20.530	24.812	24.591	9.873	32.139
C7552	2.337	11.552	2.557	10.026	15.870	26.603
C880	0.502	2.791	0.343	2.676	3.831	4.881
alu4	1.415	15.736	0.959	13.181	6.660	20.620
Cu	0.746	2.156	0.256	0.393	2.565	10.840
Des	0.425	3.437	2.121	2.761	6.969	17.907
f51m	0.233	6.775	0.296	5.373	0.341	6.188
Vda	0.168	4.907	1.716	3.637	6.771	14.361
Average	0.978	7.476	4.064	8.248	7.000	19.327

Table 3
Power estimation errors of method of [10] for *Depth* = 3

Circuit	ZERO		UNIT		REAL	
	Total	Time	Total	Time	Total	Time
C1355	1.83	2.28	0.43	4.66	16.02	18.42
C1908	N/A	N/A	N/A	N/A	N/A	N/A
C2670	N/A	N/A	N/A	N/A	N/A	N/A
C3540	N/A	N/A	N/A	N/A	N/A	N/A
C499	0.35	1.82	0.74	4.67	6.07	18.45
C6288	4.81	63.37	22.48	330.28	280.77	1902.03
C7552	N/A	N/A	N/A	N/A	N/A	N/A
C880	N/A	N/A	N/A	N/A	N/A	N/A
alu4	N/A	N/A	N/A	N/A	N/A	N/A
cu	1.43	0.88	1.33	0.74	2.96	5.18
des	N/A	N/A	N/A	N/A	N/A	N/A
F51m	0.26	9.41	2.06	3.94	1.65	11.26

the efficient partitioning, using the heuristic presented in Section 4 and the efficient manipulation of the constructed OBDDs.

Although the primary input signals are assumed to be mutually independent, we perform another set of experiments using spatiotemporal primery inputs to check the accuracy of the method. For this reason an input stream of 500,000 spatiotemporal vectors generated by a LFSR (*linear feedback shift register*), are used. The results are shown in Table 4.

It is inferred that the average errors are increased and equals to 9.6%, 12.5% and 28% assuming zero-, unit-, and inertial-gate delay model respectively. Although, the proposed method does not capture the dependencies of the primary inputs, since they are assumed to be mutually independent, the error levels are adequate. There is an increase of 10%, when inertial delay is assumed, compared with the errors that are coming by using uncorrelated primary inputs.

Table 5 presents the run times in seconds of the proposed method. These figures were obtained on an HP-UX C180 with 512 Mbytes of main memory (while 64 Mbytes are quite enough for the proposed method). The estimated run times of the

Table 4
Power estimation errors for LFSR input with $Depth = 3$, $N\_vars = 8$

Circuit	ZERO		UNIT		INERTIAL	
	Total	Mean	Total	Mean	Total	Mean
C1355	0.445	2.028	2.345	4.066	9.214	24.809
C1908	0.413	4.832	0.235	11.837	15.379	47.617
C2670	0.492	7.992	1.459	8.934	16.267	26.025
C3540	0.098	13.144	12.475	14.211	9.221	18.915
C499	0.144	0.732	1.167	4.282	9.896	28.425
C6288	4.929	19.340	21.340	22.276	15.568	31.946
C7552	1.617	5.413	1.345	6.448	19.109	27.522
C880	0.488	5.499	1.308	6.930	2.666	8.999
Alu4	0.052	21.606	0.838	22.480	9.933	31.554
Cu	0.284	12.271	0.343	8.364	2.350	14.027
Des	1.083	5.924	0.550	7.053	9.871	29.220
f51m	6.063	18.336	4.424	16.200	6.084	18.968
Vda	0.912	7.898	7.839	29.993	24.781	54.832
Average	1.309	9.617	4.282	12.544	11.565	27.912

Table 5
Average power values and run times

Circuit	ZERO	UNIT	INERTIAL
	Time	Time	Time
C1355	1.22	1.35	1.43
C1908	0.73	0.83	1.14
C2670	0.76	1.58	1.64
C3540	1.69	4.02	4.07
C499	0.18	0.44	0.57
C6288	3.39	13.07	17.16
C7552	2.87	5.47	5.97
C880	0.36	0.86	0.89
alu4	0.89	2.72	2.93
cu	0.08	0.14	0.14
des	9.41	13.64	14.06
f51m	0.12	0.20	0.20
vda	0.58	1.26	1.32
Average	1.71	3.51	3.96

proposed method are small enough and the average run time is 1.71, 3.51 and 3.96 s for zero-, unit- and real-inertial gate delay model, respectively. In order to achieve better accuracy, we have to increase the chosen depth of the reconvergent regions, *Depth* and/or the number, *N_vars* of maximum variables for each *RDBF*.

The errors of the proposed method are coming from: (i) the consideration of the first order temporal correlations only, (ii) the values of the parameters *Depth* and *N_vars*, which are used in the experimental procedure, and (iii) the assumption that the input vectors are mutually independent. More specifically, the most important factor that decreases the accuracy of the proposed method is the assumption that the primary inputs are assumed to be independent. Also, higher order temporal correlations can be handled easily by extended the mathematical model. However, as it proved in [6] the accuracy is improved slightly, while the computational complexity is increased prohibitively.

6. Conclusions

Assuming a real delay gate model, a method to estimate the power dissipation of a logic circuit was introduced. The proposed method is an extension of the zero-delay probabilistic methods and takes into account the first-order temporal correlations and structural dependencies. A modified Boolean function, which describes the logic behaviour of a signal in time domain, is proposed. An efficient algorithm to handle accurately large combinational circuits is presented. The accuracy and efficiency of the introduced method to handle

large and complex combinational circuits is proved by a set of experimental results. Since the proposed method does not capture the spatiotemporal dependencies among the circuit signals our future work is to extent the proposed method to fetch the above issue.

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