**Proceedings of the**

# 33rd International Workshop on Logic & Synthesis (IWLS 2024)

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## Keynotes

### Can AI Design and Verify Your Design?

Ziyad Hanna, *Cadence Design Systems, Israel*

Abstract: In this talk, I will explore the significant impact of artificial intelligence (AI) in addressing the mounting complexity and demands within chip design domain. With an anticipated exponential growth in annual revenue reaching the trillion-dollar mark, driven by the rapid growth in key markets in 5G, Hyperscalers, autonomous vehicles, AI, and industrial IoT. The chip design market is trending into a fourfold increase in project volume with tenfold complexity. The current design and verification methodologies are lacking in capacity to meet this surge, highlighting the shortage of qualified engineers to meet the aggressive market demand. AI technologies stand at the forefront of transforming design and verification processes, offering unparalleled efficiency and cost-effective solutions to meet the escalating market needs. In this talk, I will address the inherent challenges in the chip design industry, analyze the current landscape of automation, machine learning (ML), and cutting-edge generative AI technologies. I will also discuss a strategic direction for harnessing AI to enhance design synthesis and verification, including the automatic generation of programs supported by natural language processing (NLP) and generative AI, the creation of temporal assertions from design specifications, the integration of high-level synthesis (HLS) and formal verification, and the exploration of the latest advancements in AI technologies for full design and verification flow for achieving the aggressive demand on performance, power and area. Furthermore, the presentation emphasizes the essence for collaborative initiatives between industry and academia to drive forward transformative advancements and innovations within the chip design and verification domain with AI.

### Symmetric Is Better: Can We Exploit Regularities in Logic Synthesis?

Valentina Ciriani, *University of Milano, Italy*

Abstract: The standard synthesis of Boolean functions is aimed at designing optimized circuits according to given cost criteria. For this purpose, the algebraic form of the function is manipulated, as it directly reflects the cost of the corresponding circuit. Depending on the design needs, different two-level or multi-level forms are considered, and ad hoc algorithms are used to express and minimize such forms. In all cases, the functions under consideration encode “real life” problems, hence they often exhibit a “regular” structure that can be exploited by synthesis algorithms. This talk aims to describe several function regularities based on the EXOR operator. Moreover, we show how these regularities can be exploited in logic synthesis for standard and emerging technologies. Finally, we show how regularities can also ease polynomial verification.

**Toward Software-to-Atoms Open-Source RISC-V Computing Platforms: Is Open-Source Synthesis Ready for Prime Time?**

Luca Benini, *ETH Zurich / University of Bologna, Switzerland / Italy*

Abstract: The success of the RISC-V free and open ISA has ushered us in the era of open-source computing hardware. As of today, open-source designs exist targeting a wide range of RISC-V based computing systems, from tiny microcontrollers to high-performance many-core, and industry adoption of open-source computing hardware is accelerating. However, a key open question is if we can, or even should, push further, open-sourcing design automation tools and technology libraries, PDKs, toward the vision of enabling "software-to-atoms" open-source computing platforms. In this talk I will try to assess where we stand and provide a personal view on key challenges and future trajectories, drawing from a decade of experience in designing and industrializing open-source hardware.

## Special Session: Unconventional Cost Functions for Logic Synthesis

Abstract: In recent years, the field of logic synthesis for beyond-CMOS technologies has seen significant changes, revealing new cost functions and constraints that challenge traditional assumptions. In some implementations, splitters and buffers are essential for path balancing. However, recent advancements in fabrication and physical simulation of certain computational nanotechnologies revealed the necessity for 100% planar networks. This unconventional cost metric creates a new playground for innovation in logic synthesis.

This special session will provide a physical background on why wire crossings are infeasible in computational nanotechnologies, and present initial strategies for crossing mitigation and legalization. Most importantly, it serves as a call to the logic synthesis community to participate in this exciting new field.

**Logic Synthesis for Emerging Nanocircuits**

Zhufei Chu (Ningbo University)

**The Case for Planar Logic Synthesis: Crossing Costs in Nanotech**

Marcel Walter (Technical University of Munich)

## Programming Contest Session

**Programming Contest Presentation and Award Announcement**
Alan Mishchenko and Yukio Miyasaka (UC Berkeley)

## Regular Papers

**Information Graph-Based Resubstitution For Networks of Look-Up Tables (best student paper candidate)**
Andrea Costamagna, Alessandro Tempia Calvino (EPFL), Alan Mishchenko (UC Berkeley), and Giovanni De Micheli (EPFL)

**Post-Mapping Resubstitution For Area-Oriented Optimization**
Andrea Costamagna, Alessandro Tempia Calvino (EPFL), Alan Mishchenko (UC Berkeley), and Giovanni De Micheli (EPFL)

**Randomized transduction for high-effort logic synthesis**
Yukio Miyasaka, Alan Mishchenko, John Wawrzynek (UC Berkeley), Dino Ruic, and Xiaoqing Xu (X, the moonshot factory)

**New Stories on the Structural Bias**
Petr Fišer and Jan Schmidt (Czech Technical University in Prague)

**Row-Shift Decompositions for Classification Functions: Application to Machine Learning Problems**
Tsutomu Sasao (Meiji University)

**Practical Boolean Decomposition for Delay-driven LUT Mapping (best student paper candidate)**
Alessandro Tempia Calvino (EPFL), Alan Mishchenko (UC Berkeley), Giovanni De Micheli (EPFL), and Robert Brayton (UC Berkeley)

**Recovering Hierarchical Boundaries in a Flat Netlist (best student paper candidate)**
Kuo-Wei Ho, Yu-Wei Fan, Jie-Hong Roland Jiang (National Taiwan University), Alan Mishchenko, Robert Brayton (UC Berkeley), and Sean Weaver (U.S. National Security Agency)

**To Box or Not to Box: Preserving Special Logic Blocks in Technology-Independent Logic Optimization**
Siang-Yun Lee and Heinz Riener (Cadence Design Systems)

**SimGen: Simulation Pattern Generation for Efficient Equivalence Checking**
Carmine Rizzi, Sarah Brunner (ETH Zurich), Alan Mishchenko (UC Berkeley), and Lana Josipović (ETH Zurich)

**Elevating Boolean Matching to the Word Level (best student paper candidate)**
Jiun-Hao Chen, Hsin-Ying Tsai, Kuo-Wei Ho, and Jie-Hong Roland Jiang (National Taiwan University)

**Reducing Wire Crossings in Field-Coupled Nanotechnologies**
Benjamin Hien, Marcel Walter (Technical University of Munich), and Robert Wille (Technical University of Munich, Software Competence Center Hagenberg GmbH)

**Insights from Basilisk: Are Open-Source EDA Tools Ready for a Multi-Million-Gate, Linux-Booting RV64 SoC Design?**
Philippe Sauter, Thomas Benz, Paul Scheffler, Frank K. Gürkaynak (ETH Zurich), and Luca Benini (ETH Zurich, University of Bologna)

**Enabling Scalable Sequential Synthesis and Formal Verification in an Industrial Flow**
Eleonora Testa (Synopsys), Dewmini Marakkalage (EPFL), Michael Quayle, Sudipta Kundu, Abhishek Kumar, Diptanshu Ghosh, Giulia Meuli (Synopsys), Giovanni De Micheli (EPFL), and Luca Amaru (Synopsys)

**CRUSH: A Credit-Based Approach for Functional Unit Sharing in Dynamically Scheduled HLS**
Jiahui Xu and Lana Josipović (ETH Zurich)

**Global Crossover: An Evolution Strategy for Logic Synthesis**
Hanyu Wang (ETH Zurich), Chang Meng, and Giovanni De Micheli (EPFL)

**On Neural Networks for Automatic Test Pattern Generation**
Lizi Zhang and Azadeh Davoodi (University of Wisconsin–Madison)

**HardCore Generation: Generating Hard UNSAT Problems for Data Augmentation**
Joseph Cotnareanu (McGill University), Zhanguang Zhang, Hui-Ling Zhen, Yingxue Zhang (Huawei Noah's Ark Lab), and Mark Coates (McGill University)

**GraSS: Combining Graph Neural Networks with Expert Knowledge for SAT Solver Selection**
Zhanguang Zhang, Didier Chetelat (Huawei Noah's Ark Lab), Joseph Cotnareanu (McGill University), Amur Ghose, Wenyi Xiao, Hui-Ling Zhen, Yingxue Zhang, Jianye Hao (Huawei Noah's Ark Lab), Mark Coates (McGill University), and Mingxuan Yuan (Huawei Noah's Ark Lab)

## Poster Papers

**Maelstrom: A Logic Synthesis Technique for Asynchronous Circuits**
Karthi Srinivasan and Rajit Manohar (Yale University)

**Logic Synthesis with Generative Deep Neural Networks**
Xihan Li (University College London), Xing Li, Lei Chen, Xing Zhang, Mingxuan Yuan (Huawei Noah's Ark Lab), and Jun Wang (University College London)

**A Systematic Framework for Opportunistic Pruning of Deep Neural Networks on Edge Devices**
Robert Viramontes and Azadeh Davoodi (University of Wisconsin–Madison)