On Neural Networks for Automatic Test Pattern Generation

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ABSTRACT

Automatic Test Pattern Generation (ATPG) algorithms such as FAN and PODEM heavily rely on a backtracing step to explore the search space. Conventional implementations often use a single metric such as a testability measure to guide backtracing. Recently, Neuron Network (NN) models were proposed which combine multiple metrics to make a better backtrace decision. This paper identifies two fundamental, unresolved issues for effective and efficient use of NNs for ATPG: (1) portability of the NN model across different levels of a combinational circuit; (2) significant runtime overhead when using the NN model in backtrace decisions of each gate. To address these issues, a hybrid approach is proposed which builds and applies the NN model to only selected levels of the circuit. Guidelines to select the level and to train circuits are also discussed in this context. Also, a lookup technique is proposed to reuse the results of prior inferences at each gate to further accelerate the runtime. Experiments show significant improvement in runtime and/or ATPG-related metrics compared to an NN model adopted from a recent work.

1 INTRODUCTION

Automatic Test Pattern Generation (ATPG) is an NP-hard problem [10]. Many existing heuristics aim to improve the runtime of achieving a reasonable solution. Most recent ATPG algorithms are based on extensions of PODEM [2, 11] which search the space of assignments to a subset or all Primary Inputs (PIs), or the flipflop content (if adopted for sequential circuits). The search space in PODEM-like algorithms is modeled as a decision tree with nodes representing the PIs. The actual size of the decision tree which directly impacts the runtime of the algorithm is known when a feasible assignment is found for some (or worst-case for all) PIs to ensure activating a fault site and propagating the fault effect to at least one primary output (PO).

A fundamental issue impacting the runtime of PODEM-like algorithms is effective realization of a recurring backtracing step to build a path from an internal signal line (such as the fault site) to a PI. Building a backtrace path requires making backtrace decisions at individual gates to select the most promising fanin based on known information about the circuit. Each backtrace path identifies a PI and its assignment, hence the order of backtrace paths impacts the order the PIs are listed in the decision tree. They also impact the number of back*tracks* before the algorithm can terminate, hence the tree size. A back*track* (different from a back*trace*) occurs whenever an infeasible PI assignment is found and requires expanding the tree to explore new directions in the circuit.

Figure 1(a) shows an example circuit. Two decision trees are shown in (b) corresponding to different backtrace paths based on fanin selection at the output gate. In the left one, no backtracks happen by selecting signal E which assigns $B = 0$. However, in the right tree, signal L is initially selected which causes a backtrack.

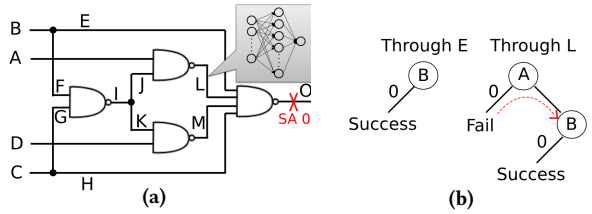


Figure 1: (a) Circuit with a stuck-at-0 fault; (b) Two possible decision trees corresponding to selecting different backtracing paths based on fanin selection at the output gate. Neural networks are used to predict the most promising fanin of a gate for better backtracing. Our work discusses challenges and opportunities of using neural networks for ATPG.

The above example shows that the core part impacting the runtime of a PODEM-like algorithm is correctly identifying the fanin to backtrace at a single gate to avoid backtrack when reaching the PI. Different heuristic metrics may be used to make this decision, e.g., selecting the fanin with the best testability measure such as COP [1], SCOAP [7], and CAMELOT [12].

Recently, neural networks (NNs) have been used to combine different metrics with the goal to improve backtracing at a gate [14–17]. In [14], an NN model was proposed which received different testability measures and information about the gate type as input features. (The information about the gate type was fed as a 'one-hot' vector of all 0s except a 1 entry at the index corresponding to the gate type in question.) The model was integrated with PODEM which required inference calls to the NN for each backtrace decision. The runtime benefits happened when the number of backtracks was significantly reduced to compensate for the overhead of inferences.

Next, unsupervised learning techniques were proposed [16, 17] which first applied Principal Component Analysis (PCA) to deal with correlated input features. The top two principal components were used as input features to create a smaller NN model. Performing PCA before each inference introduced overhead. Moreover, PCA was not compatible with the one-hot format needed to communicate the gate type information. The one-hot gate type vector which carried important information for making a backtracing decision was then dropped as a feature in the unsupervised approaches.

In this paper, besides the above-listed areas of improvement, we identify two fundamental issues to make NN-guided backtracing effective and efficient for ATPG. These two are: (1) portability of a NN model across different levels of a combinational circuit; (2) significant runtime overhead of NN inference calls at each gate throughout the course of the algorithm. First, we show there exists significant variations in the values of some input features (i.e., testability measures) based on the level of a gate in the circuit. We show building a single NN model across all levels cannot improve ATPG due to this variation. There is also no runtime advantage to use NN when the level is small or large.

We then propose a hybrid approach to train and apply the NN model at only select levels of the circuit. We propose guidelines on how a level can be selected. We also introduce metrics to decide which circuits may be selected to extract data for training purposes.

We also propose a lookup technique to speed up the runtime of NN-guided backtracing at each gate. This is based our observation that majority of the inferences at each gate are already-computed values which can be reused.

Overall, the summary of our contributions are listed below:

- We identify fundamental issues with NNs to make the backtracing step of ATPG efficnet and effective.
- We propose hybrid use of NNs at select levels, and discuss effective selection of training data to address the issues.
- We also show a significant amount of NN computations can be reused at a gate which allows skipping many inferences.
- Our NN model is flexible in receiving different types of input features such as gate type information in the one-hot format.

In our experiments, we integrate our ideas with the FAN algorithm implemented by the open source ATALANTA tool [3]. We show improvements of on-average 32.6% in the number of backtracks and 26.9% in runtime compared to ATALANTA, when varying the number of backtracks. This is with same or better fault coverage and/or ATPG effectiveness. We also show high improvement rates compared to NN-guided backtracing using supervised learning.

2 RELATED WORK

One of the earliest ATPG algorithms is Roth's D-Algorithm [4] which defines the D algebra. It is a complete algorithm with the search space size of 2^N where N is number of all signal nodes in the circuits. Later, PODEM [11] improved it by searching assignments for only the PI nodes. It decreased the size of search space to $2^{\#PI}$ and incorporated use of heuristic measures to guide its backtracing. Next, FAN [2] was proposed which compared to PODEM, it detected conflicts much faster and reduced the cost of backtracks.

Early work since 90s showed attempts to learn from data to improve ATPG. The work SOCRATES [9] used static and dynamic learning to accelerate ATPG. Static learning applied a preprocessing step that assigned certain signals and stored implications. Dynamic learning applied a similar procedure dynamically, for all signals that have unspecified logic values. The work [6, 8] was among the first to use information from previously detected faults by introducing an E-frontier. The first explicit application of NNs in ATPG was [18] which used a bi-directional binary NN.

Recent works have used NNs to improve backtracing in PODEM [14–17] by effectively combining multiple heuristic metrics [5, 13]. Both supervised learning [14, 15] and unsupervised learning [16, 17] were applied. The work [14] used a two-layer NN with a single output to combine multiple heuristic metrics including gate type, circuit level, COP controllability and observability. The NN model was called for any (not-yet implied) fanin of a gate, for each gate on a backtraced path. The output of the NN represented probability of successful backtrace if a particular fanin of a gate was selected. The fanin with highest probability was selected for backtracing. The NN model was called for every fanin of a gate in every backtraced path in the circuit. Training data was collected from different levels of a circuit in a mixed fashion.

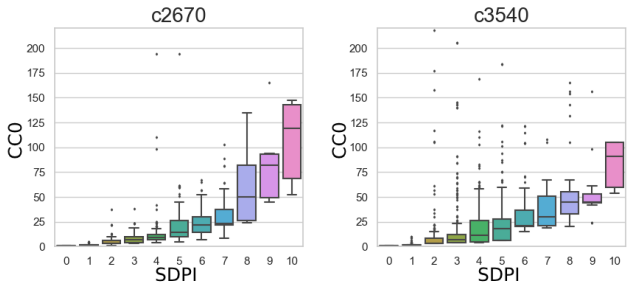


Figure 2: Statistics of SCOAP Combinational Controllability 0 (CC0) as a function of the Shortest Distance to the PIs (SDPI). Data shows training/building a single NN model across all circuit levels is not effective.

3 EFFECTIVE NN-GUIDED BACKTRACING

3.1 Our Observations

The NN-based backtracing techniques described earlier suffer from a number of challenges which we have identified and listed below:

- **Variations in signal line features in the same circuit:** Signal line features such as SCOAP testability and COP are important inputs to the NN model. However, they can significantly vary as a function of distance to PIs with some features not having any guaranteed range. For example, combinational controllability (CC0 and CC1) are much smaller when a line is close to the PIs (i.e., more controllable) and greater near the POs. This means the knowledge derived from data near the PIs cannot be directly transferred to circuit lines near POs. Figure 2 shows an example of the ranges of CC0 as a function of Shortest Distance to any PI (SDPI) for two circuits. As can be seen, for the same circuit, there is significant variation in the values of CC0. Training a NN by directly using these values across all levels won't be effective.
- **Variations in signal line features across circuits:** The previous issue also exists from one circuit to another even when considering the same circuit level. This is primarily due to the distinct characteristics exhibited by individual circuits. For example, as seen in Figure 2, for SDPI=10, the highest CC0 is about 150 in c2670 while it is about 100 in c3540. We note the variation seen at the same level across different circuits is significantly lower than variations across different levels even in the same circuit.
- **Not all signal lines can benefit from NN models:** The cost of a backtrack is very low for a line which connects to a small number of PIs (i.e., line close to the PIs). The search space for these lines is so small that even considering an exhaustive approach, the cost is still lower than the cost of computing the output of a simple NN model. Moreover, the lines near PIs have very similar feature values, e.g., similar distances to PIs, similar controllability measures, etc. The high resemblance of data make it hard for NNs to learn and be useful in such scenarios. For the lines near PO, there is not much benefit to use NN to decide backtrace at a gate because they have a huge search space and all fanins of a gate are likely to lead to a successful backtrace. Using NN-guided backtracing is not beneficial in these cases.

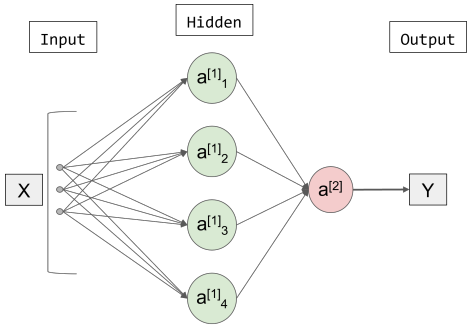


Figure 3: Single-layer NN used for integration with ATPG.

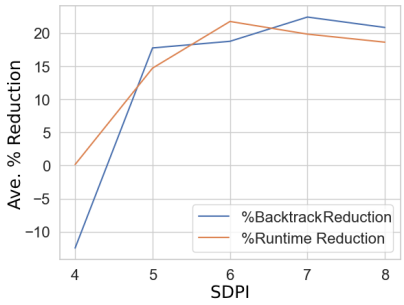


Figure 4: Average reduction in backtrack and in runtime as a function of circuit level (SDPI). We observe SDPI=6 results in the most overall reduction in runtime.

3.2 Proposed Techniques

To develop an ATPG algorithm which effectively uses neural networks, it is important to acknowledge that while sophisticated NN models can result in better performances, they may not be worth the runtime overhead of additional inferences.

Based on the presented observations, in this work, a single hidden-layer NN model is found to be most effective for ATPG. Shown in Figure 3, the model consists of input features, a hidden layer, and an output neuron. The input features are denoted as $X \in \mathbb{R}^{d_1}$ and the hidden layer neurons are $A \in \mathbb{R}^{d_2}$, where d_1 is the number of input features and d_2 is the number of neurons in the hidden layer. The output Y is a real value between 0 and 1. The output works as a measurement of how likely this line may backtrace successfully. The forward propagation is expressed as:

$$A = f(W_1^\top X + b_1) \tag{1}$$

$$Y = f(W_2^\top A + b_2) \tag{2}$$

where $W_1 \in \mathbb{R}^{d_1 \times d_2}$ and $W_2 \in \mathbb{R}^{d_2 \times 1}$ are the weight matrices, and $b_1 \in \mathbb{R}^{d_2}$, $b_2 \in \mathbb{R}$ are the biases, f is the activation function implemented as the sigmoid function.

3.2.1 Hybrid Implementation and Acceleration. In our hybrid implementation, the NN model is trained on data generated for specific levels and is only applied to the same corresponding levels of a circuit. For the remaining levels, the default metrics in the ATPG tool are used to decide the fanin during a backtrace. This addresses the issues discussed earlier: Since the model is trained on and applied to the same level, the features are always comparable to each other.

Figure 4 shows how a circuit level may be identified for hybrid implementation. The plot shows average percentage reduction in number of backtracks and in runtime as a function of circuit level (SDPI). This is compared to a non-hybrid version of ATPG when NN is not used at all. For each SDPI, a separate NN was trained using circuit data for only that level. The trained NN is only used for that level. As can be seen SDPI=6 results in the most reduction in runtime which is used in our experiments. At this level the backtrace can always benefit from the NN model such that the computation cost of NN is quiet often smaller than the cost of backtracks.

To further accelerate NN-guided backtracing, we observed that some circuit lines may be backtraced many times during the course of the algorithm (as the PI assignments change or due to signal implications). Therefore, a lookup table is established to record the NN model outputs for these lines to avoid redundant computations.

3.2.2 Input Features and Normalization. In this work, we adopt a broad range of input features for NN training. Whenever possible, data corresponding to a feature is normalized to ensure the gradient descent is much more stable and converges faster. Our considered input features are listed below:

- Shortest and Longest Distance to the PIs denoted by SDPI and LDPI, respectively. The LDPI feature is normalized to [0,1] for all gates with same SDPI, as explained earlier.
- SCOAP controllability measures, i.e., Combinational Controllability 0/1 (CC0 and CC1), which represent the difficulty of setting a line to 0 or 1, respectively. These measures contain valuable information in the paths containing the considered lines to the PIs. The SCOAP contrallability measures are also normalized between [0,1] for all gates with the same SDPI.
- COP controllability for a line is the probability of the line being 1 if the PIs are uniformly and randomly set to 0 or 1. This feature provides another approximation of how hard it is to observe a specific signal on a line. They are already in the [0,1] range so normalization is not needed.
- Encoded gate type. The gate type that connects to a line has a great impact on the backtracing process because it may directly impact the values that should be taken by the inputs. A gate type is encoded as one-hot vector. For example, "AND" gate is encoded as 0000001 and "OR" gate is encoded as 0000010. In our work, we consider 7 gate types.

Example: Consider the circuit in Figure 1. The features corresponding to line L are (LDPI, SDPI, CC0, CC1, COP) = (2, 1, 4, 2, 0.625). The gate type is "NAND", hence the one-hot vector 0100000.

Data Collection Process: To generate training data, a default ATPG algorithm (e.g., ATALANTA tool [3] in this work) was applied to several circuits. Both successful and failed backtracing instances were recorded. Meanwhile, the features of lines were also recorded during backtracing. When backtracing is completed (which could be either successful or fail), the same label is assigned to all lines on the same backtracing path. Specifically, if the backtracing results in PI assignment without any conflicts, it is considered successful and the related lines are labeled '1'. Otherwise, it is a fail and backtrack is needed so all lines on the backtracing path are labeled '0'.

It is very possible that a line may be recorded many times during the course of the ATPG algorithm run. The frequency of the labels for the same line represents the likelihood of successful backtracing if this line is chosen.

Example: Consider line O in the same example circuit. Table below shows the generated data (prior to normalization) for a successful backtrace to detect stuck-at-0 fault at this line.

Line	COP	LDPI	SDPI	CC0	CC1	Type	Label
O	0.902	3	1	7	2	0100000	1
L	0.625	2	1	4	2	0100000	1
J	0.750	1	1	3	2	0100000	1
F	0.500	0	0	1	1	0100000	1
B	0.500	0	0	1	1	0100000	1

3.3 Circuit Selection for Training

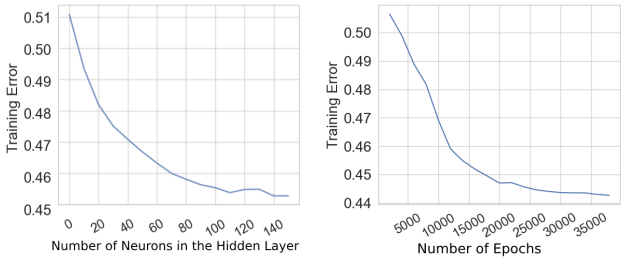
In practice, given a collection of circuits, a subset should be selected for training with the rest to be used for testing. To decide which circuits are suitable for training, the number of samples and the ratio between positively and negatively -labeled data are important. Positive and negative samples have 1 and 0 labels, respectively. If the number of training data points is small, the model will not function properly. Also, if the training data is highly imbalanced (as far as ratio of positive to negative samples), the model tends to have great bias. Table below shows data statistics that are collected from different circuits during the ATPG process.

	Signal Lines with SDPI=6				
Circuit	#Samples	#Pos	#Neg	Ratio	#Samples/Ratio
c1908	318	242	76	3.18	99.87
c1355	259	208	51	4.08	63.50
c2670	366	256	110	2.33	157.27
c3540	191	152	39	3.90	49.01
c5315	269	258	11	23.45	11.47
c6288	84	62	22	2.82	29.81
c7552	907	786	121	6.50	139.63

For each circuit, columns 2, 3, 4, 5 correspond to number of samples, positive samples, negative samples, and ratio of larger to smaller samples. The smallest value that the ratio can take is 1 when the number of positive and negative samples are equal to each other. This is ideal for training to have equal number of positive and negative samples. Column 6 reports total number of samples divided by the ratio in column 5. Column 6 may be used as a metric to decide if a circuit is a good candidate to select for training the NN. The higher number indicates a better candidate due to higher number of samples and/or sample ratio closer to the minimum (equal positive and negative samples). In this work, we used data from c1908 and c2670 for NN training. These two had the highest value in column 6 (except c7552 which we reserved for testing due to its larger size).

3.4 NN Design for Better Training

The main design decision for the NN is number of neurons in the hidden layer. We decide this number by looking at how the training error is impacted. As shown in Figure 5(a), models trained tend to have lower training error as the number of neurons in the hidden layer increases. But the improvement becomes trivial when the number of neurons is beyond 60, accompanied by an increase in the inference time. Therefore, in this work, the NN is designed to have a hidden layer with 60 neurons.



(a) (b)

Figure 5: Training error as function of (a) number of neurons in the hidden layer and (b) number of training epochs

In the figure, the training error is measured using the Binary Cross Entropy (BCE) which is defined as follows:

$$loss(X, y) = -[y \cdot log(f(X)) + (1 - y) \cdot log(1 - f(X))]$$

where X is the input feature, y is the label and $f(X)$ is model output.

Figure 5(b) shows the training error as a function of number of epochs. We set the number of epochs to 30000 to achieve the best training quality. Since we apply a pre-trained model, this number is not considered a significant overhead in runtime.

4 SIMULATION RESULTS

To show the impact of our NN-guided ATPG, we compared the following approaches in our experiments.

1. **FAN**: We used the open-source ATALANATA [3] tool which implements FAN using LDPI (Longest Distance to any PI) as heuristic measure for fanin selection during backtracing.
2. **NN-Hybrid**: This is the hybrid NN-guided approach proposed in this work. Specifically, we implemented a hybrid version using FAN as the base with the changes discussed in Section 3: The NN model was applied only to lines with SDPI=6. The model was designed and trained as presented in Section 3.4. For the remaining lines, we used the default SCOAP controllability measures for backtracing.
3. **NN-All**: This approach similar to NN-Hybrid, except that the ML model is applied on *all* circuit lines. The main difference compared to NN-All is that the NN model was trained using data extracted across *all* levels. This approach is essentially our best effort implementation of [14, 15] based on available information. We note, all configuration setup is same between NN-All and NN-Hybrid approaches.

The following metrics were used for evaluation:

- **Fault coverage** defined as percentage of detected faults compared to total number of faults.
- **ATPG effectiveness** defined as number of detected faults and number of faults identified as untestable divided by total number of faults. Untestable faults (a.k.a redundant) are typically a small percentage of total number of faults in practice but may take a significant portion of the ATPG runtime because they often require building a complete decision tree (exhausting all test patterns) to conclude a fault is untestable.
- **Number of backtracks** reported both as absolute and as a percentage improvement relative to the FAN case.
- **Runtime** reported in seconds.

Table 1: Comparison for the 'all-faults case' when stuck at 0/1 faults are injected on *all* lines. Parameter K is the backtrack limit.

		K=1000			K=10000			K=25000		
		FAN	**NN-All**	**NN-Hyb**	**FAN**	**NN-All**	**NN-Hyb**	**FAN**	**NN-All**	**NN-Hyb**
c1908	FaultCov.	99.52	99.52	99.52	99.52	99.52	99.52	99.52	99.52	99.52
	ATPG-Eff.	100	100	100	100	100	100	100	100	100
	#BTracks	1124	1037	486	4818	1037	486	4818	1037	486
	%BTrack	0	7.74	56.76	0	78.48	89.91	0	78.48	89.91
	Runtime	0.08	0.05	0.03	0.25	0.05	0.03	0.23	0.05	0.02
c2670	FaultCov.	95.74	95.74	95.74	95.74	95.74	95.74	95.74	95.74	95.74
	ATPG-Eff.	99.02	99.02	99.02	99.16	99.16	99.16	99.16	99.16	99.31
	#BTracks	31643	32743	30054	266551	273924	255392	611551	618924	545396
	%BTracks	0	-3.48	5.02	0	-2.77	4.19	0	-1.21	10.82
	Runtime	0.58	0.60	0.62	4.32	4.43	4.28	9.03	9.63	7.40
c3540	FaultCov.	96	96	96	96	96	96	96	96	96
	ATPG-Eff.	100	100	100	100	100	100	100	100	100
	#BTracks	181	232	193	181	232	176	181	232	176
	%BTracks	0	-28.18	-6.63	0	-28.18	2.76	0	-28.18	2.76
	Runtime	0.10	0.12	0.10	0.10	0.10	0.12	0.08	0.13	0.12
c5315	FaultCov.	98.9	98.84	98.9	98.9	98.84	98.9	98.9	98.84	98.9
	ATPG-Eff.	100	99.94	100	100	99.94	100	100	99.94	100
	#BTracks	116	3235	117	116	30235	117	116	75235	117
	%BTracks	0	-2688.79	-0.86	0	-25964.66	-0.86	0	-64757.76	-0.86
	Runtime	0.20	0.25	0.15	0.15	0.92	0.17	0.17	2.05	0.18
c6288	FaultCov.	99.38	99.35	99.56	99.41	99.43	99.56	99.41	99.43	99.56
	ATPG-Eff.	99.82	99.79	100	99.85	99.87	100	99.85	99.87	100
	#BTracks	15563	40835	7071	122384	197953	36230	302384	452212	81230
	%BTracks	0	-162.39	54.57	0	-61.75	70.4	0	-49.55	73.14
	Runtime	0.58	1.23	0.38	4.1	4.87	1.58	10.00	10.65	3.27
c7552	FaultCov.	98.16	98.08	98.17	98.16	98.08	98.17	98.16	98.08	98.17
	ATPG-Eff.	99.18	99.1	99.19	99.18	99.1	99.19	99.18	99.1	99.19
	#BTracks	99330	112005	80601	990330	1102005	792384	2475330	2752005	1977384
	%BTracks	0	-12.76	18.86	0	-11.28	19.99	0	-11.18	20.12
	Runtime	2.58	3.25	2.15	26.28	29.02	16.57	60.5	73.55	40.08
	Ave. Imp. #BTracks		-481.31%	**21.29%**		-4331.69%	**31.07%**		-10794.90%	**32.65%**
	Ave. Imp. Runtime		-95.69%	**21.75%**		-77.19%	**26.27%**		-190.66%	**26.89%**

4.1 Comparison in the All-Faults Case

Here, we consider the case when stuck-at-0 and stuck-at-1 faults are injected on all lines of each circuit. The three approaches were applied on the two training circuits (c1908, c2670) and four testing circuits (c3540, c5315, c6288, c7552), from the ISCAS85 suite, similar to [14, 15]. The approaches were also compared for different backtrack limits (denoted by K). Test pattern generation procedure terminates for each fault when the backtrack limit is reached. The results are shown in Table 1. Average improvements in number of backtracks and in runtime are reported for NN-All and NN-Hyb relative to FAN. We make the following observations:

- In terms of number of backtracks, NN-Hyb on-average has reduction of 21.29%, 31.07%, and 32.65% with increase in K. Higher K allows more time to detect a fault which makes NN-guided backtracing to have more improvement.
- Reduction in runtime is a direct consequence of reduction in number of backtracks. On-average reduction in runtimes are 21.75%, 26.27%, and 26.89% with increase in K.
- Fault coverage is always the same or even better (for c6288 and c7522) in NN-Hyb compared to the other approaches.
- ATPG effectiveness is always same or better. Specifically, for c6288, NN-Hyb achieves a fault coverge of 100% indicating all detectable and redundant faults are identified.
- The NN-All approach has worse performance. (The number of backtracks are only reduced in NN-All for c1908 compared to FAN.) Our NN-All is identical to NN-Hyb (so they are optimized extensively and in the same way) except that the neural network in NN-All is trained with data extracted across all levels.

4.2 Comparison for Hard-to-Detect Faults

In this experiment, we consider hard-to-detect (H2D) faults. To identify these, we first ran FAN with a list of all possible stuck-at-faults (0 and 1 stuck-at faults for each signal line). Next, FAN generates a list of aborted faults which are the ones it was not able to generate a test pattern with its default backtrack limit. These are also known as aborted faults. They may be detectable if a higher backtrack limit is given or they may be inherently untestable. In this experiment, we only used the circuits which had more than 10 H2D faults (i.e., more than 10 aborted faults). We additionally experiment with a higher backtrack limit (K=50000).

For each circuit, we report the number of H2D faults (aborted faults generated by FAN with K=100). Next, after running each approach with a higher backtrack limit (K=25000 and 50000), we also report the number of redundant and number of aborted faults. The results are reported in Table 2. We make the following observations from the table:

Table 2: Comparison for hard-to-detect (H2D) faults

		K=25000		K=50000	
		FAN	NN-Hyb	FAN	NN-Hyb
c2670	#H2D Faults	31	31	31	31
	#Redu+#Abor	8+23	12+19	8+23	16+15
	ATPG-Eff.	25.81	38.71	25.81	51.61
	#BTracks	598971	541183	1173971	980483
	Runtime	9.15	7.72	17.78	13.32
c6288	#H2D Faults	24	24	24	24
	#Redu+#Abor	0+12	0+8	0+12	0+8
	ATPG-Eff.	50.00	66.67	50.00	66.67
	#BTracks	302344	253790	602344	503790
	Runtime	9.98	3.83	20.03	7.85
c7552	#H2D Faults	68	68	68	68
	#Redu+#Abor	6+62	6+62	6+62	6+62
	ATPG-Eff.	8.82	8.82	8.82	8.82
	#BTracks	1550170	1550546	3100170	3100546
	Runtime	35.38	29.22	71.90	58.27
	Ave. Imp. ATPG-Eff		**27.77%**		**44.43%**
	Ave. Imp. #BTracks		**8.56%**		**10.94%**
	Ave. Imp. Runtime		**31.56%**		**34.96%**

- NN-Hyb performs significantly better than FAN as far as resolving the number of H2D faults. First, it performs better in terms of detecting a higher number of redundant/untestable faults. For example, in c2670 and for K=25000, out of 31 H2D faults, the number of aborted faults were reduced from 23 (in FAN) to 19 (in NN-Hyb). The number of faults identified as redundant/untestable was increased from 8 (in FAN) to 12 (in NN-Hyb). Therefore, NN-Hyb identified more faults as redunant and finished with fewer aborted faults. This behavior holds consistently and for both values of K.
- NN-Hyb has same or higher ATPG effectiveness for the same value of K. This means NN-Hyb is able to detect same or higher number of H2D faults (given that it identifies higher faults as redundant and has fewer aborted faults).
- Finally, in terms of runtime and number of backtracks, NN-Hyb is significantly better. For example, the average improvement in runtime over FAN is 31.56%and 34.96% for K=25000 and 50000, respectively. The average improvements in ATPG effectiveness were 27.77% and 44.43% with increase in K.

Note, in c7552, 62 of the H2D faults remain aborted for both FAN and NN-Hyb. Further experiments (even with backtrack limit of 10 million) suggest that these faults are highly unlikely to be detected. However, there is significant reduction in runtime in NN-Hyb compared to FAN for each K.

4.3 Impact of the Lookup Approach on Runtime

In our last experiment, we disable the lookup-based acceleration in NN-Hyb and compare the runtime with the case when it is enabled. The results are reported in Table 3. Recall, the lookup-based acceleration records NN inferences for each signal and only computes inferences if they have not been computed before. As can be seen, on average 30.33% improvement in runtime can be achieved. The dynamically-generated lookup table effectively eliminates the need for forward propagation of the NN model in the test pattern generation process, greatly reducing the computational efforts.

Table 3: Runtime of NN-Hyb with and without acceleration

	NN-Hyb (K=10000)	
	w/o lookup	w/ lookup (%Impr.)
c1908	0.067	0.033 (51%)
c2670	13.350	4.283 (68%)
c3540	0.117	0.117 (0%)
c5315	0.200	0.167 (17%)
c6288	1.867	1.583 (15%)
c7552	23.867	16.567 (31%)
Ave. Imp.		**30.33%**

5 CONCLUSIONS

In this work we first elaborated the issues with existing approaches for NN-guided ATPG algorithm. We then proposed a hybrid procedure for applying NN to select levels, along with guidelines for level selection, and effective training of the NN. We also proposed a lookup technique to reuse the existing computations in a NN as much as possible for higher speedups. Our simulation results demonstrated the effectiveness of our procedure in reducing the number of backtracks and in runtime of ATPG. These were observed along with same or better fault coverage *and* ATPG effectiveness.

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