Steven Bolt – Arbitration Demo Writeup

Initial Results

	Fmax	Setup Time
Slow 1100mV 85C	457.04 MHz	-1.188
Slow 1100mV 0C	433.84 MHz	-1.305
Fast 1100mV 85C	N/A	-0.245
Fast 1100mV 0C	N/A	-0.173

Largest failing path (also only path shown):

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
-1.188	q2[3]	Result[14]~reg0	clock	clock	1.000	-0.071	1.947

After new clock constraint created

	Fmax	Setup Time
Slow 1100mV 85C	317.26 MHz	16.848
Slow 1100mV 0C	313.58 MHz	16.811
Fast 1100mV 85C	N/A	18.059
Fast 1100mV 0C	N/A	18.169

Only path shown after new clock constraint created:

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
16.848	q1[3]	Result[13]~reg0	clk	clk	20.000	-0.118	2.864

Fmax is the maximum frequency that a design's clock can run at while still passing the timing report constraints as estimated by Quartus. The Fmax value is directly based on the design's Worst Negative Slack path (or longest path). Slack is the difference between the data request time and the actual arrival time of the data, according to the clock frequency specified in the sdc file. Setup time refers to the time before a rising clock edge in a synchronous design. The TimeQuest tool is used to validate the timing performance of all logic in a design. It supports the Sysnopsis Design Constraint format or sdc to allow the designer to specify timing constraints.

(shoutout this reddit post for helping me understand a lot of this)