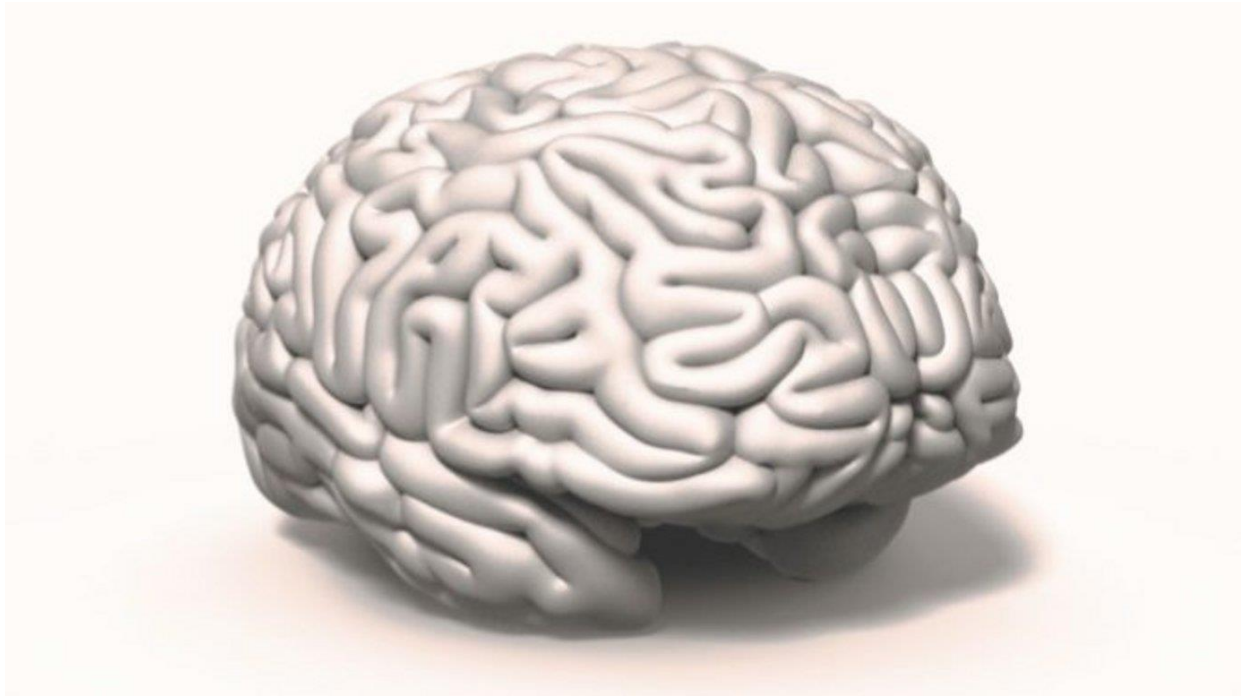
LUND UNIVERSITY

Lecture 13 – Neuromorphic systems

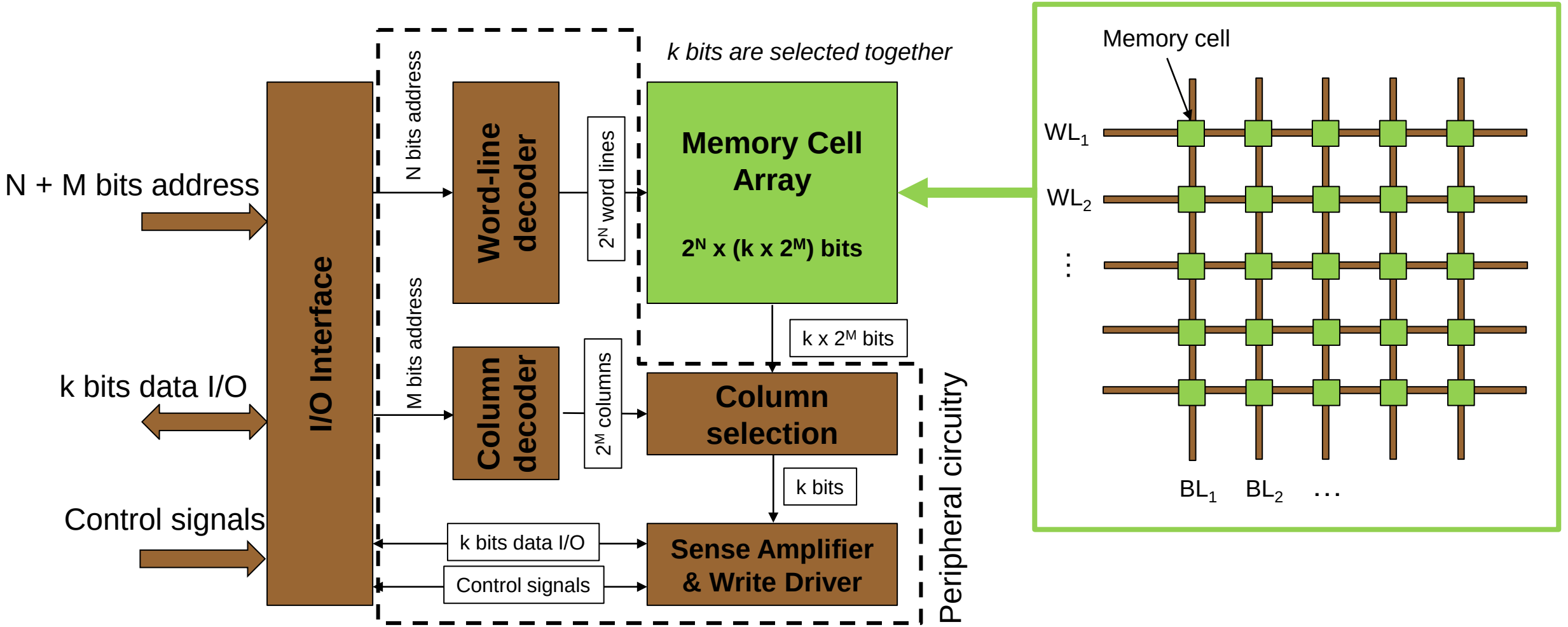
Outline – Lecture 13

- Selector devices
- CrossNet architecture
- Neuromorphic systems – examples
  - TrueNorth
  - Loihi
  - SpiNNaker



A full neuromorphic system?

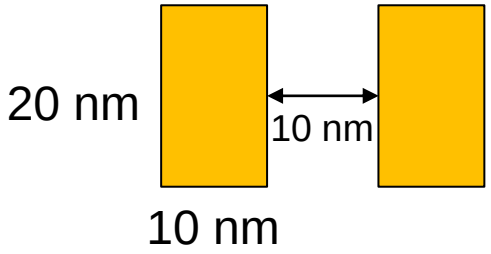
Architecture of the crossbar memory array



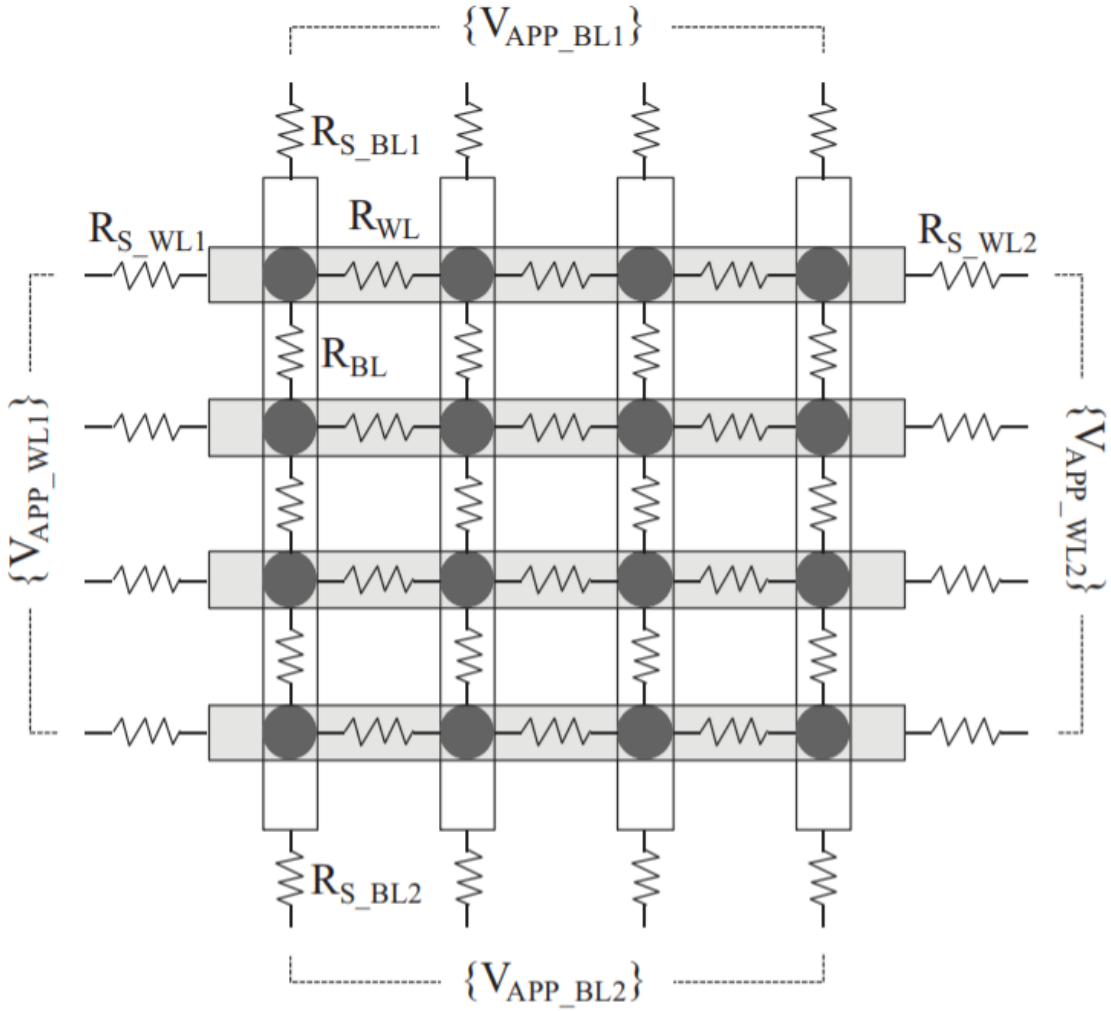
The crossbar

- Maximum density
  - → $4F^2$ per memory element, F as small as possible
  - → As large arrays as possible (> 1000 x 1000)

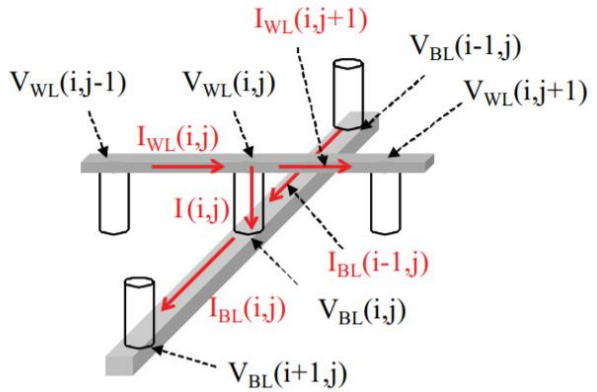
- 20 nm node:

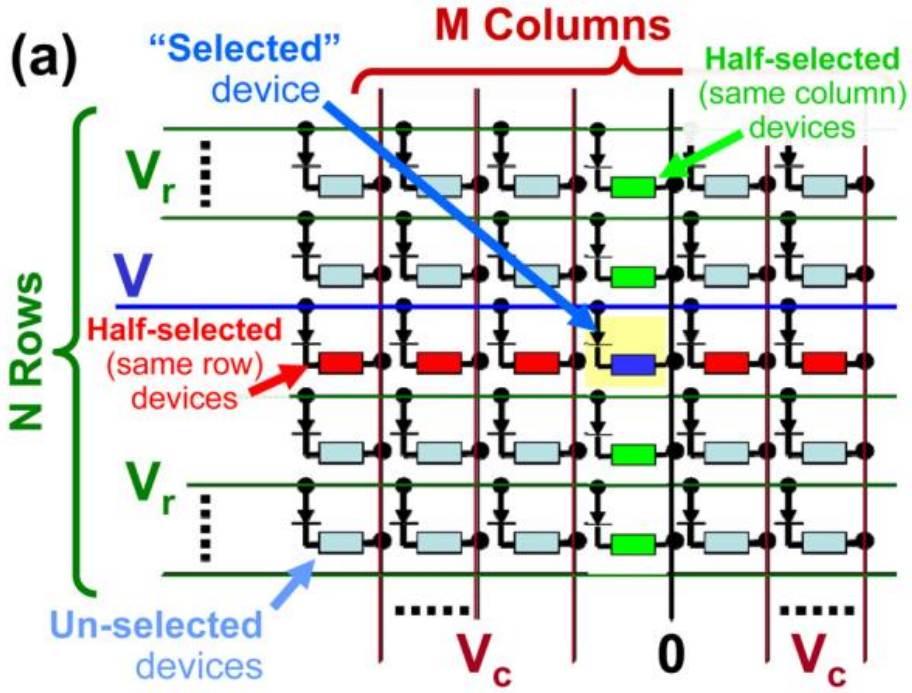


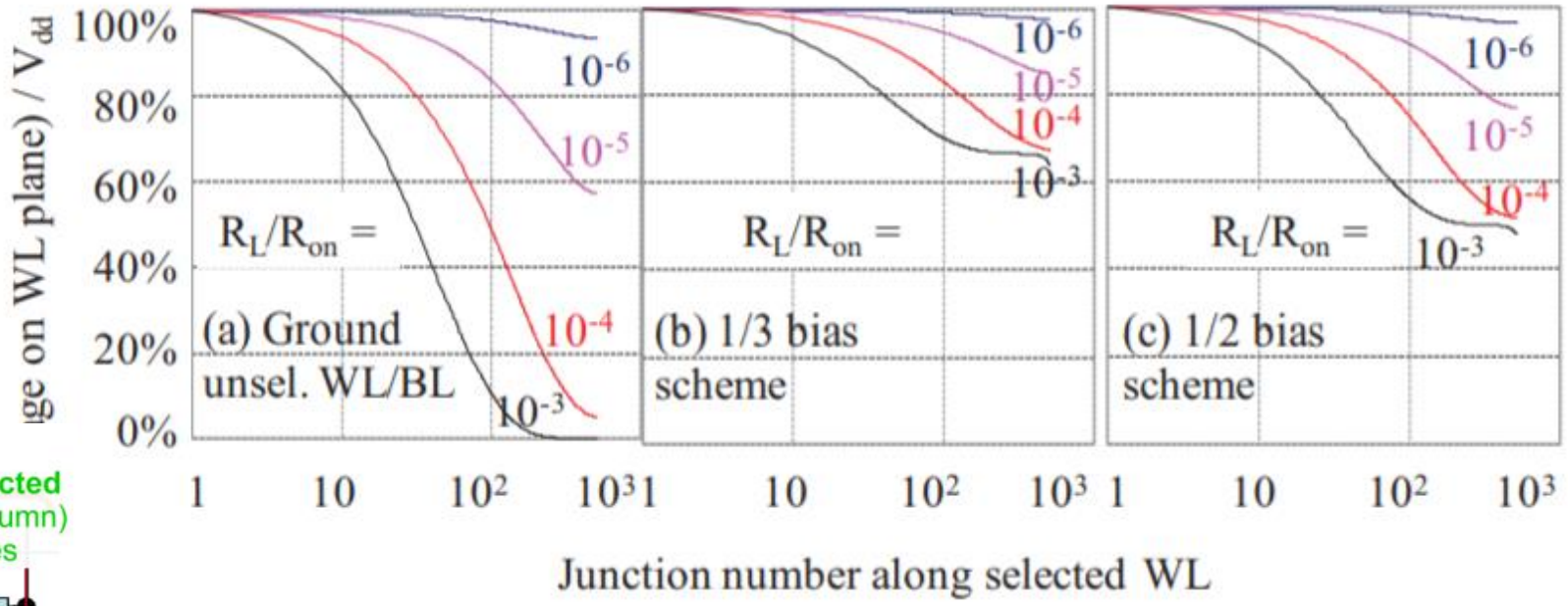
- Line resistance and Capacitance limits size



Biasing schemes





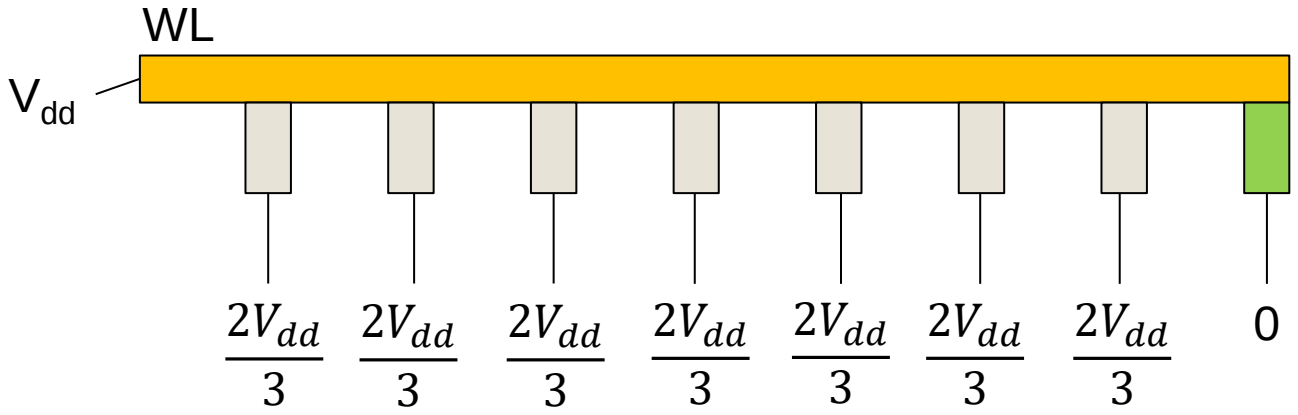


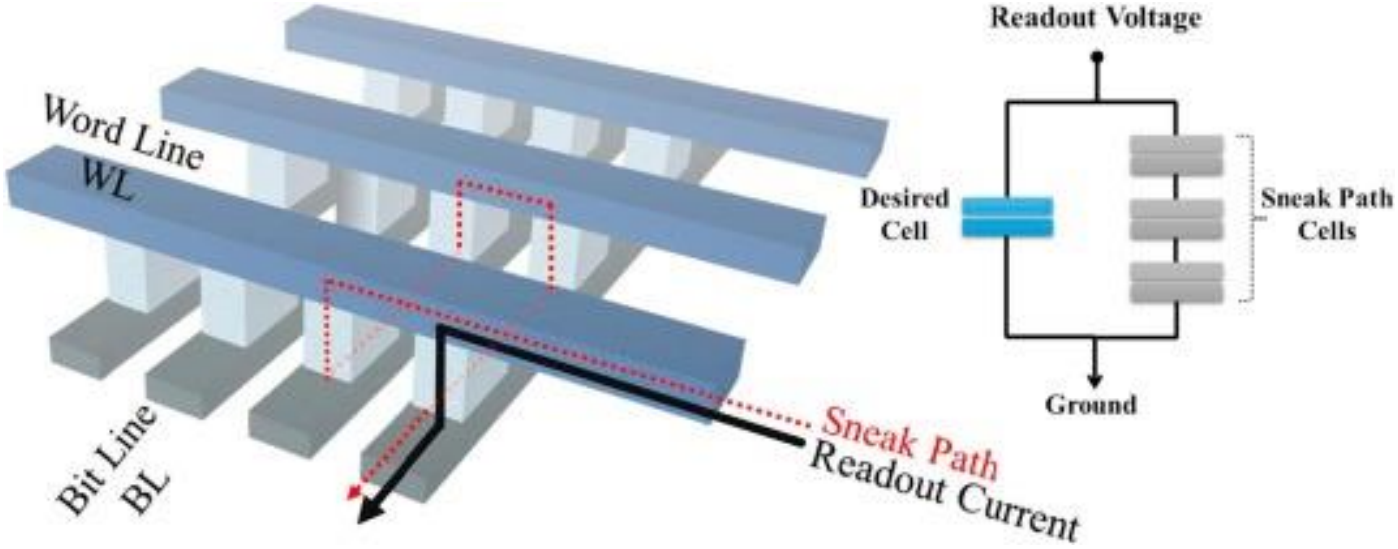
	Ground unsel.	V/3 scheme	V/2 scheme
V	V_{dd}	V_{dd}	V_{dd}
V_r	0	$V_{dd}/3$	$V_{dd}/2$
V_c	0	$2V_{dd}/3$	$V_{dd}/2$

Chen TED 2013

Current sink

- What happens to the current as it goes towards the “last” device?

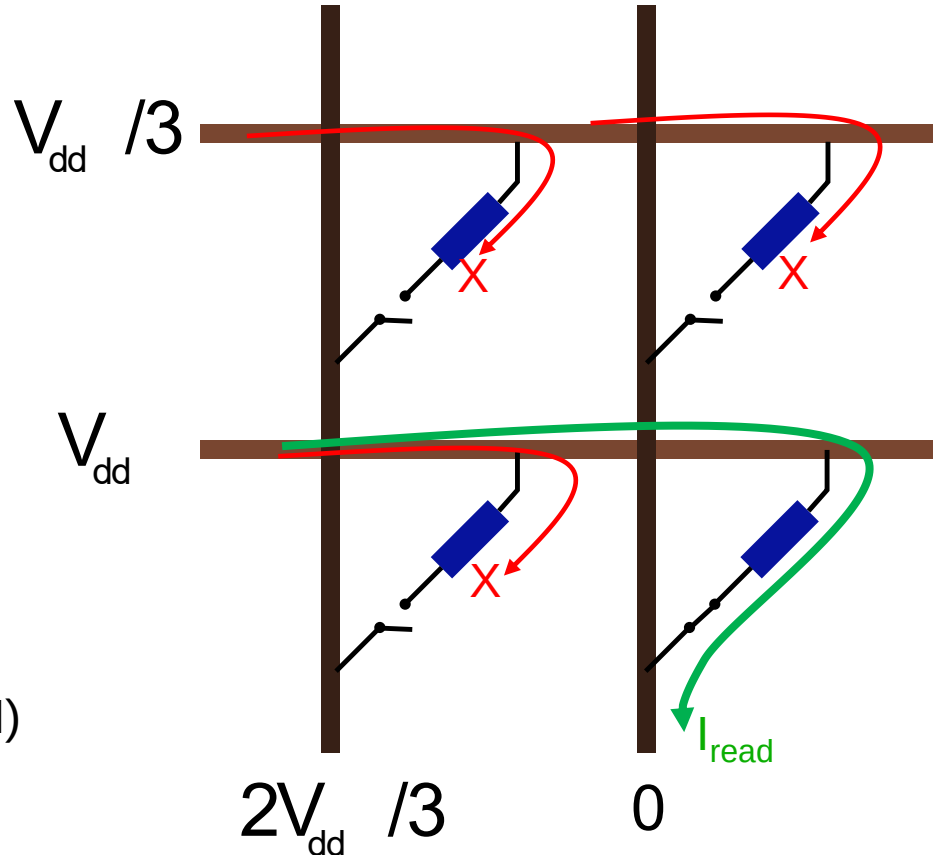




The Selector device

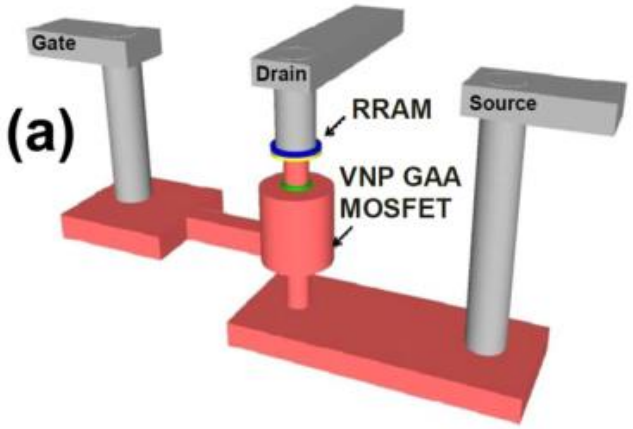
- Purpose: To cut of leakage paths through unselected memory devices
- A switch - Implementation should be compact and efficient

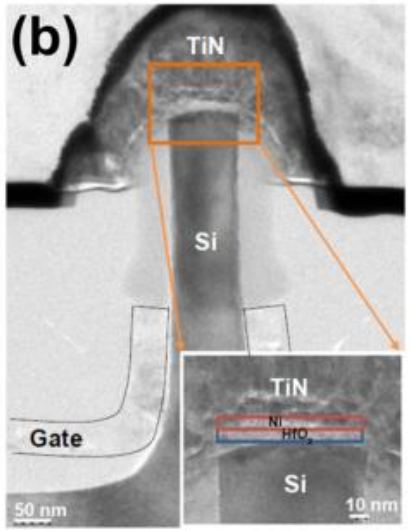
- Ideas:
  - Transistor:
    - Good switch
    - Third terminal
    - Footprint
  - Diode:
    - high currents at high V
    - Very low currrents at low V
    - only for unipolar memories (PCM, some RRAM)

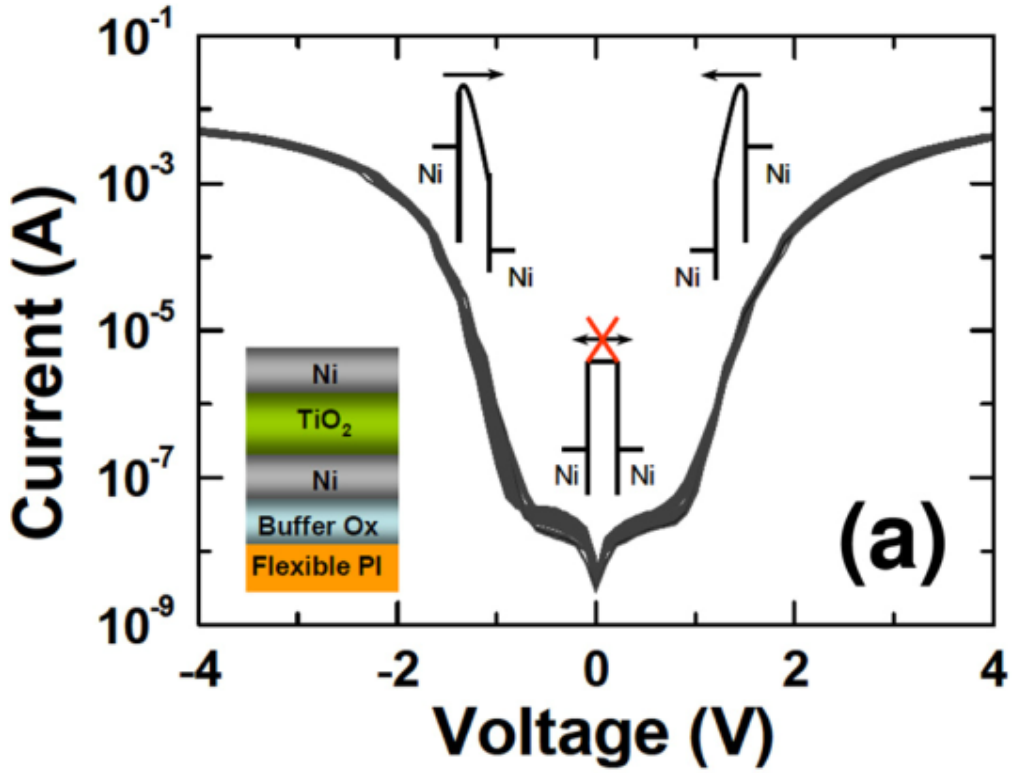


Examples of selector devices

- **Requirements**: High nonlinearity (10^6), high current density (10s MA/cm^2), (bipolar)
- Vertical Transistors → Excellent performance, 3-terminal → complexity, not easy in BEOL
- Oxide Schottky barriers → limited currents, bidirectional





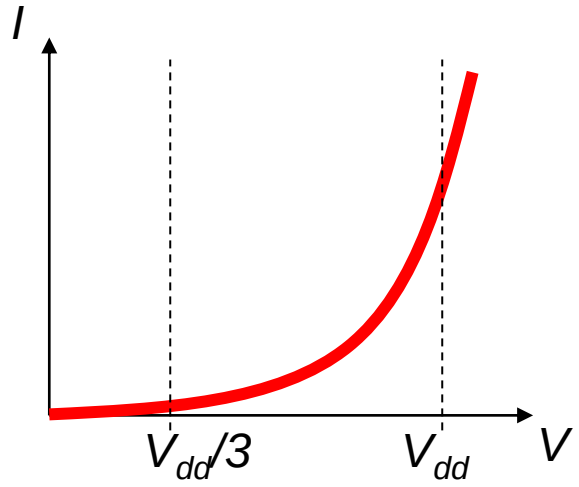


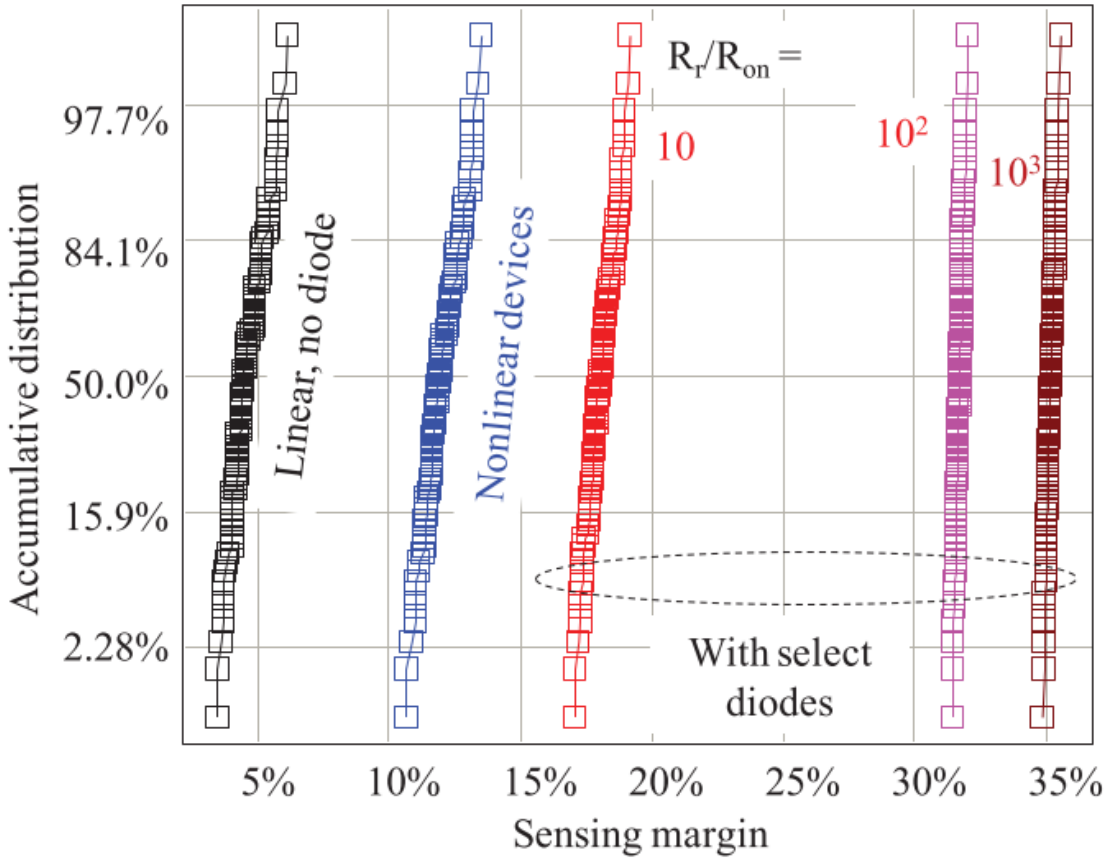
Nonlinear memory devices

- Nonlinearity decreases leakage through unselected devices
- Unselected devices have lower bias → higher R

- $\eta = R(0)/R(V_{dd})$: nonlinearity factor

- Parabolic nonlinearity: ReRAM, PCM ($\eta \sim 10 - 100$)
- Exponential: MRAM, FTJ ($\eta > 1000$)

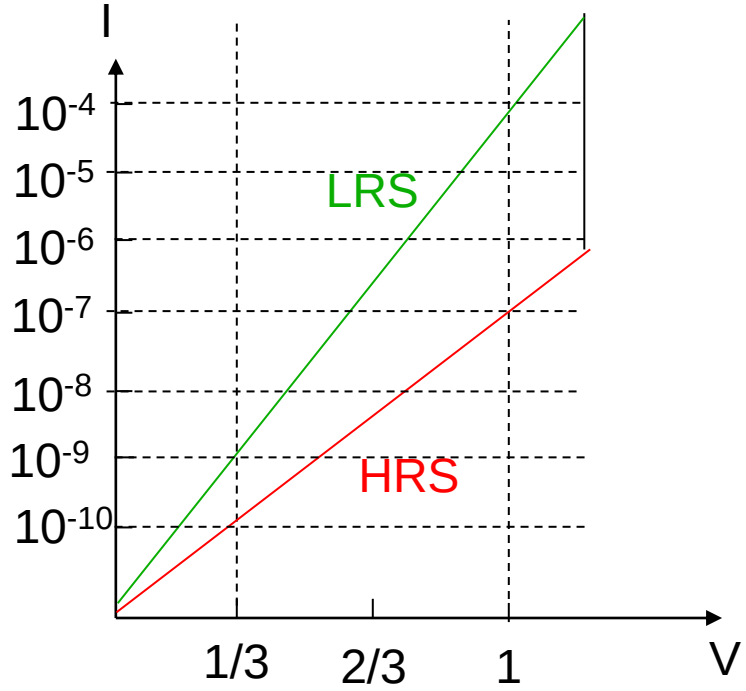




Chen IEEE Trans. Electron. Dev. 2013

Exercise – Selector-less device

A FTJ has the following I-V characteristic



A selected device in HRS and half-selected in LRS, V_{dd} = 1 V

Compare the leakage current through the half-selected device ($V_{dd}/3$) to the current through the current through the selected device (V_{dd})

A: $\frac{I_{sel}}{I_{leak}} = 1$

B: $\frac{I_{sel}}{I_{leak}} = 100$

C: $\frac{I_{sel}}{I_{leak}} = 1000$

D: $\frac{I_{sel}}{I_{leak}} = 10000$

Is that sufficient for a 1000x1000 memory array?

Go to PollEv.com/mattiasborg110

A B C D

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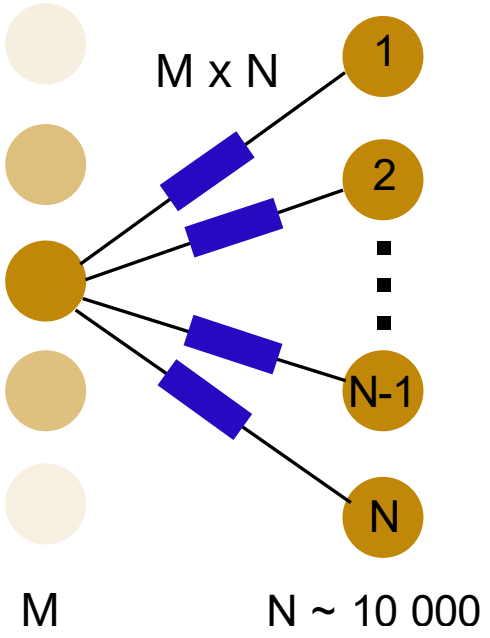
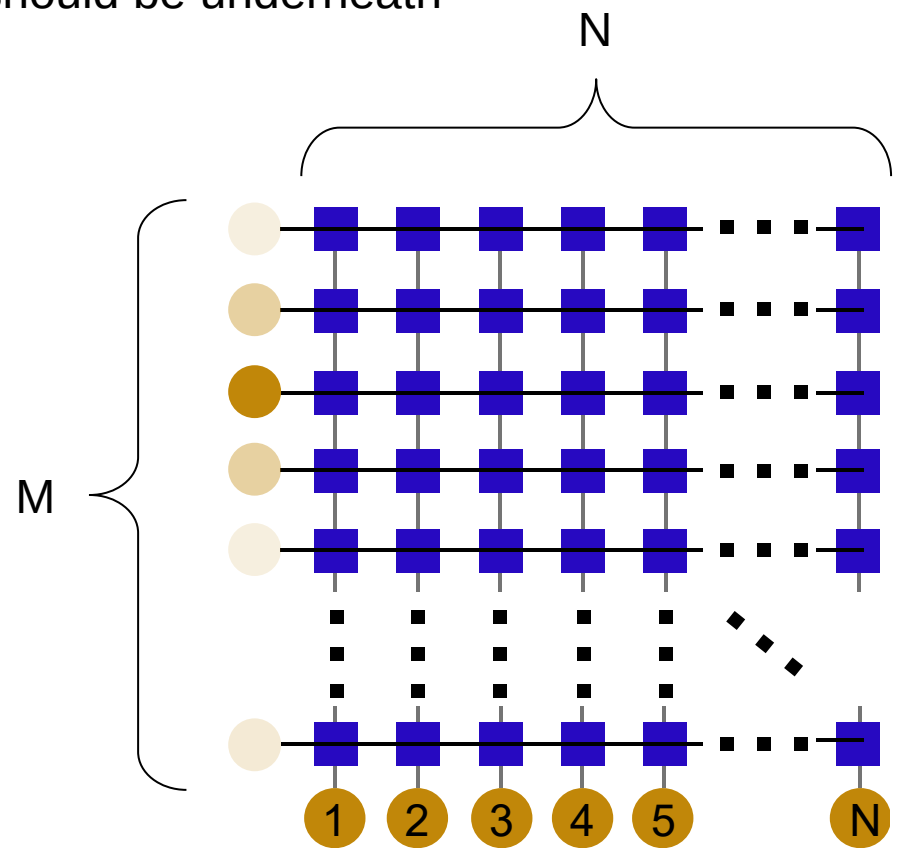
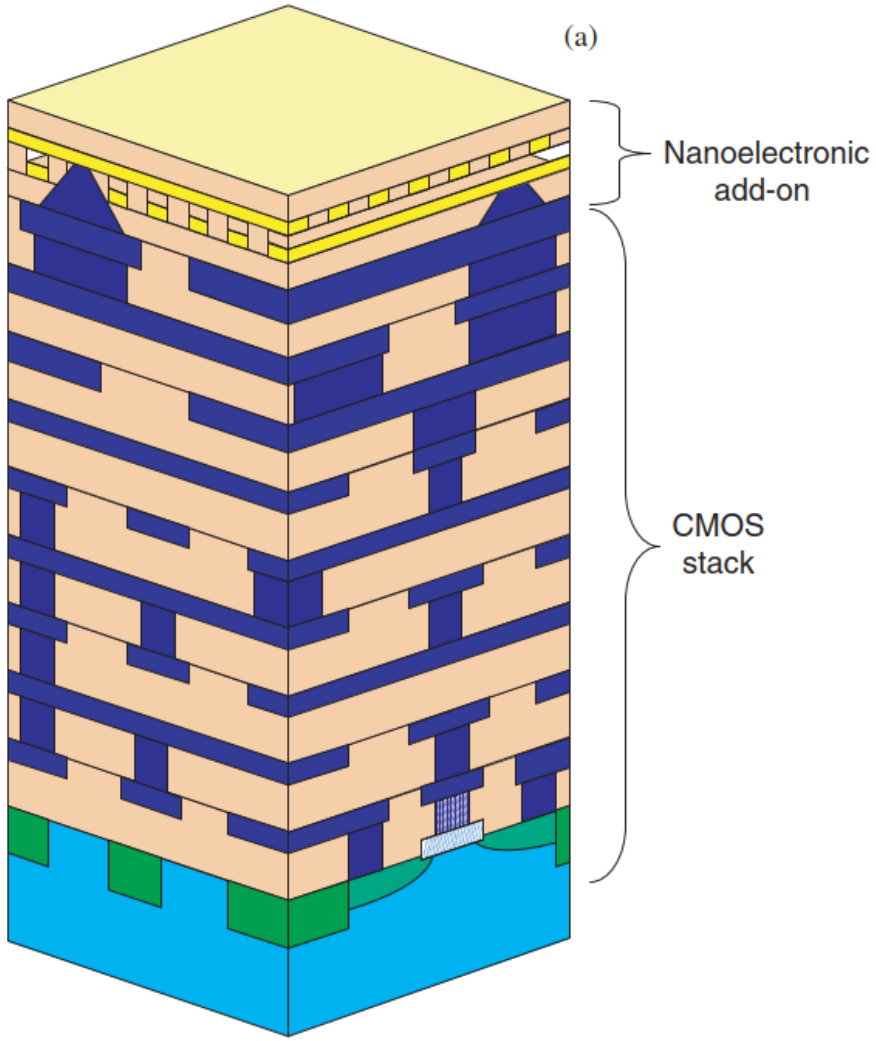
Hybrid Neuromorphic systems

- Synapses in memristor arrays (4-6F^2)
- Neurons in CMOS (>100F^2)
- For density CMOS should be underneath

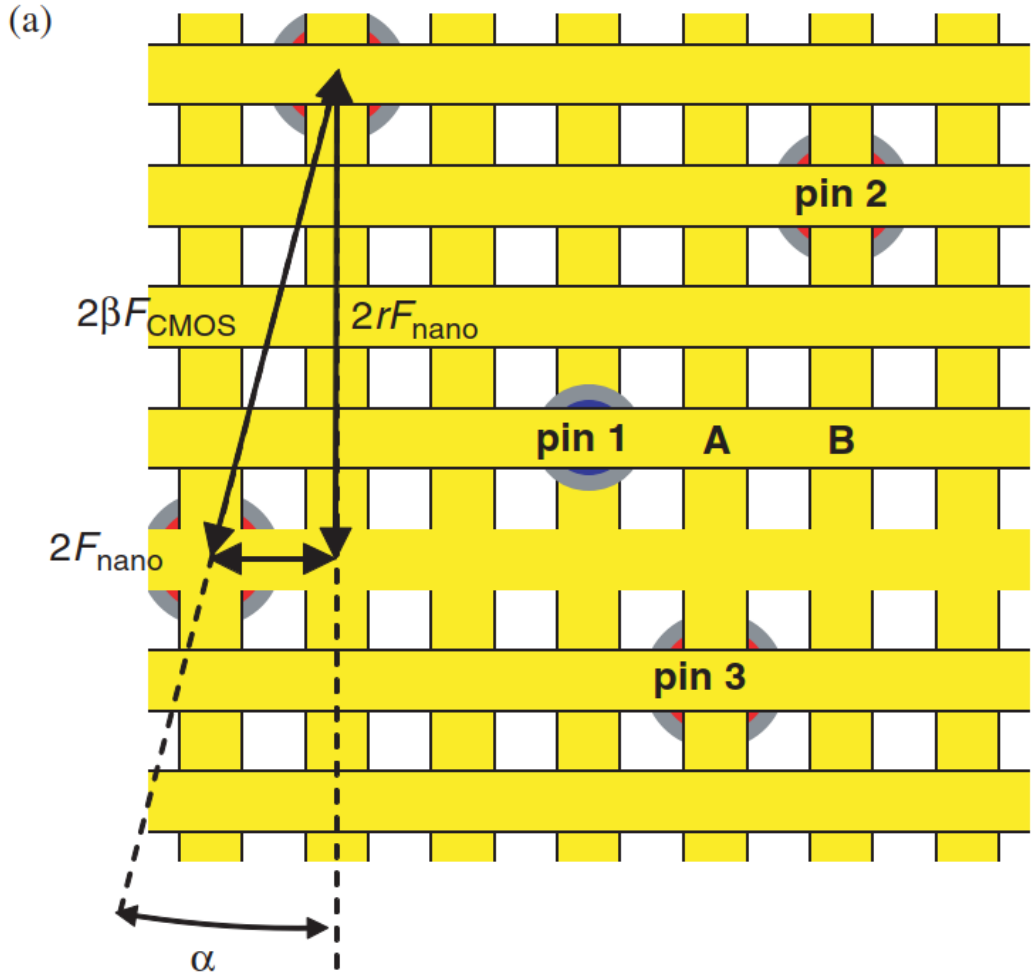


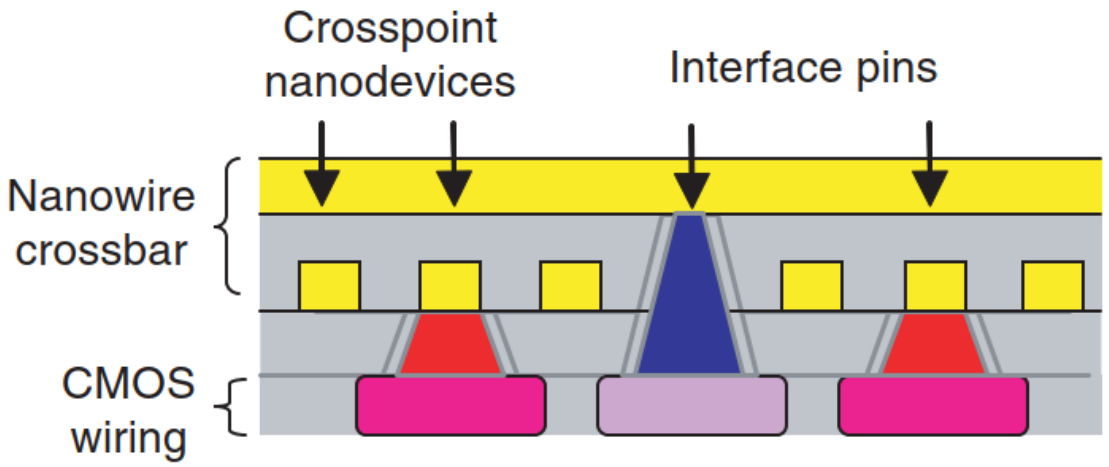




Likharev J. Nanoelectron. Optoelectr. 2008

CrossNet architecture



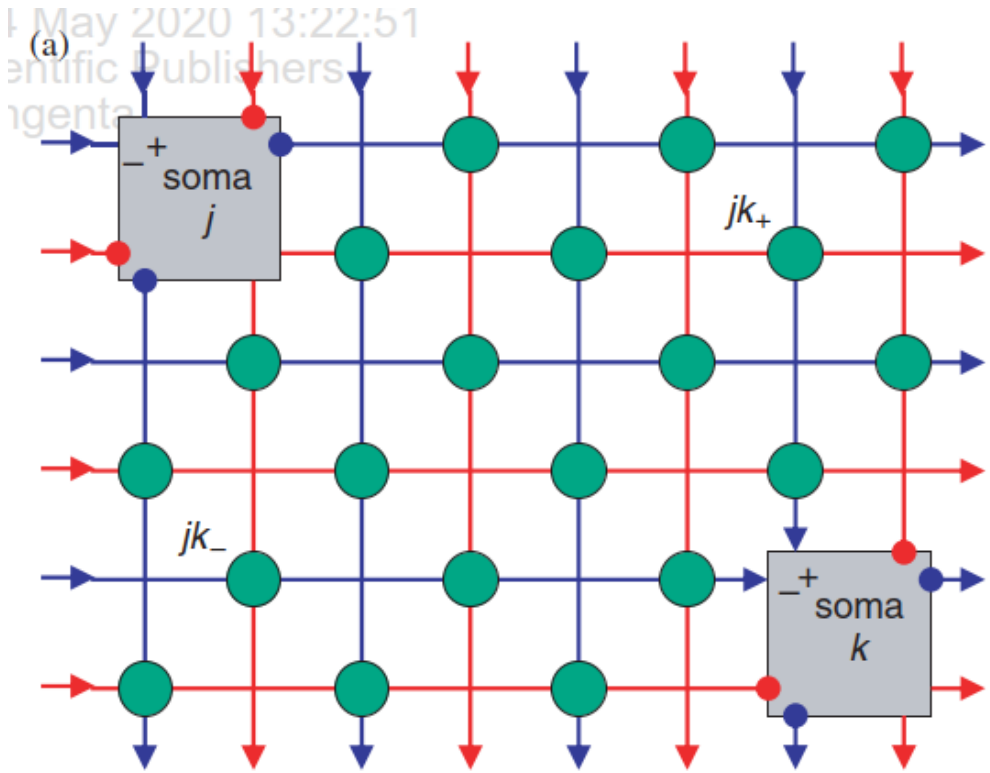


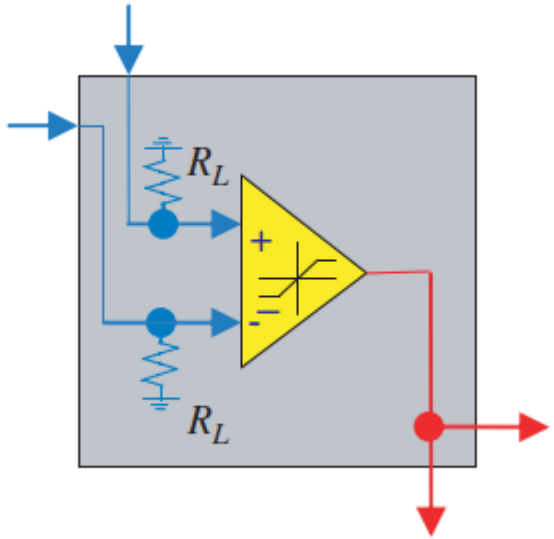
- Memory crossbar above CMOS neuron arrays at $2F_{nano}$ pitch.
- Interface pin network in two heights
  - Pitch: $2\beta F_{CMOS}$
  - Offset angle: $\alpha = \text{asin}\left(\frac{F_{nano}}{\beta F_{CMOS}}\right)$
  - $\beta > 1$, depends on size needed for CMOS cell
- Allows for $F_{nano} \ll F_{CMOS}$!!

Likharev J. Nanoelectron. Optoelectr. 2008

Neural nets in CrossNet topology

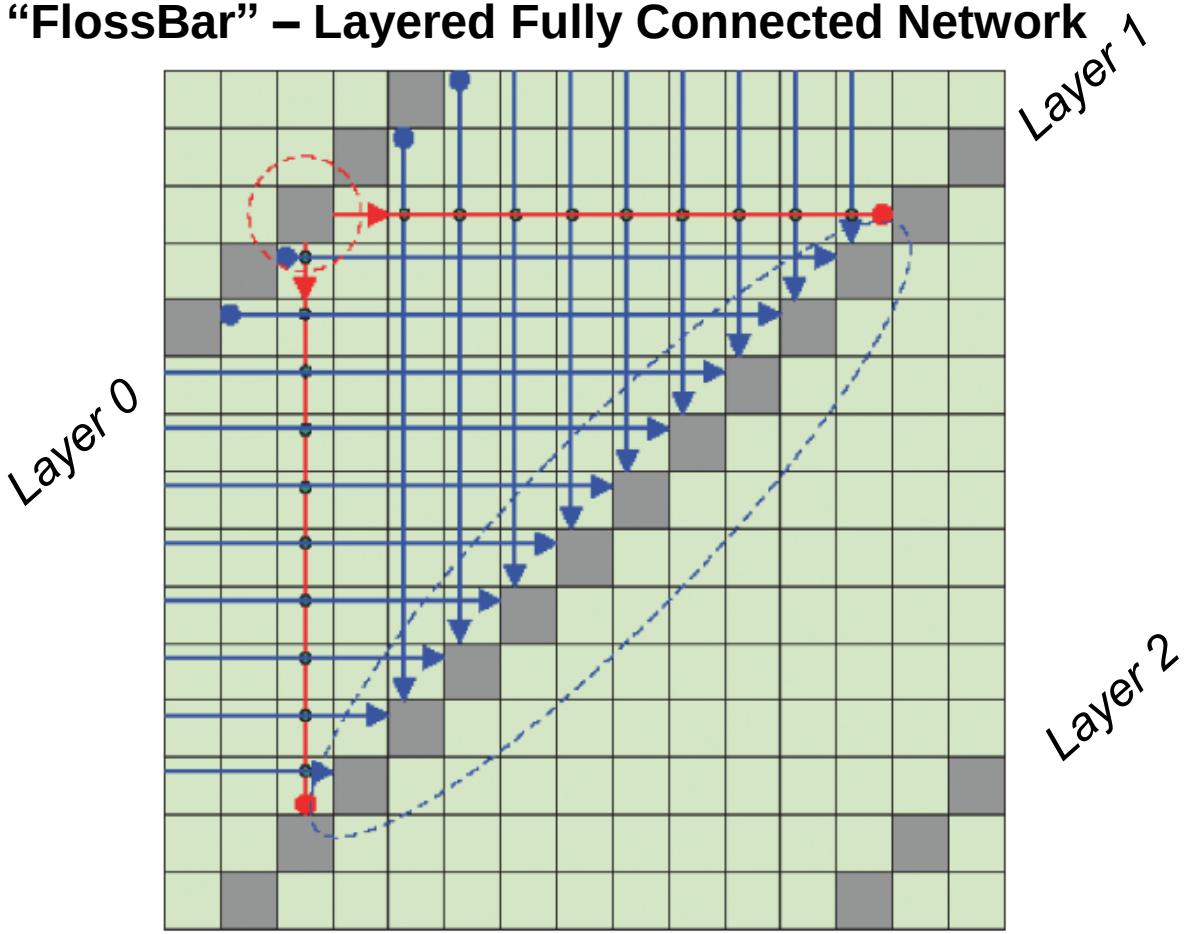
- Connectivity can be arbitrarily defined by distance between CMOS neurons



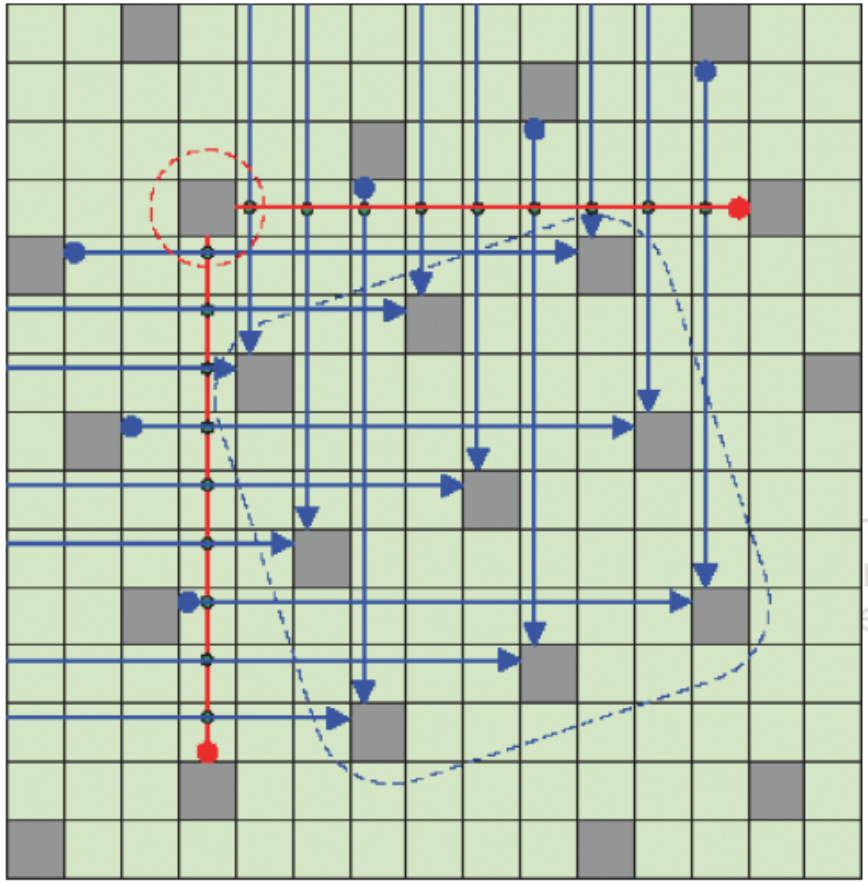


Neural nets in CrossNet topology II

“FlossBar” – Layered Fully Connected Network



“InBar” – Non-layered (N=9) – F_{nano} can be smaller



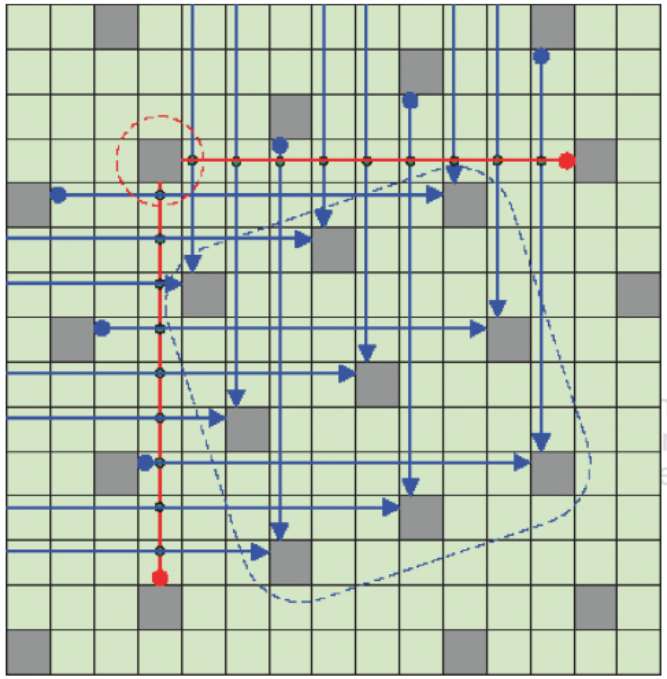
Likharev J. Nanoelectron. Optoelectr. 2008

Exercise – Neural density in CrossNet?

"InBar" topology
F_{nano} = 10 nm
N = 10 000

How many neurons on a 100 mm^2 chip?

The human brain has 200 billion…



3 options

A: 100 000
B: 100 million
C: 100 billion

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A B C

Start the presentation to see live content. For screen share software, share the entire screen. Get help at pollev.com/app

Examples of existing neuromorphic hardware

SpiNNaker (Uni Manchester)
v1 in 2009

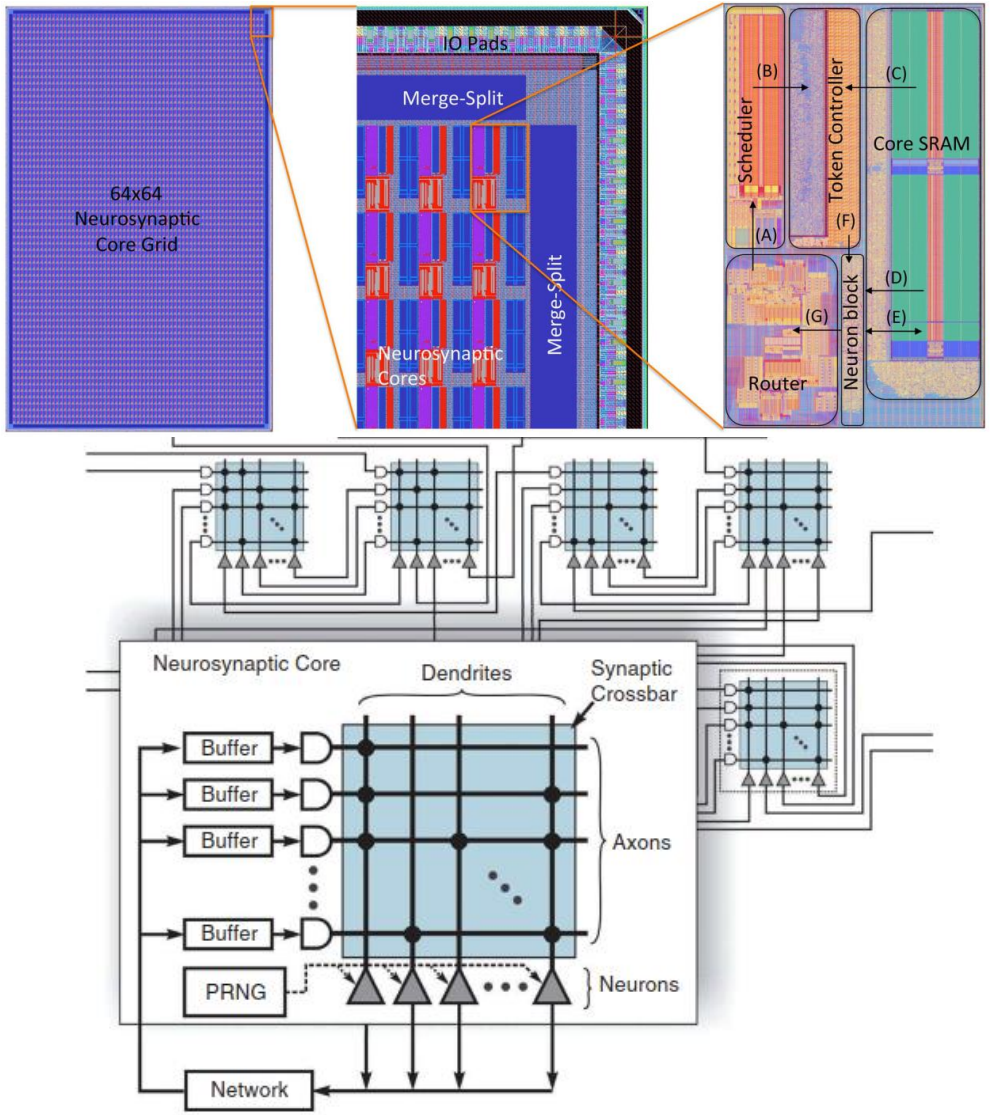
TrueNorth (IBM)
v1 in 2015

Loihi (Intel)
v1 in 2018

Other chips: HICANN (Heidelberg), Neurogrid (Stanford)

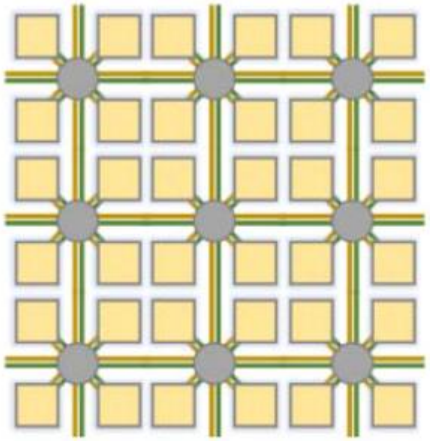
TrueNorth

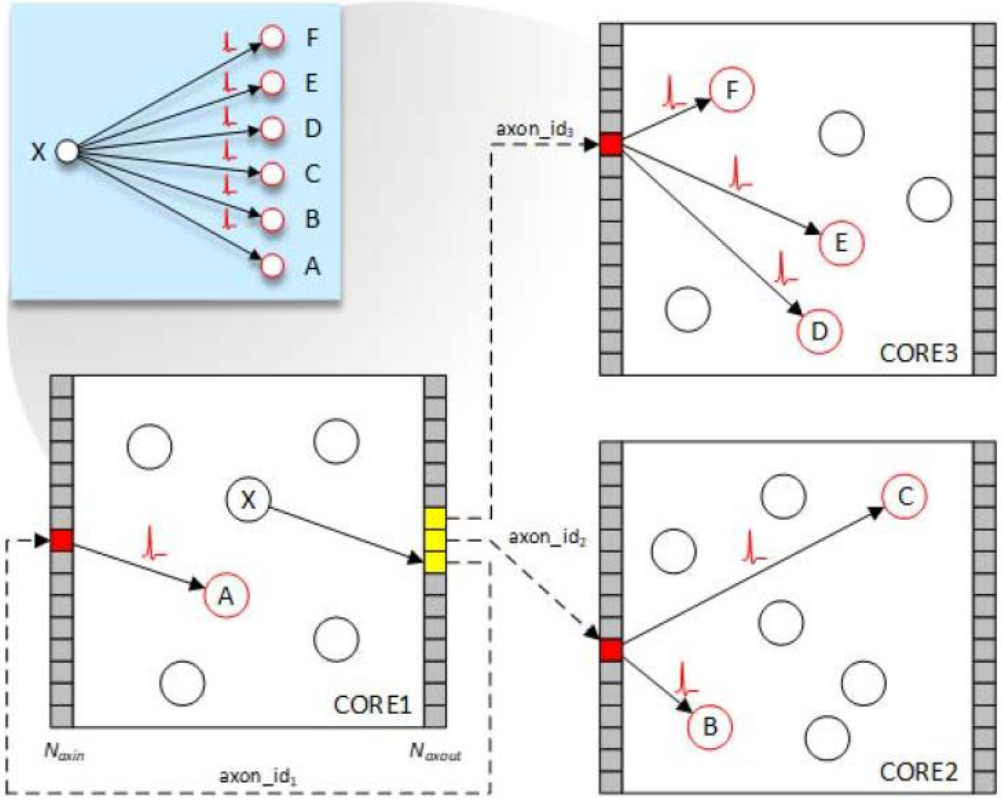
- 4096 neurosynaptic cores á 256x256 synapses
- Digital implementation of Spiking Neural Network
  - Digital LIF Neurons
- Mixed asynchronous-synchronous design
  - Asynchronous event-based connections between cores
  - Collects spikes in each core input
  - After global “ticks” every 1 ms keep execute core computations and send new events
- 80 chip system (80M neurons, 20B synapses @ 20W)



Loihi (Intel)

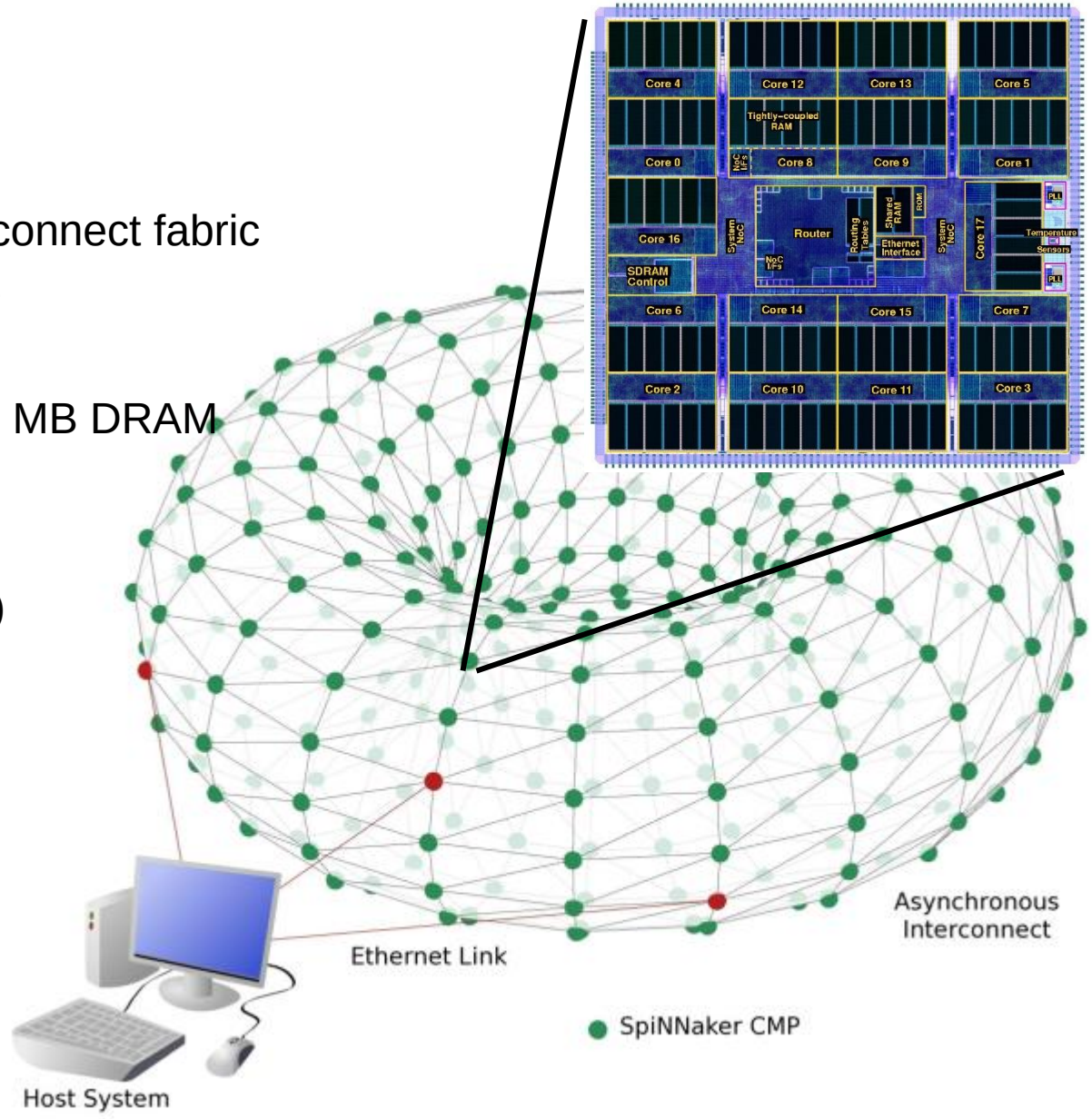
- Fully digital implementation of SNN
- 128 neuromorphic cores (x1024 neurons) connected by Network-on-chip
- Implements LIF Neurons
- Homeostasis, refractoriness, stochasticity, STDP
- SRAM Synapses (1-9 bit)
- Connectivity by network communication, not physical
  - Tricks to handle N ~ 10 000
- Each time step
  - Integrate neuronal input messages, update potential
  - Neurons that should fire sends messages to corresponding cores
  - Cores send barrier messages to synchronize before next time step



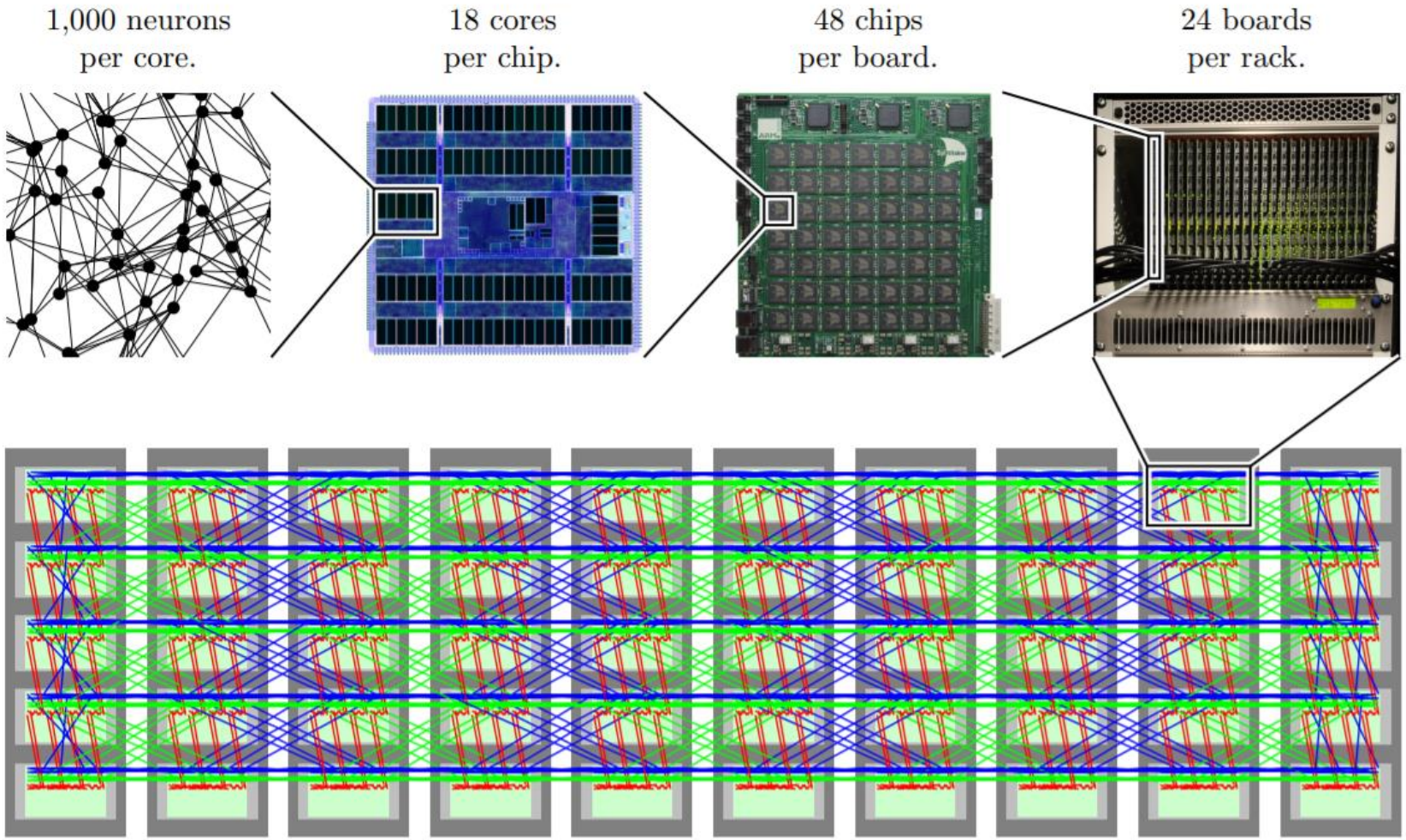


SpiNNaker

- Array of ARM9 cores communicating on custom interconnect fabric
  - 1000 neurons and their connections in each core
  - Same principle as Loihi
- 57K chips, Each 102 mm^2 chip with 18 cores and 128 MB DRAM
- >1 M ARM cores, 7 TB (!) RAM
- Part of EU Human Brian Project
- Designed to be connected together (up to 65K nodes)
  - Now at > 1M ARM cores
  - SpiNNaker2 in 2023



Scaling SpiNNaker to a billion neurons



100 kW power!

Benchmarking

	SpiNNaker	TrueNorth	Loihi
Model	Digital	SNN, digital	SNN, digital
Chip area mm^2	102	430	60
Process tech	UMC 130 nm	Samsung 28 nm	Intel 14 nm
Neurons / chip	18K	1M	131K
Synapses / chip	18M	256M	120M
Power / chip (mW)	1000	100	100
Release year	2011	2014	2018

Summary

- Line resistance + current drop limits memory array size
- Large scale memory arrays require non-linearity to avoid leakage
- Selector devices : non-linear ($\eta > 10^6$), bidirectional, high current density
- Non-linear memory devices can avoid selectors

- CrossNets, a promising approach to high-density hybrid neuromorphic systems
  - High density synapses on top
  - CMOS neurons underneath

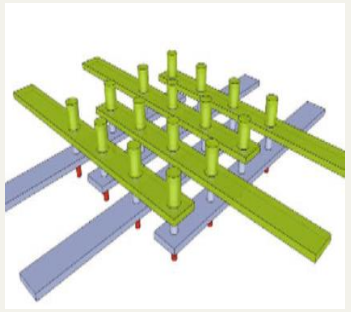
- Neuromorphic systems available with < 100 mW power consumption
  - CMOS based
- Still no full-scale memristor-based neuromorphic system on market

Exam information

- Online Written Exam
- June 4th 2.00pm – 18.00pm
- https://lu-se.zoom.us/j/66625232949?pwd=Q1I4MFJmdXpycW1aSW5JQnAvY2o1QT09
  Meeting code: 666 2523 2949
  Password: 027756
- ID check starts at 1.45pm
- Exam is visually monitored (need camera on at all times)
  - >5 min downtime
- Oral follow-up exam in case of suspicious behaviour
- Solutions to be scanned and uploaded to Canvas before 6.10pm
- **Allowed aids for the exam:**
  - Writing aids – e.g. Pen, paper, ruler, etc..
  - Calculator
  - Printed notes (i.e. your own list of important things to remember), 1 A4 paper (double-sided printing is ok)
- Computer or similar for displaying the exam questions, but not for anything else.

Master project openings

Investigating ITO electrode properties for low-power self-compliant RRAMs



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Optimization of Ferroelectric Tunnel Junctions

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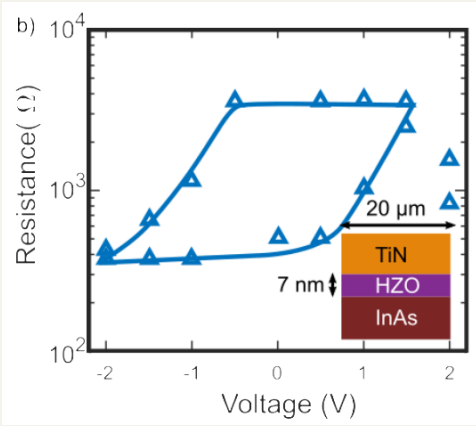
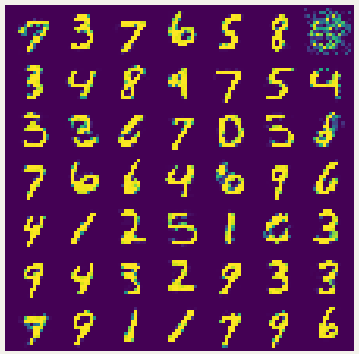


Performance of binary ferroelectric synapses in Spiking neural networks



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Piezoresponsive Microscopy of ferroelectric devices

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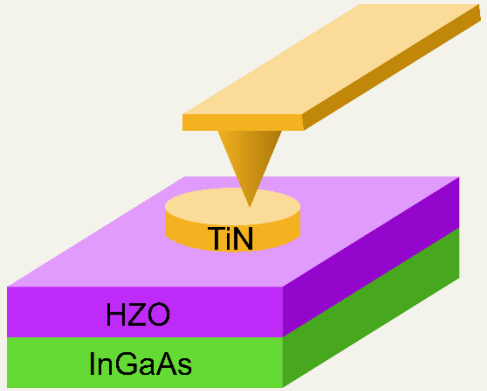

More information on Canvas ("Openings for Master Thesis")