EITP25 2020

Lecture 8 –
Redox resistive memories

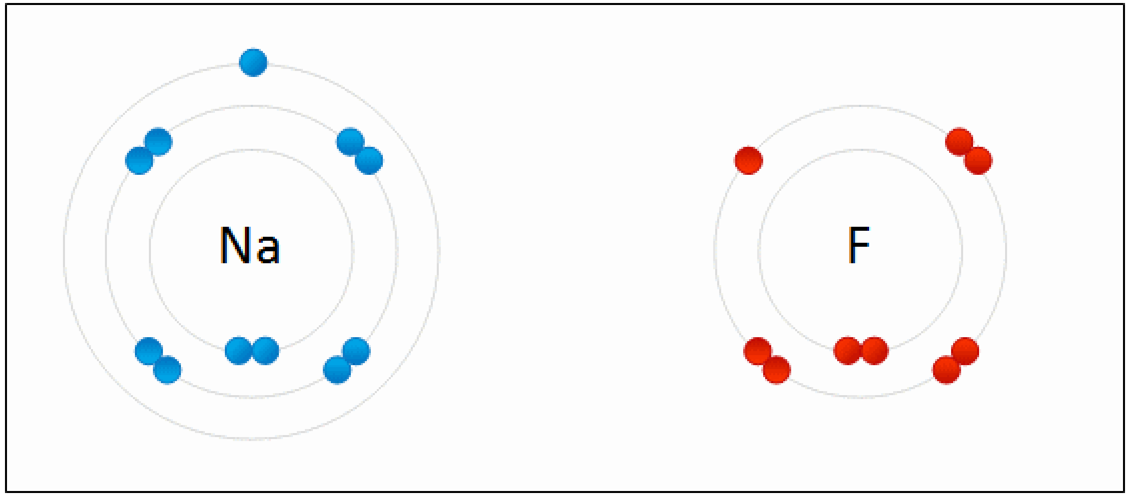
Outline

- Physical description of functionality
  - Electro-chemical metallization
  - Valence-change
- ReRAM as storage
- Multibit operation
- ReRAM synapse devices

This lecture is based on Chapter 8 in *Emerging Nanoelectronic Devices*

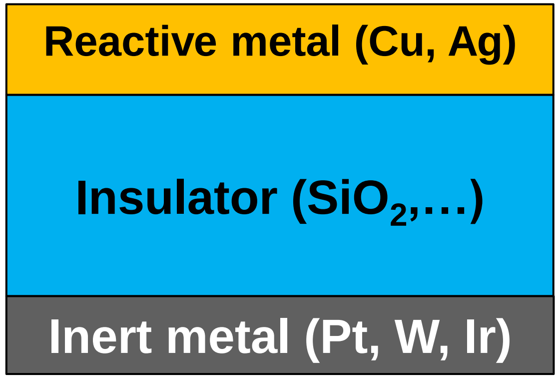
Redox reactions

$$Na + F \rightarrow Na^{+} + F^{-} = NaF(s)$$

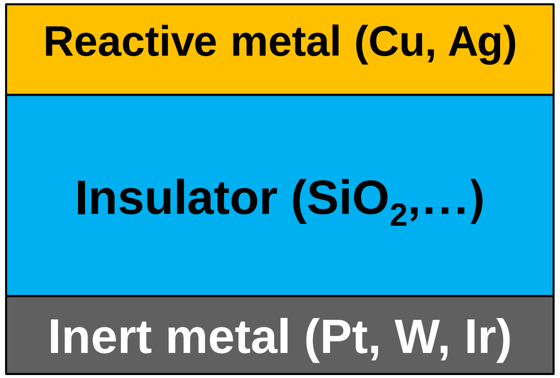


- Reaction in which the oxidation number of atoms is changing
  - Typically by transfer of electrons between atoms
- Oxidation: losing an electron
- Reduction: obtaining extra electron

- <u>In memories two common types:</u>
  - Electrochemical Metallization (ECM)
    - Metal ions diffuse
  - Valence change (VCM)
    - Oxygen ions/vacancies diffuse

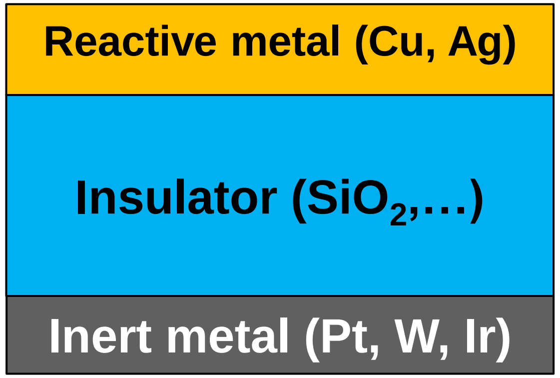


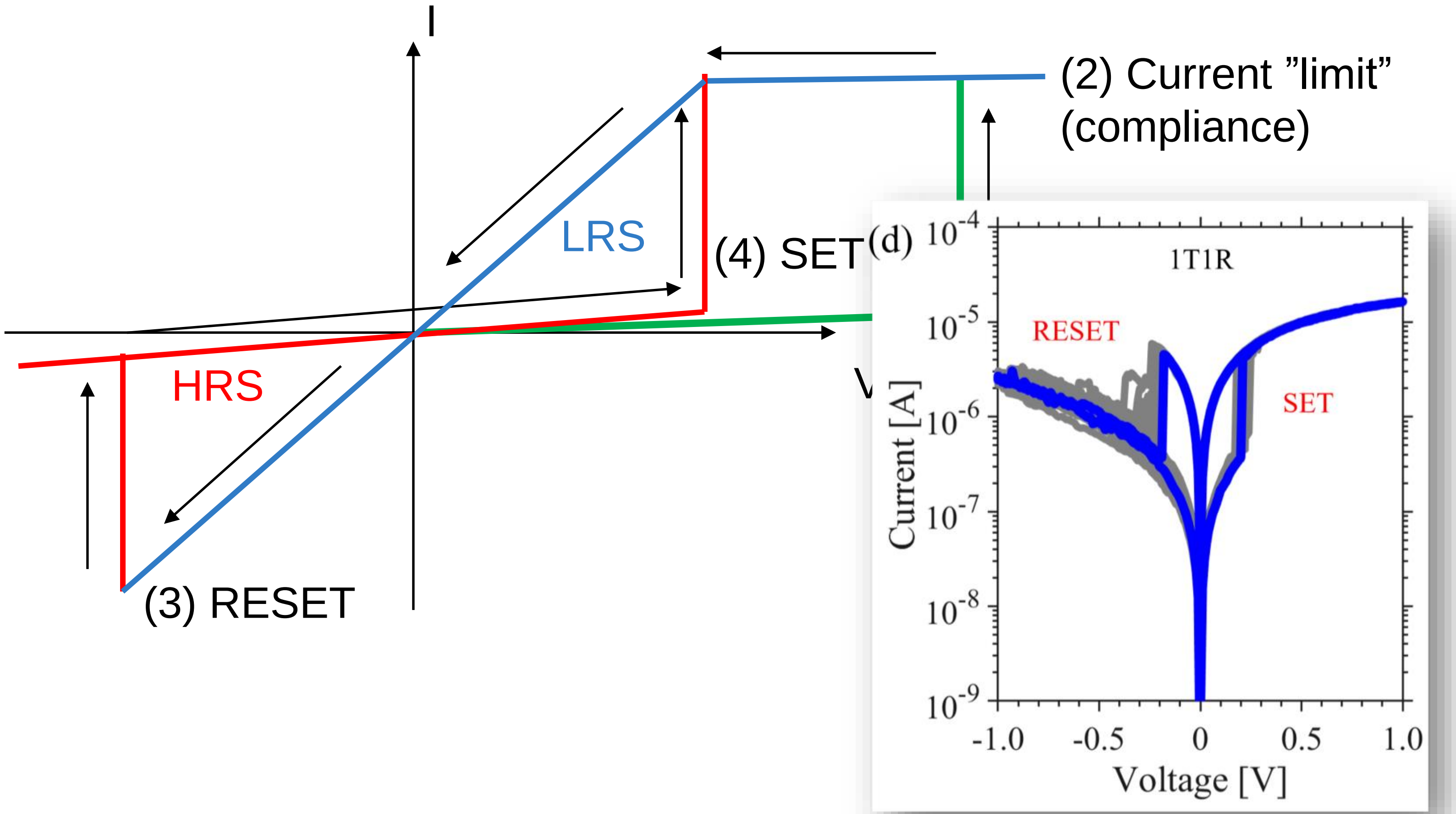
$$Cu \rightarrow Cu^{2+} + 2e^{-}$$



$$XO_2 \rightarrow XO^{+} + O^{-}$$

Operation in brief





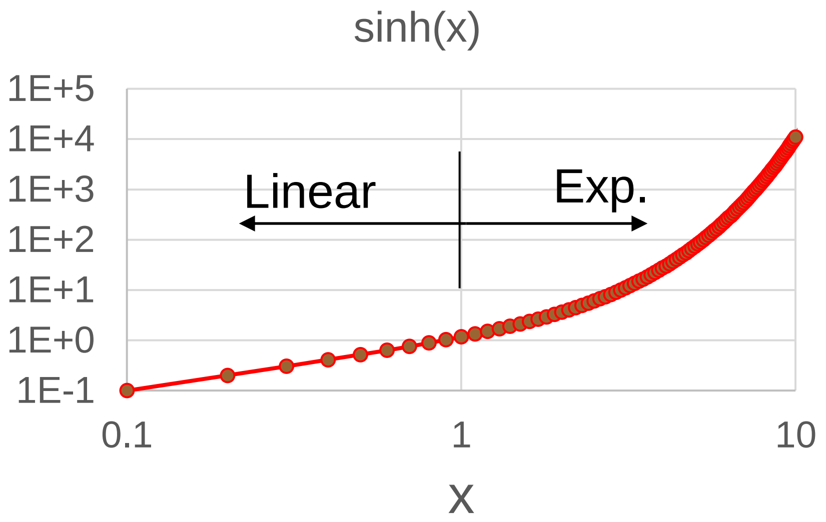
Ionic conduction in Redox memories

$$\sinh(x) = \frac{e^{x} - e^{-x}}{2}$$

- Formation of the conducting path depends on movement of ions

- Mott-Gurney equation of ion hopping:
- $J_{hop} = 2ACf exp\left(-\frac{\Delta E_{hop}}{kT}\right)\sinh\left(\frac{A}{2kT}\mathcal{E}\right)$
  - Linear for $\mathcal{E} < \mathcal{E}_c = \frac{2kT}{A}$
  - Exponential for $\mathcal{E} > \mathcal{E}_c$

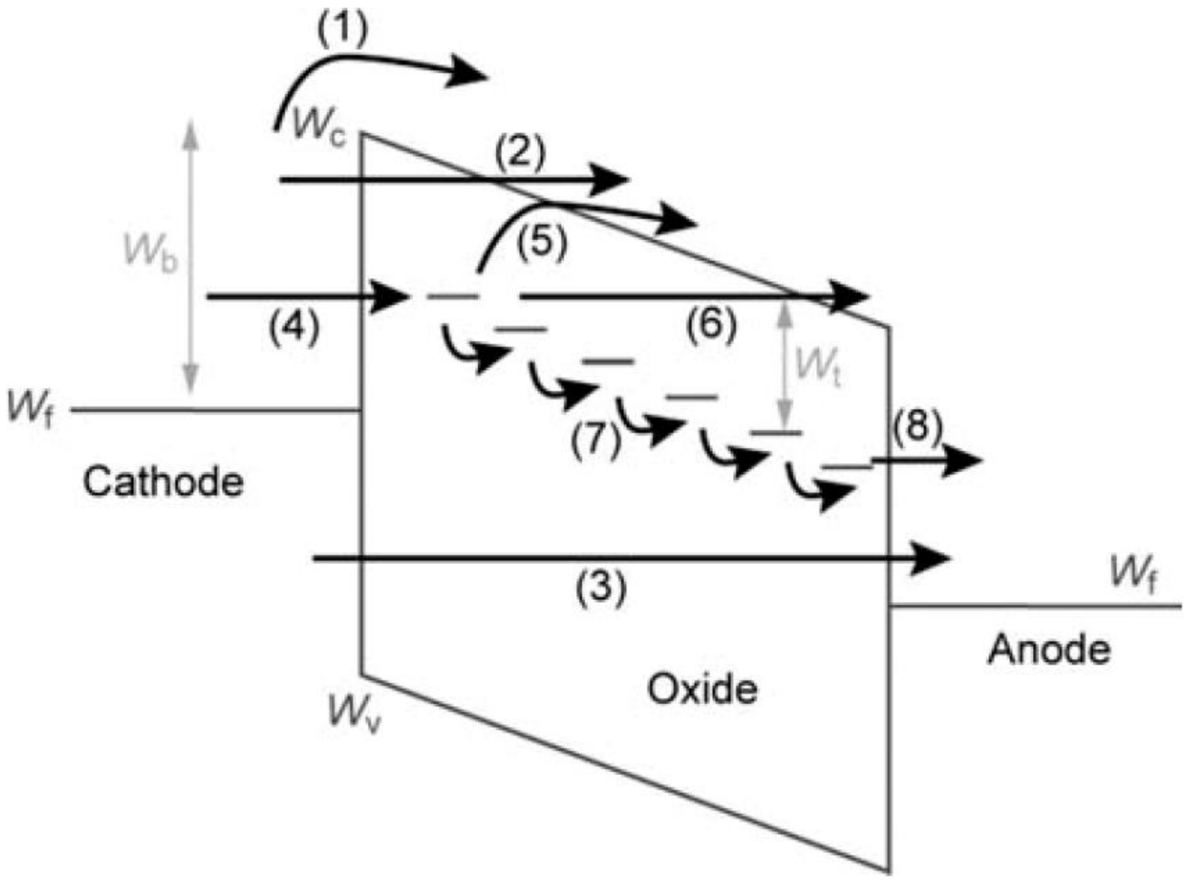
- Results in highly non-linear switching (SET ←→ RESET) behaviour for ReRAM



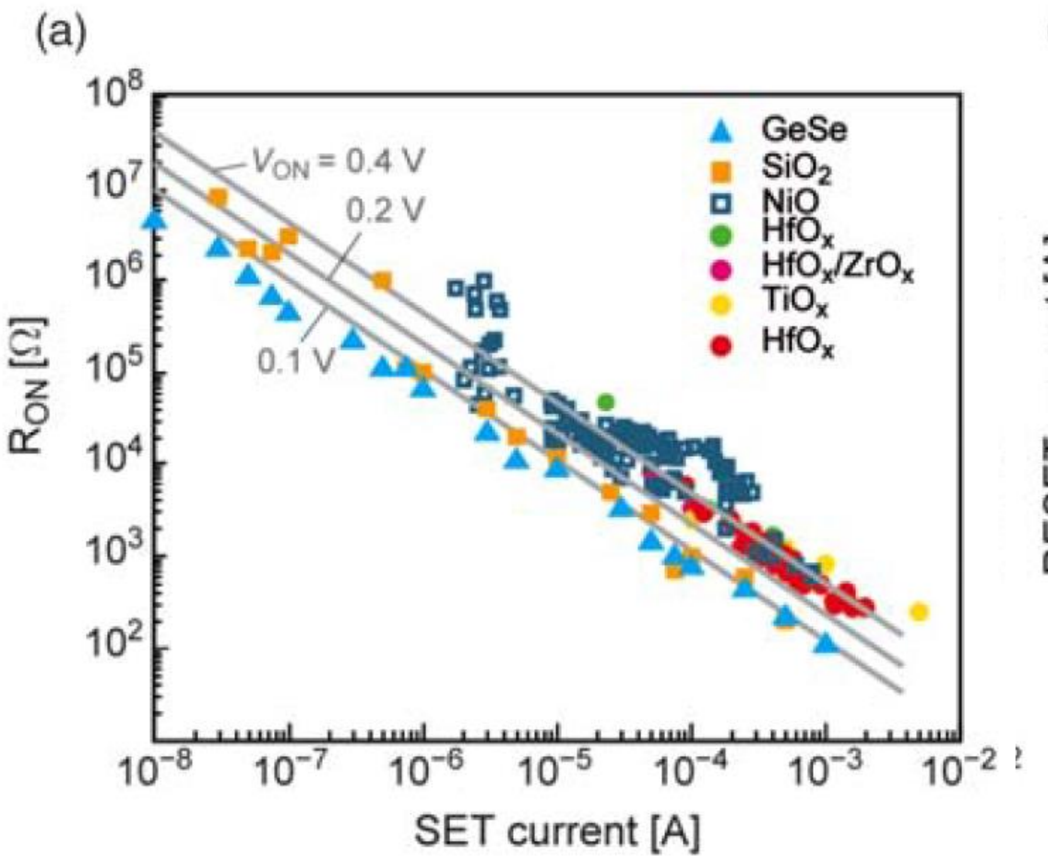
Electronic Conduction in Redox Memories

(1) Thermionic emission
(2) Electron tunnelling to conduction band
(3) Direct tunnelling through stack
(4) Electron injection into trap states

(5) Thermionic emission from trap
(6) Tunnelling from trap to conduction band
(7) Electron hopping
(8) Tunnelling from trap to anode

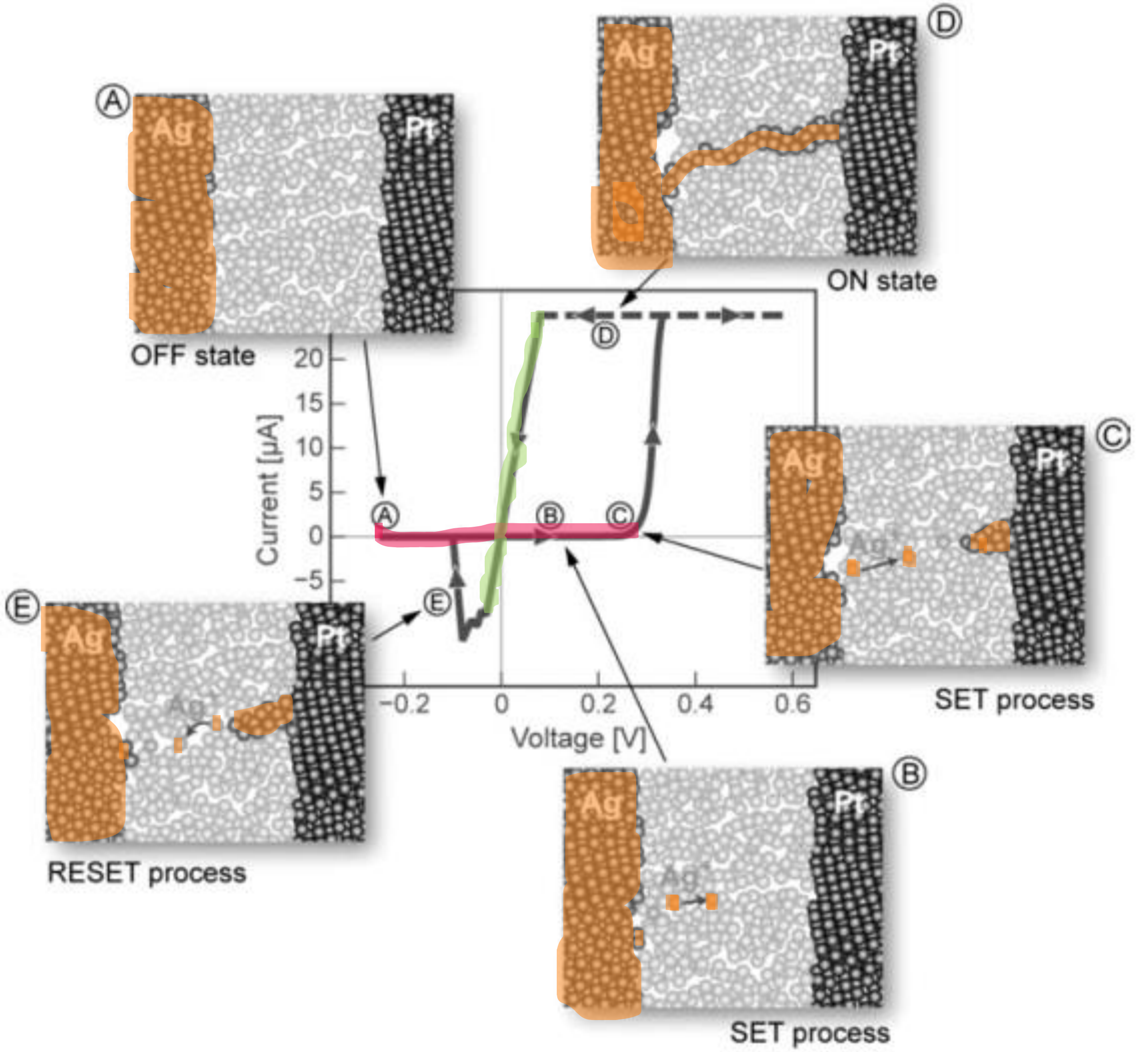


Generic switching properties



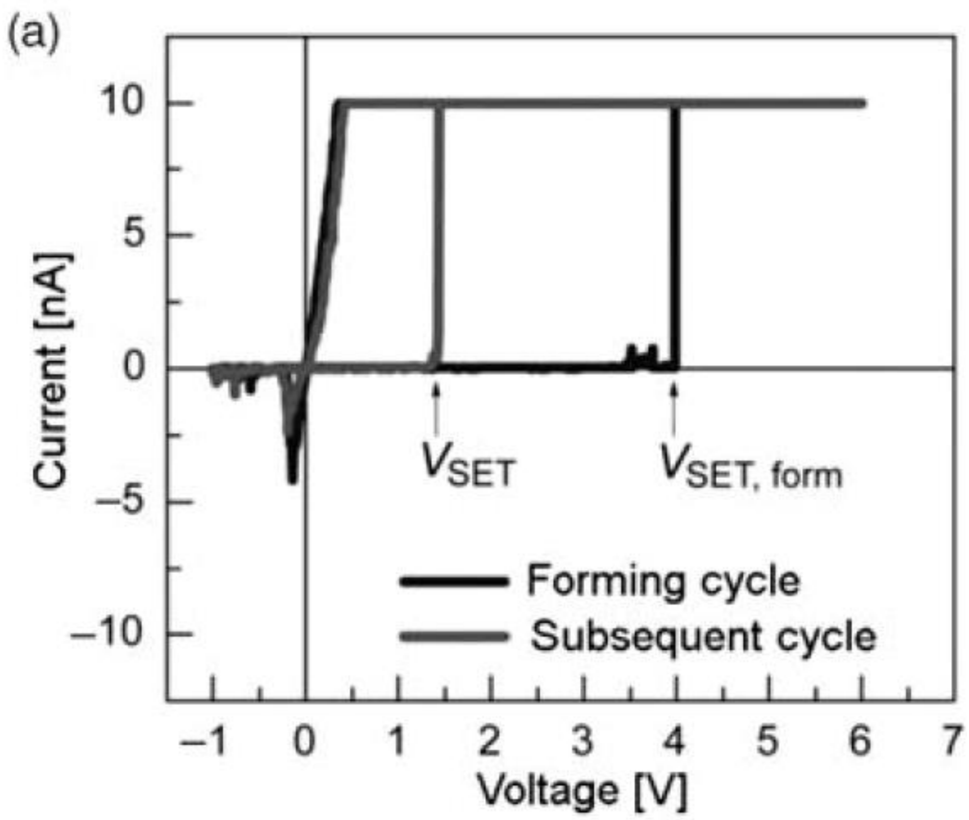
Electrochemical metallization memory (ECM)

- Also called Conductive-Bridge RAM (CBRAM)
- Electric field ionizes cations (Ag, Cu) on reactive contact
- Ions diffuse towards negative (inert) electrode
  → Reduce again to form filament
- Conductive Filament bridge gap → <u>set</u> LRS
- Reverse bias → reverses process <u>reset</u> to HRS



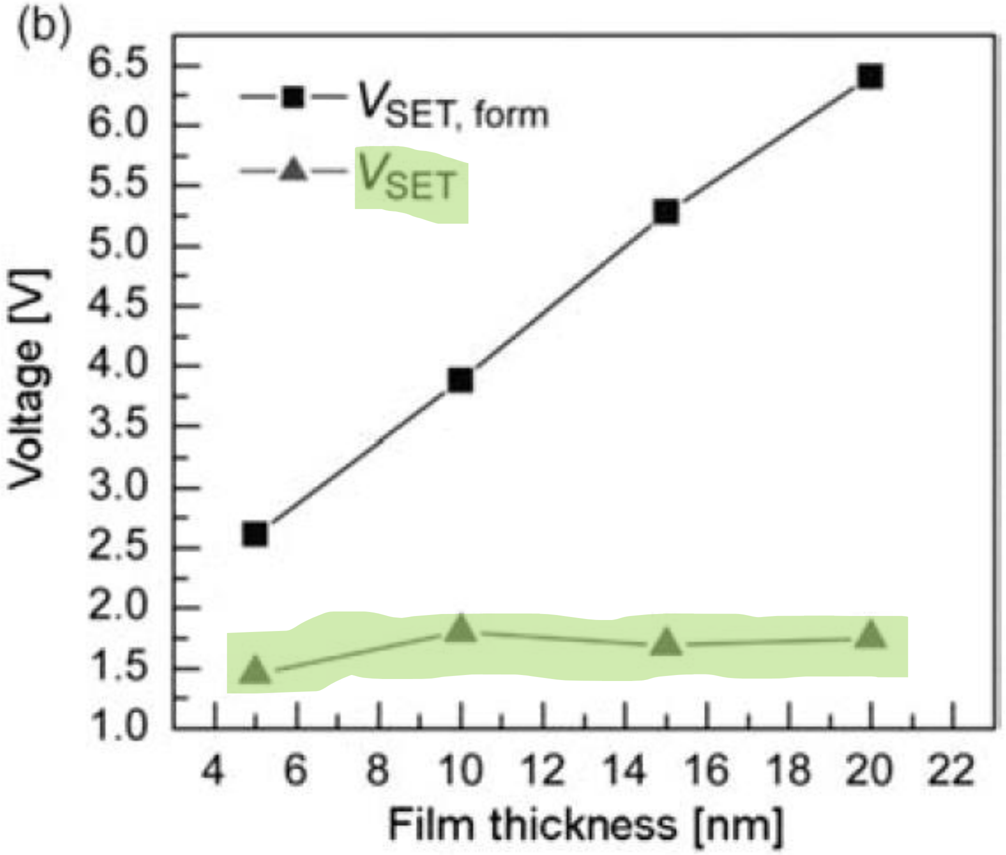
Forming in ECM

- First filament <u>formation</u> is hard (needs high voltage, $V_{SET,\ form}$)
  - Filament growth limits process
  - Formation thickness dependent!
    - Need critical field



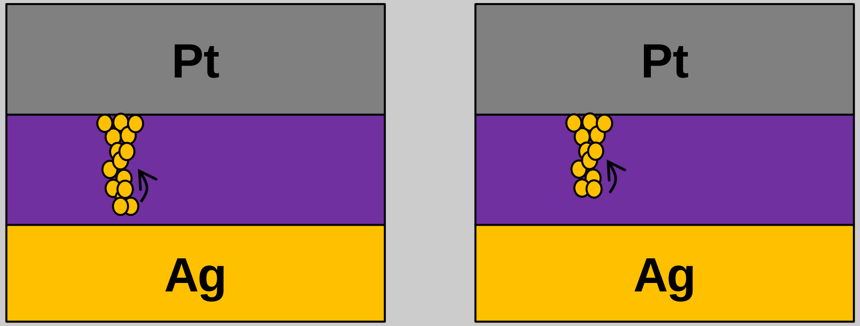
SET in ECM

- LRS decided by compliance level!
- Once formed, an ion channel “template” facilitates filament growth
  - $V_{SET} << V_{SET,form}$
  - NOT thickness dependent!



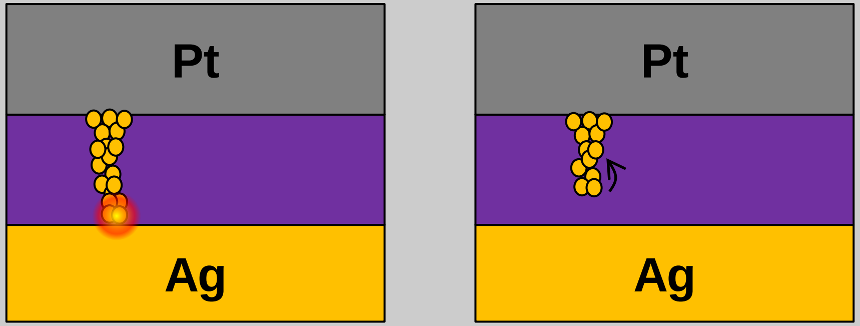
RESET in ECM

Tunneling gap still exists - low compliance



Reverse process to SET
Inherently bipolar…

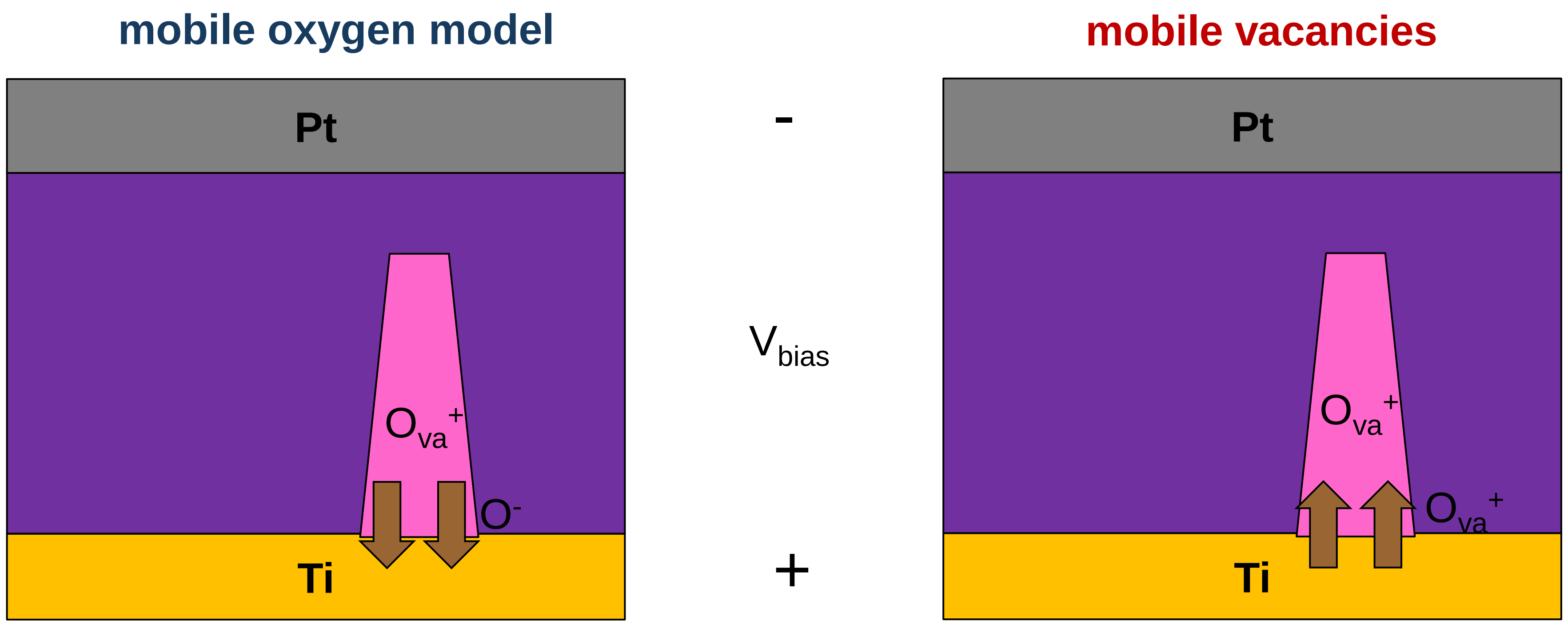
Galvanic contact – high compliance



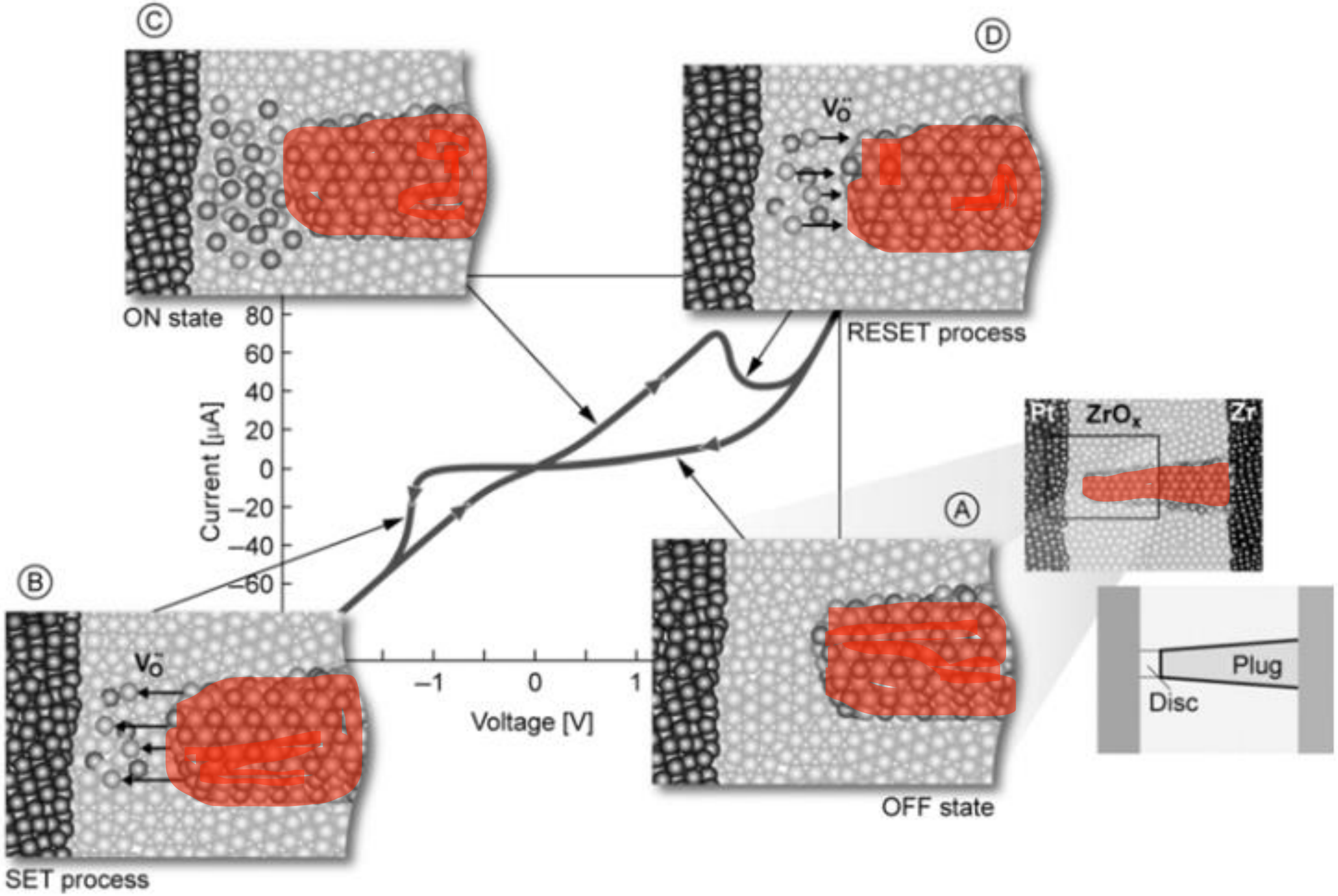
Joule heating at thinnest point
→ ruptures filament
Can be independent of polarity…

Valence change memory (VCM)

- Conductive filament by charged oxygen vacancies in the dielectric layer.
- Typically: Oxide sandwiched between <u>one passive</u> and <u>one reactive</u> electrode
- Two models! Either **mobile oxygen** interstitials/fixed vacancies or **mobile vacancies**

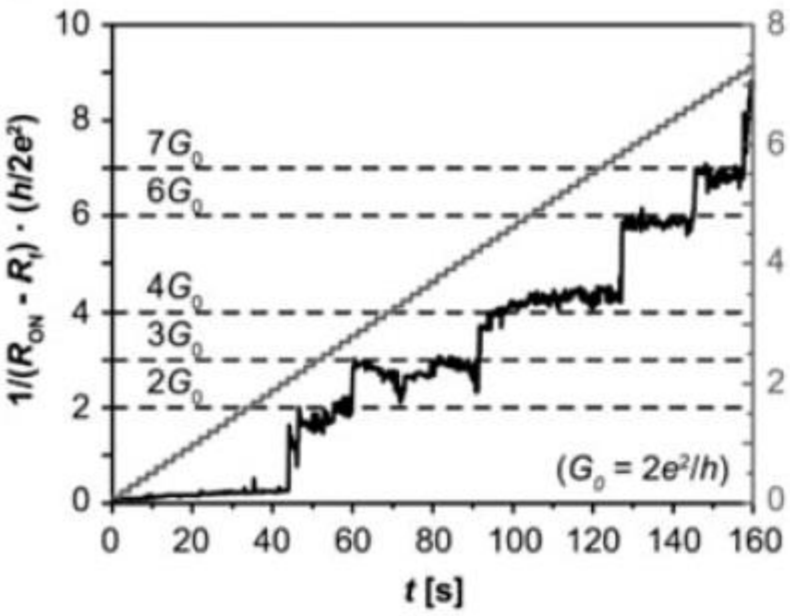


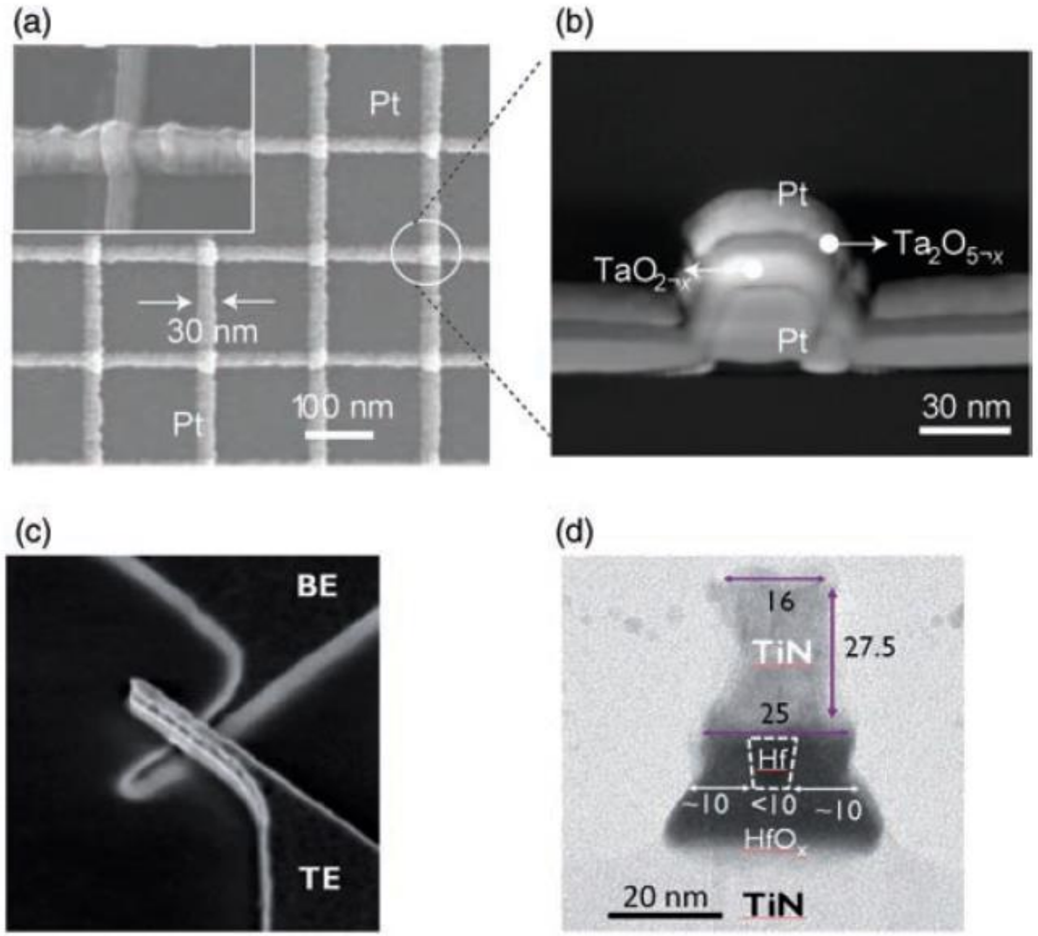
SET/RESET in VCM



Scalability of Redox Memory

- ECM demonstrated with only a few atoms involved (ref 29)
  - Quantized conductance
- VCM down to 10 nm demonstrated





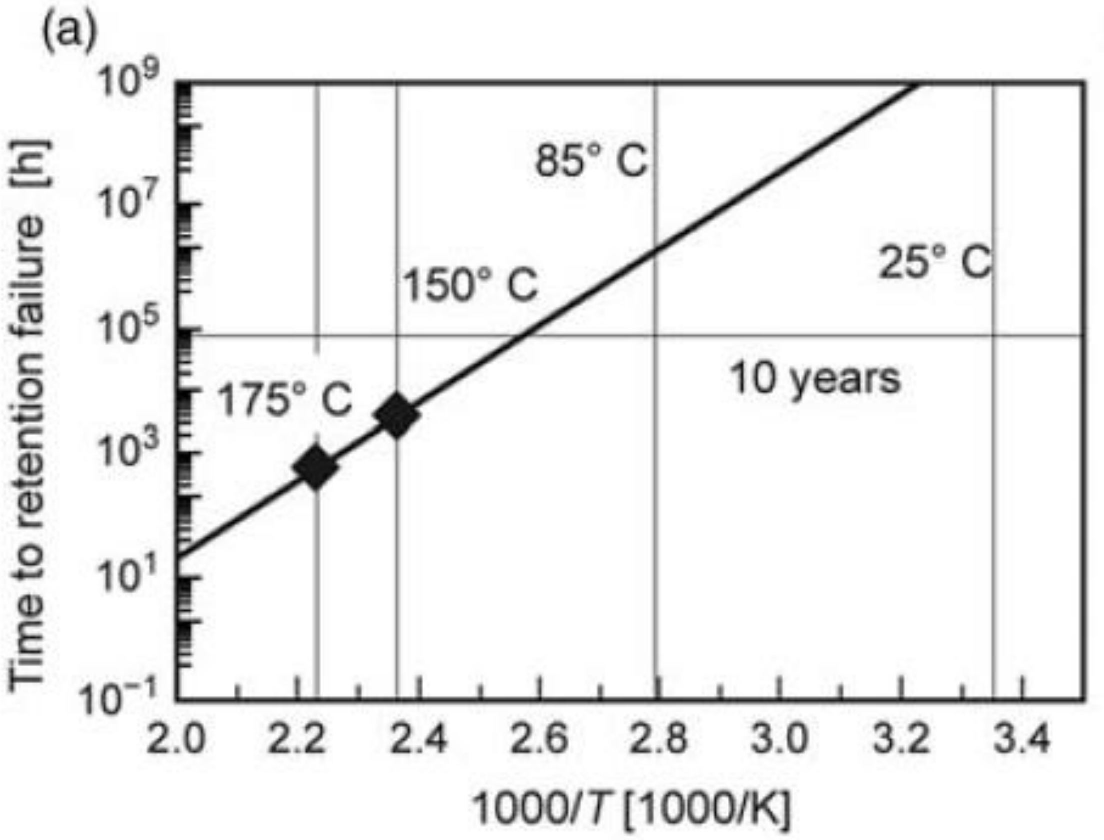
Retention in Redox memories

$$J_{hop} = 2ACf exp\left(-\frac{\Delta E_{hop}}{kT}\right)\sinh\left(\frac{A}{2kT}\mathcal{E}\right)$$

How to estimate

- Measure until failure at elevated temperatures (at least 3 temperatures)
- Extrapolate in time to get time to failure at RT or 85C (standard operating T)

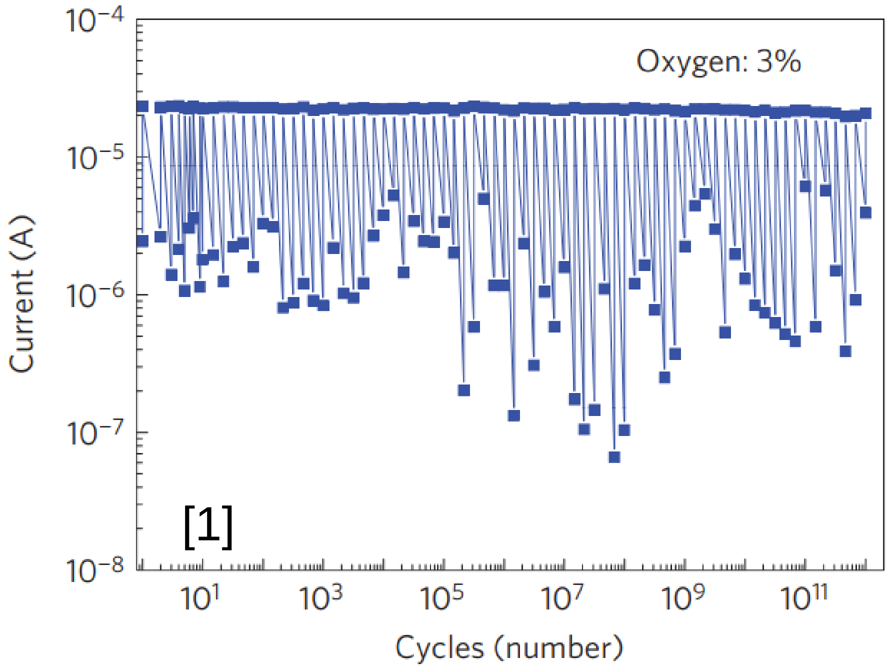
- > 10 years at 85 ˚C observed for both VCM and ECM

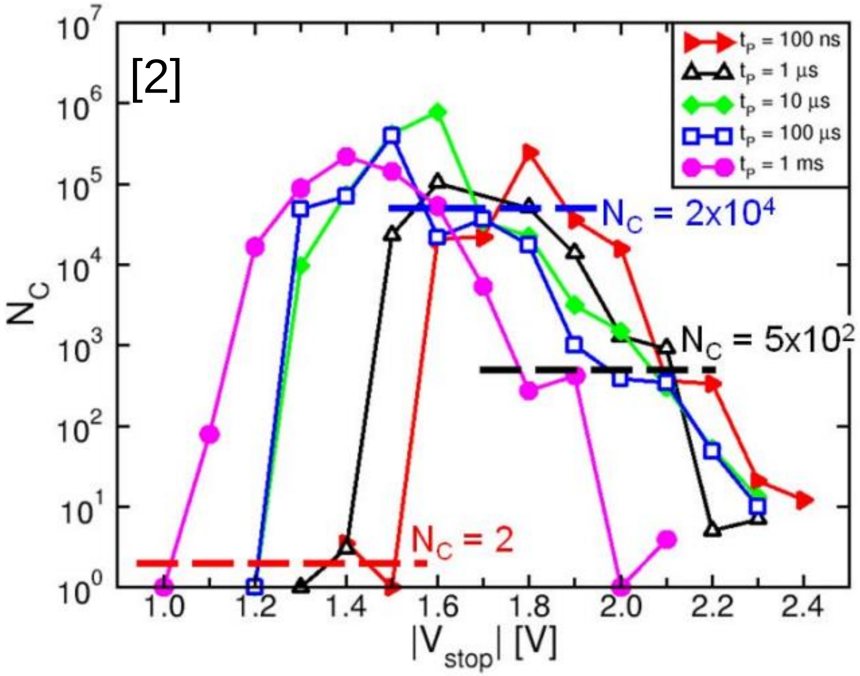


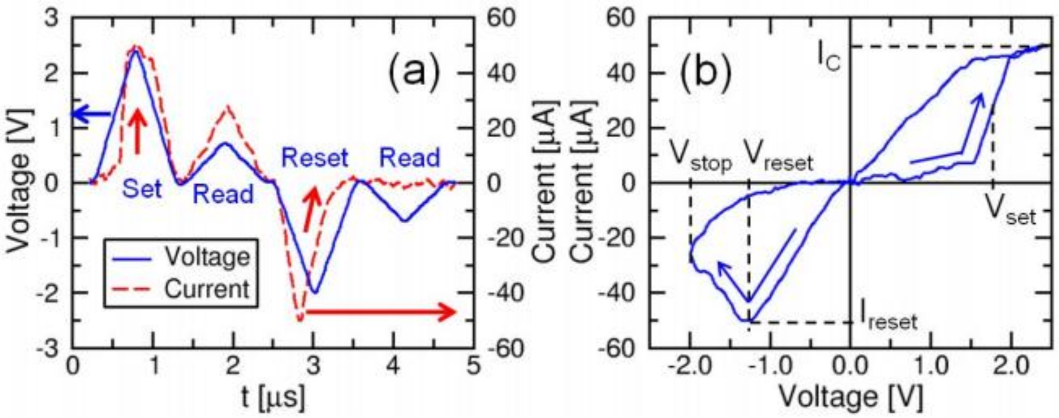
Endurance in ReRAM

- Typically in the range 10^6-10^7 cycles before device breakdown.
- Best result 10^{12} cycles using TaO_x devices![1]

- Breakdown depends on SET/RESET pulse time t_p
  - AND the stop voltage during RESET.
  - → Arrhenius type process
  - (Joule heating over energy barrier) $N_C \sim \exp\left(-\frac{E_A}{kT}\right)$





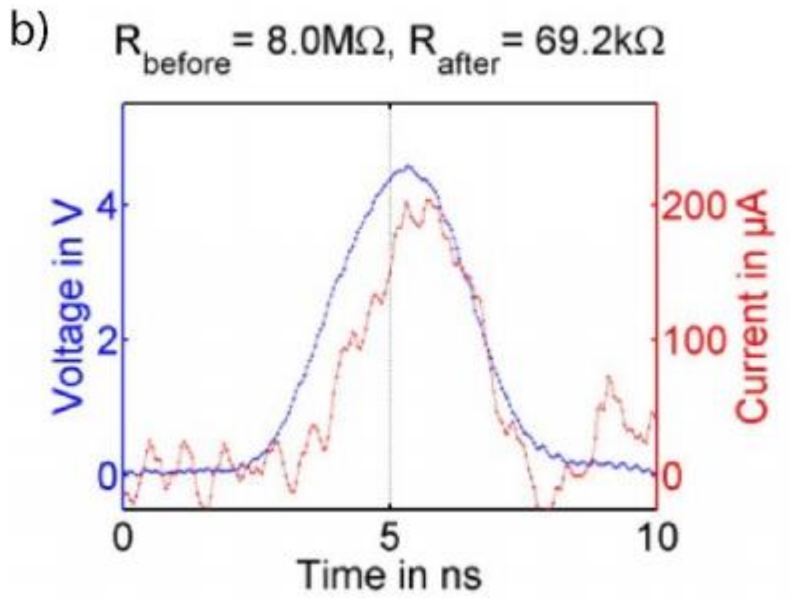


[1] Lee et al. Nat. Mater 2011, [2] Balatti et al. IRDS 2015

Write energy and speed

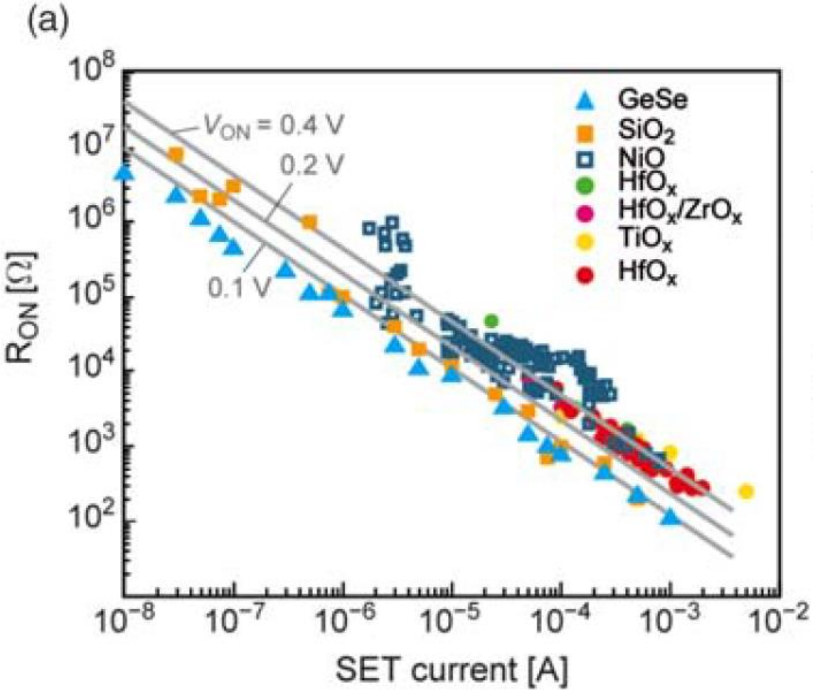
- Down to < 5 ns
  - No switch limit found (yet).
  - **Q: Why could that be?**

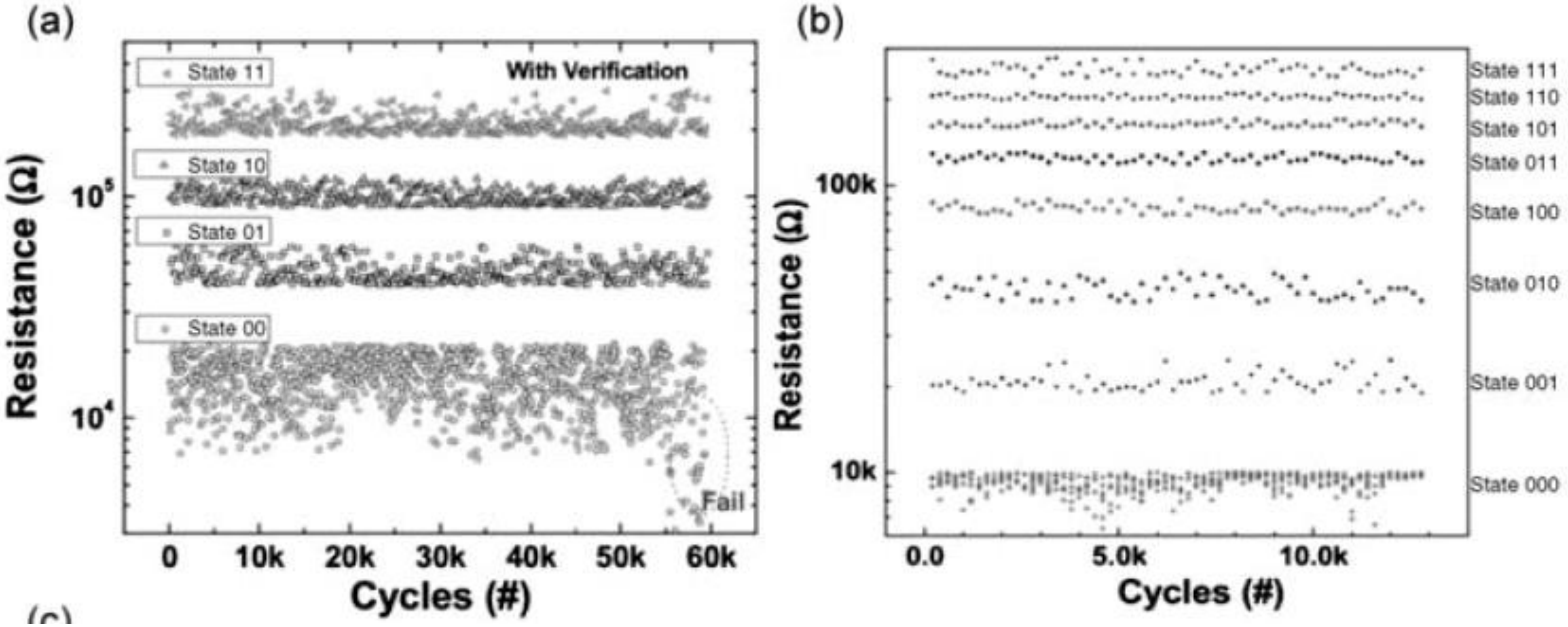
- Write energy <u>limited by current</u> needed to SET/RESET filament
  - 0.1-1 pJ/switch event
  - Different memory types require different current levels
    - Energy barriers, oxide thickness etc..



Multilevel storage

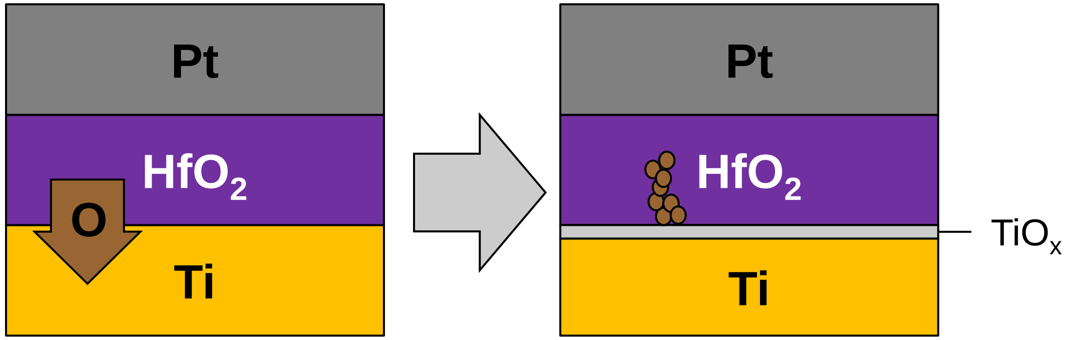
- Choosing the SET current allows for setting the LRS “arbitrarily”
- 3 bit storage has been shown to be feasible in WO_x-based VCM

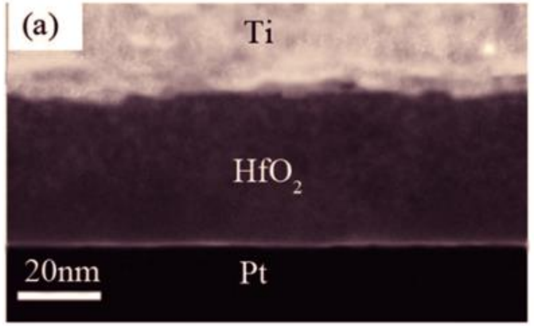


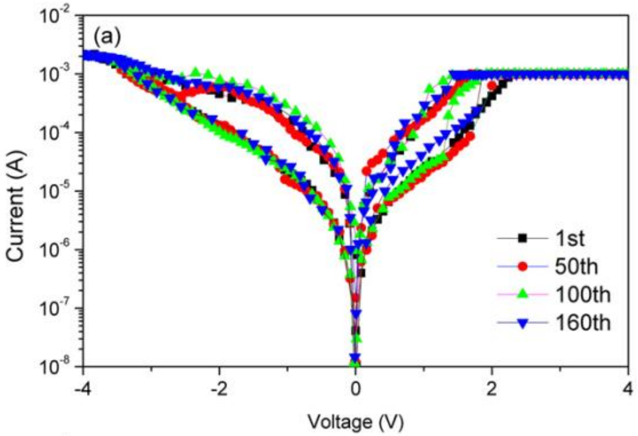


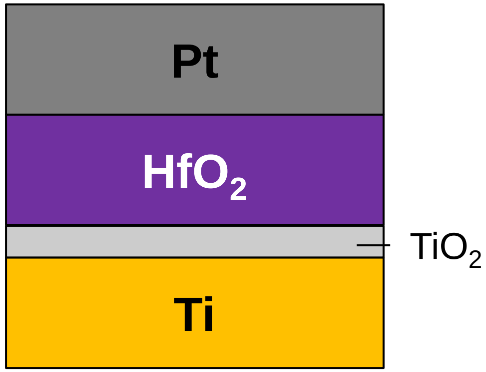
Stability of operation

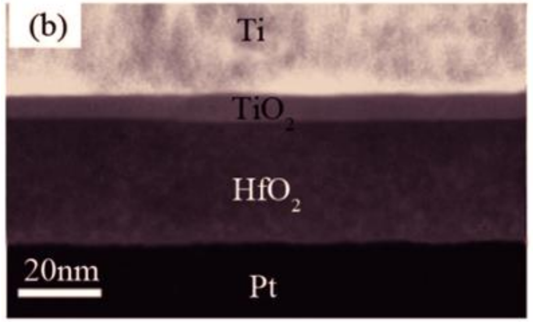
- Reactivity is needed for operation, but can lead to variations

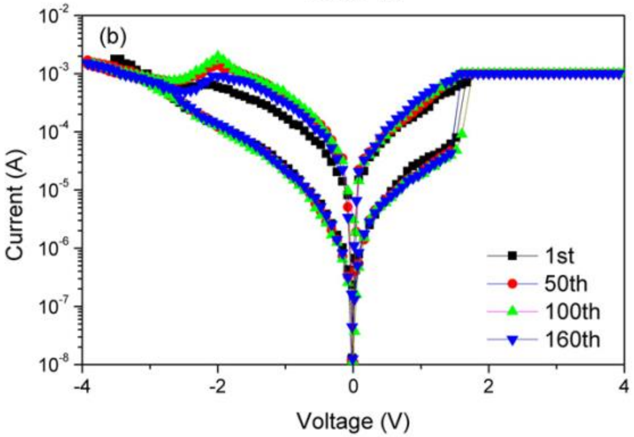


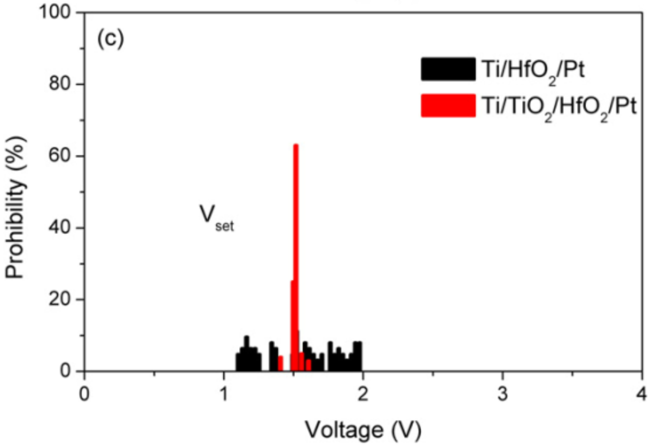








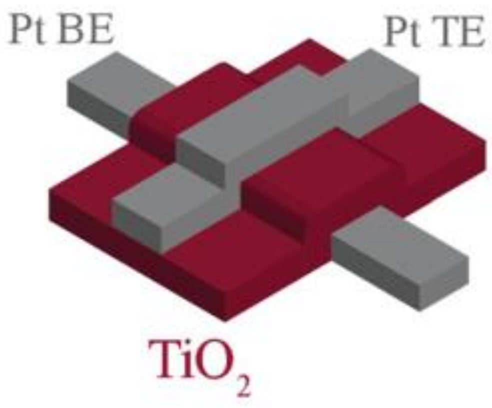


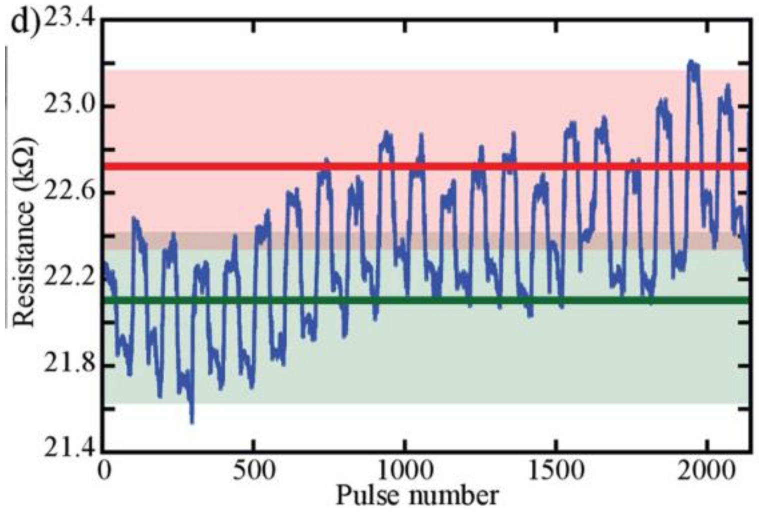


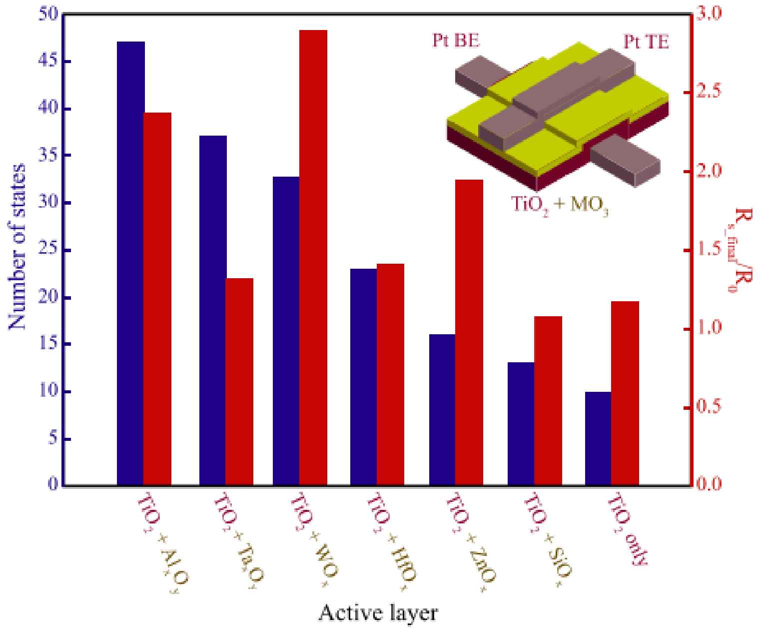
Jiang et al. Microelectron Reliab. 2016

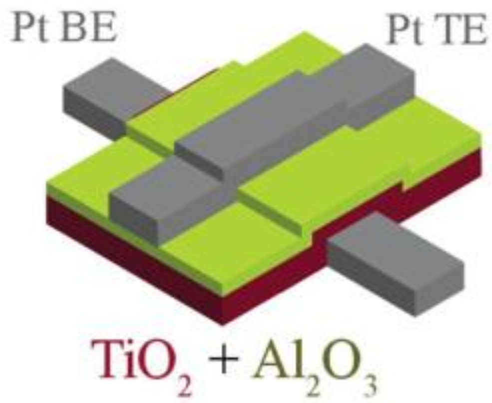
Bilayer ReRAM for stability

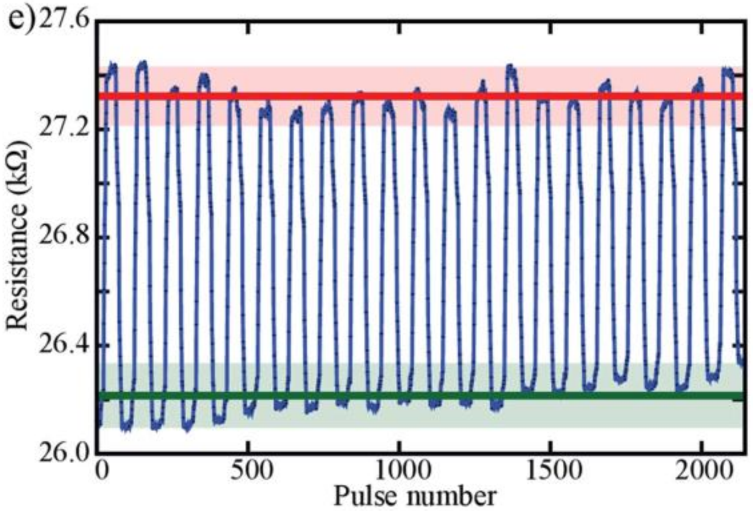
- Ultra-stable switching needed for multibit devices.
- Cycle-to-cycle drift not acceptable
- Introduction of barrier layers can improve stability
- Tested many barrier materials
  - Al_2O_3 gives best results







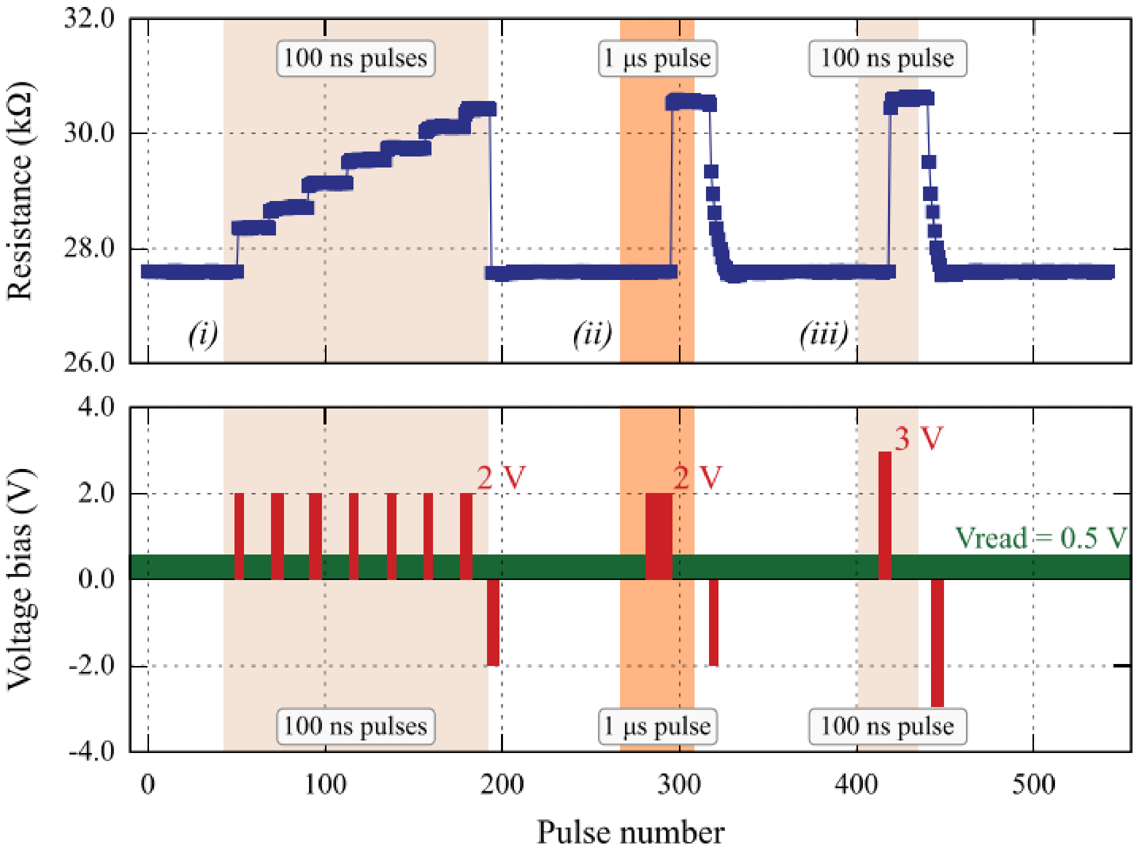


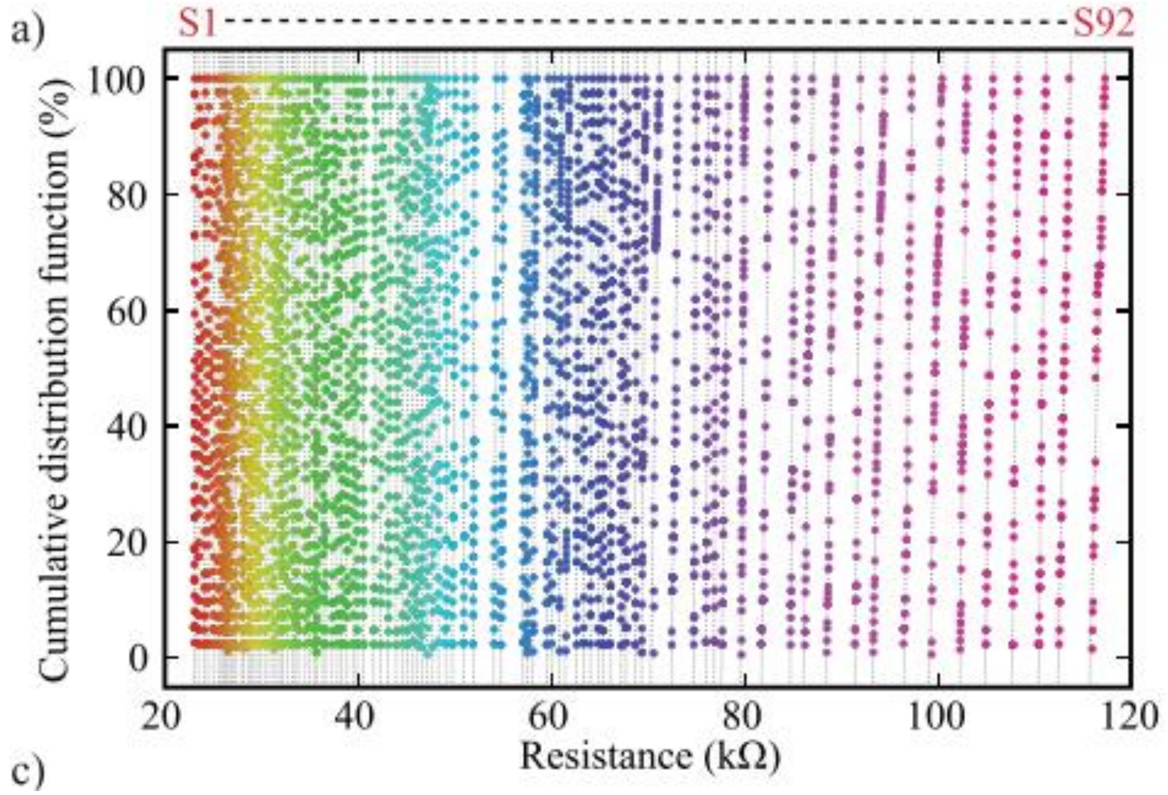


Stathopoulos et al. Nat. Sci. Rep. 2017

Pulsed SET enables even more levels

- State definition: "Sufficiently stable over time" (hours)
  + after 50 read pulses: new state separated to previous state by 3σ
- Device yield: 97% > 4 bits, 33% > 6 bits





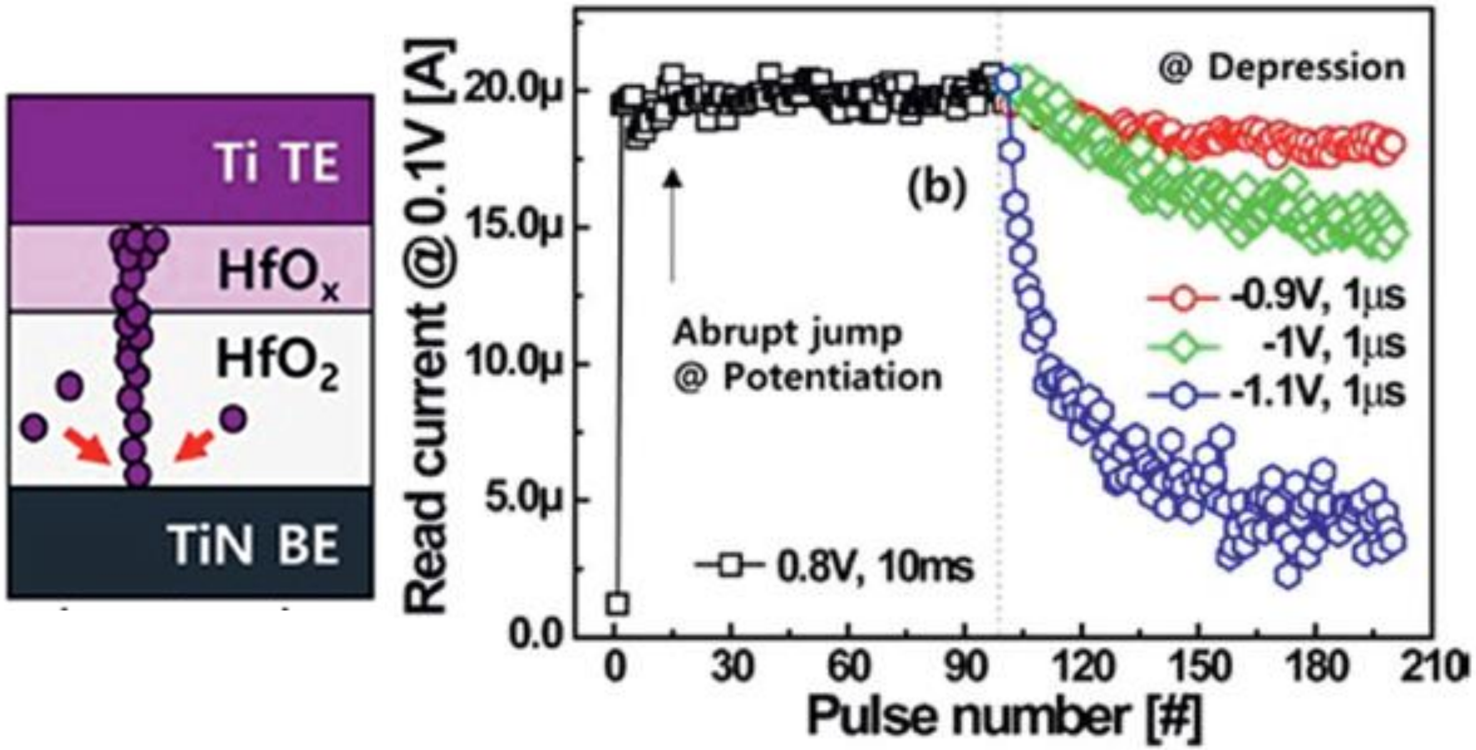
Stathopoulos et al. Nat. Sci. Rep. 2017

ReRAM as storage memory

	DRAM	3DNAND	RRAM
Nonvolatile	No	Yes	Yes
Speed (ns)	10	10^4	>5 ns
Energy use (pJ/write)	0.1	1	0.1-1
Endurance (cycles)	10^{16}	10^5	10^6-10^7
Multilevel?	No	Yes	3-6 bit
Scalability	6-8F^2	3D!	3D!
Other	Destructive Read	High Voltage	Abrupt SET

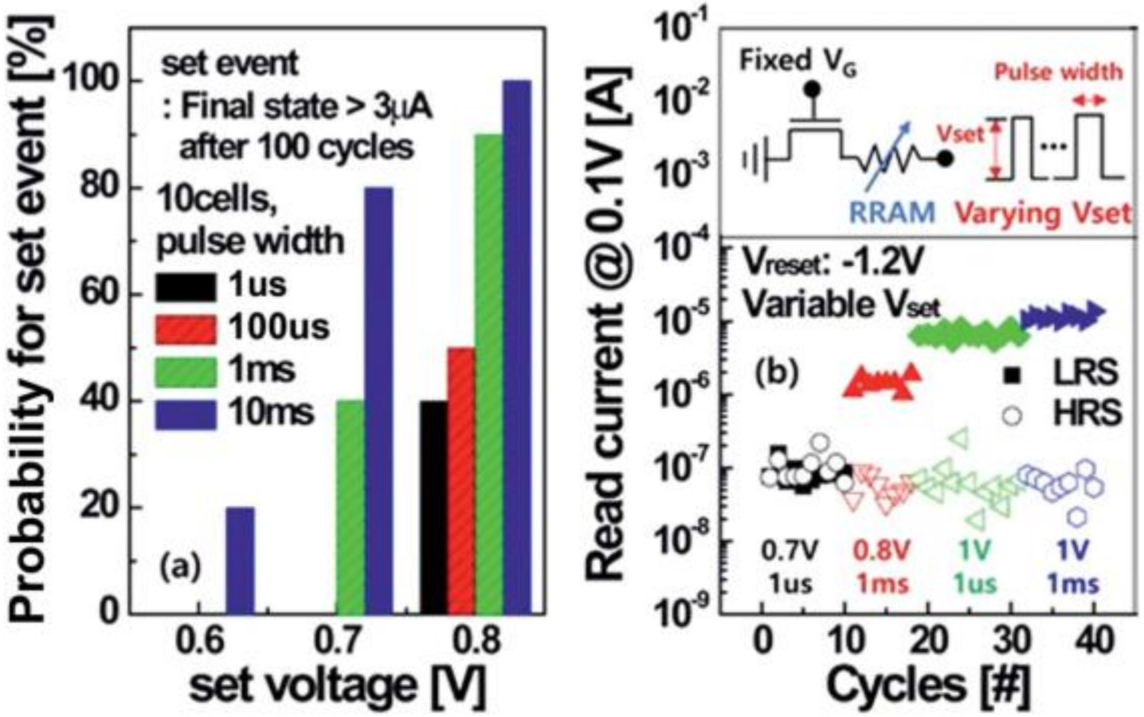
ReRAM as synaptic device in SNN

- SET is an abrupt event
  - E-field → O_{Va} diffusion towards BE
    ”Stops” when filament forms
- RESET is more gradual
  - O_{Va} diffuse back from BE leaving growing tunnel junction behind



Moon et al. Faraday Disc. 2019

Controlling potentiation

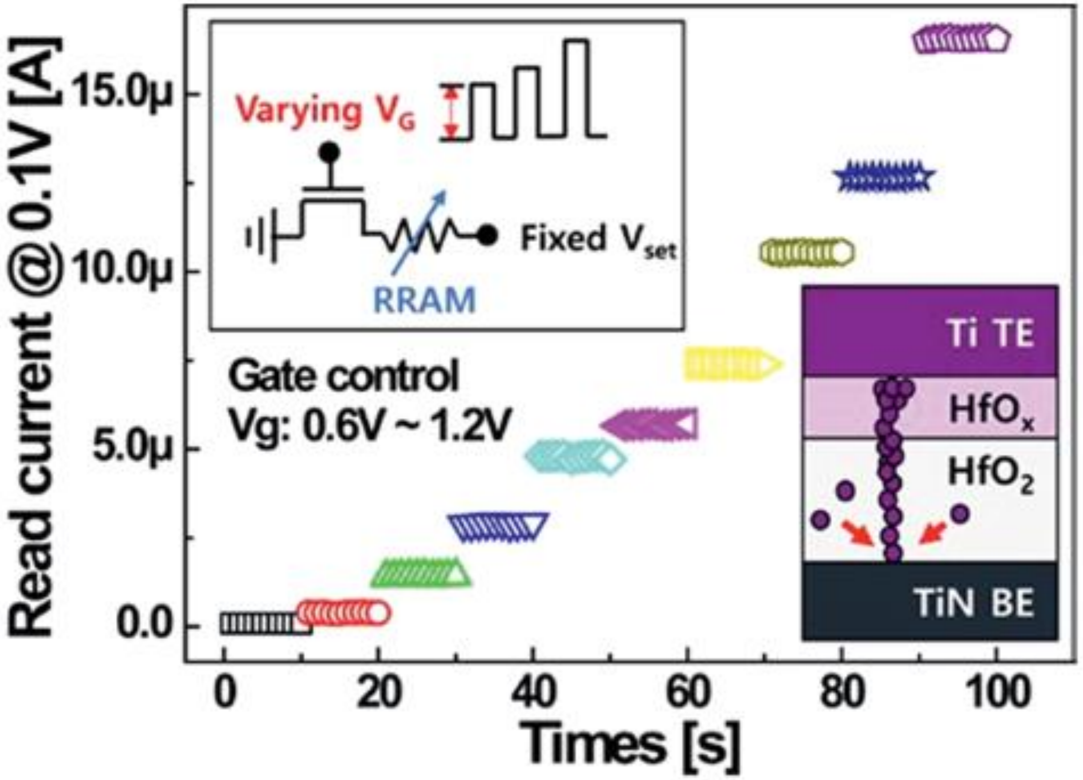


- Maximum current is fixed by V_g on Transistor
- SET is probability controlled
- Can affect probability by time/bias

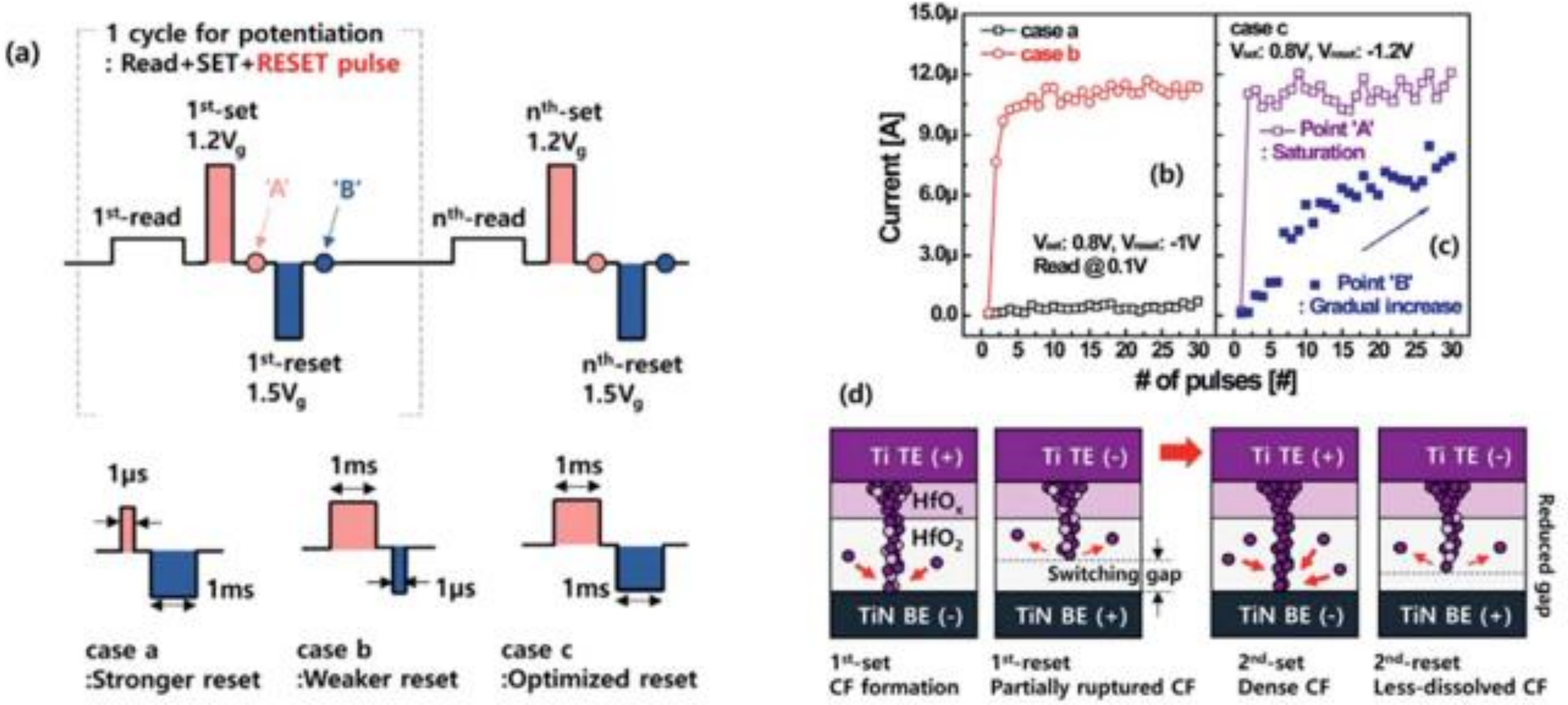
→ Variable LRS state

Control potentiation by V_G

- V_G on transistor essentially sets the maximum current → ”compliance level”
- Variable V_G → Additional burden to peripheral circuit design

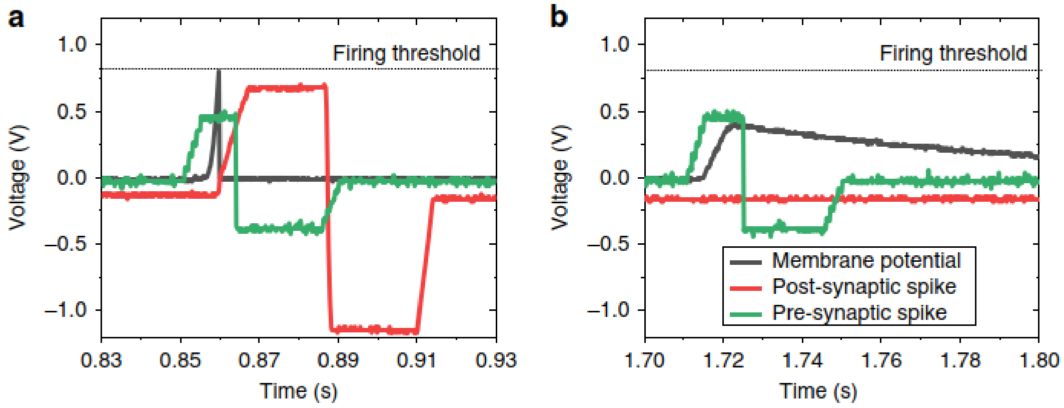


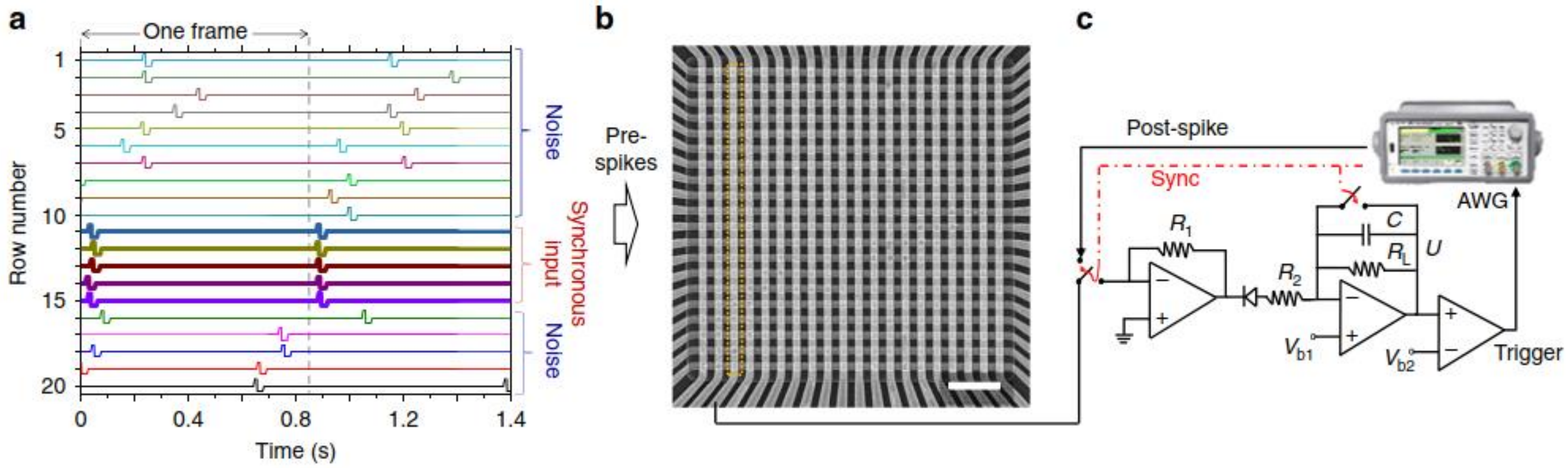
Double pulse for gradual potentiation



Example of SNN implementation with ReRAM

- 20 pre-neurons, 20 RRAM synapses, 1 Si post-neuron
- Coincidence detection
- Learning by STDP

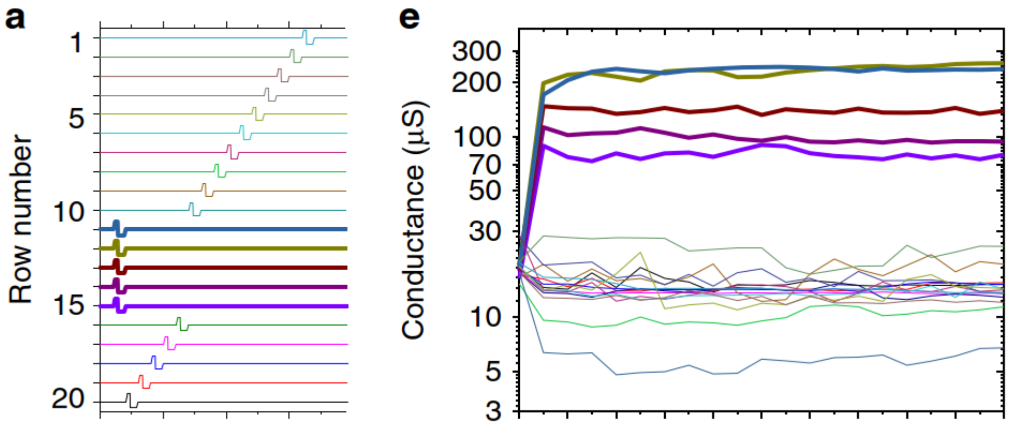




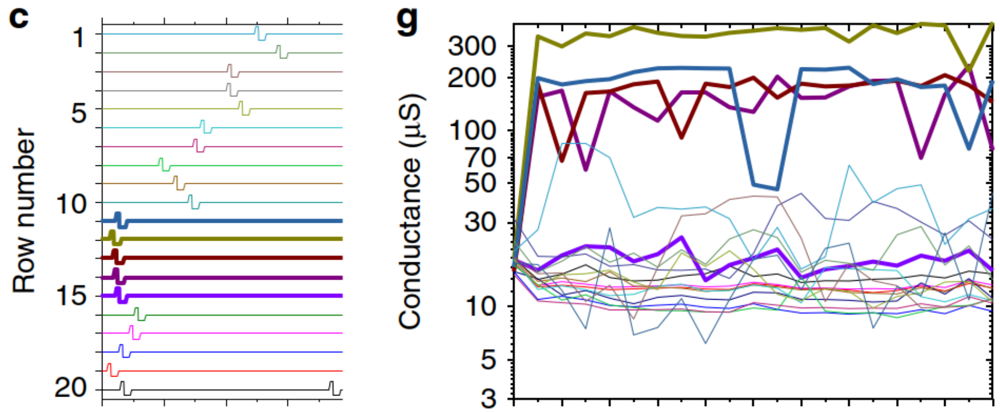
Presioso et al. Nat. Comm. 2018

Coincidence detection

- Synapses learn pattern even with large induced noise, and noise on other channels.



$$\left(\Delta_{offset}\right)_{max} = 0\,ms$$



$$\left(\Delta_{offset}\right)_{max} = 216\,ms$$

Relearn pattern

- First learned pattern can be forgotten
- New pattern learned.