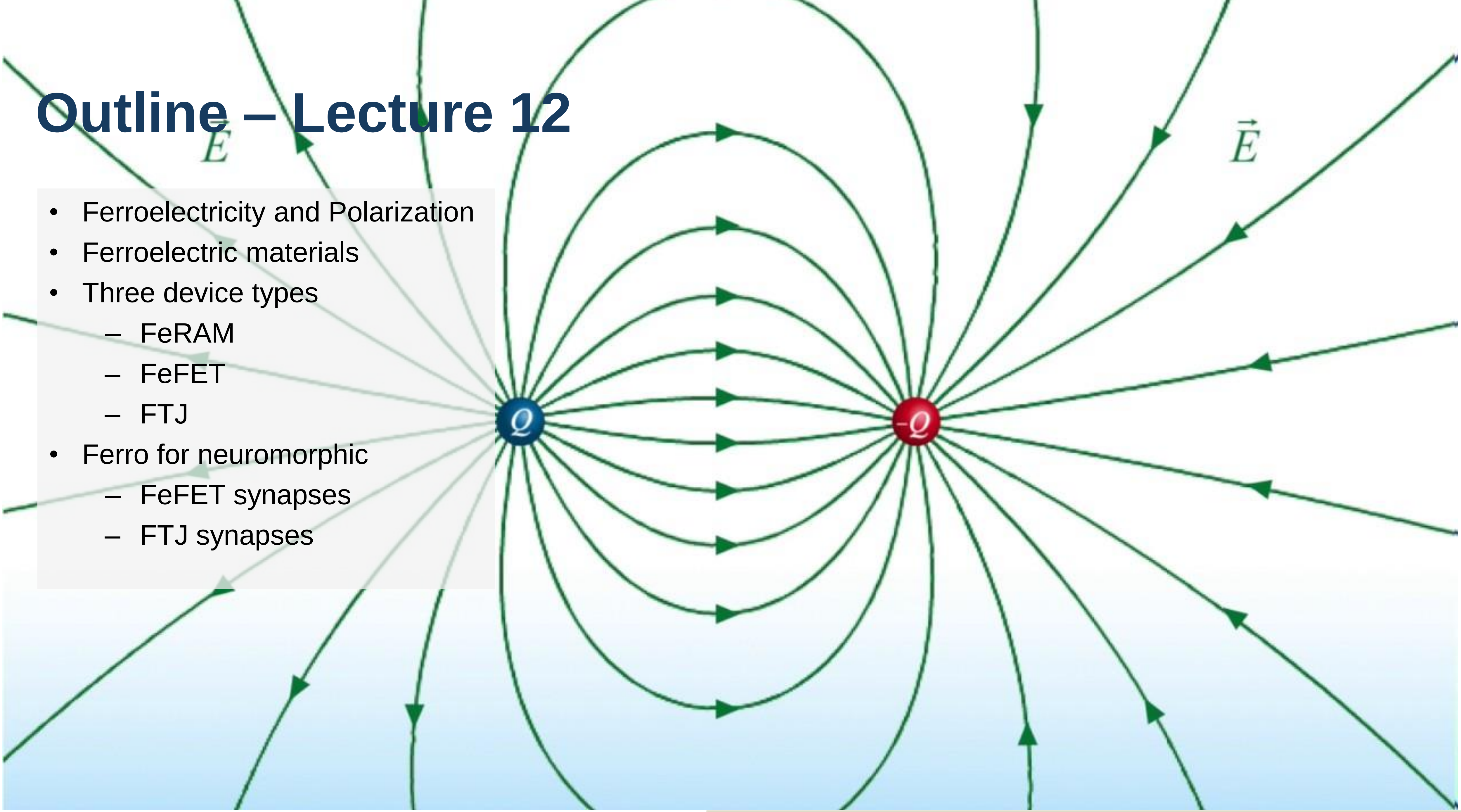
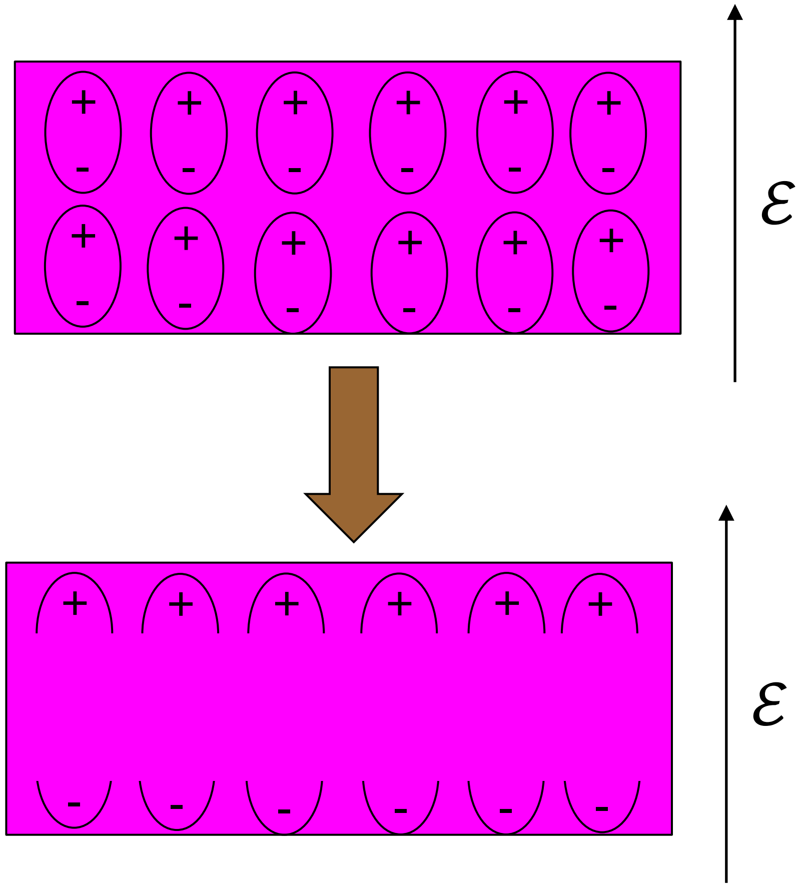
Lecture 12 – Ferroelectric Memories

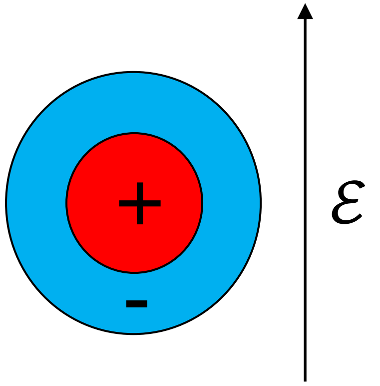
Outline – Lecture 12

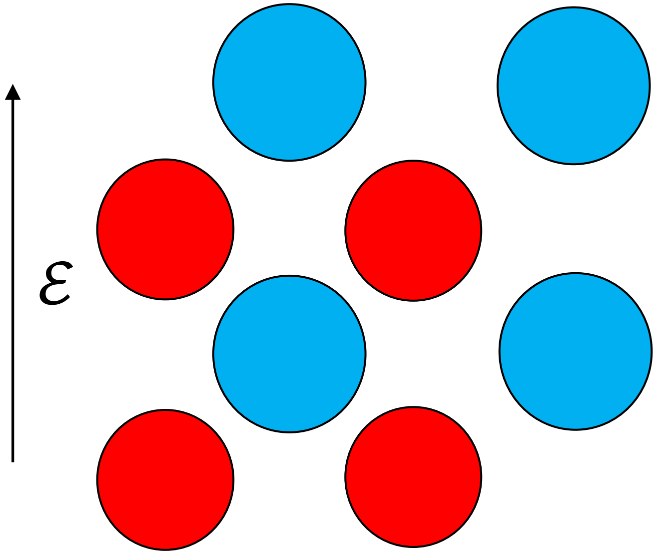
- Ferroelectricity and Polarization
- Ferroelectric materials
- Three device types
  - FeRAM
  - FeFET
  - FTJ
- Ferro for neuromorphic
  - FeFET synapses
  - FTJ synapses



Polarization







$$P = \varepsilon_0 \chi \mathcal{E}$$

$$D = \varepsilon_0 \mathcal{E} + P$$

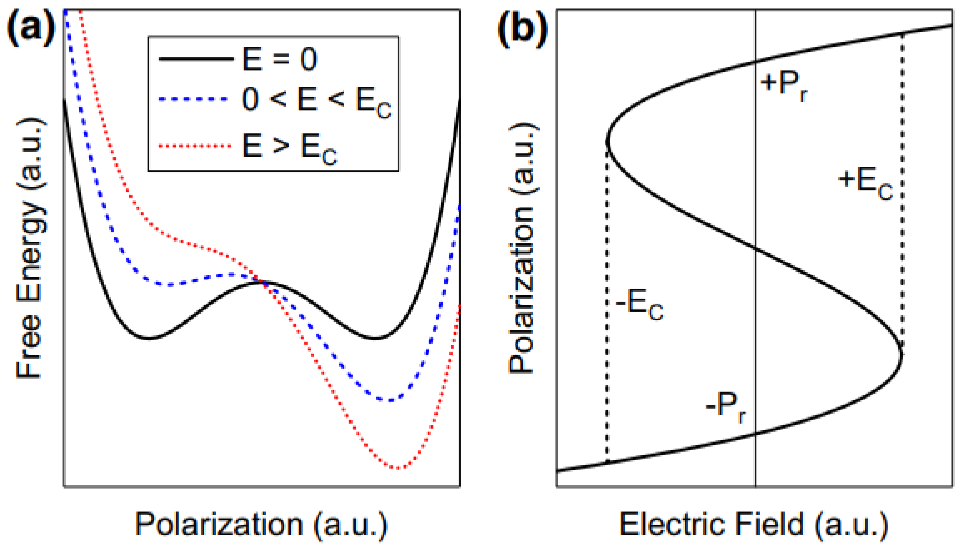
$$\rightarrow \varepsilon_r = 1 + \chi$$

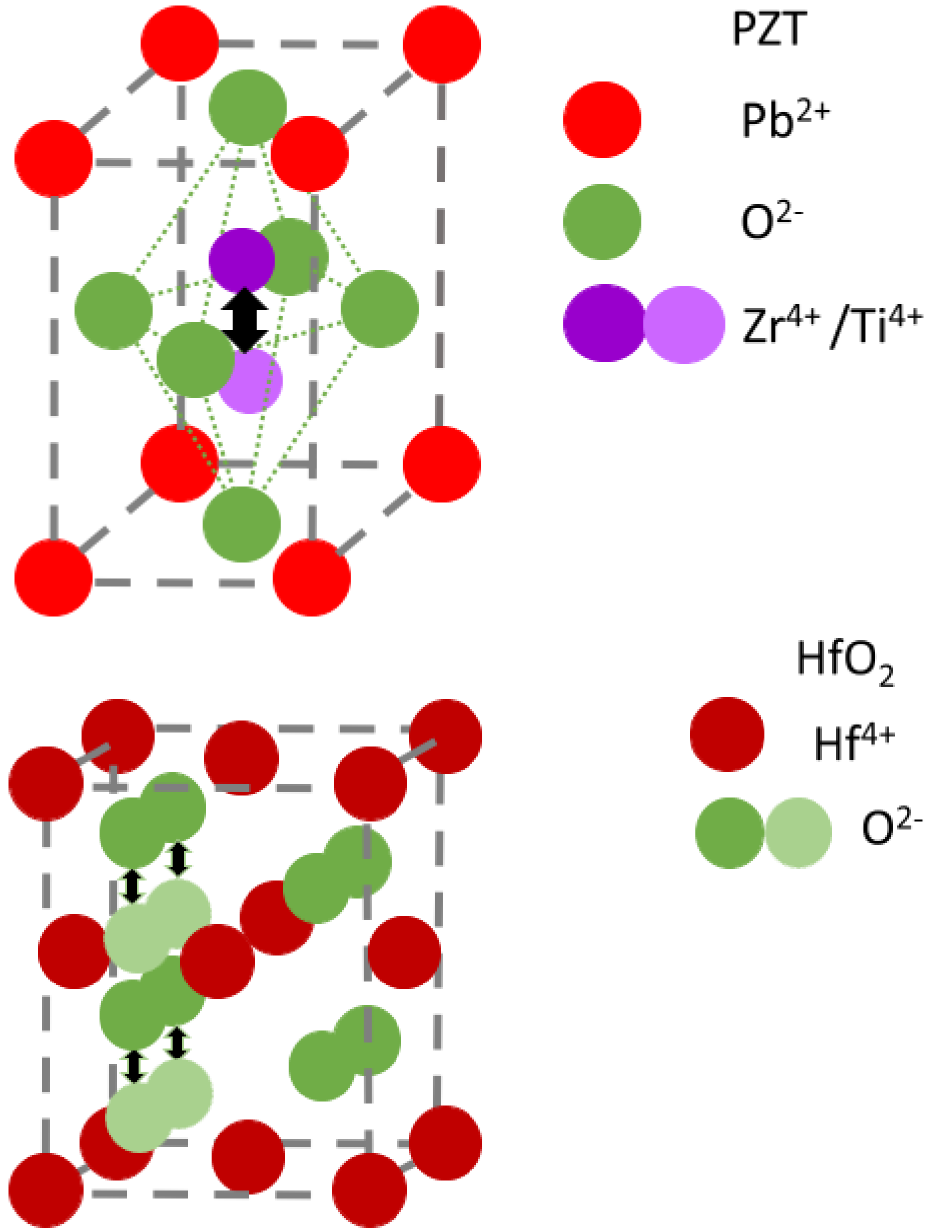
Ferroelectric polarization

- Ferroelectricity: Polarisation remains even **without** externally applied electric field
- Requires non-centrosymmetric crystal structure
  → two polar equilibrium states

Free energy vs Polarization

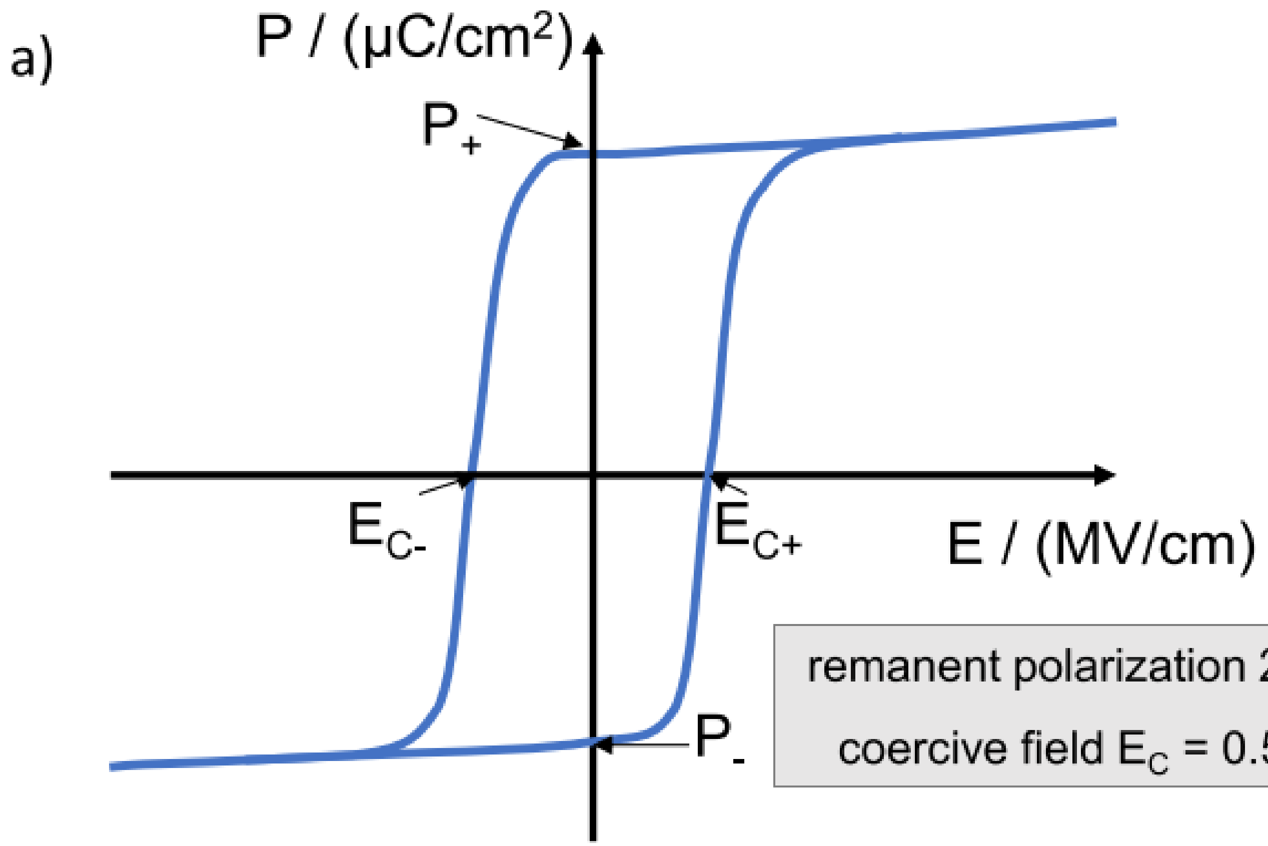
$$U = \alpha P^2 + \beta P^4 - \mathcal{E}P, \qquad \alpha < 0, \beta > 0$$





Mikolajick et al. IEEE Trans. Electron Dev. 2020, Pêsic et al. J. Comp. Electron. 2017

Polarization – electric field curve



remanent polarization $2P_R = |P_+| + |P_-|$

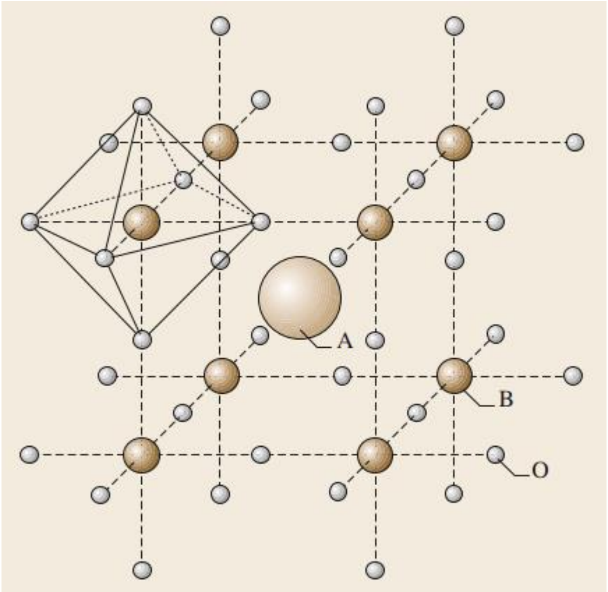
coercive field $E_C = 0.5\,(|E_{c+}| + |E_{c-}|)$

Mikolajick et al. IEEE Trans. Electron Dev. 2020

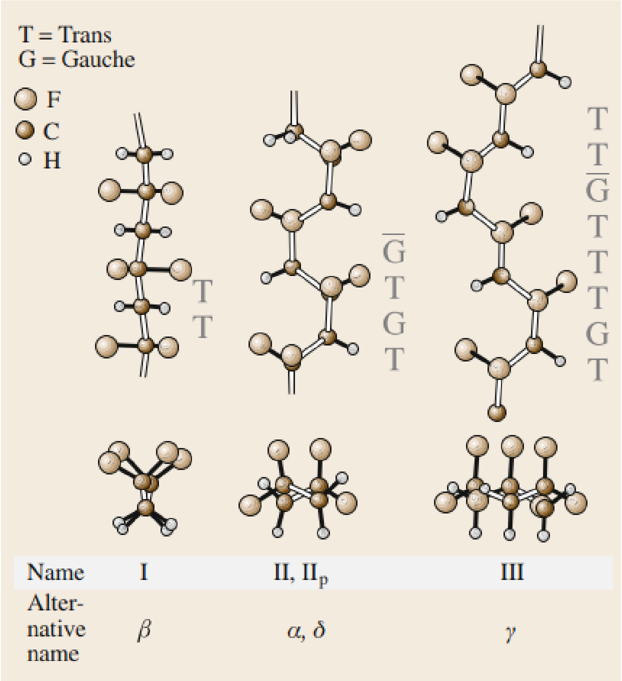
Ferroelectric materials

- Perovskite ferroelectrics
  - Distorted structures → ferroelectricity
  - $BaTiO_3$, $PbTiO_3$, $KNbO_3$, $Pb(Zr, Ti)O_3$ (PZT)…
  - Very high $\varepsilon_r \sim 100 - 1000$!!
- Polyvinylidene fluoride (PVDF)
  - Polar bonds perpendicular to polymer chain aligns
  - $P_r \sim 13\ \mu C/cm^2$
  - Flexible material
- Hafnium dioxed, HfO_2
  - FE effect discovered as late as in 2011!
  - Doping/stress → ferroelectricity
  - P_r 20-30 $\mu C/cm^2$
  - Ferroelectric at least down to 1 nm thickness
  - CMOS compatible

Perovskite crystal ($CaTiO_3$)



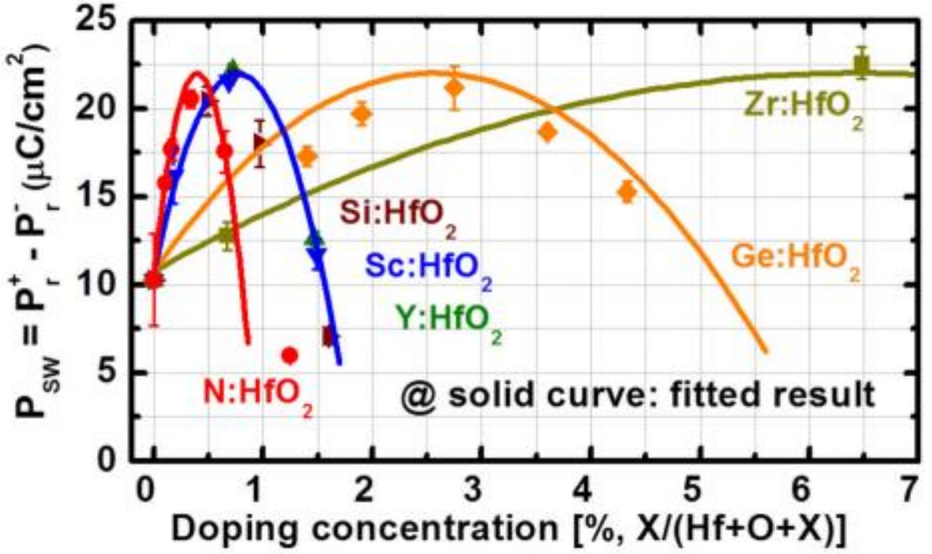
PVDF polymer chains

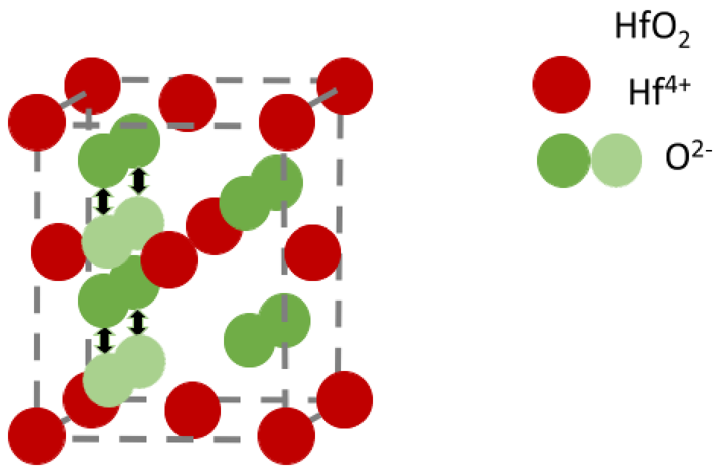


Ferroelectricity in doped HfO_2

- HfO_2 dopants: Si, Al, Y, Gd, La, Zr, …
- Crystallization during thermal annealing
- Strain induces phase transition
  - Rhombohedral ferroelectric phase
  - O atoms switch place

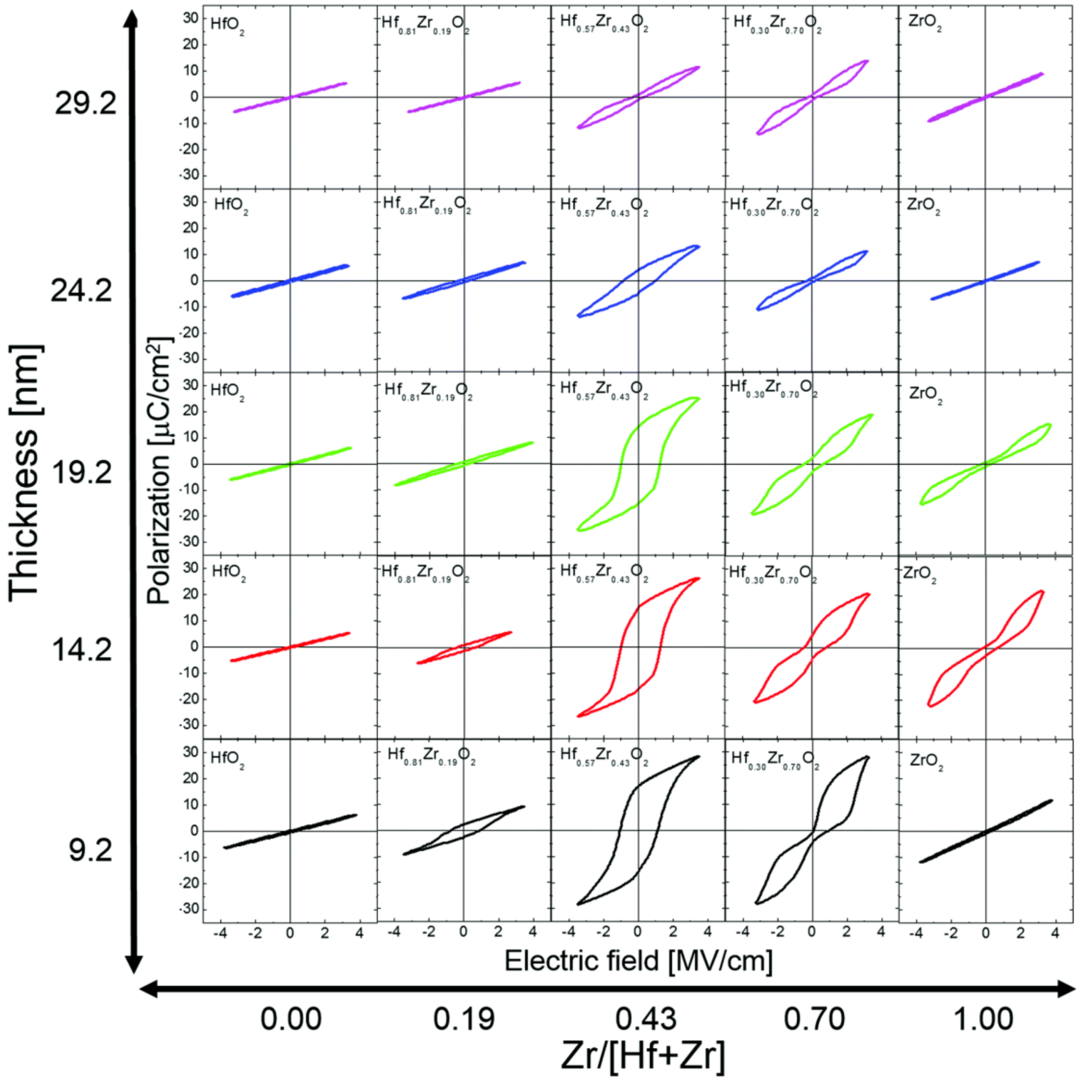
- $Hf_{1-x}Zr_xO_2$ has become the most successful material





$HfZrO_2$ (HZO)

- P_r high for wide range of Zr content ($Hf_{1-x}Zr_xO_2$)
  - Maximum around x = 50%
- Antiferroelectric at higher Zr-content.
- Thinner films (< 15 nm) yield higher P_r.
- Related to fraction of phases:
  - **Monoclinic m-phase:** paralectric
    - Most stable at large thicknesses
  - **Orthorhombic o-phase:** ferroelectric
  - **Tetragonal t-phase:** antiferroelectric
    - Most stable in ZrO_2



Park et al. Nanoscale 2017

Exercise: High coercive field in HZO

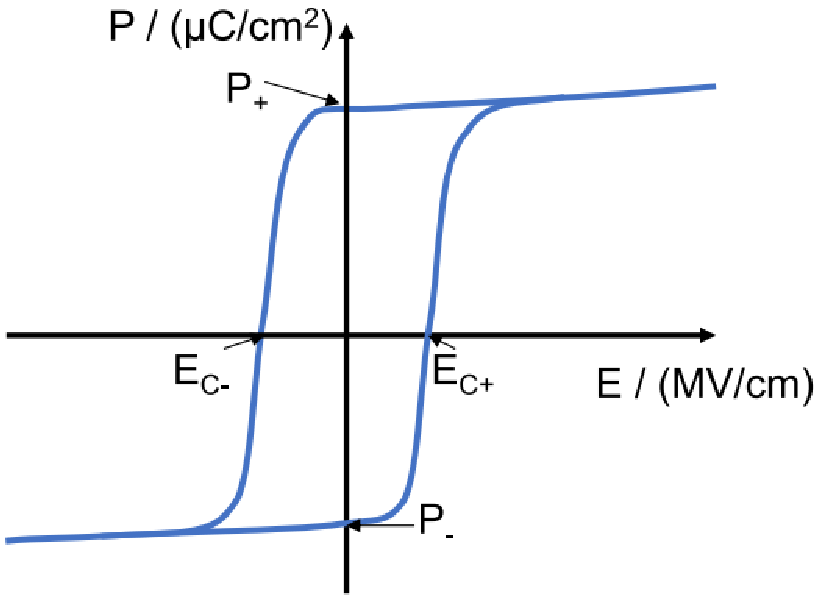
The higher E_c allows for scaling down the thickness.

1. Why is that?

2. Why is this important from a technological point of view?

Coercive field comparison

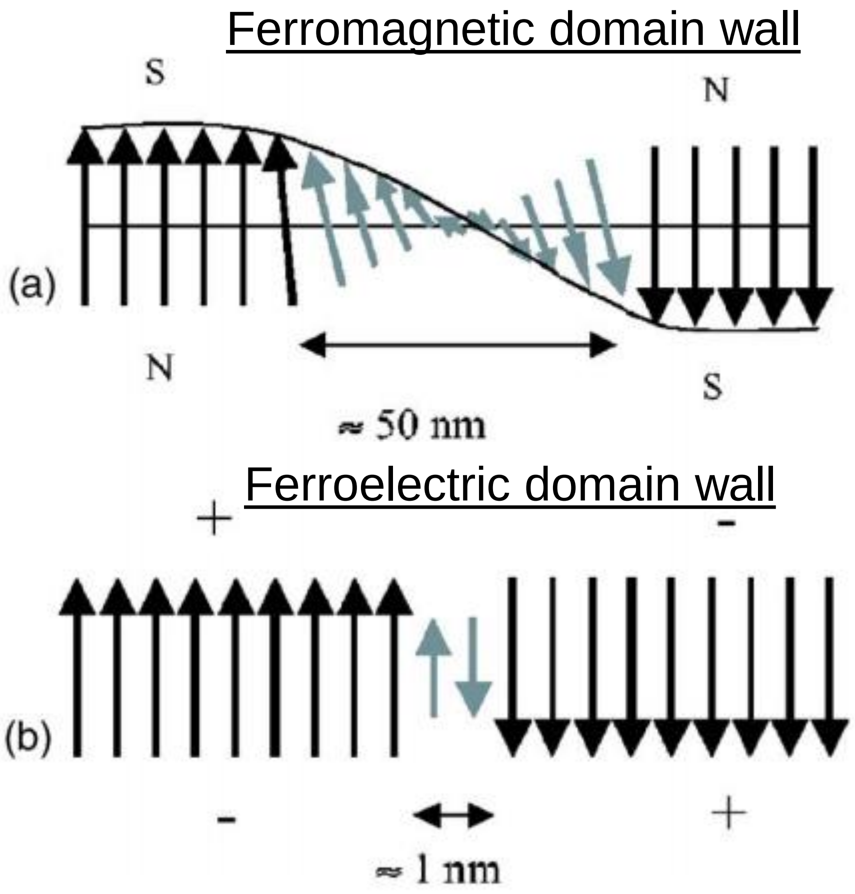
Material	E_C (MV/m)
PVDF	1
$LiTaO_3$	1.7
$LiNbO_3$	4
$PbZrTiO_3$	10
$HfZrO_3$	**150-200(!!)**



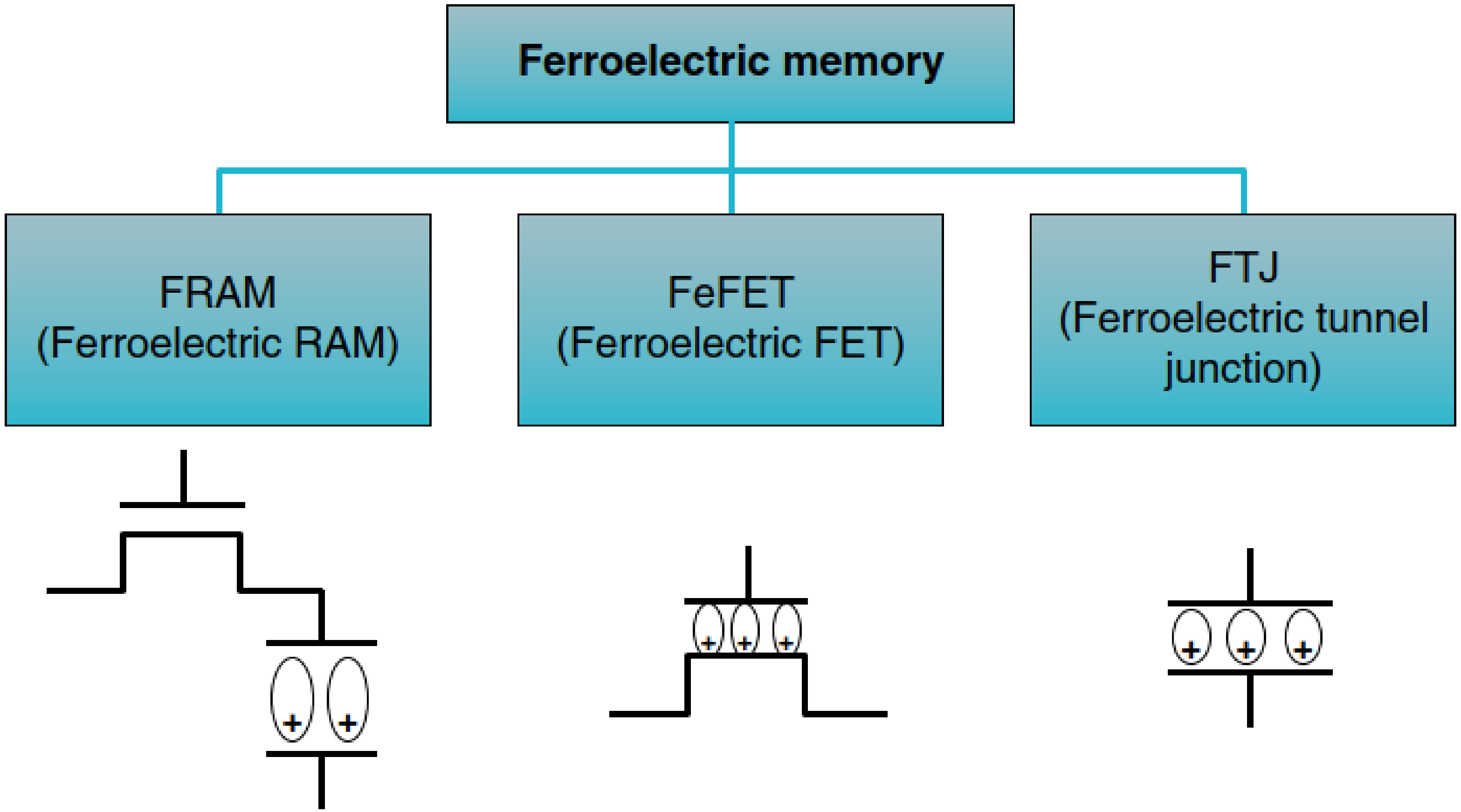
Scalability of ferroelectric memories

- Ferroelectricity scales better than ferromagnetism!

- Scaling limited by minimum size of a stable FE domain
- At least retains ferroelectricity below 10 nm diameter.
- HZO retains FE down to 1 nm thickness (at least!)



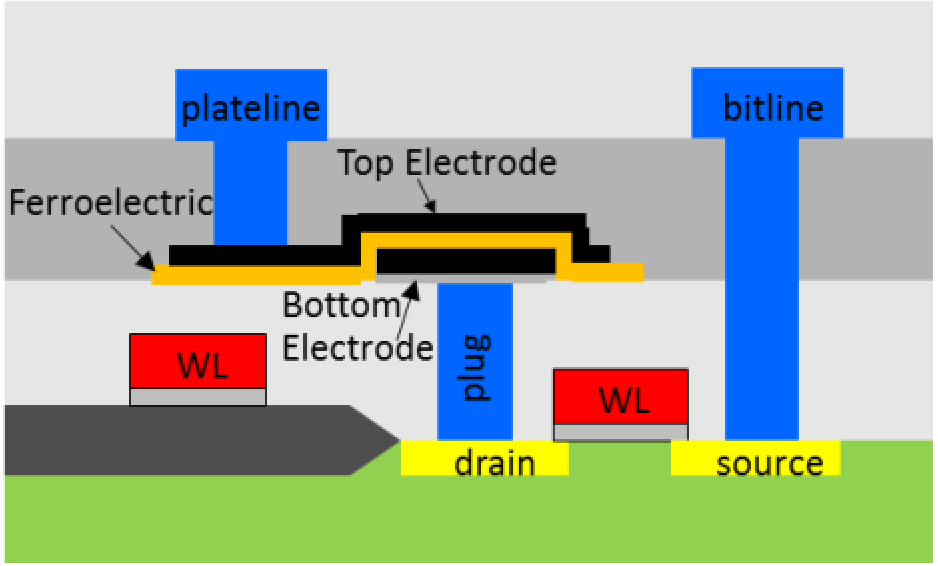
Three types of memory types



FeRAM

- Ferroelectric capacitor placed in series with MOSFET selector.
  - Structure is identical to DRAM, but non-volatile!
- Ferroelectric state is sensed by applying switching voltage and see whether it switches or not
- Destructive read
- Limited scalability due to needed size for sizeable capacitive current – 90 nm
- Endurance demonstrated up to 10^{12} cycles!

- Commercially available
  - 32 kbit Fujitsu FRAM in PS2

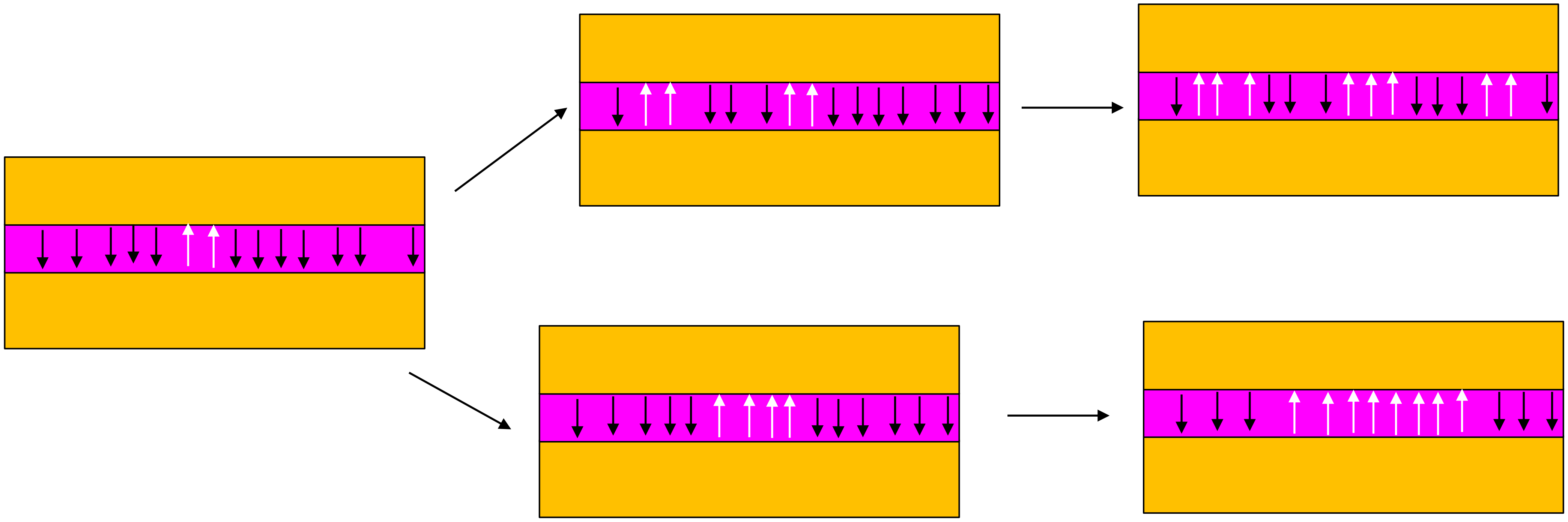


Mikolajick et al. IEEE Trans. Electron Dev. 2020

Switch speed

- Speed is limited by generation of new reverse ferroelectric domains, nucleation rather than domain motion < 1 ns
- 280 ps is the record measured in FeRAM

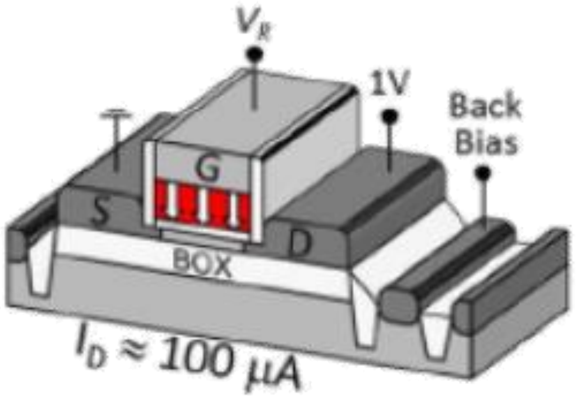
Nucleation-limited

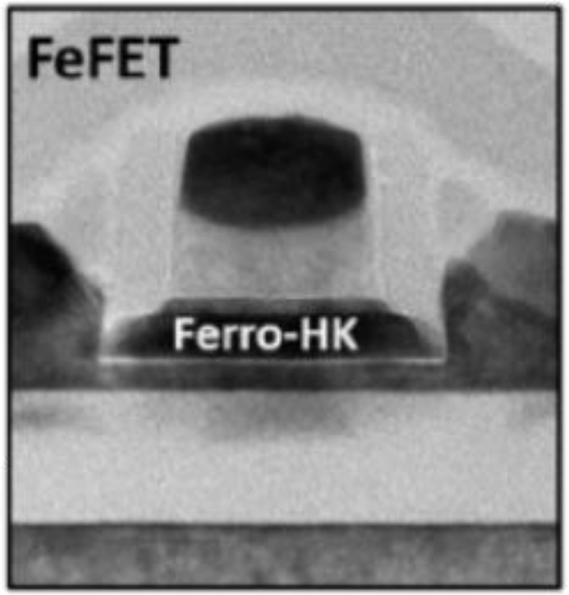


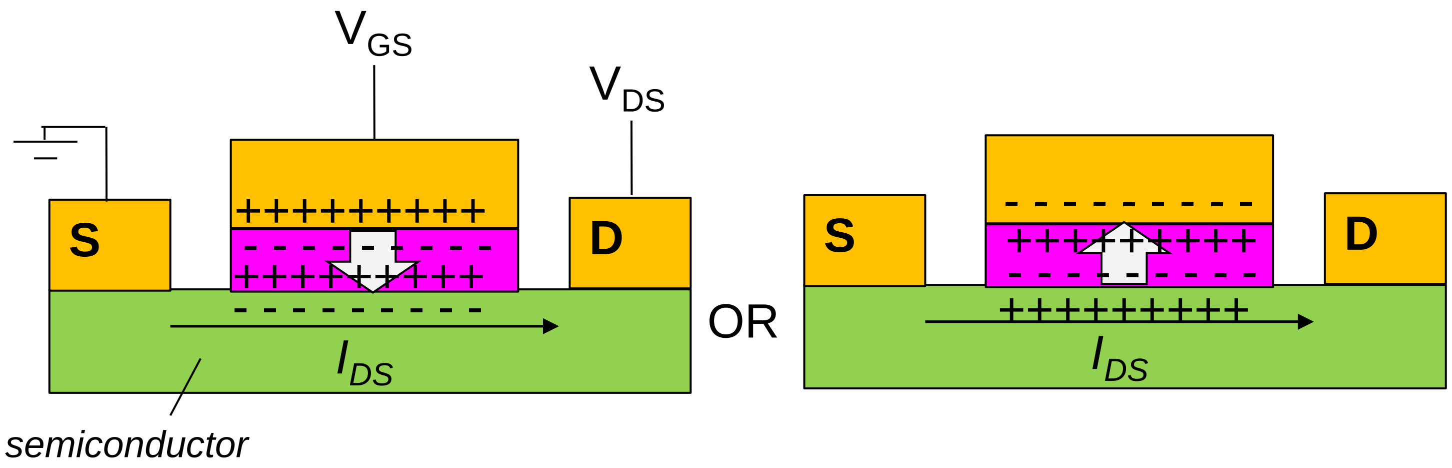
Domain wall motion limited

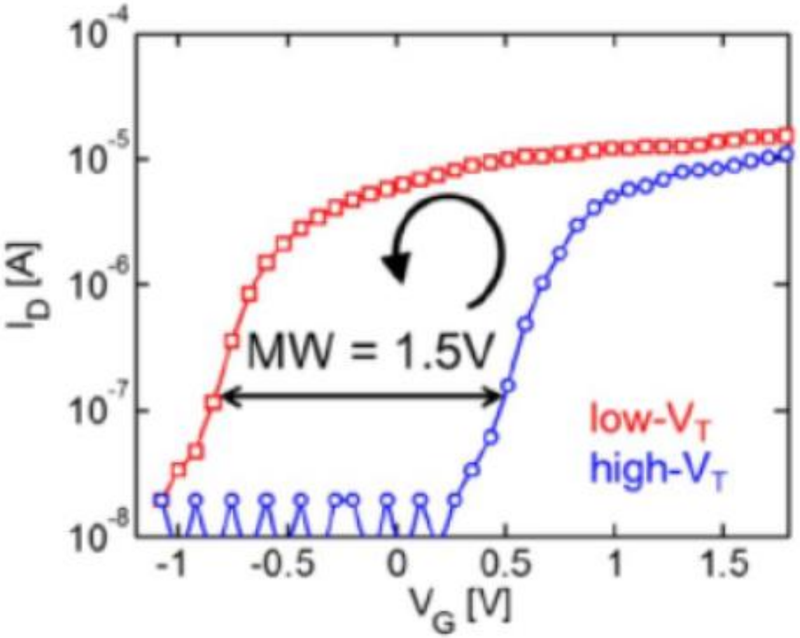
FeFET

- Integrate ferroelectric gate dielectric in MOSFET
- Polarization state shifts MOSFET threshold voltage









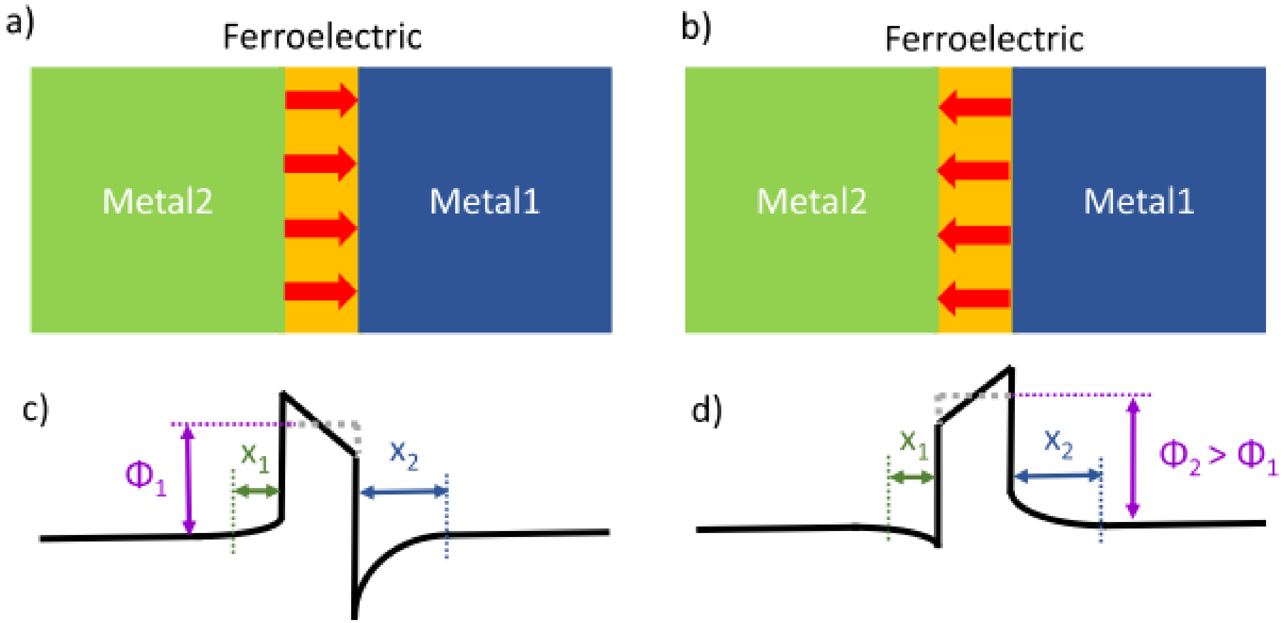
Three main challenges:

1. Control the interface in metal-FE-semiconductor system
2. Realizing 10 year retention
3. Realizing high endurance

Mikolajick et al. IEEE Trans. Electron Dev. 2020

Ferroelectric Tunnel junction

- Two-terminal resistive memory
- Relies on transport through the ferroelectric layer
- Contacts have different anisotropy in screening length
  → different electronic band bending
- Leakage current depends on the polarization state → R_{off}/R_{on} contrast



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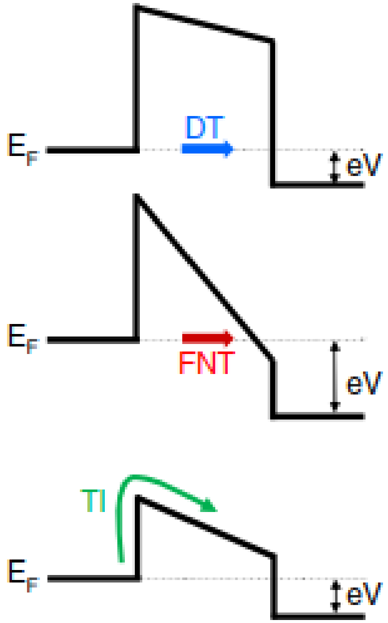
Transport in metal-FE-metal FTJs

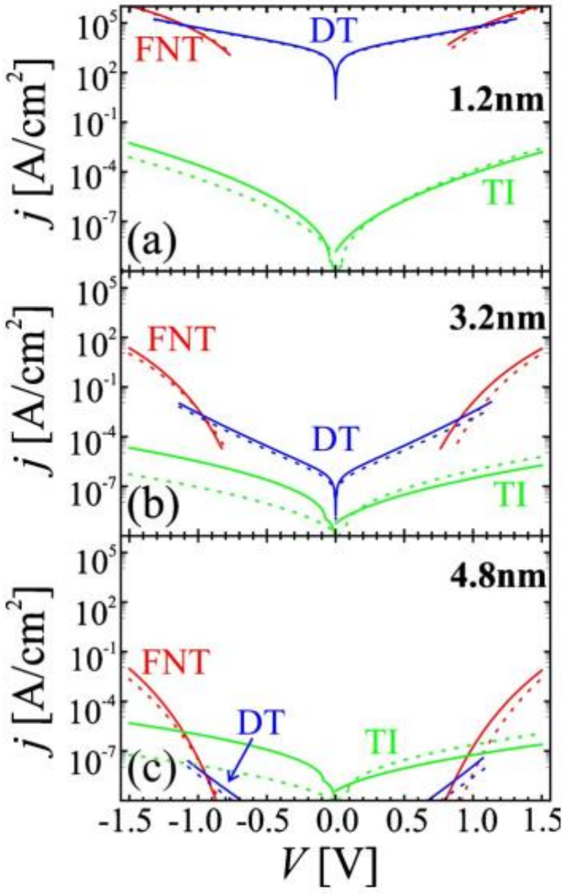


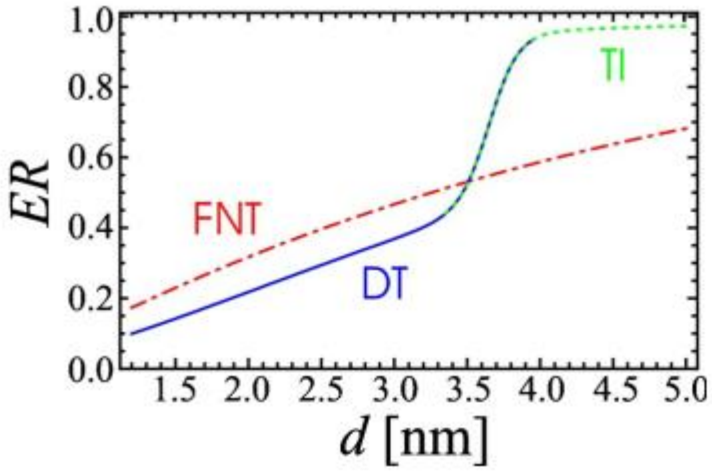
- Like in ReRAM, many transport paths, not all affected by FE
- For maximum R_{off}/R_{on}:
  - Thermionic Injection (TI)
  - Direct tunneling (DT)
  - Fowler-Nordheim Tunneling (FNT)
  - Trap-assisted tunneling
  - Electron hopping

→ Need thin enough layer for efficient TI

→ But not too thin! → DT, FNT

- Examples of TER > 1000



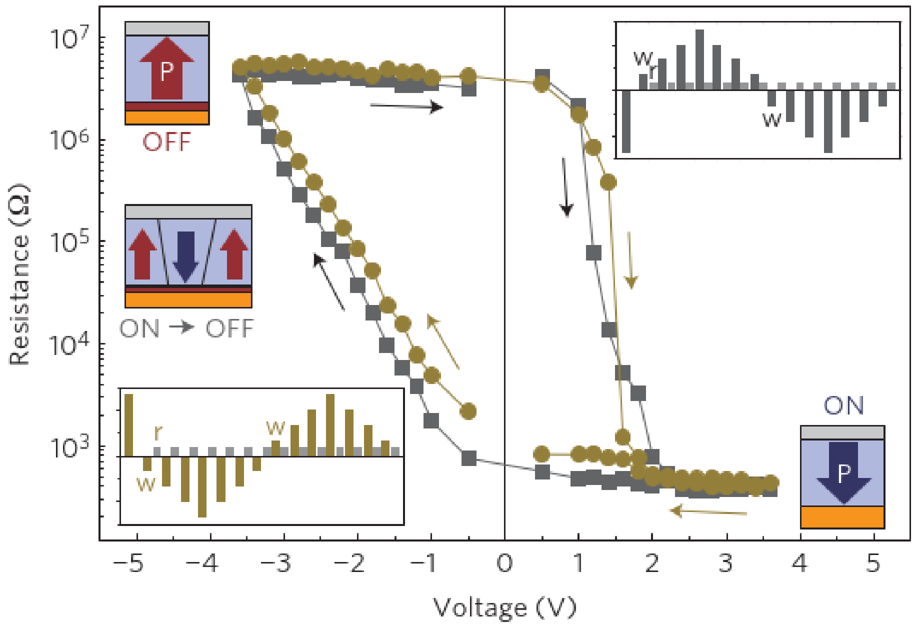


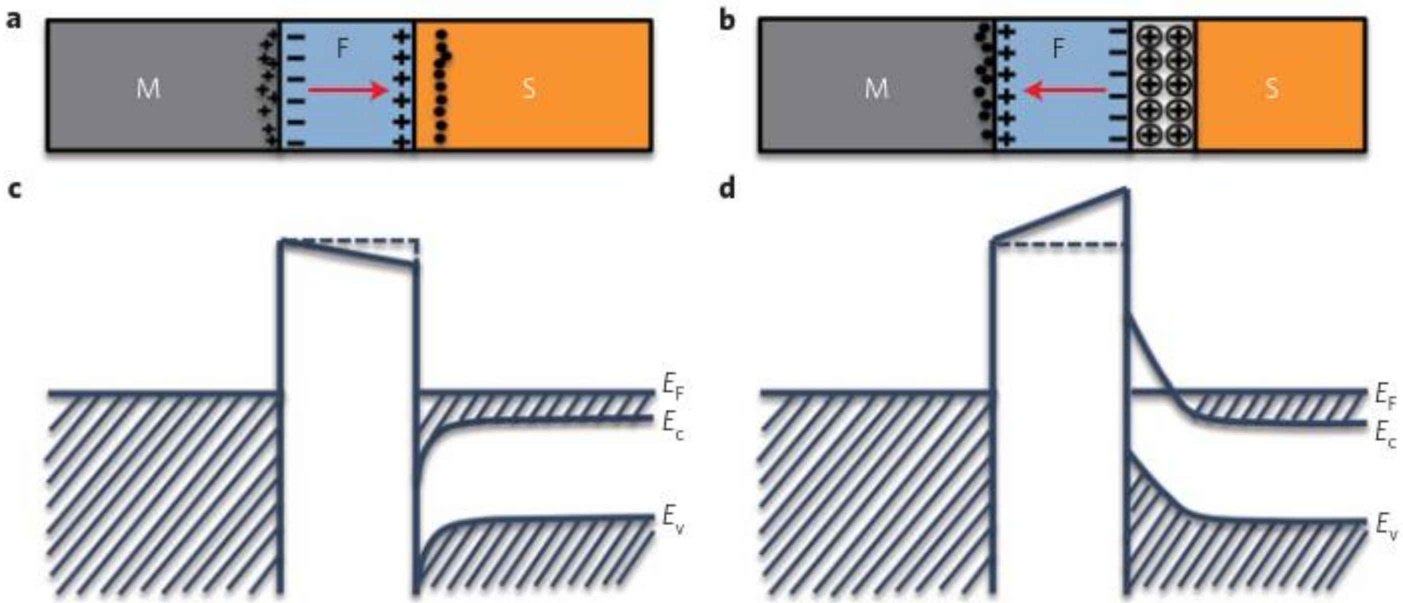
$$ER = \frac{j(P>0) - j(P<0)}{j_>},$$

Metal-FE-semiconductor FTJs

- Semiconductors can be depleted → Modulation of tunnel barrier **width**!
- Large R contrast even with direct tunneling

- TER > 10^6 achieved





Wen et al. Nat. Mater. 2013

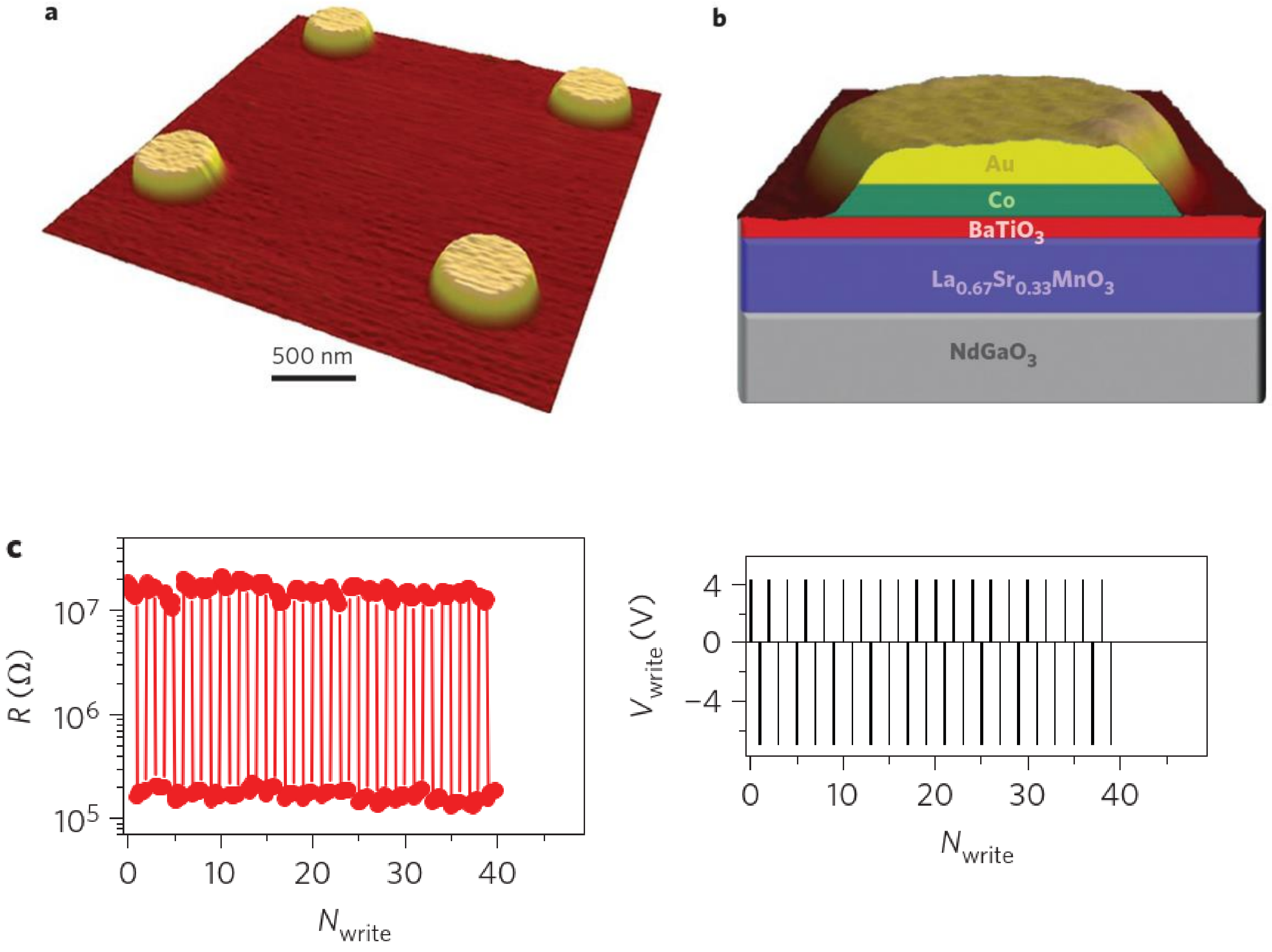
Energy consumption FTJs

- 200 nm devices contacted by conductive AFM
- $t_{write} = 10\ ns$ write pulses at 4 V.

→ $E = t_{write} * V_{write} * I = 130\ fJ$

- For 50 nm devices → E ~ 10 fJ/bit

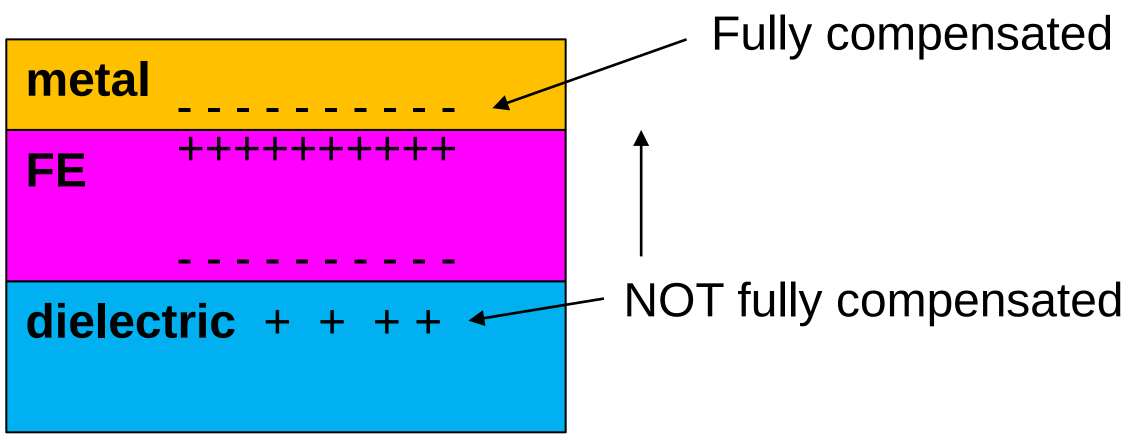
- Why?
  - Purely electrostatic writing
  - No filament formation
  - No phase change
  - Not current-induced (like STT)



Chanthbouala et al Nat. Nano 2012

Retention in FE memories - Depolarization field

- If the surface surrounding the ferroelectric material cannot supply the charge to completely compensate the polarization charge → depolarization field
- Acts to depolarize → reduces retention
- Any interfacial layers will lead to a depolarization field



$$E_{dep} = -\mathrm{P}\left[\varepsilon_0 \varepsilon_{FE}\left(\frac{C_{di}}{C_{FE}} + 1\right)\right]^{-1}$$

- Want $C_{di} \gg C_{FE}$ to minimize depolarization field

→ $\varepsilon_{di} \gg \varepsilon_{FE}$, and $t_{di} \ll t_{FE}$

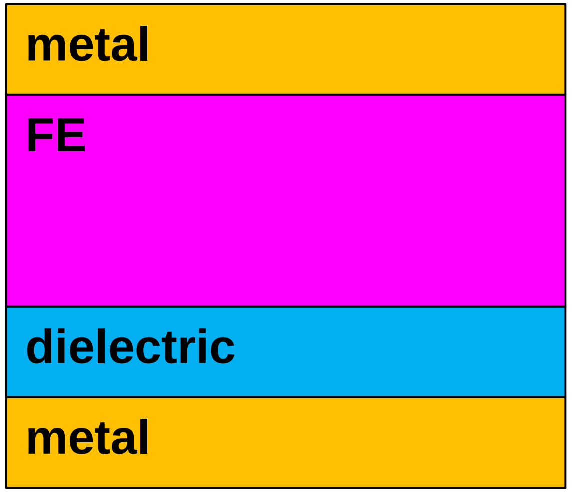
Ma et al. IEEE EDL 2002

2 min exercise – Magnitude of depolarization?

- How big is this compared to the critical field $\mathcal{E}_c$ of HZO (1.5 MV/cm)
- What will be the impact on retention?

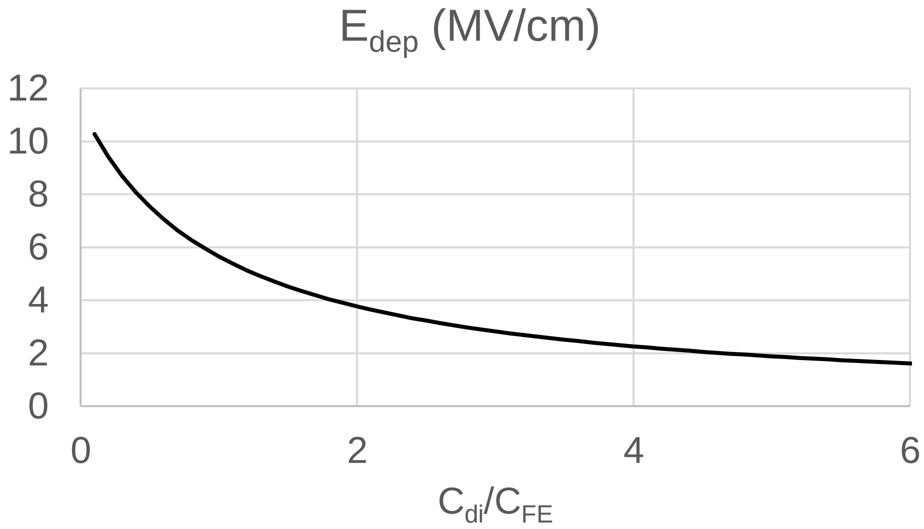
$$E_{dep} = -\mathrm{P}\left[\varepsilon_0 \varepsilon_{FE}\left(\frac{C_{di}}{C_{FE}} + 1\right)\right]^{-1}$$

$$P = 20\ \mu C/cm^2$$
$$\varepsilon_0 = 8.83 * 10^{-14}\ F/cm$$



$t_{FE} = 10\ nm$
$\varepsilon_{FE} = 20$

$t_{di} = 1\ nm$
$\varepsilon_{di} = 10$

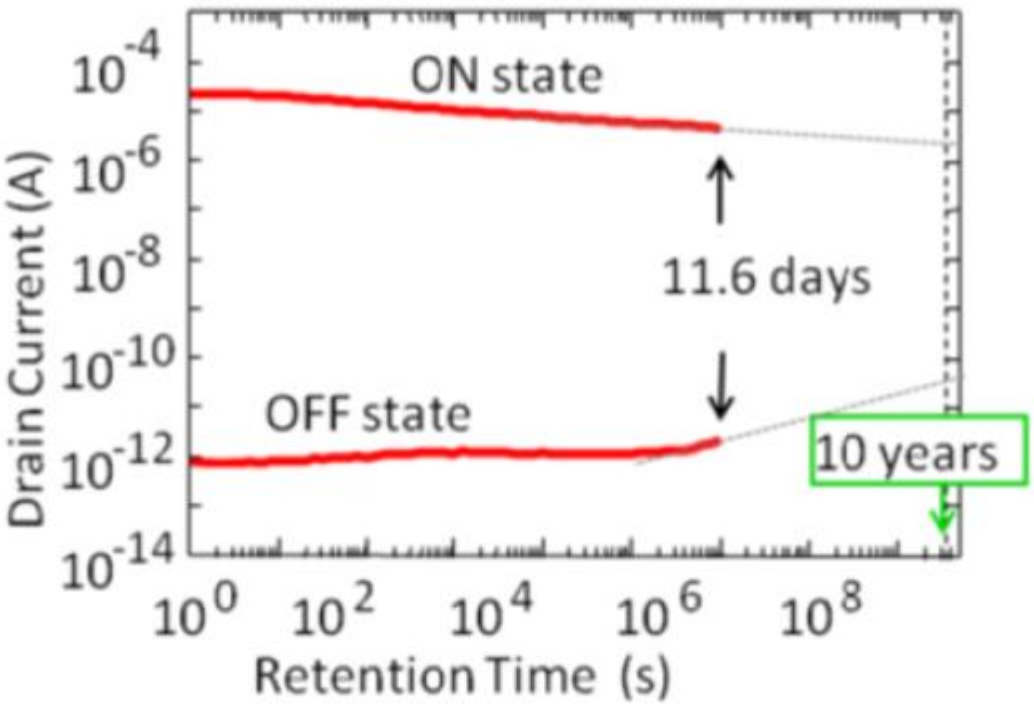


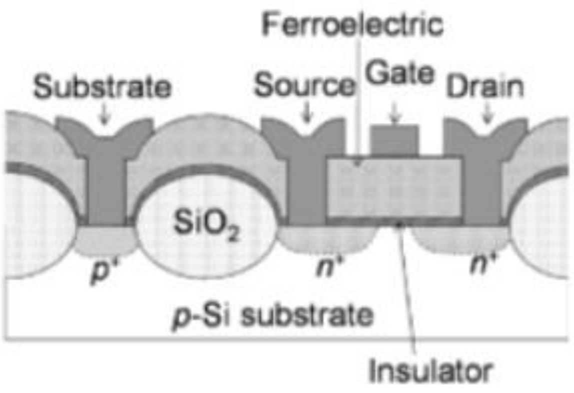
Achieving 10 year retention

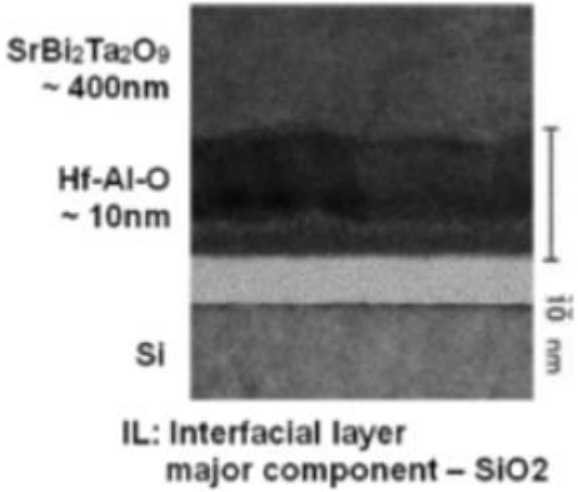
$$\varepsilon_{SBT} \sim 110,$$
$$\varepsilon_{HfAlO_2} \sim 11$$

$$\frac{C_{HAO}}{C_{SBT}} = \frac{\frac{11}{10\ nm}}{\frac{110}{400\ nm}} = 4$$

- A matter of optimizing the layer stack, achieved in 2004
- 400 nm SBT + 10 nm $HfAlO_2$
- But not scalable! **WHY?**

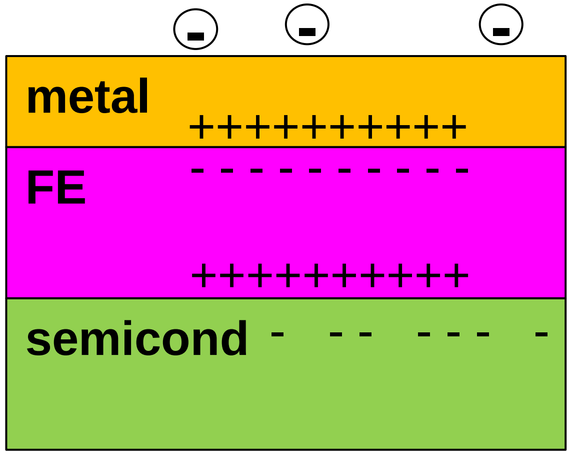


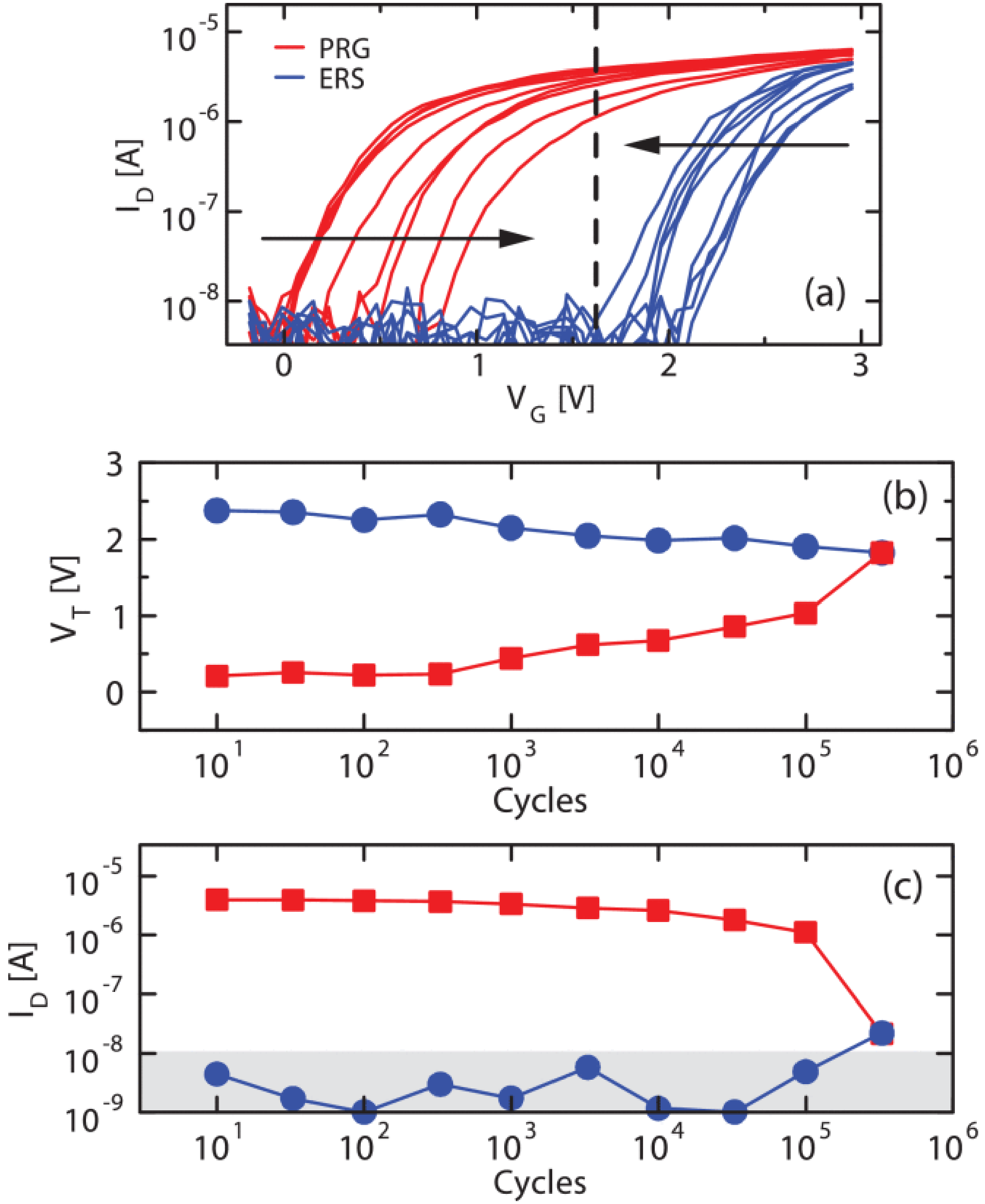




Endurance

- With each write cycle the memory window shrinks
- Due to high-voltage cycling
  - creation of additional charges in oxide (screening of P charge)
- Particularly difficult for FeFETs
  - devices demonstrated up to 10^5 cycles



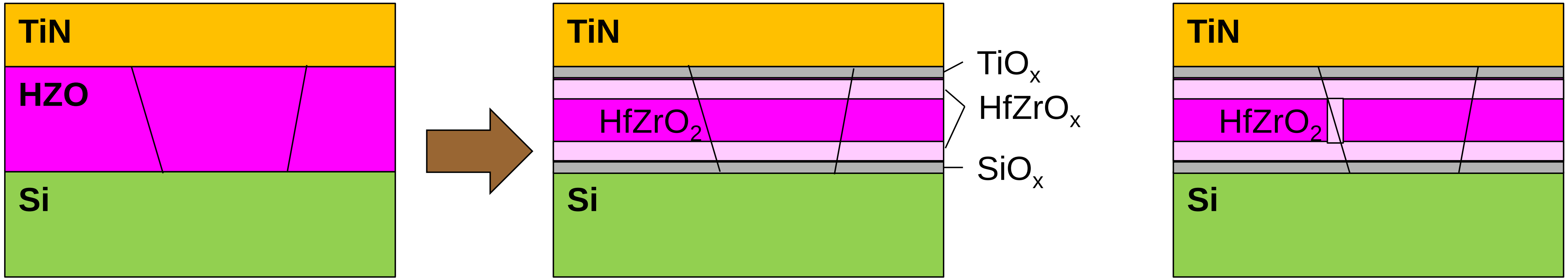


Mulaosmanovic et al. IEEE Trans. Electron Dev. 2019

Cause of endurance failure

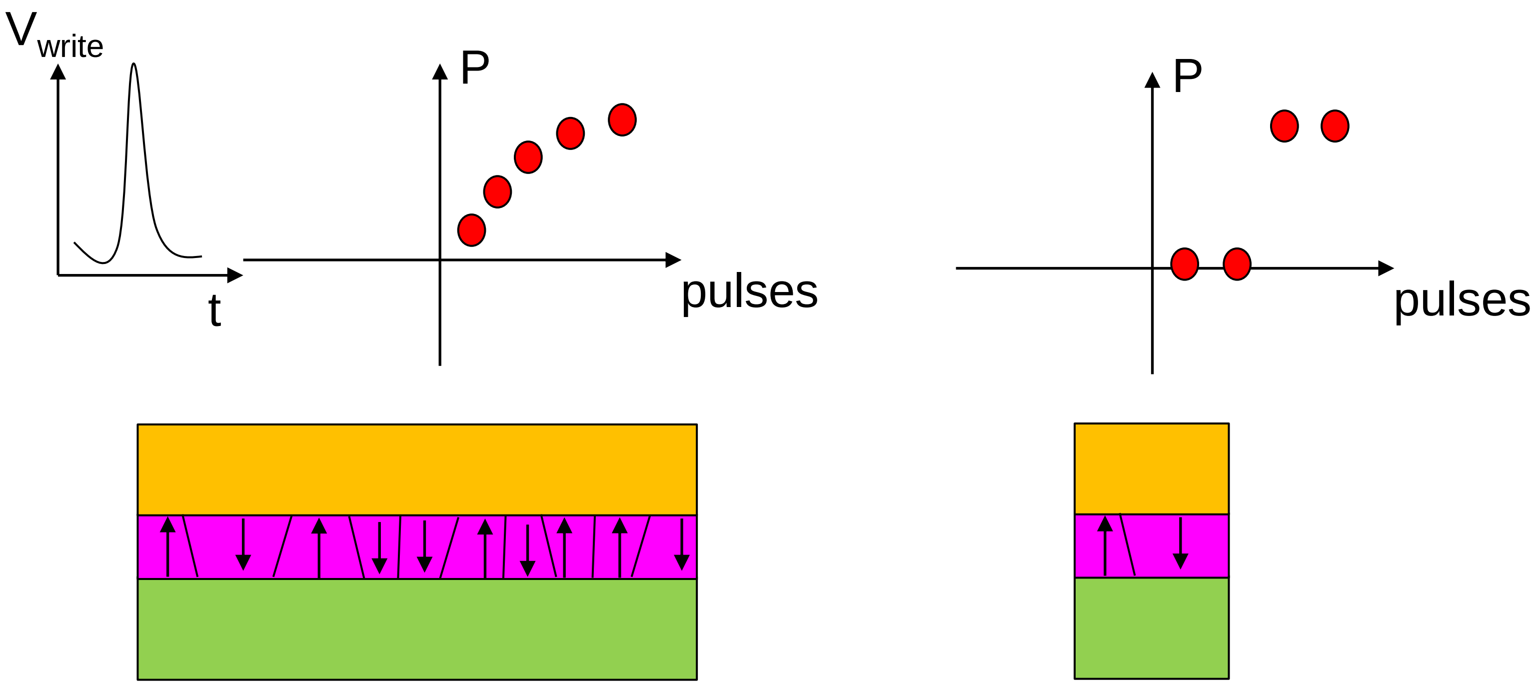
- The interface quality is vital!

- Diffusion across interfaces
- Non-switching low-k interface layers → voltage division
  - High voltage drop → more defects → layers continue to grow → less voltage over FE layer
  - Also: V_O formation/diffusion → ReRAM effect in grain boundaries! → BREAKDOWN!



Multibit operation??

- Possible in large devices (multiple domains)
- Nanoscale devices (1-few domains) → binary devices

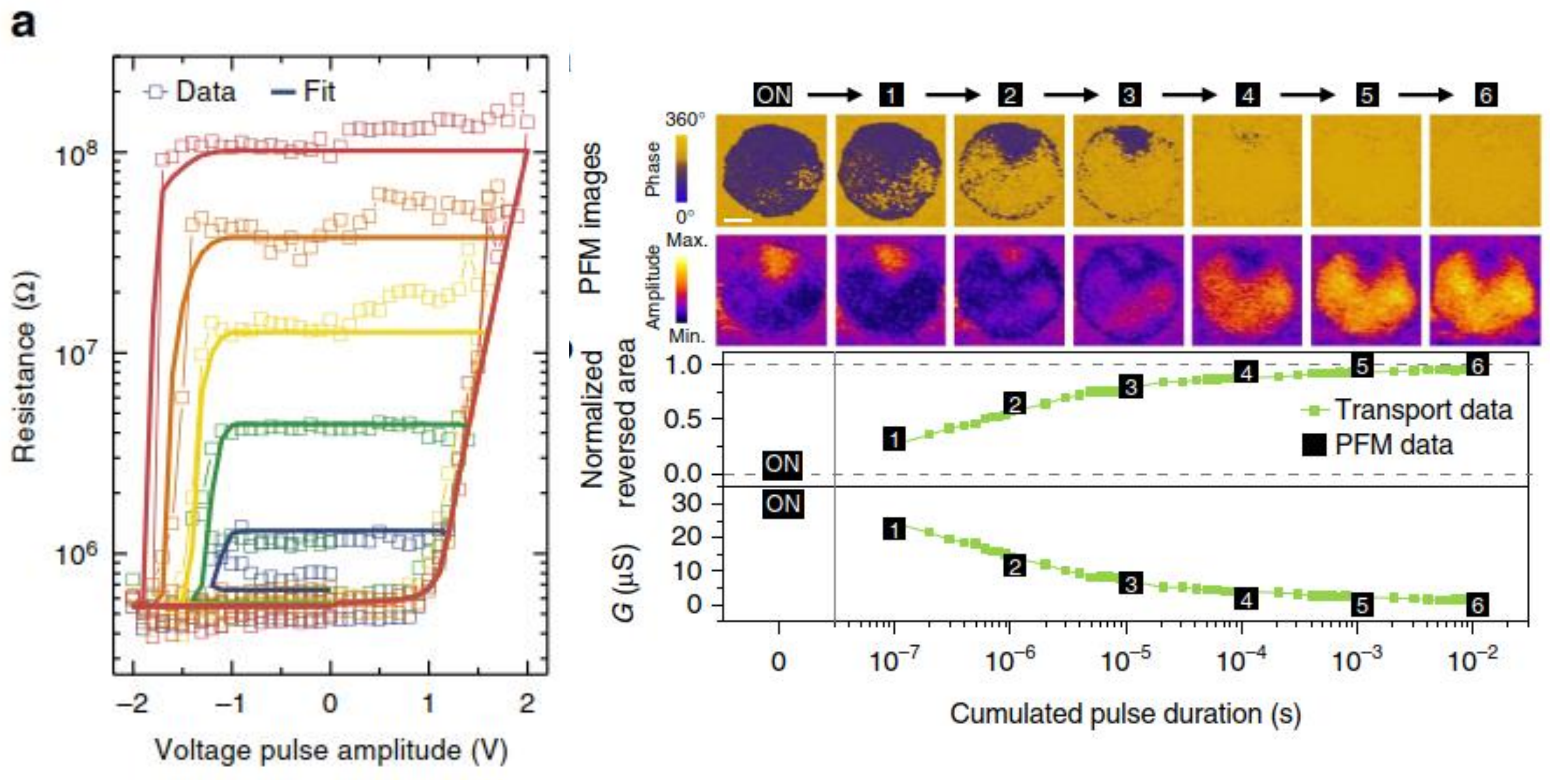


Inhomogeneous FE switching

- $BeFeO_3$ ferroelectric
  - Domain size < 10 nm
- 150 nm diameter devices
  - Scaled but still lots of domains

- FE switching nucleation-dominated
  - New domains rather than extending

- Can enable memristor behavior in FTJs



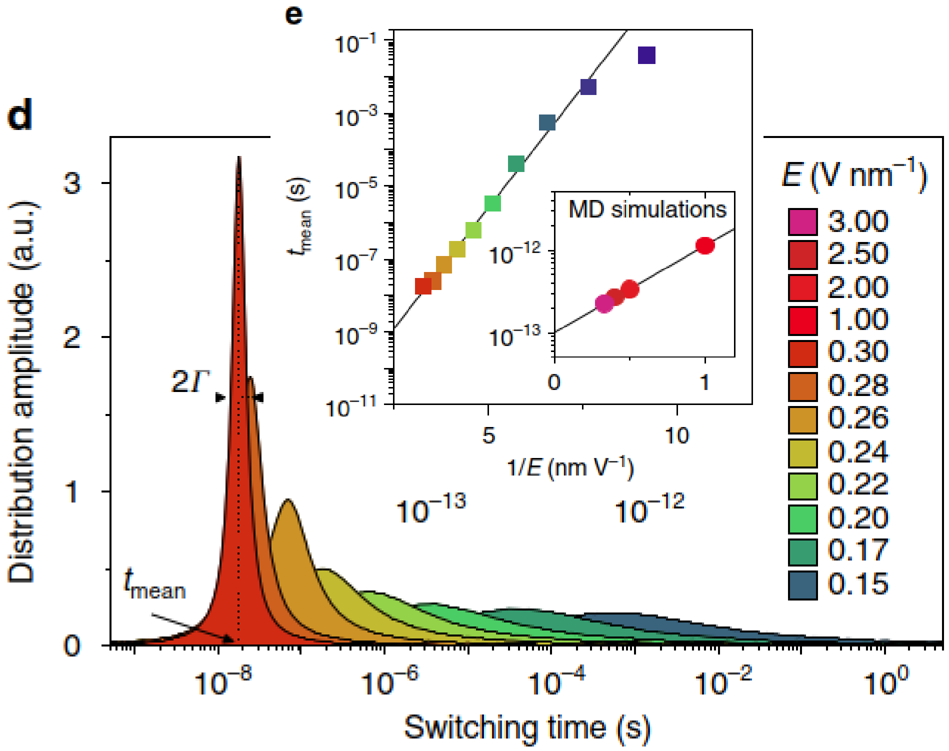
$$G = (1 - \mathrm{S})\mathrm{G_{on}} + \mathrm{SG_{off}}$$
where *S* is fraction of area with reversed polarity

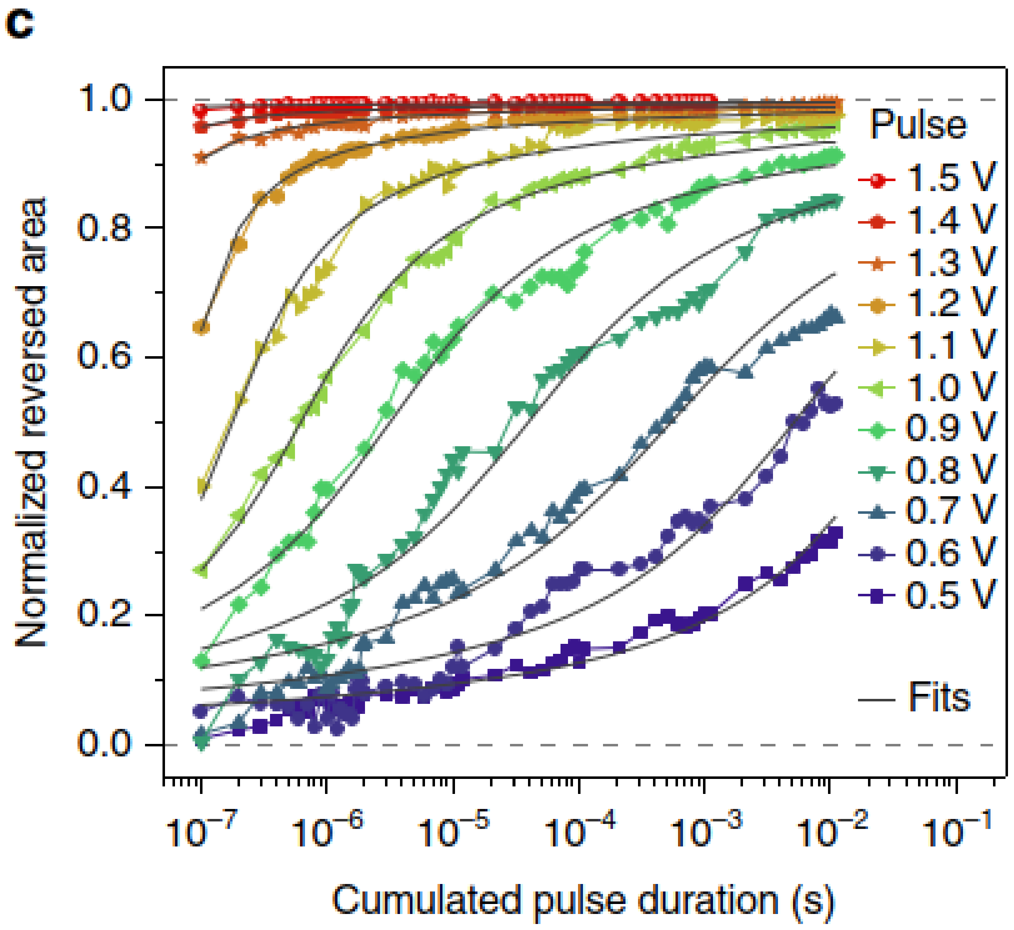
Boyn et al. Nature Comm. 2017

Domain switching time

- Lorentzian distribution of log($t_{mean}(V)$)
  - Lower E → longer time until switch

$$S_{\pm}(t, V) = \frac{1}{2} \mp \frac{1}{\pi} \arctan \frac{\log(t_{\text{mean}}(V)) - \log(t)}{\Gamma(V)}$$



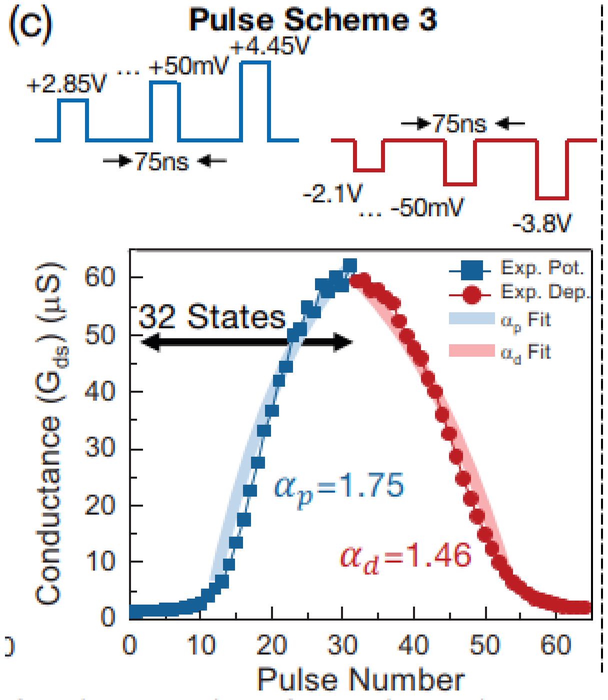


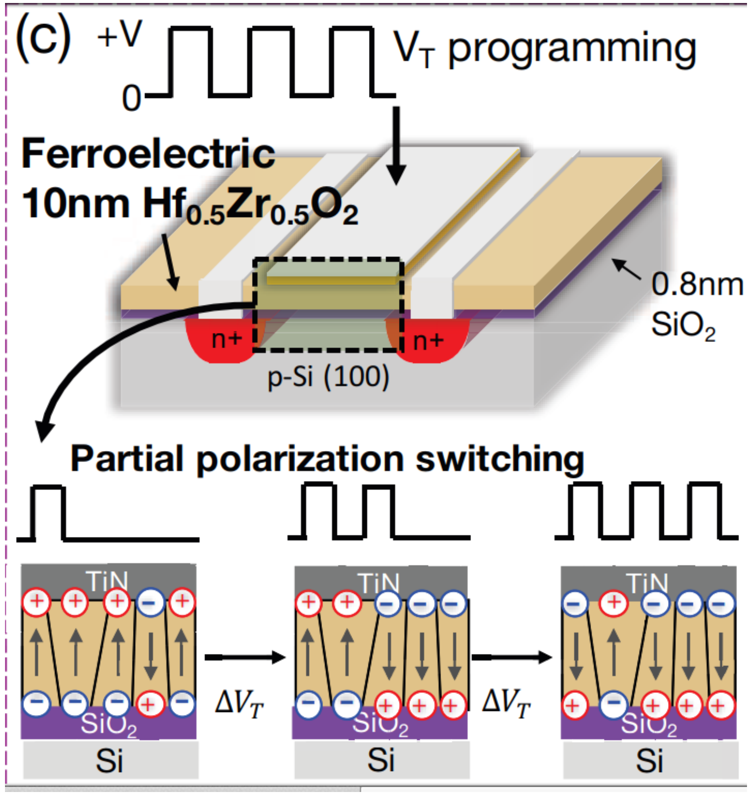
Ferroelectrics as storage

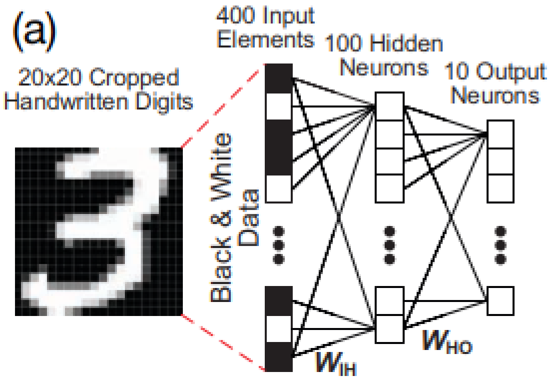
	DRAM	3DNAND	RRAM	PCM	STT-MRAM	Ferro
Nonvolatile	No	Yes	Yes	Yes	Yes	Yes(?)
Speed (ns)	10	10^4	< 5 ns	10 ns	< 5 ns	< 5 ns
Energy use (pJ/write)	0.1	1	0.1-1	>1	< 0.2 pJ	0.01 (!)
Endurance (cycles)	10^{16}	10^5	10^6-10^7	10^9	>10^{15}	10^5-10^{12}
Multilevel?	No	Yes	3-6 bit	4 bit	No	Yes(?)
Scalability	6-8F^2	3D!	3D!	3D!	6F^2	4-6F^2, 3D
Other	Destructive Read	High Voltage	Abrupt SET	R drifts	Scaling limited by needed current	Depolarization a challenge No multilevel when scaled?

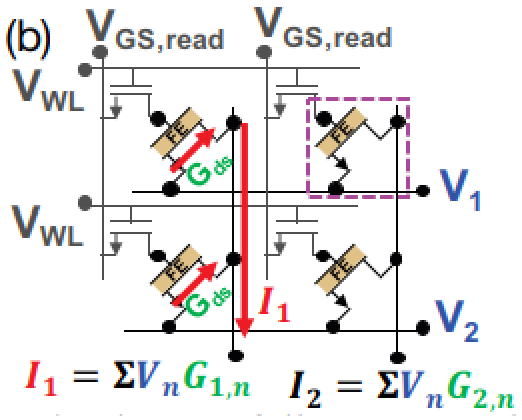
FeFET synapse

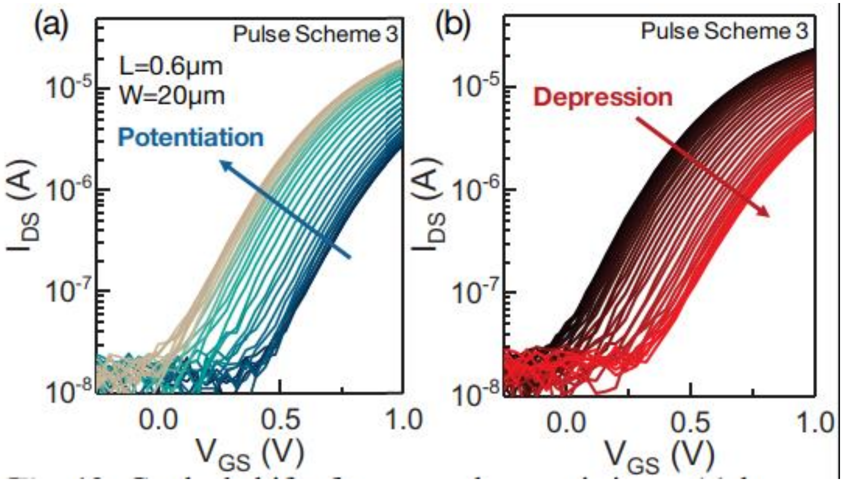
- Based on partial polarization switching
- Pulse scheme with varying amplitude used → symmetric LTP/LTD
- R_{off}/R_{on} ~ 45, "5 bit" precision
- Tested with peripherals on MNIST numbers → 90% accuracy at 35 µW
  - 10x area saving, > 30x less leakage power comp. with SRAM







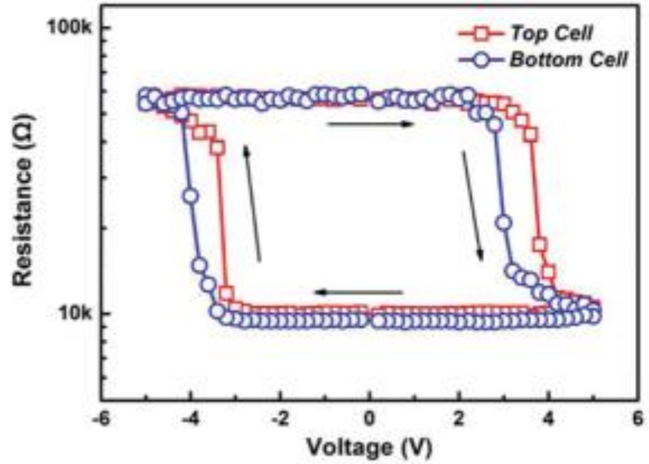


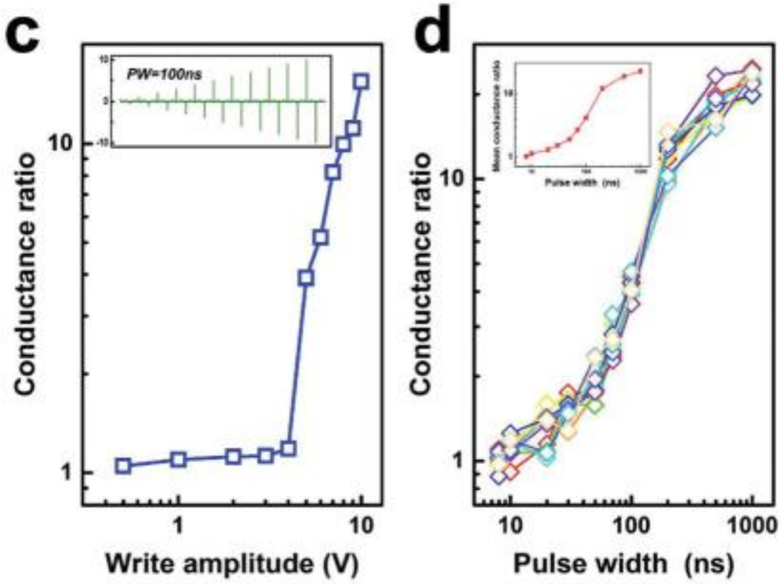


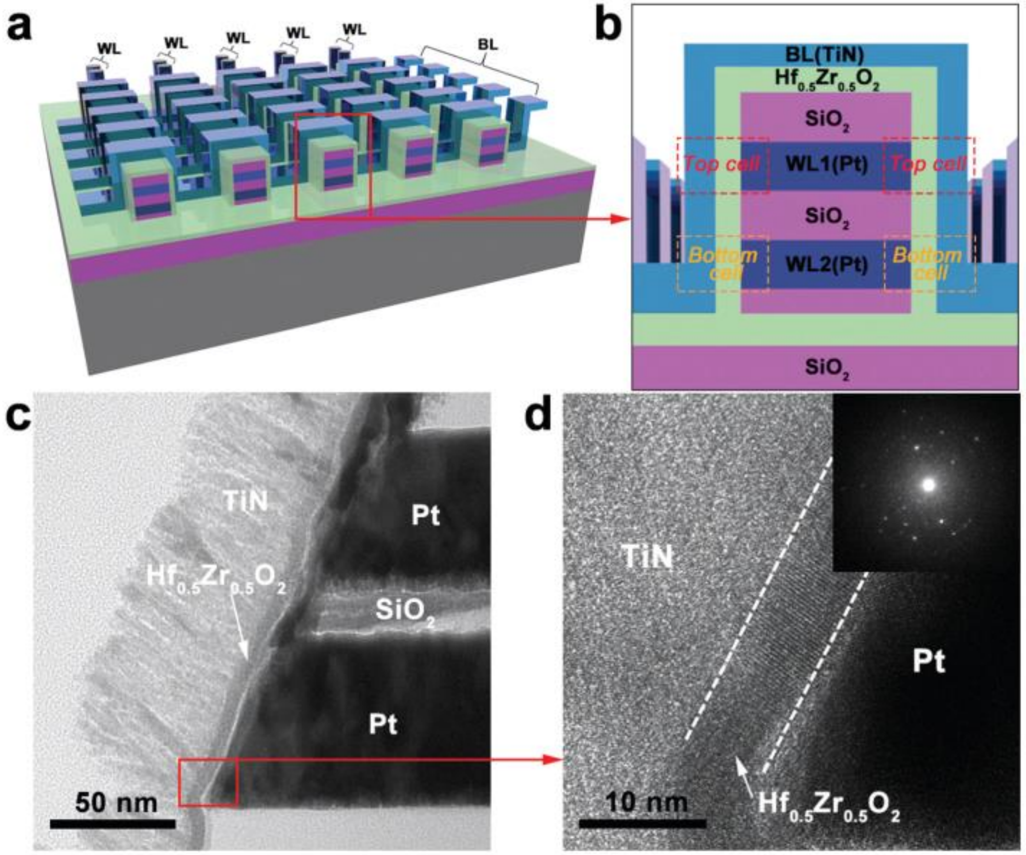
Jerry et al. IEDM 2017

FTJ synapses

- 3D stacked FTJs implemented with HZO ferroelectric
- Control of resistance state by V_{write} and t_{write}
  - Exponential change…



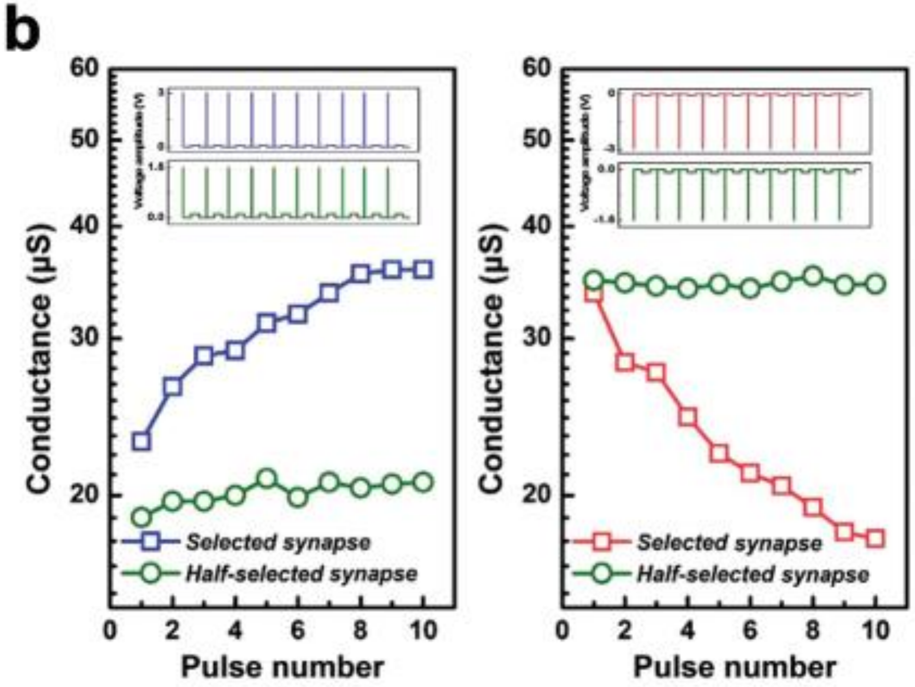


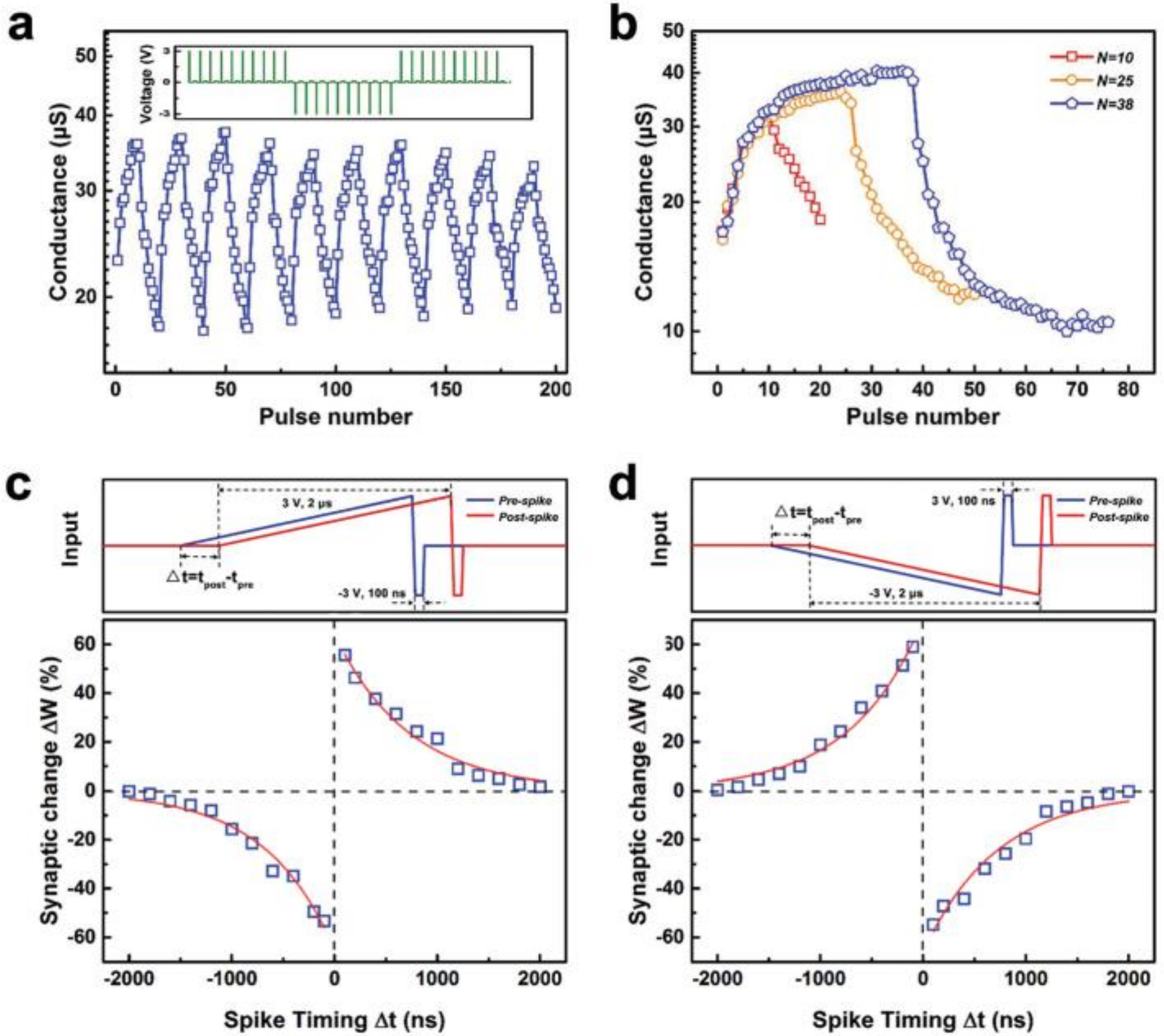


Chen et al. Nanoscale 2018

Weight change in FTJ

- LTP and LTD possible, 1.8 pJ/spike (2.5 µm^2)
- Rather non-linear behaviour,
  more linear if not using full range
- STDP functionality is viable
- Selector-free operation is possible → 4F^2





Summary

- Ferroelectricity → purely electronic effect (robust)
  - Promise of extreme energy efficiency: < 10 fJ/bit
- Three types of memories
  - FeRAM (stable but not scalable, destructive read)
  - FeFET (drop-in tech, challenging retention)
  - FTJ (new, two-terminal)

- FeFET and FTJ promising for synapse devices