Written Examination EITP25

June 4th 2020

Useful constants:

$$\hbar = 1.055 \times 10^{-34}\ Js$$

$$k_B = 1.381 \times 10^{-23}\ J/K$$

$$m_0 = 9.109 \times 10^{-31}\ kg$$

$$\varepsilon_0 = 8.85 \times 10^{-12}\ Fm^{-1}$$

$$e = q = 1.602 \times 10^{-19}\ C$$

$$c = 2.998 \times 10^{8}\ m/s$$

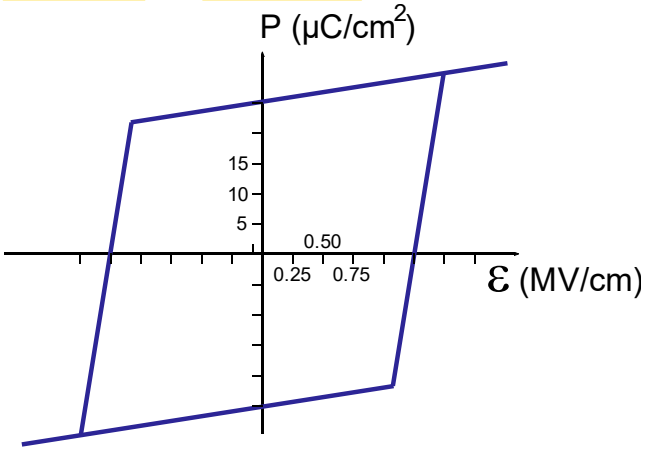
Solve the Five tasks below. Maximum score is 60p.

1. Spiking Neural Networks (SNN) (12p)

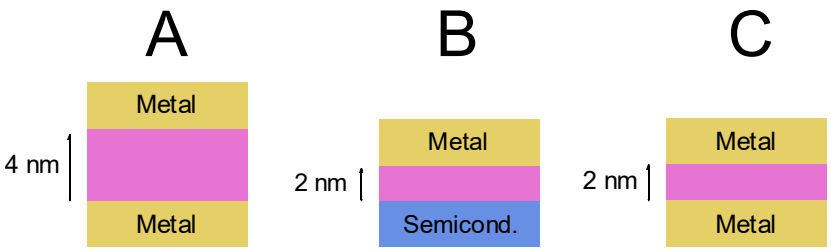
a. Explain what makes an SNN so much more energy efficient compared to a regular artificial neural network.
b. What is Spike-Time-Dependent Plasticity (STDP) and how does one implement it in an memristor-based SNN?
c. Explain how STDP achieves stable neuron output activity level given an excessive and random input activity.

2. Ferroelectric devices (12p)

a. In the following diagram measured on a FERAM device extract the remanent polarisation and coercive field.



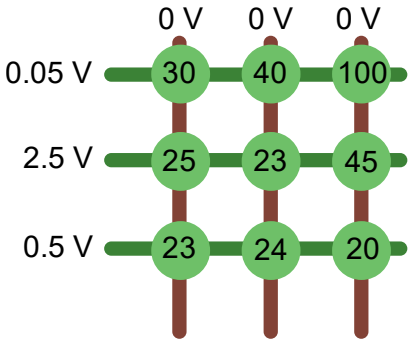
b. Rank the following FTJ devices in terms of their resistance contrast (R_{high}/R_{low}):



c. Given a FeFET with a 10 nm $HfZrO_2$ ferroelectric gate oxide ($\varepsilon_r = 20$) and $\mathcal{E}_c = 1.5\ MV/cm$. Defects at the interface to the semiconductor results in a series capacitance of 5 µF/cm^2. Using the following expression for the depolarisation field $E_{dep} = -\mathrm{P}\left[\varepsilon_0\varepsilon_r\left(\frac{C_{series}}{C_{FE}}+1\right)\right]^{-1}$ calculate the remanent polarisation in the device.

3. ReRAM and MRAM (12p)

a. An 8-bit ReRAM memristor array is programmed to the following conductance values and word line voltages (bit lines are grounded):



What will the current on each bit line be, and what linear matrix equation does this situation map to? What is the solution to the equation?

b. Describe what happens on a microscopic scale during FORMING, SET and RESET operations in a ReRAM device based on valence-change.

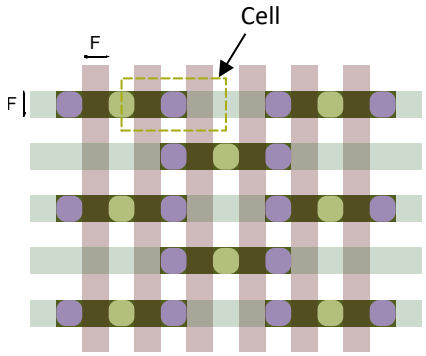
c. Name and explain the three key physical mechanisms that has enabled MRAM as a viable technology?

4. Integration (12p)

a. Given a large memory array, if the device furthest from the WL bias source is selected, name and explain two potential issues and how to solve them.

b. What are the important characteristics of selector devices to be used for an array of PCM or FeFET memory cells, respectively? Explain why.

c. Assume a DRAM technology with where each DRAM cell looks like this with F = 30 nm:



Assuming a chip size of 50 mm^2 and area efficiency of 50%, how high memory capacity does the chip have?

5. Neuromorphic technology (12p)

a. Rank the following non-idealities of a memristor device in terms of their negative influence of the training performance of a SNN (worst comes first):
    1. Non-linear potentiation/depression
    2. Asymmetric potentiation/depression
    3. Cycle-to-cycle pot./dep. Variation
    4. Dynamic range

b. Using a 2-PCM device one can achieve a negative synaptic weight. How do you operate such a device considering that SET can be gradual but RESET is abrupt for PCM?

c. Draw a circuit that implements a Leaky Integrate-and-Fire Neuron.

Good Luck!