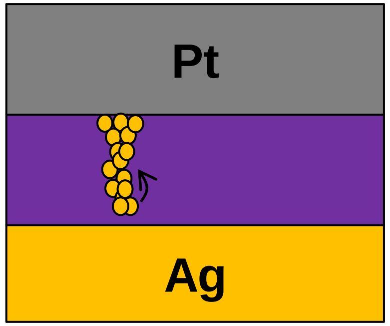
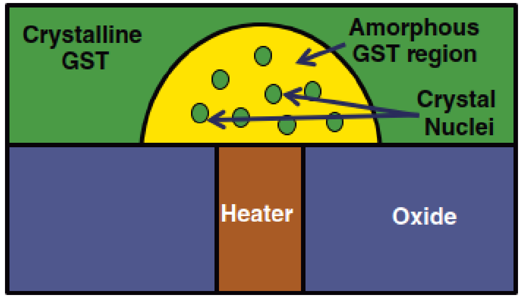
EITP25 2020

# Lecture 12 – Neuromorphic device in reality

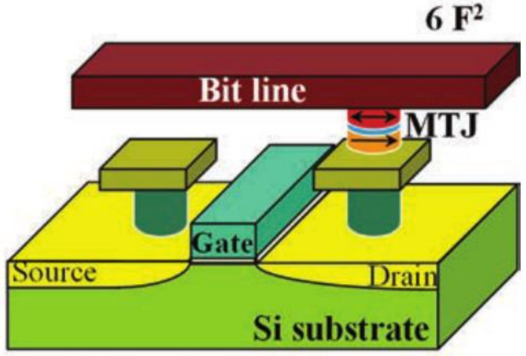
# Self-summary of memory technologies



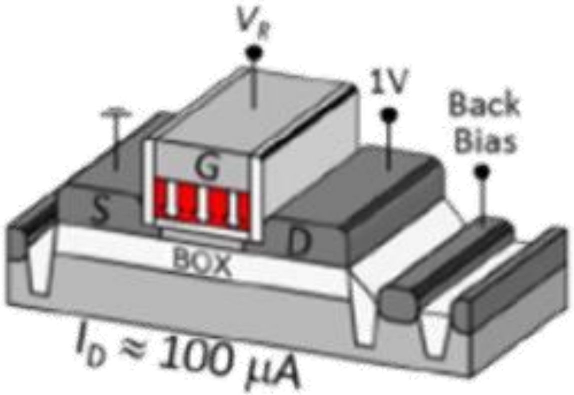

Group 1: ReRAM




Group 2: PCM




Group 3: STT-MRAM




Group 4: Ferroelectric memory

1. How does it work?
2. What is the best thing about the technology?
3. What is the biggest drawback of the technology?

5 min in subgroups (break-out rooms)
Each group answer questions for one tech → write in padlet

https://padlet.com/fovmester/2rpsy67bp41sibdt

# Outline – Lecture 12

- Requirements on synaptic devices
- Impact of variabilities
- Hardware neurons
- Make your own quiz question!

# The ideal synapse and reality of devices

Ideal synapse behavior

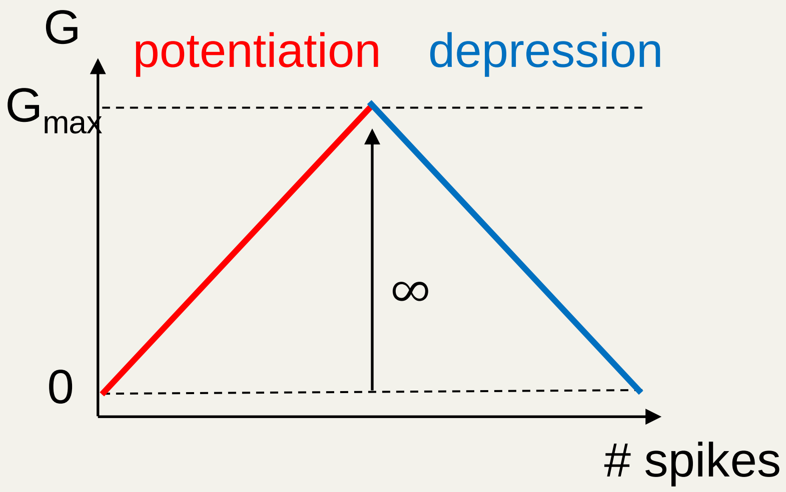
$$\Delta \mathrm{w} = \mathrm{constant}$$

$$\Delta \mathrm{w}_{0_+} = \Delta \mathrm{w}_-$$

$$G_{min} = 0$$

$$\frac{G_{max}}{G_{min}} = \infty$$

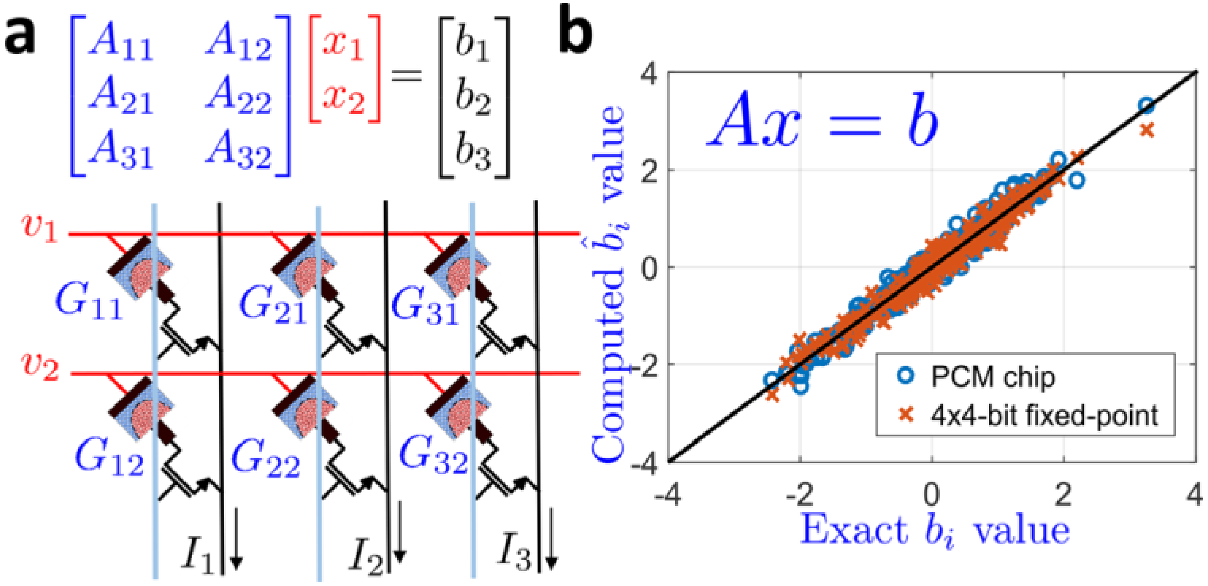
**Device variation = 0**

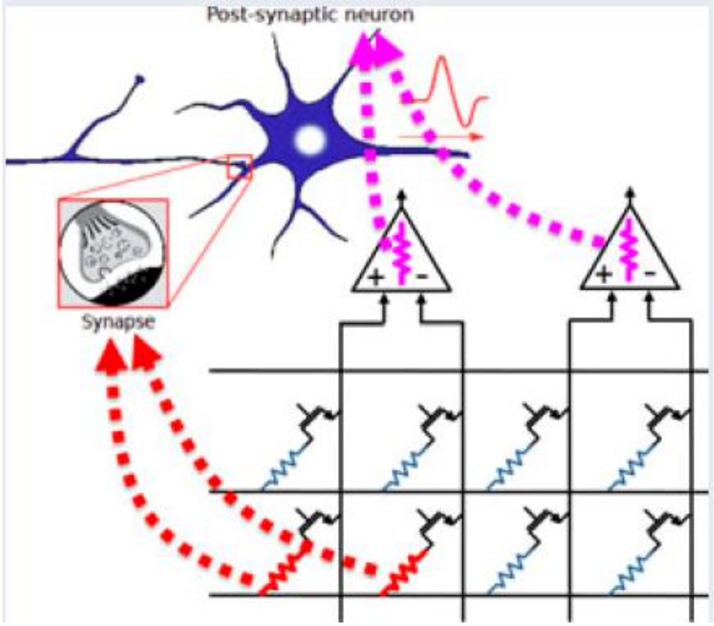



*Symmetric* + *linear*

# Negative weight

- Need to represent negative numbers in matrix operations!
- Conductance cannot be negative…
- 2 memristive devices + OP amp → synapse with symmetric weight



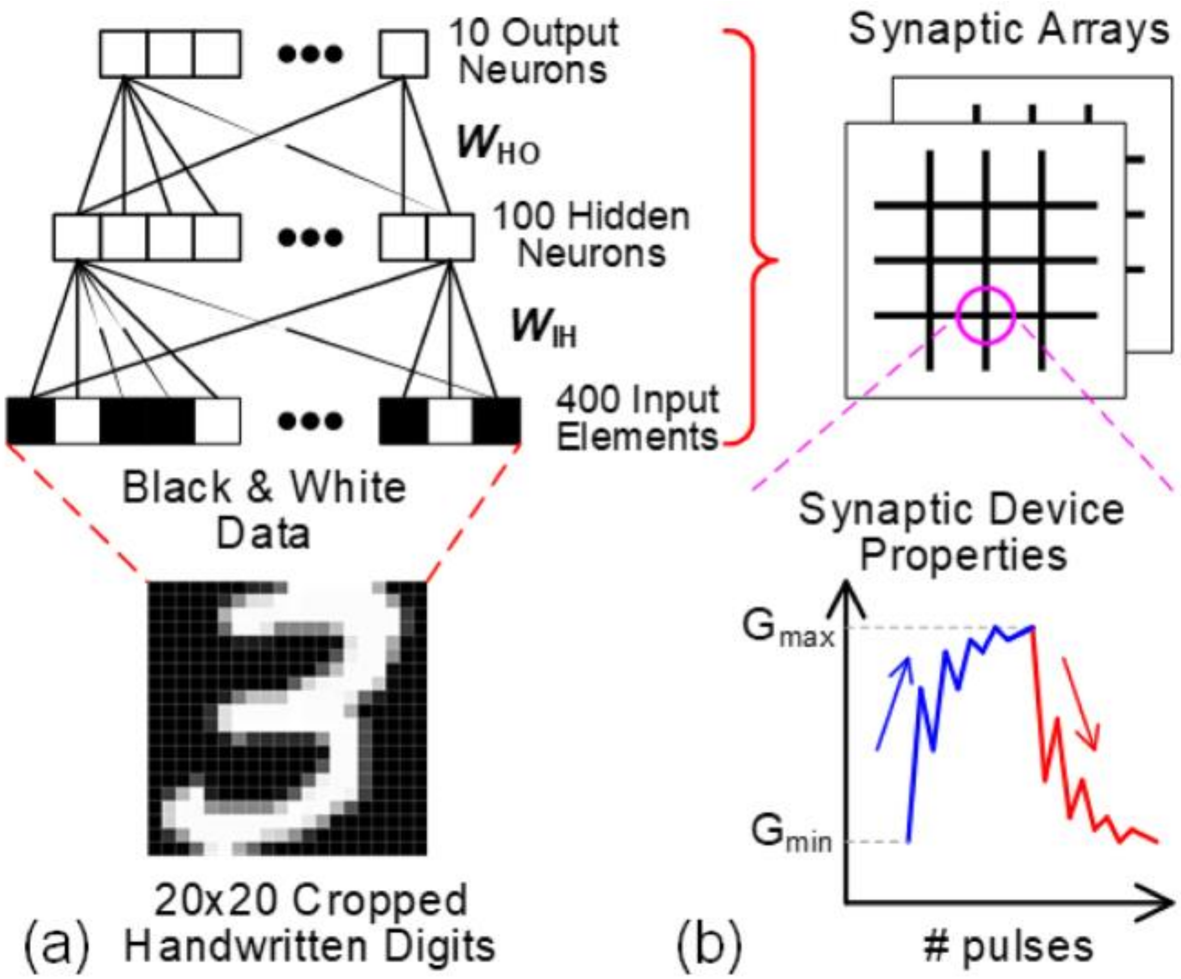




- Negative weights in neuromorphic?
  → Inhibitory synapses, but can be realized in other ways

*Burr et al. Adv Phys. X. 2017*

# The impact of synapse non-idealities on learning

- Using software NeuroSim
- In software → 96-97% accuracy



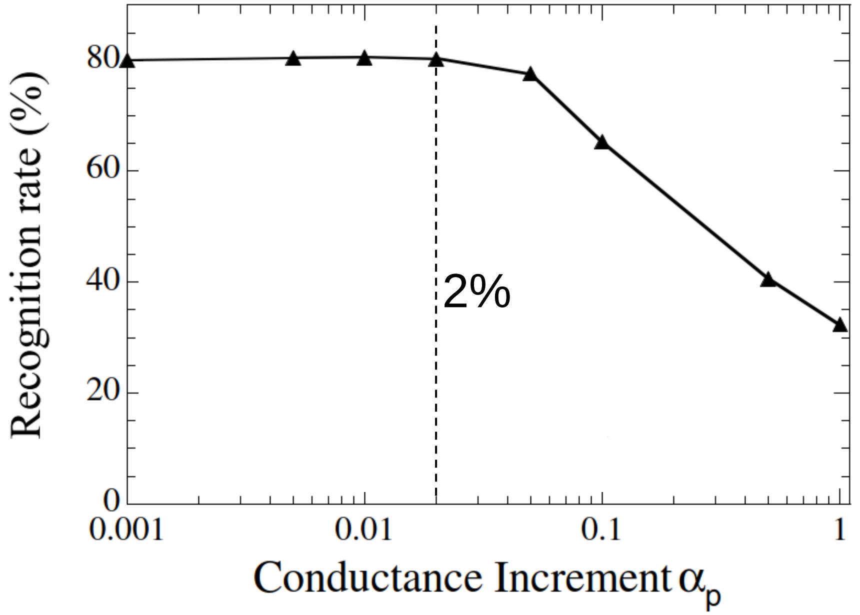

Islam et al. J Phys. D. 2019

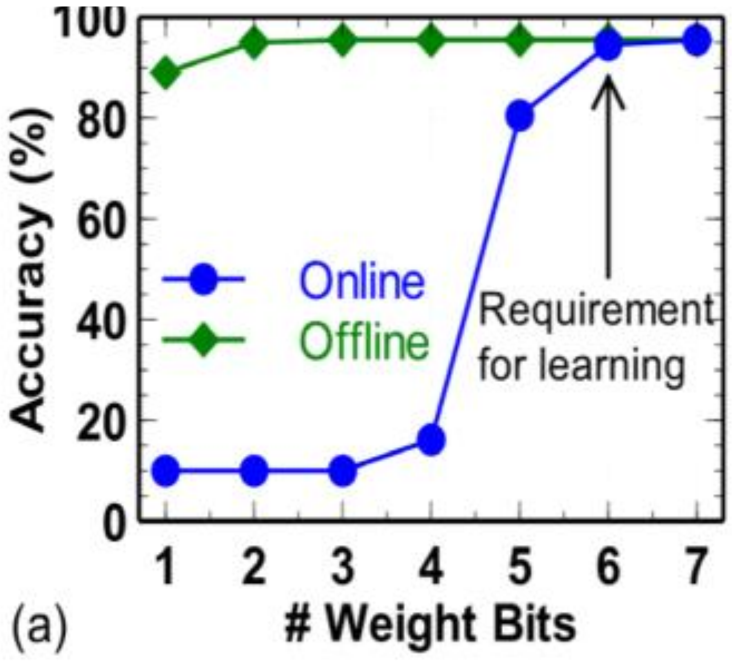
# Weight precision

- Weight updates at most 2% of Gmax
- → 1/0.02 = 50 states → 6 bit precision needed

- If only for inference 2 bit is enough!

- MRAM and scaled Ferroelectric thus cannot do it
- RRAM (4-6 bit) and PCM (4 bit) are getting close to sufficient



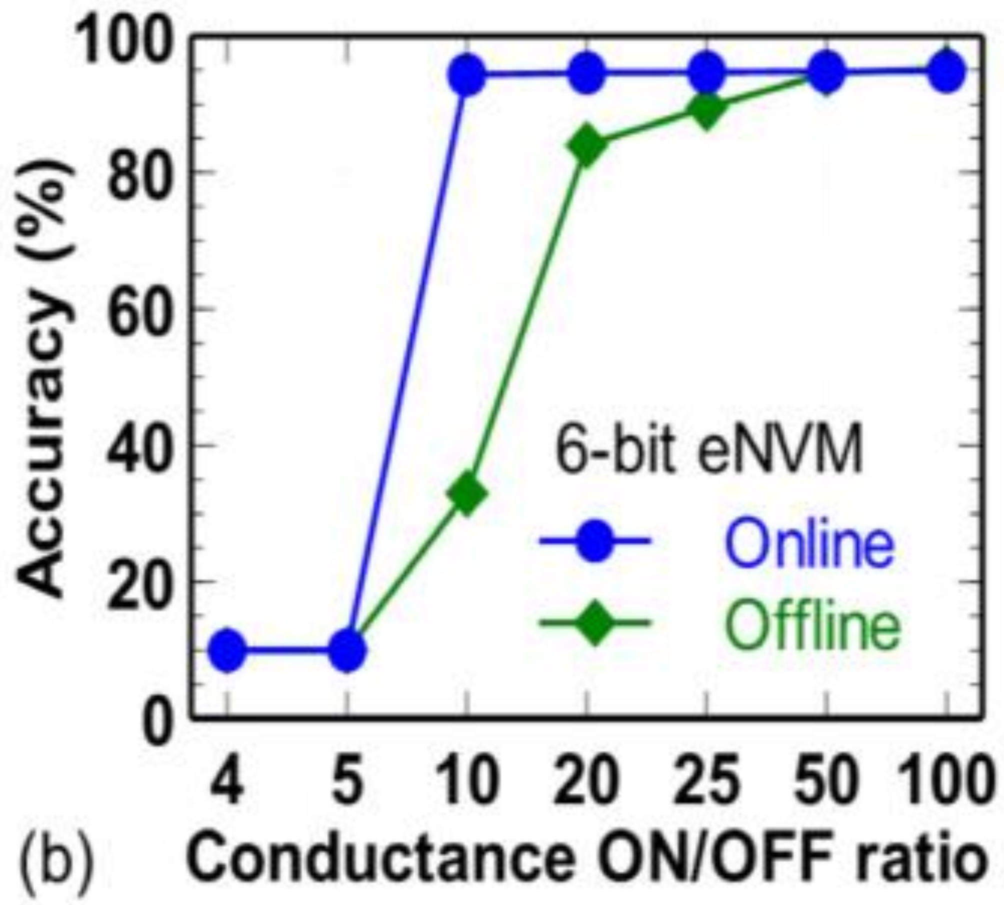

*Islam et al. J Phys. D. 2019, Querlioz et al. TNANO 2013*

# Dynamic range

- $R_{off}/R_{on}$ should be larger than 50 for inferencing
- On-line learning is more adaptable → $R_{off}/R_{on} > 10$

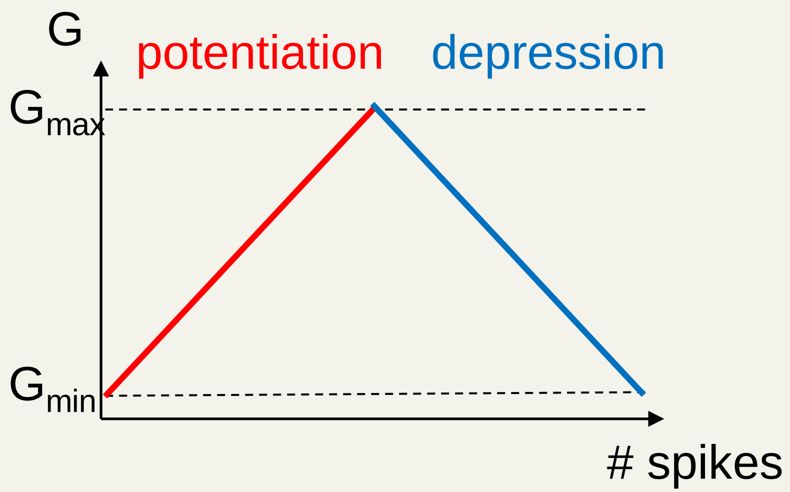
- One doesn't need extreme ratios!
- MRAM on/off ratio is very limited!

- Important that $R_{off}$ can represent zero level

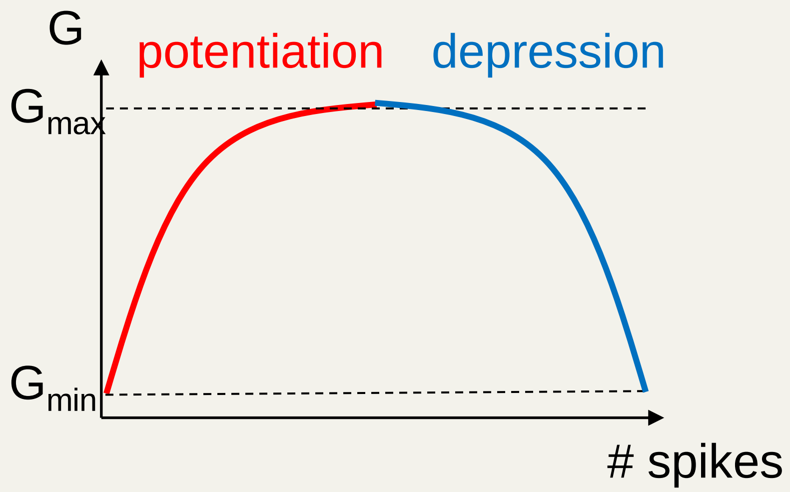



Islam et al. J Phys. D. 2019

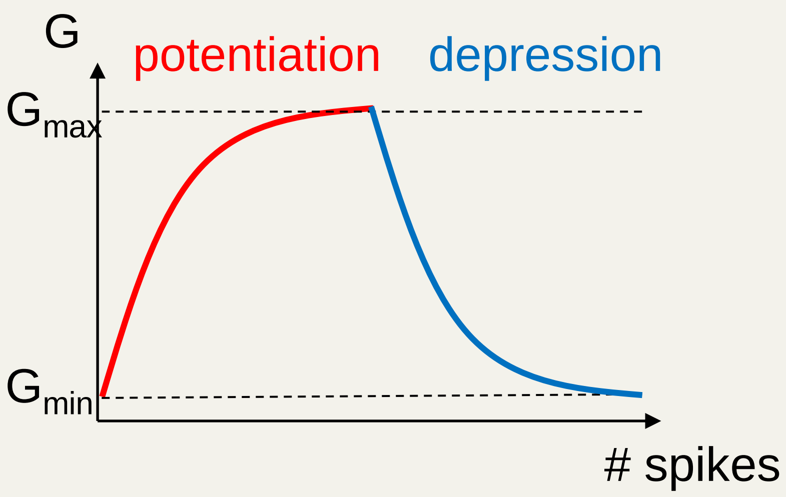
# Nonlinearity and asymmetry




*Symmetric* + *linear*



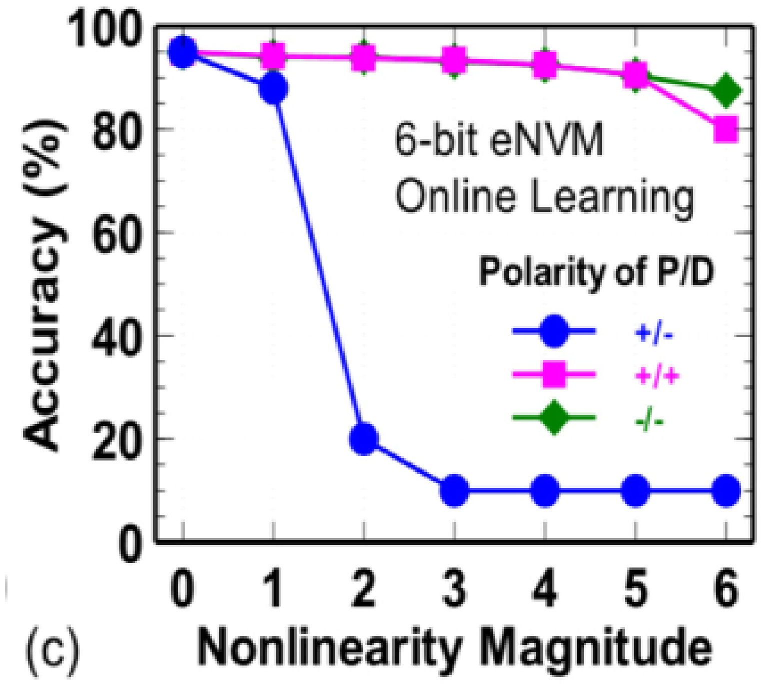

*Symmetric* + *nonlinear*

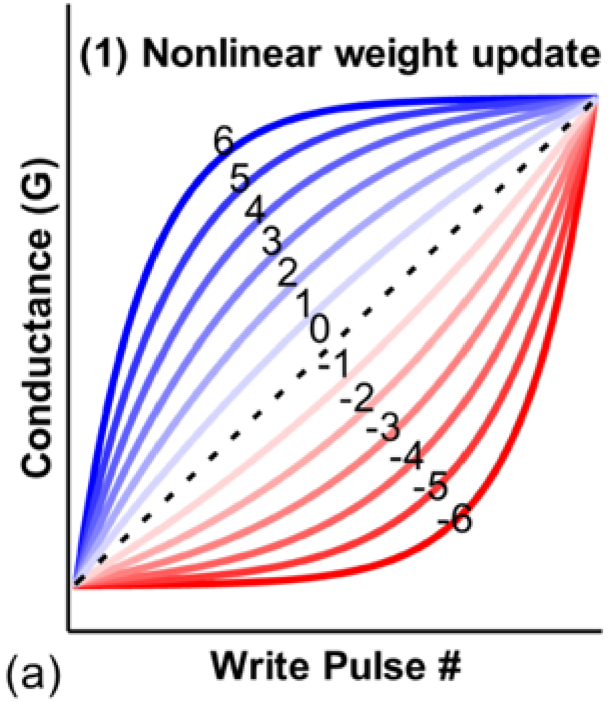


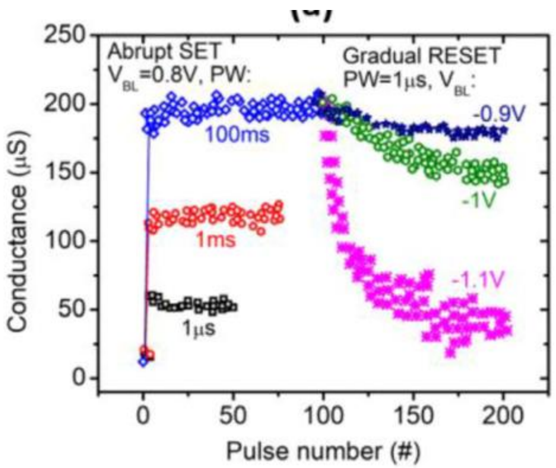

*Asymmetric* + *nonlinear*

# Impact of non-ideal weight change

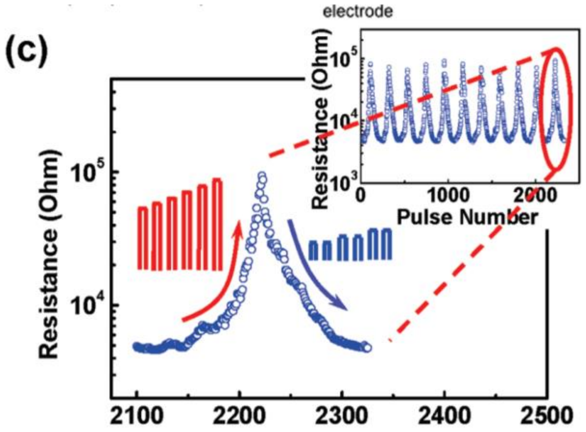
- Nonlinearity itself is not a problem unless very strong
- Asymmetry very quickly becomes problematic
  - Typical in real devices…



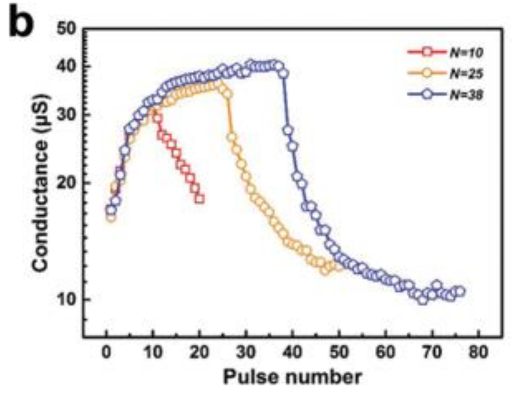




ReRAM



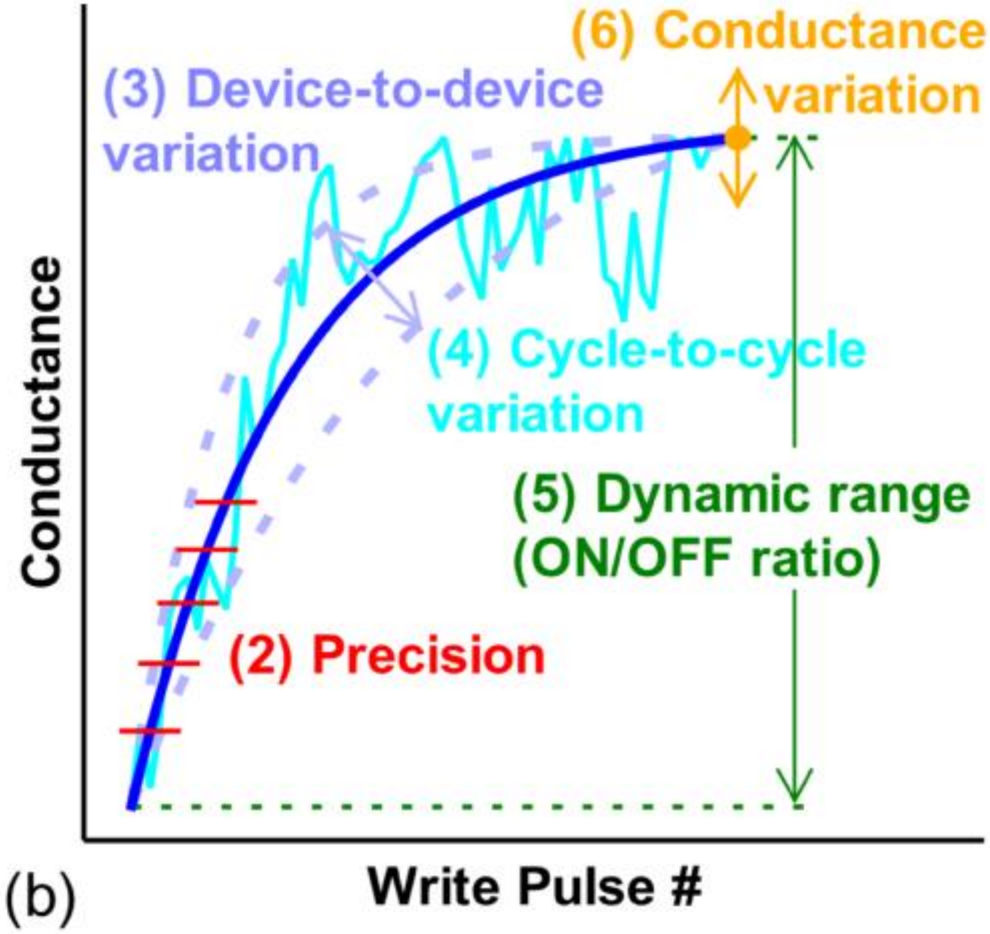

PCM




FTJ

Islam et al. J Phys. D. 2019

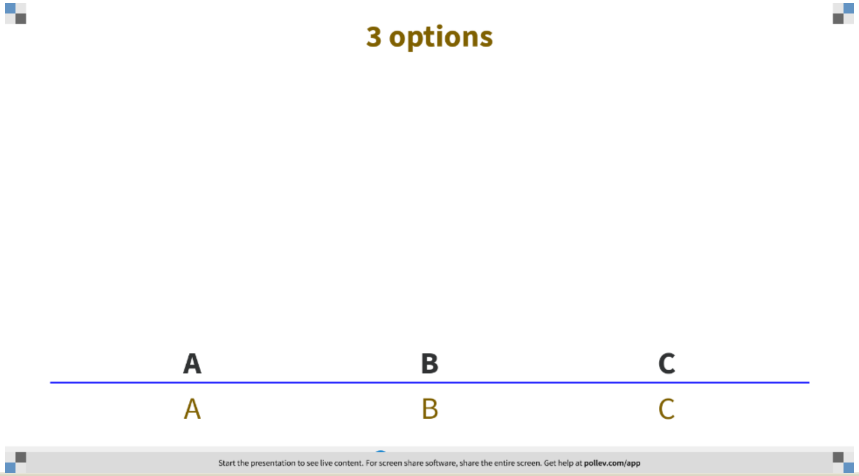
# Impact of variability?




**Which has the most negative impact on learning?**

A. Device-to-device variation
B. Conductance variation
C. Cycle-to-cycle variation

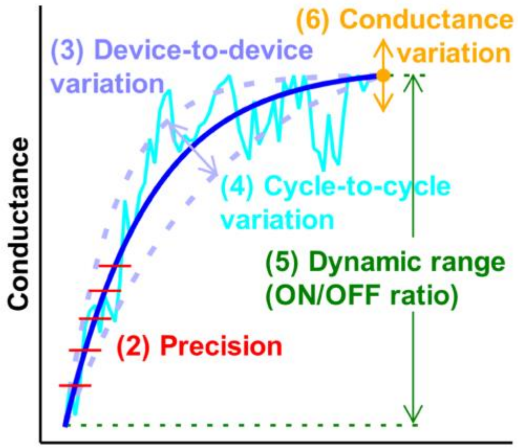
Go to PollEv.com/mattiasborg110



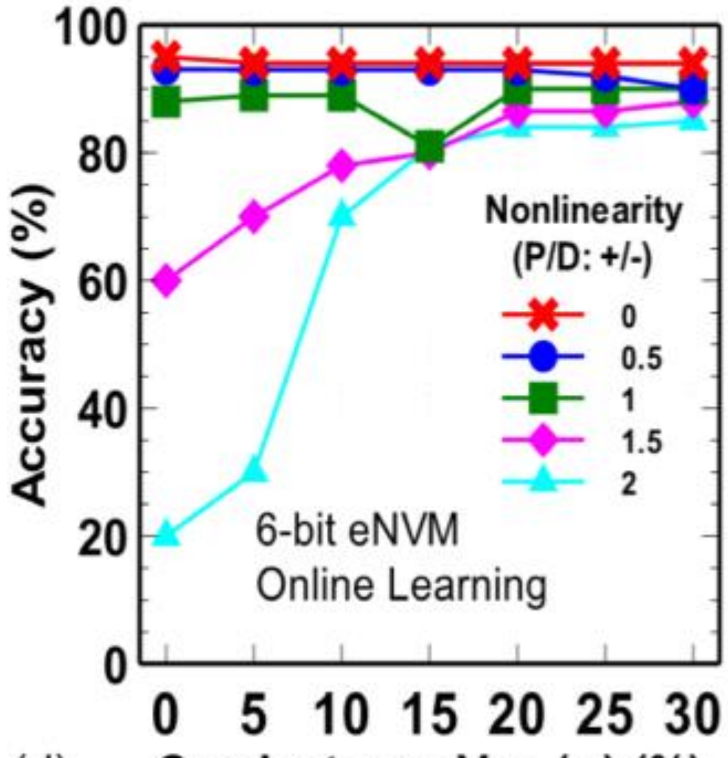
# Conductance variation (6)

- Variation in maximum conductance value → $\sigma$
- No negative impact!
- Even remedies negative impact of asymmetry!

- **Q: What is the implication of this?**




(b)



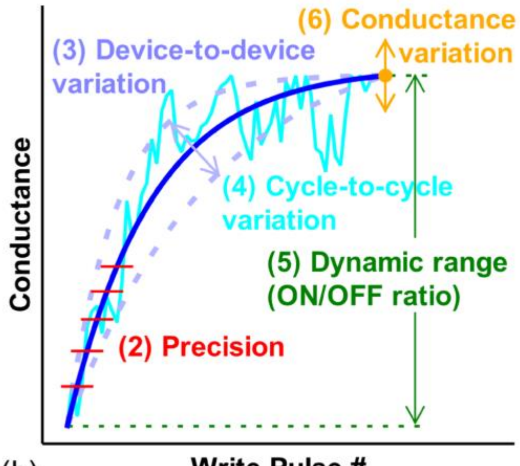

(d)

Islam et al. J Phys. D. 2019

# Impact of device to device variation (3)

- Variations in nonlinearity between devices is detrimental

- **Why?**



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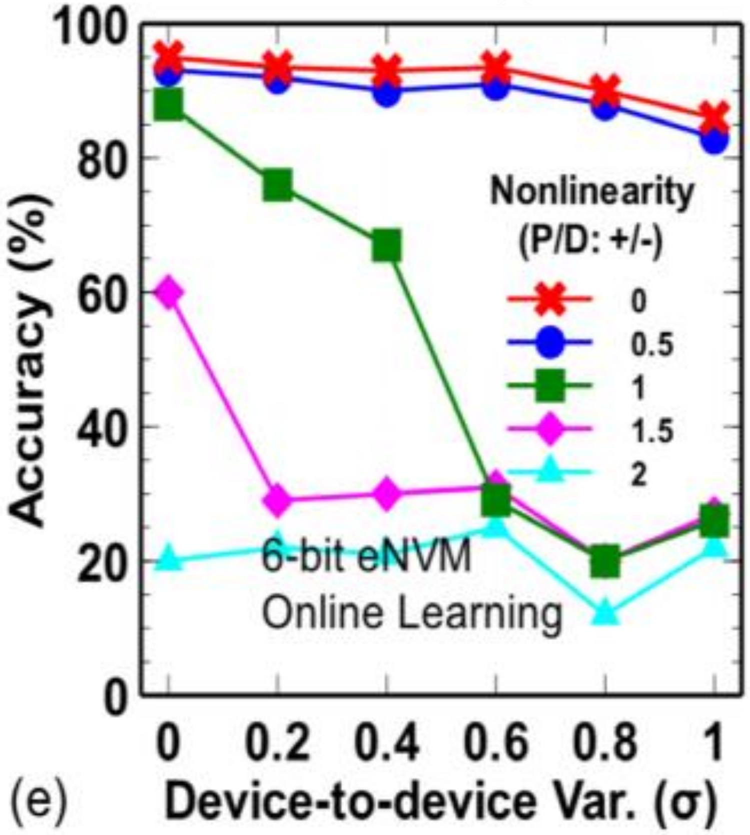
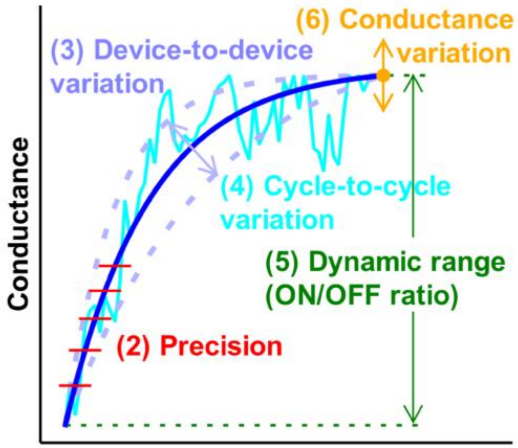


(e)

*Islam et al. J Phys. D. 2019*

# Cycle to cycle variation (noise, 4)

- Small amount of noise in weight update remedies effect of asymmetry
  - Helps to converge weights to optimal pattern
- Too high noise level obviously decreases performance overall.

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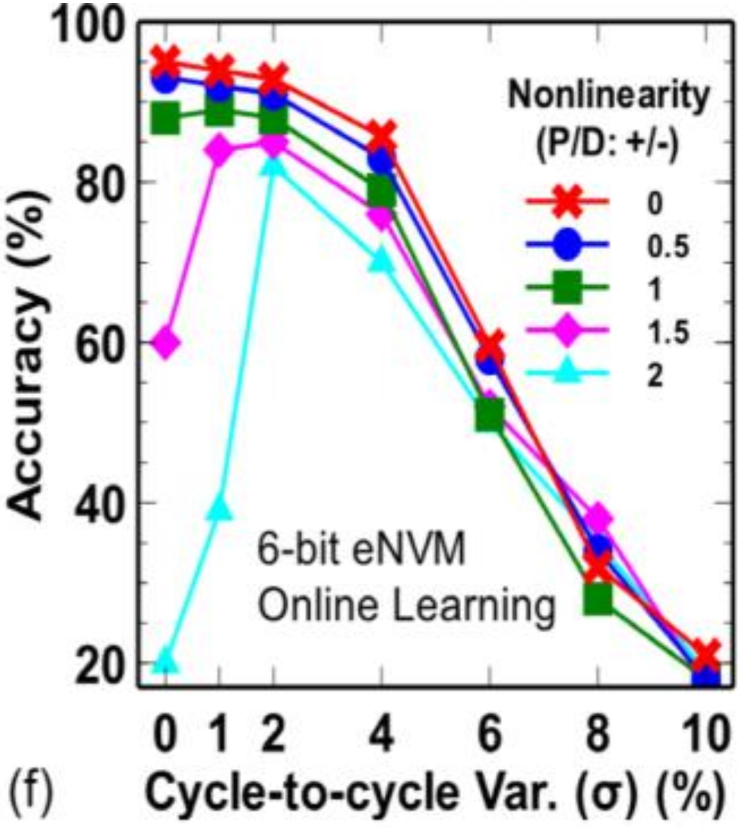



(f)

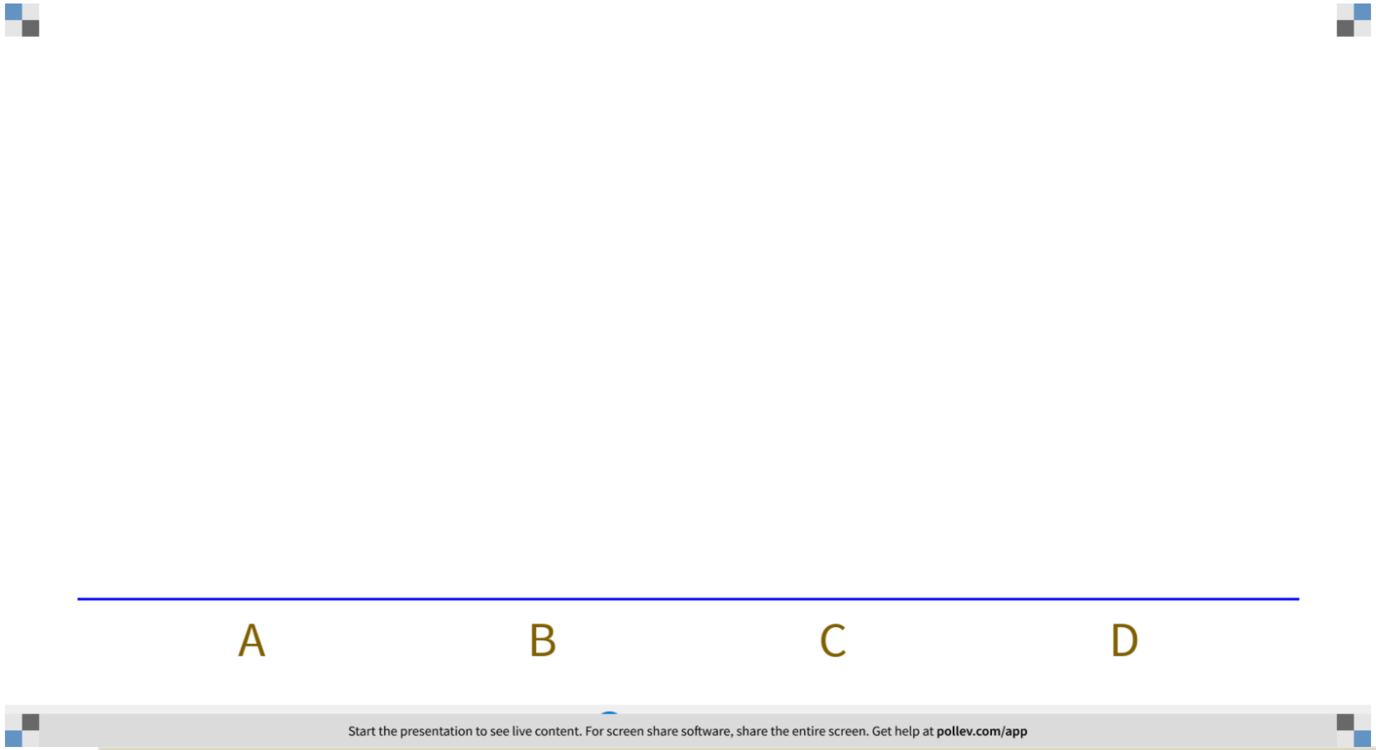
Islam et al. J Phys. D. 2019

# Quiz

What is the most important parameter to control in a memristive synapse device,
assuming high precision of states (6 bits)?

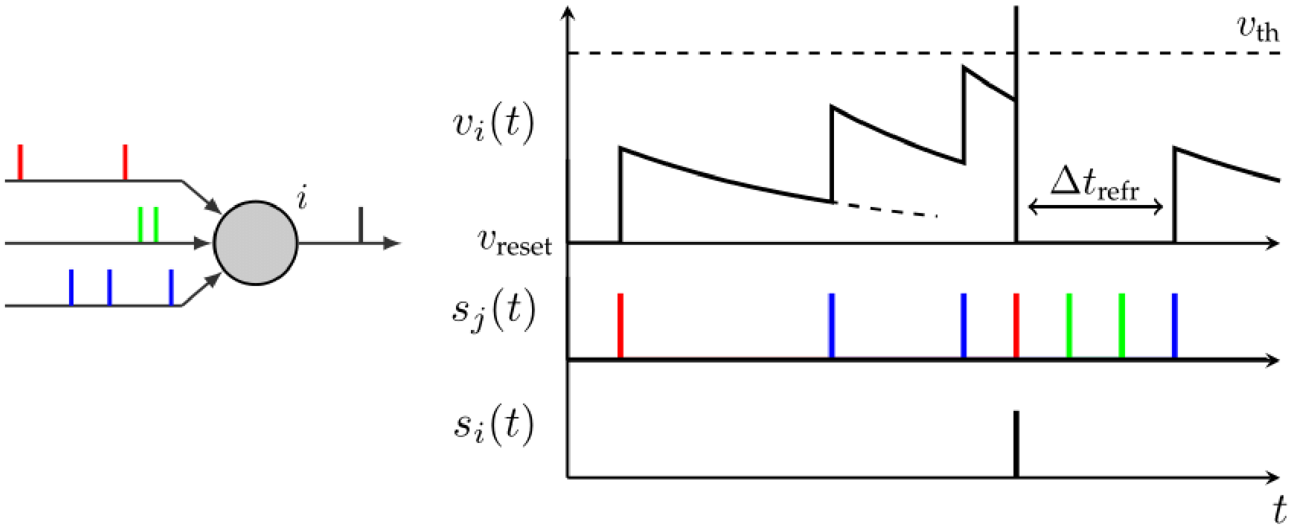
A: Dynamic range ($G_{on}/G_{off}$)
B: Asymmetry
C: Device-to-device $G_{max}$
D: Cycle-to-cycle noise

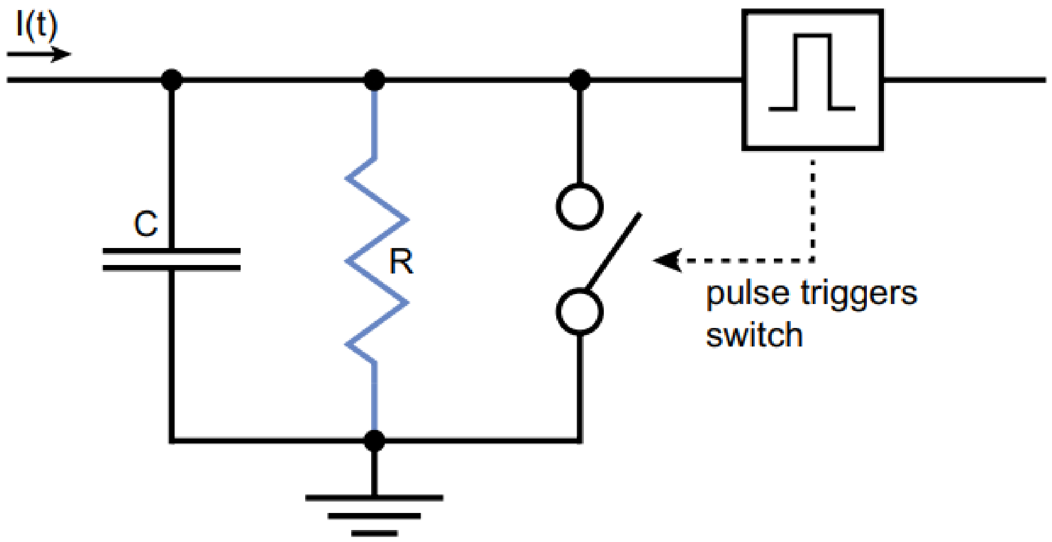
Go to PollEv.com/mattiasborg110



# Hardware neurons

- How to implement Leaky Integrate & Fire neurons in hardware?

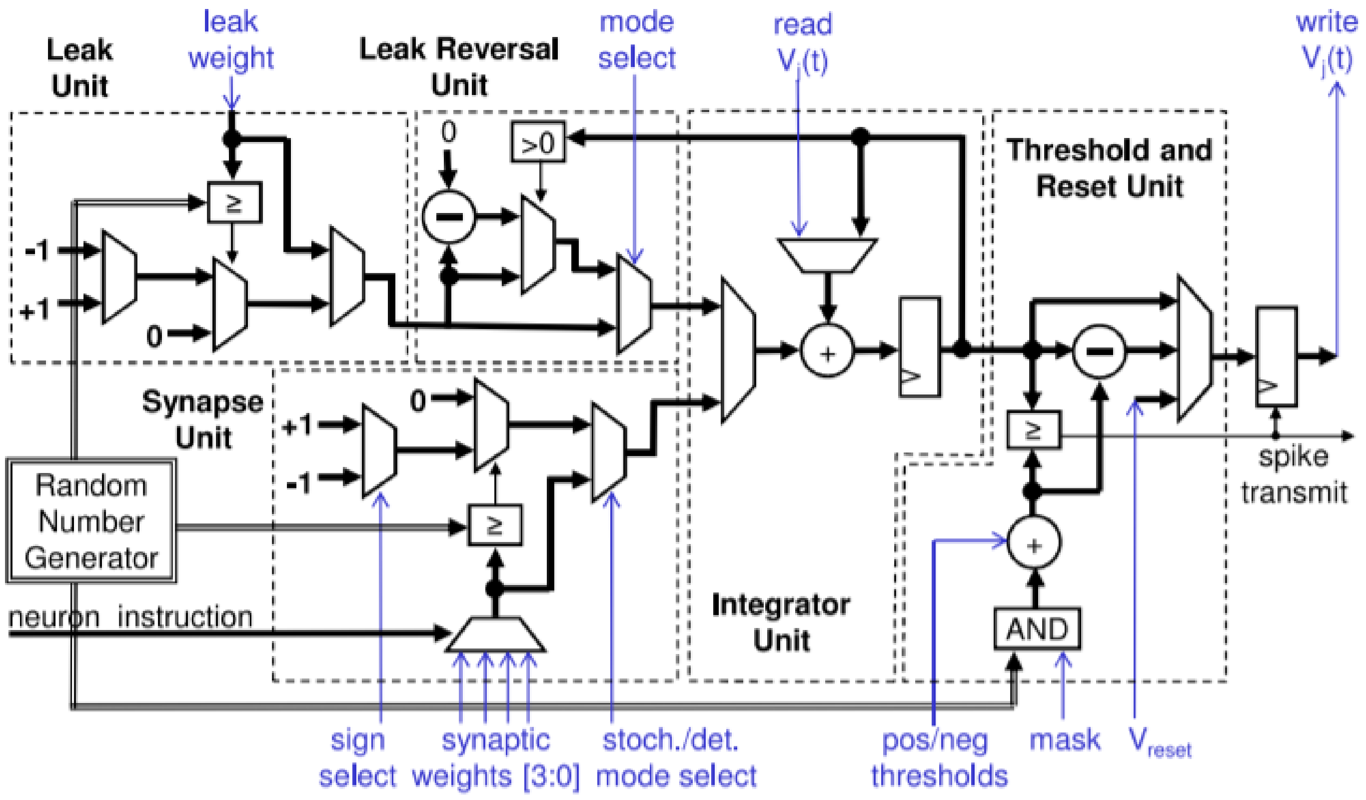



- Integrate input signals
- Fire when ”potential” above threshold
- ”Leak” potential
- Adaptive threshold
- Refractory period after spike
- Lateral inhibition

# Example: Si CMOS neuron

- CMOS Neuron in TrueNorth chip




- Synchronous, event-driven circuit
- Time-multiplexing
  → one circuit for 256 logical neurons
- Membrane state and synapse connections stored in SRAM when not used

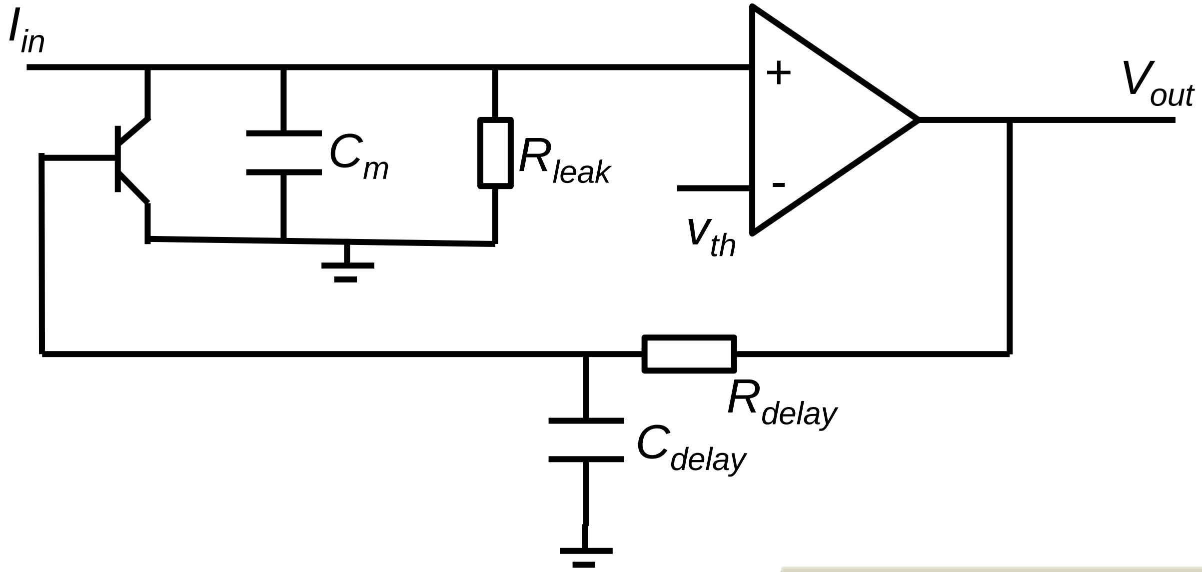
- Implements:
  - Integration
  - Threshold
  - Leak
  - Lateral inhibition
  - …

But very complex…and big circuit!
What is actually needed?

*Akopyan et al. IEEE Trans CAD of IC Sys 2015*

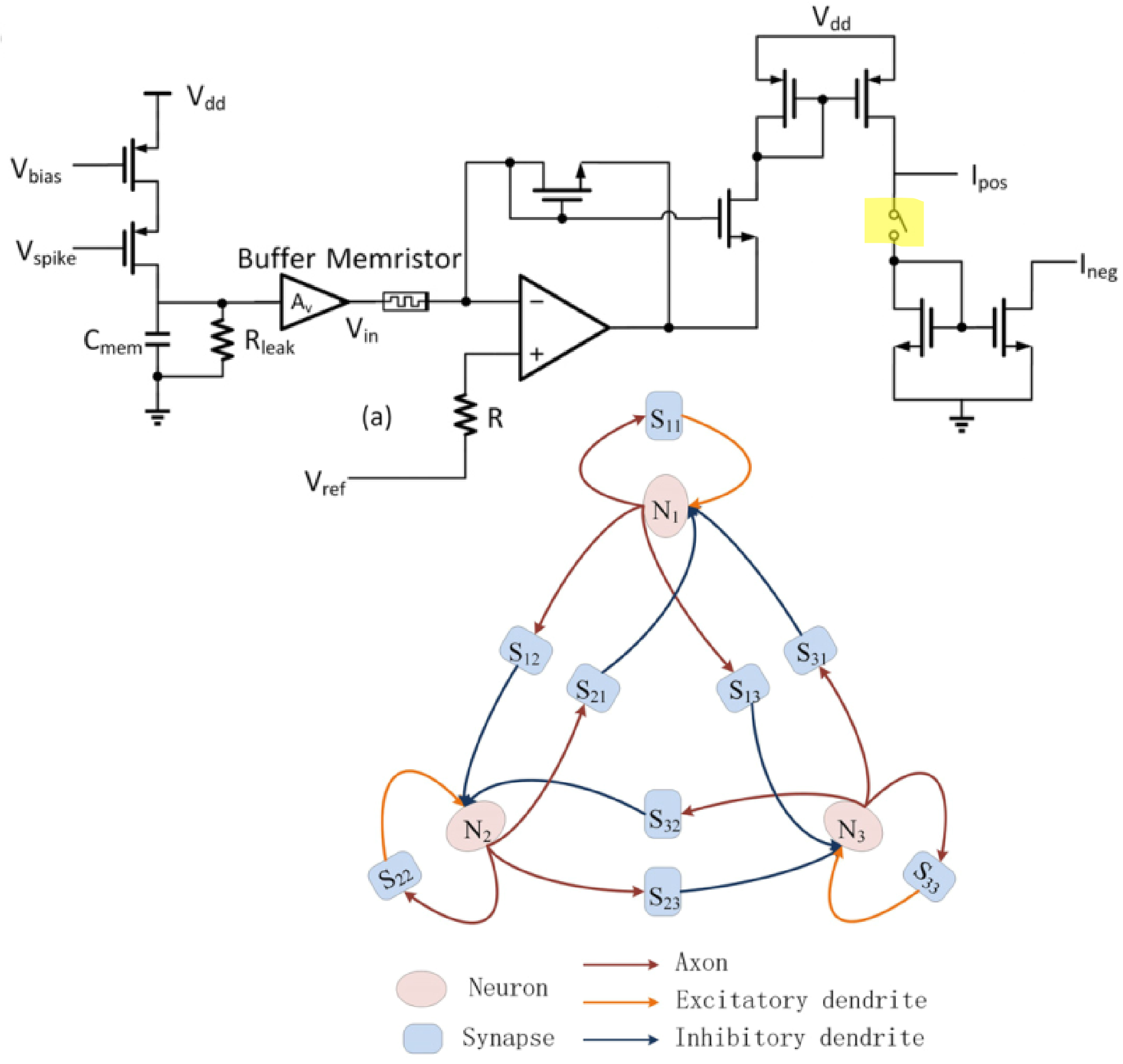
# Simple CMOS neuron

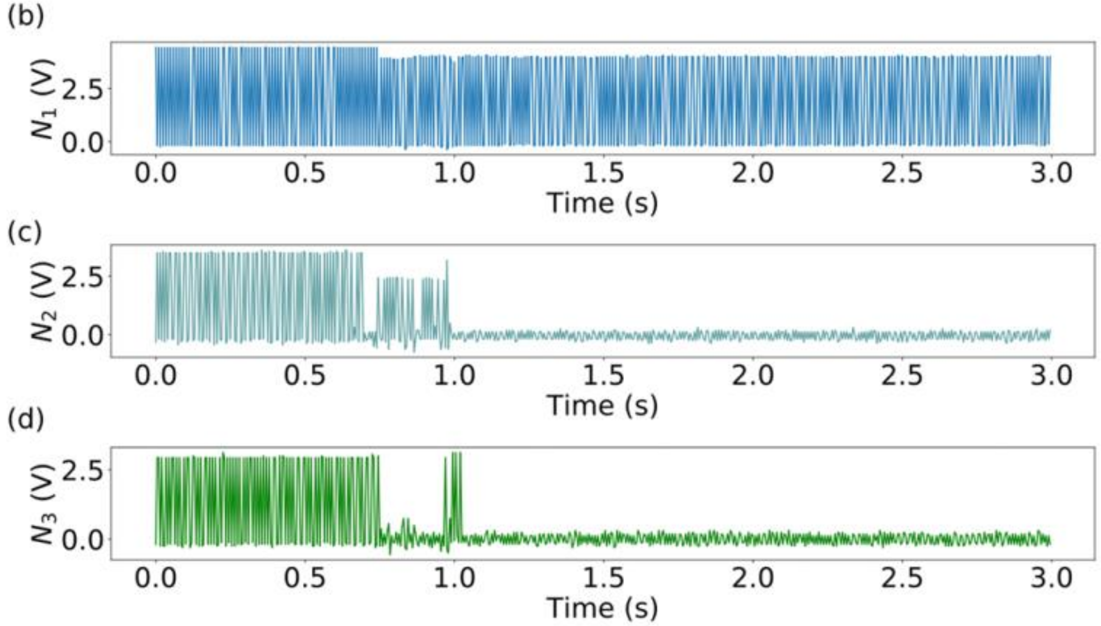
- Implements LIF neuron
  - Integration, Leakage
- Needs spike forming network
- Capacitors still needs lots of space, can we avoid them?



# Winner-takes-all (lateral inhibition)

- Implemented by ”inhibitory” memristor synapses
  - Moves implementation from neuron → synapse
- External switch determine sign of weight

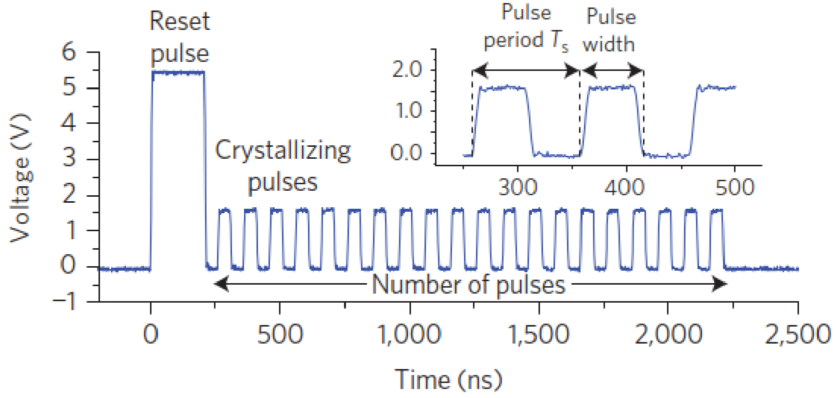


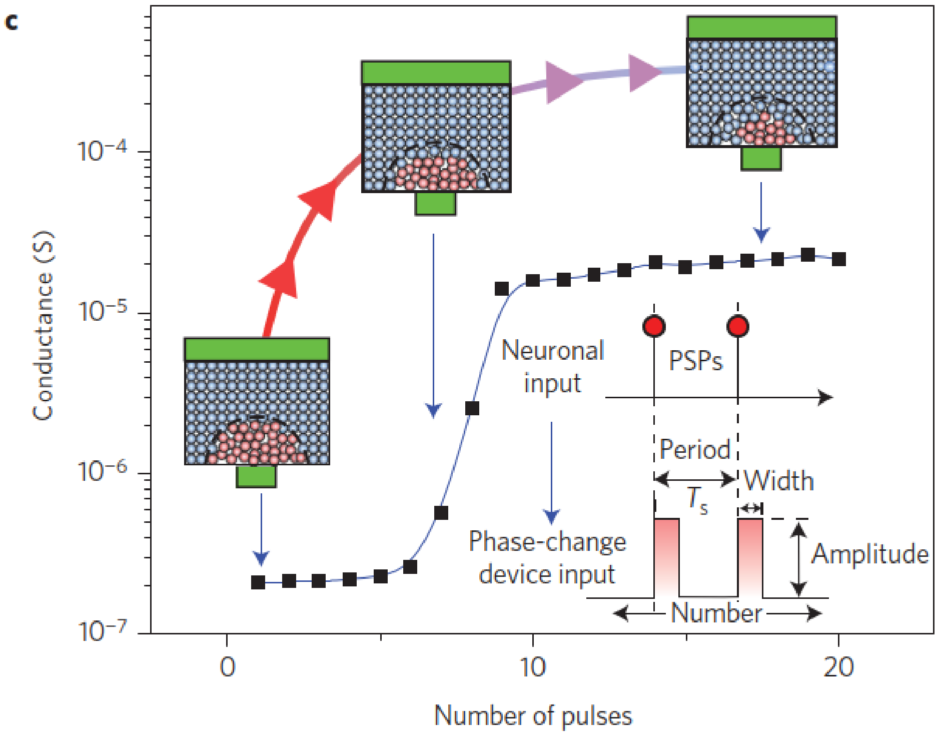



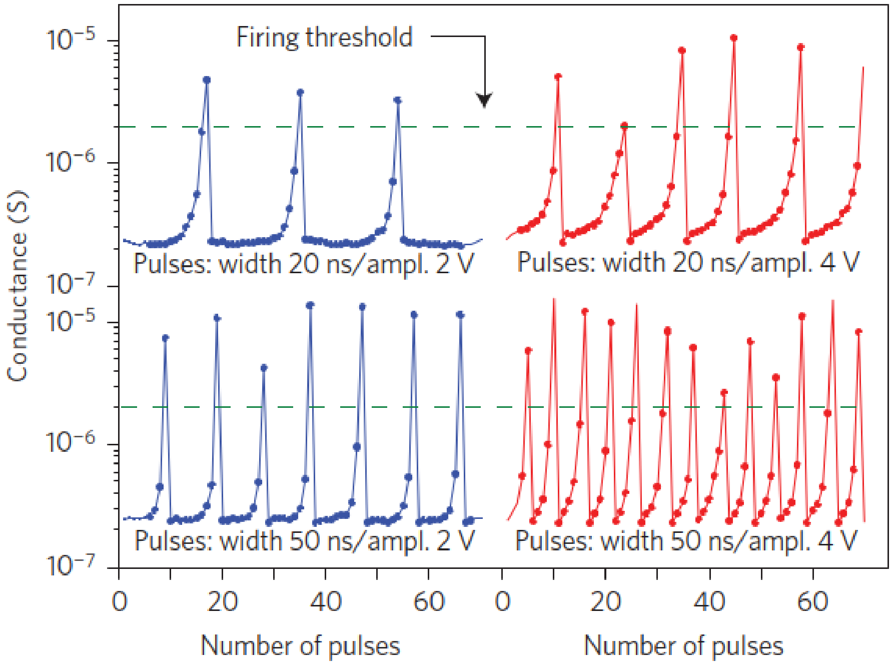

*Wang et al. APL 2019*

# PCM Neuron

- Exponential change of conductance with crystallization pulses → Integrate and Fire
- Non-volatile → No ”Leak”
- Requires manual reset pulse after each ”spike”



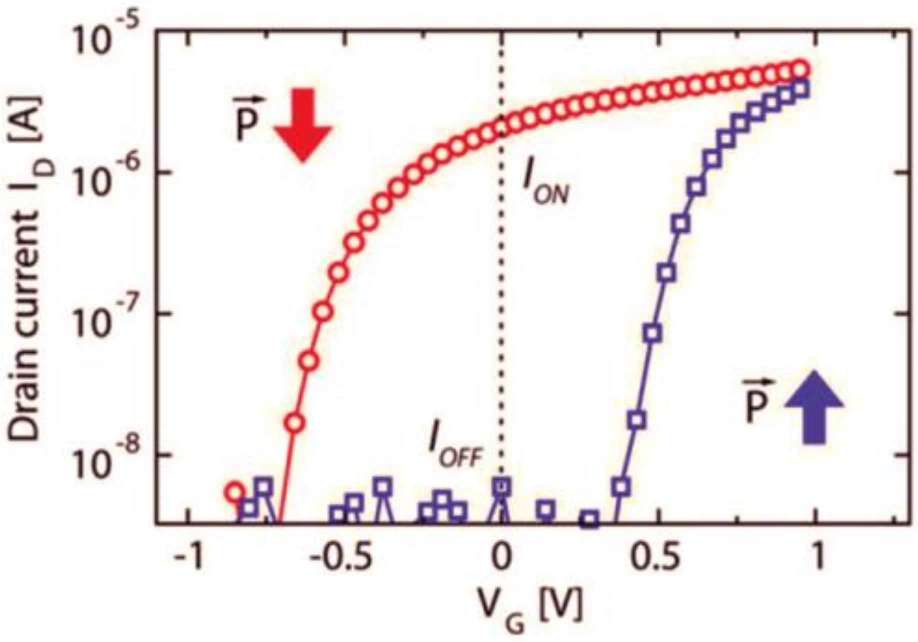



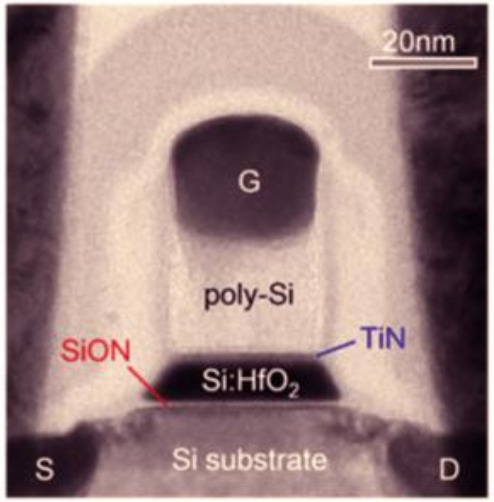



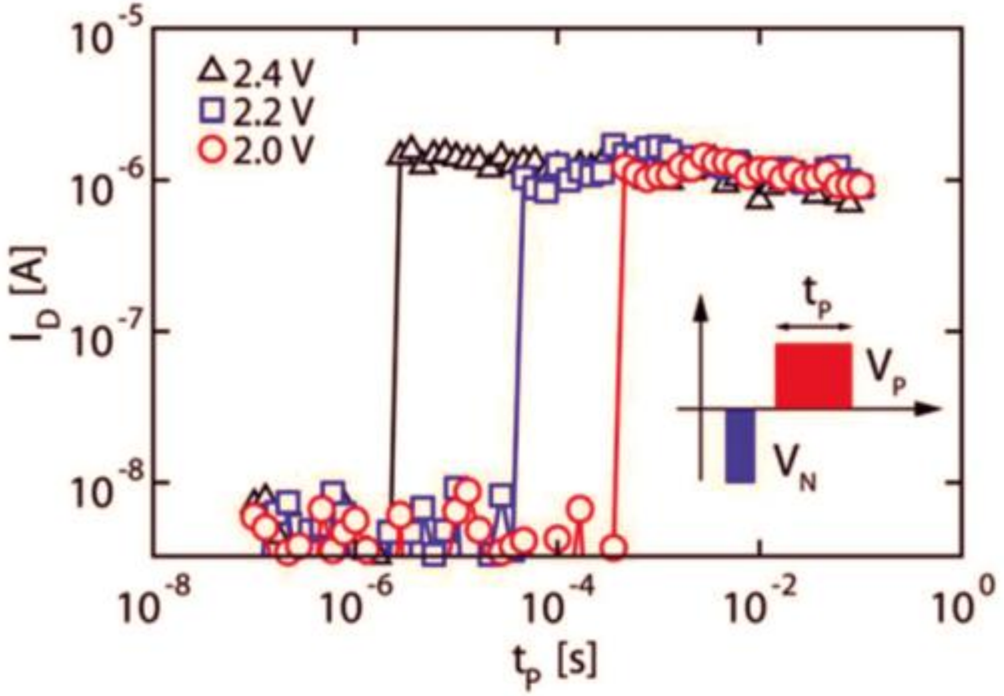

*Tuma et al Nature Nanotechn. 2016*

# FeFET neuron

- Single FeFET can implement Integrate-Fire Neuron → avoids bulky capacitors!
- Pulse length threshold for switching polarity in nanoscale FeFETs
- Multiple ”non-switching” pulses accumulate to cause switching



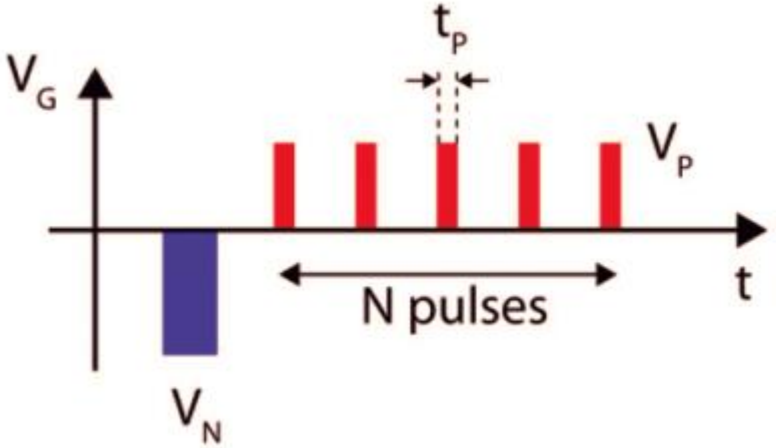



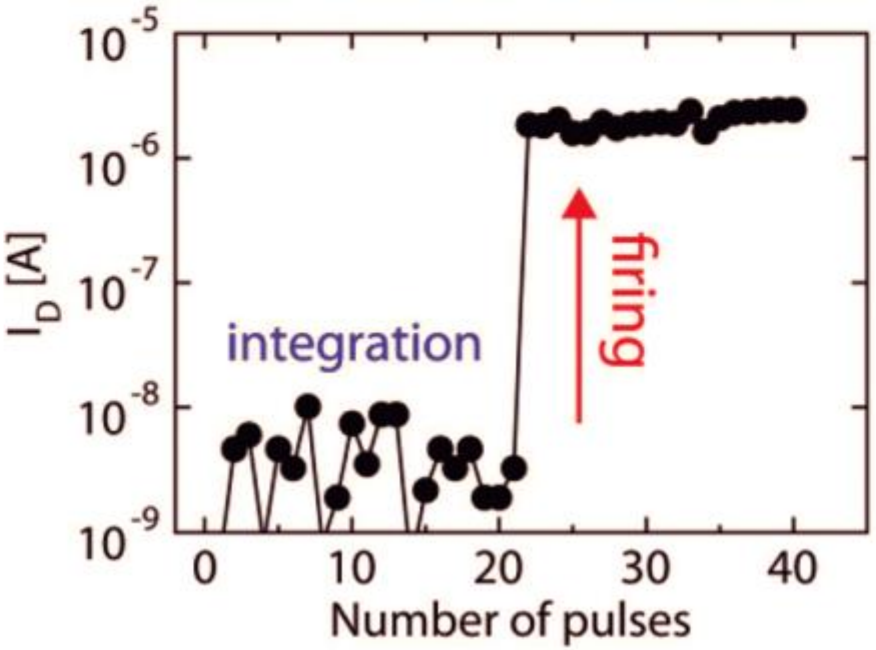



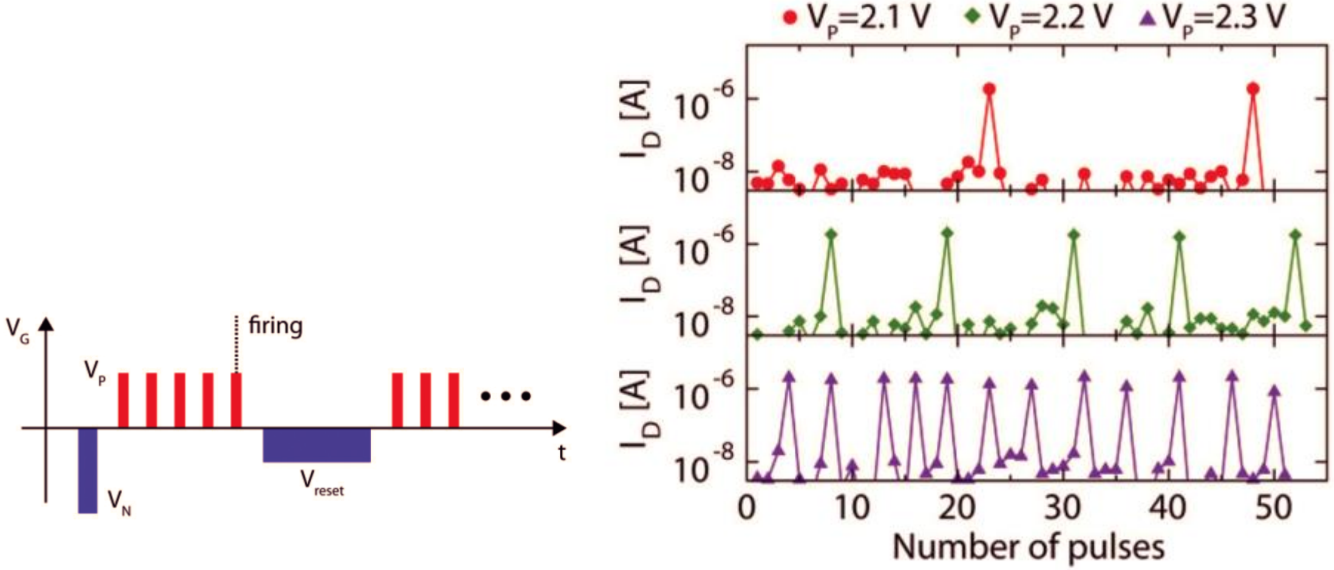

*Mulaosmanovic et al. Nanoscale 2018*

# FeFET Neuron II

- Implements integrate & fire
- Depolarization field → leakage
- Negative pulse needed for resetting
- Refractoriness implemented by negative pulse
- Would need coupling to CMOS spike generation network




*Mulaosmanovic et al. Nanoscale 2018*

# Summary

- Memristive memory devices (that we have) are not ideal
- Some non-idealities we can live with
  - Device-device variations in range
  - Noise
  - Limited dynamic range
- Some are more important to fix
  - Asymmetric weight update

- Neuron circuits are big and complex
- Possibility to use memristor devices for neurons, but early research

# Make your own quiz question!

- Come up with a good quiz question based on the topics of L8-L11
- You have until the end of the lecture/day → Send it to mattias.borg@eit.lth.se
- Quiz will be posted on Canvas for you to practise on..

**What is the chance that you win on the lottery?**

1. Chance? I always win
2. 1 in 100 000
3. As good as dying in a plane crash
4. I will win when pigs can fly

Lecture 8 – ReRAMs

Lecture 9 – Phase change Memory

Lecture 10 – STT-MRAM

Lecture 11 – Ferroelectric Memory