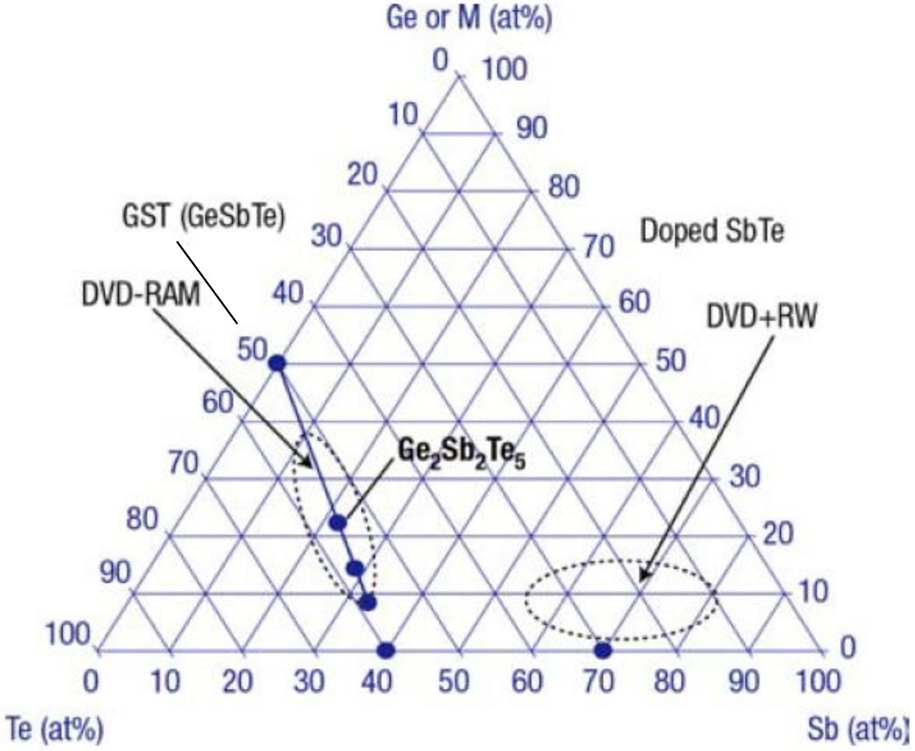
EITP25 2020

Lecture 9 –
Phase-change memories

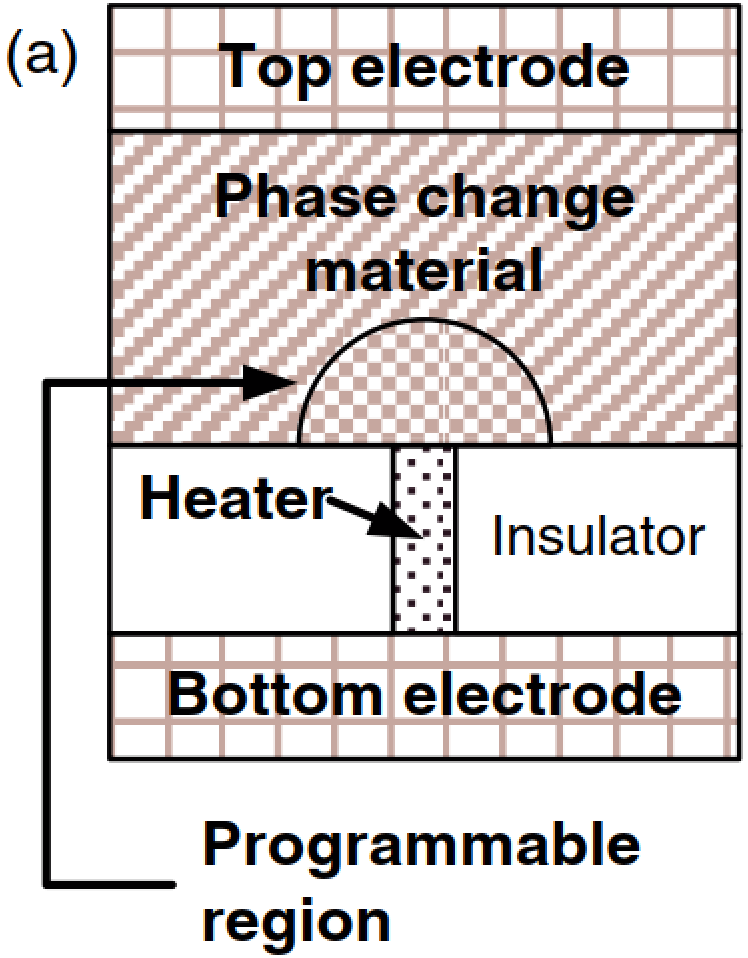
Outline

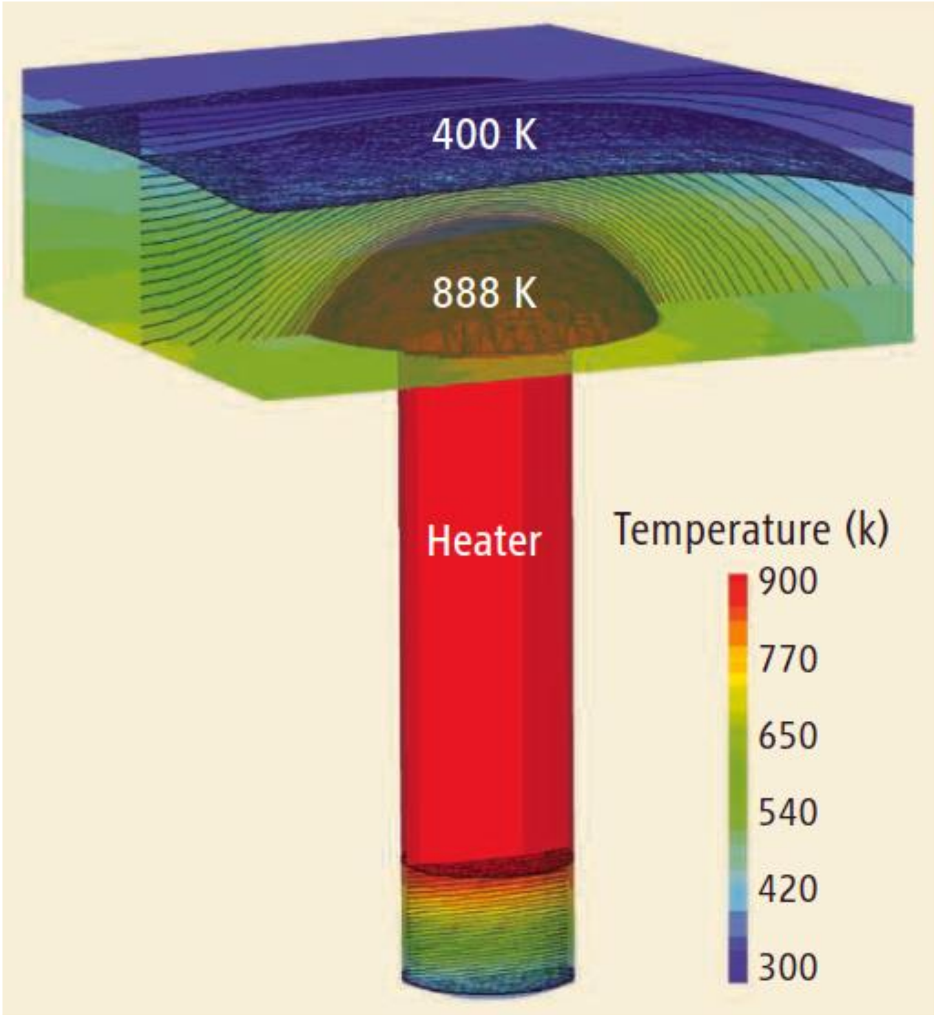
- Phase change materials
- Physics of switching in PCM
- Scalability of PCM
- Benchmarking
- PCM in neuromorphic computing

How does DVD and BluRay work?



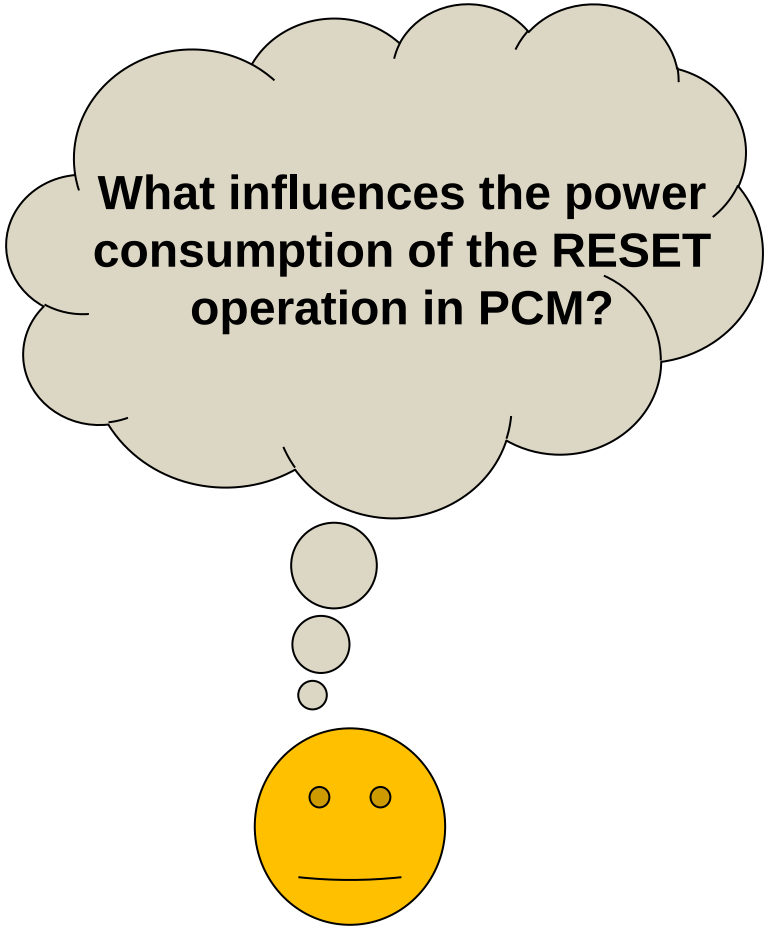
The PCM device structure

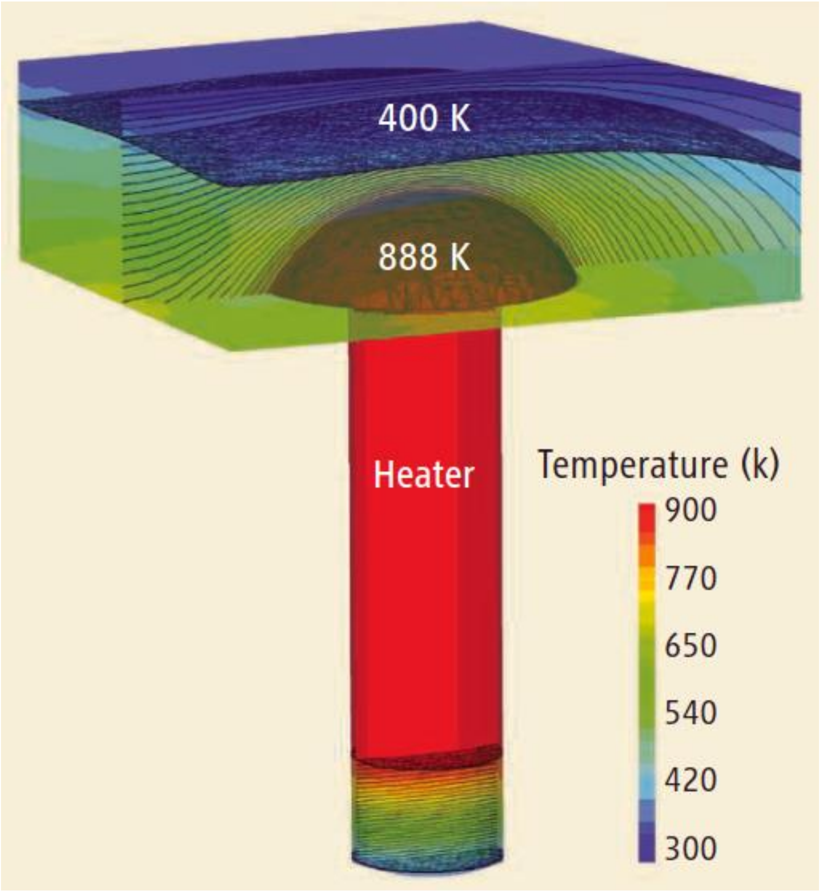




Atwood, Science 2008

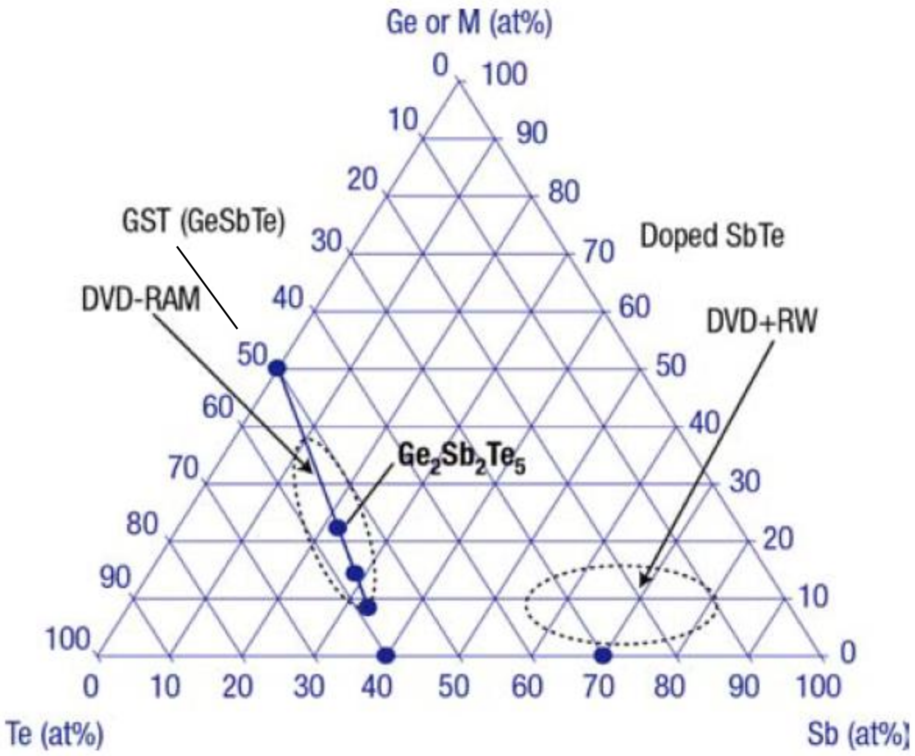
Think-share: RESET Power consumption





Needed material properties

1. Reversible switching between phases → lifetime
2. High electrical resistivity contrast → signal to noise
3. Fast crystallization → Operation speed
4. Stable resistance states → Reliability
5. Properties stable to nanosize → Scalability

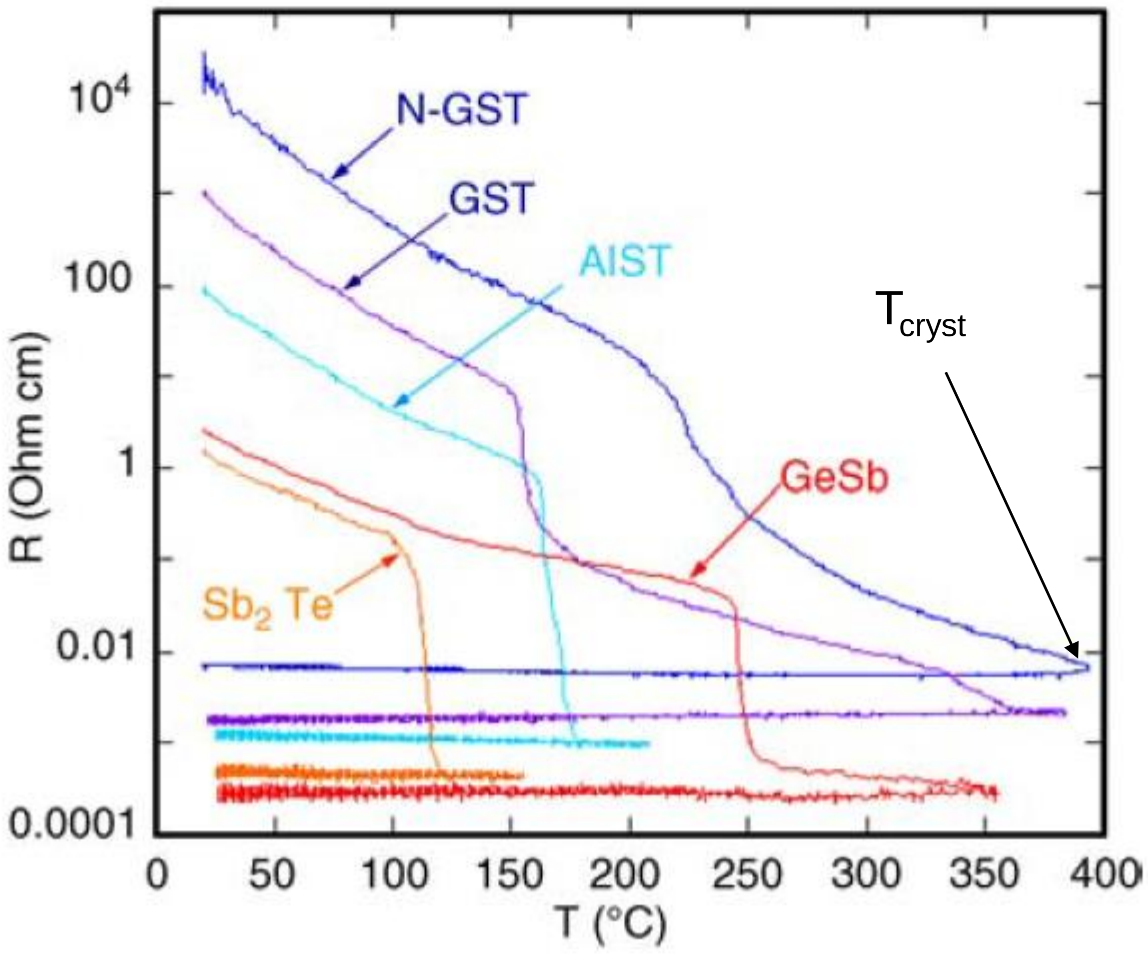


Electrical Resistivity Contrast

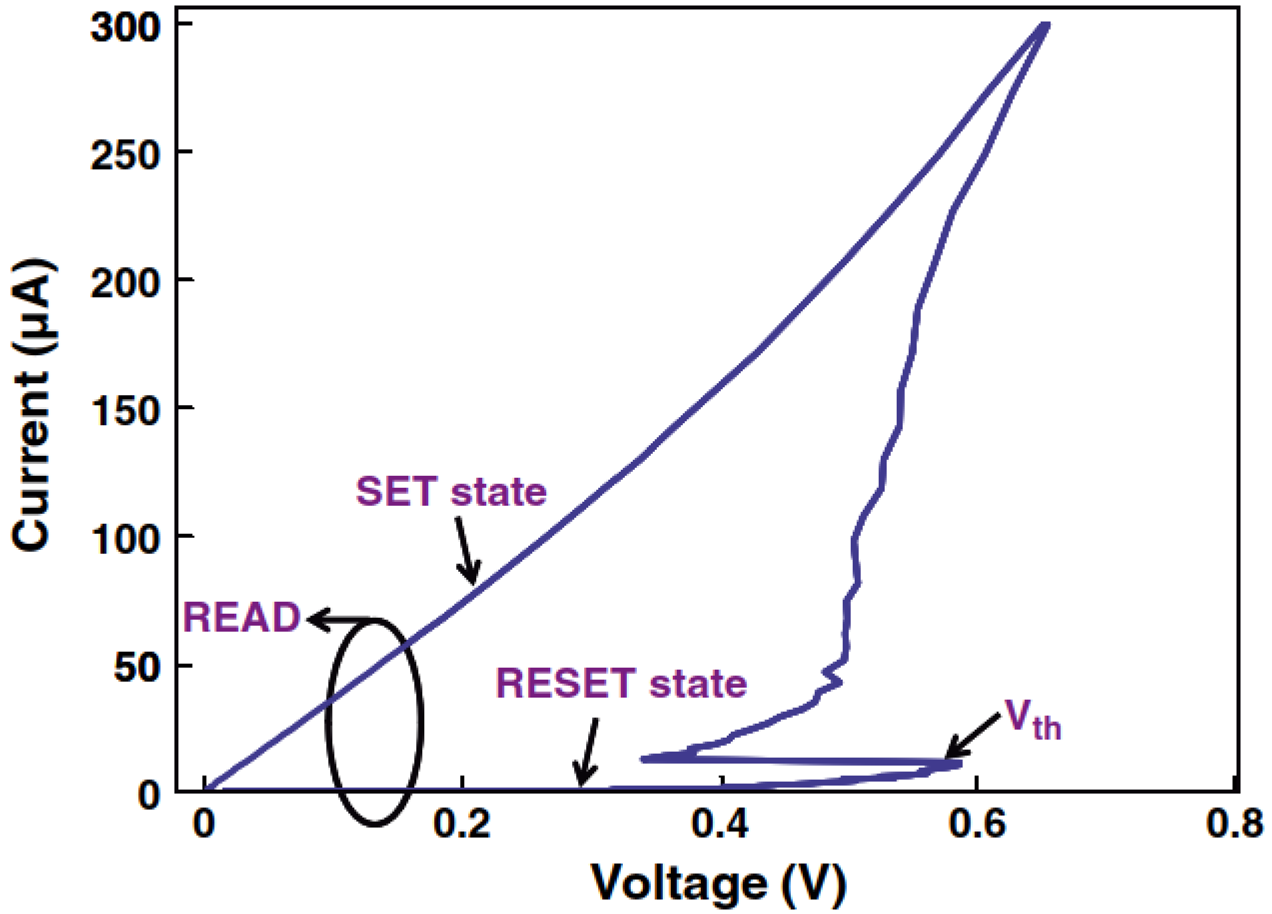
- R_{RESET}/R_{SET} > ~ 10^5-10^6

- Sharp decline in resistance above certain T
  → T_{cryst}
- T_{cryst} must be high enough to retain memory state

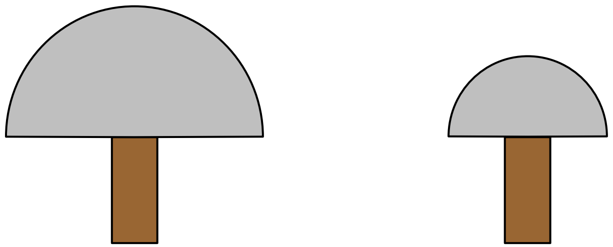
- AIST ($AgInSb_6Te_{12}$) and Sb2Te may not be suitable for some applications, why?



Conduction mechanism



Resistance drift



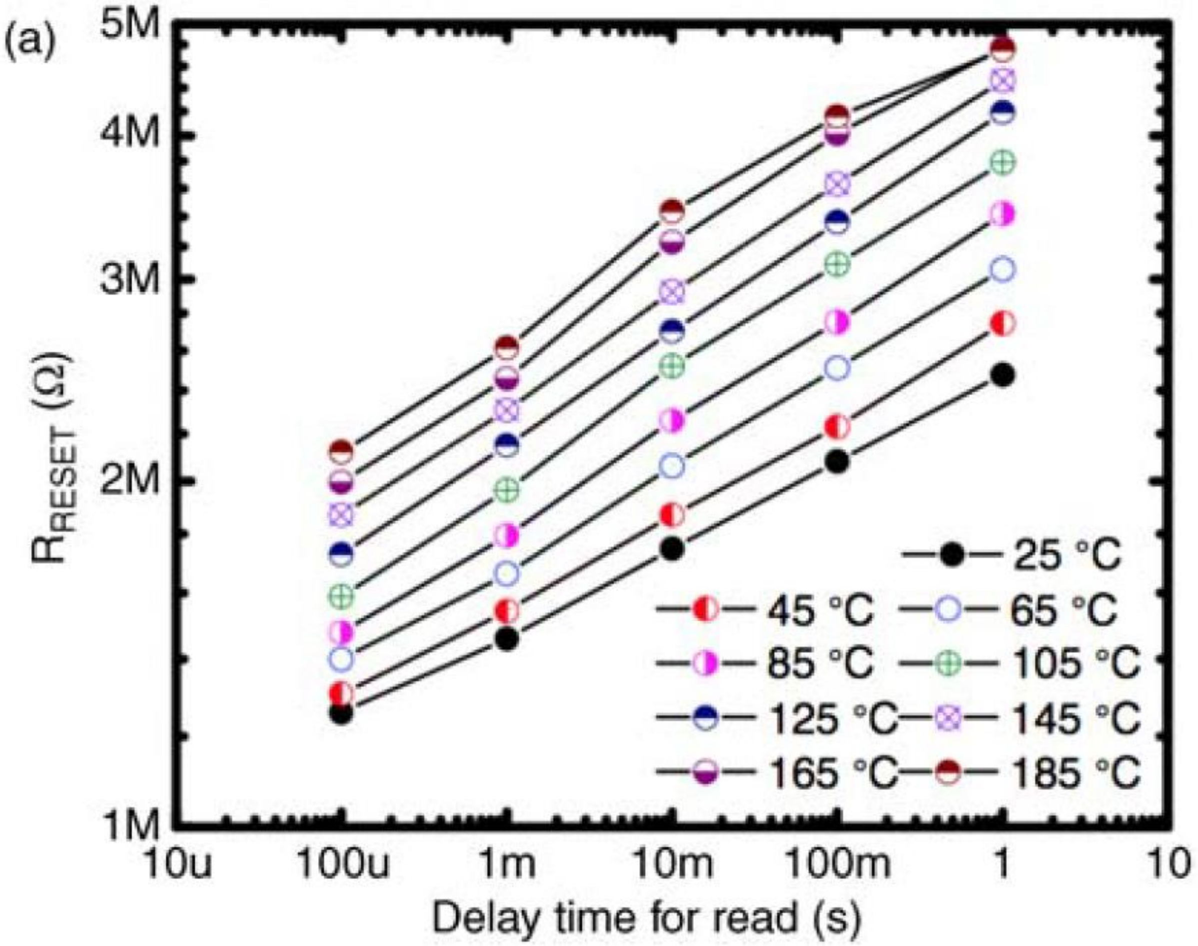
- High-resistance state (HRS) depends on the volume and nature of the amorphous region

- HRS varies between cycles
- HRS drifts (increasing R) over time!
  - Defects “heal”
    → longer between remaining defects
    → larger transport energy barrier

$$R(t) = R(t_0)\left(\frac{t}{t_0}\right)^{\nu}$$

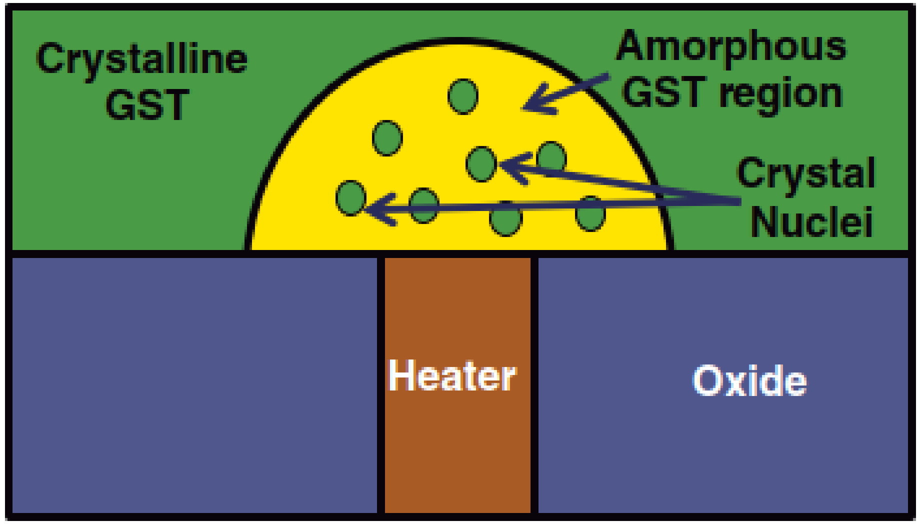
$$\nu = drift\ exponent$$

- Drift is a strong function of temperature and size of the amorphous region

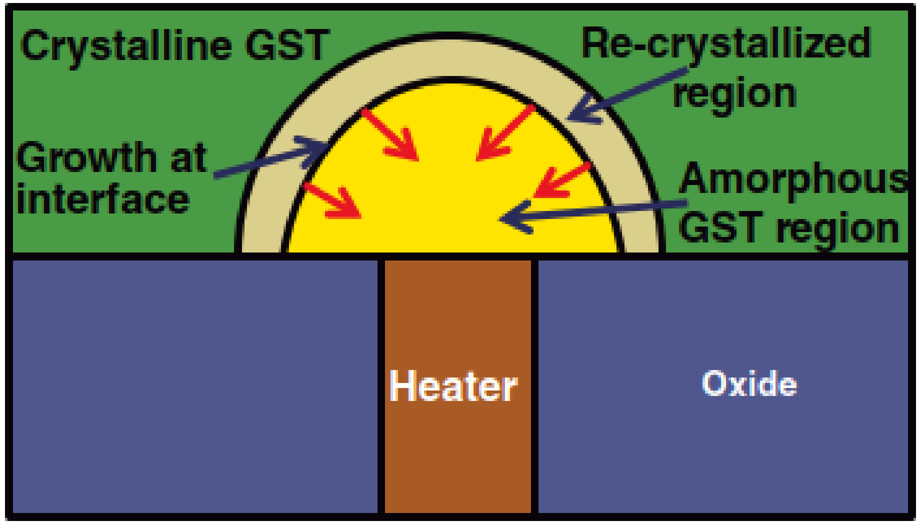


Mechanism of crystallization

Nucleation-dominated



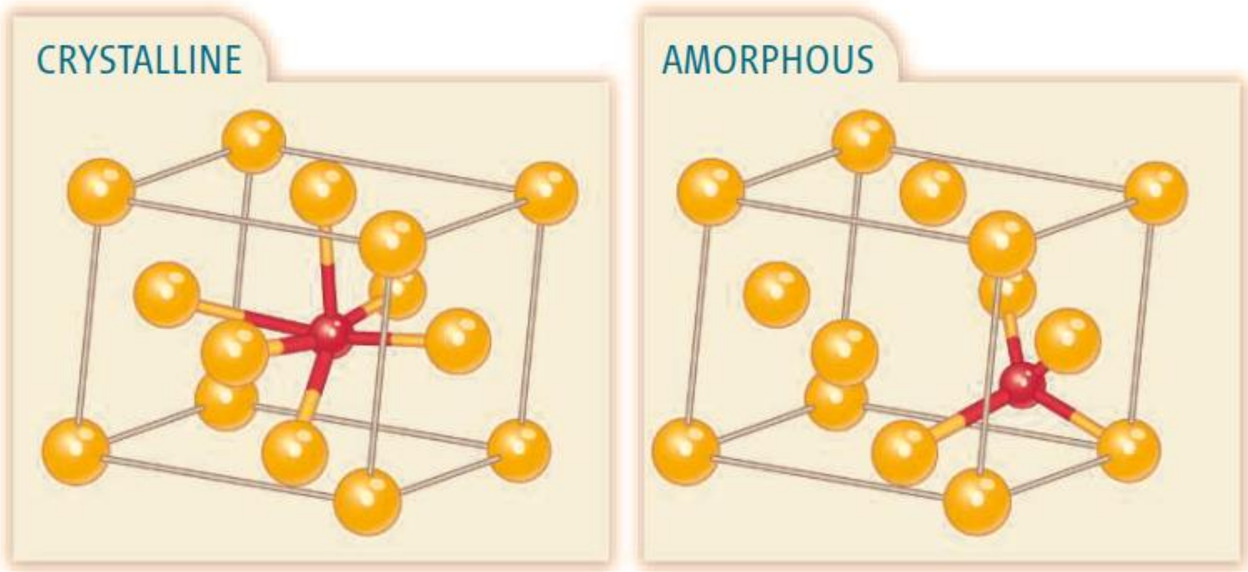
Growth-dominated



Crystallization speed

- Typical speed: ~10 ns
- Crystal structures with small difference between amorphous and crystalline are faster
- Small pre-set incubation field induces local preordering → 100’s ps!

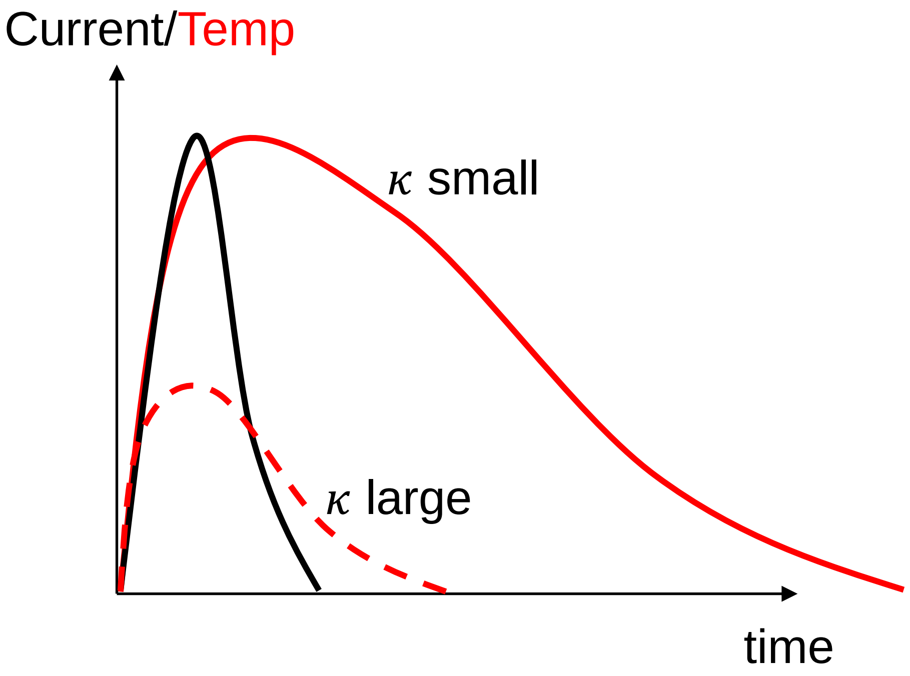
- Limits the operation speed of PCM!

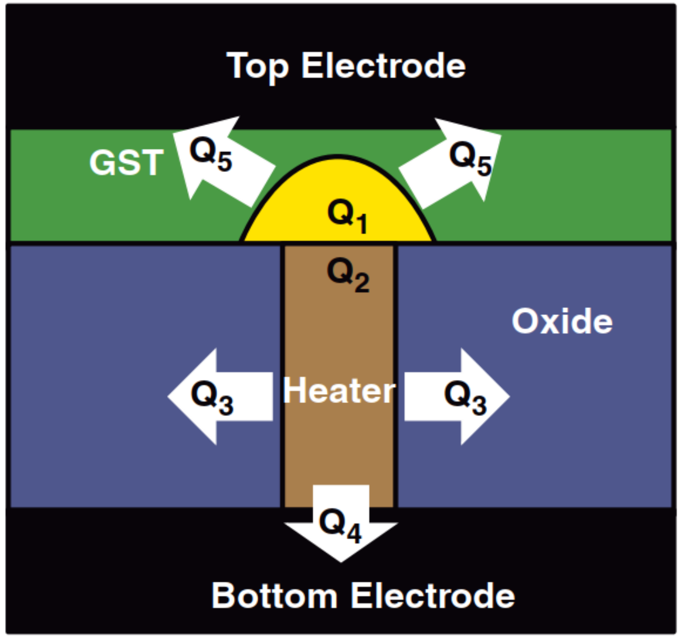


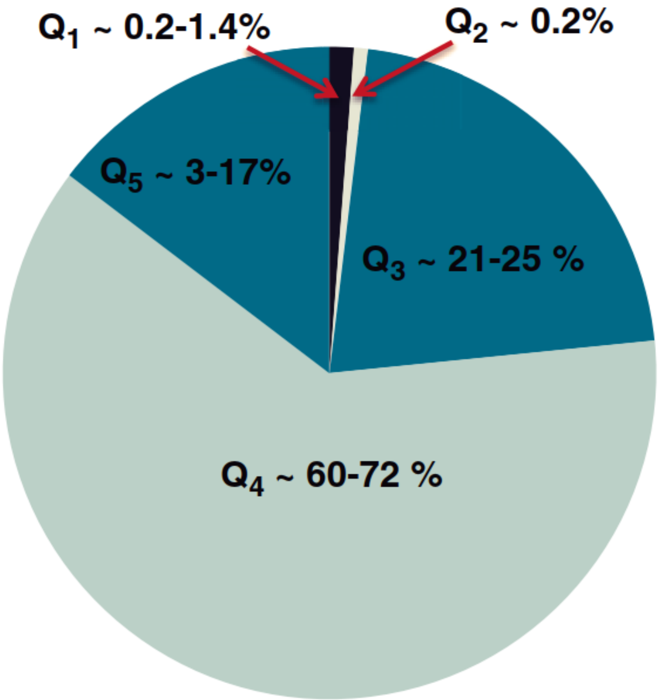
Amorphization and Thermal properties

- High enough current → high enough Temperature for melting
- Ultrashort time → quenching crystallization → amorphous phase

- Thermal properties are vital for low power amorphization (RESET)

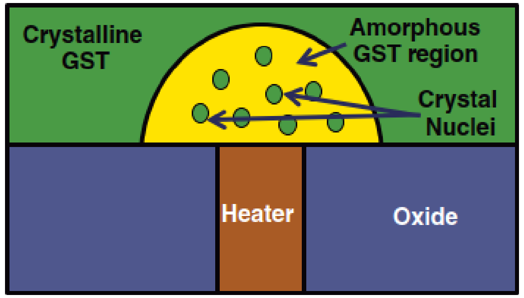


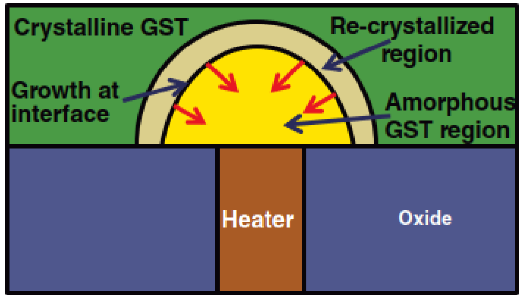


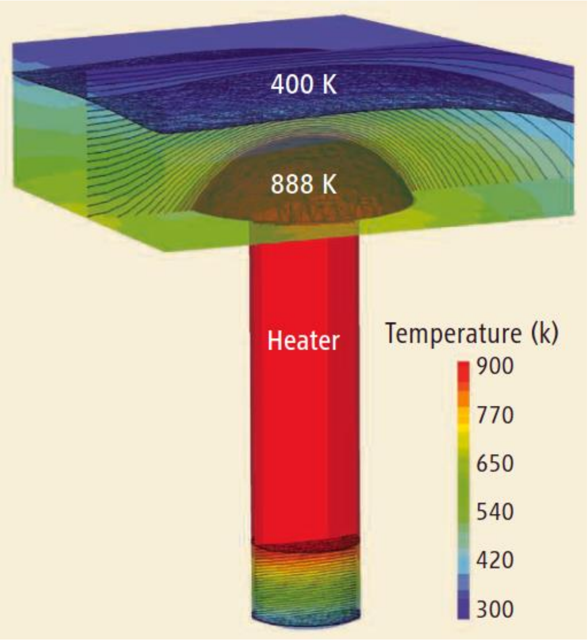


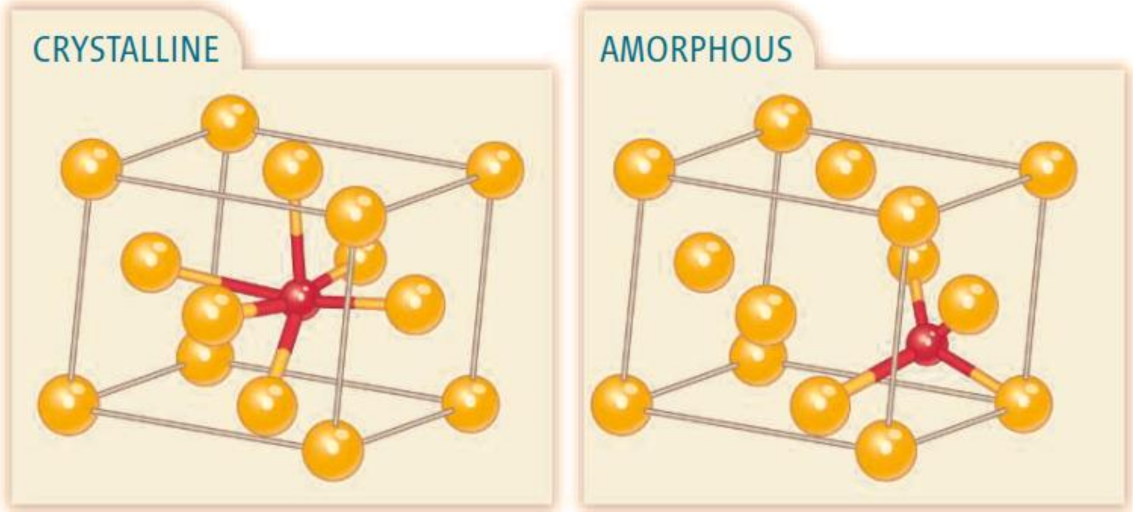
Think a bit - Scaling materials

1. What happens to the ratio between volume and surface when devices are scaled down?
2. What could be the ultimate scaling limits?
3. What important parameters could shift?





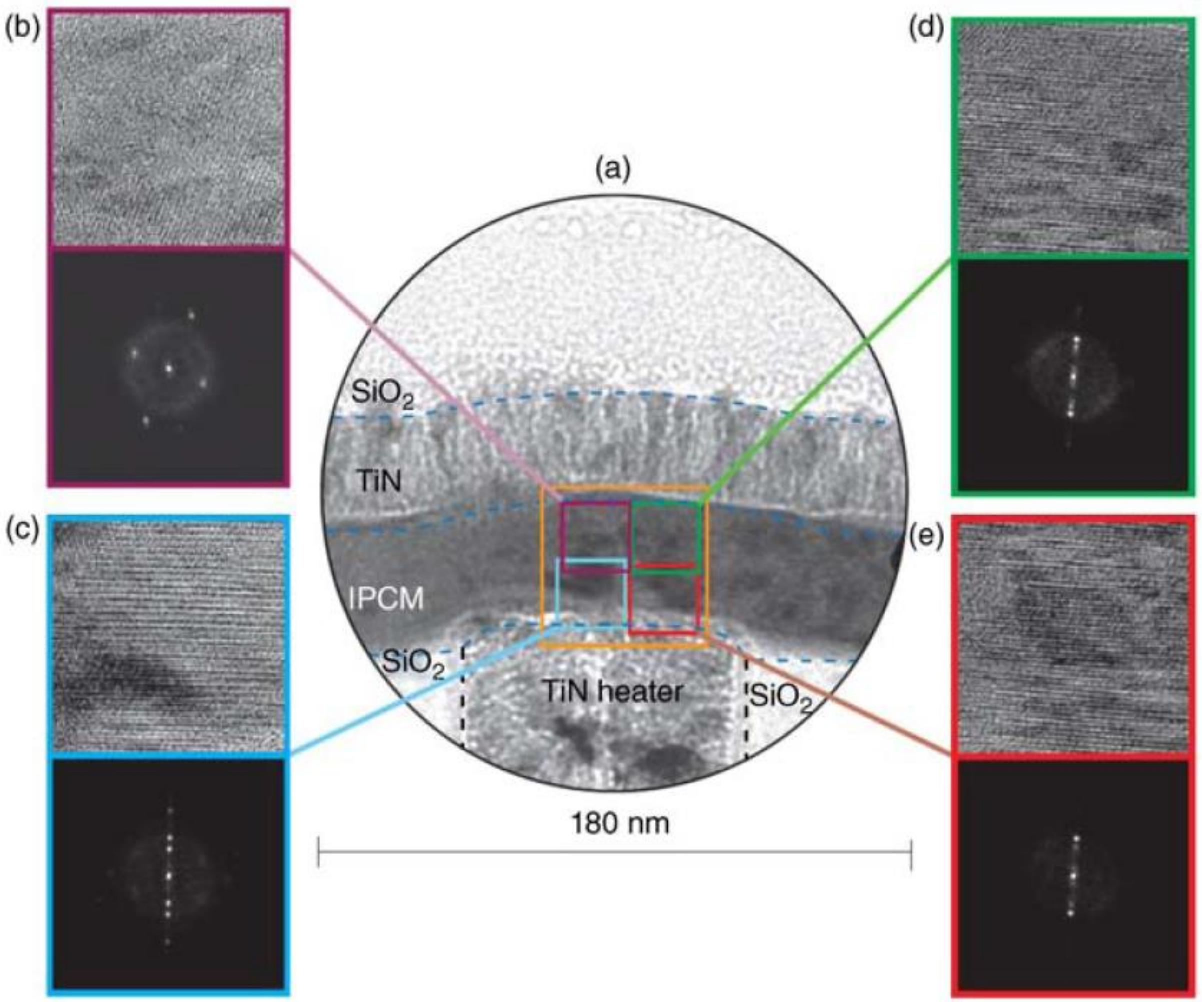




Example: Interface-engineered PCM

- Superlattice-like structure (GeTe-Sb_2Te_3)
  - Maximizing interface effect!
- Phonon confinement at interface → Thermal conductivity very low
- Long range order reduce entropy cost of amorphidization
  - → reduced energy for SET/RESET
  - → reduced cycle-cycle variability
  - → faster switch times

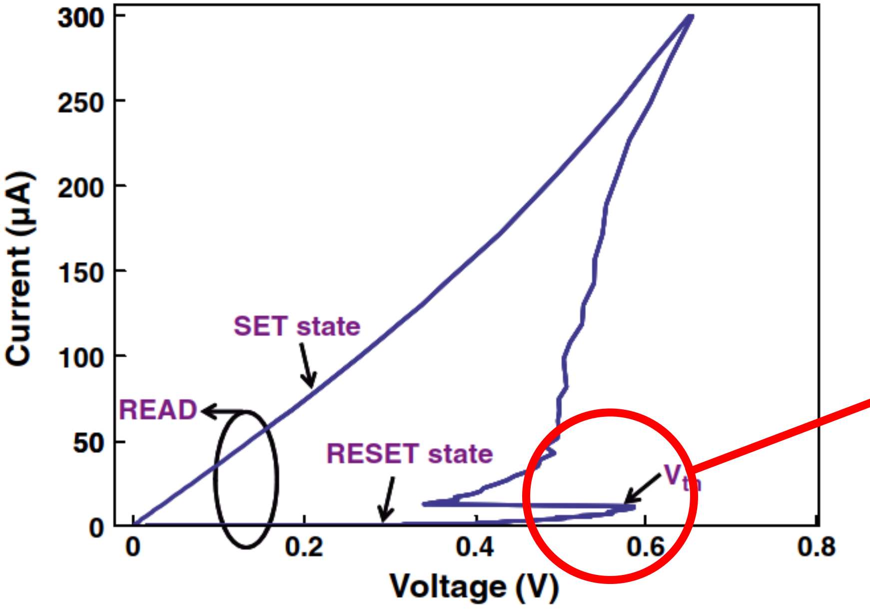
- Similarly, nanostructured GST shows:
  - Reduced thermal conductivity
  - Reduced resistance drift
  - Higher crystallization T
  - Lower melting T

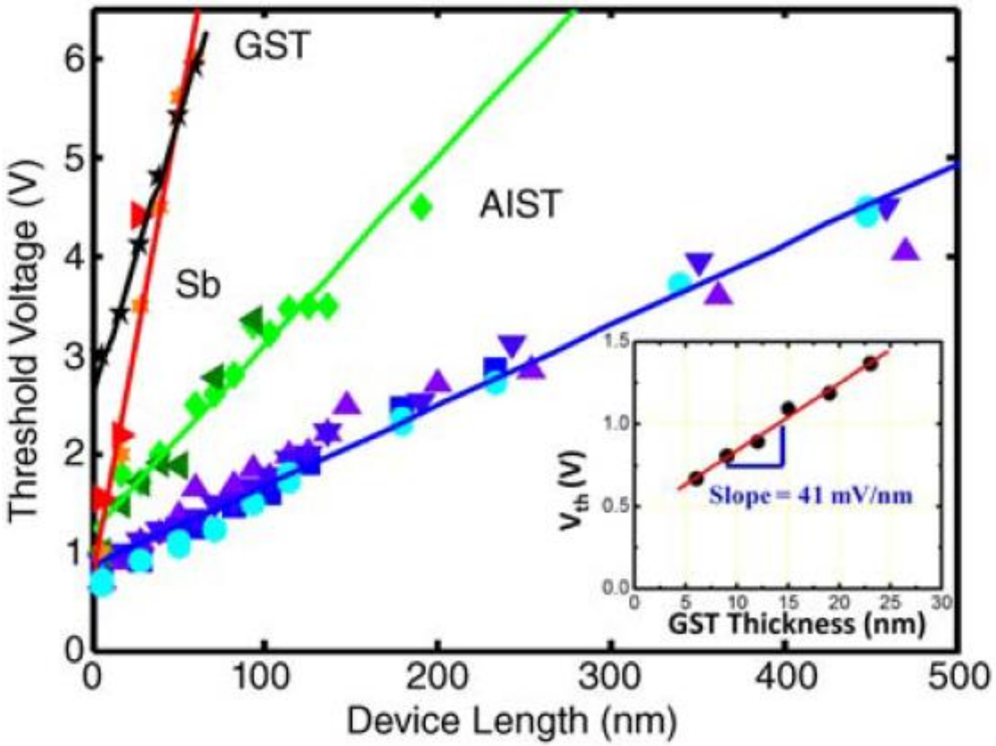


Scaling threshold voltage

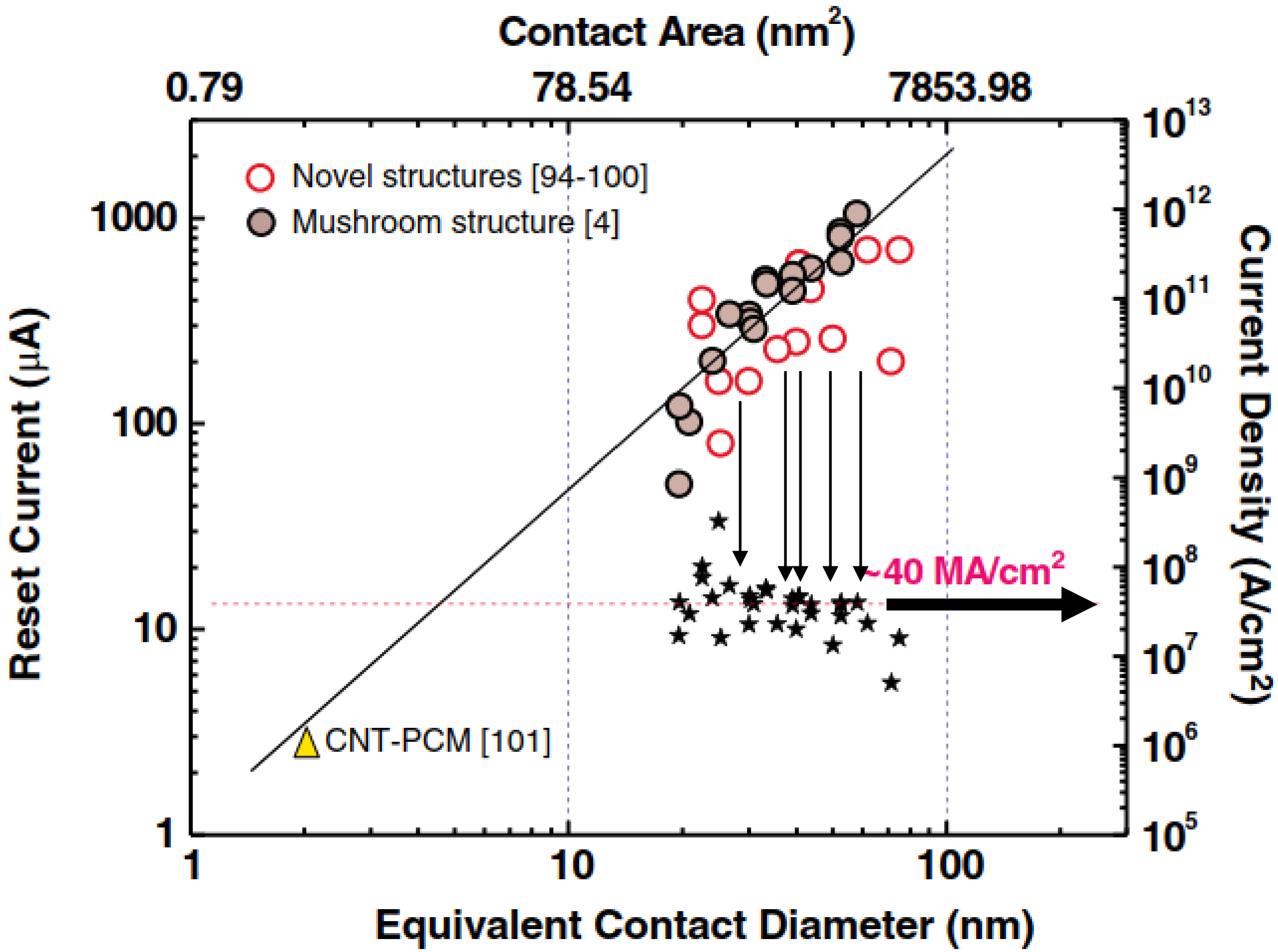
- Apparently all (common) materials exhibit linearly changing threshold voltage
- Offset at device length = 0!

- **Q: What does this offset signify?**

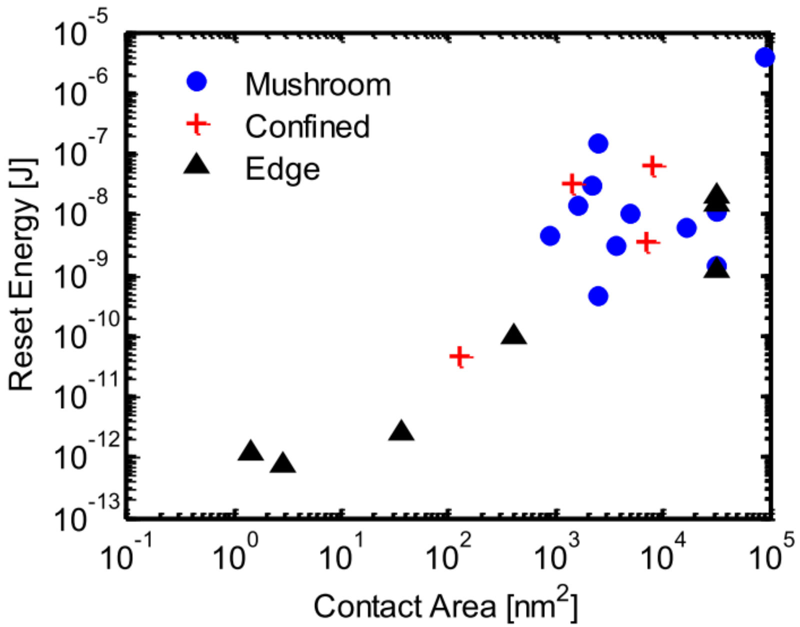




Scaling reset current



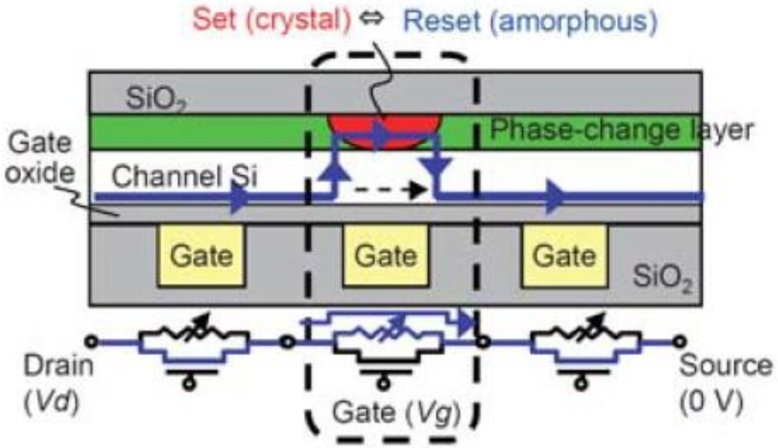
- RESET current supply a limiting factor
- Typically 40 MA/cm^2 is needed
- Careful engineering needed to scale this down further.
- **Possible limitation for PCM scalability?**



Fong et al IEEE Trans. Electron Dev. 2017

3D PCM

- High current density prohibits PCM scaling → go 3D instead!



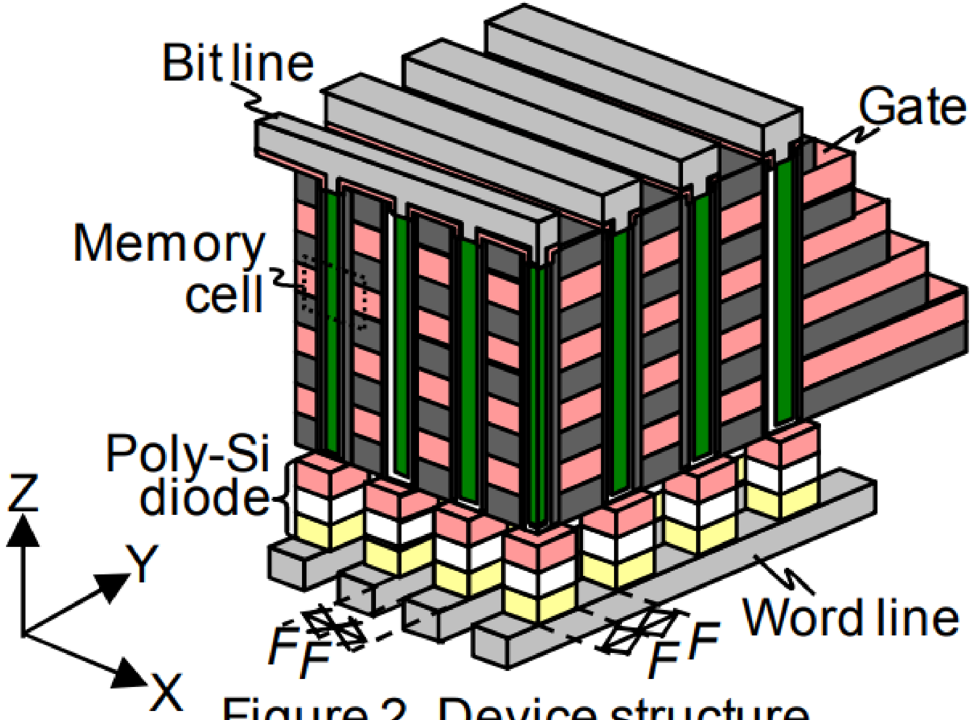
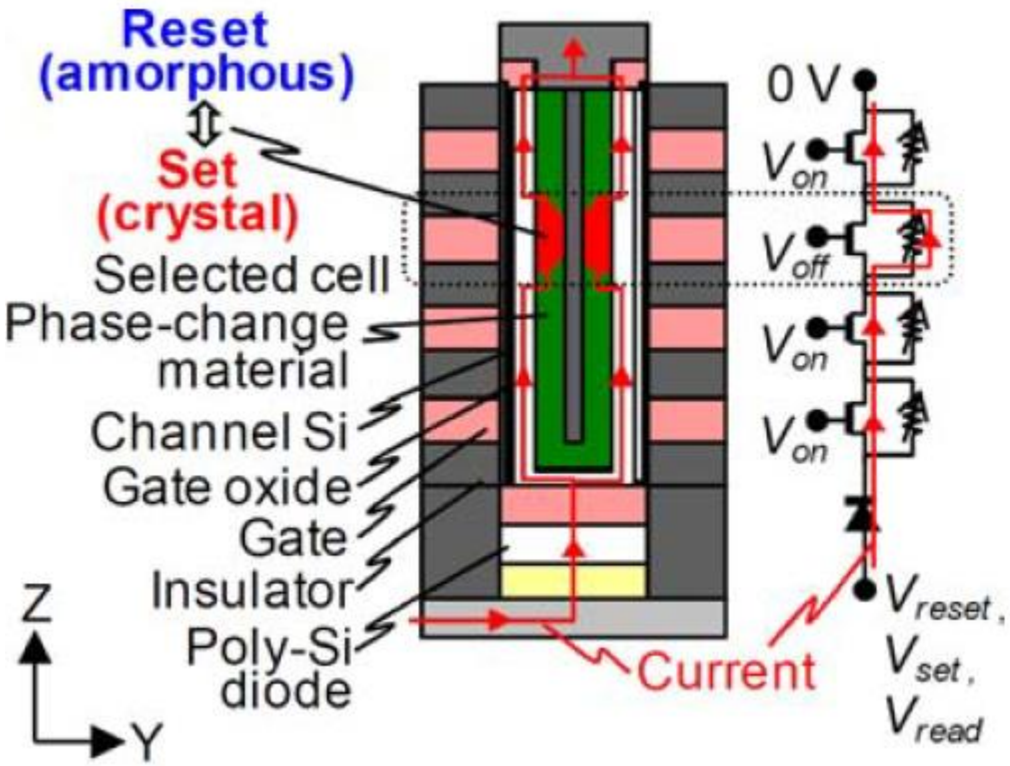


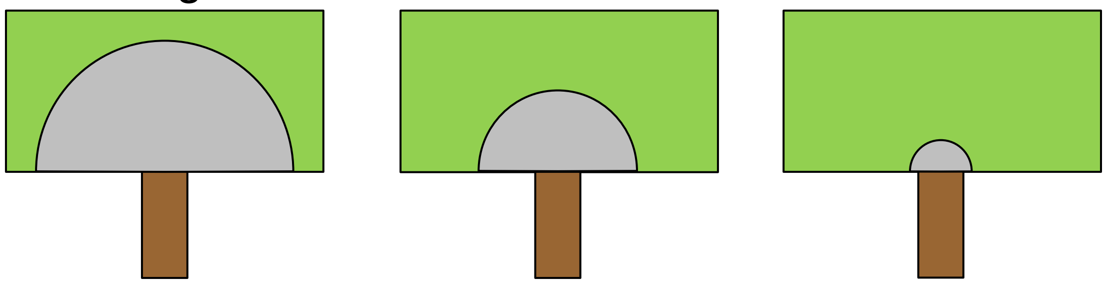
Figure 2. Device structure of VCCPCM array

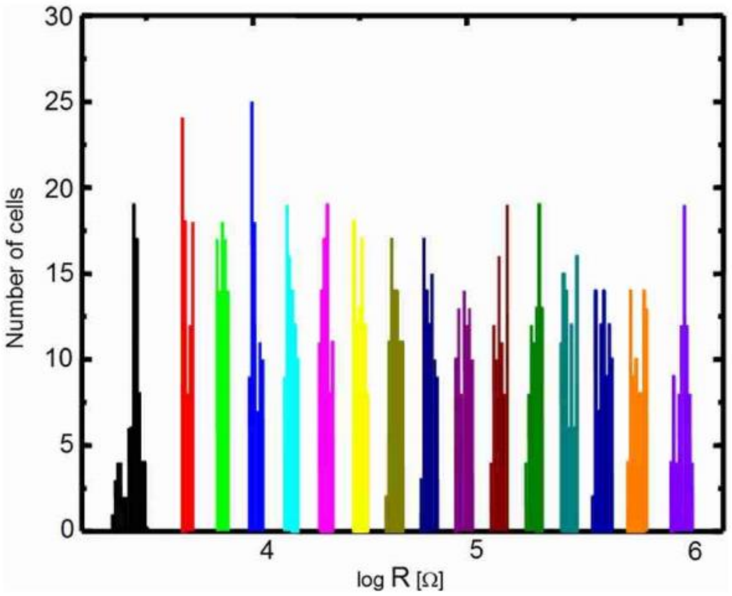


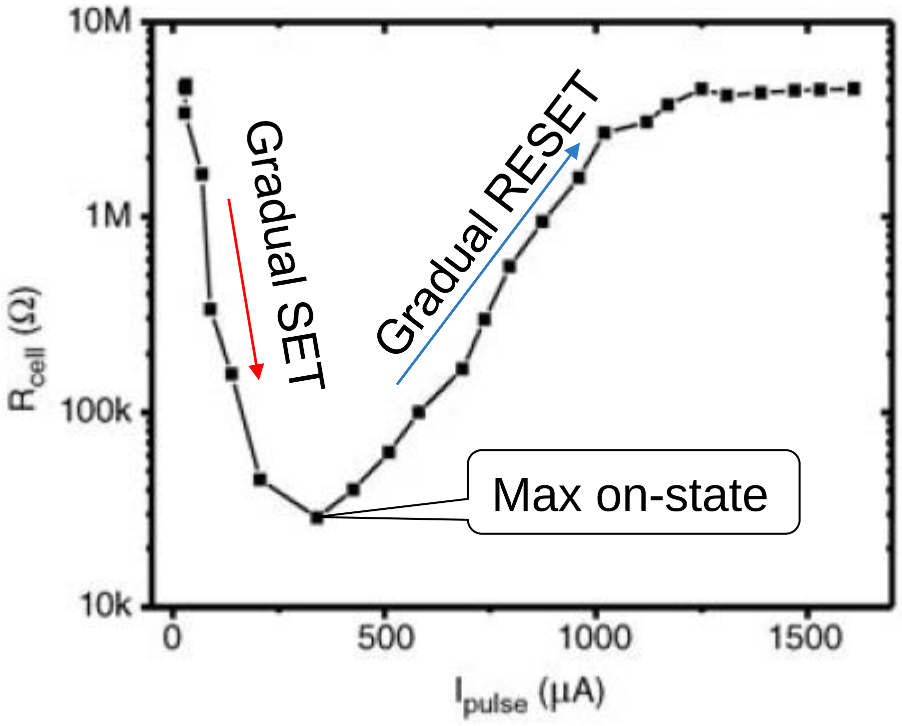
Kinoshita et al VLSI 2012

Multibit operation

- SET level depends on size of amorphous region
- Size changes as function of write pulse amplitude
  - Variations give broad distribution in *R*
- Sequence of write and verify (feedback loop)
  → 16 intermediate levels (4 bit precision)







Multilevel operation is very sensitive to resistance drift!

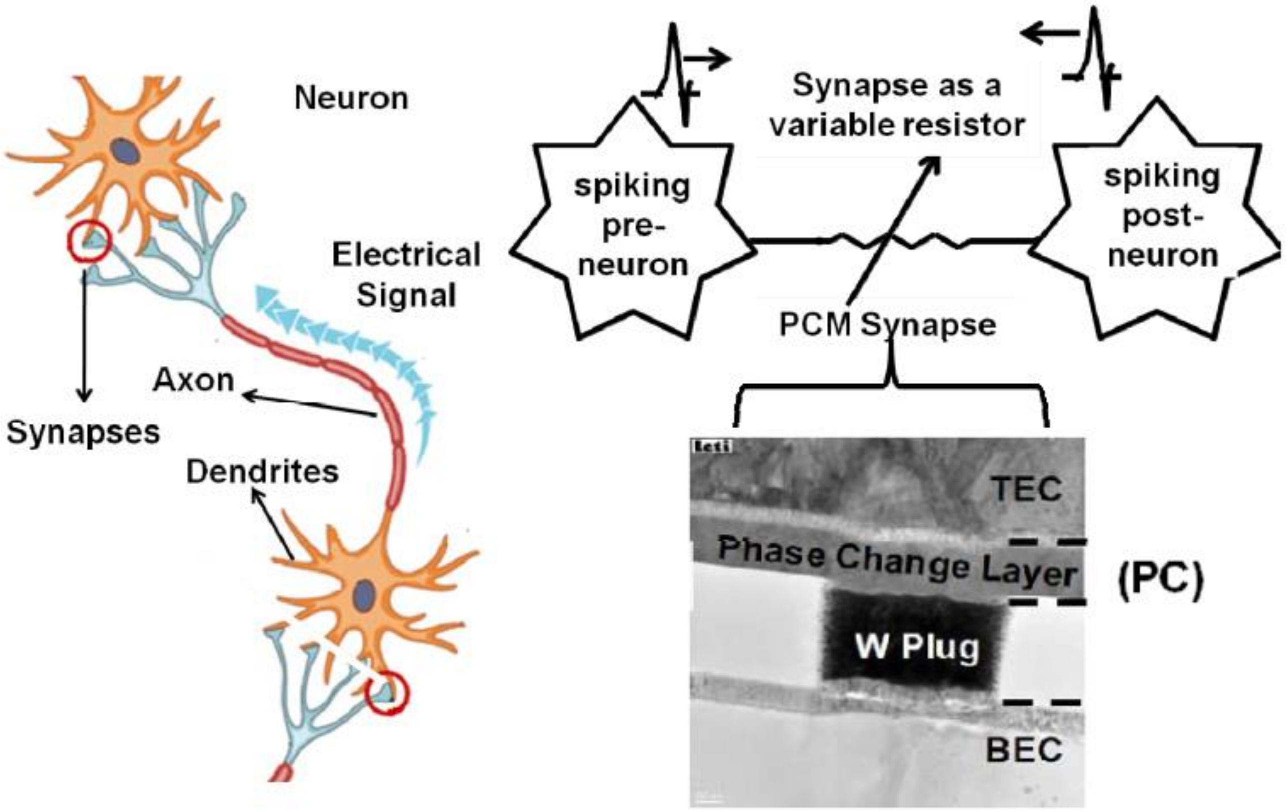
Wong et al. Proc. IEEE 2010

PCM as storage

	DRAM	3DNAND	RRAM	PCM
Nonvolatile	No	Yes	Yes	Yes
Speed (ns)	10	10^4	>5 ns	10 ns
Energy use (pJ/write)	0.1	1	0.1-1	>1
Endurance (cycles)	10^{16}	10^5	10^6-10^7	10^9
Multilevel?	No	Yes	3-6 bit	Yes
Scalability	6-8F^2	3D!	3D!	3D!
Other	Destructive Read	High Voltage	Abrupt SET	R drifts

PCM in neuromorphic computing

- Conductivity ←→ synaptic weight
- Has been used also for neuron implementations!

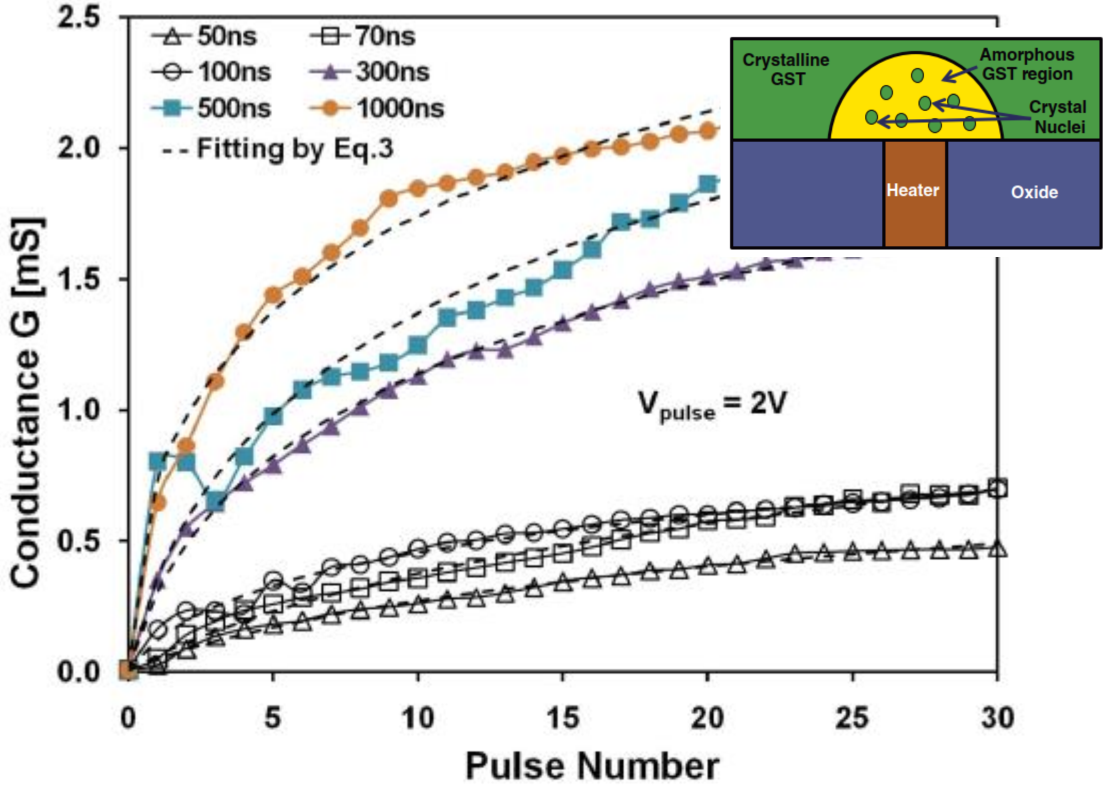


Suri et al. IEDM 2011

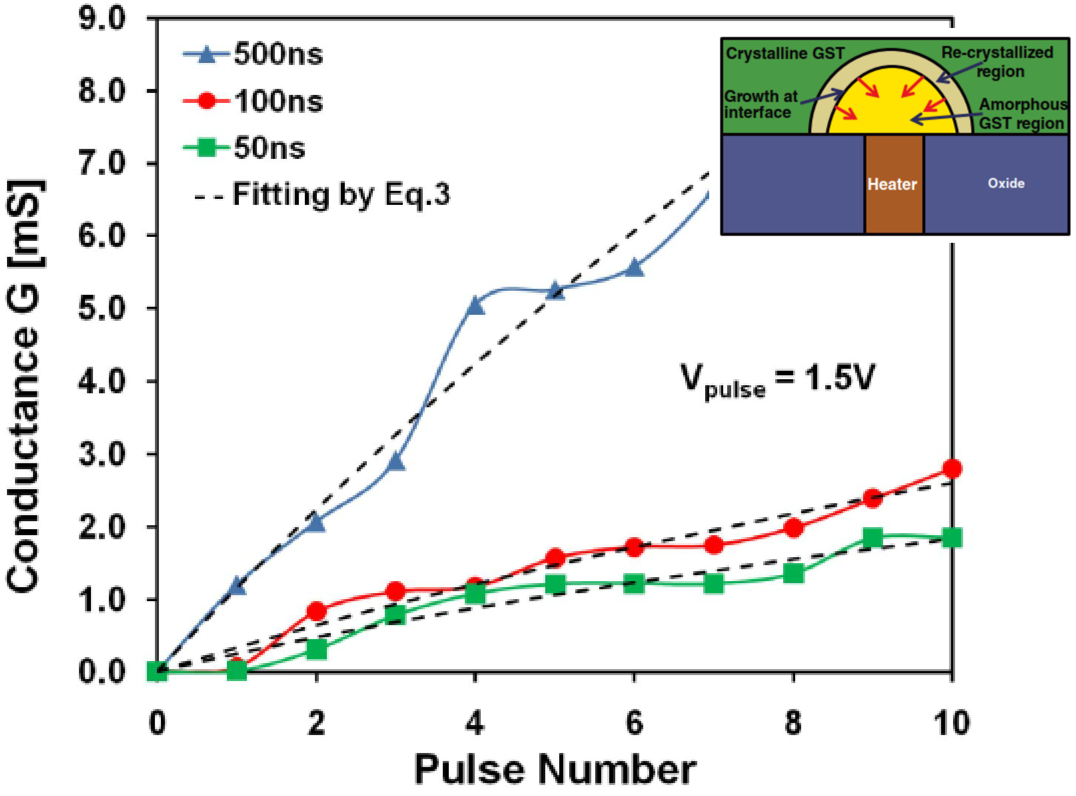
Gradual SET

- → Long Term Potentiation
- Nucleation dominated → more gradual conductance change compared to Growth-dominated

Growth-dominated (GeSbTe)



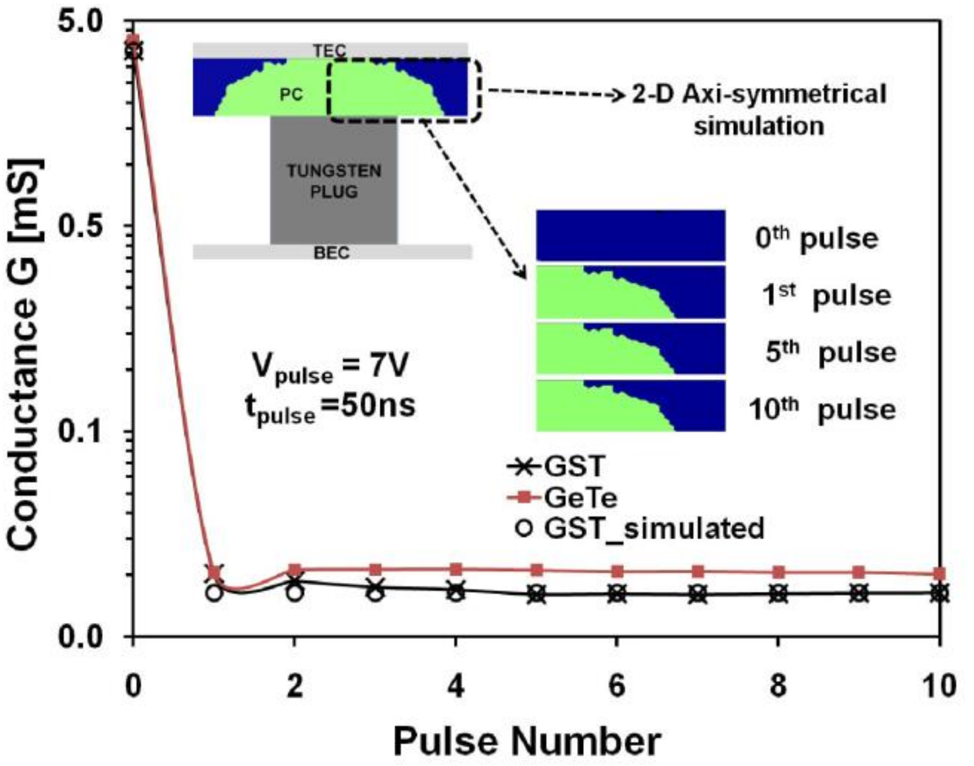
Nucleation-dominated (GeTe)



Suri et al. IEDM 2011

Gradual RESET

- → Long term depression
- Cannot be achieved by repeating pulses with same amplitude
- Increasing amplitude is necessary for gradual RESET → difficult in practice



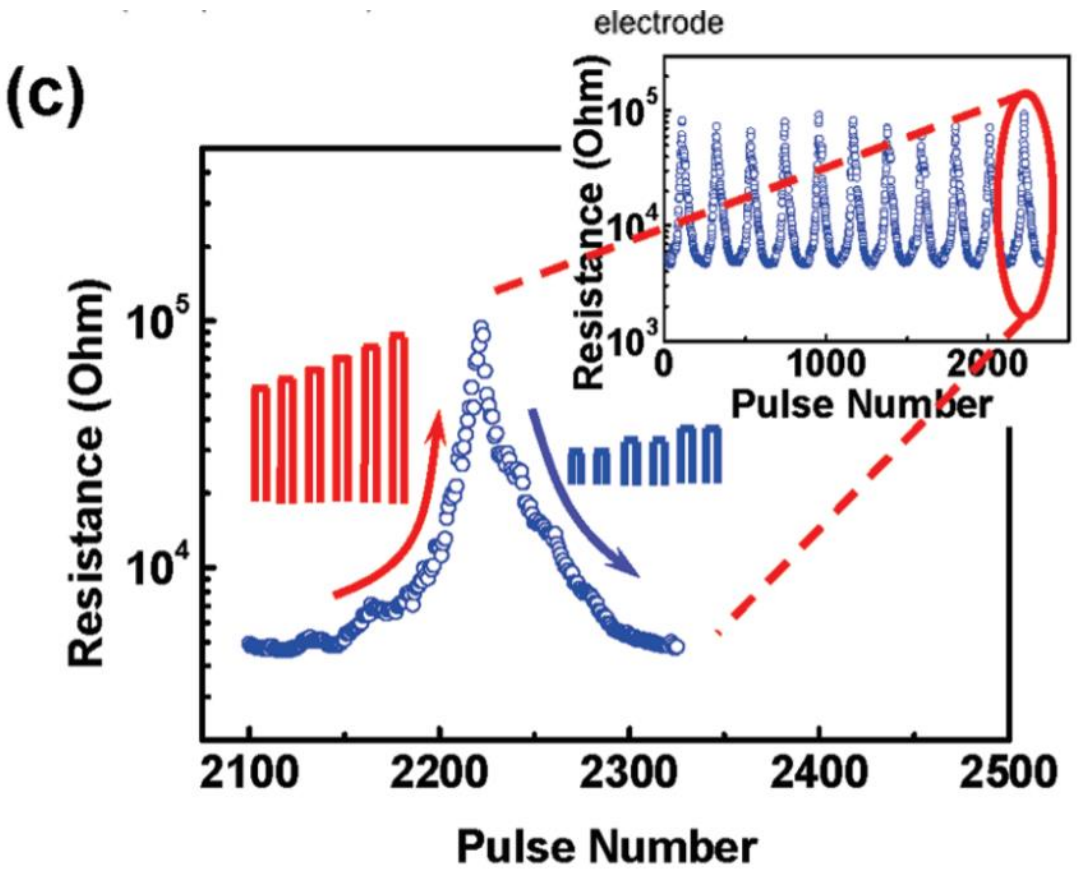
Suri et al. IEDM 2011

PCM as artificial synapse

- Conductivity ←→ synaptic weight
- SET is gradual, while RESET is abrupt

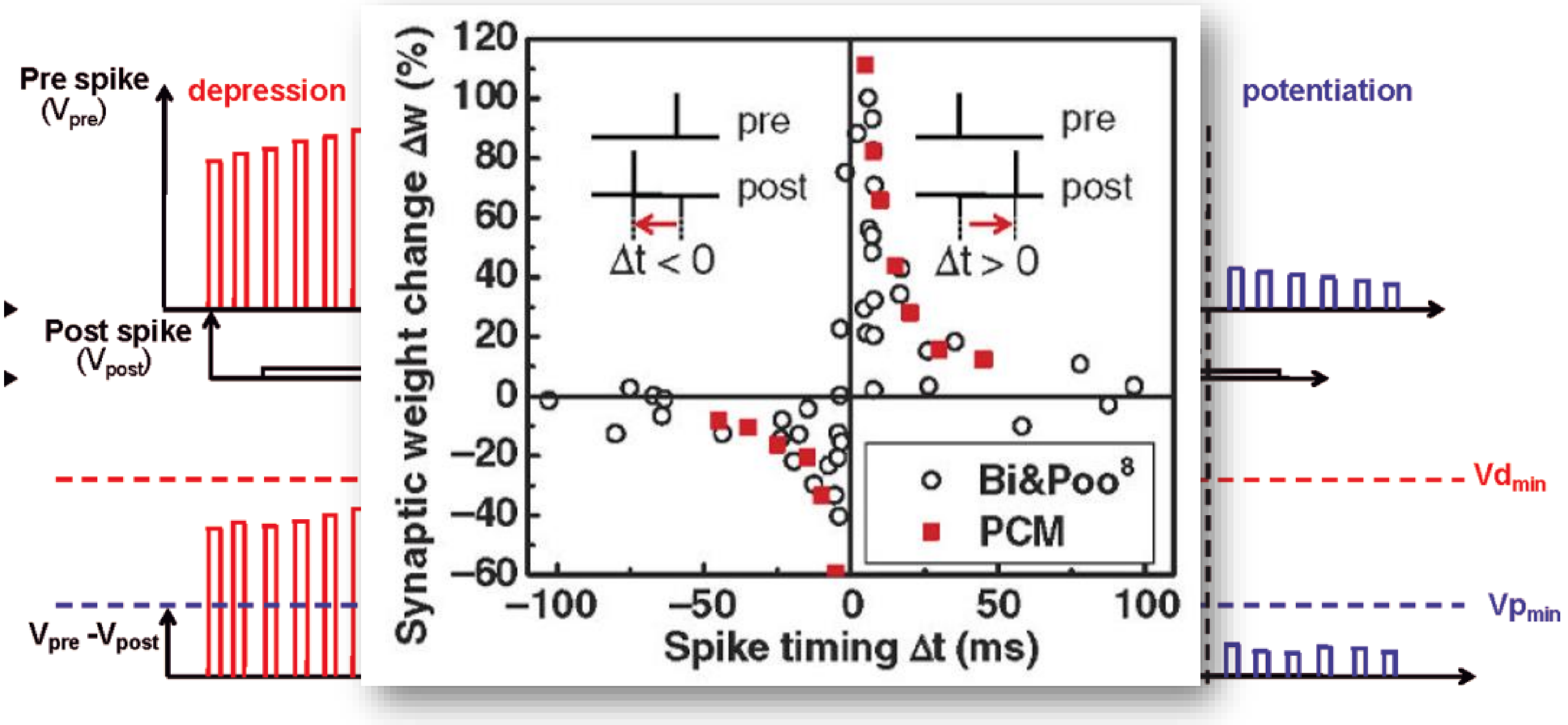
→ Asymmetry in conductivity (weight) change

- Can be amended by variable pulse heights for potentiation and depression



Kuzum et al Nano Lett. 2012

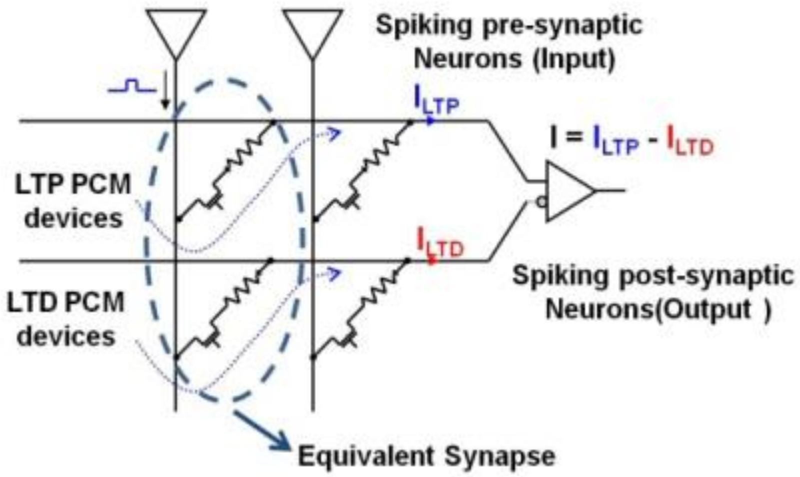
STDP protocol



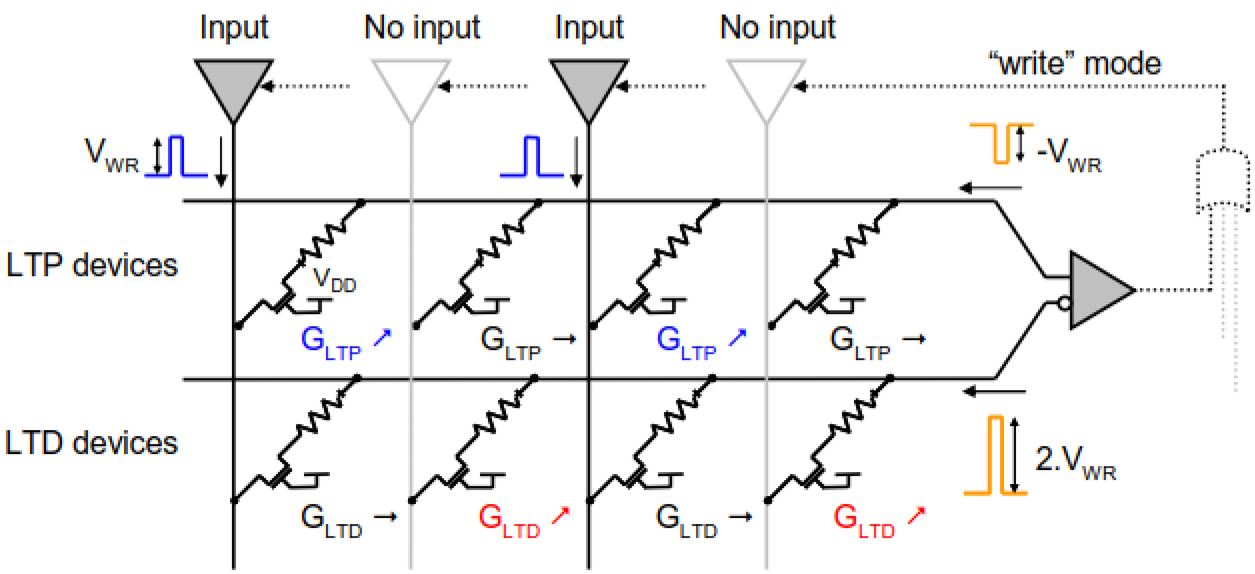
Kuzum et al Nano Lett. 2012

2-PCM synapse

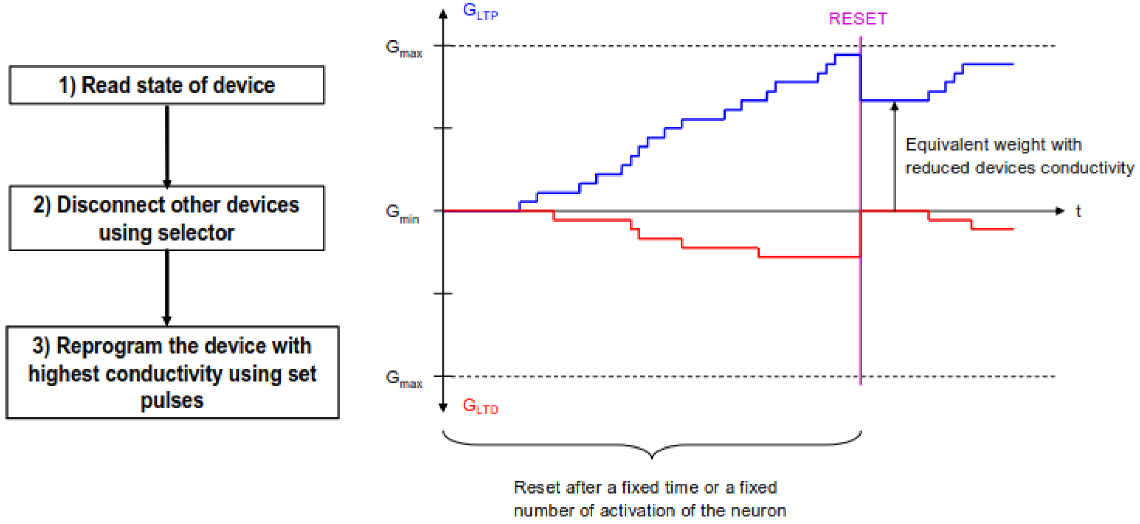
- Better way to address the asymmetric SET/RESET
- Each synapse → 1 pair of PCM's, (LTP PCM and LTD PCM)
- Signal to post-neuron $I_{post} = I_{LTP} - I_{LTD}$
- Intermittent RESETs needed to adjust conductivity (for every 10-25 SET pulse)



Weight update scheme



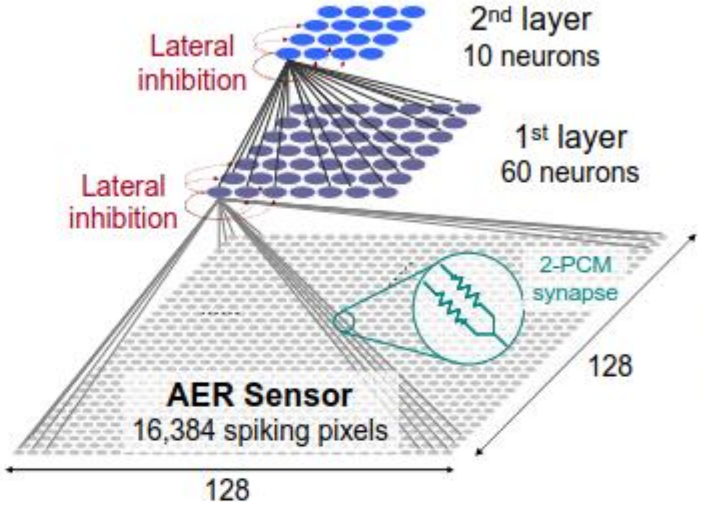
Intermittent RESET scheme

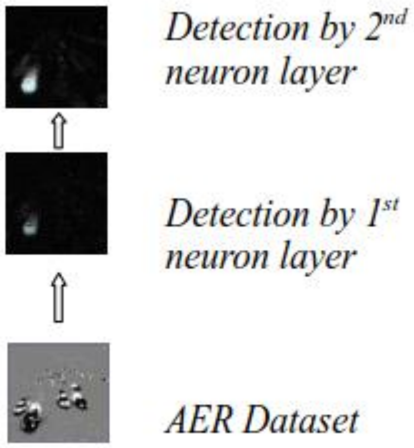


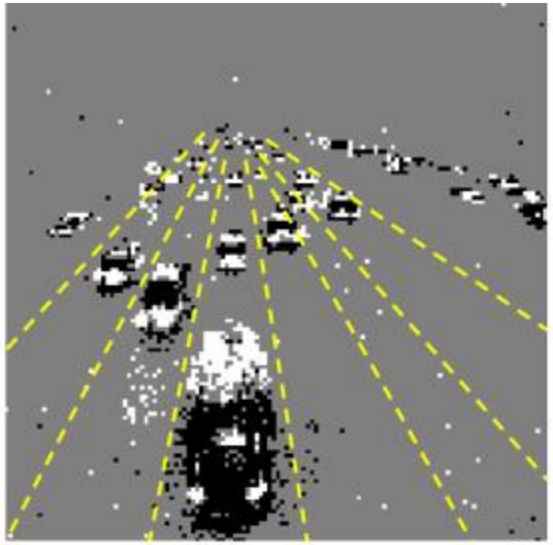
Suri et al.

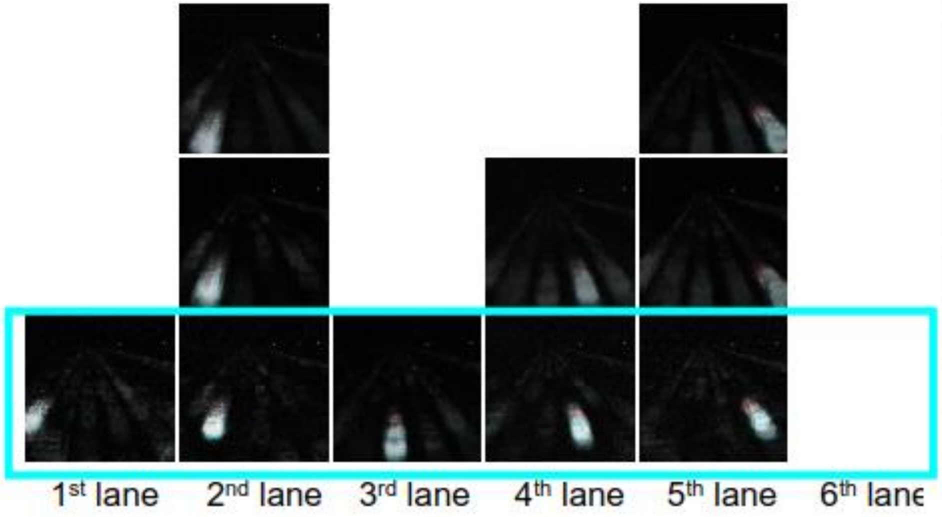
Performance in action

- Car lane detection
- GeSbTe needed less RESETs (1:35) vs (1:10)
- GeTe achieved better learning
  - 5 of 6 lanes
  - > 90% detection in 4
  - Due to better linearity in GeTe?
- Trained by STDP for 680s
- Power consumed for learning <u>112 µW!</u>
- GeTe demands more power (315 µW)









Car Detection %		
Lane	PCM	
	GST	GeTe
1st	N.A.	88
2nd	100	91
3rd	89	96
4th	89	97
5th	96	100
6th	N.A.	N.A.