# Hien Vu

hienvu@purdue.edu · 608-515-2815 · hienvuvg.github.io · linkedin.com/in/hienvuvg

A researcher specializing in the end-to-end development and optimization of machine learning models, wireless sensing, and embedded systems. Seeking an R&D role (co-op or intern) to translate complex research into tangible technological solutions.

## EDUCATION

**Ph.D. in Electrical and Computer Engineering** , GPA: 3.65 (candidate) 2024–2026 (expected)
*Purdue University, West Lafayette, Indiana, USA*

**M.Sc. in Electrical and Computer Engineering**, GPA: 3.82 2021–2023
*University of Wisconsin–Madison (UW-Madison), Wisconsin, USA*

**B.Sc. in Electronics and Telecommunications Engineering**, GPA: 3.5 2014–2018
*Hanoi University of Science and Technology (HUST), Hanoi, Vietnam*

## KEY SKILLS

- **Hardware & Embedded**: Verilog, MIPS, RISC-V, PCB Design (Altium), mmWave, UART/I2C/SPI, RF and high-speed design.
- **Software & Algorithms**: Python, C/C++, MATLAB, assembly; sensor fusion, computer vision, signal processing.

## PROFESSIONAL EXPERIENCE

**Research Assistant**, **NEIS Lab, Purdue University, Indiana, USA** 2024–Present

- Engineered an advanced mmWave radar and Edge AI system to track respiration of multiple moving subjects, achieving high accuracy in harsh environments for health monitoring applications.
- Architected an end-to-end multimodal sensor fusion pipeline for behavior classification, providing strategic insights on design trade-offs to optimize system cost and complexity.
- Recruited and trained a team of 20+ people to curate a massive multimodal dataset (20k RGB images, 300k seconds of data) for accelerating research in temporal-behavior classification.

**Research Assistant**, **WISEST Lab, UW-Madison, Wisconsin, USA** 2021–2024

- Designed a wearable sensor tag with a shared-coil architecture for simultaneous RFID and wireless charging, solving mutual coupling problem to realize a compact wearable design.
- Developed an optimized embedded firmware that reduced RFID energy costs by 15x and engineered a closed-loop wireless power transfer protocol to enable perpetual device operation.
- Collaborated with cross-discipline teams to design and deploy a multi-node IoT network, analyzing over 2,000 hours of field data to validate system reliability in complex operational settings.

**Research Assistant**, **EC Lab, Soongsil University, Seoul, South Korea** 2019–2021

- Designed a flexible, portable supercapacitor power device delivering 840W pulses, optimizing energy density for high-demand and critical military applications (photos 🖼).
- Developed a bidirectional buck-boost control algorithm enabling uninterrupted power delivery and continuous system operation under dynamic load conditions.
- Implemented a high-speed FPGA-based design for 512GB SLC-NAND flash storage, ensuring signal integrity and minimizing propagation delay across 1,000+ components (photos 🖼).
- Implemented an Extended Kalman Filter on a RISC-V MCU to process 9-DOF IMU data, integrating with Parallel Tracking and Mapping (PTAM) for real-time 3D pose estimation in AR applications (see demo ▶).

**Research Assistant**, **SPARC Lab, HUST, Hanoi, Vietnam** 2015–2018

- Built a gyroscope-based balancing system using Linear-Quadratic-Gaussian regulator for two-wheeled vehicles.
- Managed a team of 10+ people to design, produce, and deploy 100 air-quality monitoring devices throughout Hanoi city.

## SELECTED PROJECTS

**MmCows: Multimodal Deep Learning Benchmark (NeurIPS)** 2024

- Created a large-scale multimodal dataset accepted as a Spotlight paper (top 5% of ratings) at NeurIPS 2024. Benchmarked state-of-the-art action recognition models to advance edge computing capabilities.

**eTag: Battery-Free Wireless Sensing System (ACM MobiCom)** 2023

- Developed an end-to-end energy-neutral sensing system published at ACM MobiCom (24% acceptance rate), leveraging backscattering for communication and inductive coupling for power delivery, enabling maintenance-free health monitoring.

**5-Stage Pipelined CPU Design** | Course Project 2022

- Designed and verified a fully functional 32-bit MIPS processor in Verilog with 5-stage pipeline and L1-level cache. Engineered hazard detection units and data forwarding paths to resolve data and control hazards.