LIGENTEC

Design verification report

Design name: 2204_RMIT_80040_AN800_v1.gds
Submission date: 28/10/2025
Reviewer: Emmanuel Gooskens
Summary of report: Design violations / errors present - resubmission required

No.	Status description	Current Status
1	Design is accepted for production with no violations	
2	Design is accepted for production with Ligentec-accepted violations.	
3	Design violations / errors present - resubmission required	X
4	Design is accepted for production with waived violations by the customer (see waiver section)	

Following the submission of your design, LIGENTEC is providing you with information regarding design rule violations, design submission violations and other errors present on the submitted design. Attached to this report is the DRC output file please see the end of this report for instructions on how to use this file.

It is important to keep in mind that the design rules are there to ensure your design has the best chance of success. By ensuring your design is free from all violations gives you protection against low yield and increases the reliability of the design. LIGENTEC advises that all violations are corrected, regardless of the severity.

Violations fall into two categories:

- Design rule check (DRC) violations - These are violations found using our DRC script, this will check that the geometric properties of your design follow our design rules, it does not check circuit functionality.
- Design submission check (DSC) violations - These are violations of the rules we have in place to ensure your design is compatible with our process. DSC violations will not appear in the output file attached to this report.

Each violation has a related severity:

- Fatal - This violation must be corrected either because it will cause issues to our process or because the yield will be so low it would not make sense.

- Critical - This violation will cause unpredictable yield and reliability hazards. LIGENTEC will not compensate you for any yield loss and manufacture is entirely at your own risk.
- Warning - Correction is advisable.

DRC violations

Rule	Description	Severity	Comments
1.0 DRC.X1PWidth	X1P width must be >= 0.2 µm.	Critical	Please fix all width violations. Check the DRC FAQ document for more details. # violations: 6
1.0 DRC.X1PFWidth	X1P width must be >= 0.180 µm.	Fatal	Please fix all width violations. # violations: 6
2.0 DRC.X1PSpacing	X1P spacing must be >= 0.3 µm.	Critical	Please fix all spacing violations. Check the DRC FAQ document for more details. # violations: 15760
2.0 DRC.X1PFSpacing	X1P spacing must be >= 0.2 µm.	Fatal	Please fix all spacing violations. # violations: 6
2.0 DRC.X1PSpacing_WARNING	X1P spacing must be >= 0.3 µm.	Warning	Recommended to check these results for possible design mistakes. # violations: 46999
31.0 DRC.P1PWidth	P1P width must be >= 0.8 µm.	Fatal	Please fix all width violations. # violations: 18
32.0 DRC.P1PSpacing	P1P spacing must be >= 1.2 µm.	Fatal	Please fix all spacing violations. # violations: 13
36.0 DRC.VIAARea	VIA size is not conformal with 0.36 µm x 0.36 µm size.	Fatal	Please fix all violations. # violations: 1458

313.0 DRC.P1RManhattanRouting	P1R should follow Manhattan routing.	Critical	

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DSC violations

Rule	Description	Severity	Comments
200 DSC.FileReadable	File must be readable by Klayout	Passed	
201 DSC.MultipleTopCells	Layout cannot have multiple topcells	Passed	
202 DSC.TopcellName	TopCell name (TOP) must be changed to TOP.	Passed	
204 DSC.DatabaseUnit	Database unit (grid) must be 0.001 um	Passed	
205 DSC.OriginCheck	The origin must be placed at the lower-left boundary of the design (lower left of the CSL)	Passed	
206 DSC.ForbiddenLayers	Only the layers specified by LIGENTEC can be present on the design	Passed	
207 DSC.CSL/CHS missing	Both the CHS and CSL layers must be present on the design	Passed	
208 DSC.DieSizeError	The dimensions of the die do not match with the ones agreed.	Passed	
210 DSC.EmptyCellError	Empty cells should be removed.	Passed	
209 DSC.DegenerateBoundaryError	Zero-area shapes are not allowed.	Passed	
212	Cell name is not in the library.	Passed	

DSC.BlackBoxErrorName			
213 DSC.BlackBoxDimensions	Cell center/width/height does not match with BB.	Passed	
214 DSC.BlackBoxPinLocations	Pins locations do not match with the BB.	Passed	
215 DSC.BlackBoxModified	A black box seems to be modified on customer side.	Passed	
203 DSC.Name of the cell is too long.	Name of the cell cannot contain more than 100 characters.	Passed	
217 DSC.P1+layers	Are all expected P1+ layers present?	Passed	
216 DSC.BBR verification.	The BB replacement did not work as expected.	Passed	

LIGENTEC design comments:

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Waivers:

The following DRC and foundry violations are waived by the customer:

Rule	Description	Severity

Customer Signature:

Name/Department/Date

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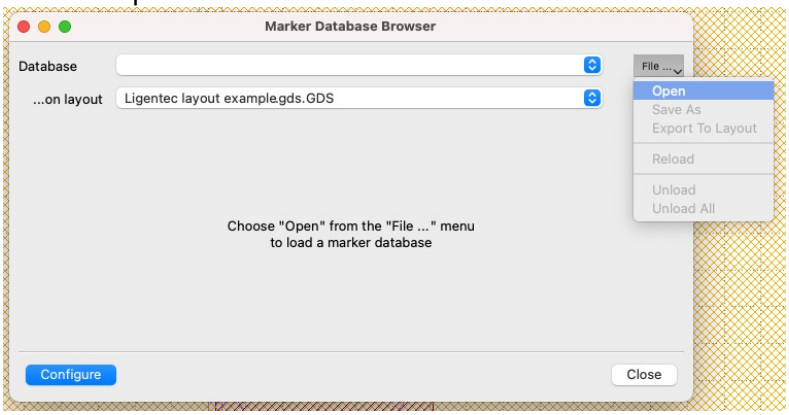
Instruction on viewing the DRC output file

1. Open your original layout file in KLayout
2. Go to Tools>Marker Browser
3. This will open the Marker Database Browser



4. Click on File>Open and select the DRC.results file provided by LIGENTEC
5. The results are then displayed in the Marker Database Browser
6. The violations can be displayed by cell or violation type. By clicking on one of the violations, the layout viewer will highlight that violation.