

**ĐẠI HỌC QUỐC GIA TP.HCM  
TRƯỜNG ĐẠI HỌC BÁCH KHOA**



**BÁO CÁO  
Thiết kế vi mạch  
LAB 1**

Lớp L06		
<b>Nhóm 1</b>		
MSSV	Họ và tên	
2110078	Huỳnh Bảo Duy	100%
2110838	Trần Phúc Chánh	100%
2110677	Tô Minh Vũ	100%
2111196	Trịnh Dương Quốc Hiếu	100%
2113752	Lê Đặng Đăng Khoa	100%

**TP.HCM, tháng 5 năm 2024**

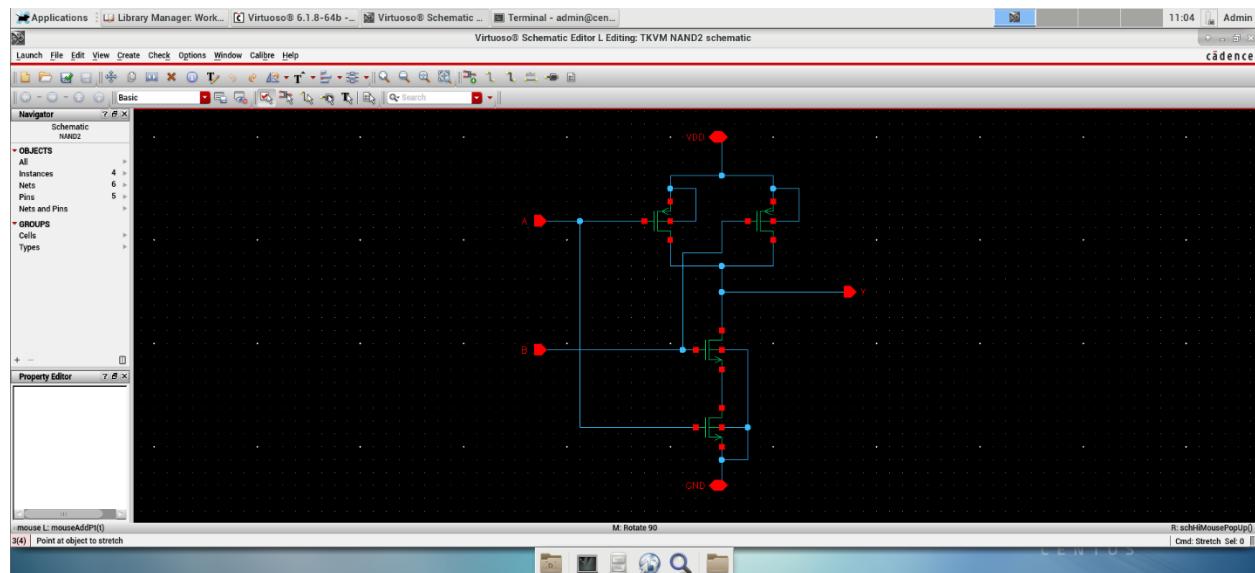
## 1. Experiment 1:

### 1.1. NAND2:

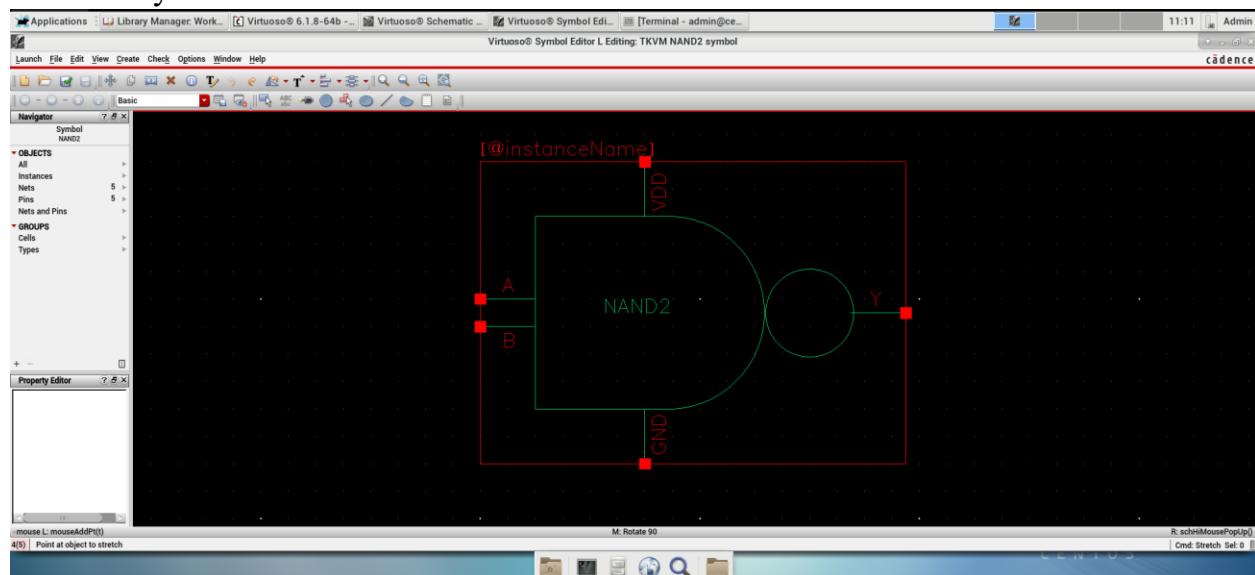
- a. Schematic:
- Truth table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

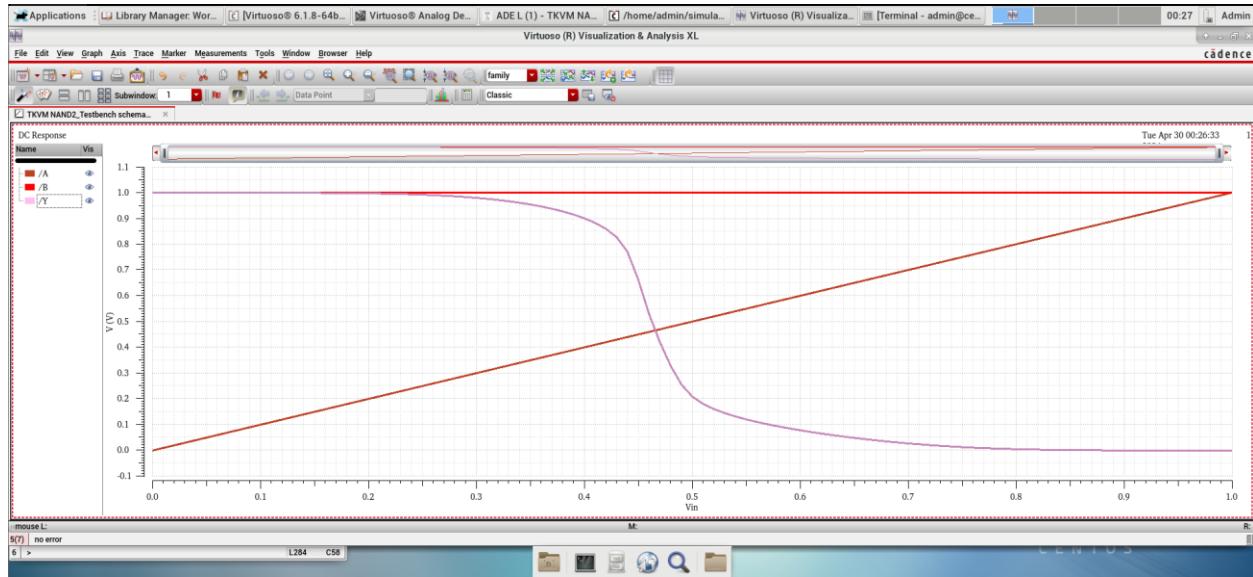
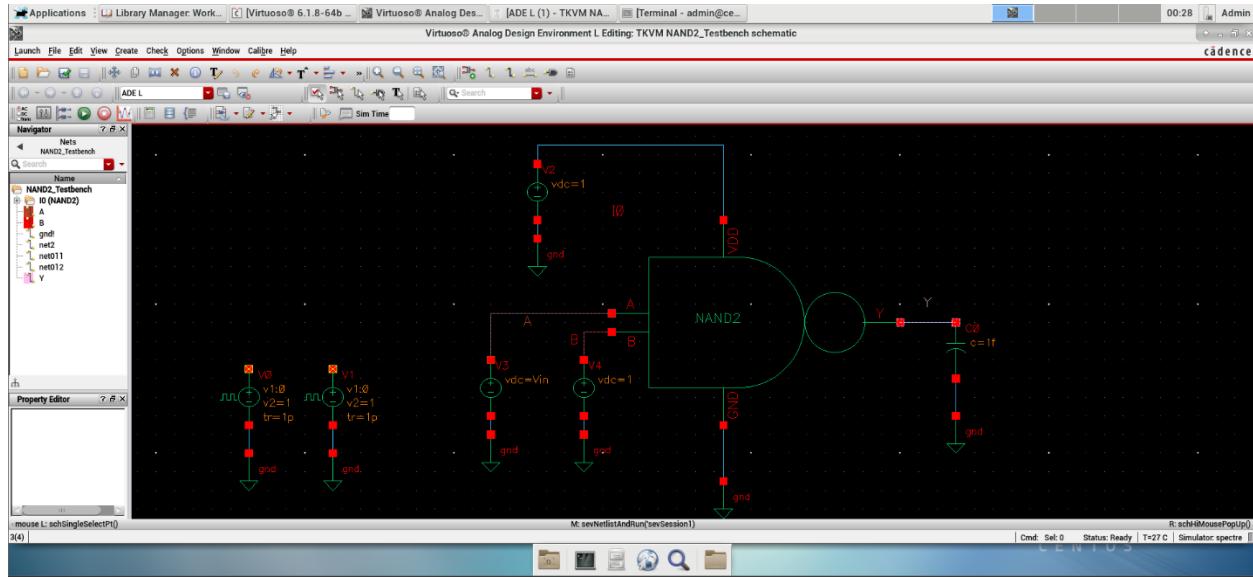
- Schematic:



- Symbol:



## b. DC Analysis simulation:



## c. Transient simulation:

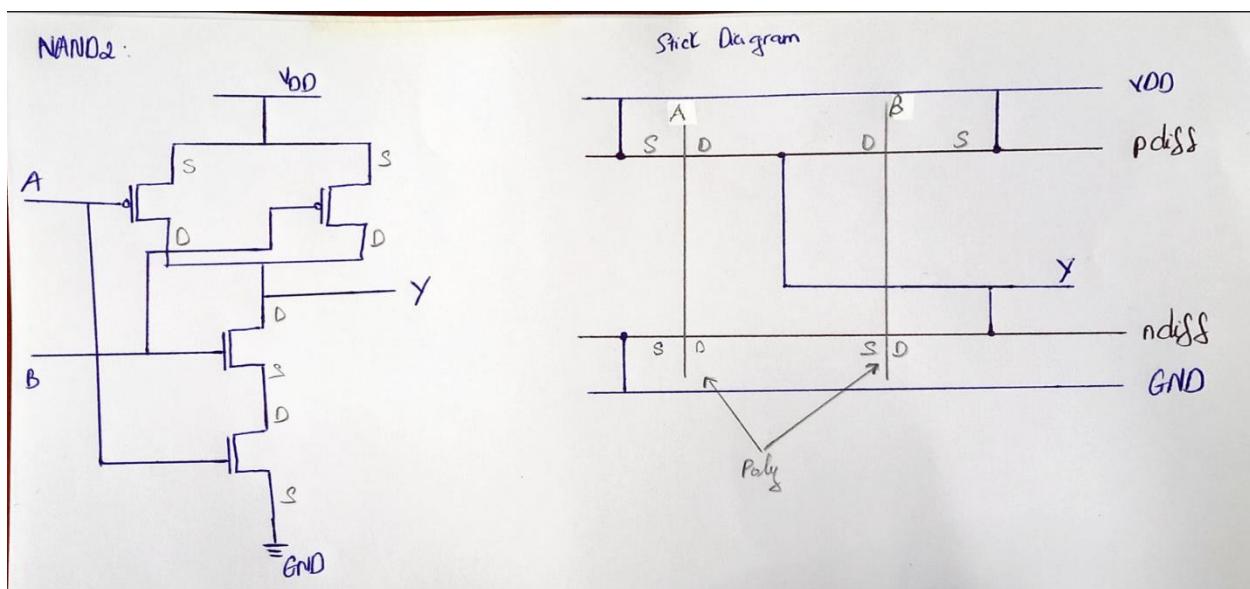
- Testbench circuit for NAND2:

	InA	InB
Voltage 1	0	0
Voltage 2	1	1
Period	4n	2n
Delay time	0.65n	0.8n
Rise time	1p	1p
Fall time	1p	1p
Pulse width	2n	1n

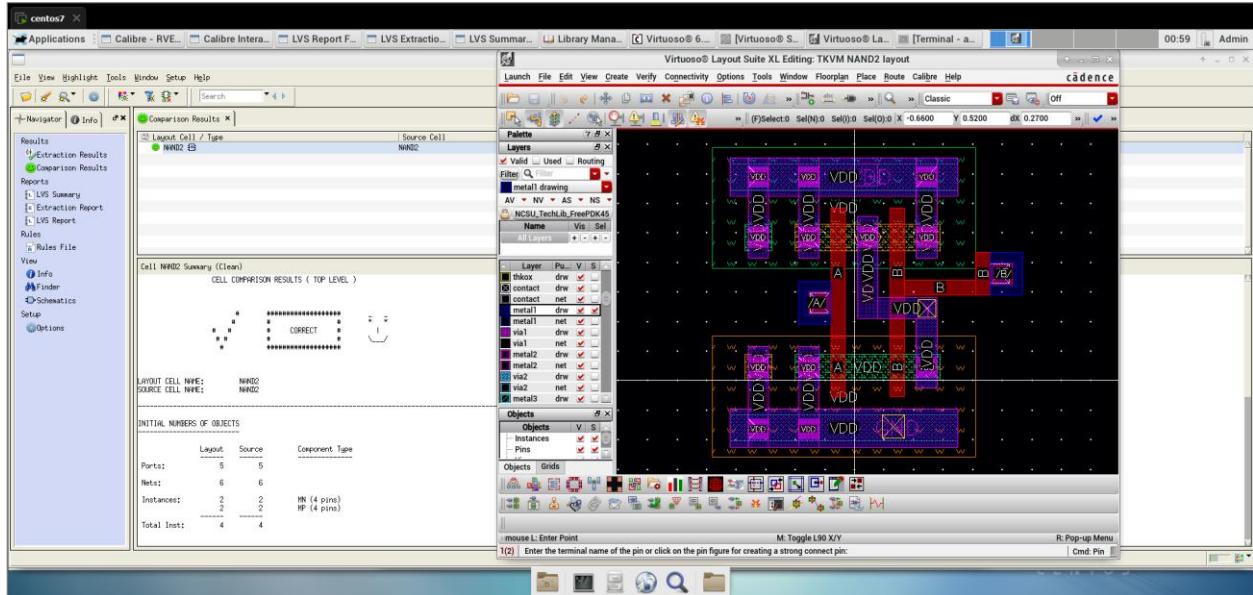
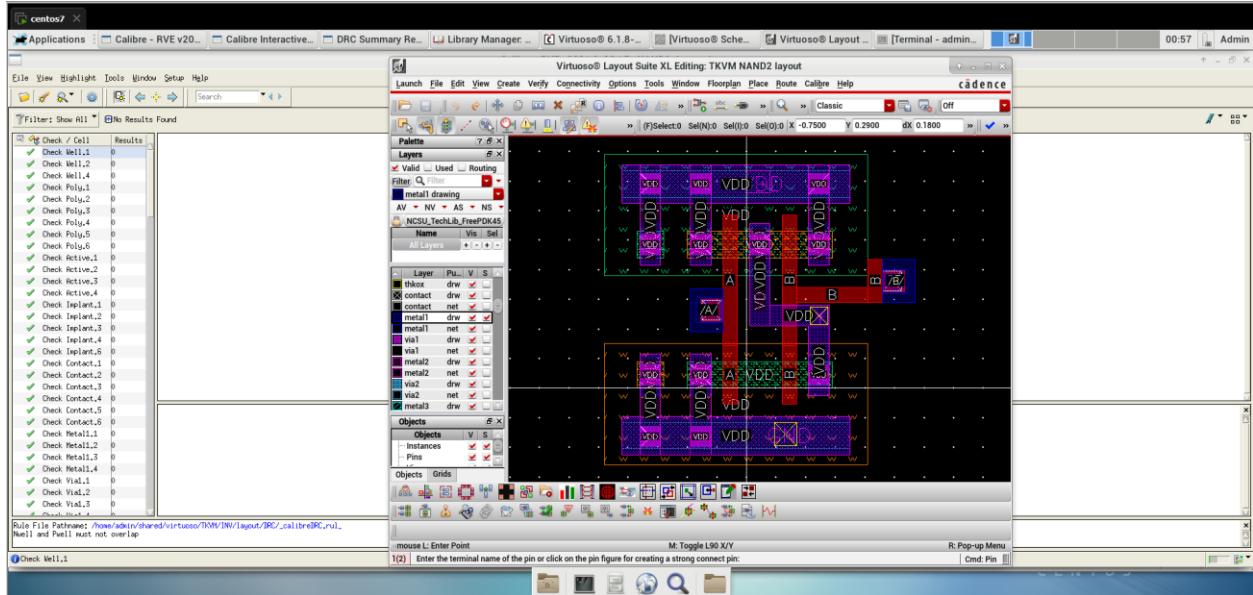


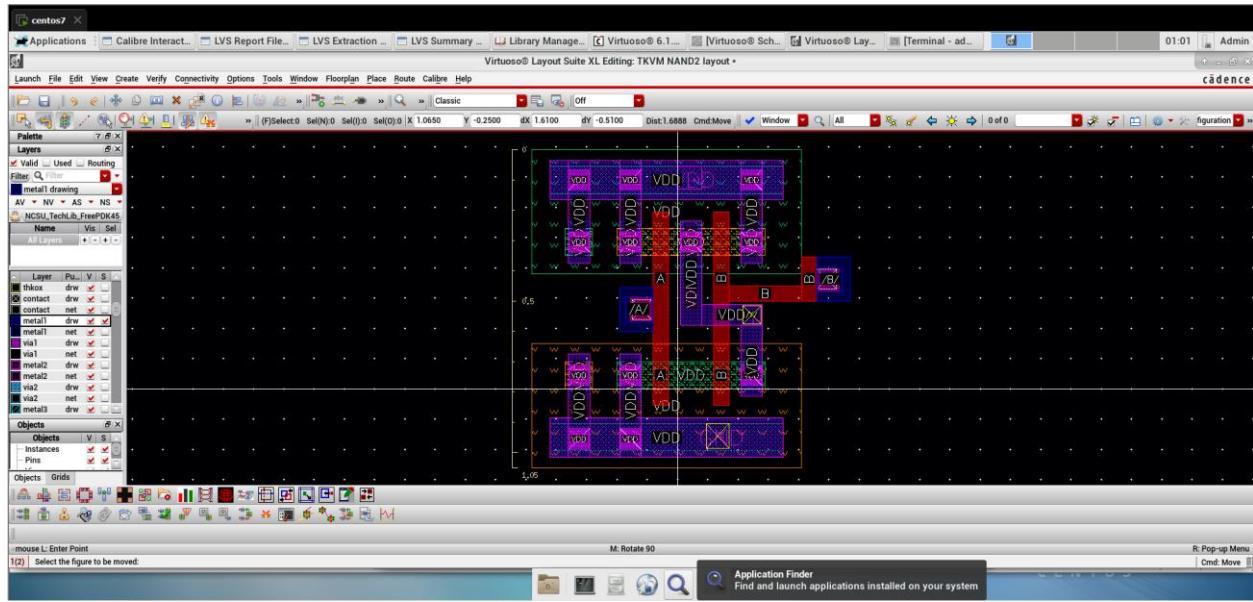
#### d. Layout:

- Stick diagram:



- Layout, check DRC, check LVS:





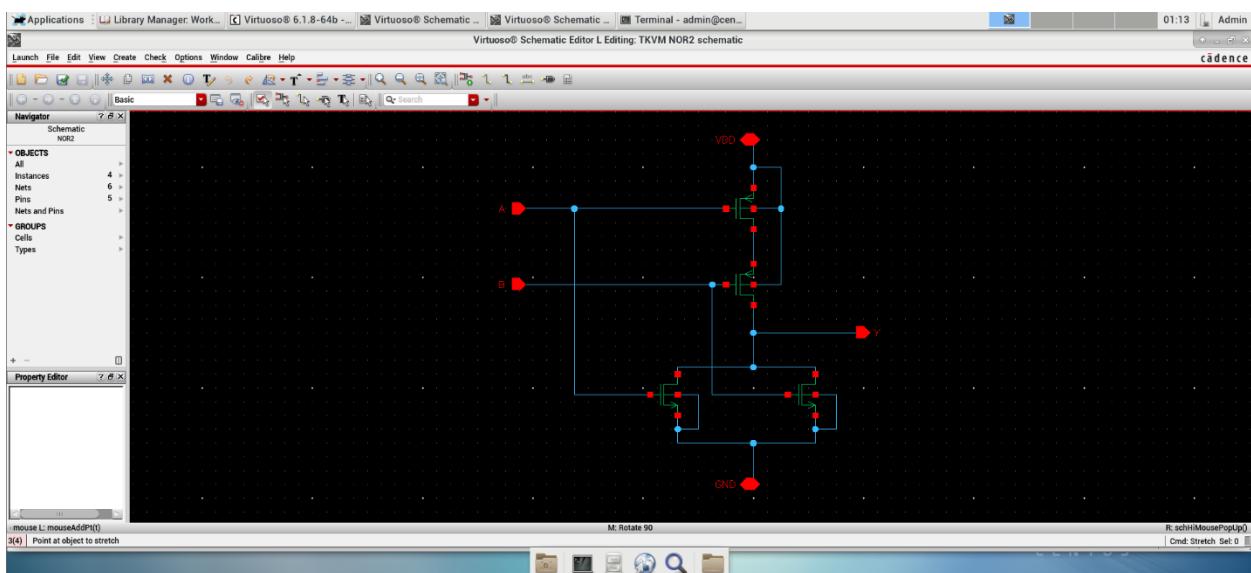
- Cell có độ cao 1.05  $\mu\text{m}$  và làm đúng DRC và LVS.

## 1.2. NOR2:

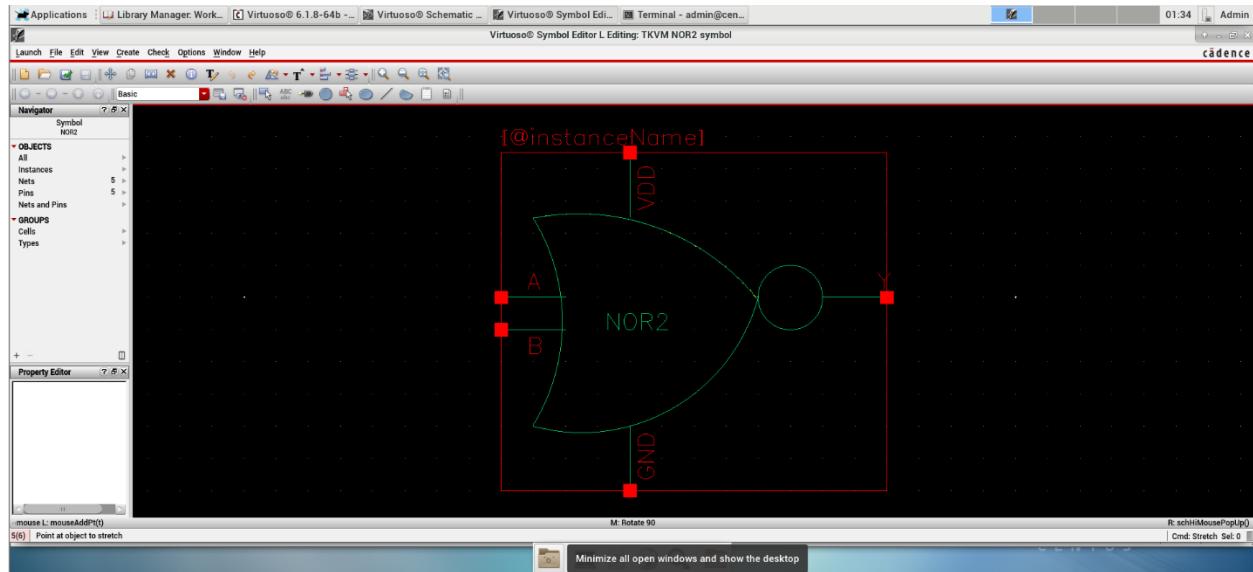
- a. Schematic:
- Truth table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

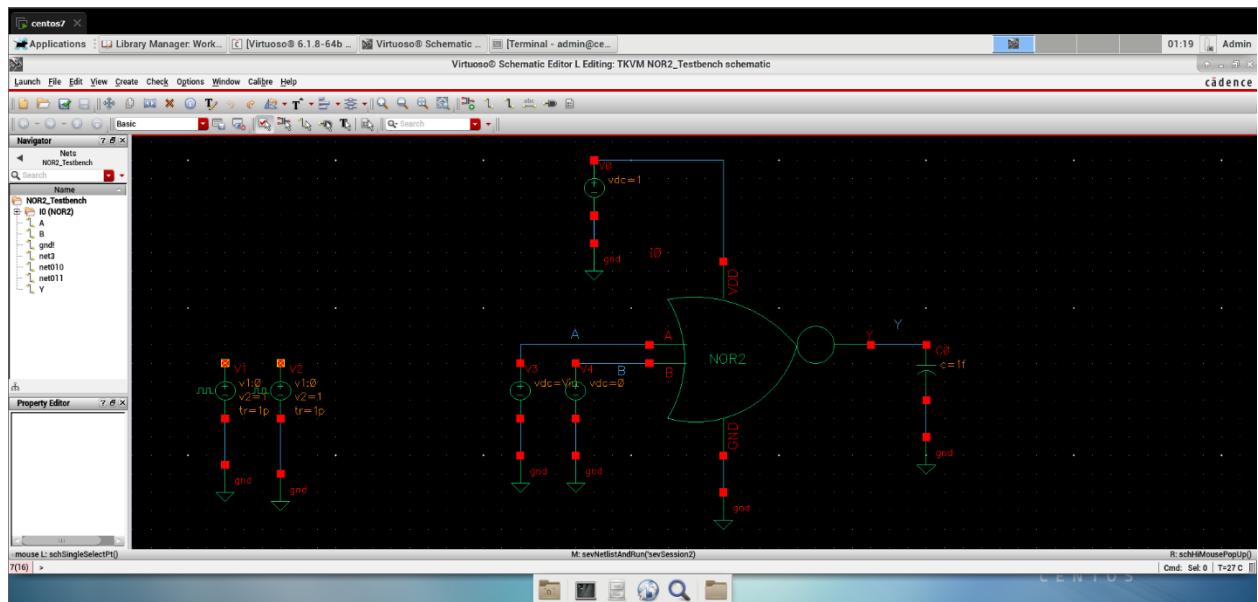
- Schematic:

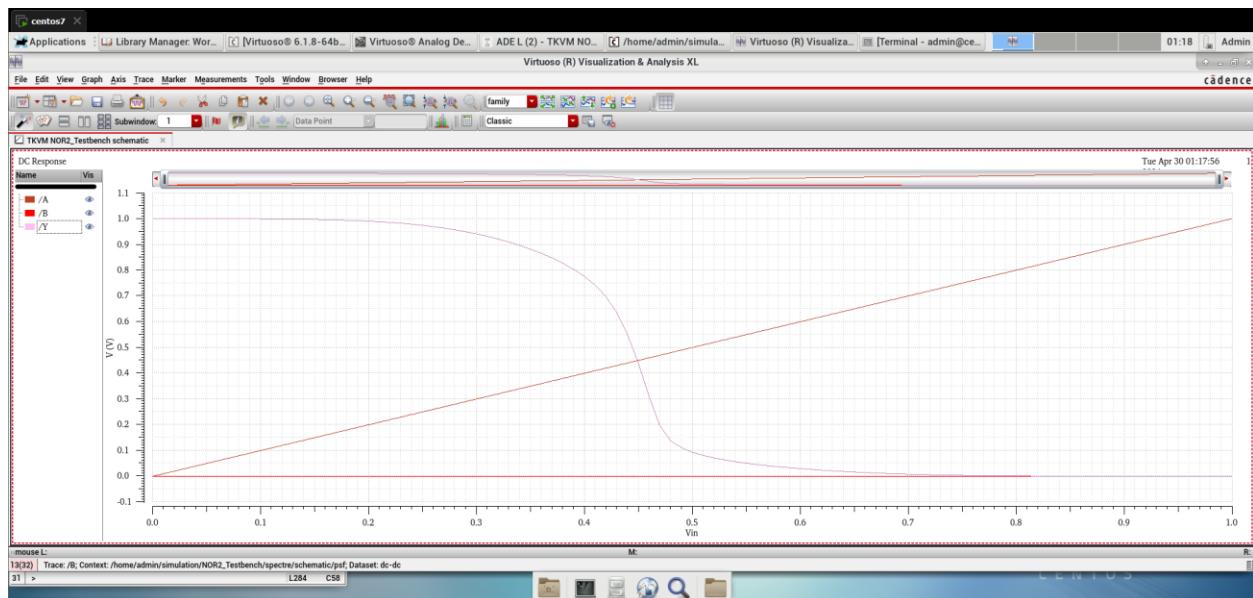


- Symbol:



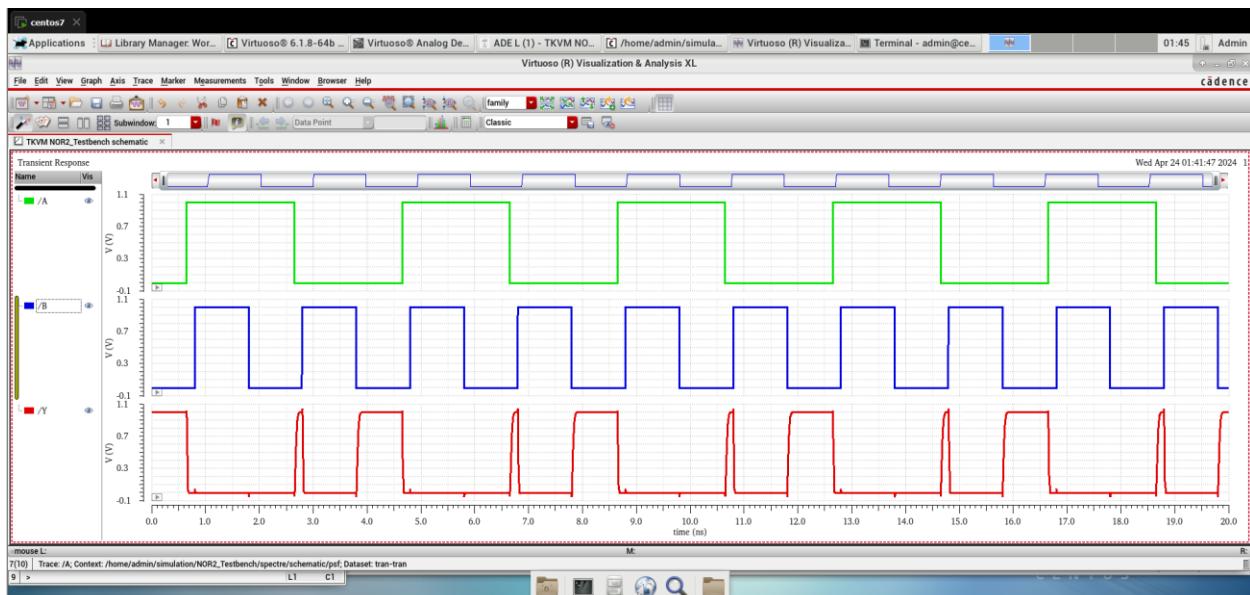
b. DC Analysis simulation:

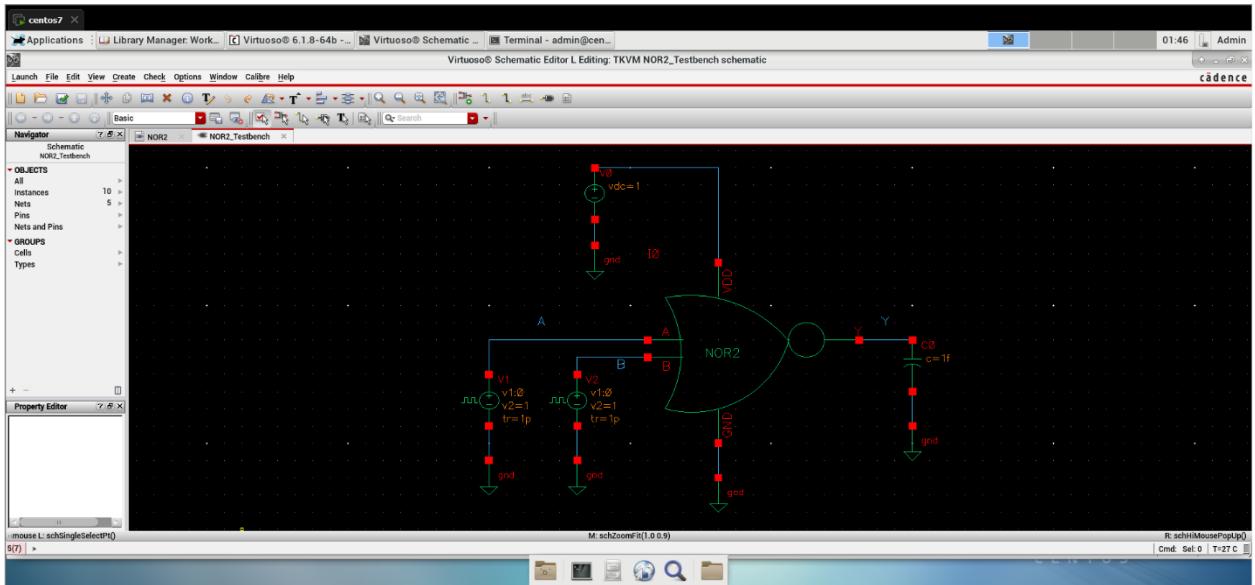




- c. Transient simulation:
- Testbench circuit for NOR2:

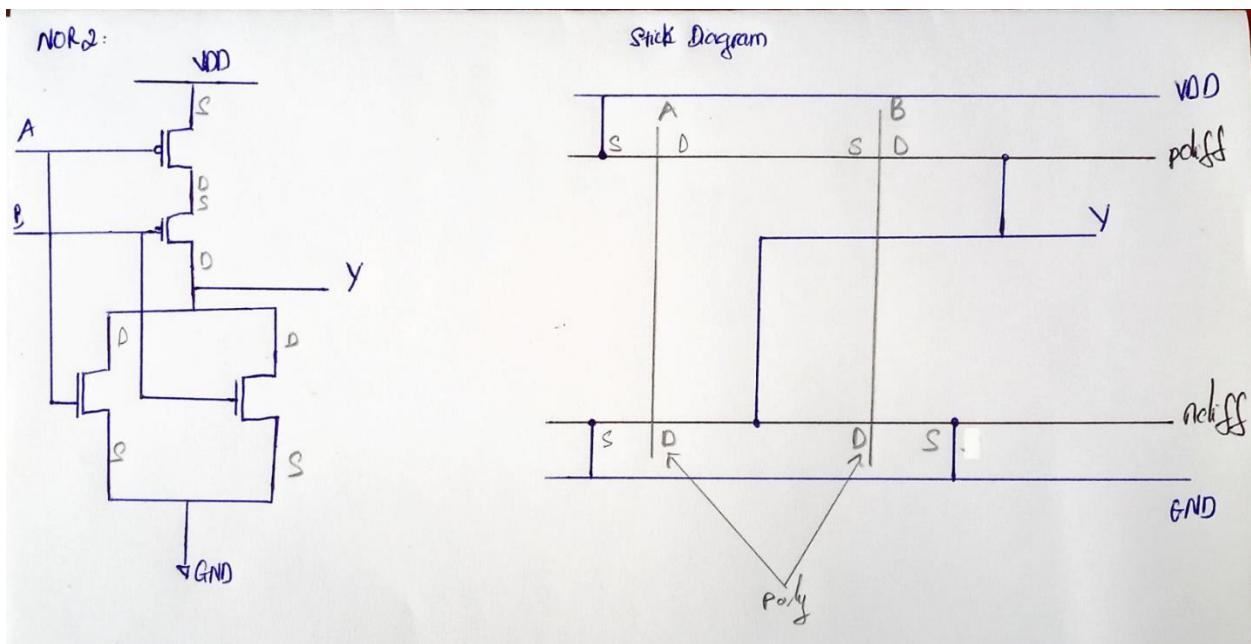
	InA	InB
Voltage 1	0	0
Voltage 2	1	1
Period	4n	2n
Delay time	0.65n	0.8n
Rise time	1p	1p
Fall time	1p	1p
Pulse width	2n	1n



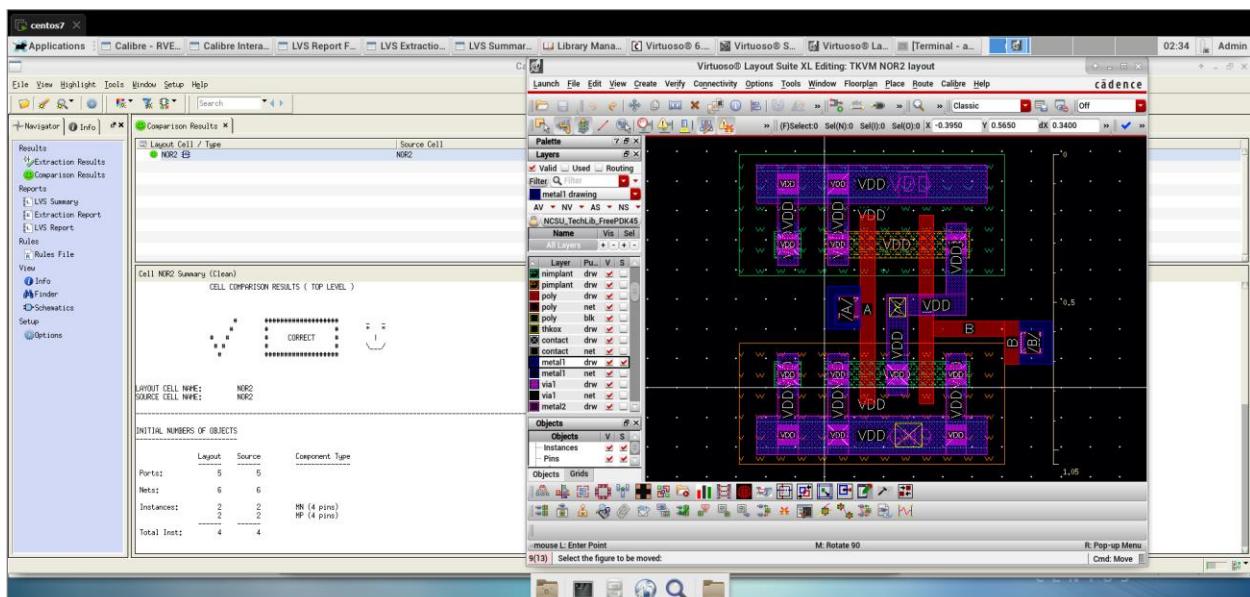
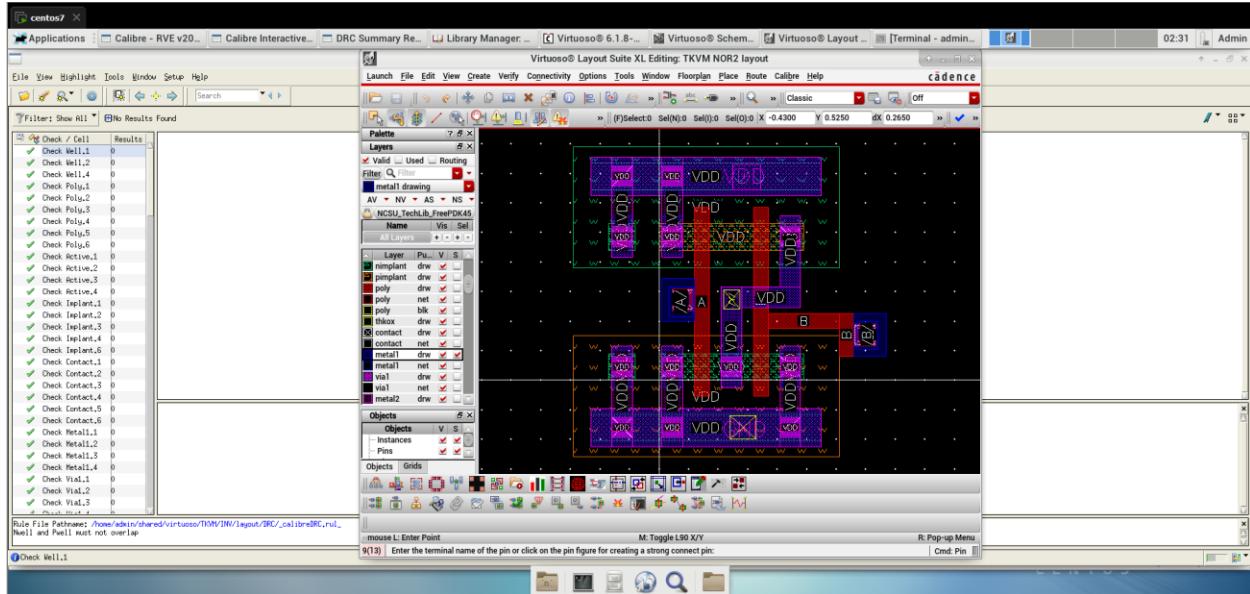


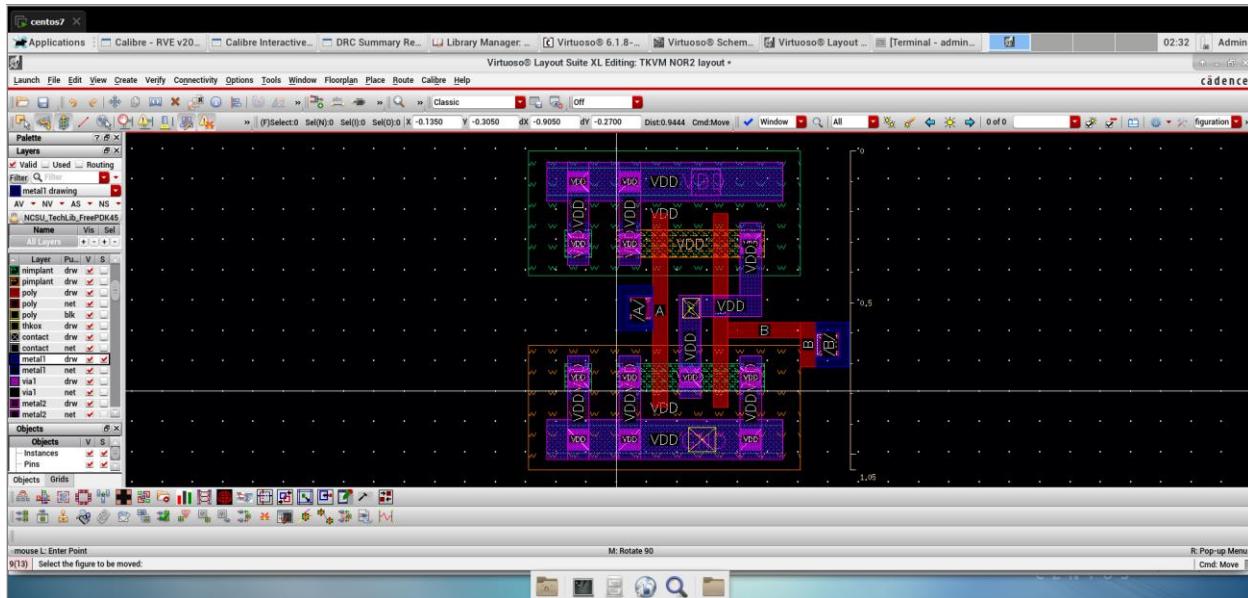
d. Layout:

- Stick diagram:



- Layout, check DRC, check LVS:





- Cell có độ cao 1.05  $\mu\text{m}$  và làm đúng DRC và LVS.

## 2. Experiment 2:

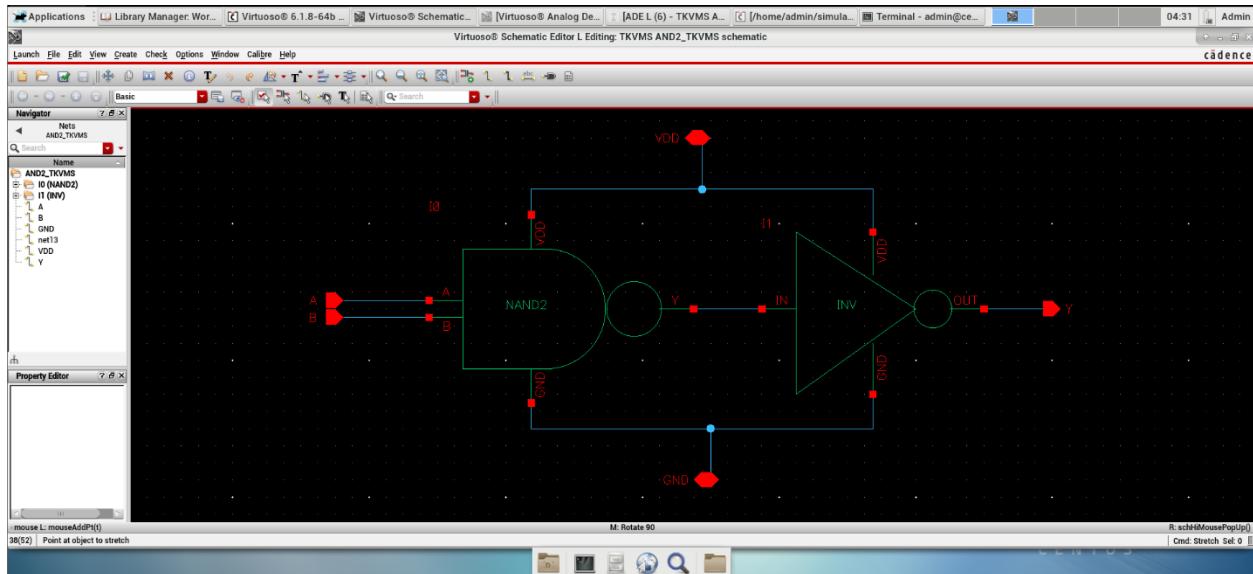
### 2.1. AND2:

a. Schematic:

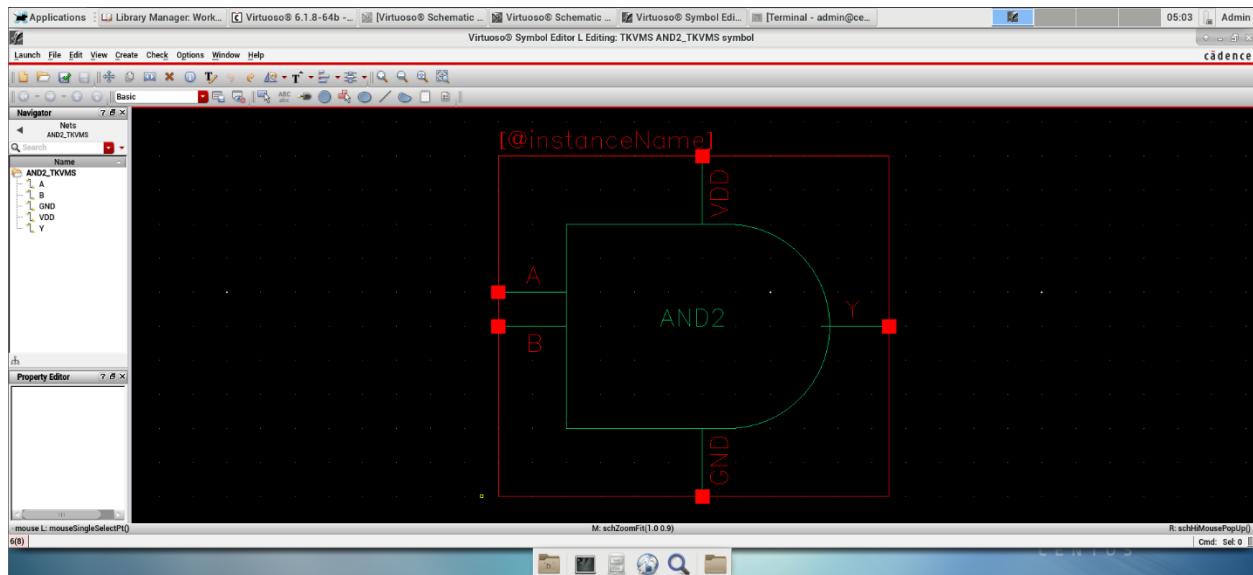
- Truth table:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

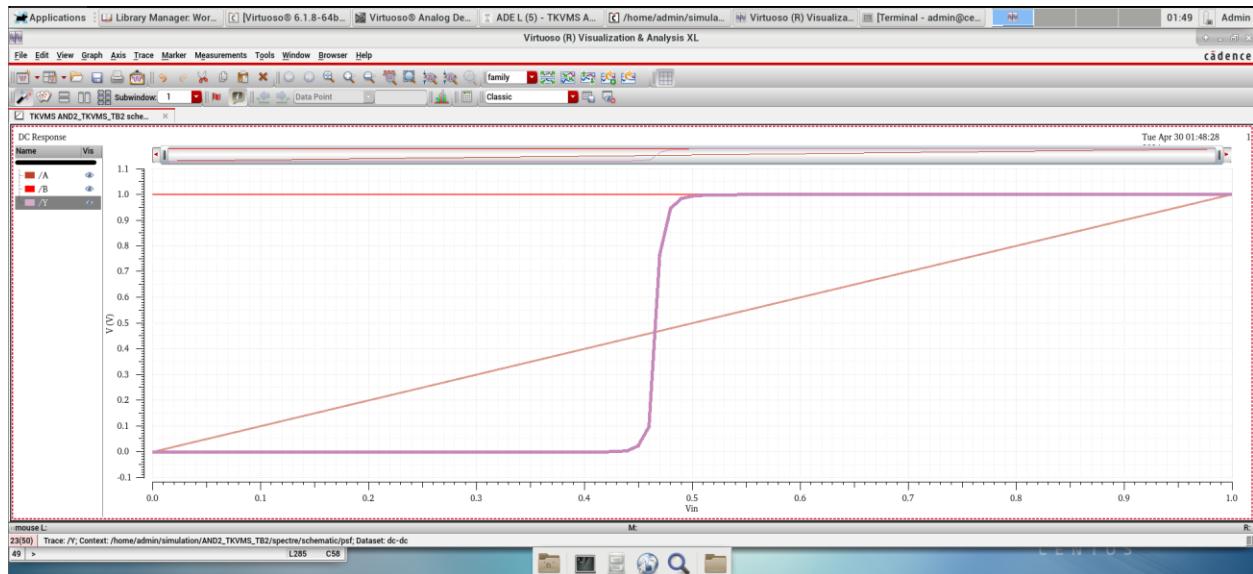
- Schematic:

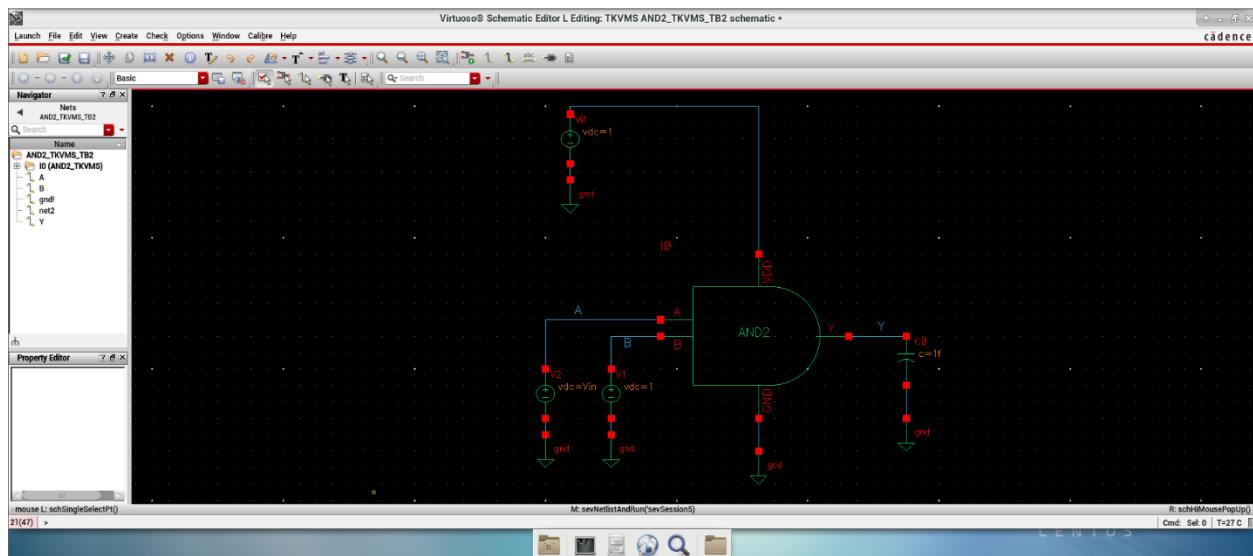


- Symbol:



### b. DC Analysis simulation:

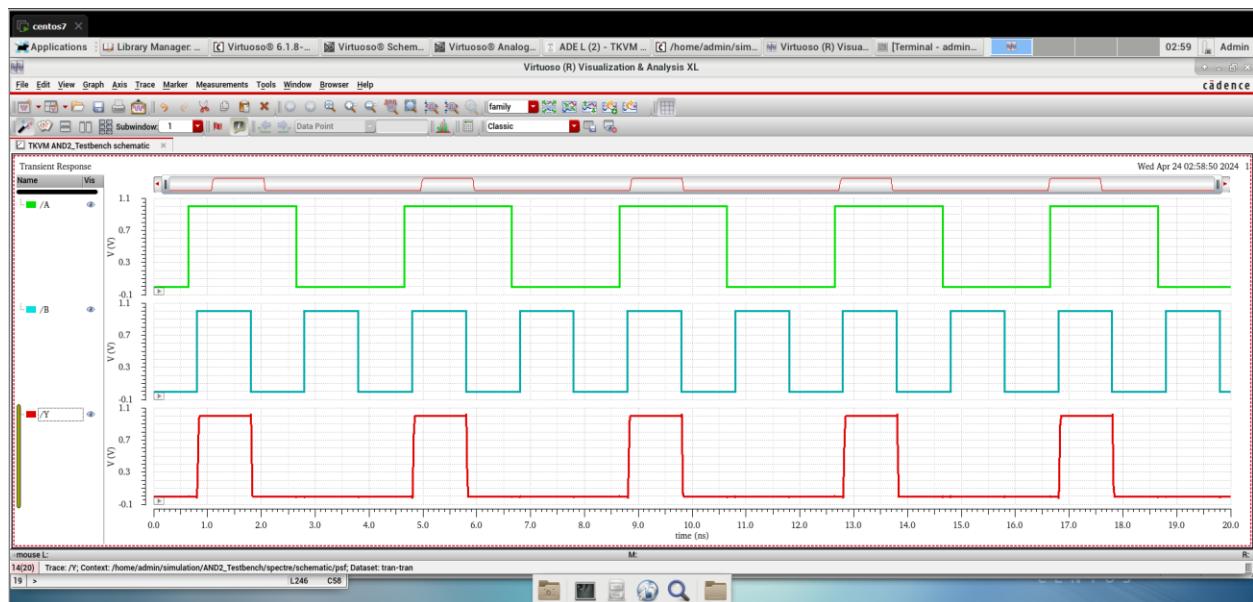


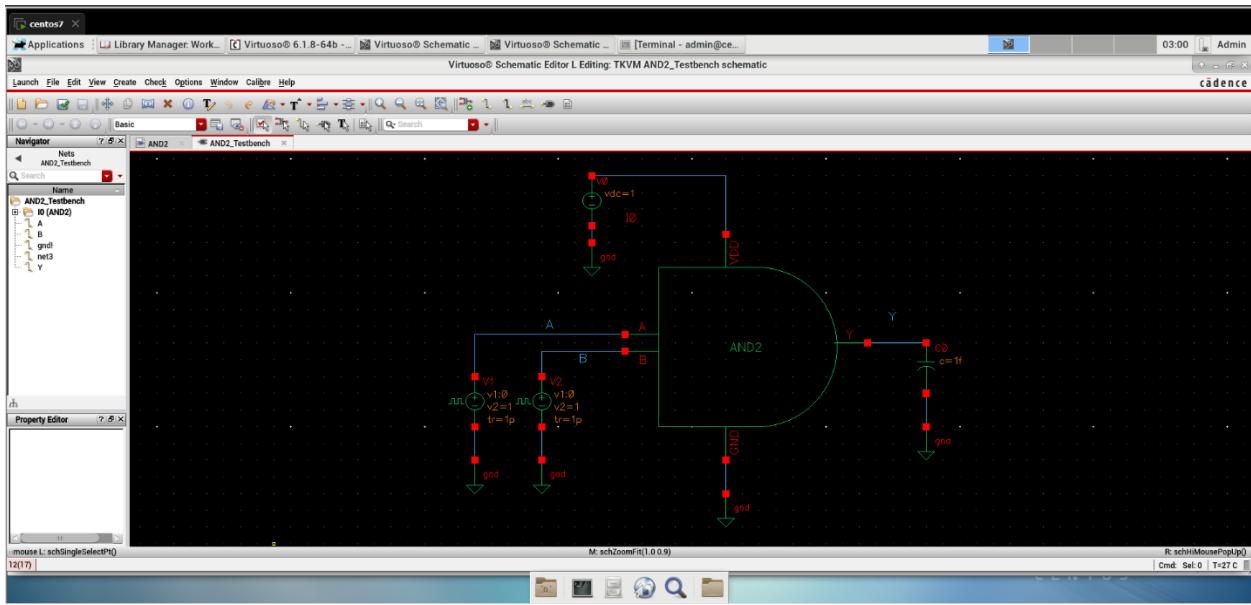


c. Transient simulation:

- Testbench circuit for AND2:

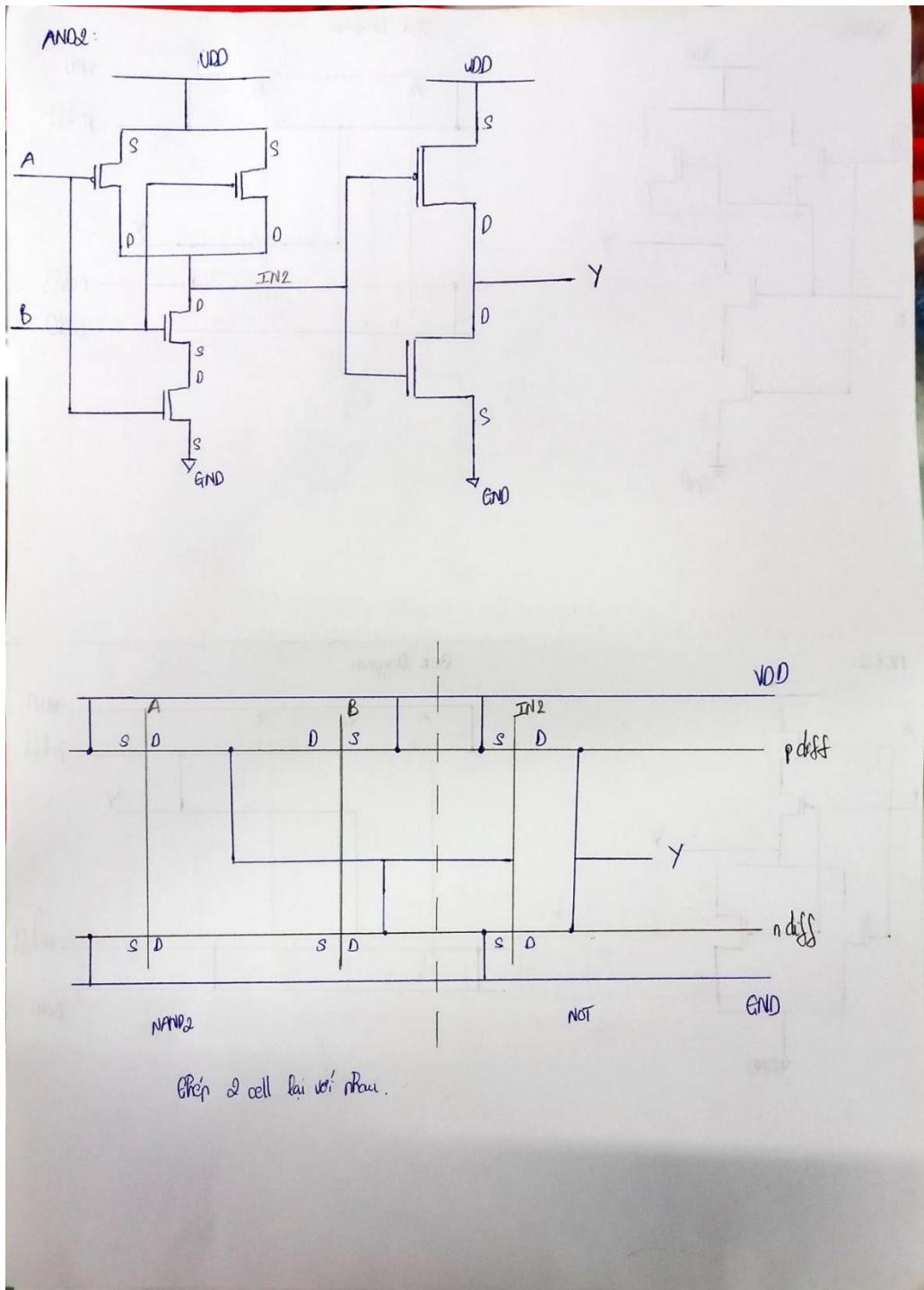
	InA	InB
Voltage 1	0	0
Voltage 2	1	1
Period	4n	2n
Delay time	0.65n	0.8n
Rise time	1p	1p
Fall time	1p	1p
Pulse width	2n	1n



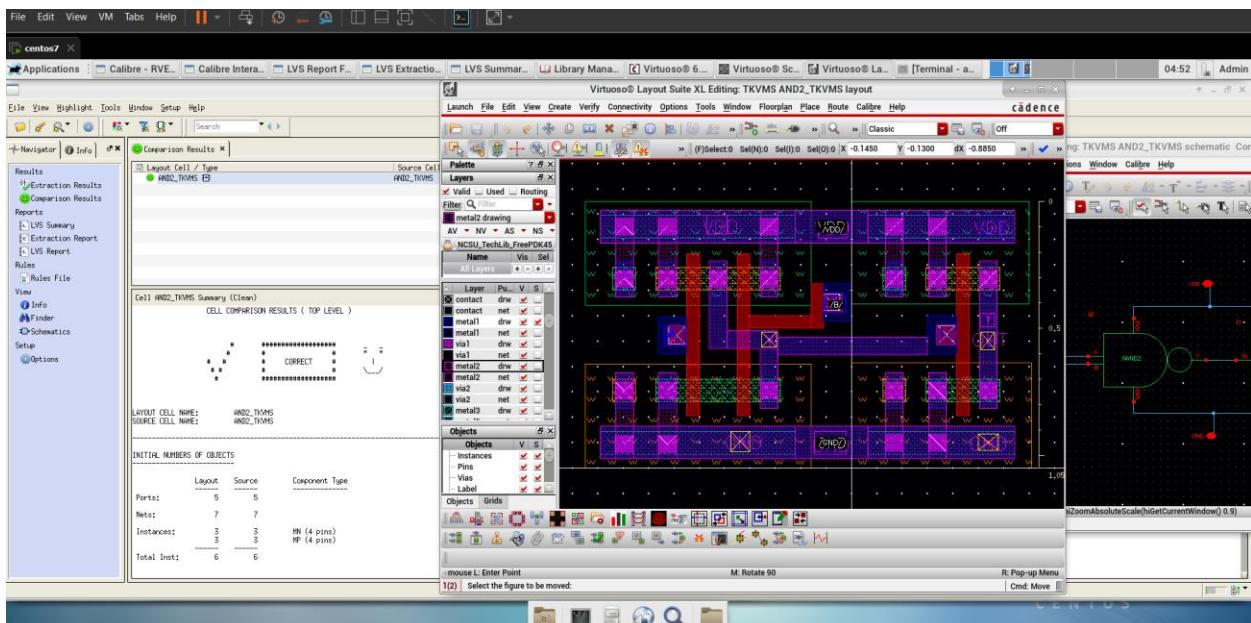
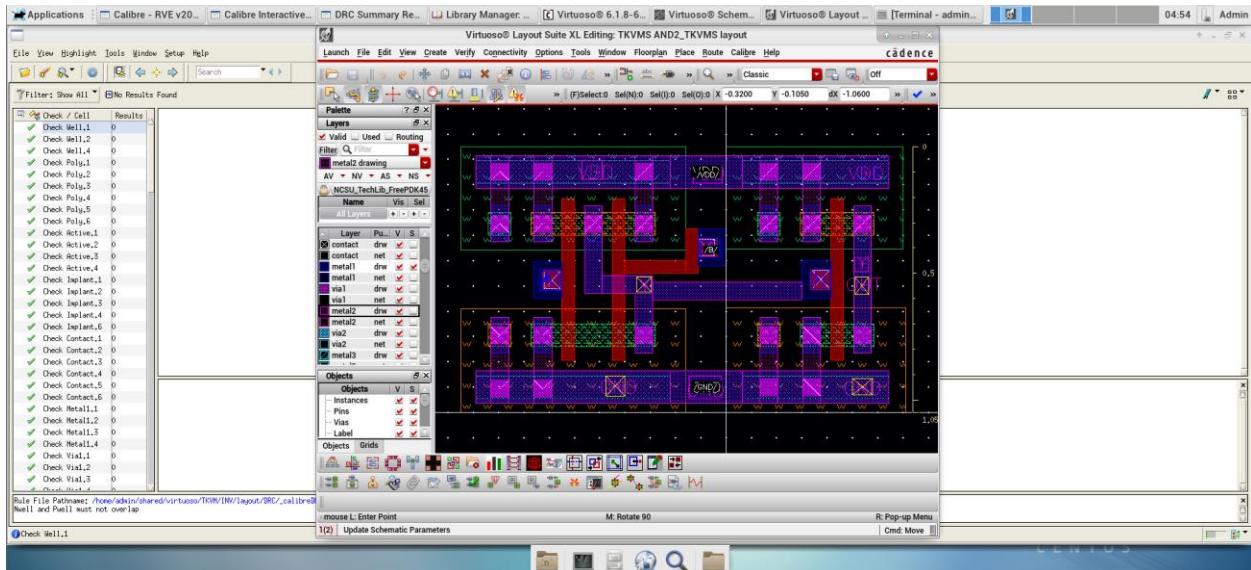


#### d. Layout:

- Stick diagram:



- Layout, check DRC, check LVS:



- Cell có độ cao 1.05um đúng như yêu cầu.

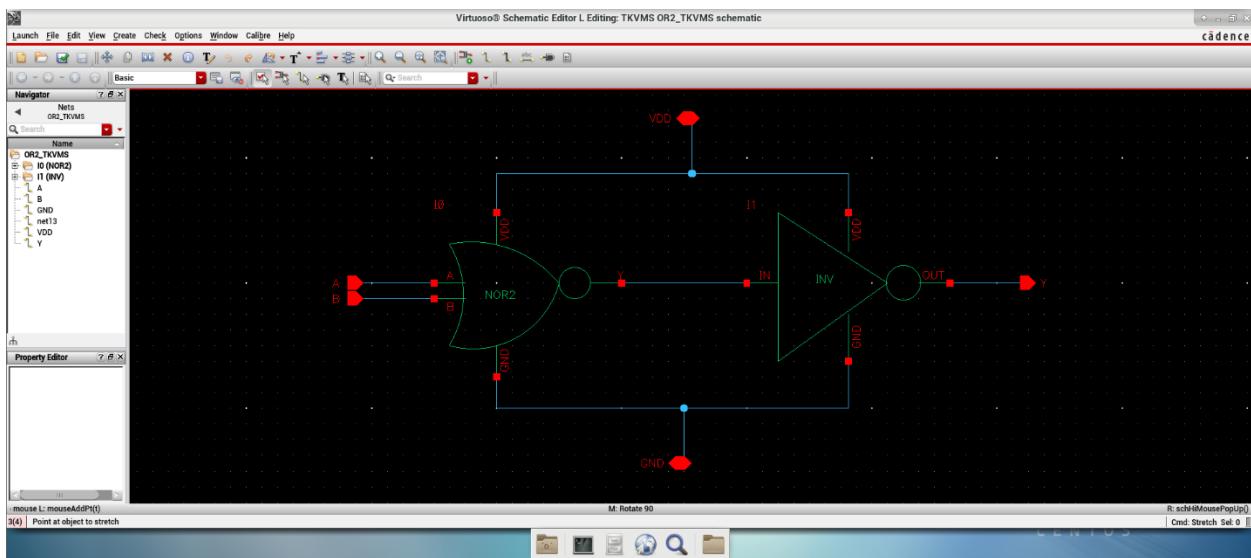
## 2.2. OR2:

### a. Schematic:

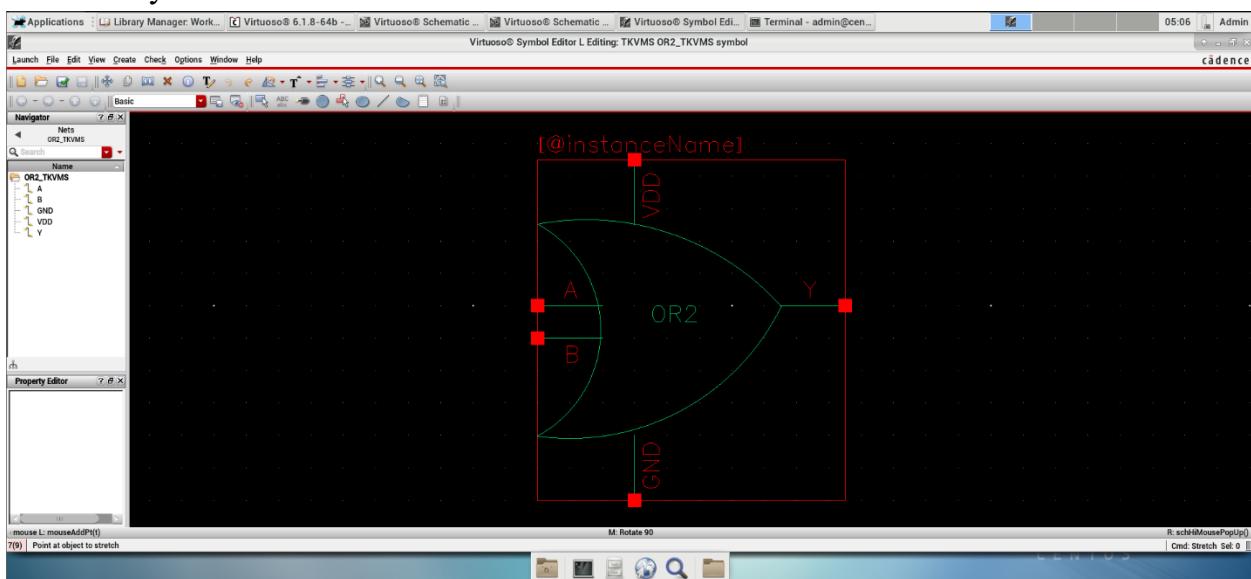
- Truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

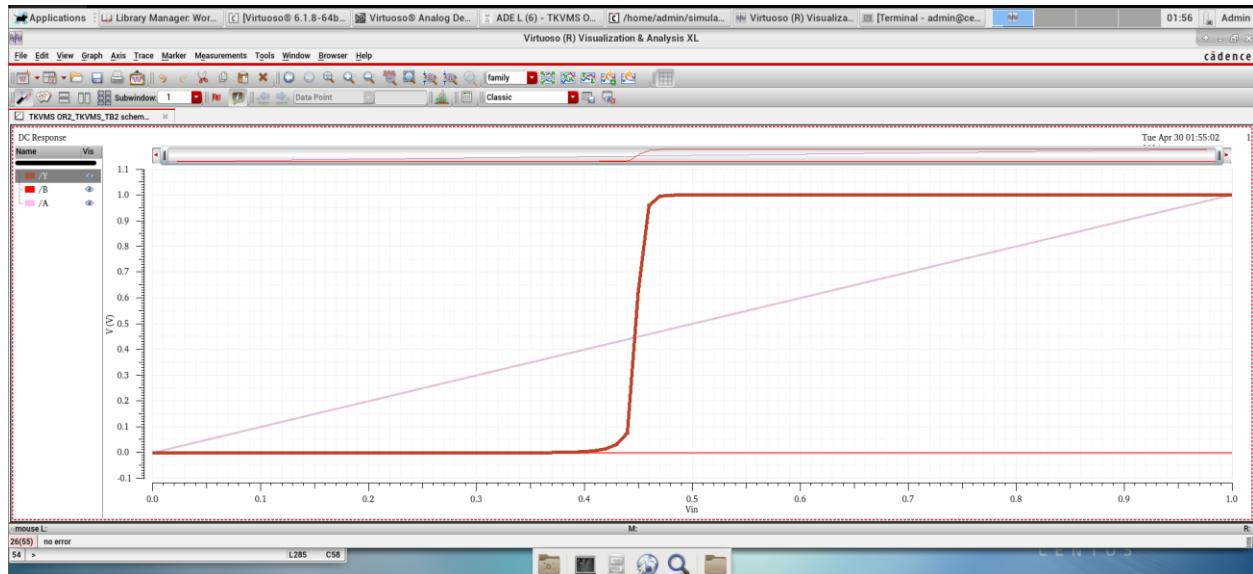
- Schematic:



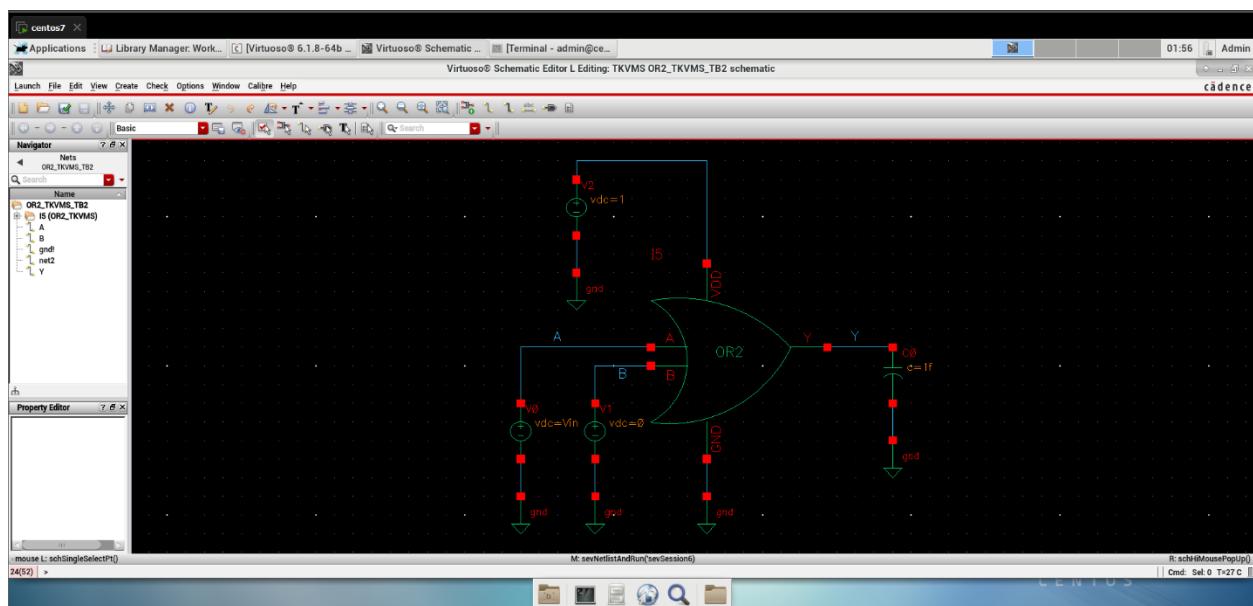
- Symbol:



### b. DC Analysis simulation:

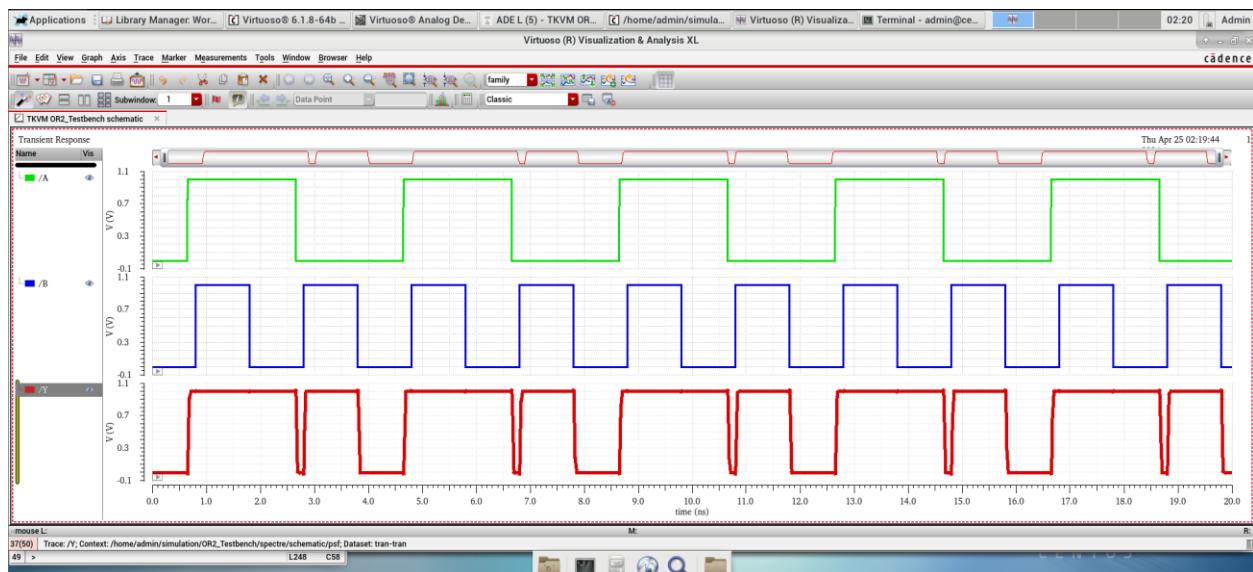
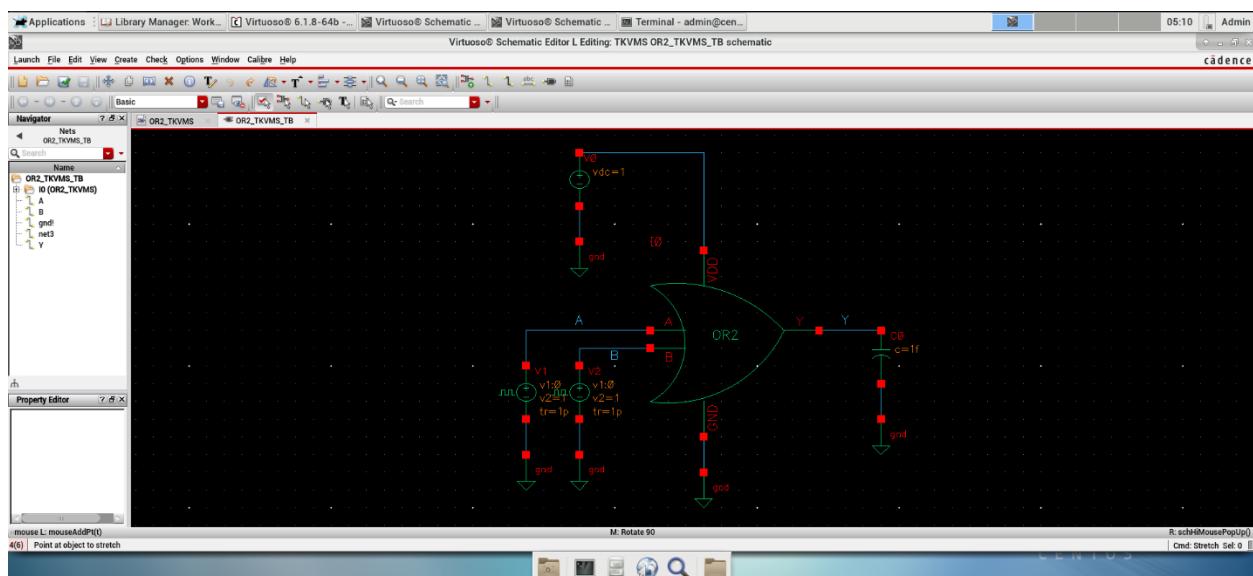


### c. Transient simulation:



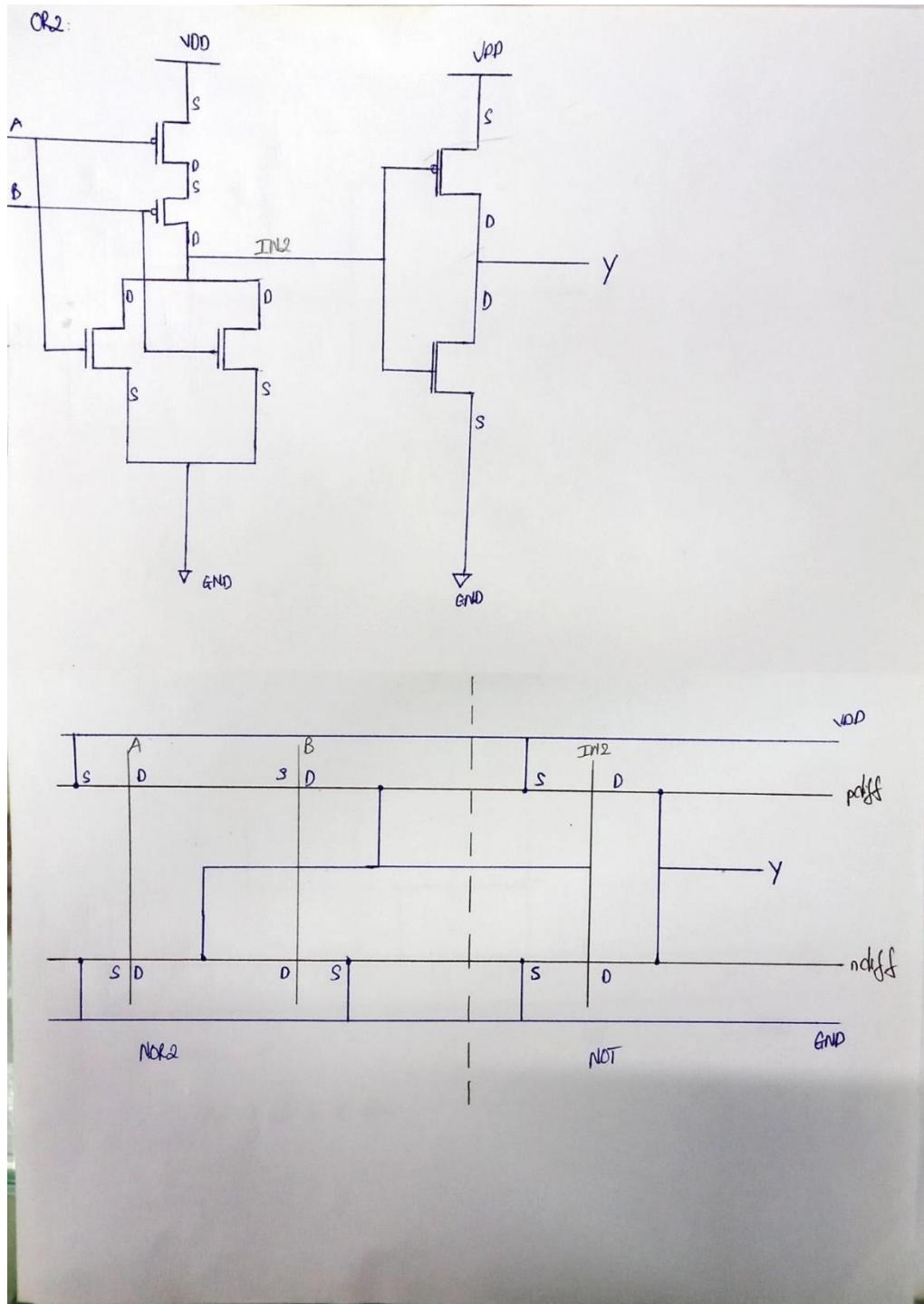
- Testbench circuit for OR2:

	InA	InB
Voltage 1	0	0
Voltage 2	1	1
Period	4n	2n
Delay time	0.65n	0.8n
Rise time	1p	1p
Fall time	1p	1p
Pulse width	2n	1n

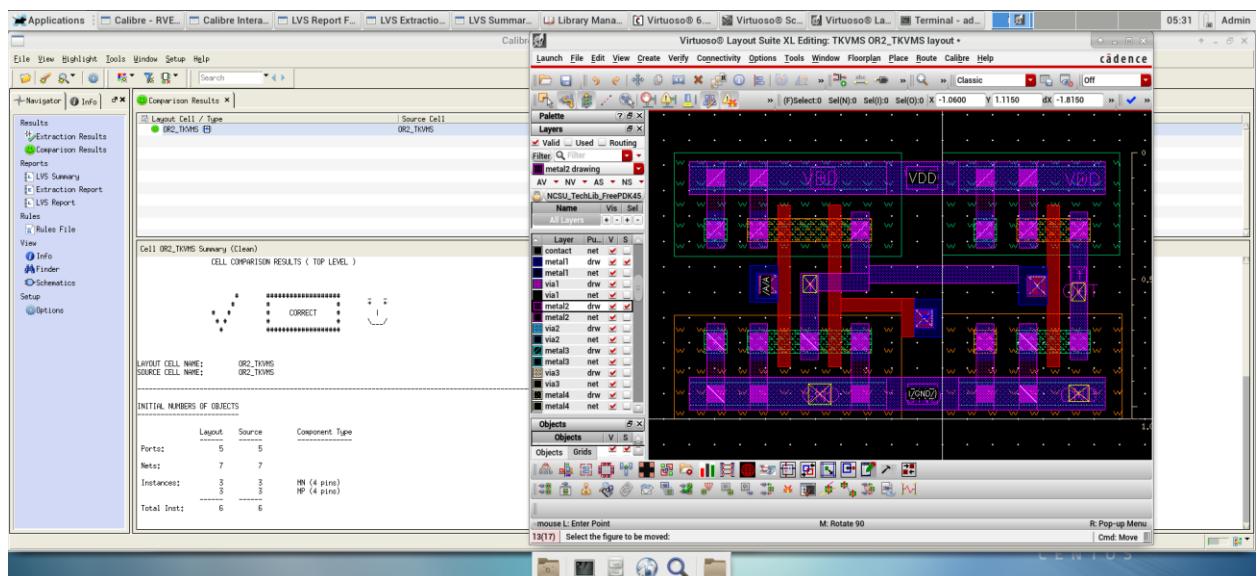
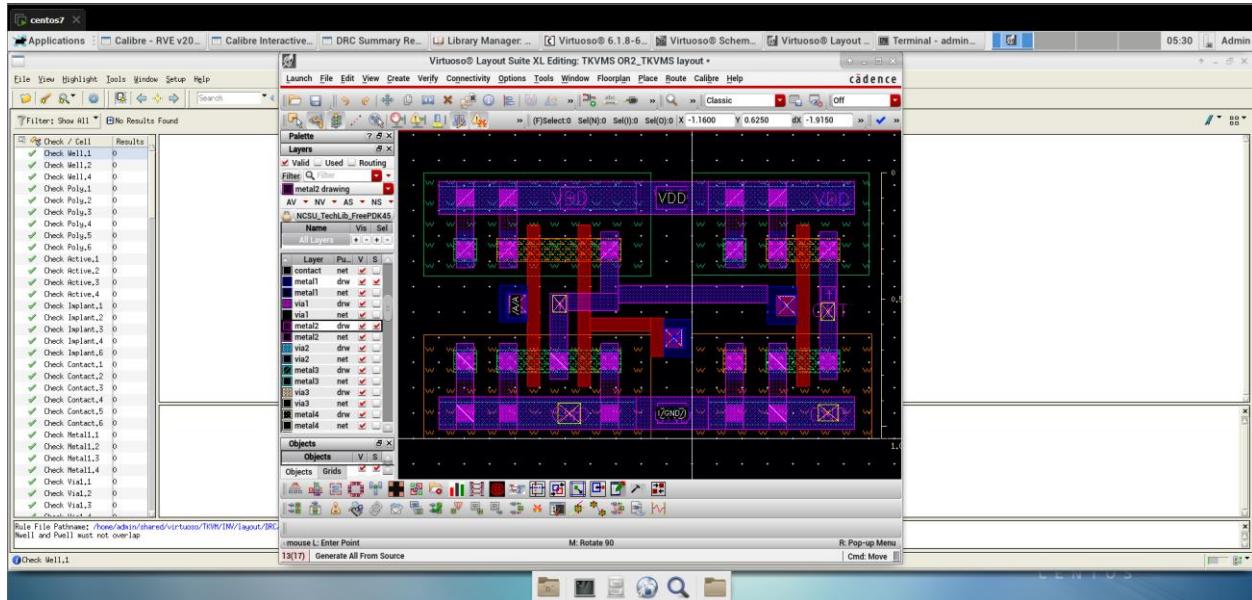


d. Layout:

- Stick diagram:



- Layout, check DRC, check LVS:



- Cell có độ cao 1.05um và check đúng DRC với LVS.