RZ/A2M Group

Camera and Display sample

Introduction

This document describes the sample program that uses the RZ/A2M group MCU to perform video input and display functions.

Target Device

RZ/A2M

Contents

1. Overview

The Camera and Display application (sample program) supports the functions to capture an image from the MIPI camera and display the captured image. Also, the CUI tool to control image correcting functions provided by Video Display Controller (VDC) is included in this package.

Table 1-1 Peripheral devices and Usage

Peripheral devices	Usage
MIPI and VIN	CMOS camera image input by MIPI interface.
VDC	Display system.
RIIC	MIPI camera configurations.
SCIF	Image quality adjustment by CUI using Terminal Application.

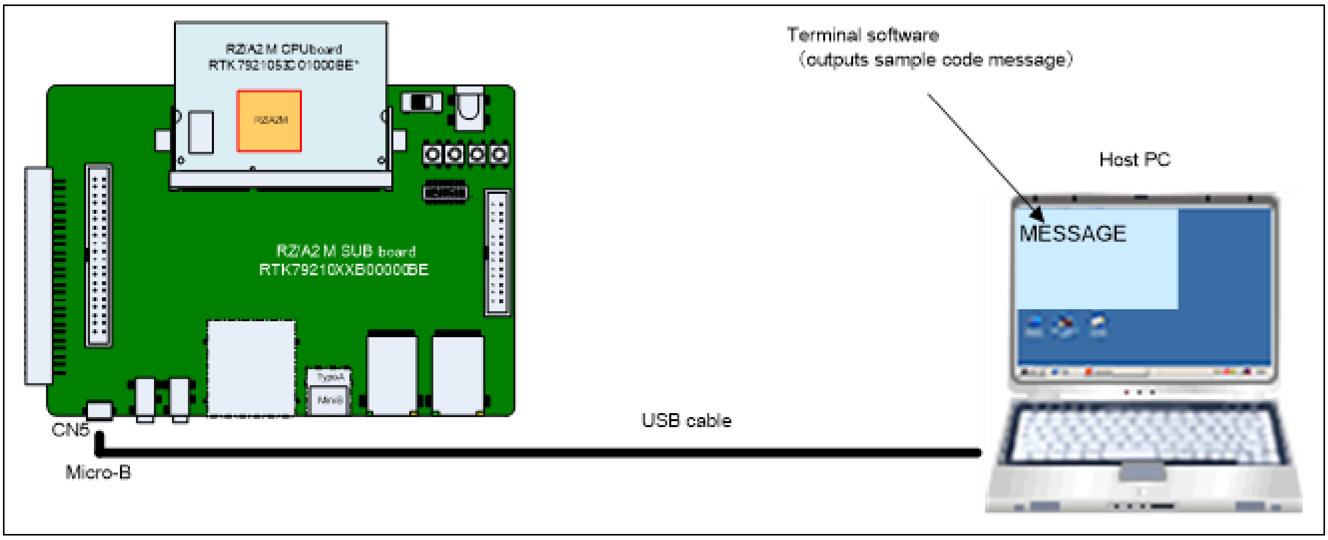


Figure 1-1 Operation check conditions

2. Operation Confirmation Conditions

The sample code of this application has been verified by following conditions.

Table 2-1 Peripheral device used(1/2)

Peripheral device	Usage
MCU Used	• RZ/A2M
Operating frequency[MHz] (Note)	CPU Clock (Iφ) : 528MHz Image processing clock (Gφ) : 264MHz Internal Bus Clock (Bφ) : 132MHz Peripheral Clock 1 (P1φ) : 66MHz Peripheral Clock 0 (P0φ) : 33MHz QSPI0_SPCLK : 66MHz CKIO : 132MHz
Operating voltage	Power supply voltage (I/O): 3.3 V Power supply voltage (either 1.8V or 3.3V I/O (PVcc SPI)) : 3.3V Power supply voltage (internal): 1.2 V
Integrated development environment	e2 studio V7.4.0
C compiler	“GNU Arm Embedded Tool chain 6-2017-q2-update” compiler options(except directory path) Release: -mcpu=cortex-a9 -march=armv7-a -marm -mlittle-endian -mfloat-abi=hard -mfpu=neon -mno-unaligned-access -Os -ffunction-sections -fdata-sections -Wunused -Wuninitialized -Wall -Wextra -Wmissing-declarations -Wconversion -Wpointer-arith -Wpadded -Wshadow -Wlogical-op -Waggregate-return -Wfloat-equal -Wnull-dereference -Wmaybe-uninitialized -Wstack-usage=100 -fabi-version=0 Hardware Debug: -mcpu=cortex-a9 -march=armv7-a -marm -mlittle-endian -mfloat-abi=hard -mfpu=neon -mno-unaligned-access -Og -ffunction-sections -fdata-sections -Wunused -Wuninitialized -Wall -Wextra -Wmissing-declarations -Wconversion -Wpointer-arith -Wpadded -Wshadow -Wlogical-op -Waggregate-return -Wfloat-equal -Wnull-dereference -Wmaybe-uninitialized -g3 -Wstack-usage=100 -fabi-version=0

Note: The operating frequency used in clock mode 1 (Clock input of 24MHz from EXTAL pin)

Table 2-2 Peripheral device used(2/2)

Operation mode	Boot mode 3 (Serial Flash boot 3.3V)
Terminal software communication settings	Communication speed: 115200bps Data length: 8 bits Parity: None Stop bits: 1 bit Flow control: None
Board to be used	RZ/A2M CPU board RTK7921053C00000BE RZ/A2M SUB board RTK79210XXB00000BE
Device (functionality to be used on the board)	Serial flash memory allocated to SPI multi-I/O bus space (channel 0) Manufacturer : Macronix Inc. Model Name : MX25L51245GXD RL78/G1C (This device communications the host PC by convert USB Communication and Serial Communication.)

Note: The operating frequency used in clock mode 1 (Clock input of 24MHz from EXTAL pin)

3. Reference Application Notes

The application note related to this sample program is shown below.

- RZ/A2M Group Video utility (R01AN4476)
  This document describes function specifications of APIs to control display and video input.

4. Software Description

Figure 4-1 shows the system block diagram of sample program. There are 2 tasks in this program. One is to control camera input and display output, and another one is for the CUI (Character User Interface) to control image correction functions. For details of the CUI task, refer to Section 7 Image Adjustment.

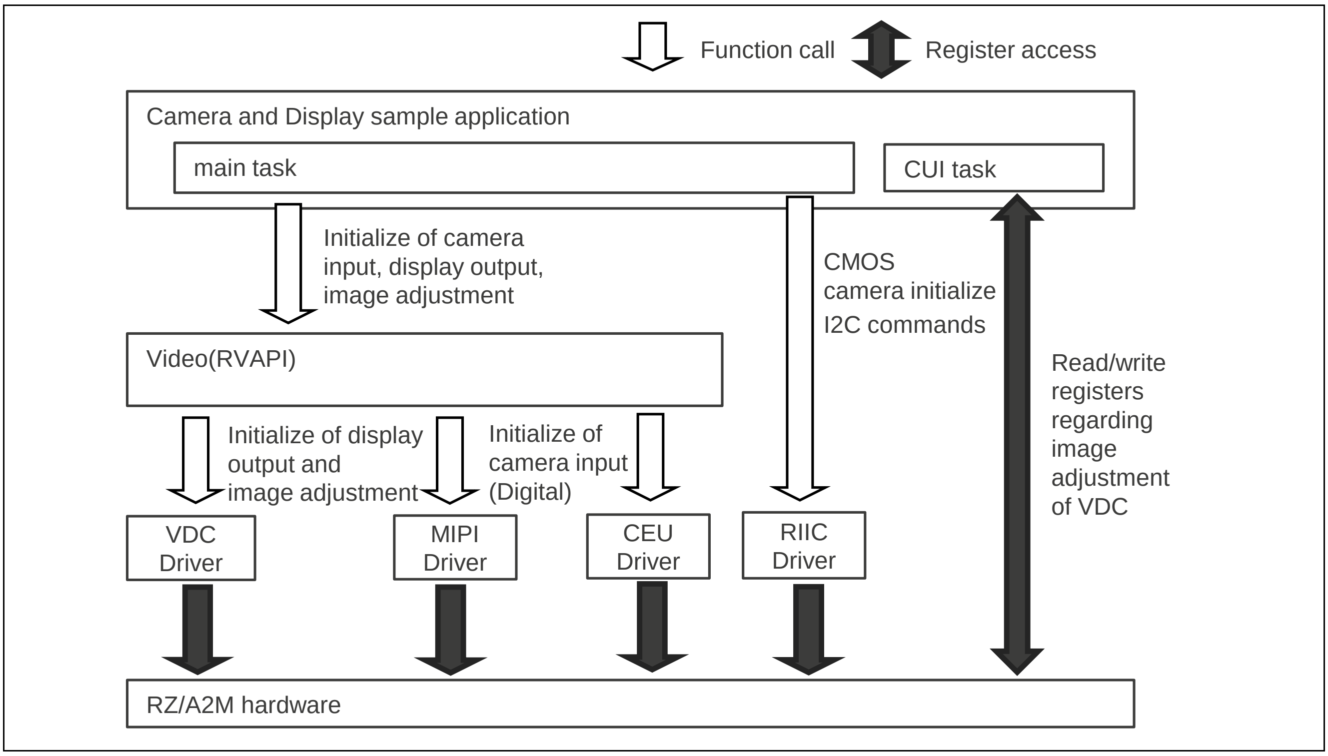


Figure 4-1 Sample program System Block Diagram

5. Display output

To use the display output feature, this sample program must be changed by user to fit actual user's display equipment. This section explains which parts in source code need to be modified and how to change them.

5.1 Configuration for panel clocks

This sample program supports following display equipment, and there are switched by "lcd_panel.h" file. To configurate the panel clocks, sample setting files for each display device are prepared, and user can use them as reference.

- LVDS display (LT070T81A0-FDR) : lcd_lvds_clk.h
- RSK TFT App board (YR0K77210C000BE) : lcd_rsk_clk.h
- Display output board (included in evaluation board)(Control IC:TFP410 TI Panel Bus™ Digital Transmitter) : lcd_dvi_clk.h

In this sample program, The Display Output Board is selected as the default setting and assumes use of PC monitor display. As those resolution setting, FWXGA (1360x768) and SVGA (800x 600) are supported. Required panel clock specifications from VESA are shown in Table 5-1.

Table 5-1 Summary of Display Monitor Timings – Standards and Guidelines

Pixel size	Refresh Rate	Panel clock	Standard Type
FWXGA (1360x768)	60 Hz	85.500 MHz	VESA Standard
SVGA (800x 600)	60 Hz	40.000 MHz(注)	VESA Guidelines

Note: LCD0_EXTCLK is connected to 40MHz clock.

Configurations to generate this panel clock are shown in Table 5-2 and Table 5-3. For more details, refer to Hardware manual documents described in Section 10 Reference Documents.

Table 5-2 Example for panel clock configurations

Definition	33.0[MHz]	22.0[MHz]
LCD_CH0_PANEL_CLK	VDC_LVDS_INCLK_SEL_PERI peripheral clock1 (P1φ) 66.0[MHz]	
LCD_CH0_PANEL_CLK_DIV	VDC_PANEL_CLKDIV_1_2	VDC_PANEL_CLKDIV_1_3
LVDS_PLL_INPUT_CLK	Not use	Not use
LVDS_PLL_NIDV	Not use	Not use
LVDS_PLL_NODIV	Not use	Not use
LVDS_PLL_NFD	Not use	Not use
LVDS_PLL_NRD	Not use	Not use
LVDS_PLL_NOD	Not use	Not use

【Note】Peripheral clock1 (P1 ϕ) is assumed as 66.0MHz.

Table 5-3 Example for panel clock to use LVDS PLL

Definition	74.25[MHz]	85.25[MHz]
LCD_CH0_PANEL_CLK	VDC_PANEL_ICKSEL_LVDS	VDC_PANEL_ICKSEL_LVDS
LCD_CH0_PANEL_CLK_DIV	VDC_PANEL_CLKDIV_1_1	VDC_PANEL_CLKDIV_1_1
LVDS_PLL_INPUT_CLK	VDC_LVDS_INCLK_SEL_PERI	VDC_LVDS_INCLK_SEL_PERI
LVDS_PLL_NIDV	Not use	Not use
LVDS_PLL_NODIV	VDC_LVDS_NDIV_4	VDC_LVDS_NDIV_4
LVDS_PLL_NFD	(27u-1u)	(31u-1u)
LVDS_PLL_NRD	(6u-1u)	(6u-1u)
LVDS_PLL_NOD	Not use	Not use

【Note】Peripheral clock1 (P1 ϕ) is assumed as 66.0MHz.

5.2 Timing control for display equipment

As for timing control setting for display equipment, the program must be modified to fit each equipment. Configuration files for each environment are prepared and user can use them as reference as well as Section 5.1.

- LVDS display (LT070T81A0-FDR) : lcd_lvds_ch0.h
- RSK TFT App board (YR0K77210C000BE) : lcd_rsk_ch0.h
- Display output board (included in evaluation board)(Control IC：TFP410 TI Panel Bus™ Digital Transmitter) : lcd_dvi_ch0.h

RSK TFT APP Board(YROK77210C000BE) Horizontal/Vertical input timing diagrams are shown as Figure 5-1 and Figure 5-2, and Horizontal/Vertical sync signal timing specifications are shown in

Table 5-4 and Table 5-5. Control timing can be set according to these specifications.

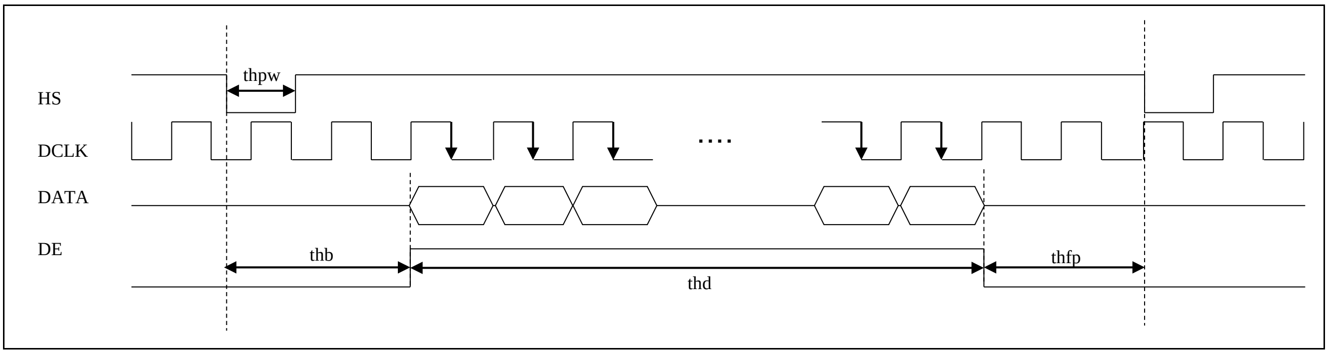


Figure 5-1 Horizontal input timing diagram

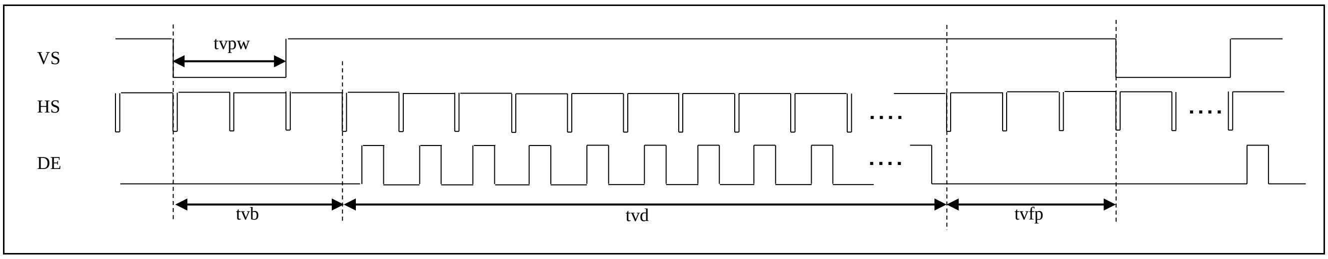


Figure 5-2 Vertical input timing diagram

Table 5-4 Horizontal input timing

Item	Symbol	Value Min.	Typ.	Max.	Unit
Horizontal display area	thd	-	800	-	DCLK
DCLK Frequency	fclk	26.4	33.3	46.8	MHz
One Horizontal Line	th	852	1056	1200	DCLK
HS pulse width	thpw	1	20	40	DCLK
HS Blanking	thb	46	46	46	DCLK
HS Front Porch	thpf	16	210	354	DCLK

Table 5-5 Vertical input timing

Item	Symbol	Value Min.	Typ.	Max.	Unit
Vertical display area	tvd	-	480	-	TH
VS period time	tv	510	525	650	TH
VS pulse width	tvpw	1	10	20	TH
VS Blanking	tvb	23	23	23	TH
VS Front Porch	tvpf	7	22	147	TH

According to the relationship between control timing and definitions (Figure 5-3), example of timing control configuration is shown in Table 5-6.

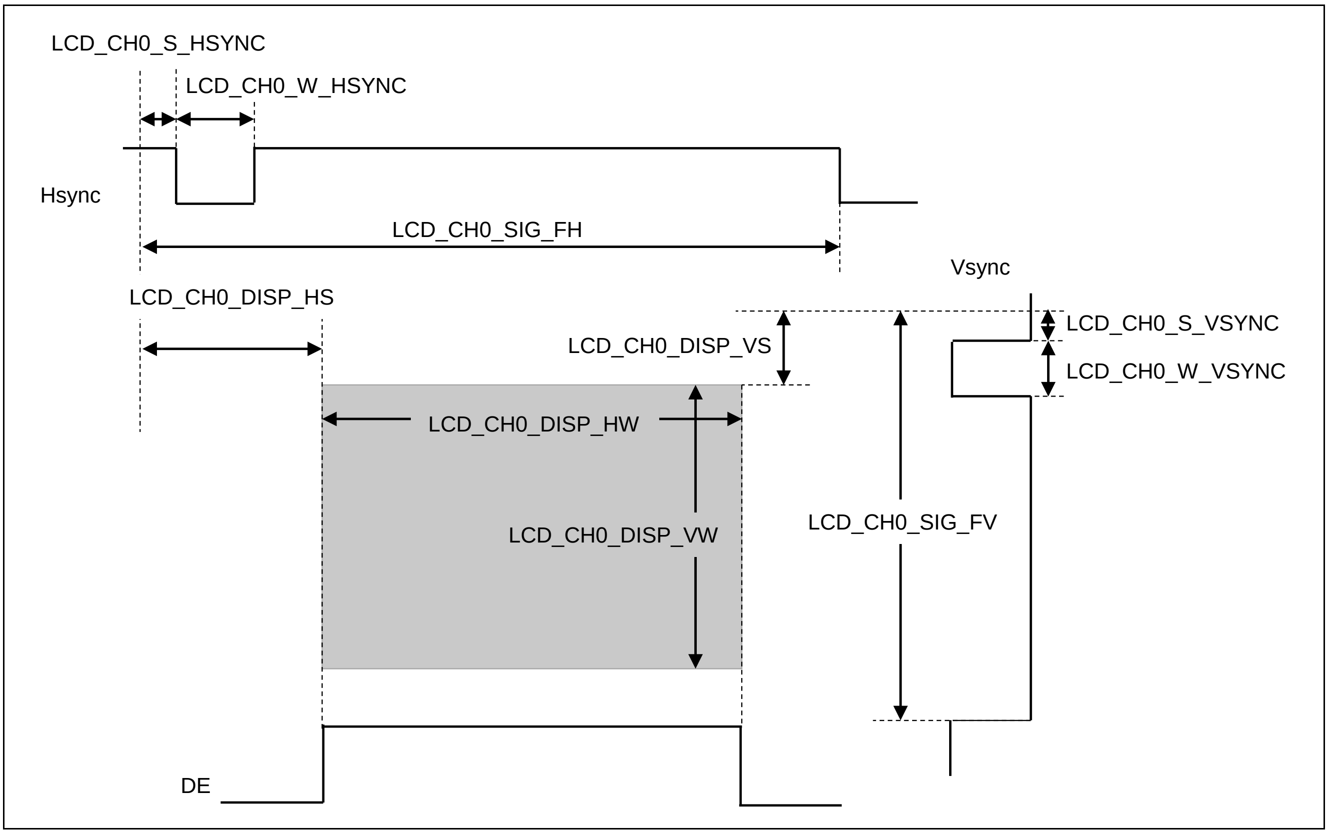


Figure 5-3 Timing configuration and definition

Table 5-6 Example of Timing Control Configuration

Definition	Setting Value	Remark
LCD_CH0_S_VSYNC	0u	-
LCD_CH0_W_VSYNC	10u	Refer to VS pulse width (Table 5-5)
LCD_CH0_DISP_VS	10u+13u	Refer to VS Blanking (Table 5-5)
LCD_CH0_DISP_VW	480u	Refer to Vertical display area (Table 5-5)
LCD_CH0_S_HSYNC	0u	-
LCD_CH0_W_HSYNC	20u	Refer to HS pulse width (Table 5-4)
LCD_CH0_DISP_HS	20u + 26u	Refer to HS Blanking (Table 5-4)
LCD_CH0_DISP_HW	800u	Refer to Horizontal display area (Table 5-4)
LCD_CH0_SIG_FV	525u - 1u	Refer to VS period time (Table 5-5)
LCD_CH0_SIG_FH	1056u - 1u	Refer to One Horizontal Line (Table 5-4)

Note: This setting is for RZ/A2M evaluation board connected to RSK TFT App board.

5.3 Output configuration of control signals

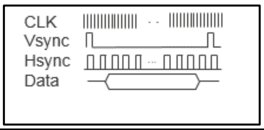
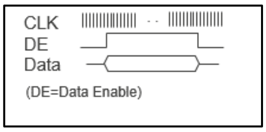
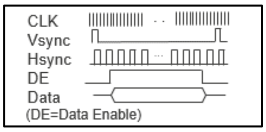
Main control signals to connect output display devices are shown in Table 5-7.

Table 5-7 Main Control Signals

Name	Function Summary
Horizontal sync signal (Hsync)	Signal that creates timing for displaying one line
Vertical sync signal (Vsync)	Signal that creates timing for displaying one screen
Panel clock (CLK)	Signal that use to sample for displaying one pixel.
Display enable (DE)	Signal indicating that valid data is being output
Data (Data)	Display data

This sample program supports 3 display types as Table 5-8 by combinations of the control signals.

Table 5-8 Control Signals Used

Name	Display Type 1 	Display Type 2 	Display Type 3 
Horizontal sync signal (Hsync)	Used	Not used	Used
Vertical sync signal (Vsync)	Used	Not used	Used
Panel clock (CLK)	Used	Used	Used
Display enable (DE)	Not used	Used	Used
Data (Data)	Used	Used	Used

According to Figure 5-1 and Figure 5-2, RSK TFT APP Board(YROK77210C000BE) requires horizontal sync signal (Hsync), vertical sync signal (Vsync), and display enable signal (DE).

User needs to set that which control signals are output as TCON pin with used board specification document. Example of combinations of control signals and TCON pin are shown in Table 5-9. In addition, set polarity of control pins as well in comply with Figure 5-1 and Figure 5-2.

Table 5-9 Example of combinations of control signals and TCON pin

Definition	Setting Value	Remark
LCD_CH0_TCON_PIN_VSYNC	VDC_LCD_TCON_PIN_0	
LCD_CH0_TCON_PIN_HSYNC	VDC_LCD_TCON_PIN_3	
LCD_CH0_TCON_PIN_DE	VDC_LCD_TCON_PIN_4	
LCD_CH0_TOCN_POL_VSYNC	VDC_SIG_POL_INVERTED	Polarity inverted. Refer to Figure 5-1,Figure 5-2
LCD_CH0_TOCN_POL_HSYNC	VDC_SIG_POL_INVERTED	Polarity inverted. Refer to Figure 5-1,Figure 5-2
LCD_CH0_TOCN_POL_DE	VDC_SIG_POL_NOT_INVERTED	Polarity not inverted. Refer to Figure 5-1,Figure 5-2

Note: This setting is for RZ/A2M evaluation board connected to RSK TFT App board.

5.4 Output timing configurations for data signals

VDC output data timing is depending on the data latch timing on display device. If display device latch the data on fall-edge, VDC has to output data on rise-edge (must be opposite edge) timing. In this sample program, according to Figure 5-1, display device latch the data on fall-edge timing, so VDC edge timing is set as rise-edge (refer to Table 5-10).

Table 5-10 Example of data output timing configuration

Definition	Setting Values	Remark
LCD_CH0_OUT_EDGE	VDC_EDGE_RISING	

Note: This setting is for RZ/A2M evaluation board connected to RSK TFT App board.

5.5 Output format configuration for data signals

User needs to set output format configuration to comply with specifications of output device and connections as Table 5-11.

Table 5-11 Example of data output format

Definition	Setting Value	Remark
LCD_CH0_OUT_FORMAT	VDC_LCD_OUTFORMAT_RGB888	

Note: This setting is for RZ/A2M evaluation board connected to RSK TFT App board.

5.6 Configuration for GPIO

In this sample program, port configurations about display device are set by Smart Configurator (Figure 5.4).

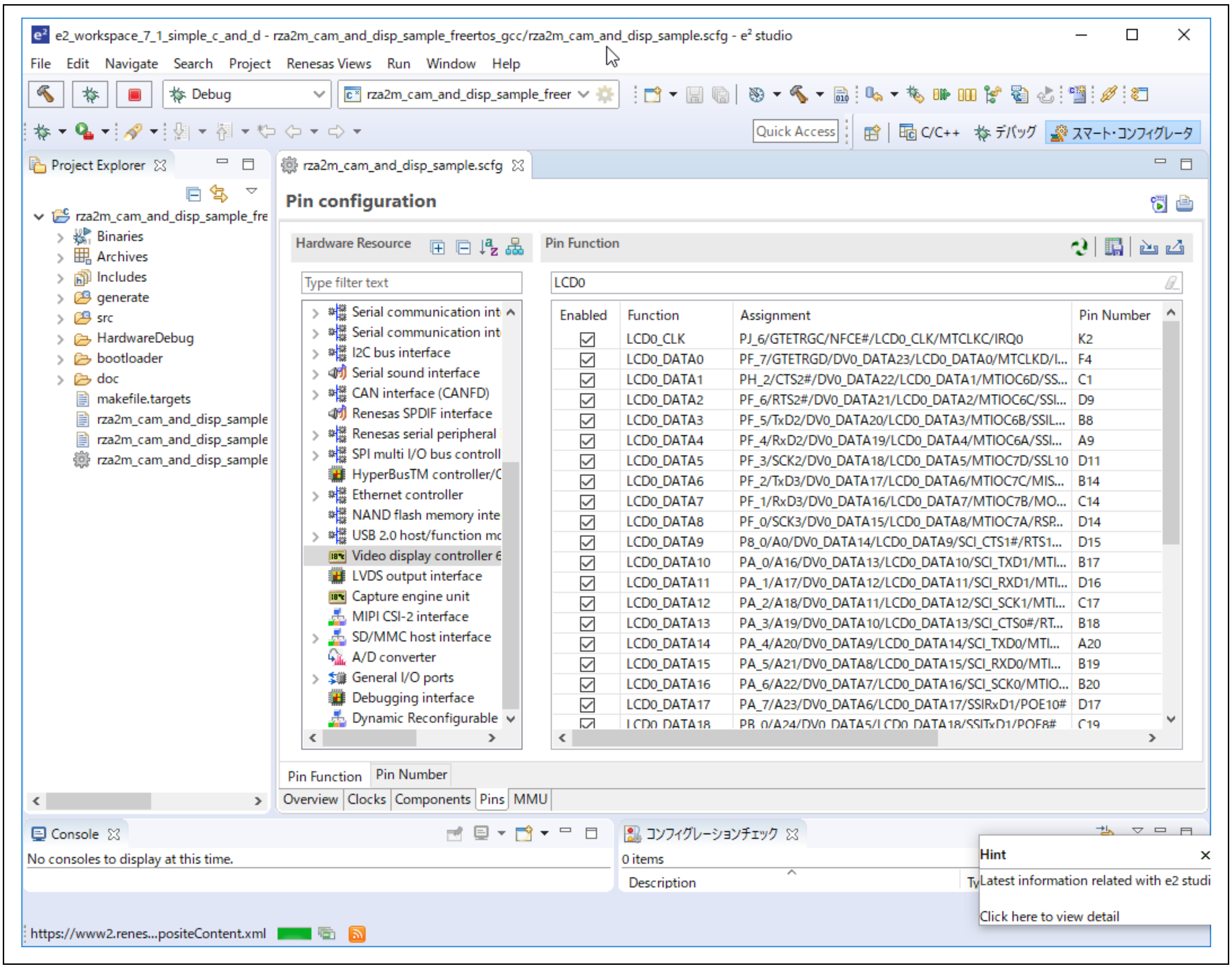


Figure 5-4 Port configuration by Smart Configurator

By changing the “Initialize” column to “By Manual” (Figure5-5), the port setting information in “vdc_portsetting.c” can be activated.

Regarding the configurations for GPIO pins, user needs to modify this file depending on the user's display device.

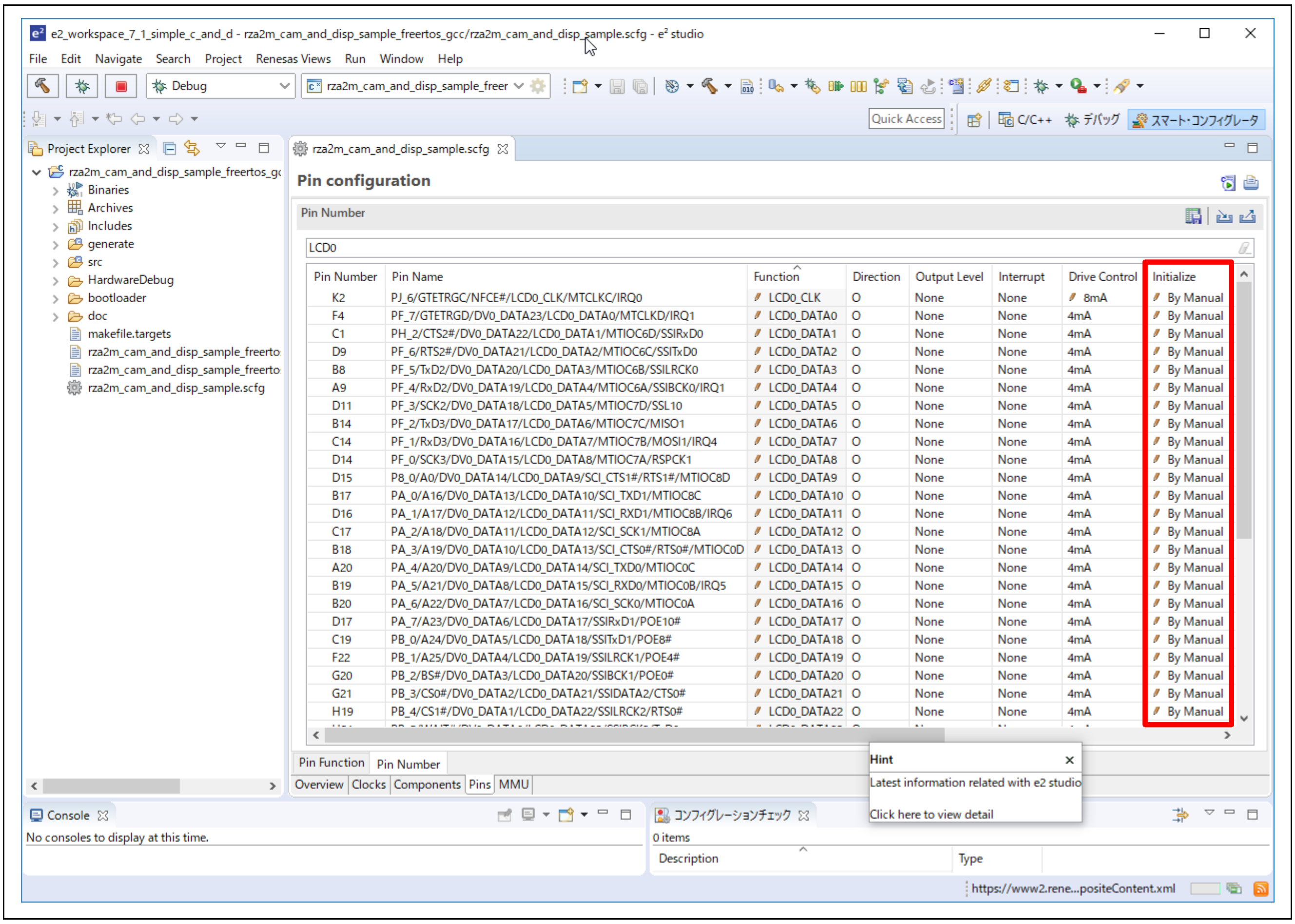
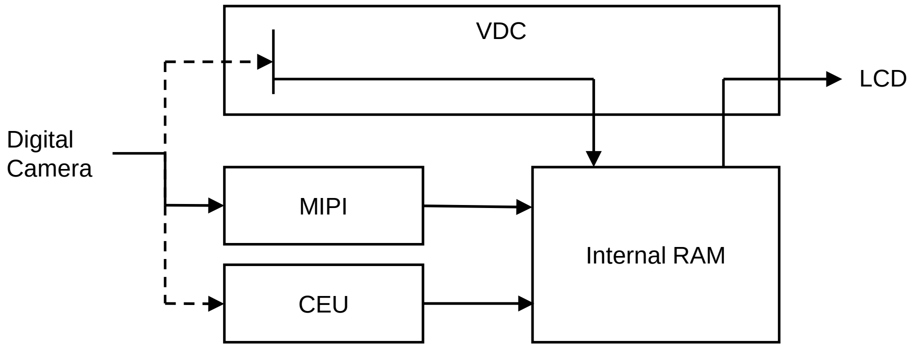


Figure 5-5 Port configuration by Smart Configurator

The display device setting is completed with the above.

6. Camera Input

The three peripherals of RZ/A2M which supports camera input are MIPI, VDC, and CEU (Figure 6-1). This sample program provides sample application which using MIPI as camera input. Please refer hardware manual which is indicated in Section 10 Reference Documents about more detail of each peripherals. Necessary settings in the case of connecting MIPI camera is described in following.



Note 1: RZ/A2M supports 3 camera inputs but this sample program supports only MIPI input.

Figure 6-1 Peripherals of RZ/A2M which supports camera input

6.1 Confirmation of MIPI Specification

The MIPI which is mounted on RZ/A2M is MIPI CSI-2 (Camera Serial Interface 2) Receiver Module. The MIPI of RZ/A2M supports MIPI CSI-2 V1.1 and MIPI D-PHY V2.0. Please choice a camera according the MIPI specification. Also, necessary to confirm about followings.

- MAX transfer rate (1.0Gbps per 1 lane)
- MAX 2048 x 2048 pixels
- 2 lane parallel operating, or 1 lane operating
- Data format
  - YCbCr-422 8bit data
  - YCbCr-422 10bit data
  - RGB-888 data
  - 8bit user defined data(RAW8)

6.2 Timing Settings

This sample program supports following MIPI camera and it can switch by "mipi_camera.h" setting. Regarding MIPI camera side settings, this sample program has following setting file for MIPI camera. If user wants to add own camera setting, please refer the setting file.

- Raspberry Pi Camera V2 : camera_imx219_b.h

PHY timing registers should be set according to CSI2 transfer rate. Please set definition that indicated in

Table 6-1 to the registers according to "Table 47.8 Example of PHY Timing Register Settings Based on Internal Bus Clock (Bφ) Frequency and Data Transfer Rate" of hardware manual of Section 10 Reference Documents.

Table 6-1 PHY timing register setting example by data transfer rate

Definition	Setting Value	Remark
CAM_MIPI_THS_PREPARE	0x00000009u	
CAM_MIPI_THS_SETTLE	0x0000000Eu	
CAM_MIPI_TCLK_PREPARE	0x0000000Au	
CAM_MIPI_TCLK_SETTLE	0x0000000Fu	
CAM_MIPI_TCLK_MISS	0x00000003u	
CAM_MIPI_T_INIT_SLAVE	0x0000338Fu	

Note: These settings are in case of connecting Raspberry Pi Camera V2 and RZ/A2M evaluation board

6.3 Setting of Capture Area

Please set capture area according to settings of camera side (Table 6-2). The relation with setting parameters is indicated in Figure 6-2.

Table 6-2 Pre-clipping setting example

Definition	Setting Value	Remark
CAM_VIN_PRECLIP_START_X	100u	vin_preclip_startx
CAM_VIN_PRECLIP_ WIDTH _X	640u	vin_preclip_endx
CAM_VIN_PRECLIP_START_Y	24u	vin_preclip_starty
CAM_VIN_PRECLIP_ WIDTH _Y	480u	vin_preclip_endy

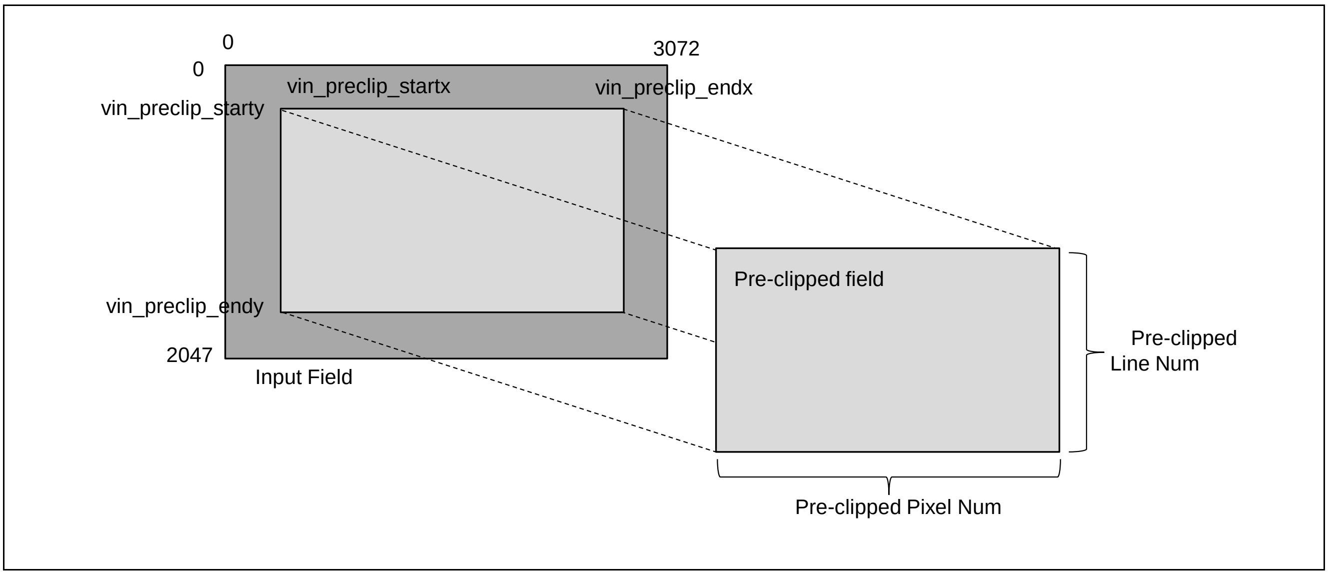


Figure 6-2 Image of pre-clipping area.

6.4 Setting of Camera Side

There is necessary to set MIPI camera side. Please set according to using MIPI camera specification.

7. Image Adjustment

By using the RZ/A2M's peripheral device VDC, this sample program adjusts an image from the camera as shown in Table 7-1. The adjustment results are reflected in the LCD display. User can confirm the adjustment effects in real time, and change the register values related to each adjustment function directly. So, the user can review or test the adjustment values to see if they suit the user's environment. For details about the image adjustment methods, refer to Section 8 Image Adjustment Effects and Adjustment Methods.

Table 7-1 Image Adjustments Supported by This sample program

Peripheral device	Adjustments	Description
VDC	Brightness (Note 1)	Adjusts brightness by changing the luminance components.
	Contrast (Note 1)	Adjusts contrast by changing the color components.
	Sharpness	Sharpens the outline of an edge by adjusting overshoot and undershoot.
	Gamma adjustment	Makes a gamma adjustment with a preset value (four types of preset gamma adjustments are enabled with preset values).
	Dithering process	Performs dithering with random patterns.
	Rotation and Horizontal Mirroring (Note 2)	Rotate an image 180 degree or flip horizontally.

Note 1. The adjustment timing is limited for camera input through the MIPI and CEU (see Section 7.3).

Note 2. Unusable in the case of camera input with MIPI and CEU.

7.1 CUI (Character User Interface)

This sample program implements CUI task which can perform image adjustment in real time with Terminal Application on PC. The CUI task operates the register value of VDC by command input from PC's Terminal Application to realize image adjustment.

This chapter describes the screen operation method and commands from Terminal Application. For details of various adjustment contents and presets, refer to Section 8 Image Adjustment Effects and Adjustment Methods.

7.1.1 Menu

Display menu of Terminal Application and operation overview shown in Figure 7-1. Please refer to Chapter 7.1.2 regarding detail of any commands in Figure 7-1.

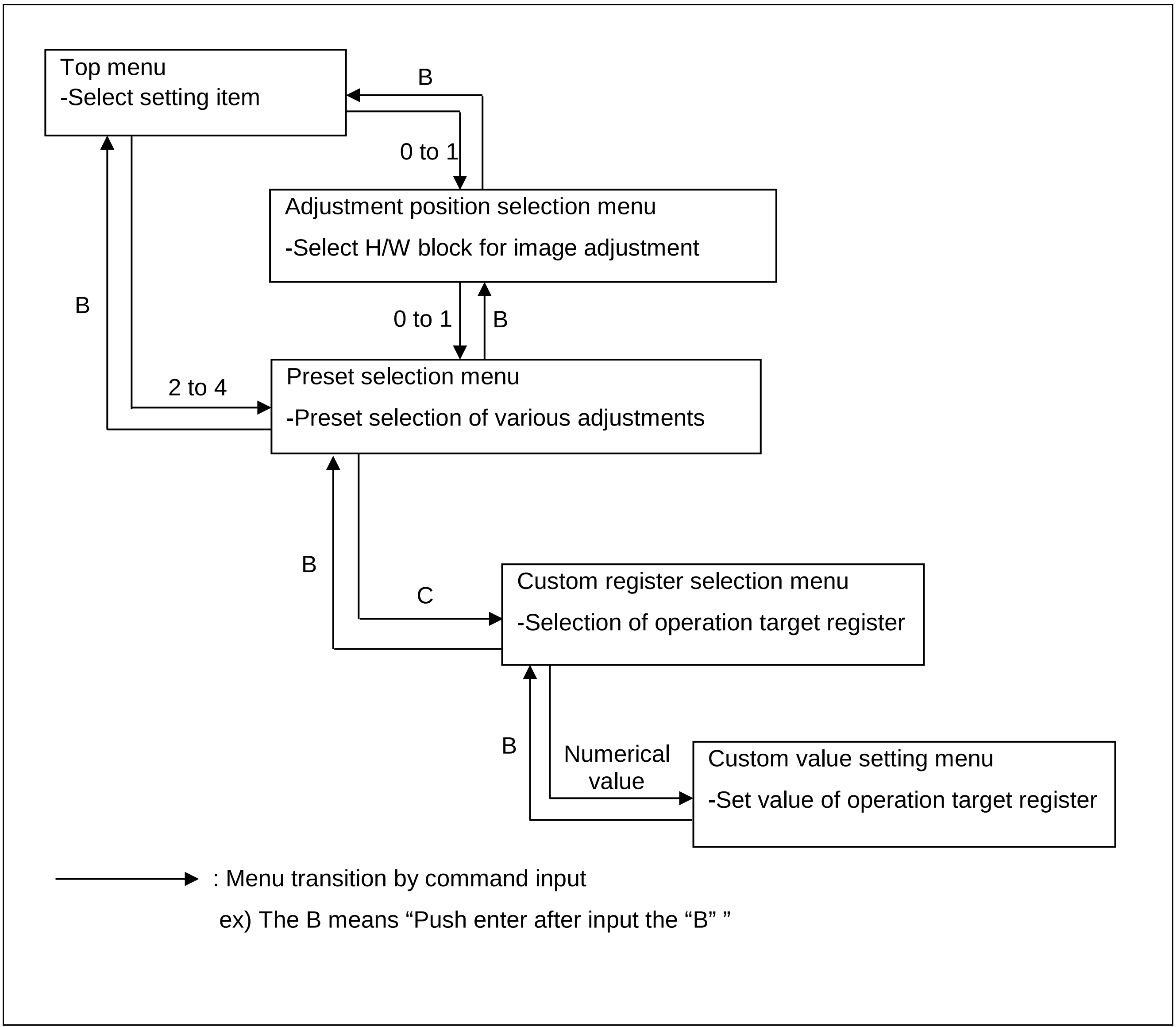


Figure 7-1 Display menu and operation overview.

7.1.2 Commands

Table 7-2 lists the CUI operation commands on the Terminal Application.

Table 7-2 CUI operation command on Terminal Application

Command	Operation
Numerical value	Operations in each menu - Selection of image adjustment content - Selection of image adjustment position (selection of H/W block for image adjustment) - Selection of presets - Input custom value
C, c	Custom setting selection (Selected when user wants to set a preset other than the various adjustment items)
D, d	Set image adjustment to default (Default value of each register described in H/W manual)
B, b	Return to the previous menu
R, r	Output current image adjustment value
T, t	Return to the Top menu
Enter	Determine contents inputted
Delete/ Back space	Delete one character from the input character

7.2 Applying Image Adjustment results

In this sample program, it is easy to apply the image adjustment results as initial setting of program after adjustment. Adjusted parameters will be output to Terminal Application as header format of C source code. For details, refer to Section.7.3.1

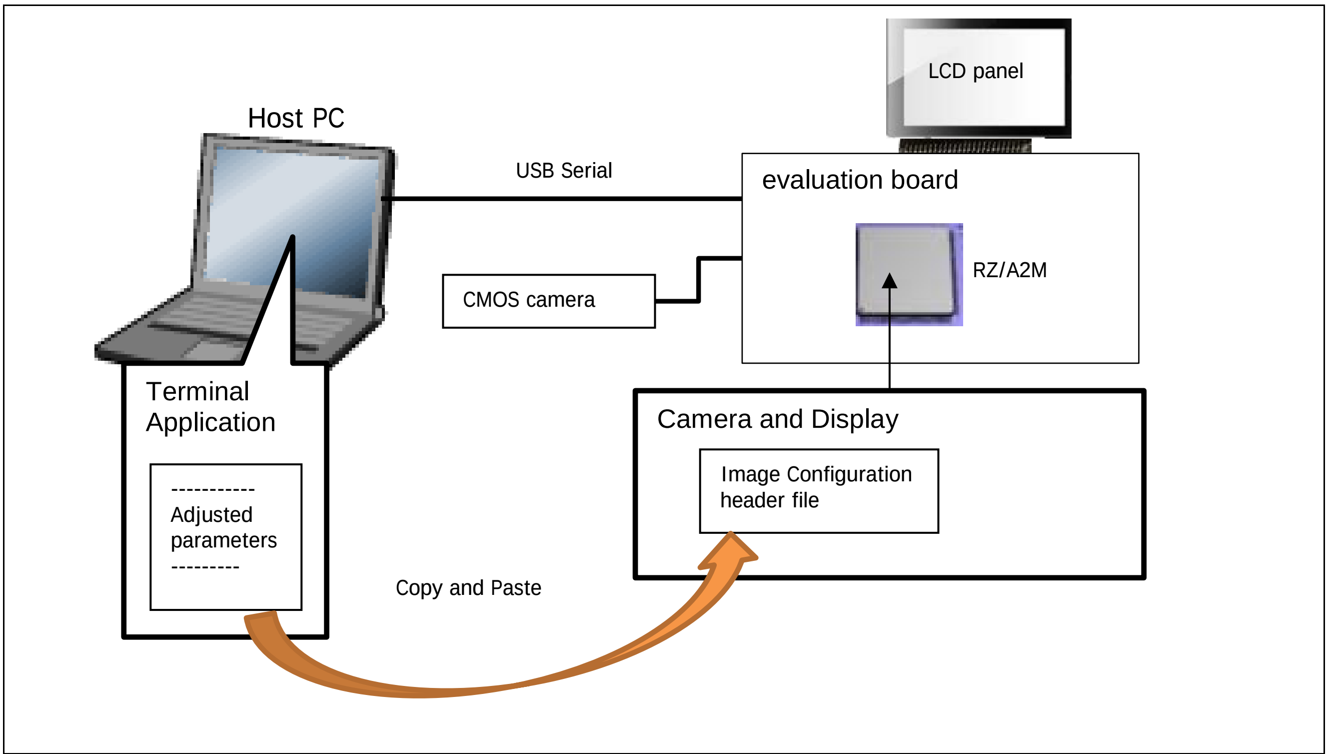


Figure 7-2 Obtaining image adjustment result and applying to sample program.

7.3 Adjusted-Image Capture

Figure 7-3 shows the adjustment timing for each adjusted image.

All of image adjustments are done by hardware. In this sample program, the software can get an adjustment image at the timing indicated in red in Figure 7-3.

In case of doing an image processing (such as recognition processing and JPEG compression for storing JPEG-compressed data), the processing can perform on an adjusted image of "Brightness 1", "Contrast 1", "Rotation and Horizontal Mirroring". Result of image processing will be reflected to "Image quality improver block" and "Output controller block".

But in the case of camera input with CEU, "Brightness 1", "Contrast 1", "Rotation and Horizontal Mirroring" are unusable. And, it is not able to be captured by software that an adjusted image after the timing indicated in red in Figure 7-3.

For details about the hardware blocks of the VDC such as “Input control block”, “Scaler block” and so on, refer to Section 8.1.

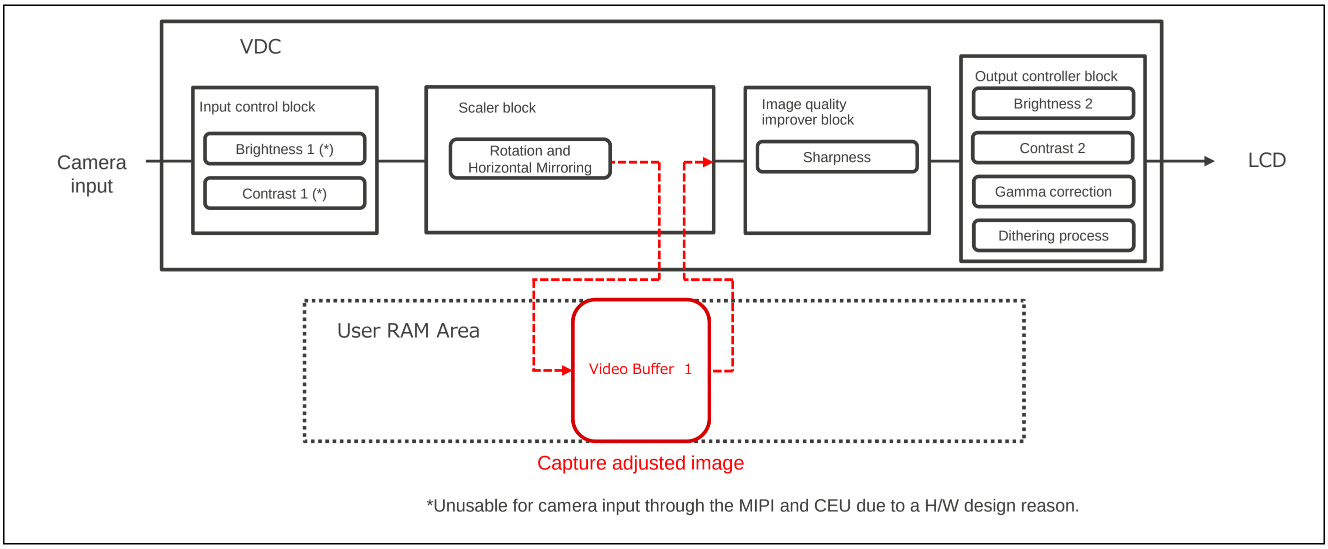


Figure 7-3 Get an adjustment image.

7.3.1 Acquisition of image adjustment value

User can acquire various image adjustment values set by preset selection or custom by executing the R command. When the R command is executed, the current values of the various adjustment parameters are output on the Terminal Application in a format that can be directly applied to the C language source code (header format). To apply the output setting value when initializing this sample, overwrite the contents output on the Terminal Application to the following file the CUI operation commands on the Terminal Application.

(Top)\src\renesas\application\r_image_config.h

8. Image Adjustment Effects and Adjustment Methods

This sample program provides preset values for various possible image adjustments. This section describes the adjustment effects and preset values. It also shows which blocks in the H/W configuration for RZ/A2M image input/output are responsible for adjustments.

8.1 Overall Configuration

Figure 8-1 shows the H/W configuration for RZ/A2M image input/output. Table 8-1 lists the functionalities of the VDC blocks.

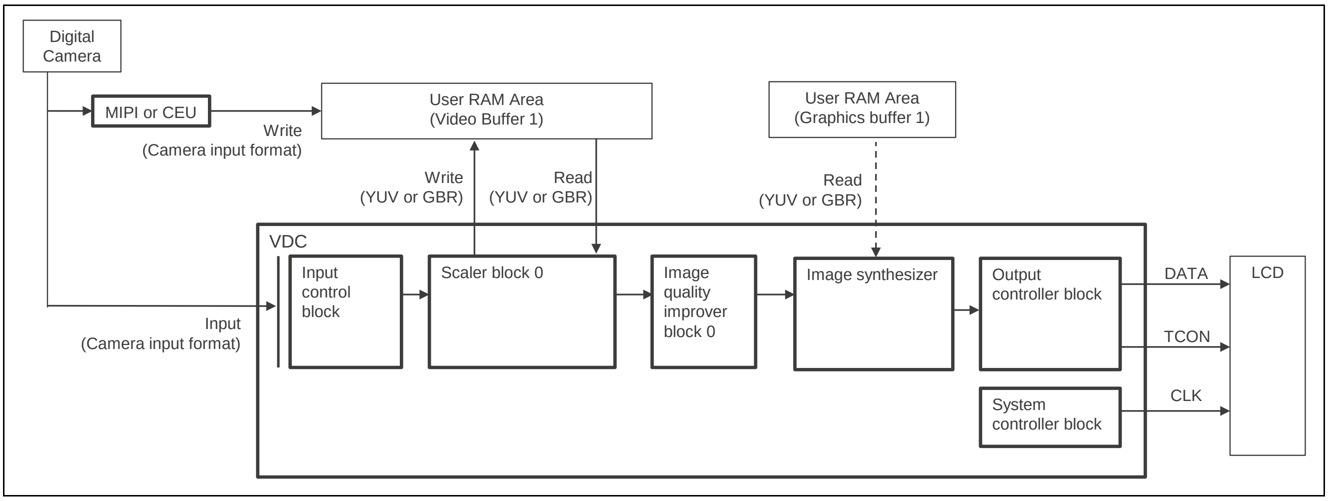


Figure 8-1 Block Diagram of the H/W Configuration for RZ/A2M Image Input/Output

Table 8-1 Functionalities of the VDC Blocks

Block	Functionality
Input control block	Converts the format through a color matrix and adjusts brightness/contrast.
Scaler block 0	Writes/reads an image (YCbCr or RGB) to/from the RAM after format conversion. Performs zoom in/out. Performs rotation/horizontal inversion. Adjusts distortions with the IMR-LS2.
Image quality improver block 0	Improves sharpness.
Image synthesizer	Synthesizes camera images and graphics data stored in the RAM.
Output controller block	Outputs the DATA and TCON signals to the LCD. Performs brightness/contrast adjustment, gamma adjustment, and dithering.
System controller block	Outputs the panel clock signal.

8.2 Brightness

User can adjust brightness of the entire screen. User can make a dark area on the screen lighter and a light area on the screen lighter.

User can adjust brightness with the input control block and output controller block of this sample program. If user adjusts brightness with the input control block, then the brightness-adjusted image data is stored in the RAM, and user can use the adjusted images stored in the RAM. If user adjusts brightness with the output controller block, then the brightness-adjusted data is not stored in the RAM. It is only reflected in the display panel.

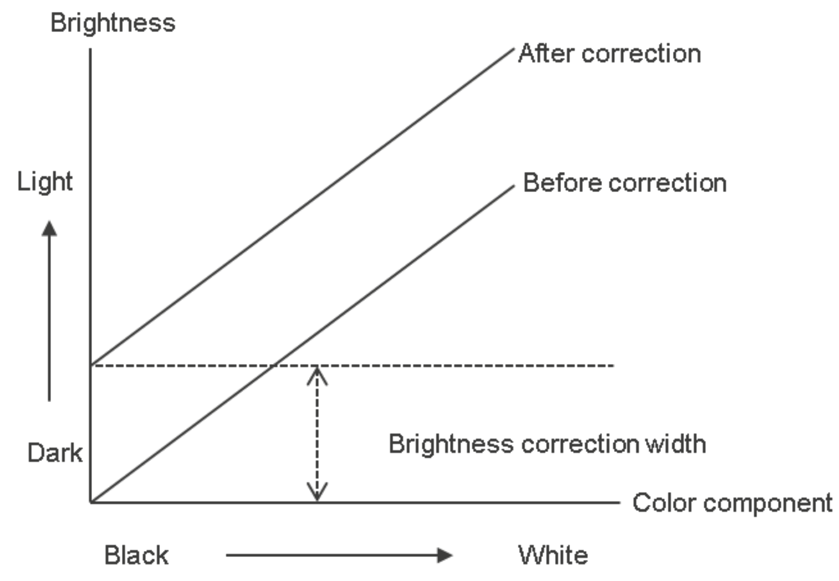


Figure 8-2 **Effects of Brightness Adjustment**

8.2.1 Preset Values

This sample program provides the values listed in Table 8-2 as preset values of brightness. User can select a preset value for each adjustment block. User can adjust brightness with the input control block and output controller block.

Table 8-2 Preset Values of Brightness

Adjustment block	Preset value	Description
Input control block	High	Makes the entire screen lighter.
	Middle	Makes the entire screen a little bit lighter.
	Low	Makes the entire screen darker.
Output controller block	High	Makes the entire screen lighter.
	Middle	Makes the entire screen a little bit lighter.
	Low	Makes the entire screen darker.

8.2.2 Custom Settings

With this sample program, user can configure custom settings for brightness adjustment. Table 8-3 lists target register information.

Table 8-3 Custom Settings for Brightness Adjustment

Adjustment block	Target register	Target bit	Initial value	Setting range	Remarks
Input control block	IMGCNT_MTX_YG_ADJ0	IMGCNT_MTX_YG [7:0]	128	0 to 255	Increasing the value makes the screen lighter.
Output controller block	OUT_BRIGHT1	PBRT_G[9:0]	512	0 to 1023	Increasing the value makes the screen lighter.
	OUT_BRIGHT2	PBRT_B[9:0]	512	0 to 1023	User needs to set the same value to these 3 registers.
	OUT_BRIGHT2	PBRT_R[9:0]	512	0 to 1023	

8.3 Contrast

By increasing the adjustment factor,user can leave a dark part of the screen as it is and make a light part of the screen lighter, emphasizing contrast.

User can adjust contrast with the input control block and output controller block of this sample program. If user adjusts contrast with the input control block, then the contrast-adjusted image data is stored in the RAM, and user can use the adjusted images stored in the RAM. If user adjusts contrast with the output controller block, then the contrast-adjusted data is not stored in the RAM. It is only reflected in the display panel.

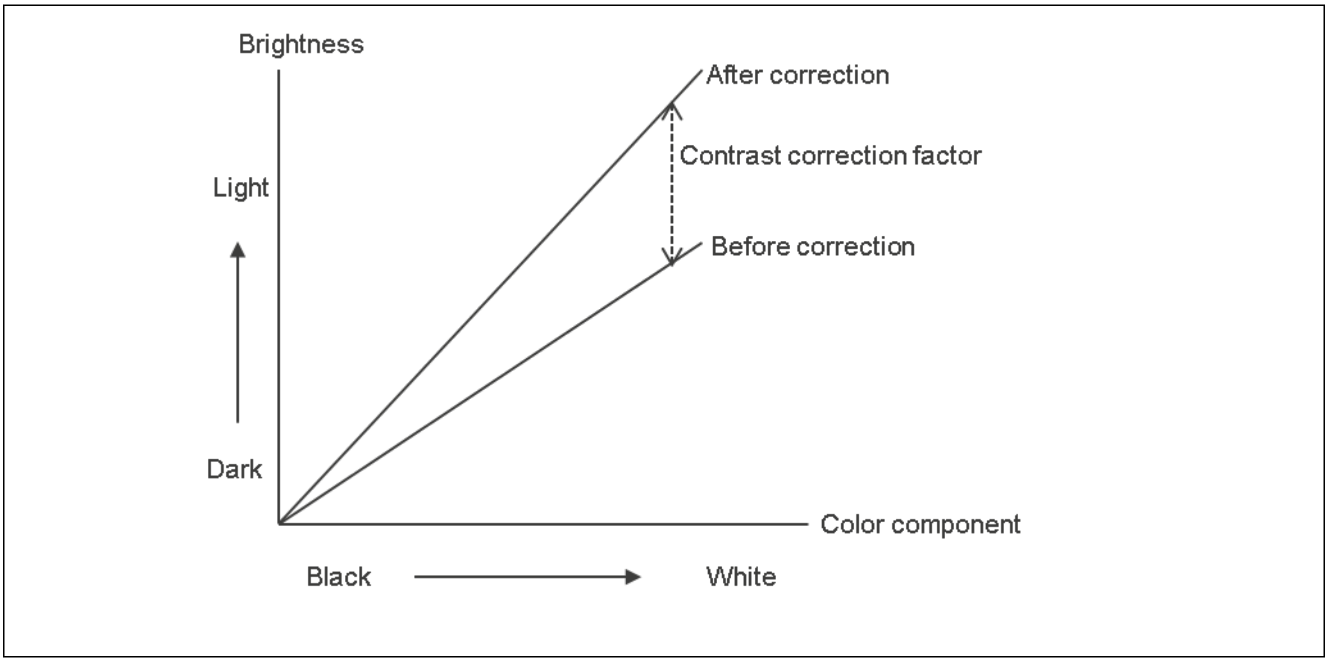


Figure 8-3 Effects of Contrast Adjustment

8.3.1 Preset Values

This sample program provides the values listed in Table 8-4 as preset values of contrast. User can select a preset value for each adjustment block. User can adjust contrast with the input control block and output controller block.

Table 8-4 Preset Values of Contrast

Adjustment block	Preset value	Description
Input control block	High	Emphasizes the light and shade in the entire screen.
	Middle	Slightly emphasizes the light and shade in the entire screen.
	Low	Deemphasizes the light and shade in the entire screen.
Output controller block	High	Emphasizes the light and shade in the entire screen.
	Middle	Slightly emphasizes the light and shade in the entire screen.
	Low	Deemphasizes the light and shade in the entire screen.

8.3.2 Custom Settings

With this sample program, user can configure custom settings for contrast adjustment. Table 8-5 lists target register information.

Table 8-5 Custom Settings for Contrast Adjustment

Adjustment block	Target register	Target bit	Initial value	Setting range	Remarks
Input control block	IMGCNT_MTX_YG_ADJ0	IMGCNT_MTX_GG[10:0]	256	-1024 to 1023	Increasing the value places greater emphasis on the contrasts of light and shade.
Output controller block	OUT_CONTRAST- OUT_CONTRAST- OUT_CONTRAST-	CONT_G[7:0] CONT_B[7:0] CONT_R[7:0]	128 128 128	0 to 255 0 to 255 0 to 255	Increasing the value places greater emphasis on the contrasts of light and shade. User needs to set the same value to these 3 registers.

8.4 Sharpness

By increasing the brightness difference between adjacent pixels (LTI adjustment) and improving the brightness overshoot and undershoot (sharpness), user can emphasize the contour.

With this sample program, user can adjust sharpness by using the image quality improver block. Sharpness-adjusted data is not stored in the RAM. It is only reflected in the display panel.

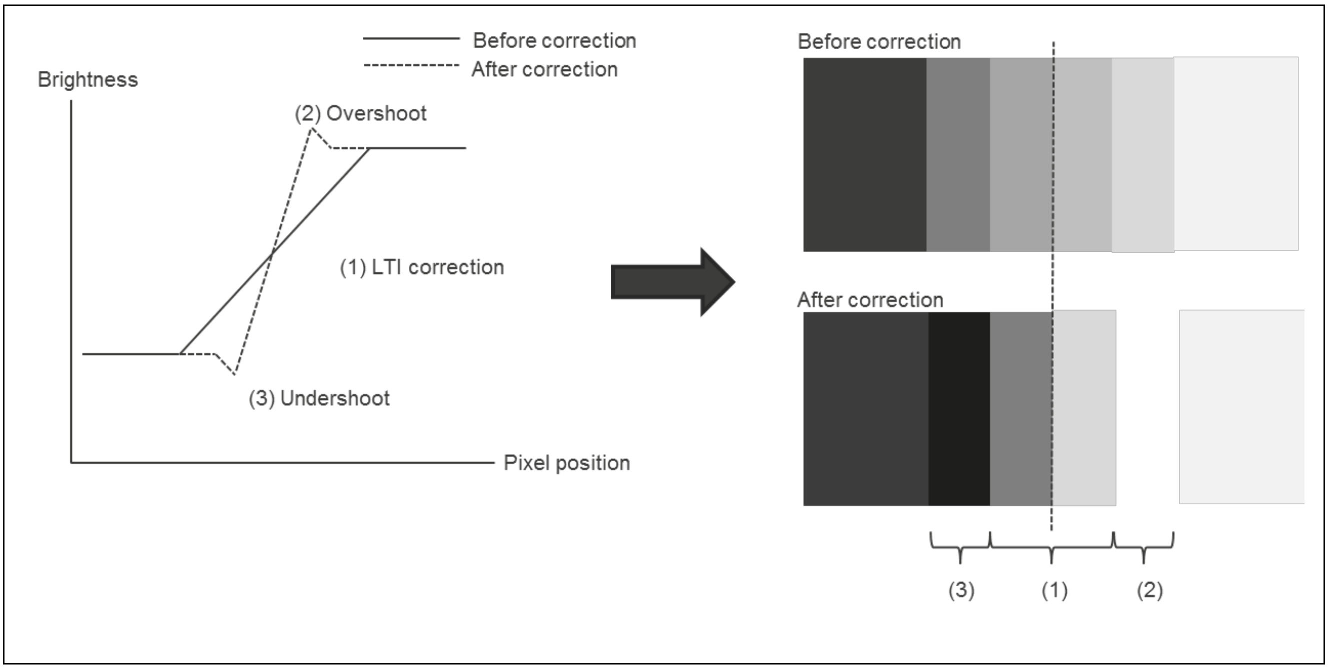


Figure 8-4 Effects of Sharpness Adjustment

8.4.1 Preset Values

This sample program provides the values listed in Table 8-6 as preset values of sharpness.

Table 8-6 Preset Values of Sharpness

Adjustment block	Preset value	Description
Image quality improver block	Strong	Puts maximum emphasis on the contour.
	Semi-strong	Puts medium emphasis on the contour.
	Weak	Puts minimum emphasis on the contour.

8.4.2 Custom Settings

With this sample program, user can configure custom settings for sharpness adjustment. Table 8-7, Table 8-8, and Table 8-9 list target register information.

Table 8-7 Custom Settings for Sharpness Adjustment (1/3)

Adjustment block	Target register	Target bit	Initial value	Setting range	Remarks
Image quality improver block	ADJ0_ENH_SHP1	SHP_H_ON	0	0 to 1	0: Sharpness ON 1: Sharpness OFF
	ADJ0_ENH_SHP1	SHP_H1_CORE [6:0]	0	0 to 127	Used to specify the range of available sharpness settings for the horizontal sharpness band (H1). The contour is emphasized when the edge amplitude value is greater than or equal to this setting.
	ADJ0_ENH_SHP2	SHP_H1_CLIP_O [7:0]	0	0 to 255	Used to adjust the clip value of overshoot for the horizontal sharpness band (H1).
	ADJ0_ENH_SHP2	SHP_H1_CLIP_U [7:0]	0	0 to 255	Used to adjust the clip value of undershoot for the horizontal sharpness band (H1).
	ADJ0_ENH_SHP2	SHP_H1_GAIN_O [7:0]	0	0 to 255	Gain value for the edge amplitude value of overshoot for the horizontal sharpness band (H1). 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_SHP2	SHP_H1_GAIN_U [7:0]	0	0 to 255	Gain value for the edge amplitude value of undershoot for the horizontal sharpness band (H1). 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_SHP3	SHP_H2_LPF_SEL	0	0 to 1	LPF settings for the horizontal sharpness band (H2) 0: LPF not present 1: LPF present
	ADJ0_ENH_SHP3	SHP_H2_CORE [6:0]	0	0 to 127	Used to specify the range of available sharpness settings for the horizontal sharpness band (H2). The contour is emphasized when the edge amplitude value is greater than or equal to this setting.
	ADJ0_ENH_SHP4	SHP_H2_CLIP_O [7:0]	0	0 to 255	Used to adjust the clip value of overshoot for the horizontal sharpness band (H2).

Table 8-8 Custom Settings for Sharpness Adjustment (2/3)

Adjustment block	Target register	Target bit	Initial value	Setting range	Remarks
Image quality improver block	ADJ0_ENH_SHP4	SHP_H2_CLIP_U [7:0]	0	0 to 255	Used to adjust the clip value of undershoot for the horizontal sharpness band (H2).
	ADJ0_ENH_SHP4	SHP_H2_GAIN_O [7:0]	0	0 to 255	Gain value for the edge amplitude value of overshoot for the horizontal sharpness band (H2) 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_SHP4	SHP_H2_GAIN_U [7:0]	0	0 to 255	Gain value for the edge amplitude value of undershoot for the horizontal sharpness band (H2) 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_SHP5	SHP_H3_CORE [6:0]	0	0 to 127	Used to specify the range of available sharpness settings for the horizontal sharpness band (H3) The contour is emphasized when the edge amplitude value is greater than or equal to this setting.
	ADJ0_ENH_SHP6	SHP_H3_CLIP_O [7:0]	0	0 to 255	Used to adjust the clip value of overshoot for the horizontal sharpness band (H3)
	ADJ0_ENH_SHP6	SHP_H3_CLIP_U [7:0]	0	0 to 255	Used to adjust the clip value of undershoot for the horizontal sharpness band (H3)
	ADJ0_ENH_SHP6	SHP_H3_GAIN_O [7:0]	0	0 to 255	Gain value for the edge amplitude value of overshoot for the horizontal sharpness band (H3) 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_SHP6	SHP_H3_GAIN_U [7:0]	0	0 to 255	Gain value for the edge amplitude value of undershoot for the horizontal sharpness band (H3) 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_LTI1	LTI_H_ON	0	0 to 1	0: LTI ON 1: LTI OFF
	ADJ0_ENH_LTI1	LTI_H2_LPF_SEL	0	0 to 1	LPF settings for the horizontal LTI (H2) band 0: LPF present 1: LPF not present

Table 8-9 Custom Settings for Sharpness Adjustment (3/3)

Adjustment block	Target register	Target bit	Initial value	Setting range	Remarks
Image quality improver block	ADJ0_ENH_LTI1	LTI_H2_INC_ZERO [7:0]	10	0 to 255	LTI adjustment threshold value for the median filter (for noise elimination). LTI is not adjusted if the frequency difference from the adjacent pixel is less than or equal to this setting.
	ADJ0_ENH_LTI1	LTI_H2_GAIN [7:0]	0	0 to 255	Gain value for the edge amplitude value of the LTI for the horizontal LTI (H2) band. 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_LTI1	LTI_H2_CORE [7:0]	0	0 to 255	Coring for the LTI for the horizontal LTI (H2) band. Coring is processed for amplitudes which are less than or equal to this setting.
	ADJ0_ENH_LTI2	LTI_H4_MEDIAN_TAP_SEL	0	0 to 1	Used to select a reference pixel for the median filter (for noise elimination) for the horizontal LTI (H4) band. 0: References the second adjacent pixel. 1: References the first adjacent pixel.
	ADJ0_ENH_LTI2	LTI_H4_INC_ZERO [7:0]	10	0 to 255	Adjustment threshold setting for median filter (for noise elimination) for the horizontal LTI (H4) band.
	ADJ0_ENH_LTI2	LTI_H4_GAIN [7:0]	0	0 to 255	Gain value for the edge amplitude value of the LTI for the horizontal LTI (H4) band. 0 (0x) - 64 (+1x) - 255 (+4x)
	ADJ0_ENH_LTI2	LTI_H4_CORE [7:0]	0	0 to 255	Coring for the LTI for the horizontal LTI (H4) band. Coring is processed for amplitudes which are less than or equal to this setting.

8.5 Gamma Adjustment

This sample program can apply gamma adjustments shown in Figure 8-5 to 256-tone input signals. The output control block makes gamma adjustments, and the results are only reflected in the display panel.

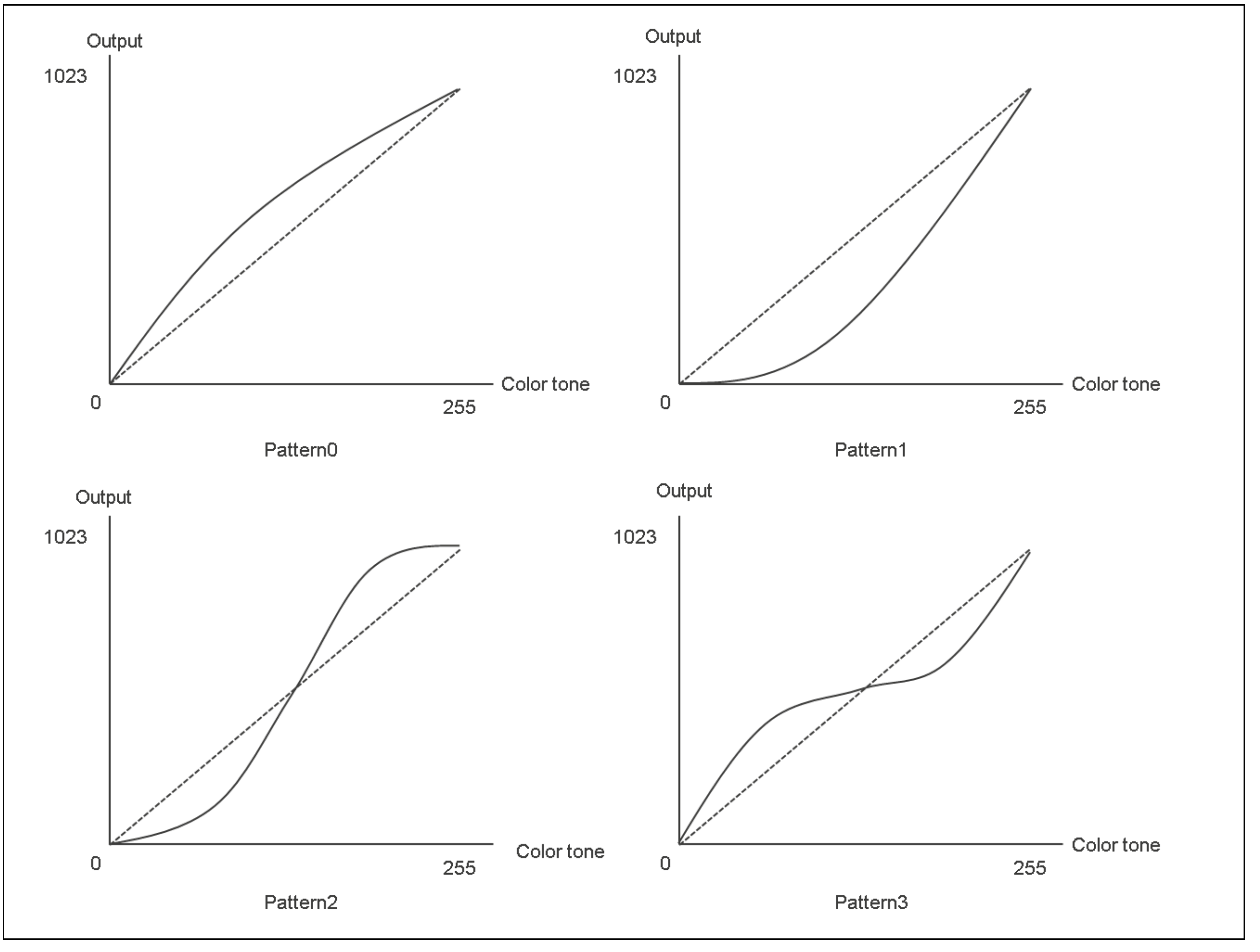


Figure 8-5 Gamma Adjustments Which Can Be Applied by This sample program

8.5.1 Preset Values

This sample program provides the values listed in Table 8-10 as preset values for gamma adjustments.

Table 8-10 Preset Values for Gamma Adjustments

Adjustment block	Preset value	Description
Output controller block	Pattern0	Gamma adjustment with γ=0.81. Makes the entire screen slightly lighter (see Note).
	Pattern1	Gamma adjustment with γ=1.98. Makes the entire screen slightly darker (see Note).
	Pattern2	Gamma adjustment with an S-shaped curve. Slightly increases contrast.
	Pattern3	Gamma adjustment with an inverse S-shaped curve. Slightly decreases contrast.

Note: Maximum and minimum values which can be set with the RZ/A2M.

8.5.2 Custom Settings

This sample program does not support custom settings for gamma adjustments.

8.6 Dithering Process

Dithering process can prevent color banding. Color banding occurs if the number of bits for processing images with the RZ/A2M exceeds that of bits output to the display panel.

If, for example, image data processed in the RGB888 (24-bit) format is output in the RGB565 (16-bit) format, then the number of tones which can be expressed is reduced. As a result, a smooth gradation pattern might look like a striped pattern. This problem is called color banding. It can be fixed by dithering.

Note that if the number of bits for processing images with the RZ/A2M is less than or equal to that of bits output to the display panel, then dithering is ineffective.

8.6.1 Preset Values

This sample program provides the mode values listed in Table 8-11 as preset values for dithering.

Table 8-11 Preset Values for Dithering

Adjustment block	Preset value	Description
Output control block	Cutoff	Cutoff mode. Truncates the fractional part of the calculation result for bit degeneration.
	Round off	Roundoff mode. Rounds the calculation result to the nearest integer for bit degeneration.
	2x2 Pattern Dither	2x2 pattern dither. Adds a pattern value to the figure in the first decimal place and truncates the fractional part of the result for bit degeneration.
	Random Pattern Dither	Random pattern dither. Adds a random pattern value to the figure in the first decimal place and truncates the fractional part of the result for bit degeneration.

8.6.2 Custom Settings

This sample program does not support custom settings for dithering.

8.7 Rotation and Horizontal Mirroring

Rotation and horizontal mirroring are processed by “scaler block 0” of VDC and output the processing result to buffer of camera input (refer to “User RAM Area (Video Buffer 1)” in Figure 8-1).

Rotation and horizontal mirroring are not able to use at same time. The possible values are shown in Table 8-13. In case of set 90 degrees rotation or 270 degrees rotation, need to change size of buffer of camera input because vertical and horizontal of image will change. And this function unusable in the case of camera input with MIPI and CEU.

8.7.1 Preset Values

This sample program provides the mode values listed in Table 8-12 as preset values for rotation and horizontal mirroring.

Table 8-12 Preset Values for Dithering

Adjustment block	Preset value	Description
Scaler block 0	Horizontal Mirroring ON Rotation (180 Degrees)	Horizontal mirroring 180 degrees Rotation

8.7.2 Custom Settings

With this sample program, user can configure custom settings for rotation and horizontal mirroring. Table 8-13 lists target register information.

Table 8-13 Custom Settings for Brightness Adjustment

Adjustment block	Target register	Target bit	Initial value	Setting range	Remarks
Scaler block 0	SC0_SCL1_WR1	SC0_RES_DS_WR_MD[2:0]	0	0 to 4	0: Normal 1: Horizontal mirroring 2: 90 degrees rotation (Note 1) 3: 180 degrees rotation 4: 270 degrees rotation (Note 1)

Note 1. Need to change buffer size for camera input if use “90 degrees rotation” or “270 degrees rotation” setting.

9. Using the Sample Program and "Camera / Display Tuning RZ (QE)"

This sample program can be linked with the development support tool "Camera / Display Tuning RZ (QE)". "Camera / Display Tuning RZ (QE)" is a plugin of the integrated development environment e2 studio and it can adjust the timing of the LCD panel with GUI. The timing setting value adjusted with "Camera / Display Tuning RZ (QE)" can be output as a header file, and by replacing it with the header file of this sample program, the setting value in the GUI can be used as initial settings of this sample program. The procedure for applying the result adjusted by "Camera / Display Tuning RZ (QE)" to this sample program is described in this section.

To install the "Camera / Display Tuning RZ (QE)" tool, click e2 studio menu "Help" → "Install New Software". Refer to the following website for more detail.

- Product page

https://www.renesas.com/qe-display

9.1 Launching "Camera / Display Tuning RZ (QE)"

From the e2 studio menu select **Renesas Views** → **Renesas QE** → **Camera / Display Tuning (QE)** to launch Camera / Display Tuning RZ (QE) (Figure 9-1).

The block diagram shown in Figure 9-1 indicates H/W block diagram of VDC and user can make out the image data flow between camera input and display output. Also, user can make out the positional relationship of various image correction.

Various image correction can be adjusted after clicking some image correction button such as Brightness, Contrast, Sharpness, and so on. The tab will move to "Image Quality Adjustment" tab after clicking image correction buttons. For detail of the way of image adjustment.

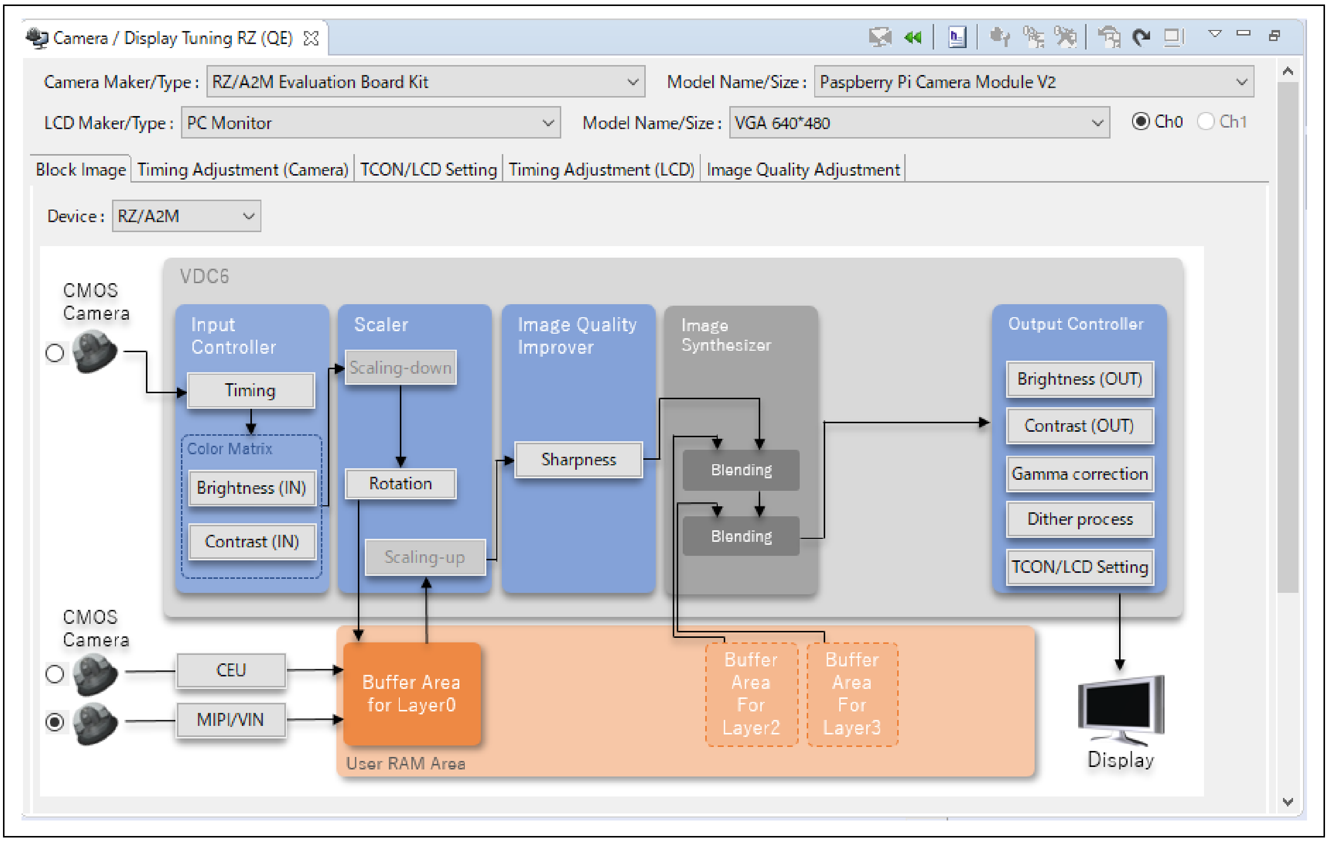


Figure 9-1 Camera / Display Tuning RZ (QE) Launch Screen

9.2 Display Device Information Settings

Select “**Custom…**” from the **LCD Maker/Type** pull-down list at the top of the dialog box shown in Figure 9-2 to display the **Edit Custom Display Data** dialog box (Figure 9-2). The display device information is input into this dialog box.

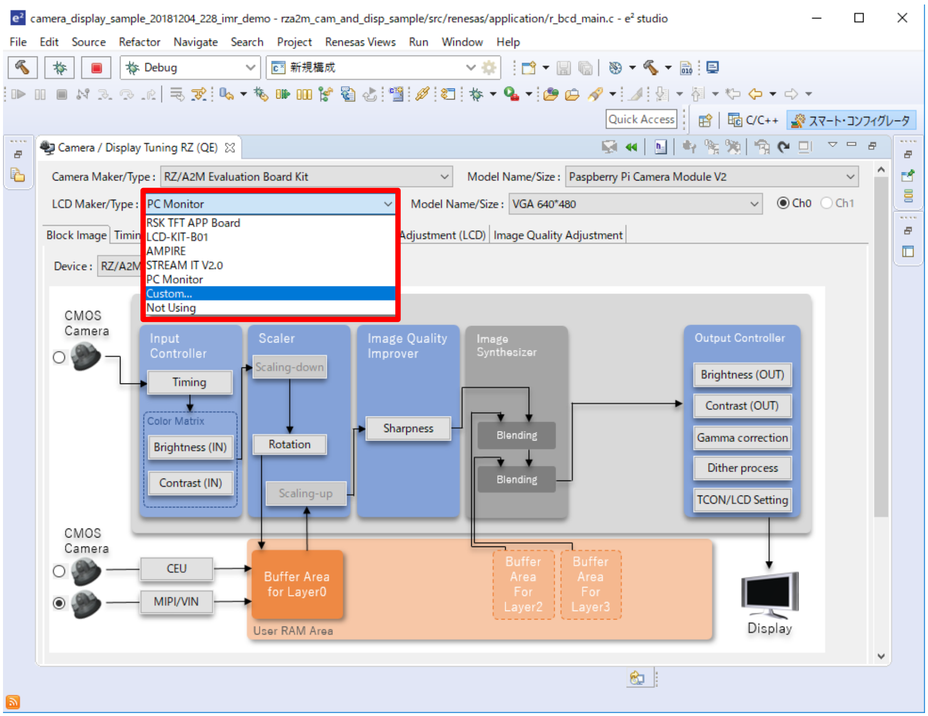


Figure 9-2 Camera / Display Tuning RZ (QE) image

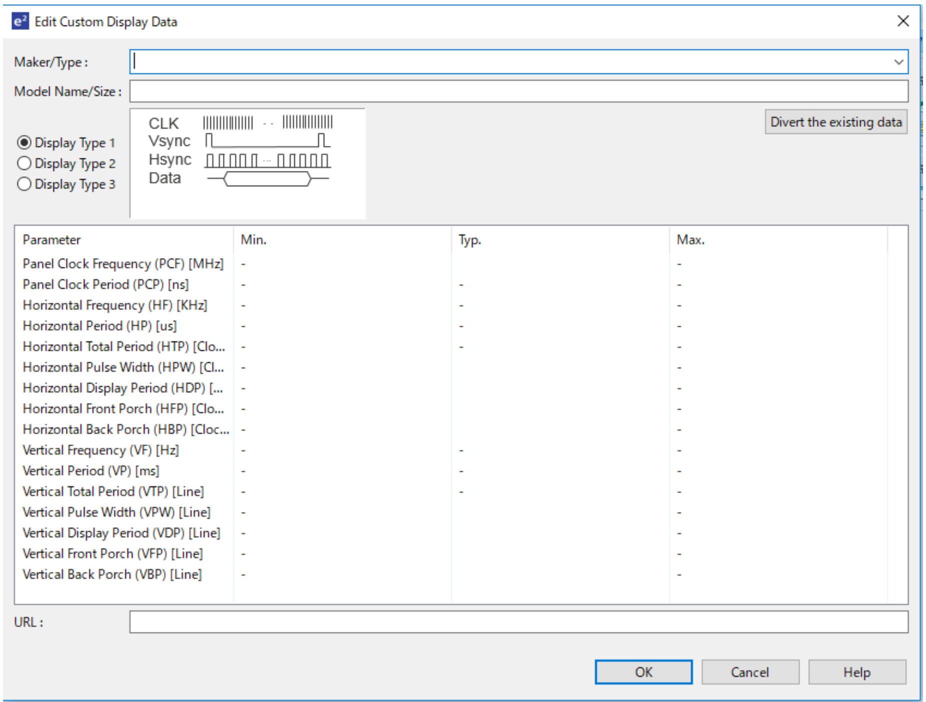


Figure 9-3 Edit Custom Display Data Dialog Box

9.2.1 Entering a Registered Name

Enter any name you wish in the **Maker/Type** and **Model Name/Size** fields of the **Edit Custom Display Data** dialog box (Figure 9-4). This name will be registered in the drop-down list and will become selectable.

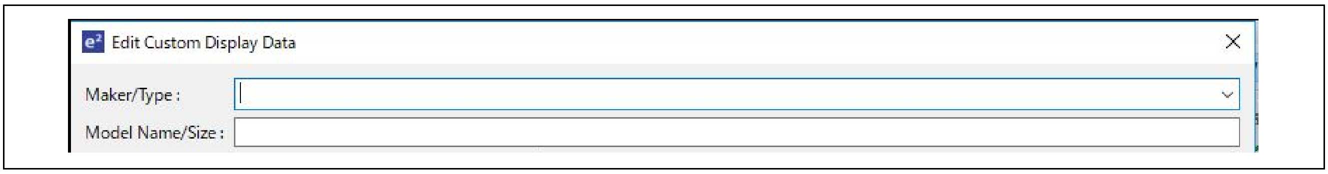


Figure 9-4 Name Registration

9.2.2 Inputting Control Timing Values

The Edit Custom Display Data dialog box needs to be filled in by user according to the specification of display equipment like section 5.2 (Figure9-5). The values input under **Typ** are used for timing control, and the values input under **Min** and **Max** are used to confirm that values are within the allowable range when the GUI is used for timing adjustment in Camera / Display Tuning RZ (QE).

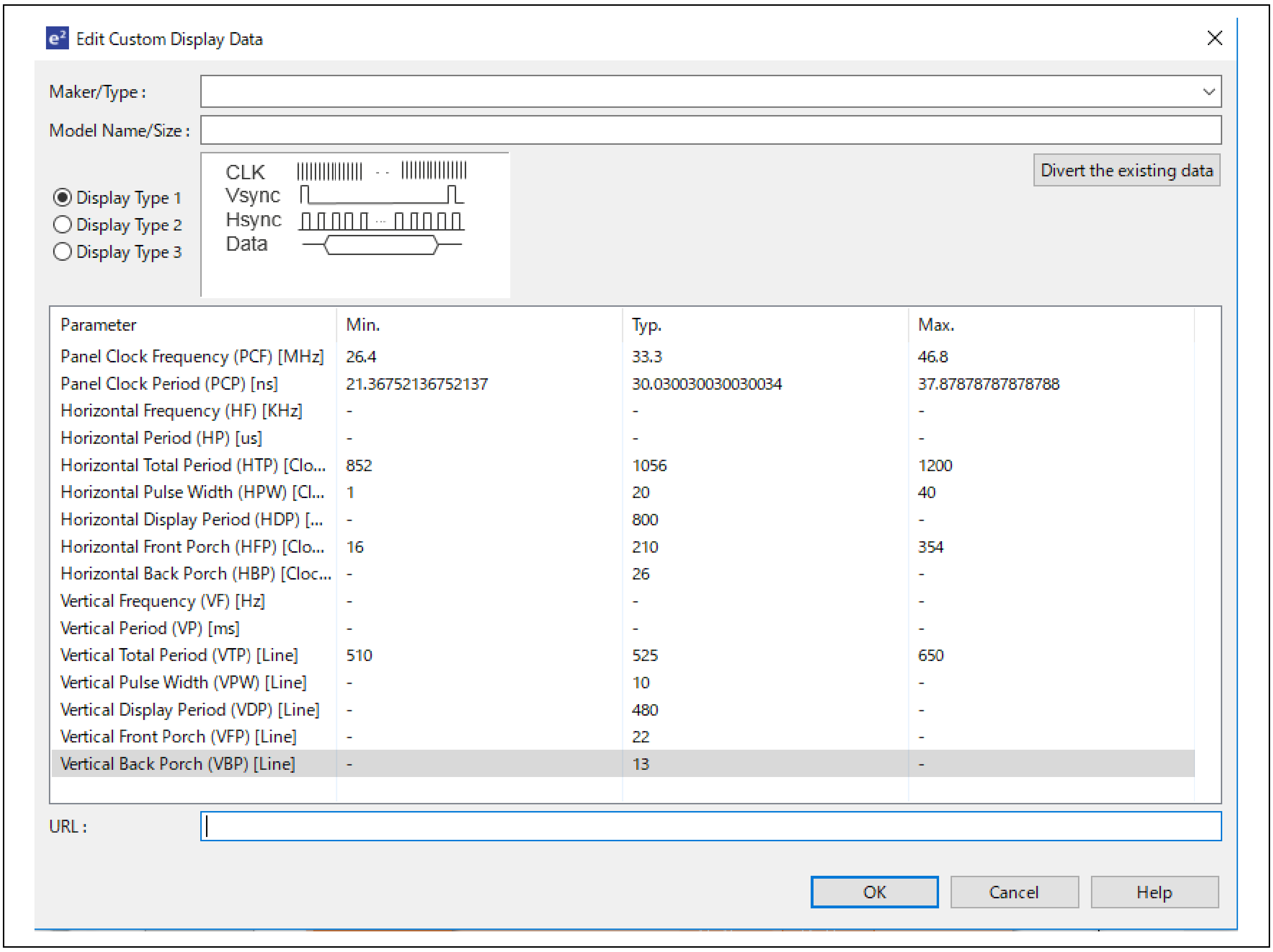


Figure 9-5 Inputting Control Timing Values

9.2.3 Control Signal Output Settings

Control signal output can be set by clicking the “TCON/LCD Setting” tab in Camera / Display Tuning RZ (QE) (Figure 9-6)

In this dialog box, output settings can be configured for the control signals as listed below.

[Panel Driver Signal (TCON) Output Selection]

- Output pin selection:
  Output to pins LCD_TCON0 to LCD_TCON6 (TCON0 to TCON6)
- Control signal polarity:
  Positive polarity (high active)
  Negative polarity (low active)

[LCD setting]

- LCD Output Format:
  24-bit RGB888 output (24-bit (VDC_LCD_OUTFORMAT_RGB888))
  18-bit RGB666 output (18-bit (VDC_LCD_OUTFORMAT_RGB666))
  16-bit RGB565 output (16-bit (VDC_LCD_OUTFORMAT_RGB565))
- Timing of Output Data:
  Output at rising edge of panel clock (Rising (VDC_EDGE_RISING))
  Output at falling edge of panel clock (Falling (VDC_EFGE_FALLING))

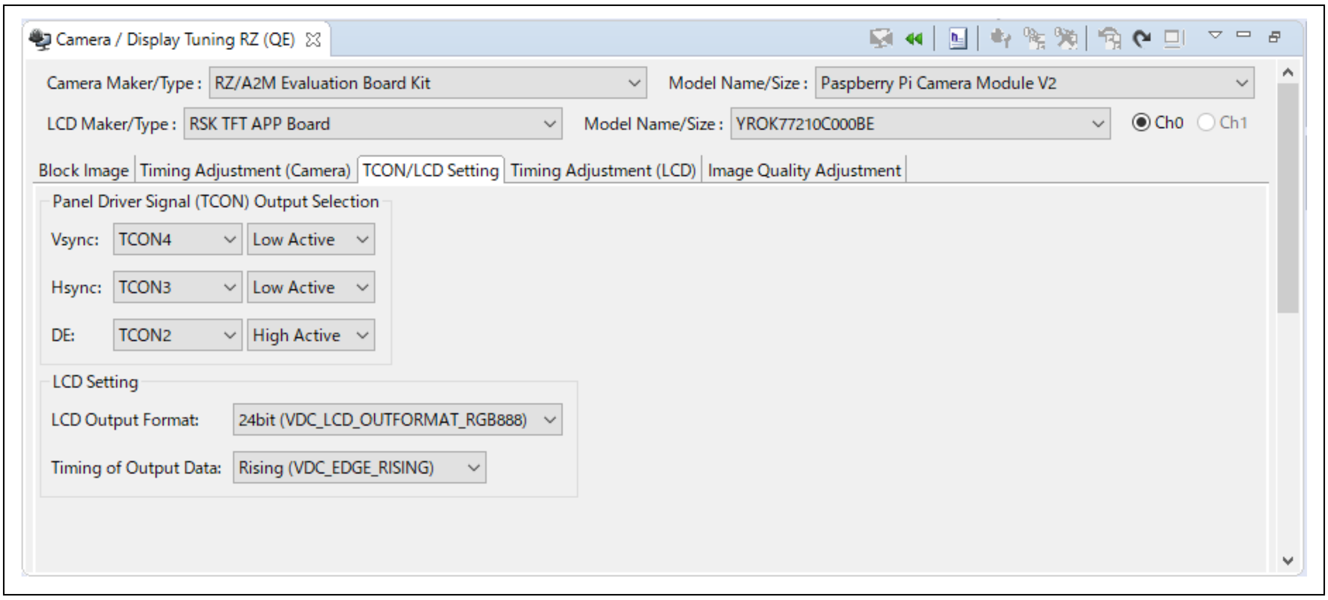


Figure 9-6 TCON and LCD Settings

9.2.4 Adjusting the Position of Display

After connecting the debugger and launching the sample program, user can set the control signal timing by changing the setting values shown in Figure 9-7. Adjustment them by viewing the results on the connected display device, then re-output the header file. Refer to Section 9.4 regarding the explanation about how to generate a header file.

In case of the set value in Timing Adjustment dialog box is indicated in red, it means the “Out of range error”. In this case, adjust the parameter so that the value is set within the VDC specification. The valid value range of the VDC specification can be confirmed by pointing the mouse to the adjustment value indicated in red.

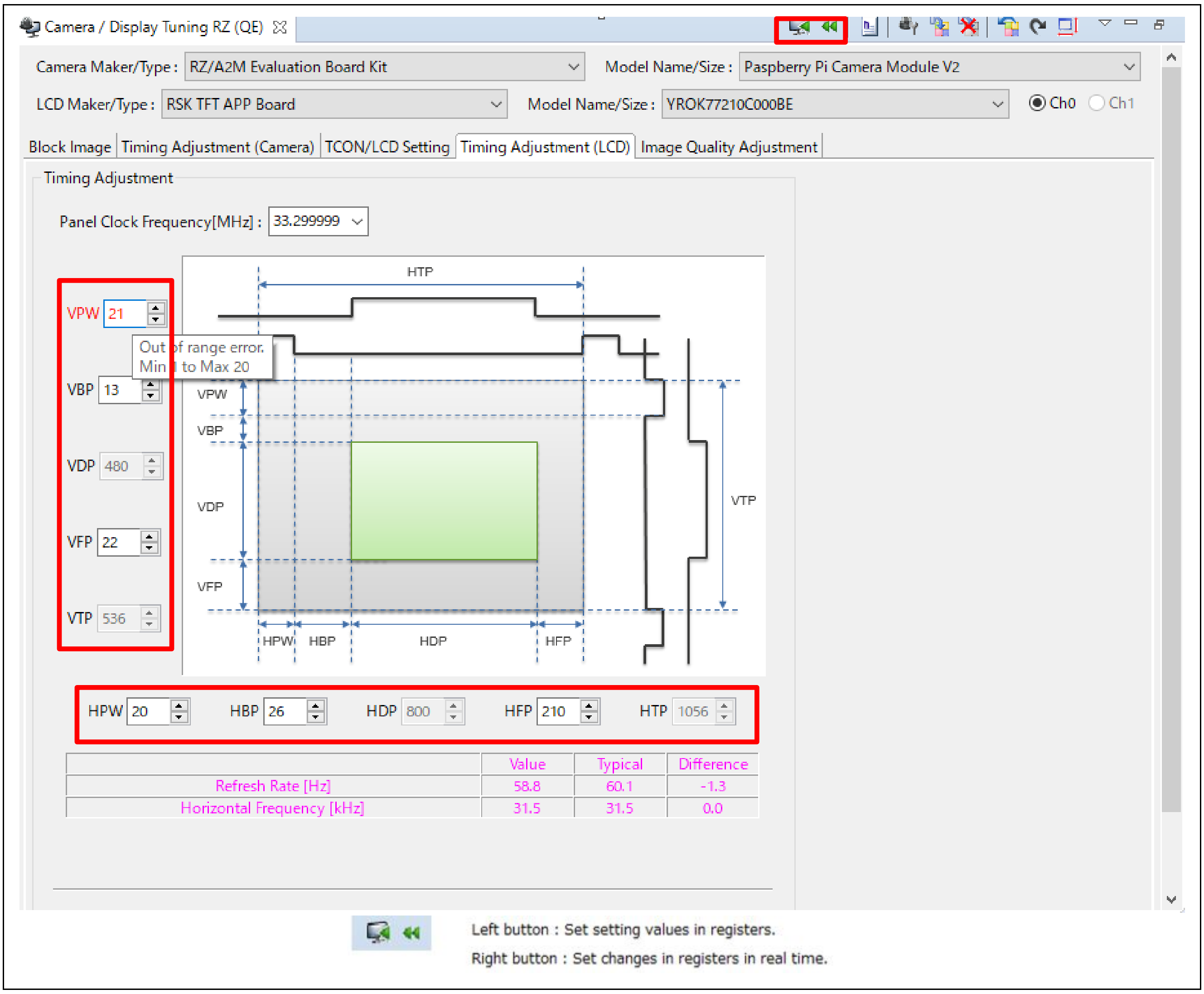


Figure 9-7 Debugging the Control Signal Timing

9.3 Image Quality Adjustment

After connecting the debugger and launching the sample program, user can adjust various image adjustment by clicking on the image adjustment contents in “Block Diagram” tab (Figure9-8) , user can switch to the image adjustment tab and adjust various images.

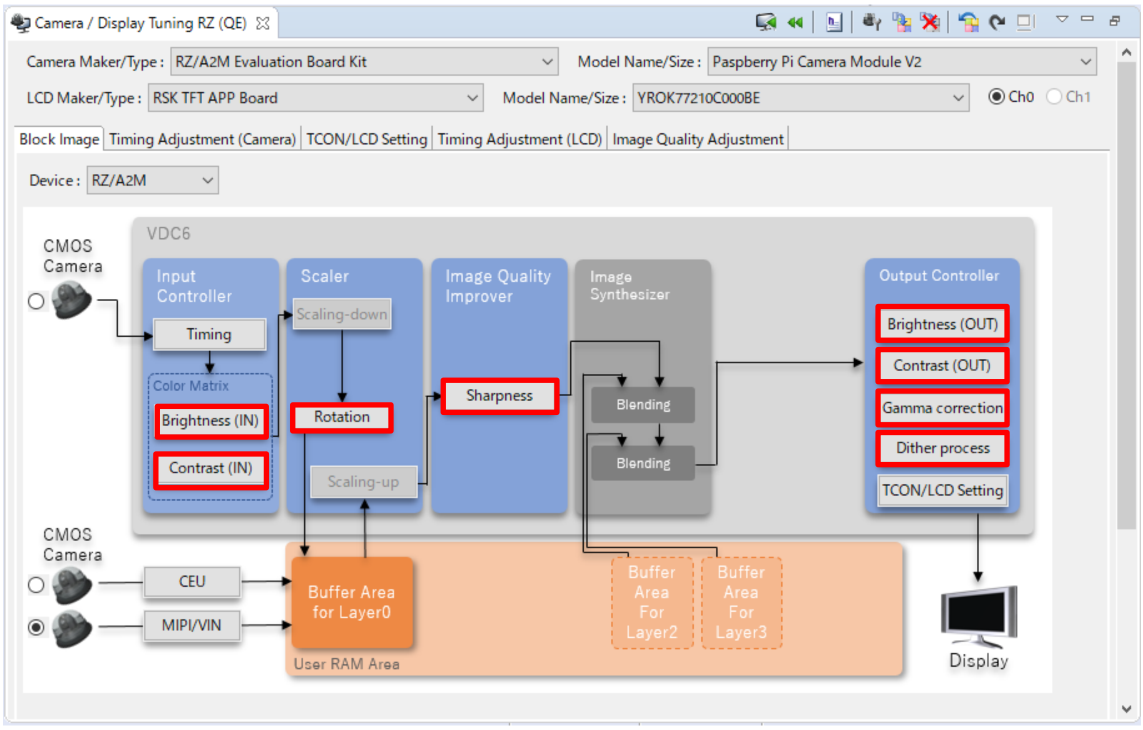


Figure9-8 Selection of Image Quality Adjustment

User can adjust various image adjustment in “Image Quality Adjustment” tab. The image adjustment can be controlled by “Quick Setting” or “Custom” (Figure 9-9). In case of adjusting by “Custom”, refer to the hardware manual to confirm the setting contents and range of each register.

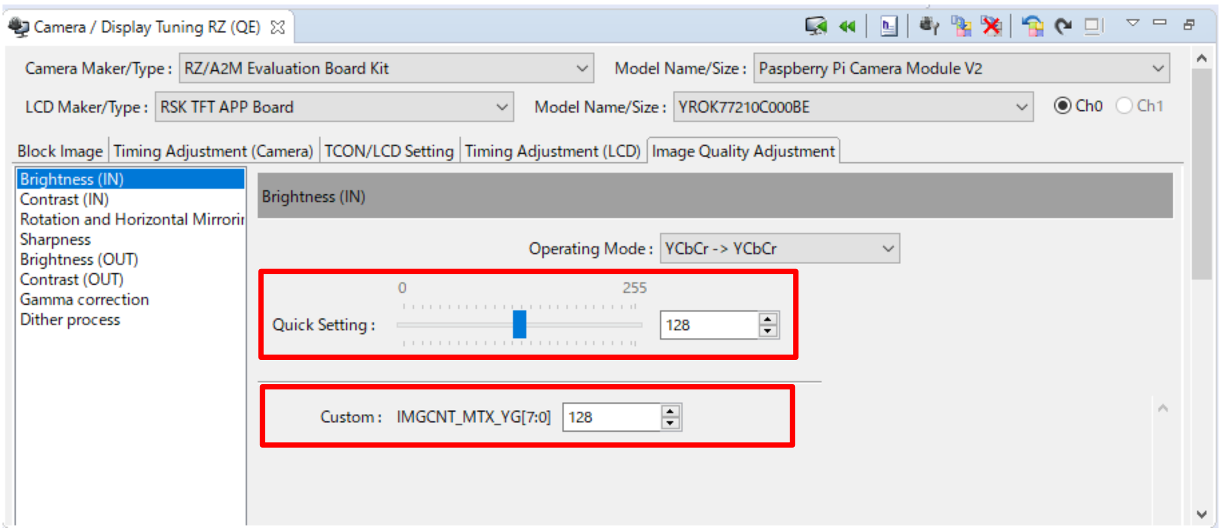


Figure 9-9 Image Quality Adjustment image

9.4 Generating a Header File including user configurations

A header file reflecting the user configuration can be generated by clicking the generate header file icon (Figure 9-10) in Camera / Display Tuning RZ (QE).

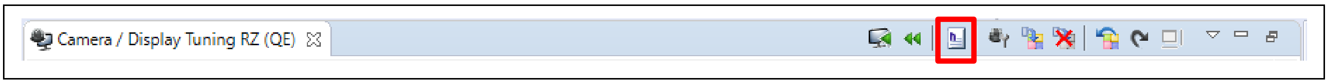


Figure 9-10 Generating a Header File icon

User can generate following three types of header files as shown in Figure 9.11.

"For Camera Timing Setting" configured in Section 9.2.4.

"For LCD Timing and TCON Setting" configured in Section 9.2.3.

"For Image Adjustment" configured in Section 9.3.

The header file can be generated by clicking the check box of the header files user wants to generate, then clicking the "Generate" button. The header file name and the path for output files can be specified by the user (Figure9-11).

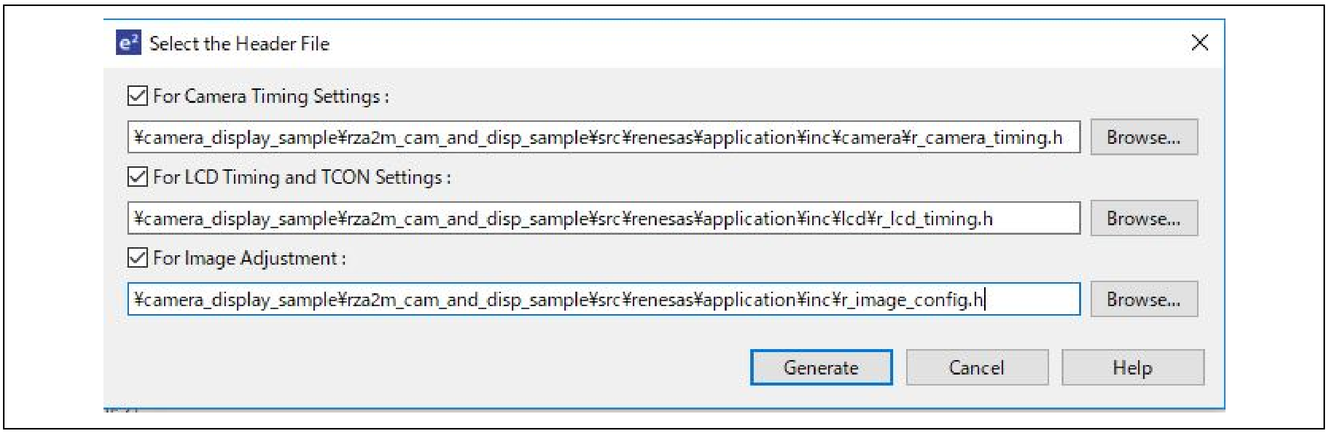


Figure 9-8 Generating a Header File including user configurations

9.5 Timing Adjustment for MIPI Camera

By connecting the debugger, and running the sample program, user can change the parameters for timing of MIPI control signals in “Timing Adjustment (Camera)” tab as shown in Figure 9-12.

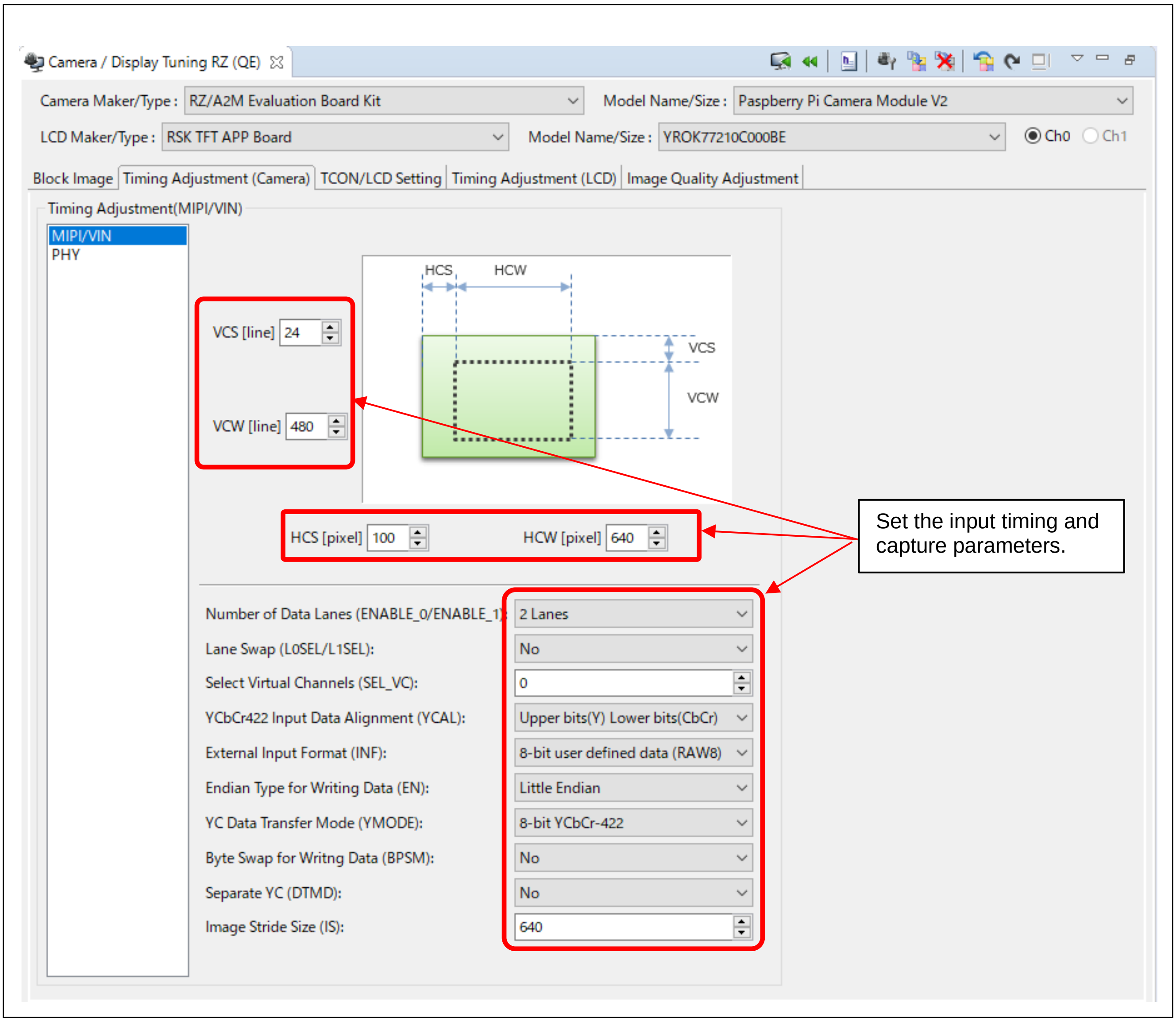


Figure 9-9 Adjusting Camera Input Timing

9.6 Camera control access via I2C

By connecting the debugger, and running the sample program, then click the “Send the Camera Module Data” icon (Figure 9-13), “Send the Camera Module Data” dialog box can be opened (Figure 9-14).

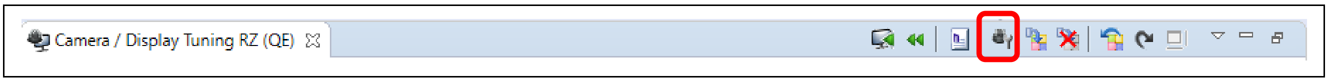


Figure 9-10 Open Send the Camera Module Data dialog box

In this dialog box, user can control the connected camera module via I2C access.

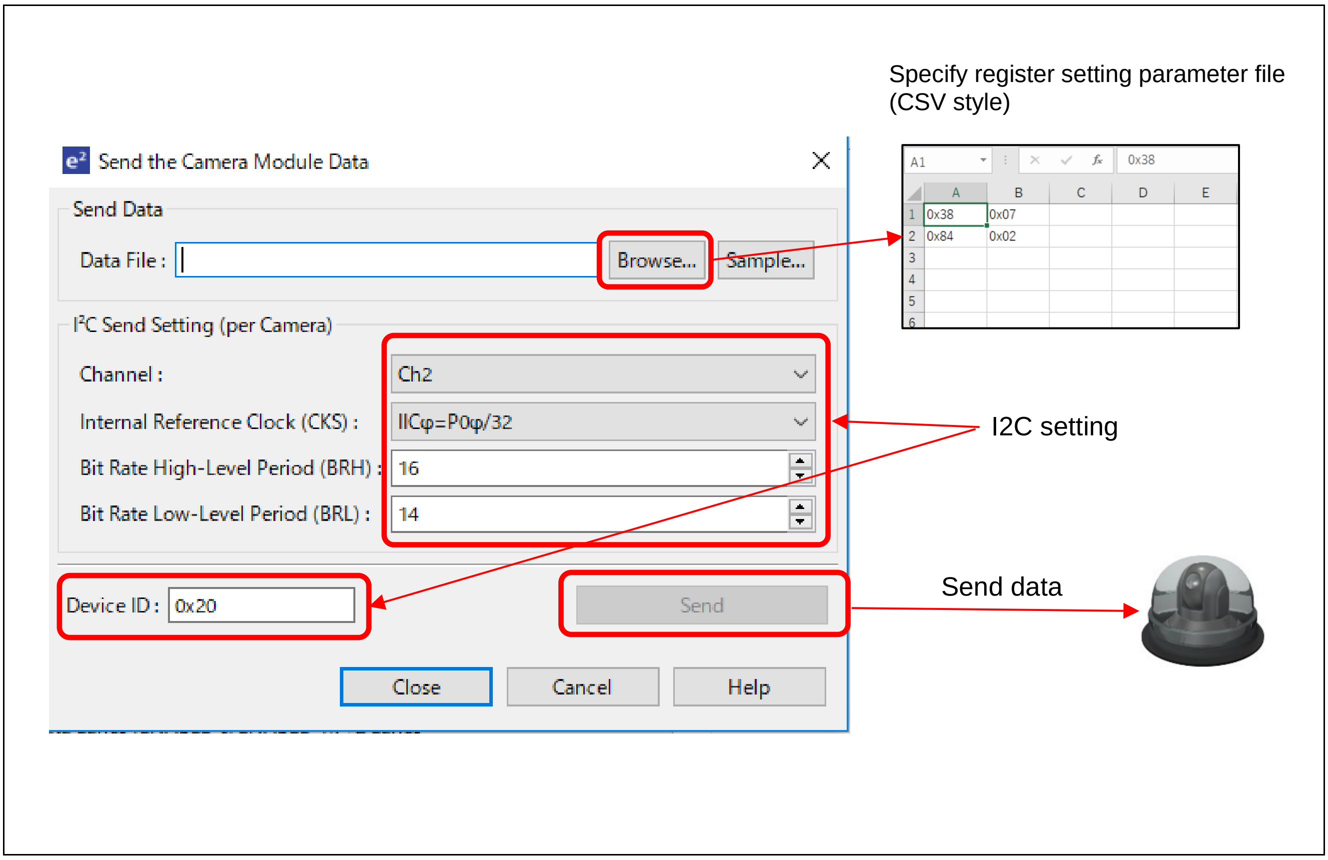


Figure 9-14 Setting of Camera Module Registers via I2C

10. Reference Documents

User's Manual: Hardware

RZ/A2M Group User's Manual: Hardware

The latest version can be downloaded from the Renesas Electronics website.

RTK7921053C00000BE (RZ/A2M CPU board) User's Manual

The latest version can be downloaded from the Renesas Electronics website.

RTK79210XXB00000BE (RZ/A2M SUB board) User's Manual

The latest version can be downloaded from the Renesas Electronics website.

ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition Issue C

The latest version can be downloaded from the ARM website.

ARM CortexTM-A9 (Revision: r4p1) Technical Reference Manual

The latest version can be downloaded from the ARM website.

ARM Generic Interrupt Controller Architecture Specification - Architecture version 2.0

The latest version can be downloaded from the ARM website.

ARM CoreLinkTM Level 2 Cache Controller L2C-310 (Revision: r3p3) Technical Reference Manual

The latest version can be downloaded from the ARM website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

Integrated development environment e2studio User’s Manual can be downloaded from the Renesas Electronics website.

The latest version can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.14.18	-	First edition issued
1.01	Dec.28.18	34~43	Addition 9.Using the Sample Program and “Camera / Display Tuning RZ (QE)”
1.02	Apr.15.19	8	・Modified name of image display board to “Display output board”. ・Modified the header file of the image display board to ”lcd_dvi_clk.h”. ・Modified the default image display board of the sample program to ”Display output board”.
		9	・Modified name of image display board to “Display output board”. ・Modified the header file of the image display board to ”lcd_dvi_clk.h”.
1.10	May.17.19	5	Table 2.1 Peripheral device used (1/2) Remove compiler option "-mthumb-interwork"

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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