The University of Texas at Austin
Cockrell School of Engineering

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GROUP 2: LOW POWER TWO-STAGE OTA DESIGN

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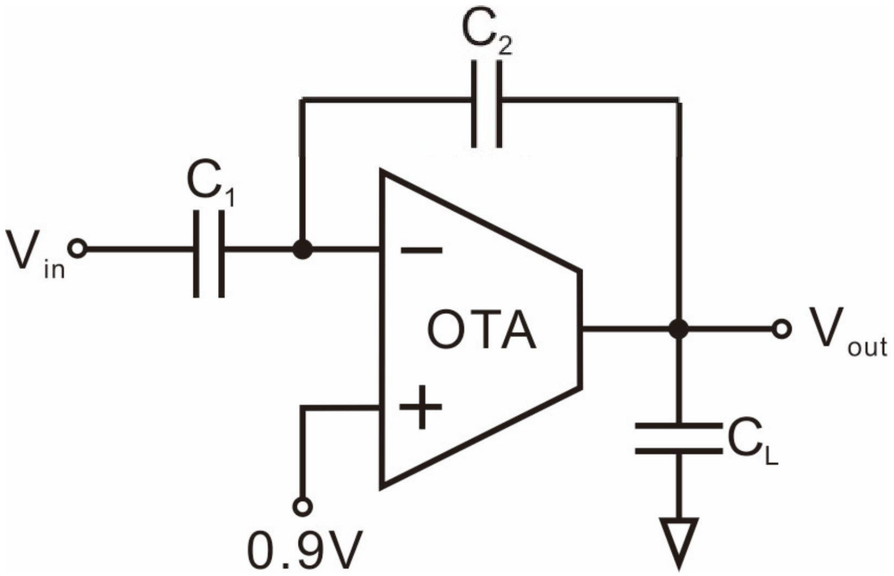
OTA Design Overview

		Requirements
Power supply		1.8 V
Minimum MOSFET channel length		0.18 um
Minimum MOSFET channel width		0.18 um
Static settling error		≤ 0.1%
Dynamic settling error		≤ 0.1%
Capacitive load		C_1=C_2, C_L≥1 pF
Output common mode voltage		0.9 V
Minimum output swing		[0.3, 1.5] V
Phase margin		> 60°
Settling time	Going up	< 45 ns
	Going down	< 45 ns
CMRR at DC		> 65 dB
PSRR at DC		> 65 dB
Current mirror ratios		≤ 10
Total output noise (RMS value)		≤ 300 uV
Total power consumption		**Minimize**

Target specifications



OTA for switched cap amplifier

1. Topology selection
2. Device & component sizing
3. Power optimization
4. Results

Presentation summary

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Topology Selection

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Target specifications

Gain requirements

$$\epsilon_0 = \left|\frac{1}{T_0}\right| = \left|\frac{1}{\beta A_v}\right| \Rightarrow A_v \geq 2500 = 68dB$$

$g_m r_o \cong 20\sim500$ for 180nm process

Need either cascode or two-stage for high gain $A_v \propto (g_m r_o)^2$

Output swing requirements

Folded cascode: $[2V_{ov},\ V_{DD}-2V_{ov}]$
Two-stage: $[V_{ov},\ V_{DD}-V_{ov}]$
$V_{ov} \cong 100\sim200mV$

Go with two-stage design

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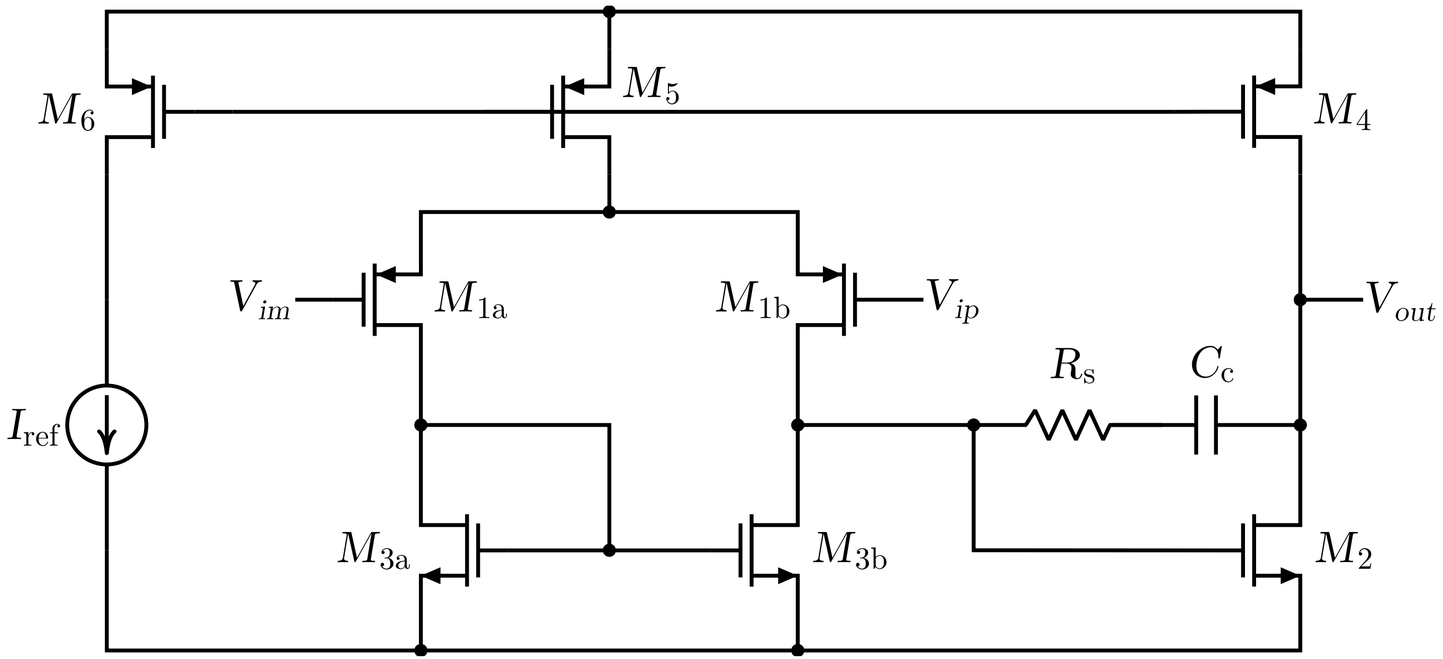
Select Gain Distribution



Two-stage OTA with PMOS input pair

$$A_{v,tot} = A_{v1}A_{v2} \geq 68\ dB$$

How do we select A_{v1} and A_{v2}?

Large A_{v1} is good for noise

But large A_{v1} requires large C_{gg1}

$\beta = \frac{C_f}{C_s+C_f+C_{gg1}}$ might get low

Settle with $A_{v1}: A_{v2} \cong 1:1$

$A_{v1} = A_{v2} = 34\ dB \cong 50$

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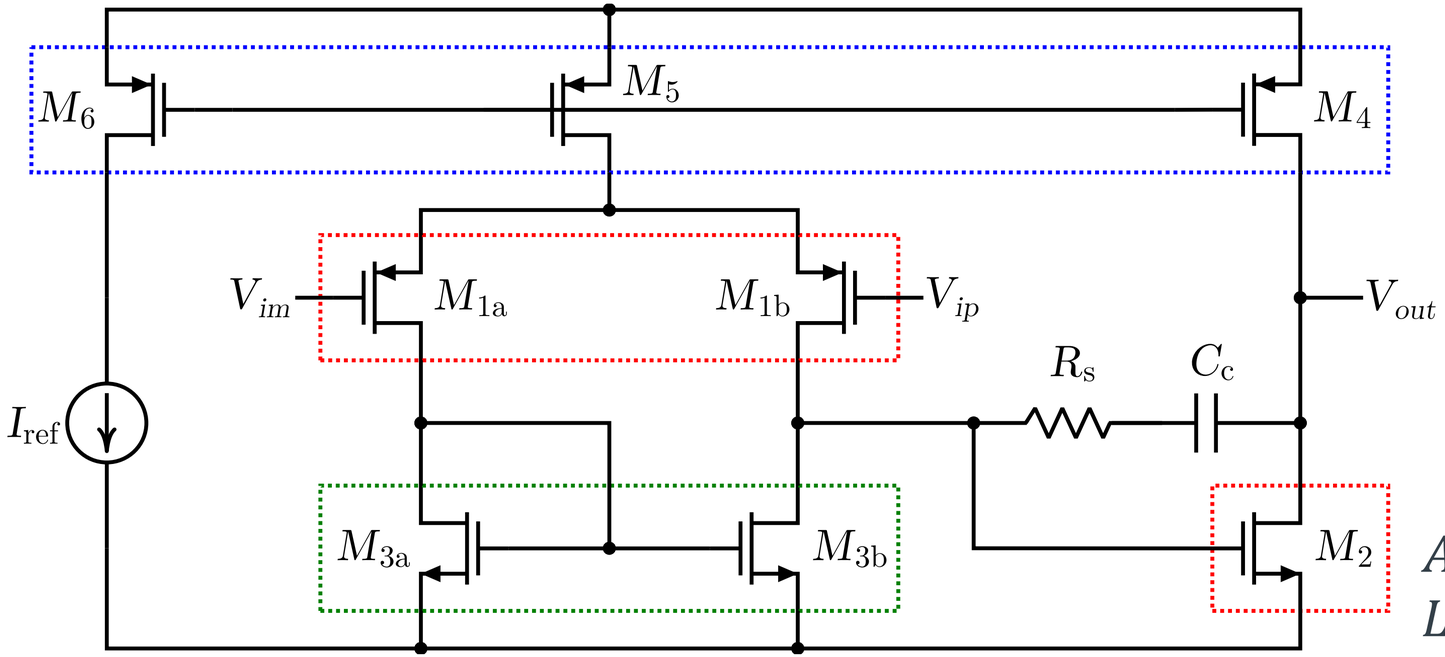
g_m/I_D Based Device Sizing



Two-stage OTA g_m/I_D selection

If we know g_m/I_D, A_v, and I_D, we can size all devices

- : Driver devices, high $g_m/I_D = 20\ S/A$
- : Current mirror, moderate $g_m/I_D = 10\sim15\ S/A$
- : Active load, (aim) moderate $g_m/I_D = 10\sim15\ S/A$

$A_v, g_m/I_D \Rightarrow g_m/g_{ds}\ plot \Rightarrow$ L obtained

$L, g_m/I_D, I_D \Rightarrow I_D/W\ plot \Rightarrow$ W obtained

How to select I_D?

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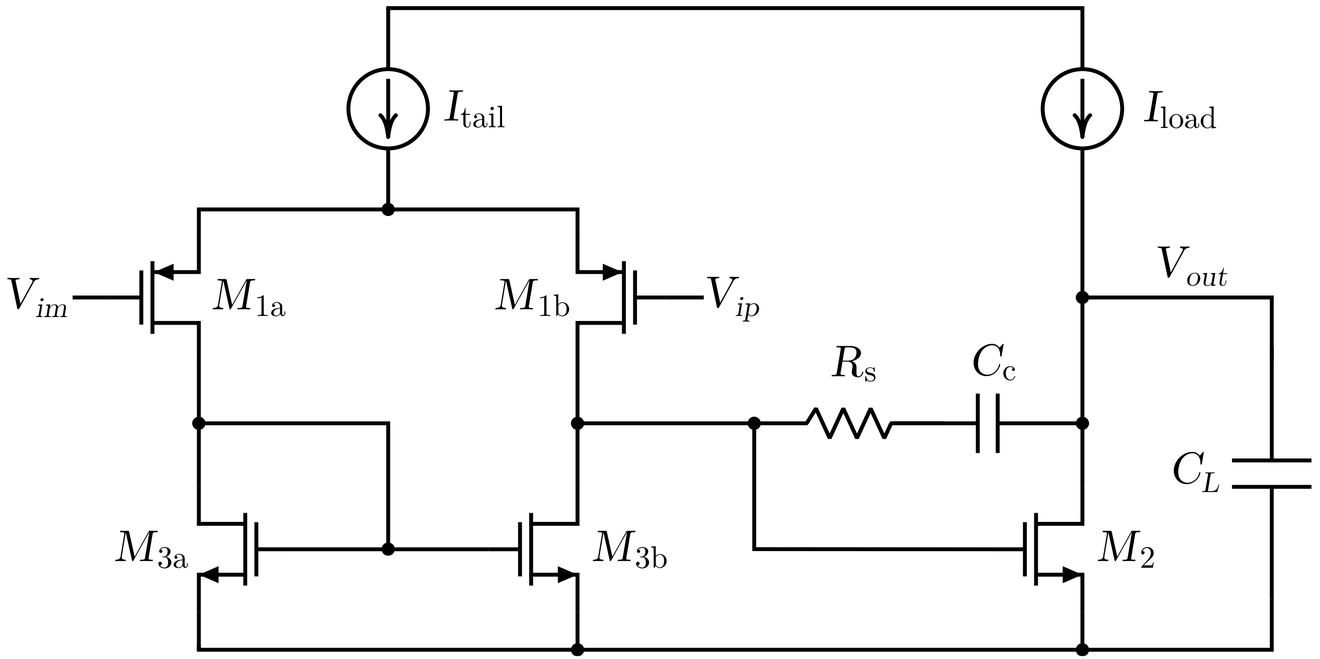
Current Budget for Speed



Two-stage OTA with current sources

V_{out} must settle from 0.9 to 1.5 V in $t_s \leq 45\ ns$

Assume 1/3 slew, 2/3 linear

$$\Rightarrow t_{slew} = 15\ ns \Rightarrow SR \geq 30\ V/\mu s$$

Slew rate requirement

$$SR_+ = \frac{I_{load} - I_{tail}}{C_L} \Rightarrow I_{load} \geq I_{tail} + 30\ \mu A$$

Bandwidth requirement

Assume $C_c \cong 0.5 C_L = 500\ fF$

$$\Rightarrow I_{tail} \geq \frac{-\ln(\epsilon_0)\, C_c}{10\ \beta\ t_{linear}} \cong 30\ \mu A$$

Set $I_{tail} = 30\ \mu A$, $I_{load} = 60\ \mu A$ to begin with

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Power Optimization

Stability requirement

$\omega_{p2,T} \geq 2.2 * \omega_{c,T}$ for phase margin

$$\Rightarrow \frac{g_{m2}}{C_L} \geq 2.2\frac{\beta g_{m1}}{C_c} \cong \frac{g_{m1}}{C_c}$$

$$\Rightarrow \frac{I_2}{C_L} \geq \frac{I_1}{C_c}, \qquad for\ \frac{g_{m1}}{I_{D1}} = \frac{g_{m2}}{I_{D2}} = 20$$

$$\Rightarrow \frac{I_{load}}{C_L} \geq 0.5\frac{I_{tail}}{C_c}$$

The ratio of I_{tail} and C_c determines speed and stability

I_{tail} can be decreased, if C_c also decreased (until noise limit)

Noise requirement

$$V_{n,out1}^2 \propto \frac{1}{C_C}\left(1 + \frac{g_{m3}}{g_{m1}}\right)$$

Output referred noise from stage 1

Power optimization process

1. For a given C_L, select I_{load}
2. Decrease I_{tail} and C_c as much as possible, until noise limit
3. Noise limit around $C_c = 200\sim300\ fF$
4. If specs met with wide margins, redesign with lower I_{load}

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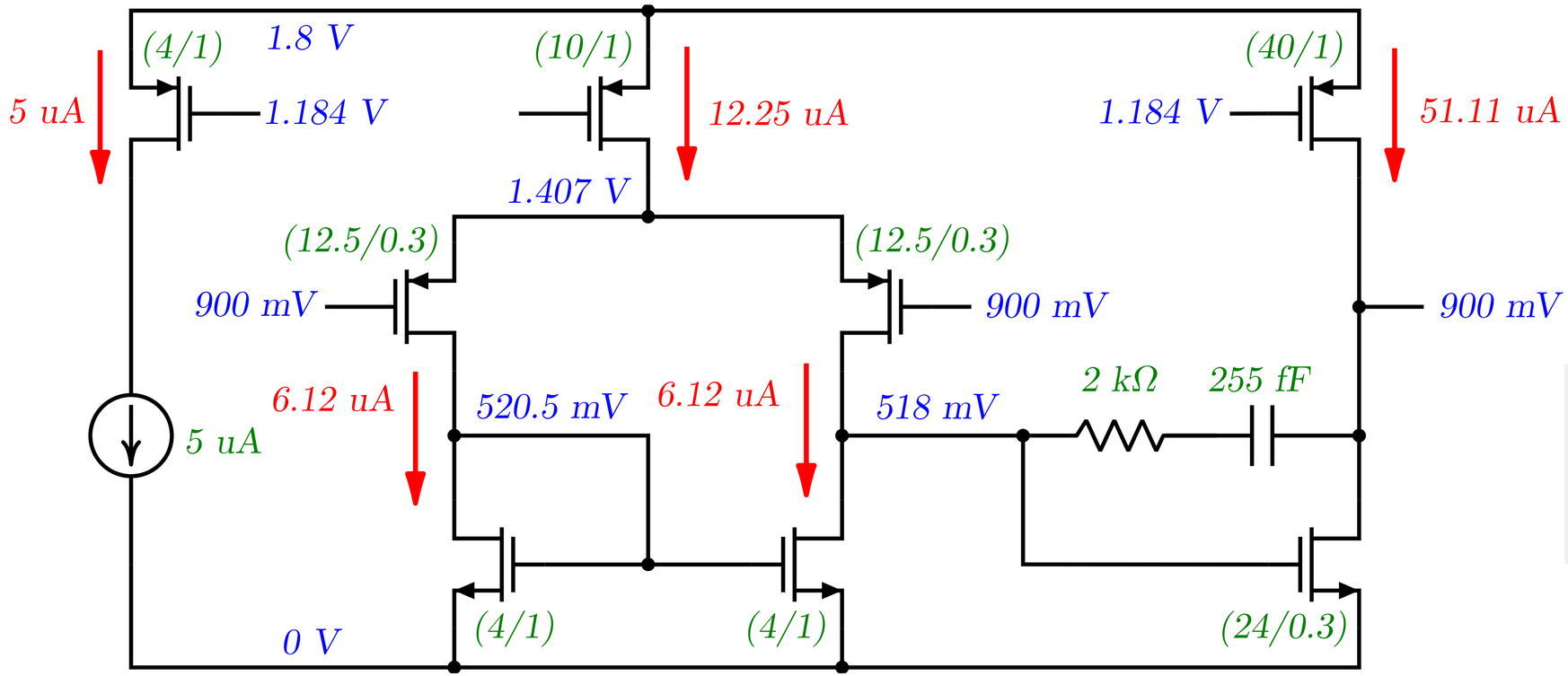
Finalized Design



Device sizing, bias voltage and current

signal	OP("/VO" "??")
i	-68.36u
pwr	-123.1u
v	1.8

OTA power consumption

$$P_{tot} = 123.1\,\mu W$$

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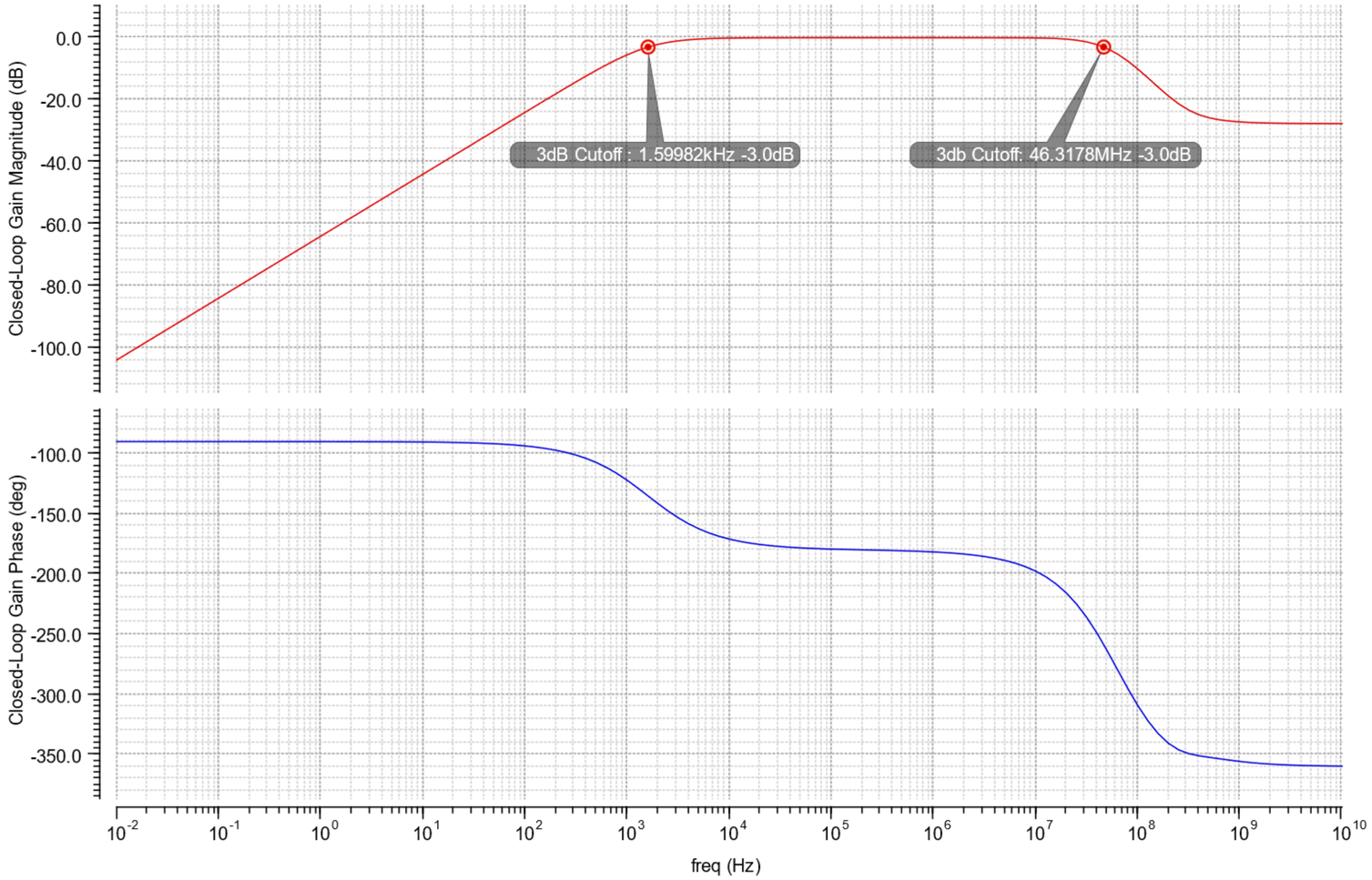
Closed-Loop Gain



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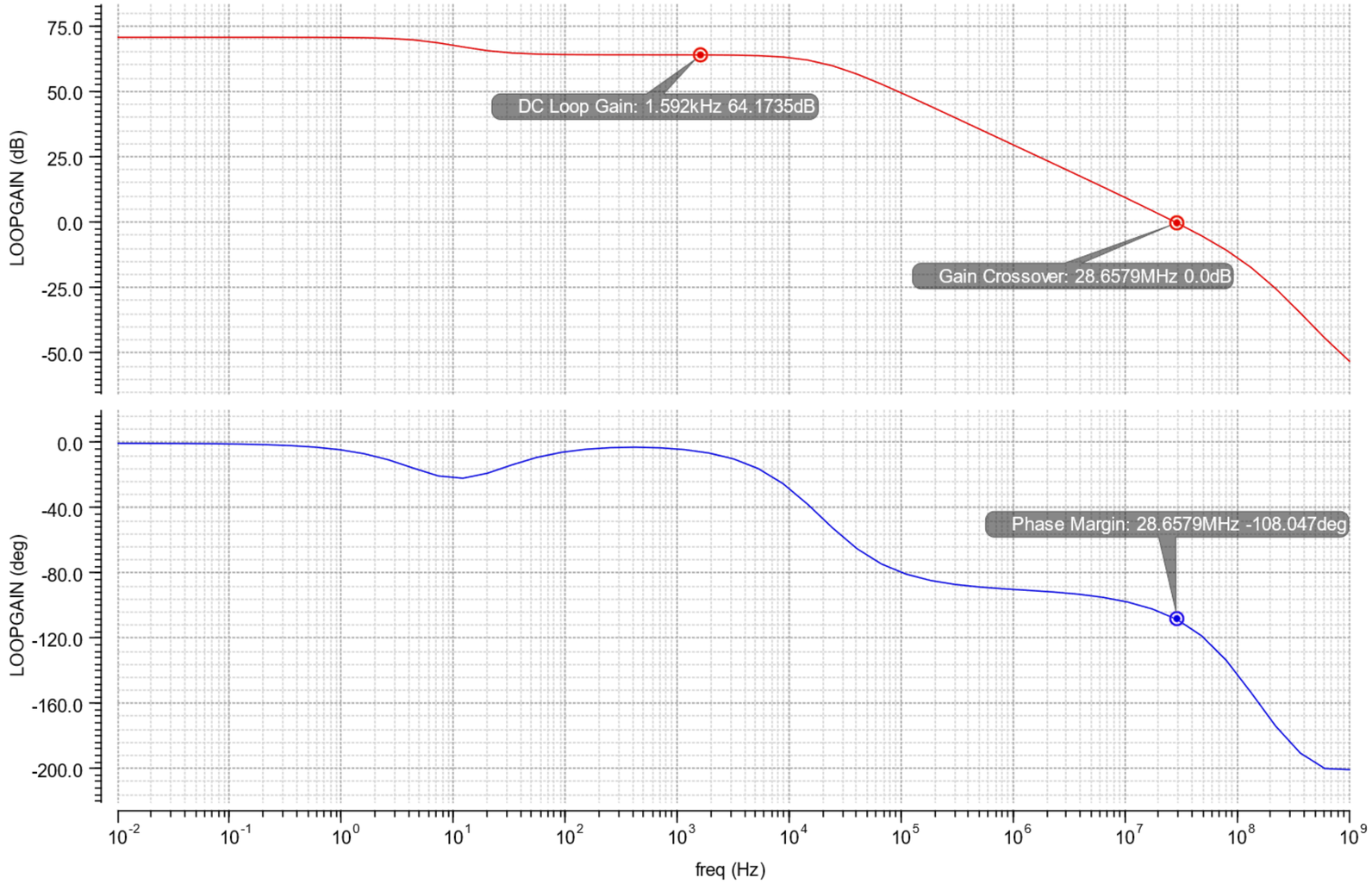
Loop Gain



$$PM = 180 + \phi = 72°$$

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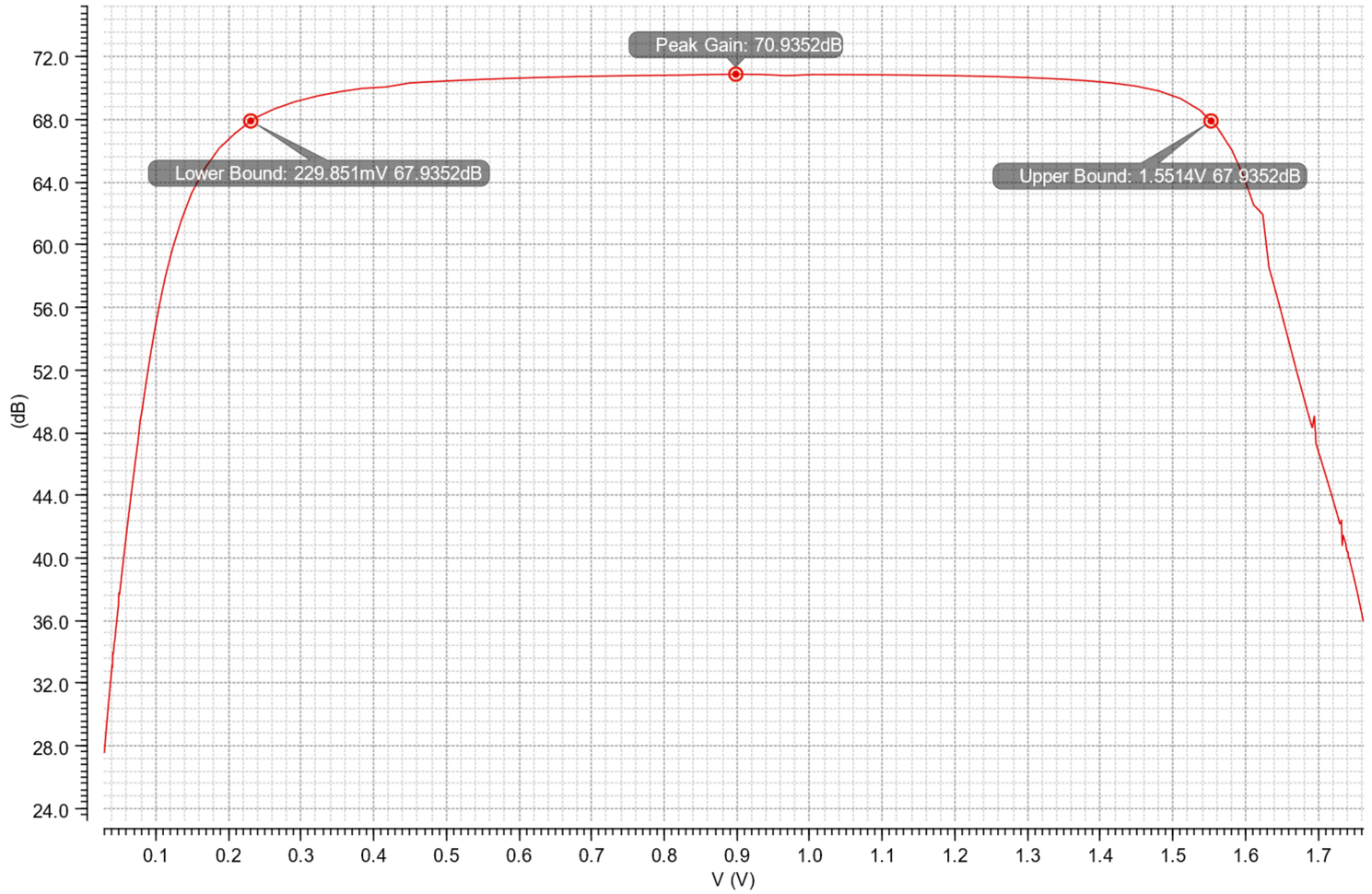
Output Swing



Output Swing: [0.23, 1.55] V

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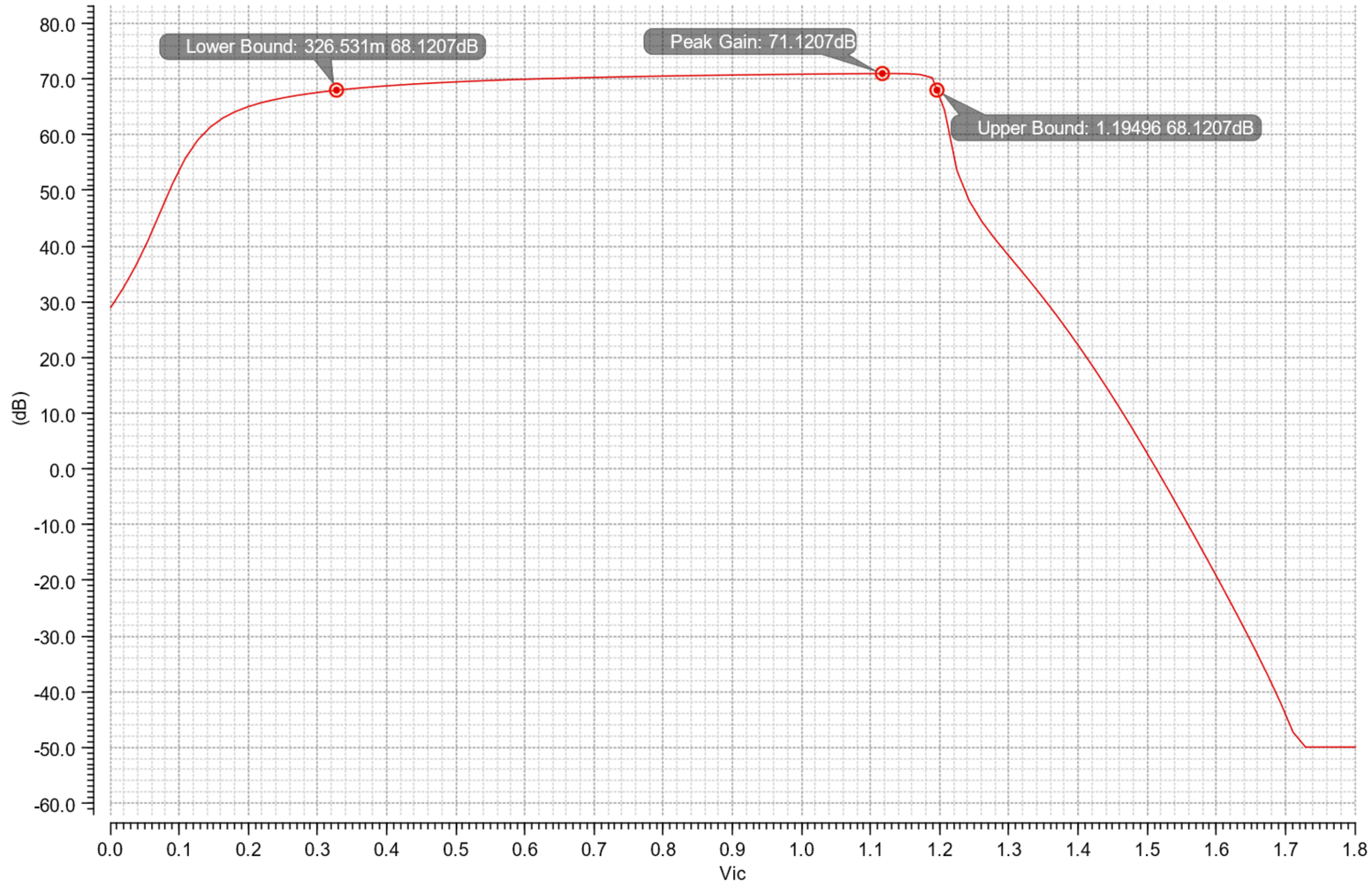
Input Common-Mode Range



ICMR: [0.33, 1.19] V

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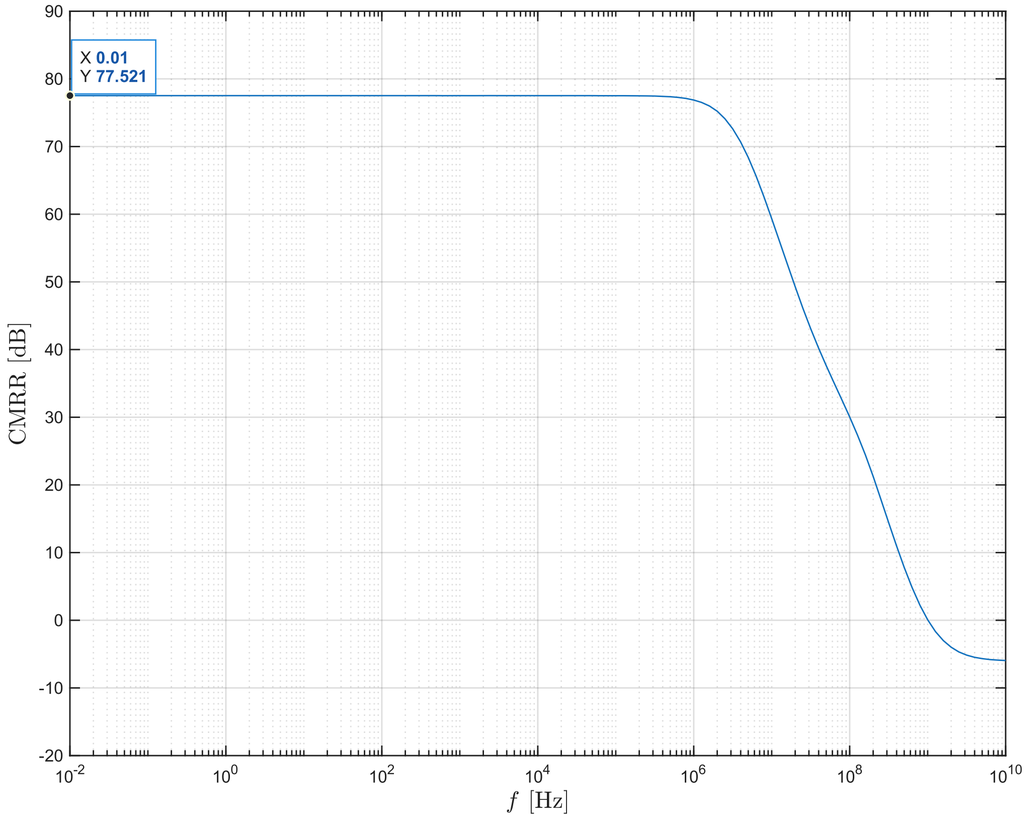
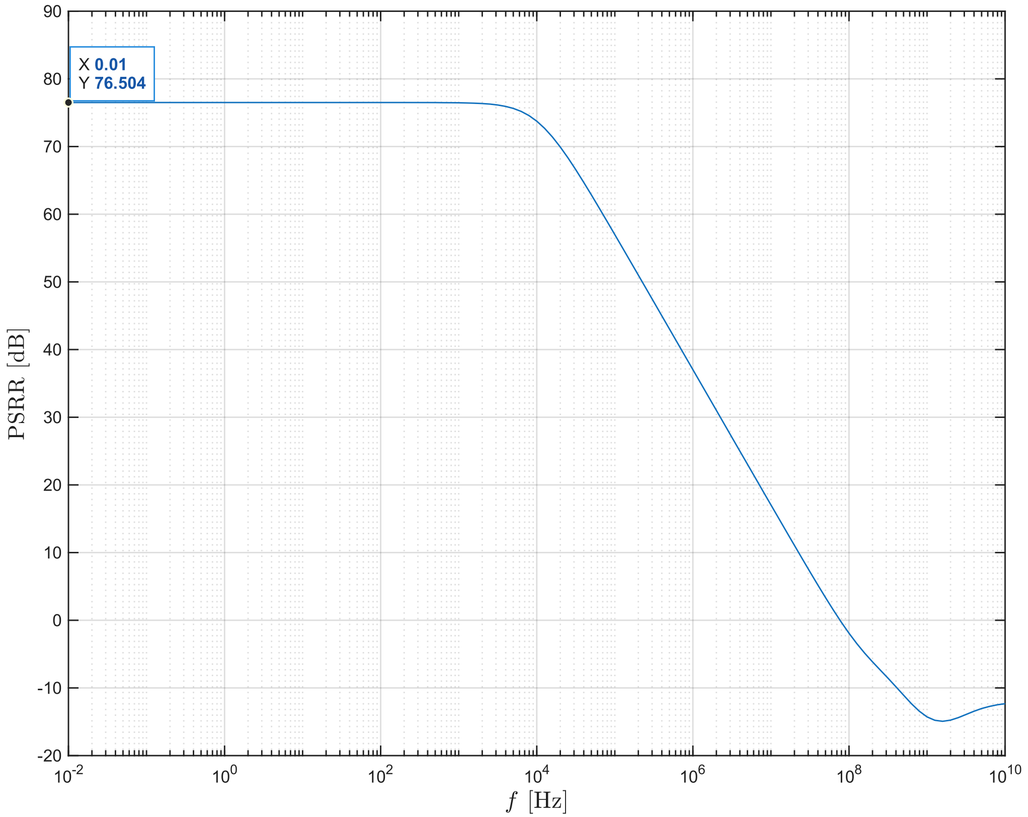
CMRR and PSRR



CMRR = 77.5 dB



PSRR = 76.5 dB

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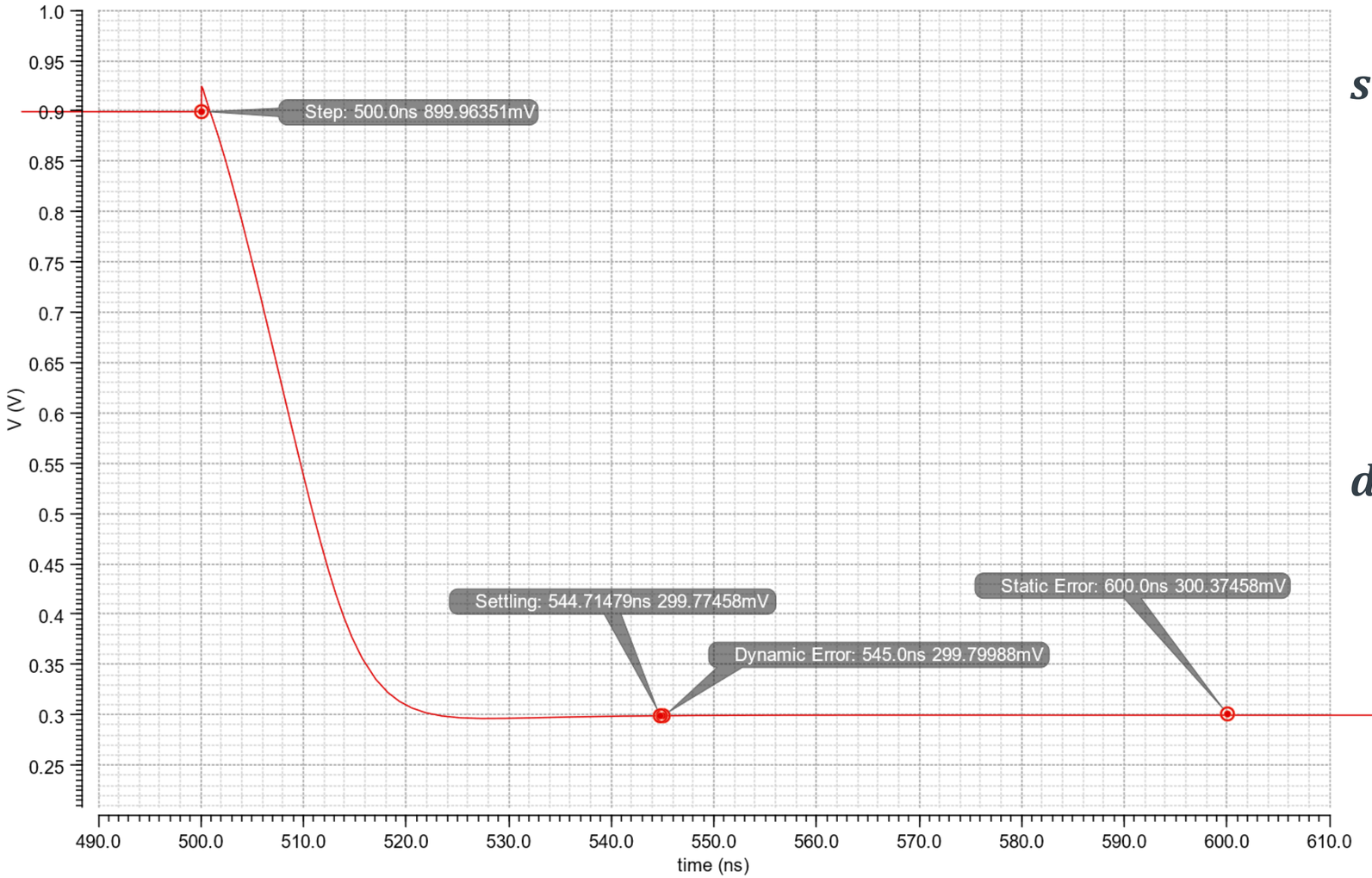
Settling Time (V_{in} Going Up, V_{out} Going Down)



V_{out} vs. t

$$\textbf{static } \epsilon_0 = \frac{|V_{ideal} - V_{stable}|}{|V_{ideal} - 0.9|}$$

$$= \frac{|300.374 - 300|}{|300 - 900|} = \mathbf{0.062\%}$$

$$\textbf{dynamic } \epsilon_0 = \frac{|V_{stable} - V_{out}|}{|V_{stable} - 0.9|}$$

$$= \frac{|300.37458 - 299.79888|}{|300.37458 - 900|}$$

$$= \mathbf{0.096\%}$$

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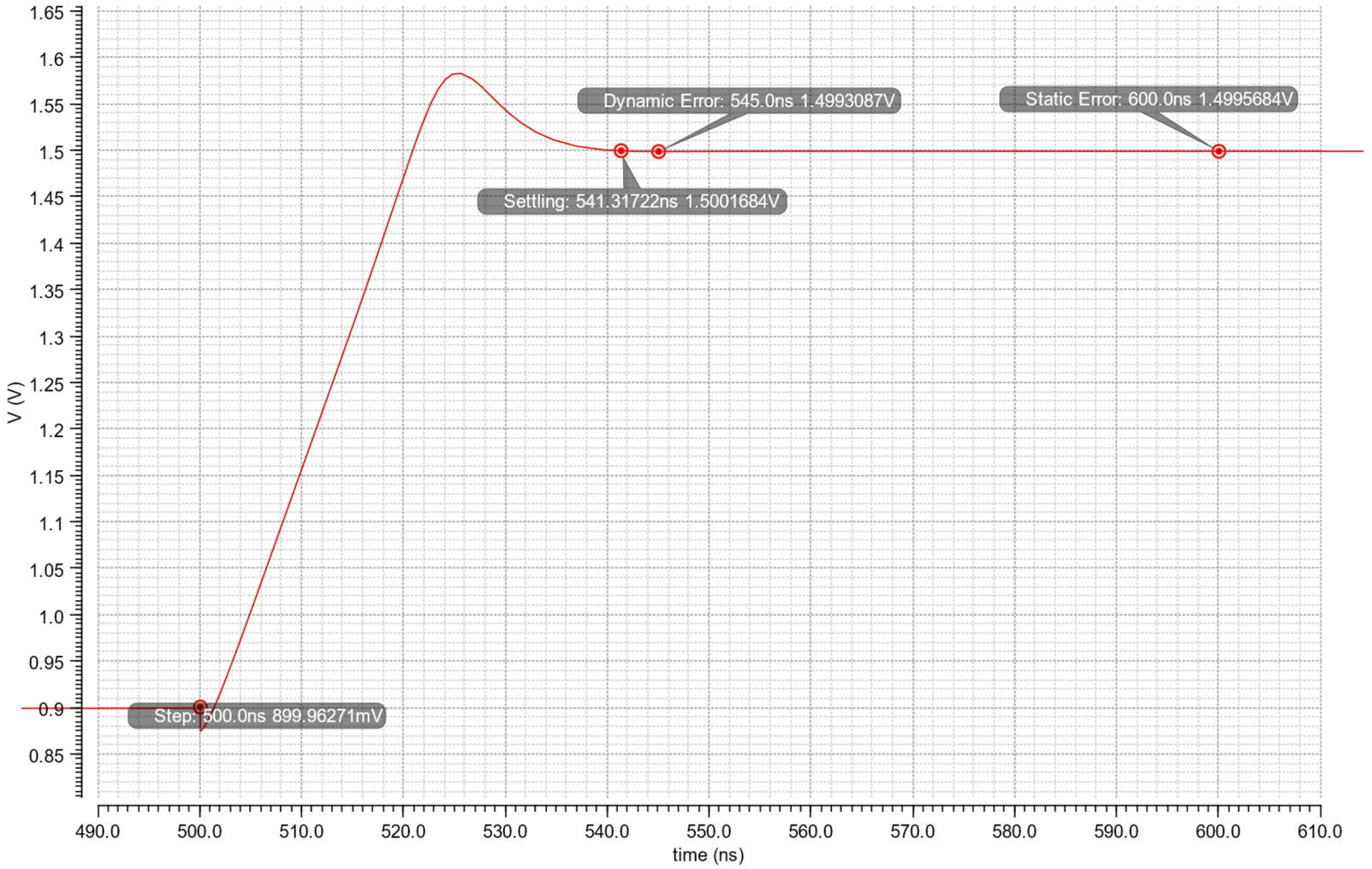
Settling Time (V_{in} Going Down, V_{out} Going Up)



V_{out} *vs. t*

$$\boldsymbol{static\ \epsilon_0} = \frac{|V_{ideal} - V_{stable}|}{|V_{ideal} - 0.9|}$$

$$= \frac{|1.5 - 1.4995684|}{|1.5 - 0.9|} = \mathbf{0.072\%}$$

$$\boldsymbol{dynamic\ \epsilon_0} = \frac{|V_{stable} - V_{out}|}{|V_{stable} - 0.9|}$$

$$= \frac{|1.4995684 - 1.4993087|}{|1.4995684 - 0.9|}$$

$$= \mathbf{0.043\%}$$

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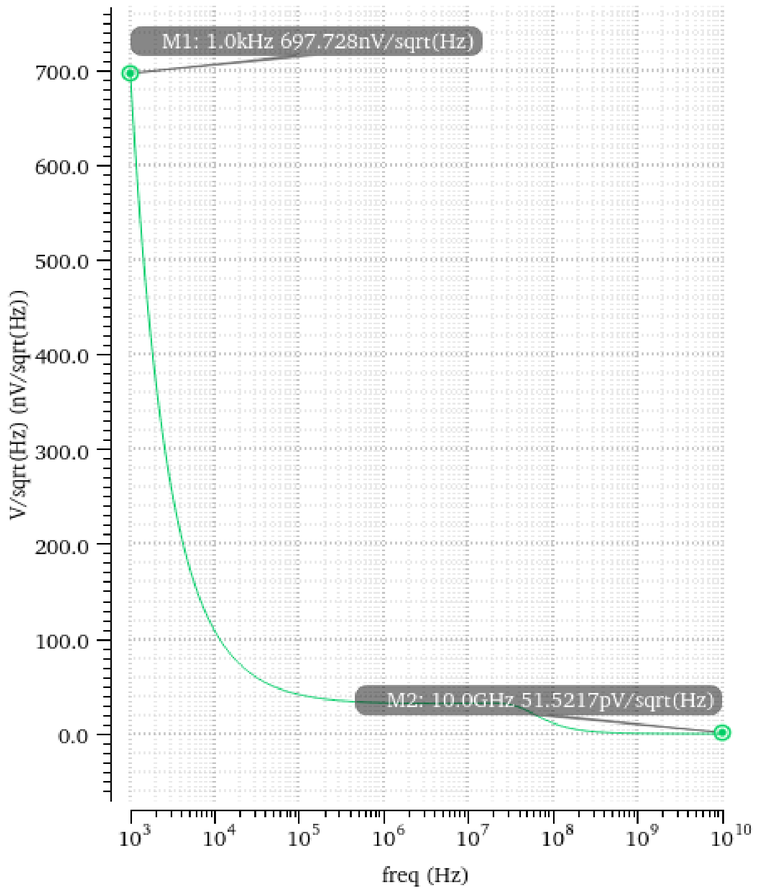
Noise Spectrum and Summary

Noise Response

Name | Vis

output noise; V / sqrt(Hz)



Device	Param	Noise Contribution	% Of Total
/I3/M1a	id	2.37755e-08	26.64
/I3/M3b	id	1.90028e-08	21.29
/I3/M1b	id	1.81885e-08	20.38
/I3/M3a	id	1.59356e-08	17.86
/I3/R0	rn	5.08004e-09	5.69
/I3/M2	id	3.40346e-09	3.81
/I3/M4	id	1.48423e-09	1.66
/I3/M6	id	7.10122e-10	0.80
/I3/M5	id	5.33665e-10	0.60
/I3/M1a	fn	4.68757e-10	0.53

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 8.92379e-08
No input referred noise available
The above noise summary info is for noise data

$$V_{n,\,out} = \sqrt{8.92379 \times 10^{-8}} = \mathbf{299\ \mu V}$$

Result Summary

		Specs	Our Result
Values for C_1, C_2, and C_L			C_1=C_2=100 fF, C_L = 1pF
Static settling error		≤ 0.1%	0.062% (0.3 V), 0.072% (1.5 V)
Dynamic settling error		≤ 0.1%	0.096% (0.3 V), 0.043% (1.5 V)
Output swing		[0.3, 1.5]	[0.23, 1.55]
Input common-mode range			[0.33, 1.19]
OTA open-loop DC small-signal gain (A_{dm})			70.9 dB
Loop gain at low-frequency ($\beta*A_{dm}$)			64.2 dB
Loop gain unity gain frequency			29 MHz
Loop gain phase margin		> 60°	72°
Settling time	Up	< 45 ns	44.7 ns
	Down	< 45 ns	41.3 ns
CMRR at DC		> 65 dB	77.5 dB
PSRR at DC		> 65 dB	76.5 dB
Total output noise (RMS value)		≤ 300 uV	299 uV
Power consumption			**123.1 uW**

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Q&A

THANK YOU.

- Hieu Nguyen
- Yoon Sheen
- BaoTong Shi

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