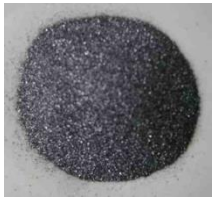
Design and Implementation of VLSI Systems
Lecture02

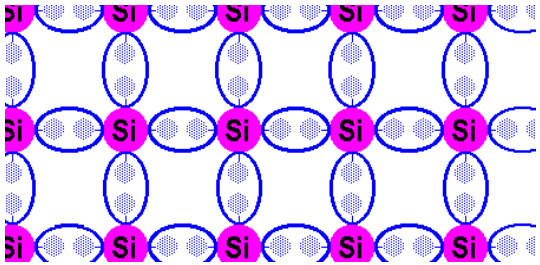
CMOS logic

Impact of doping on silicon resistivity

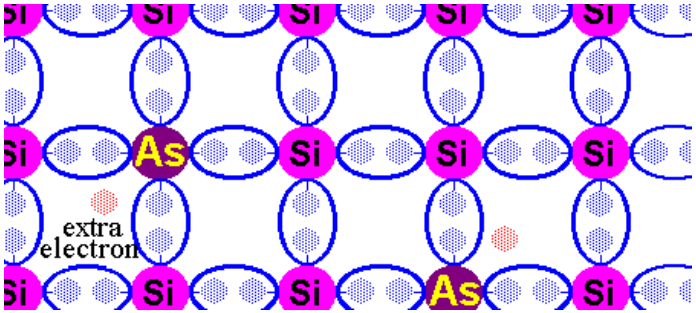


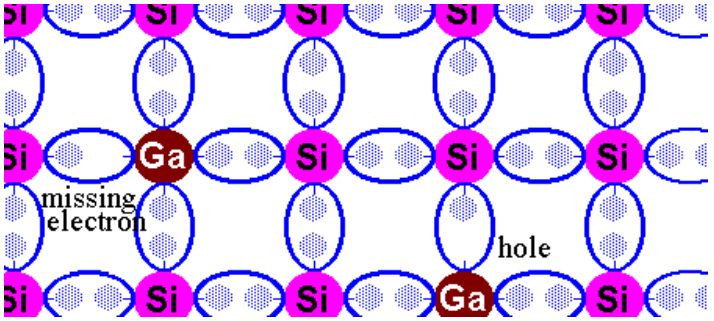
silicon
4.995×10^{22} atoms in cm^3
Resistivity $3.2 \times 10^5\ \Omega cm$

dope with phosphorous or arsenic → n-type



dope with boron → p-type





1 atom in billion ⇒
1 atom in million ⇒
1 atom in thousand ⇒

1 atom in billion ⇒
1 atom in million ⇒
1 atom in thousand ⇒

⇒ Electrons are more mobile/faster than holes

What happens if we sandwich p & n types?

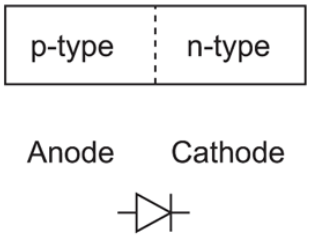
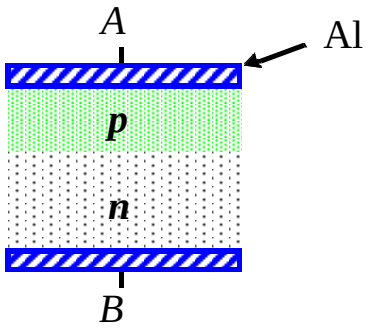
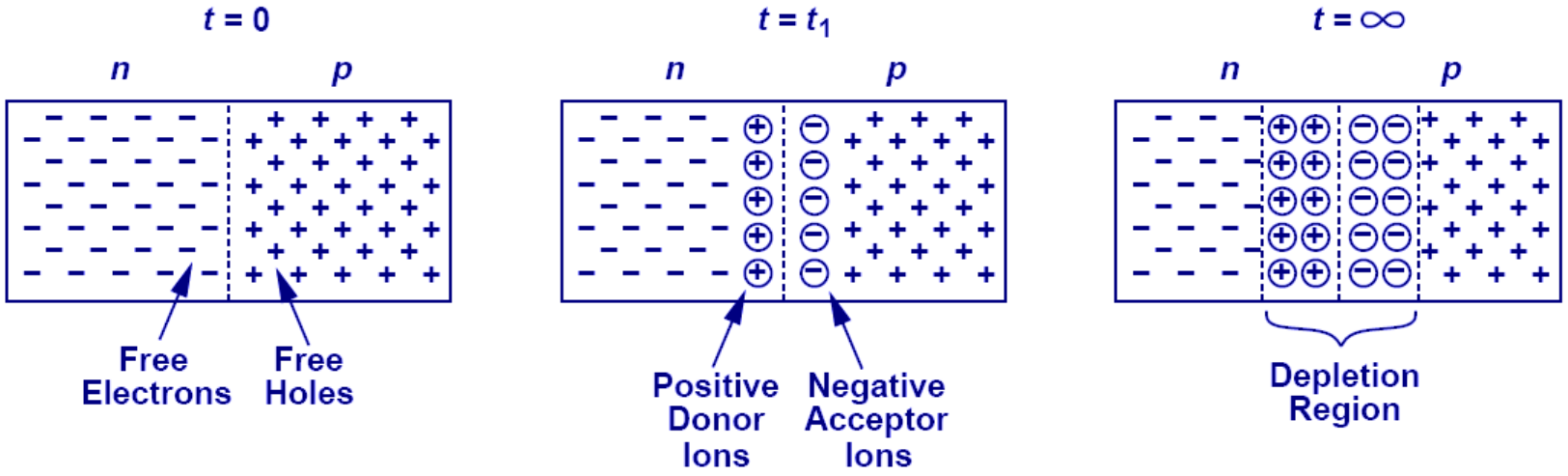


FIG 1.7 p-n junction diode structure and symbol

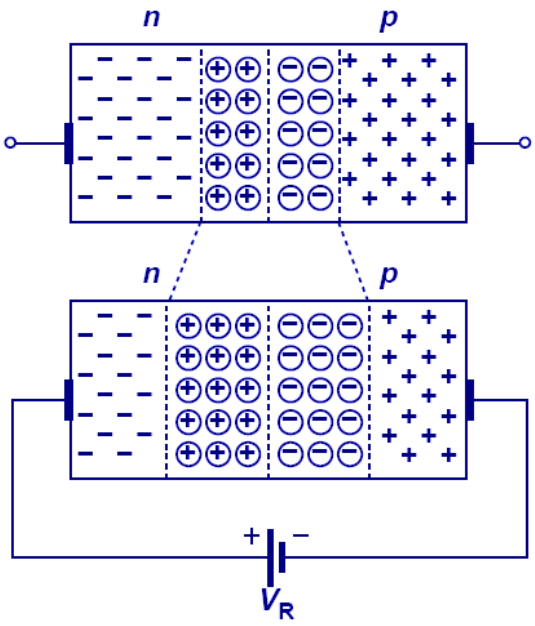


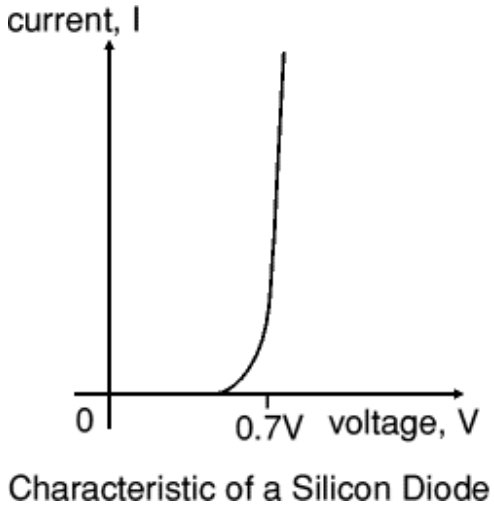
One-dimensional representation



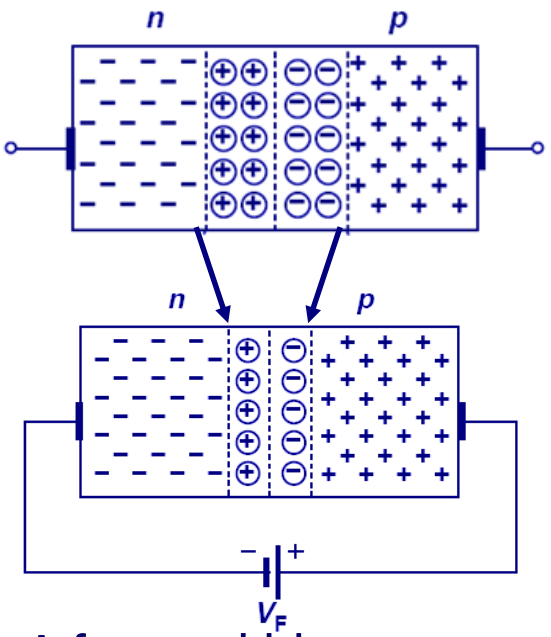
- In equilibrium, the drift and diffusion components of current are balanced; therefore the net current flowing across the junction is zero.

PN-junction regions of operation





Characteristic of a Silicon Diode



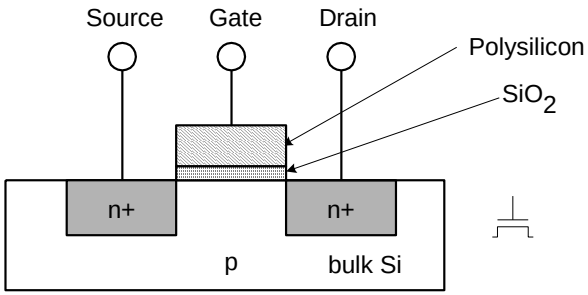
In reverse bias, the width of the depletion region increases. The diode acts as voltage-controlled capacitor.

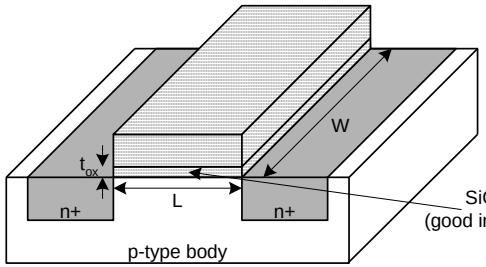
A forward bias decreases the potential drop across the junction. As a result, the magnitude of the electric field decreases and the width of the depletion region narrows.

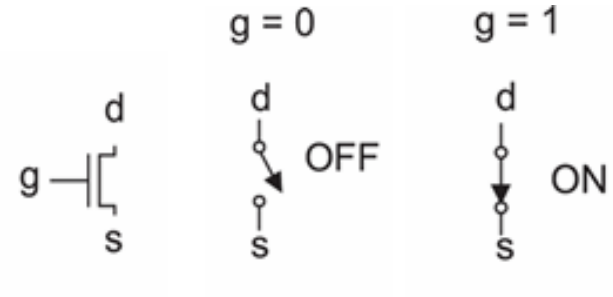
nMOS and pMOS transistors

Each transistor consists of a stack of a conducting gate, an insulating layer of silicon dioxide and a semiconductor substrate (body or bulk)

nMOS transistor

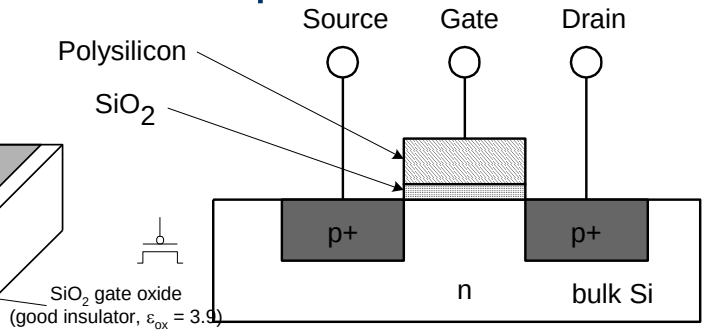


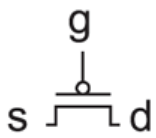


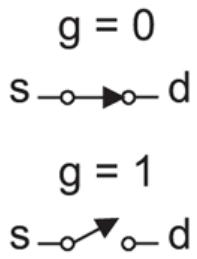


Body is typically grounded

pMOS transistor

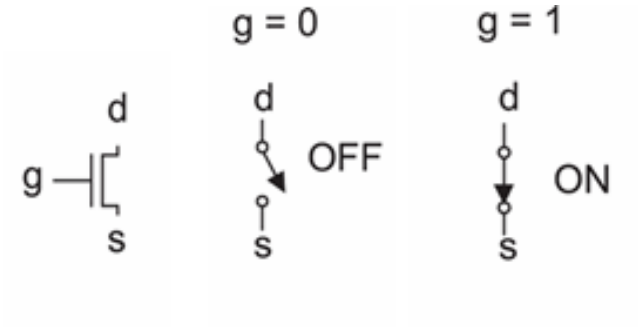


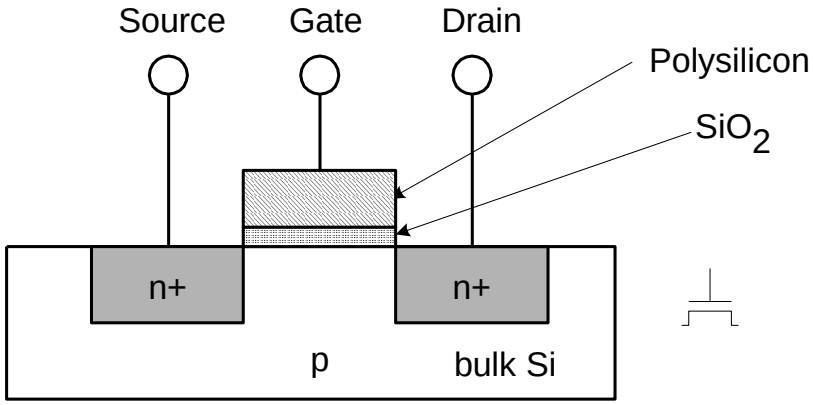




Body is typically at supply voltage

nMOS transistor



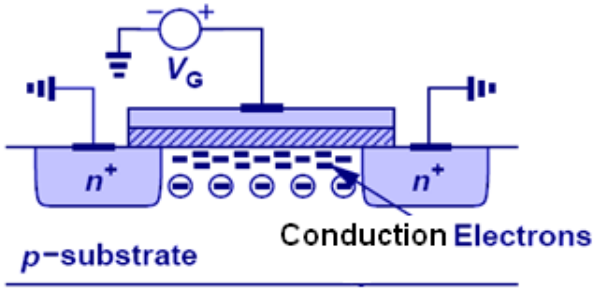


g=0: When the gate is at a low voltage ($V_{GS} < V_{TN}$):

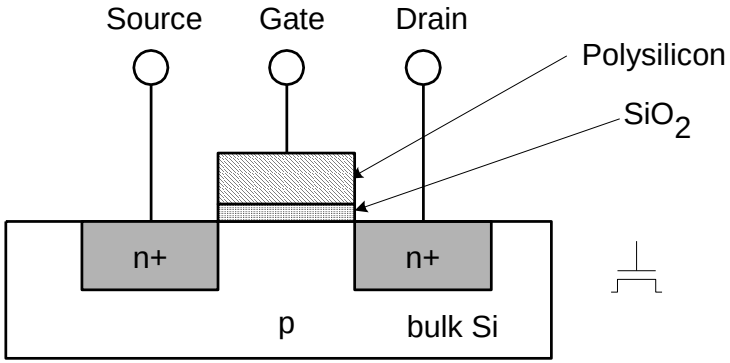
- p-type body is at low voltage
- source and drain-junctions diodes are OFF
- transistor is OFF, no current flows

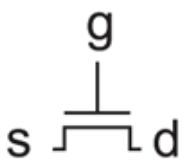
g=1: When the gate is at a high voltage ($V_{GS} \geq V_{TN}$):

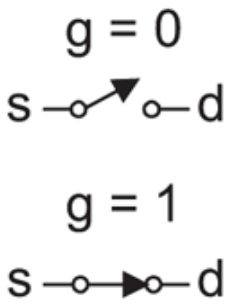
- negative charge attracted to body
- inverts a channel under gate to n-type
- transistor ON, current flows, transistor can be viewed as a resistor

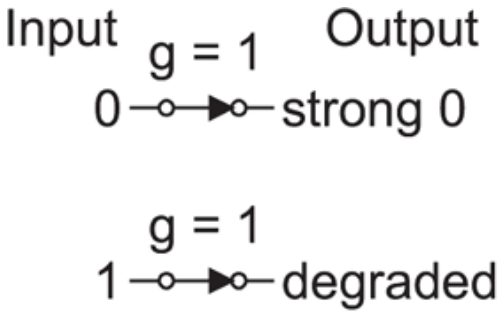


nMOS pass ‘0’ more strongly than ‘1’

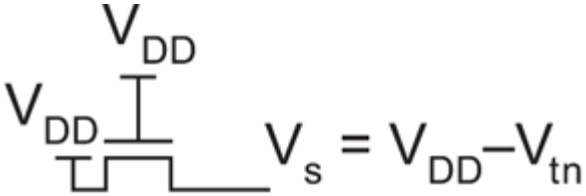




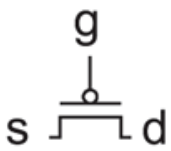


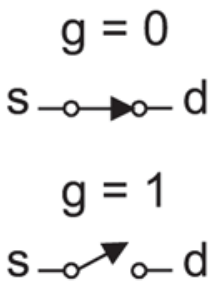


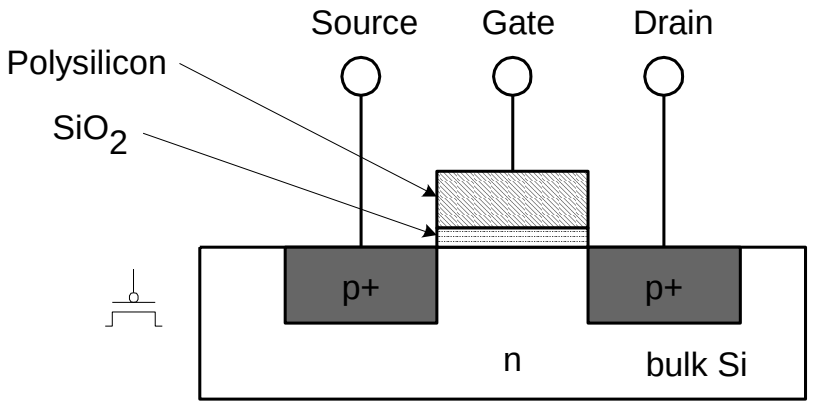
- Why does ‘1’ pass degraded?



pMOS transistor







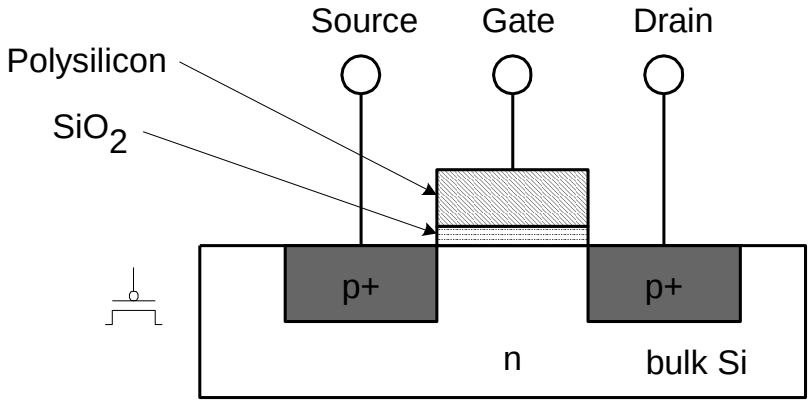
g=0: When the gate is at a low voltage ($V_{GS} < V_{TP}$):

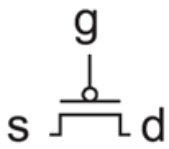
- positive charge attracted to body
- inverts a channel under gate to p-type
- transistor ON, current flows

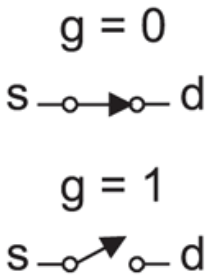
g=1: When the gate is at a high voltage ($V_{GS} \geq V_{TP}$):

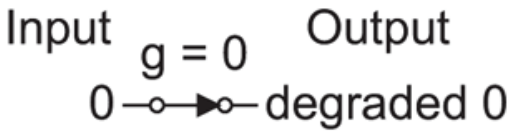
- negative charge attracted to body
- source and drain junctions are OFF
- transistor OFF, no current flows

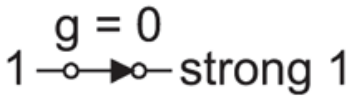
pMOS pass ‘1’ more strongly than ‘0’

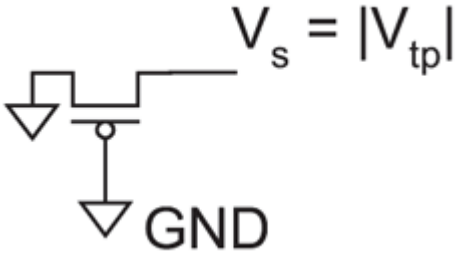






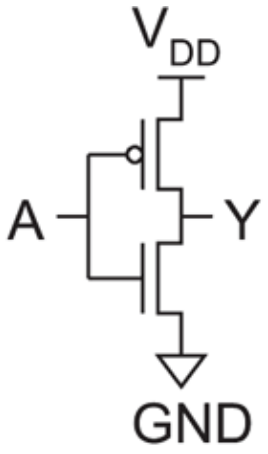




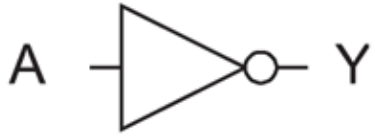


- Why does ‘0’ pass degraded?

An nMOS and pMOS make up an inverter



(a)



(b)

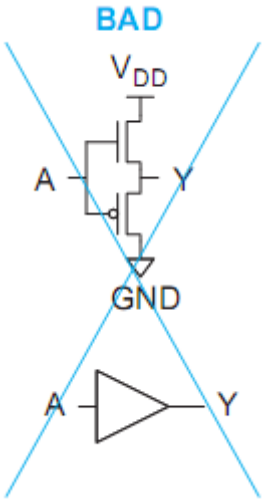
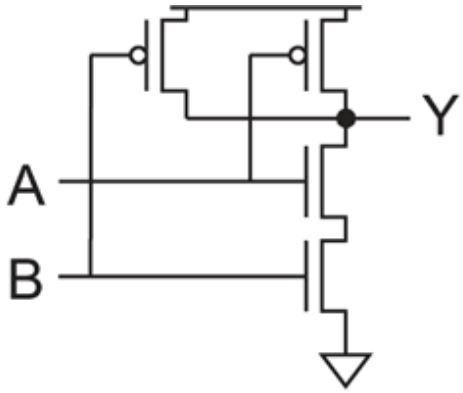


FIG 1.10 Inverter schematic (a) and symbol (b) $Y = \overline{A}$

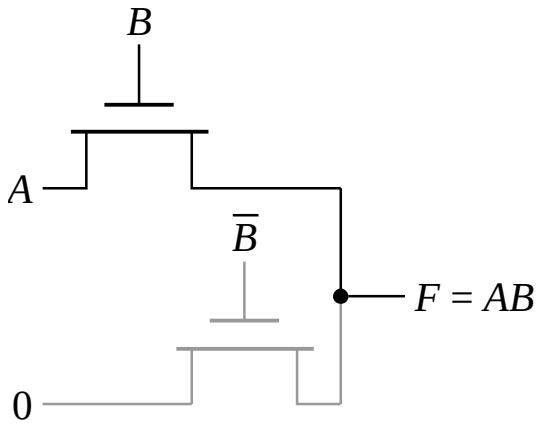
pMOS + nMOS = CMOS

More CMOS gates



What is this gate function?

$$Y = \overline{A \bullet B}$$



What's wrong about this design?

3-input NANDs

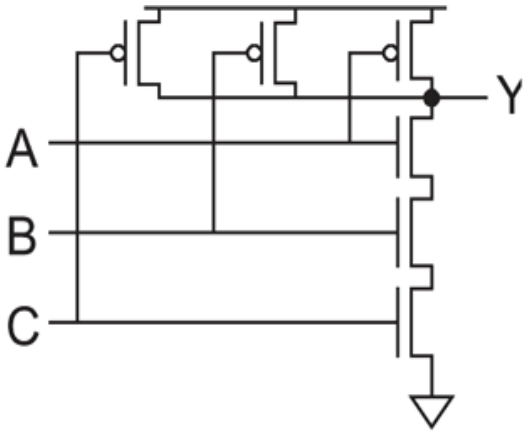


FIG 1.12 3-input NAND gate schematic

$Y = \overline{A \bullet B \bullet C}$

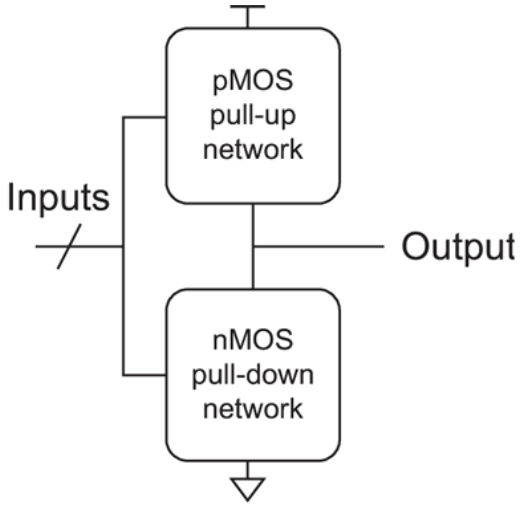


FIG 1.13 General logic gate using pull-up and pull-down networks

If: Pull up network = 1 => pull down network must = 0
If: Pull up network = 0 => pull down network must = 1

3-input NANDs

What are the advantages of CMOS circuit style?

Series-Parallel Combinations

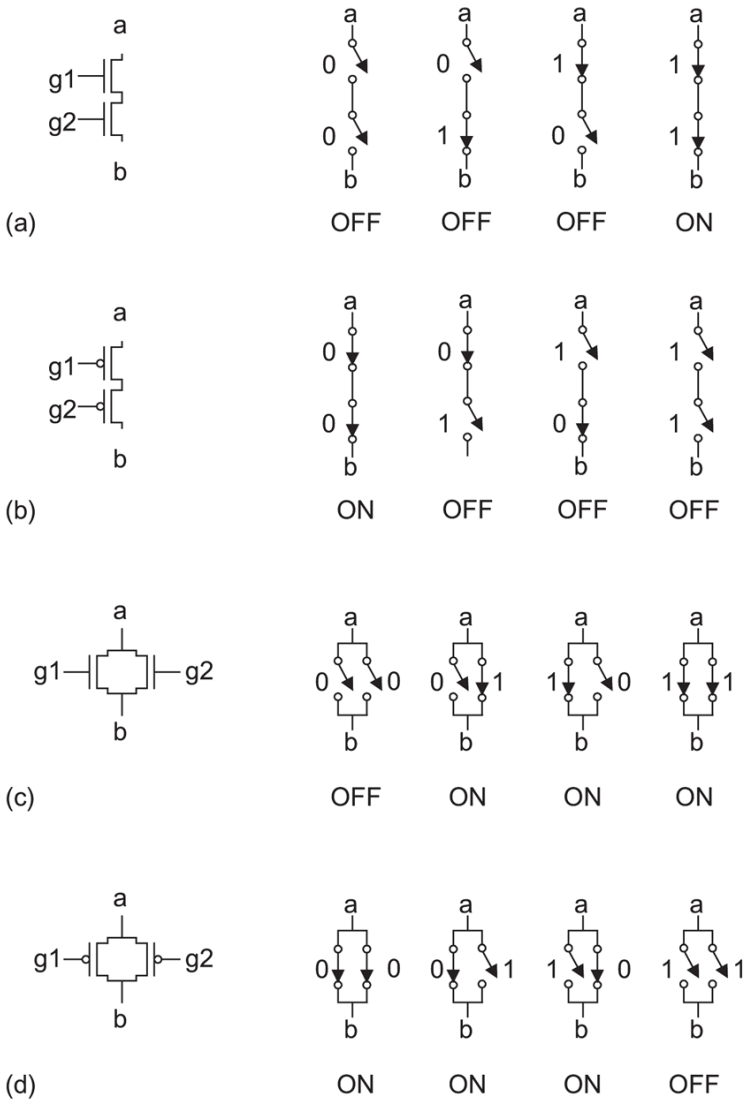
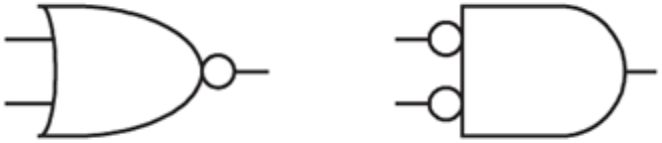
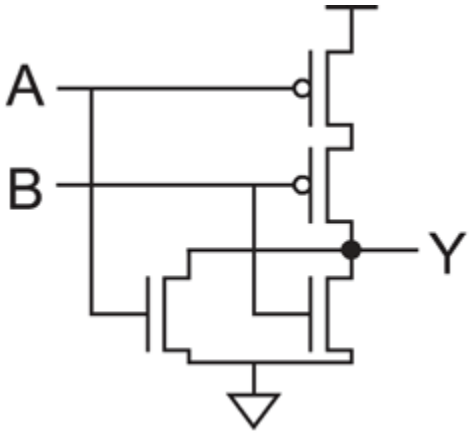


FIG 1.14 Connection and behavior of series and parallel transistors

What are the transistor schematics of the NOR gate?





And-Or-Inverter (AOI) gate

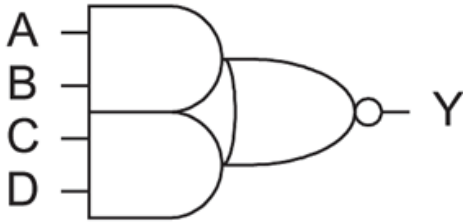
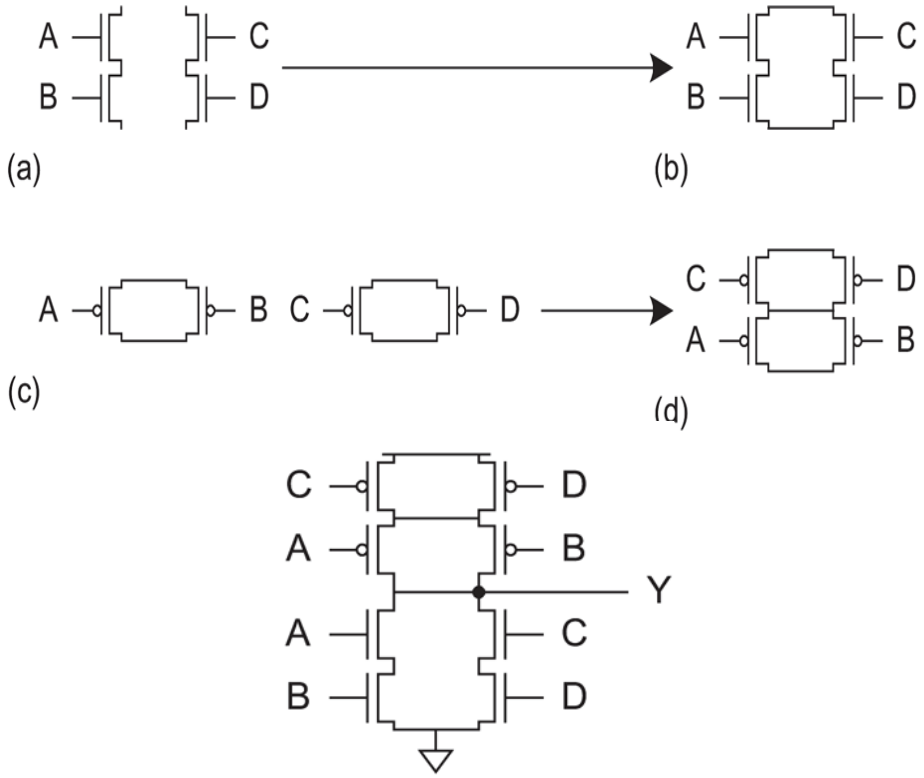


FIG 1.17 CMOS compound gate for function $Y = \overline{(A \bullet B) + (C \bullet D)}$



CMOS gate design steps

Steps:

- -Design pull down network
  - -Use the inverse of the given function
  - -NMOS circuit
- -Design pull up network
  - -Use the opposite network of the pull down network: parallel - serial; serial – parallel
  - -PMOS circuit
- -Combine 2 networks

Examples

Example 1.2

Sketch a static CMOS gate computing $Y = \overline{(A + B + C) \cdot D}$

Transmission gate

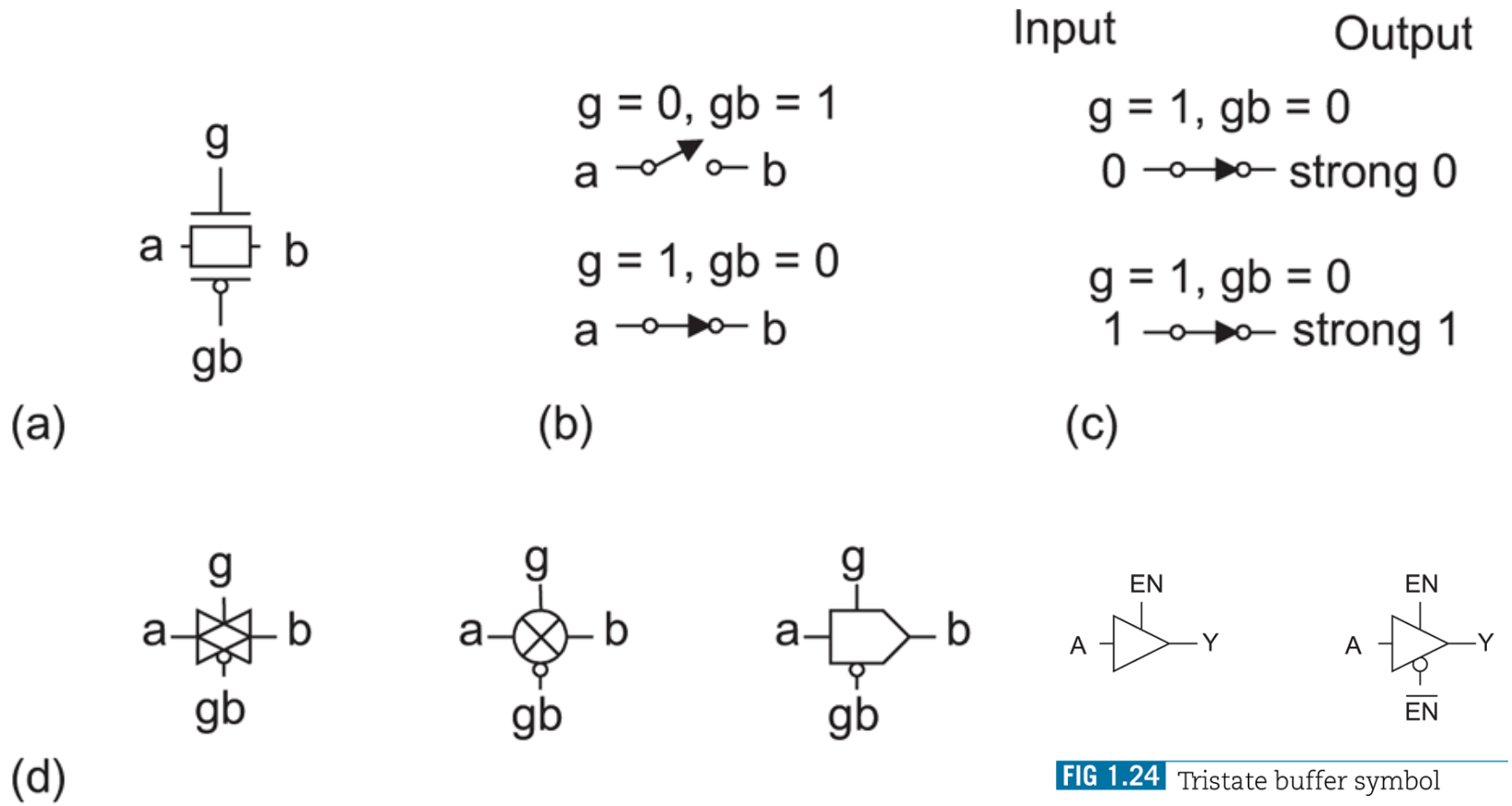


FIG 1.24 Tristate buffer symbol

FIG 1.20 Transmission gate

Tri-state inverter

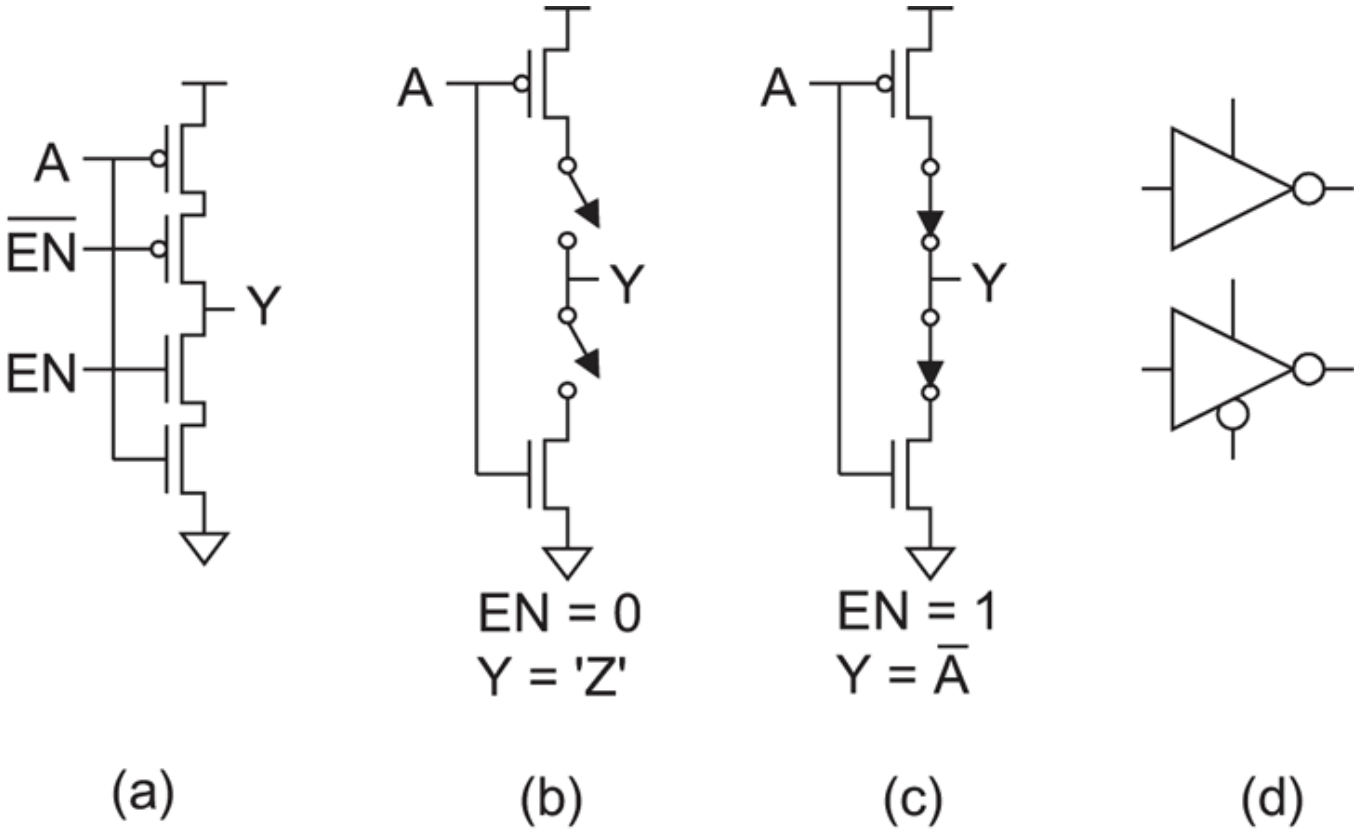


FIG 1.26 Tristate inverter

Multiplexer (MUX)

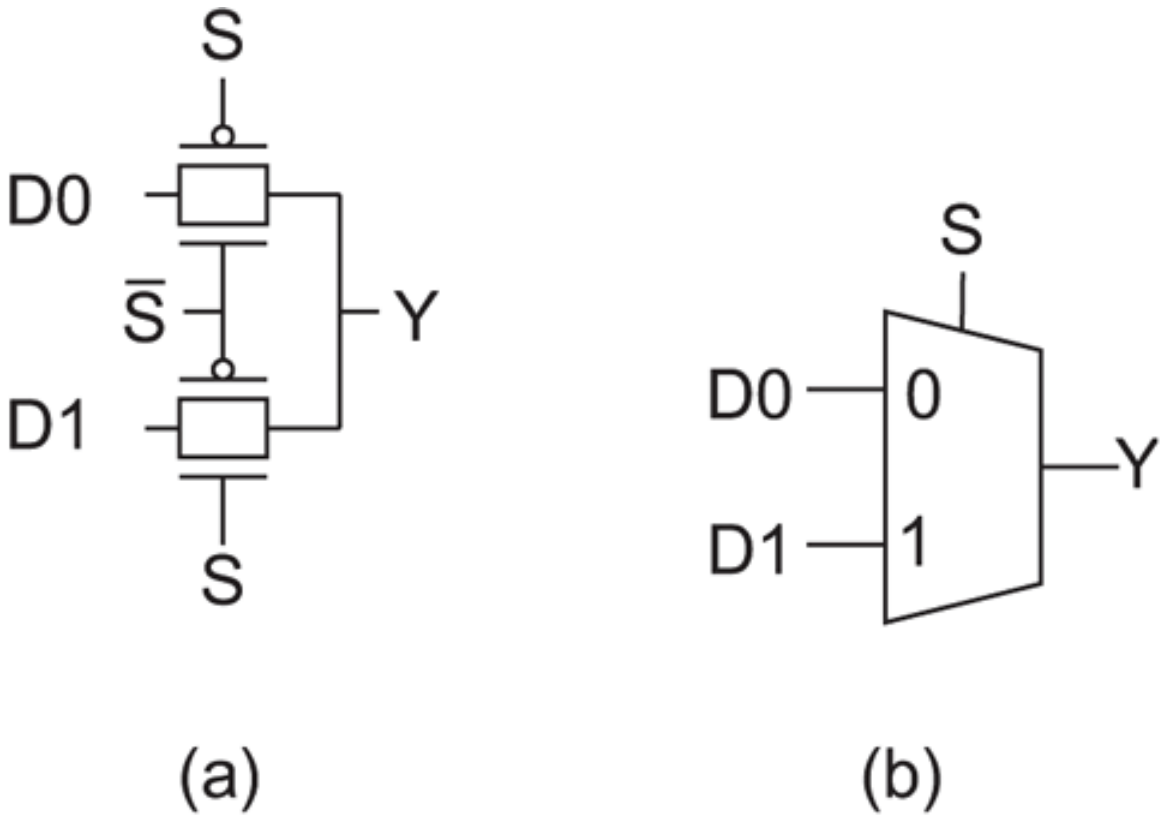


FIG 1.27 Transmission gate multiplexer

Latch design

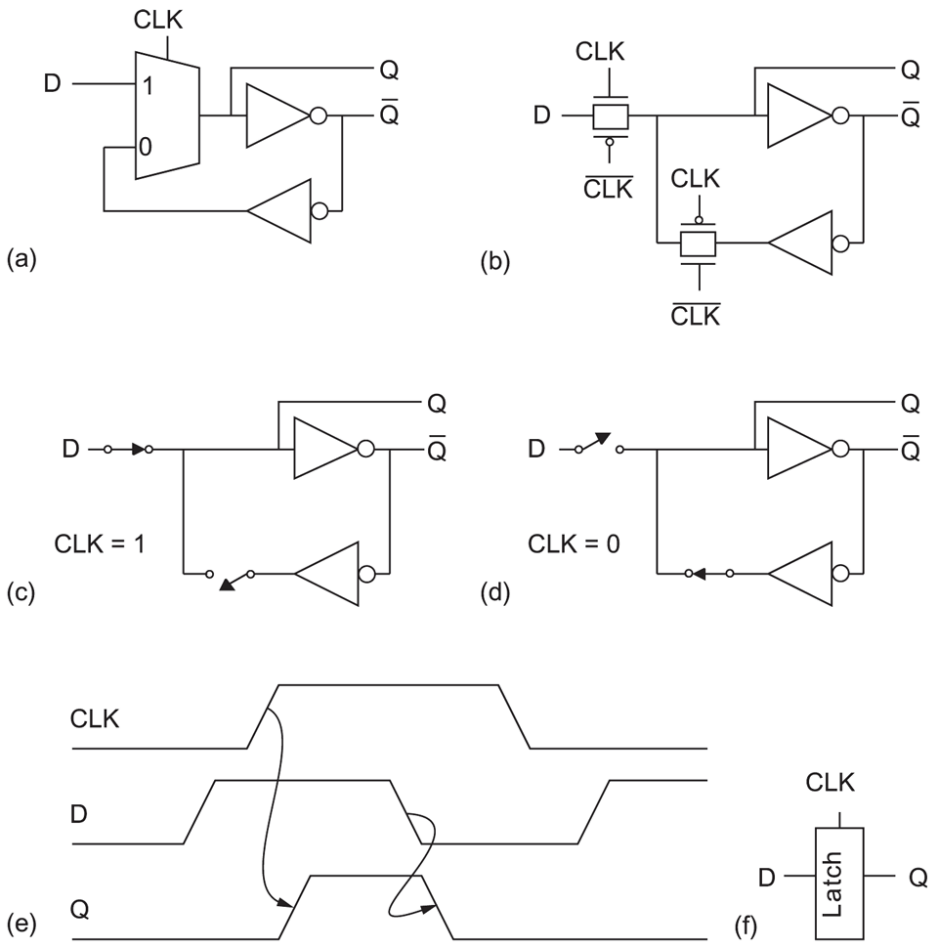
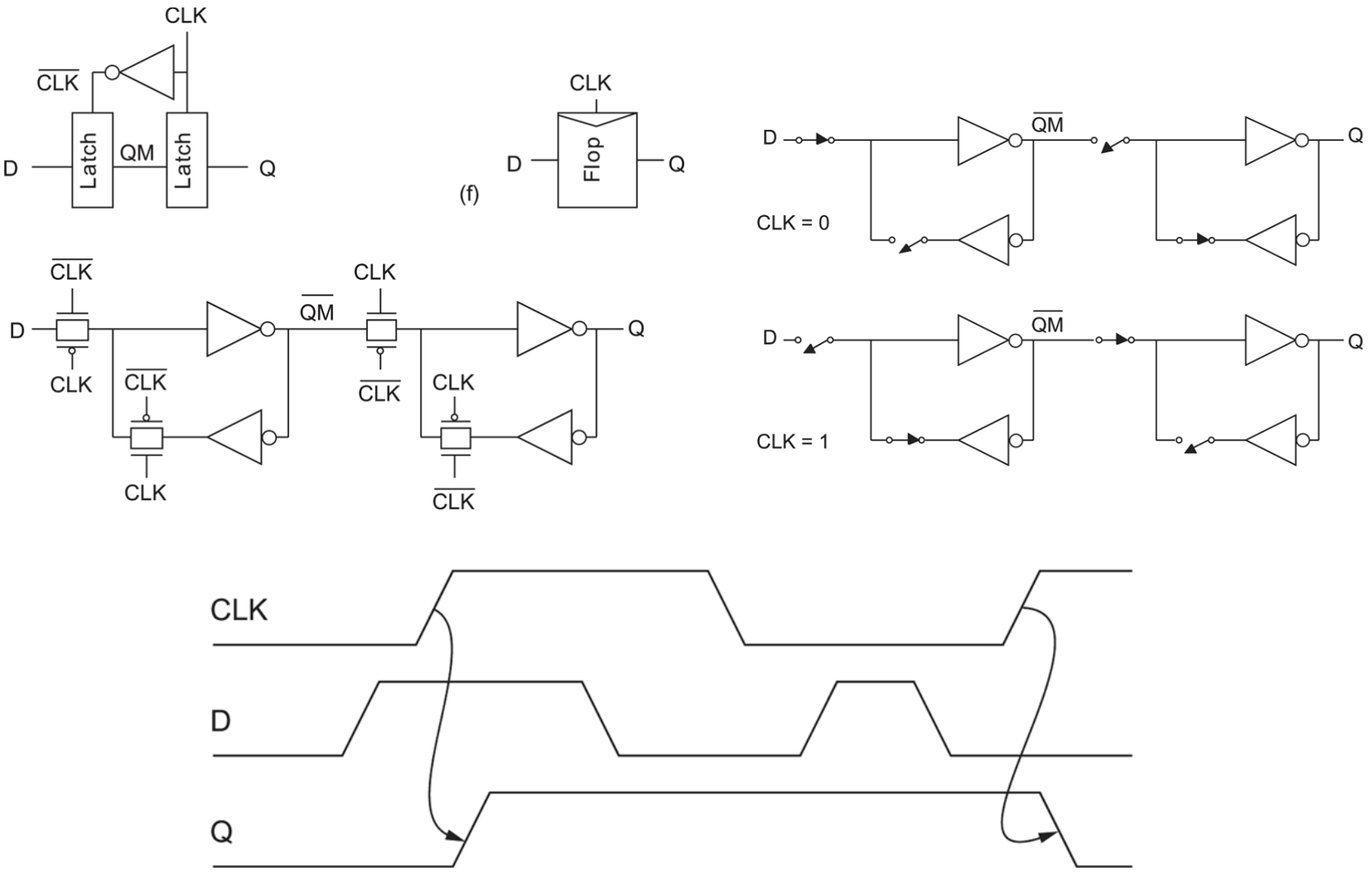


FIG 1.30 CMOS positive-level-sensitive D latch

Flip-flop (edge triggered) design



Summary

- Introduction to VLSI systems and the semiconductor industry
- Basic overview of pn junctions and MOS transistors
- Designing digital logic gates using transistors