Design and Implementation of VLSI Systems
Lecture03

CMOS fabrication

Lecture 03: CMOS fabrication

http://www.appliedmaterials.com/HTMAC/animated.html

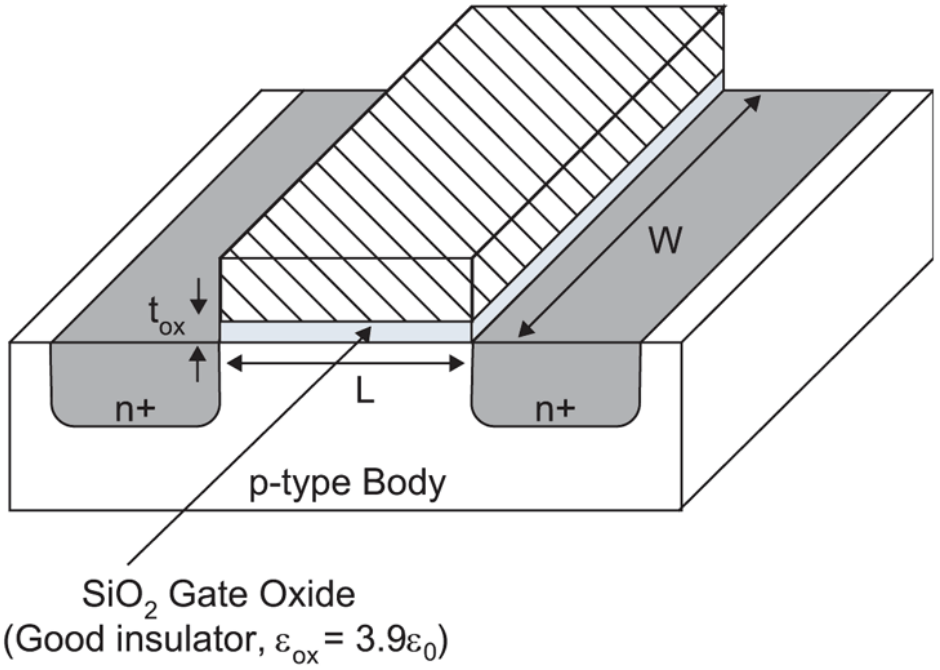
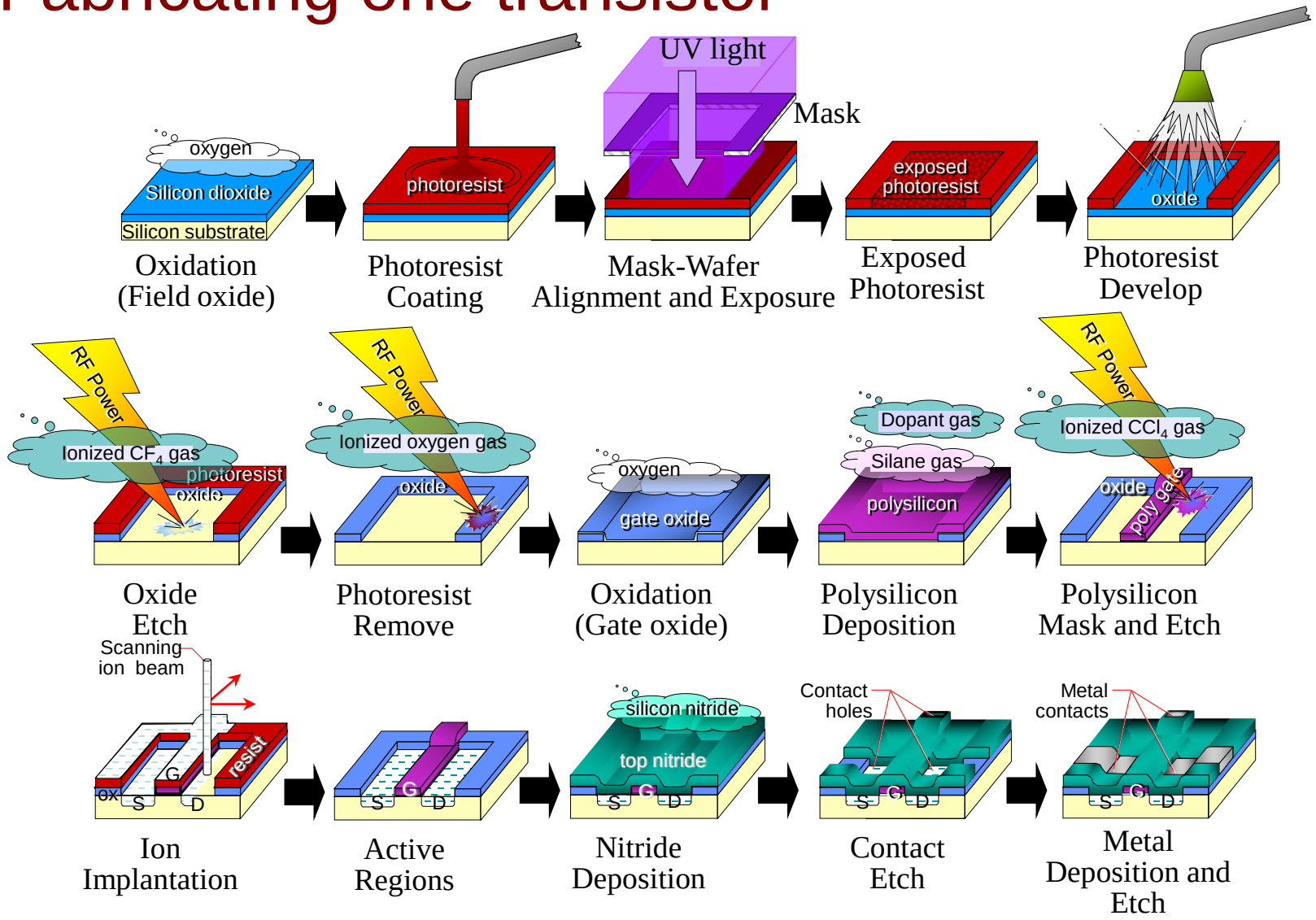
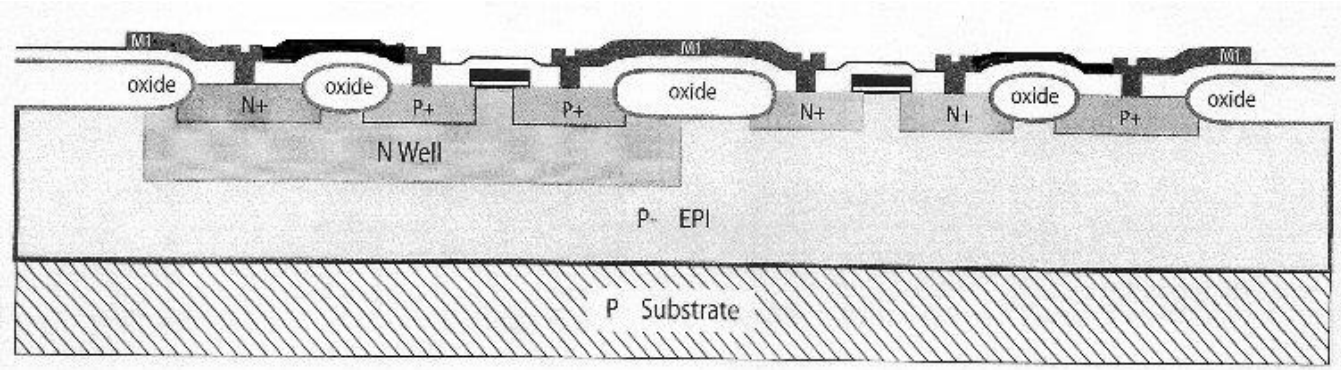


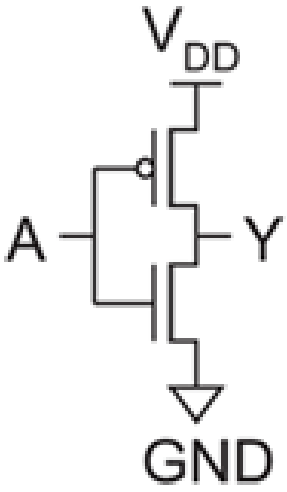
FIG 2.6 Transistor dimensions

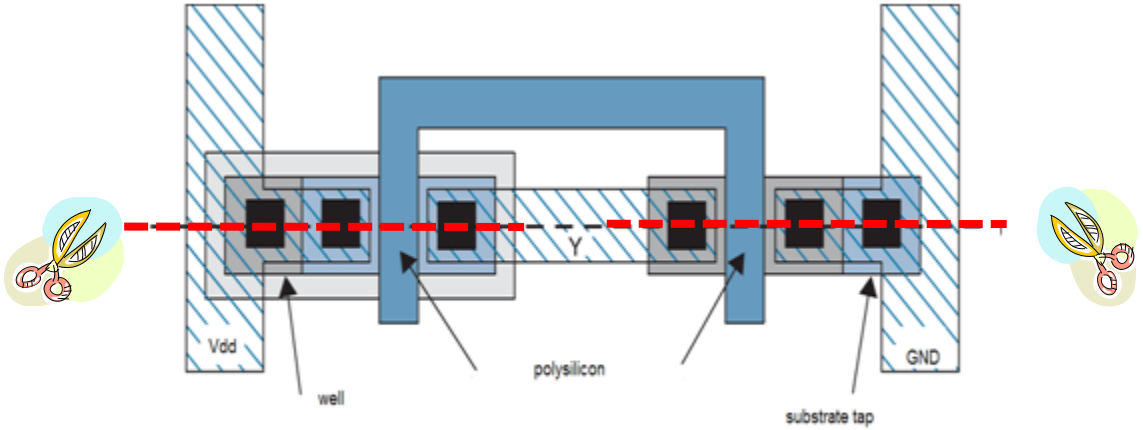
Fabricating one transistor

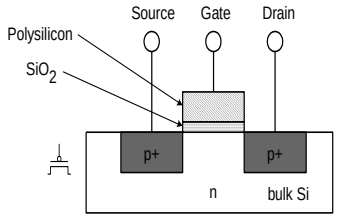


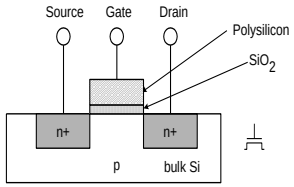
Top view


M1
oxide
N+
P+
N Well
P- EPI
P Substrate

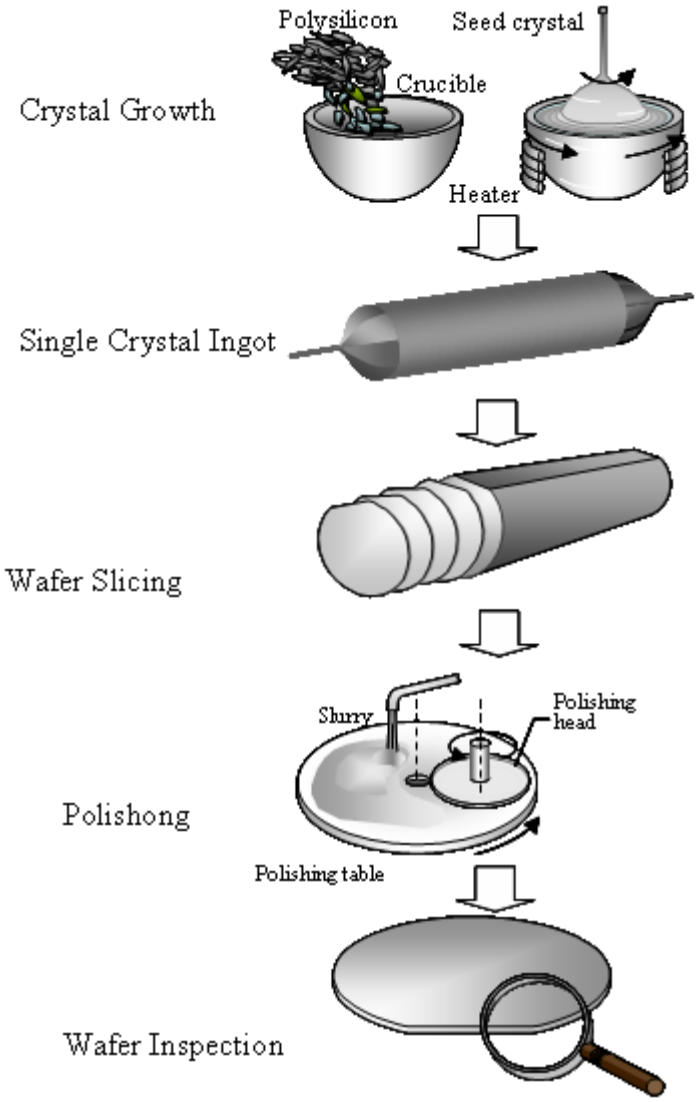

VDD
A
Y
GND

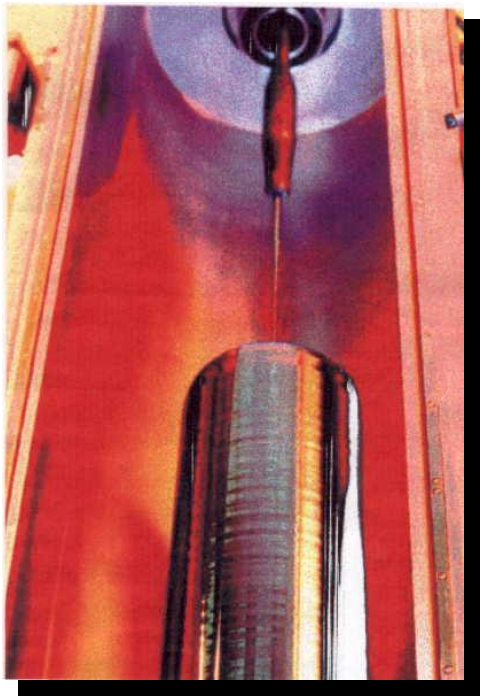

Y
Vdd
GND
well
polysilicon
substrate tap


Source
Gate
Drain
Polysilicon
SiO2
p+
p+
n
bulk Si

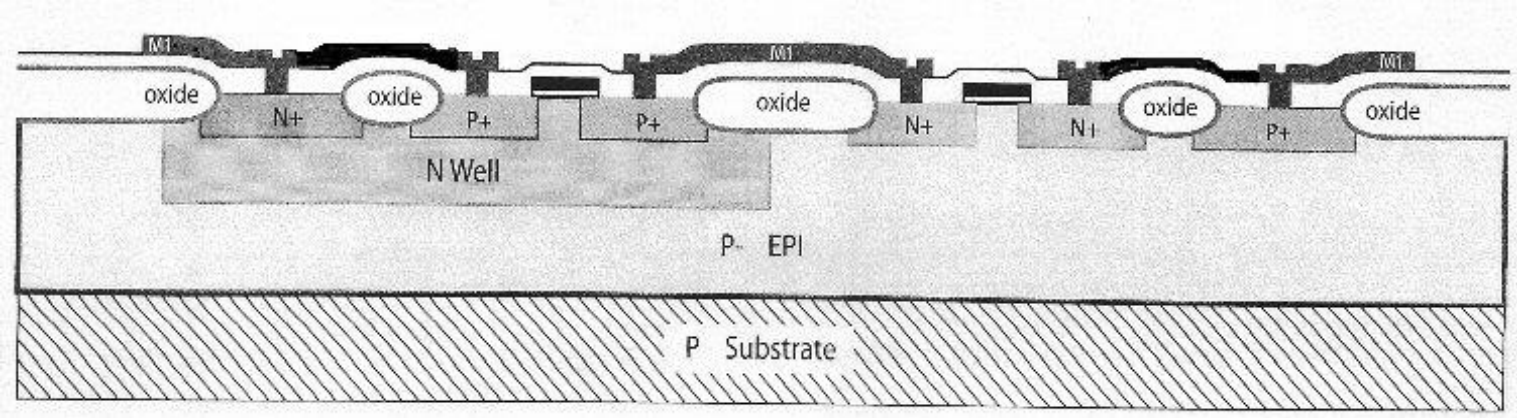

Source
Gate
Drain
Polysilicon
SiO2
n+
n+
p
bulk Si

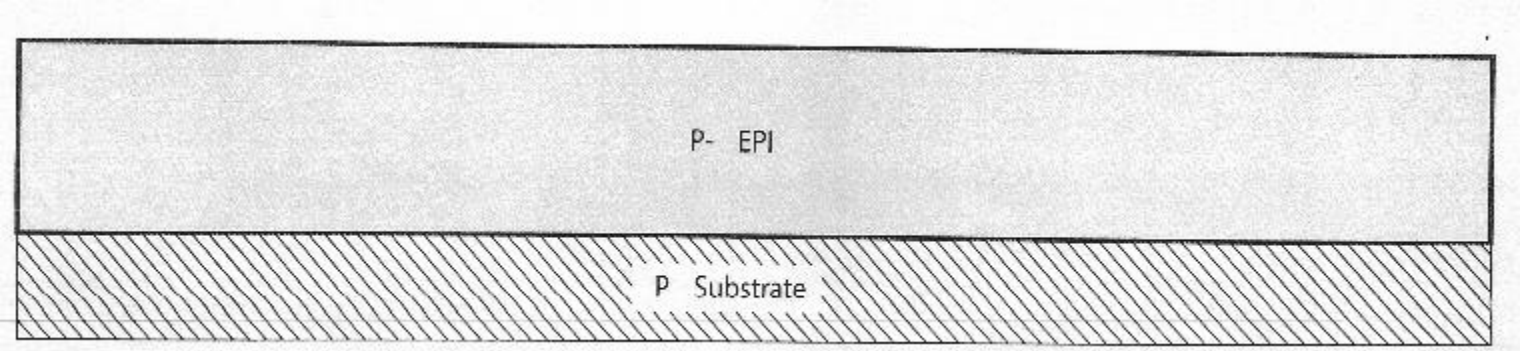
Wafer preparation



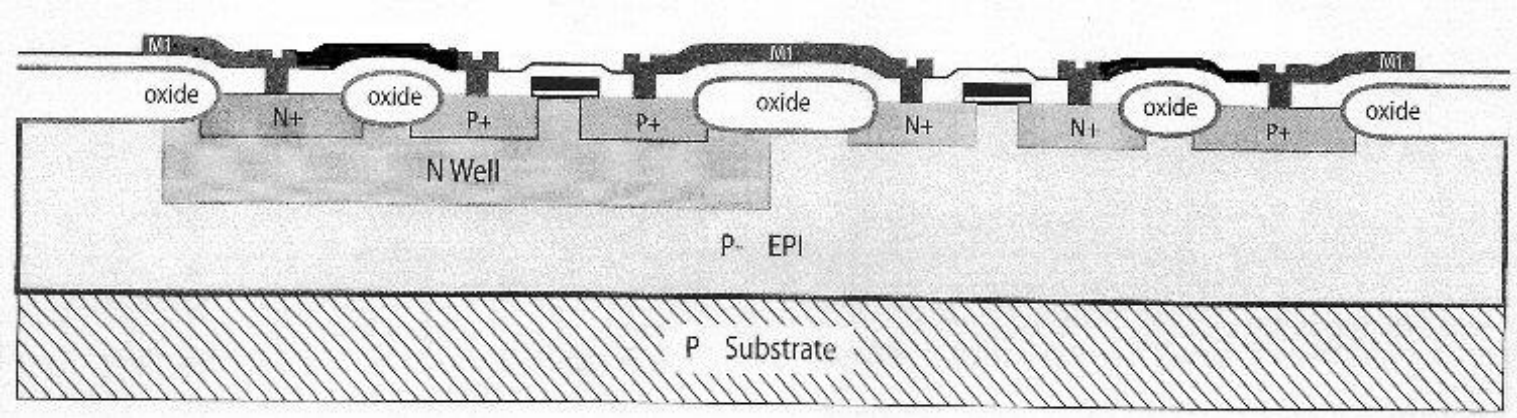


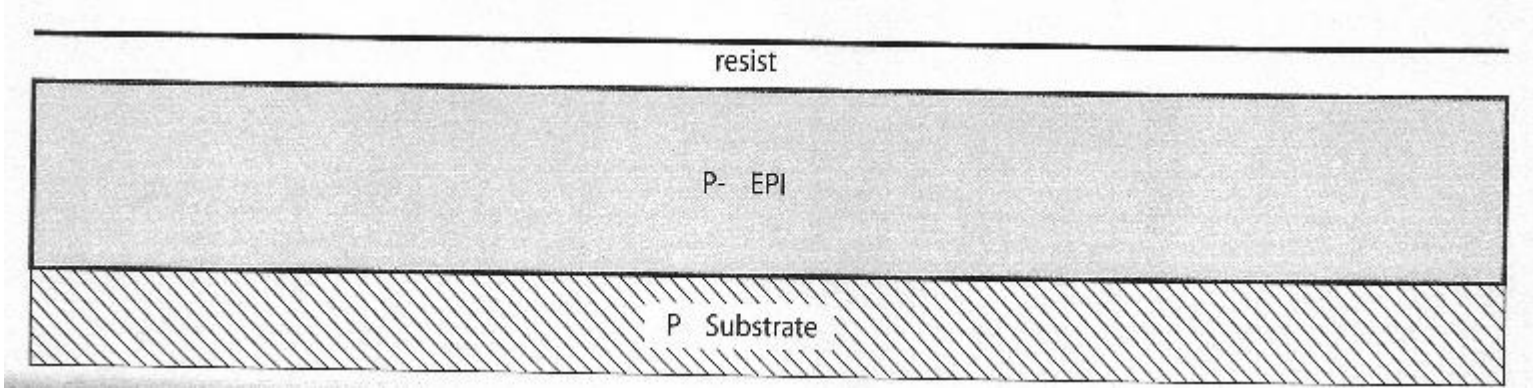
Start with P substrate



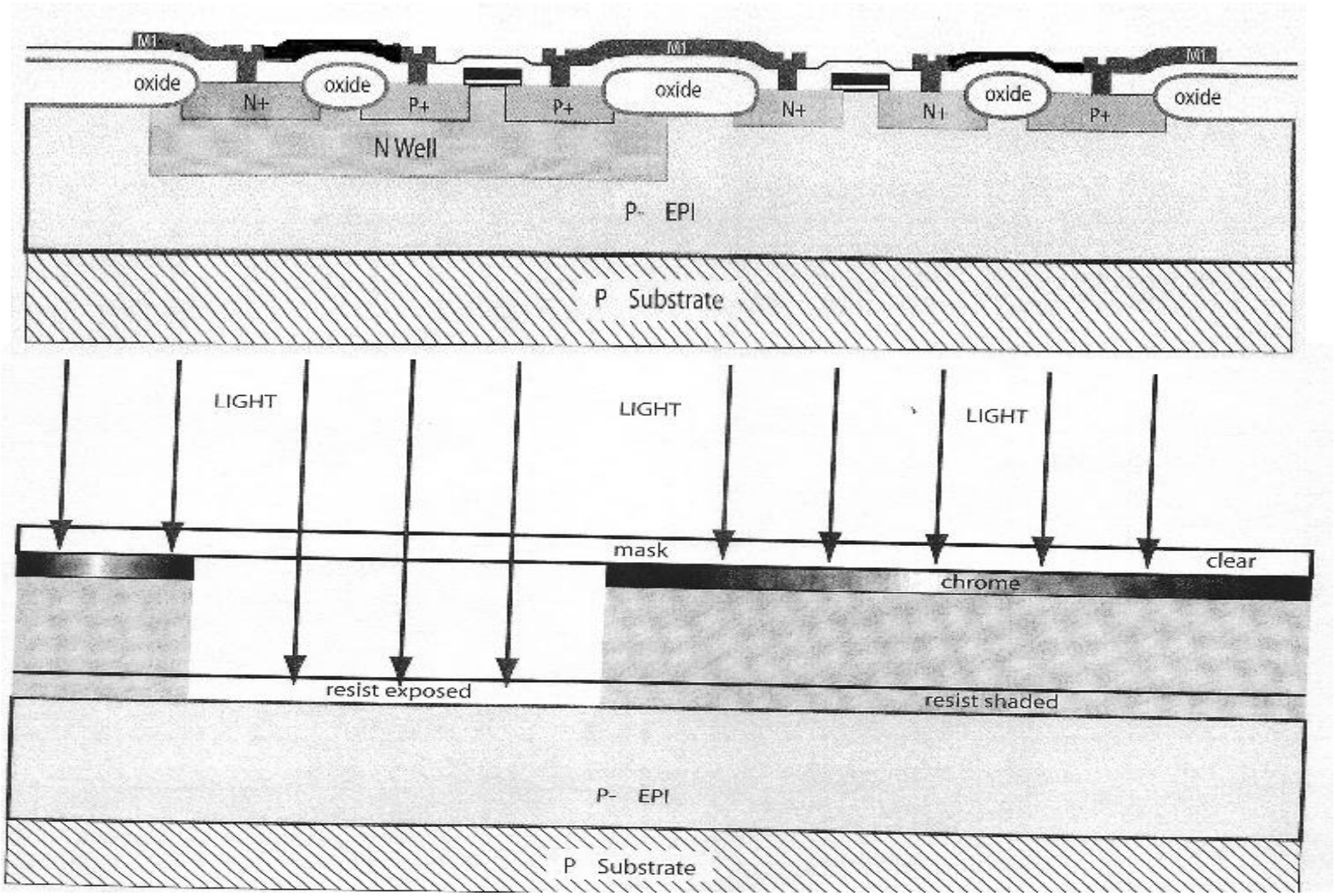


1. Spin Resist Coating

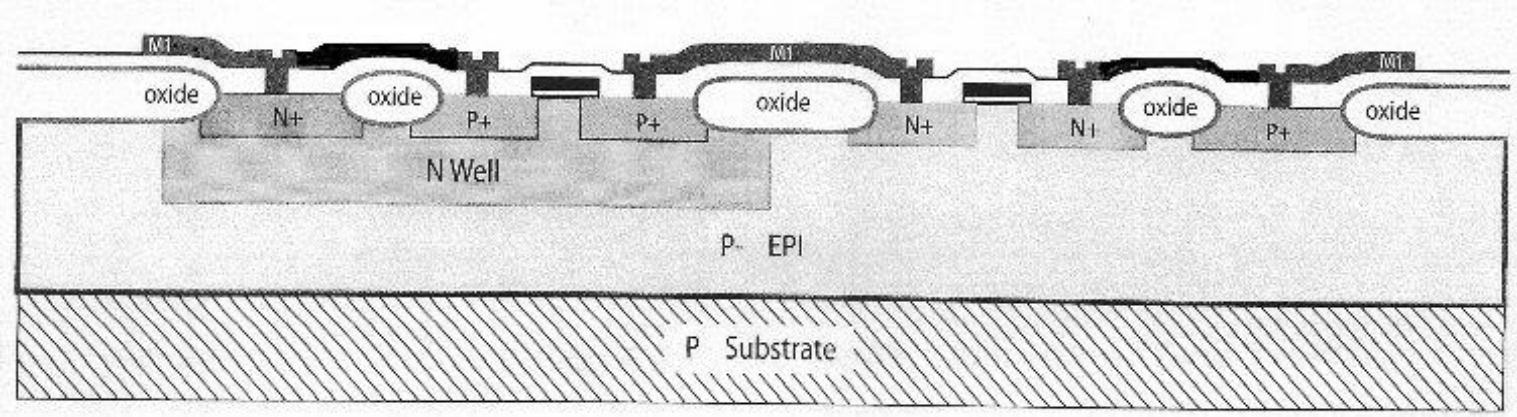


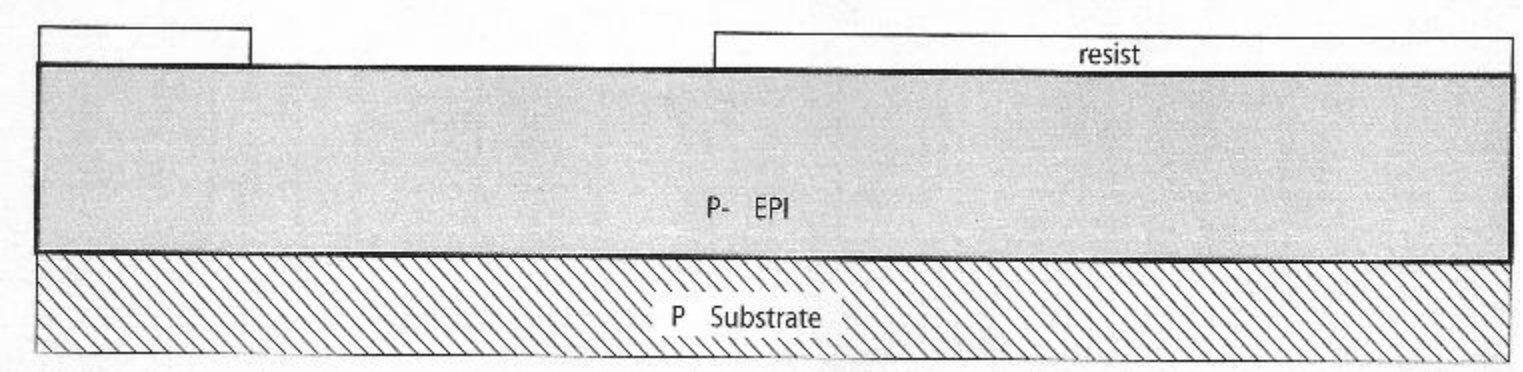


2. Expose N Well Mask

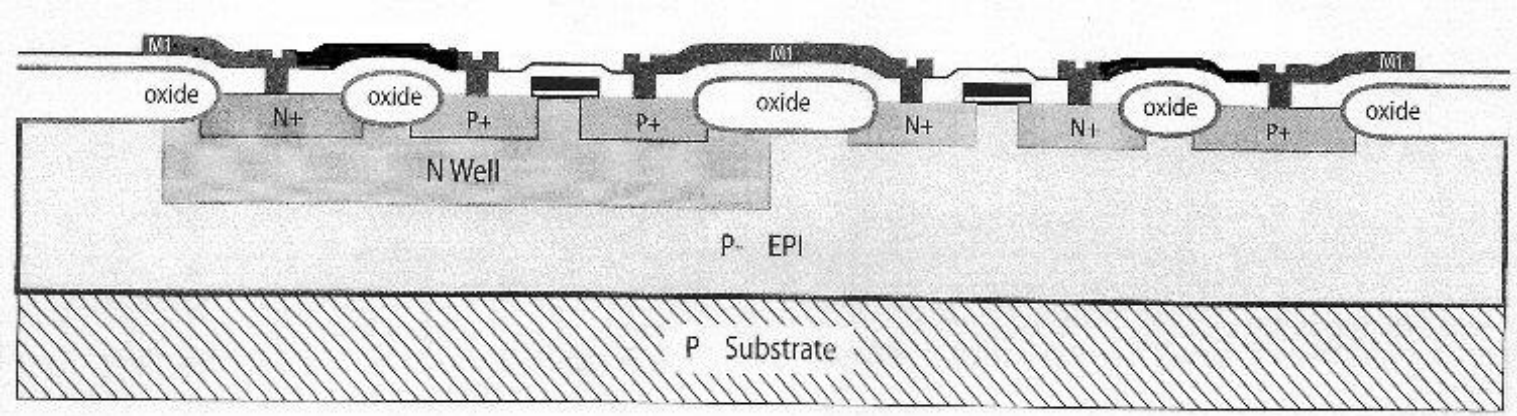


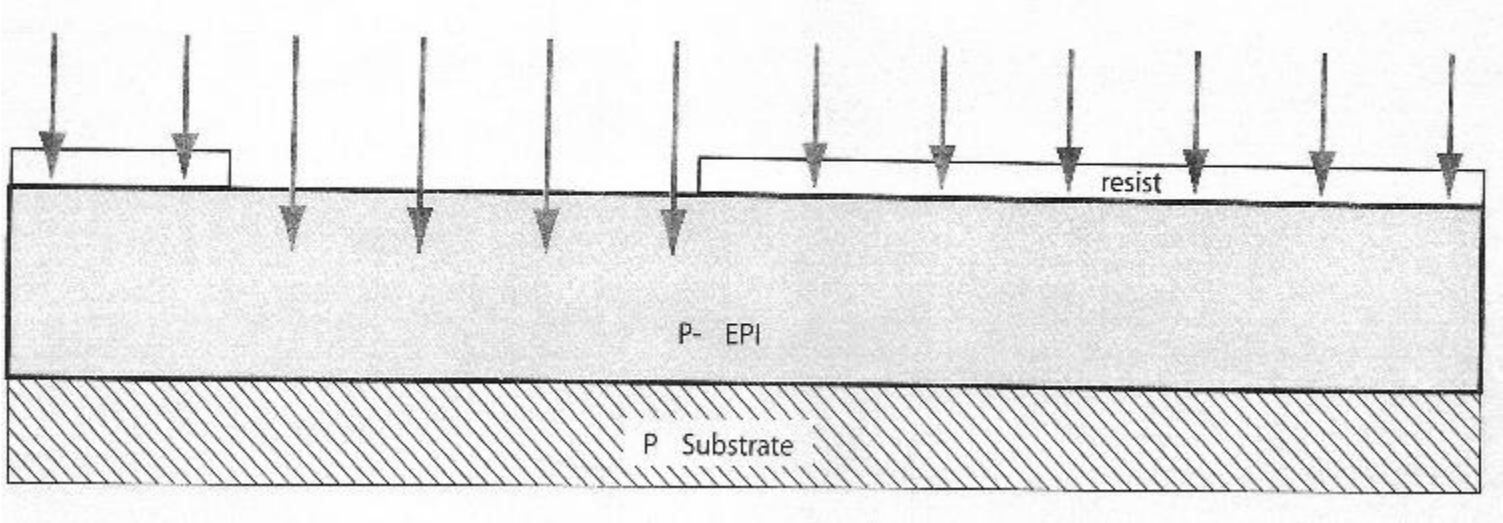
3. Develop resist



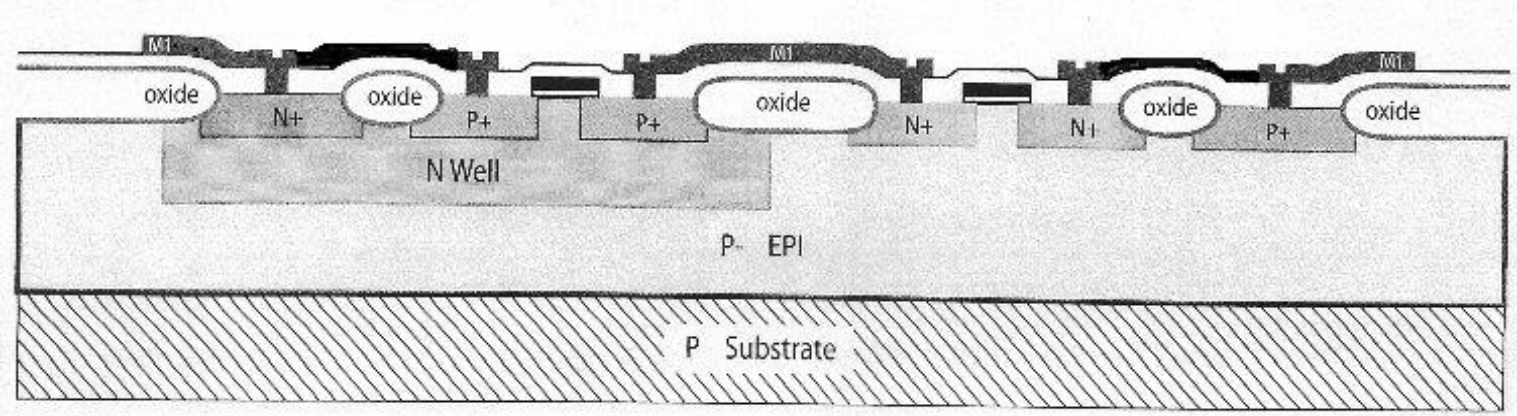


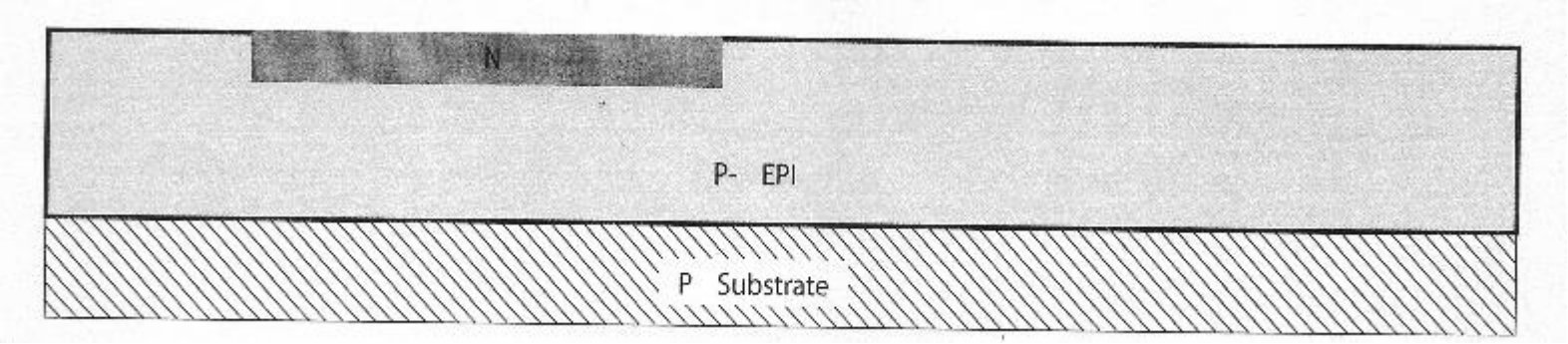
4. Implant N Well



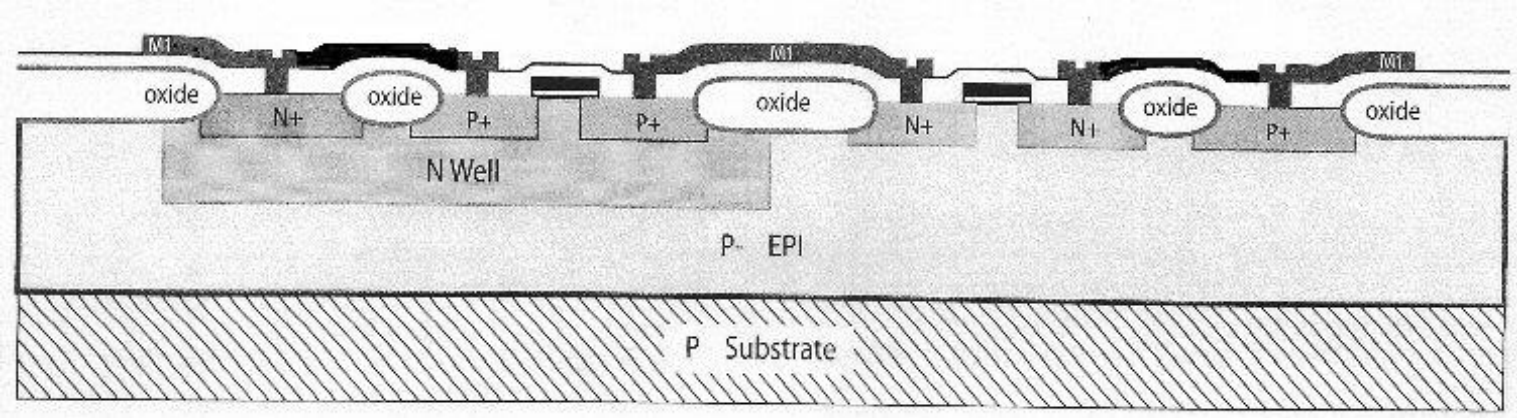


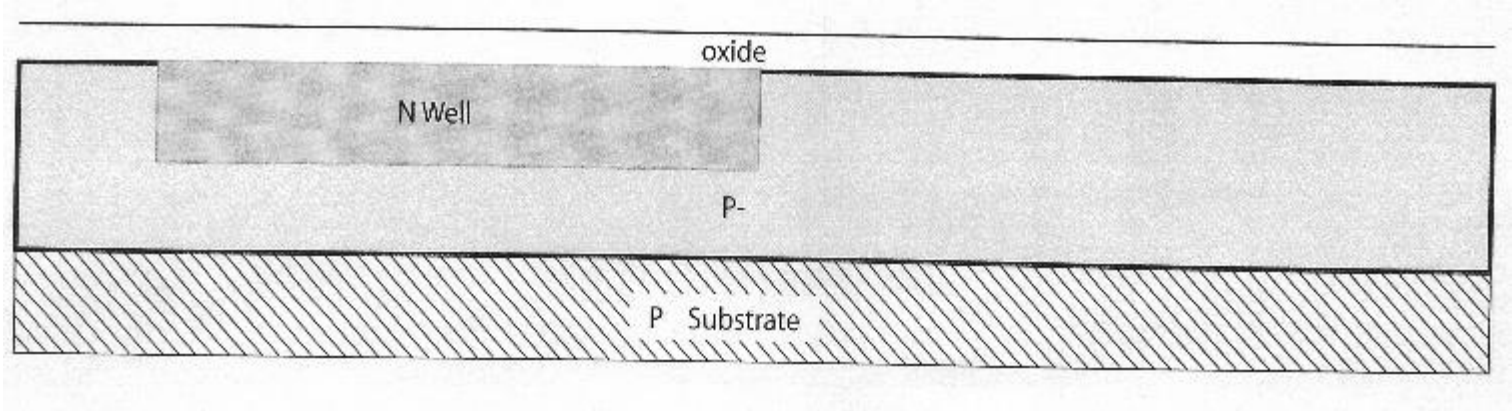
5. Remove Resist



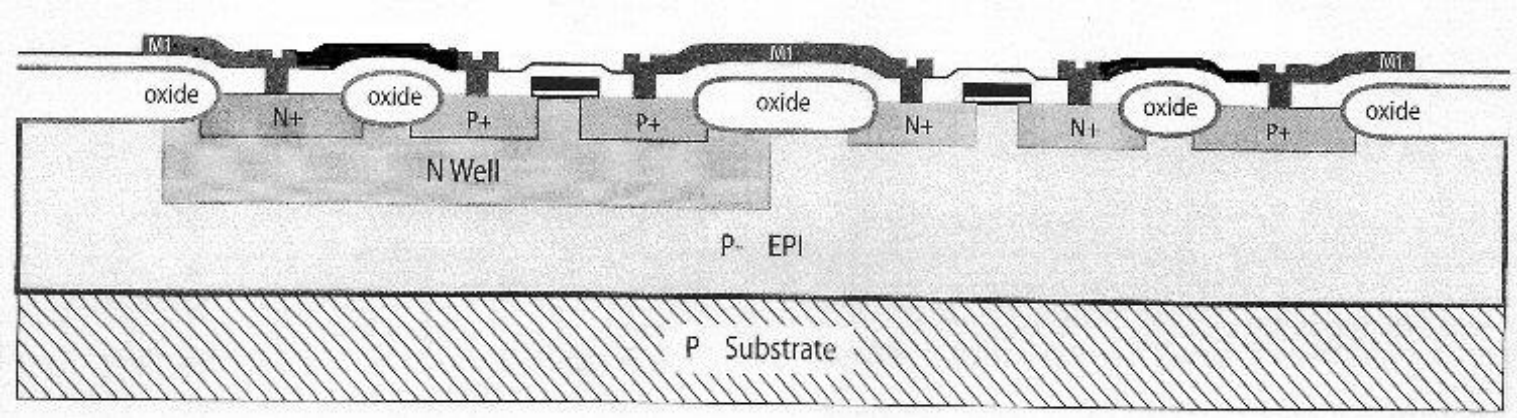


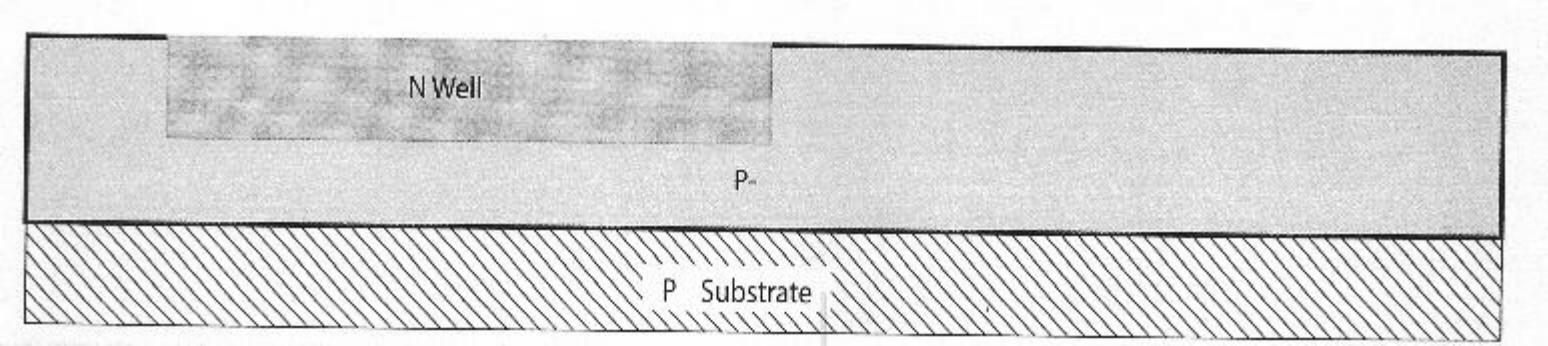
Anneal wafer to diffuses N well (heal lattice) and grow new oxide layer



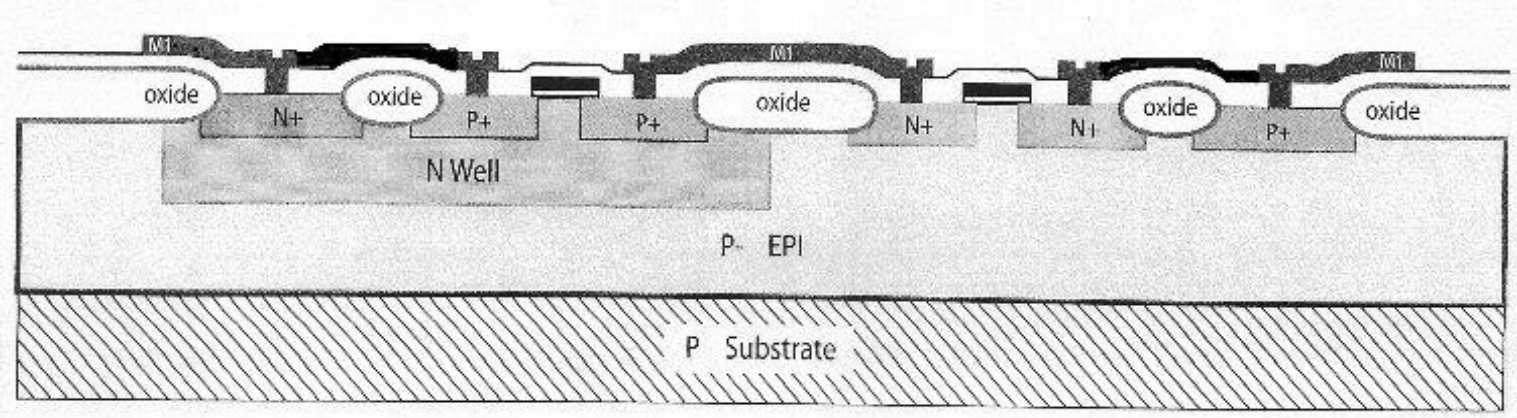


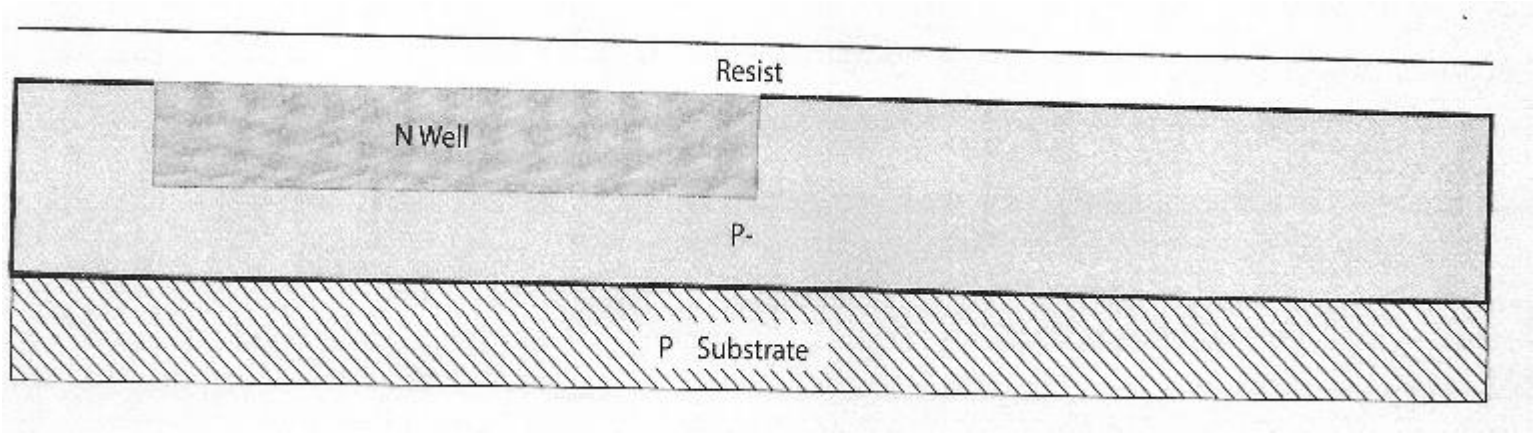
Remove oxide from anneal



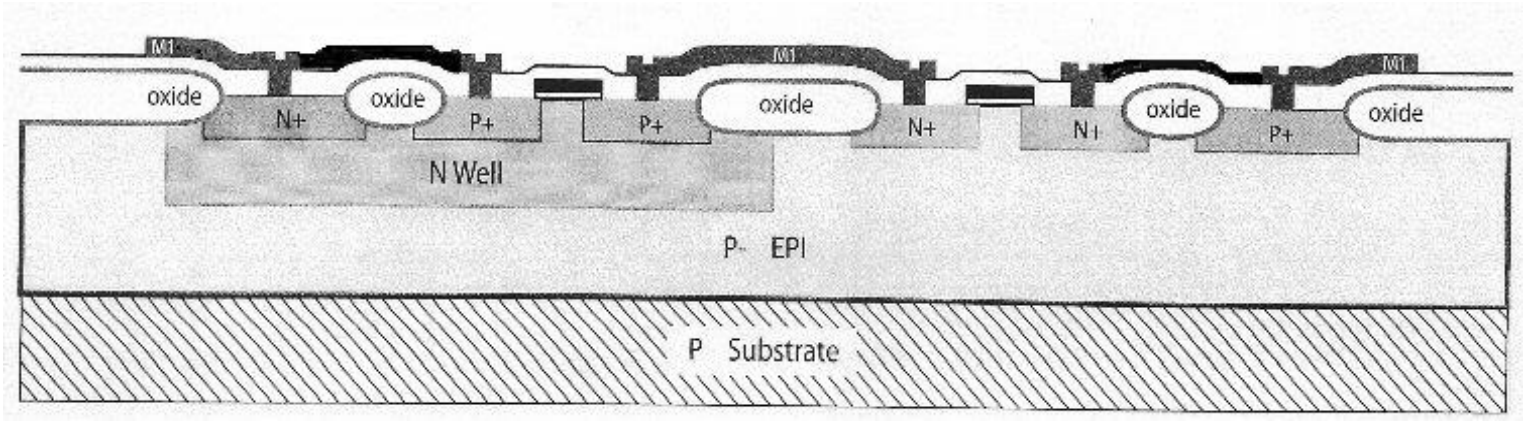


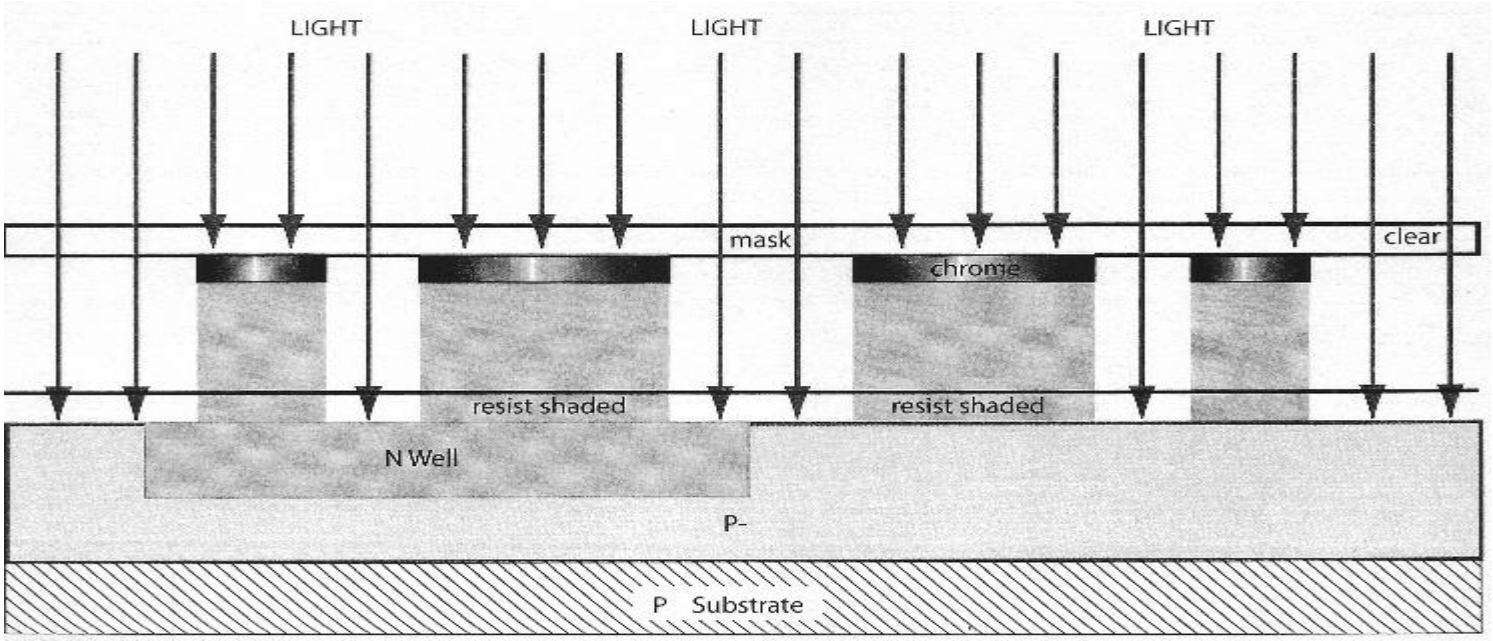
1. Spin Resist



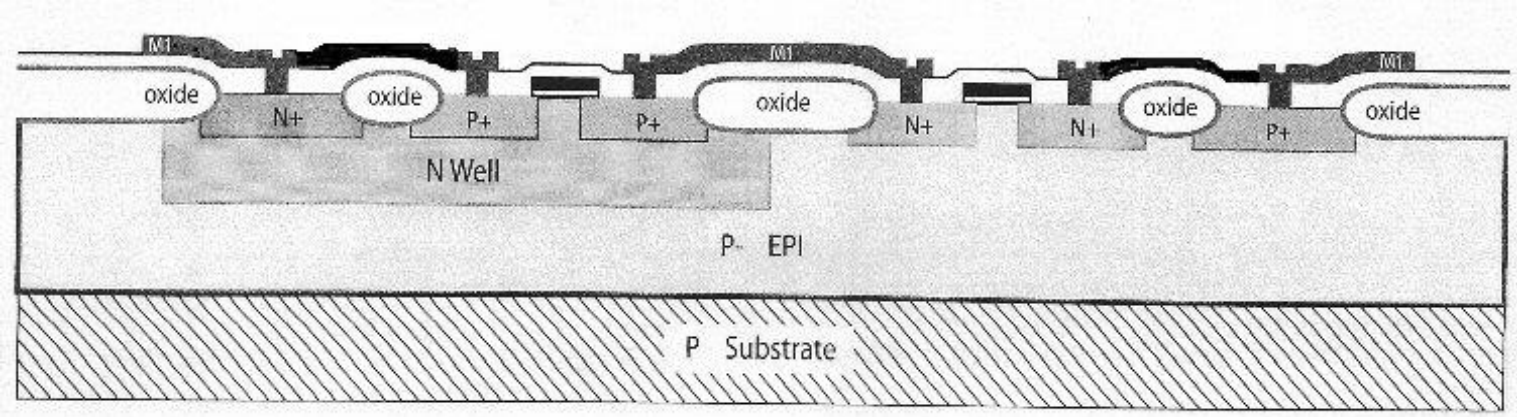


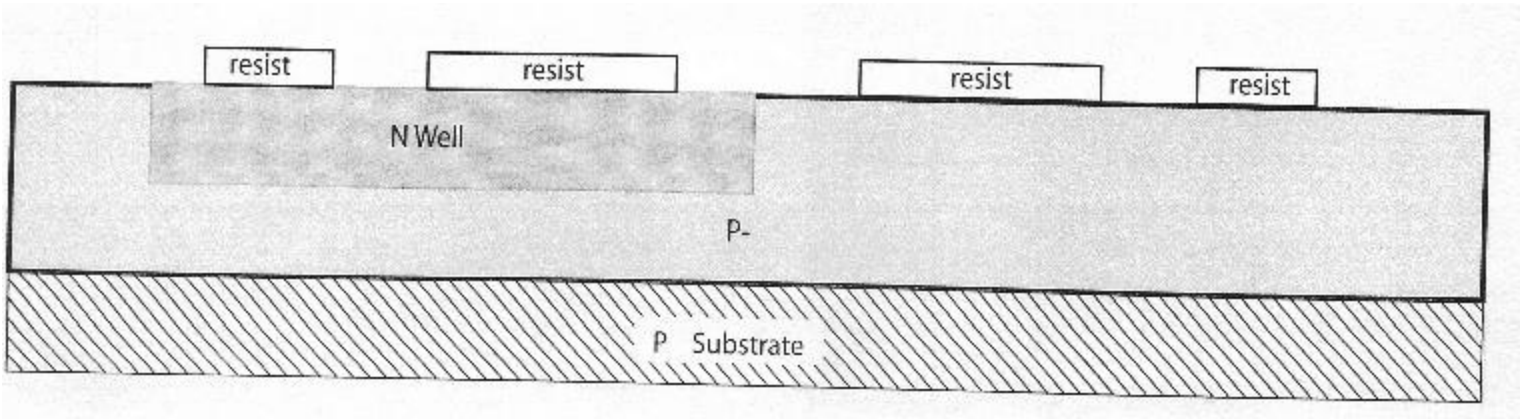
2. Expose resist with active diffusion mask



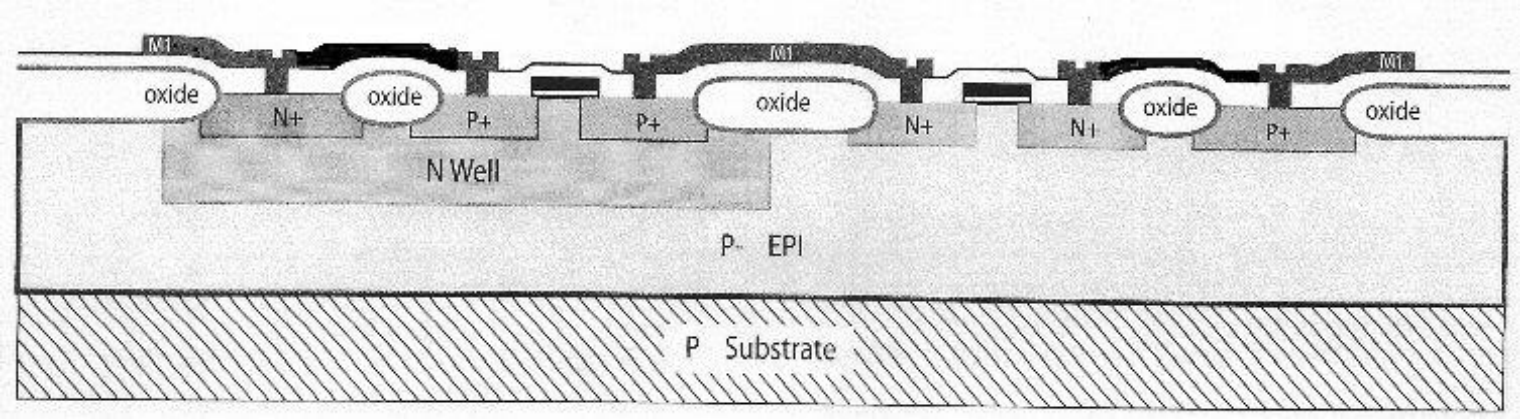


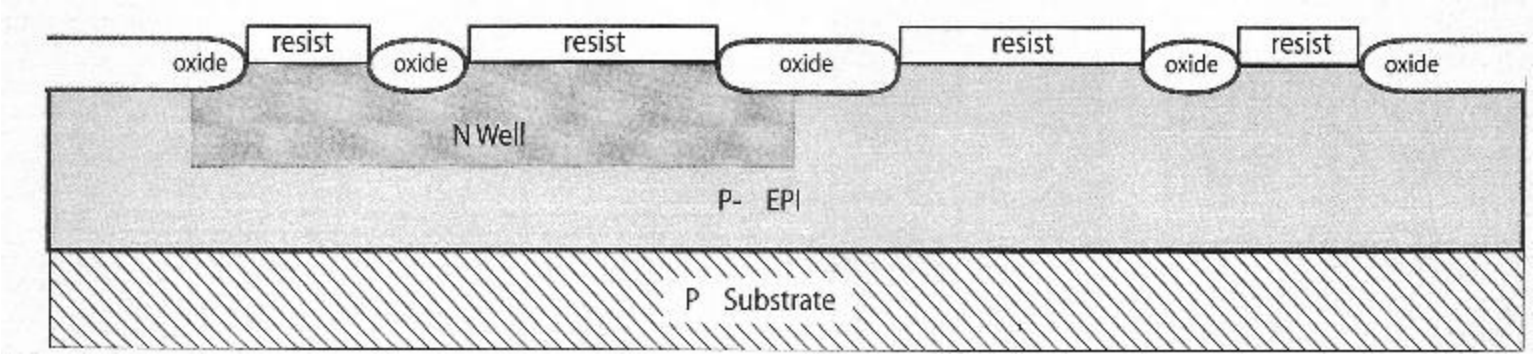
3. Develop resist



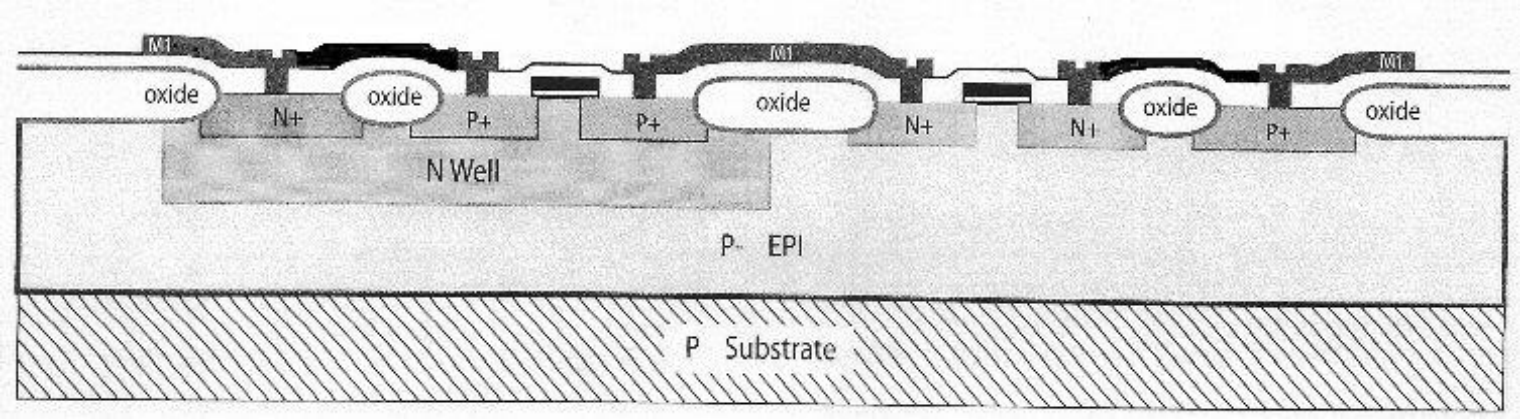


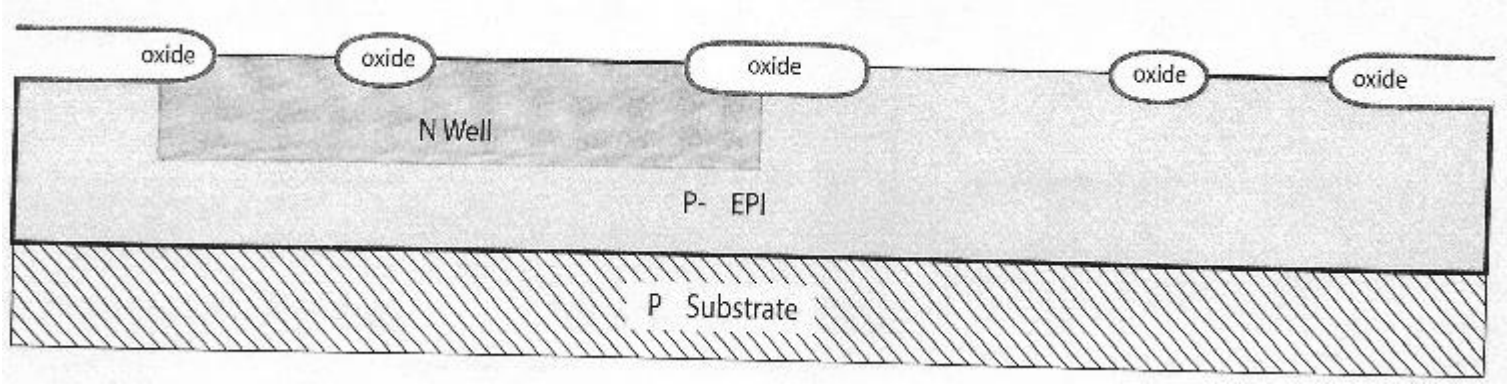
4. Grow oxide on exposed surface



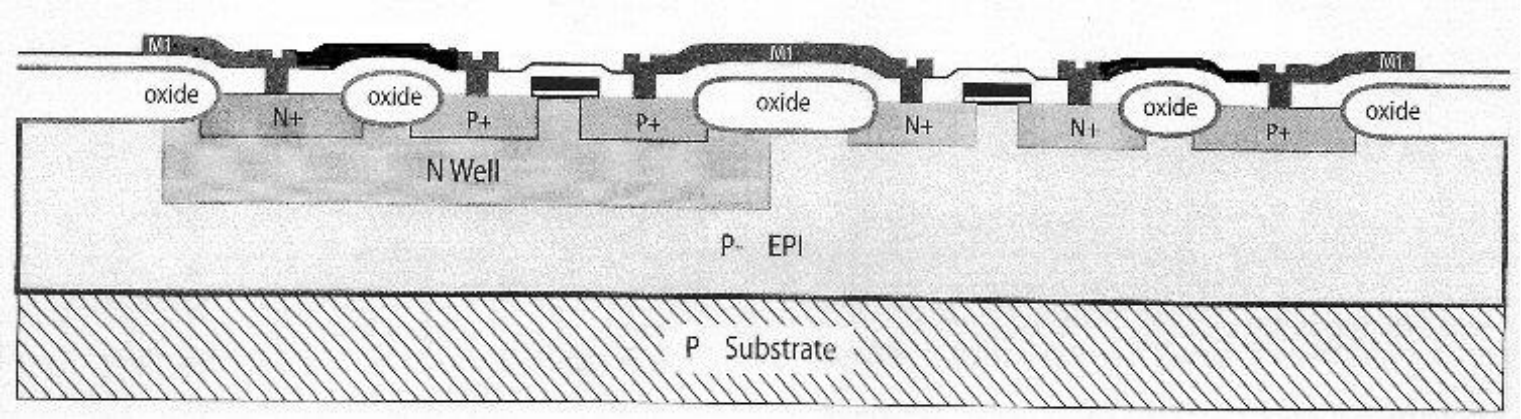


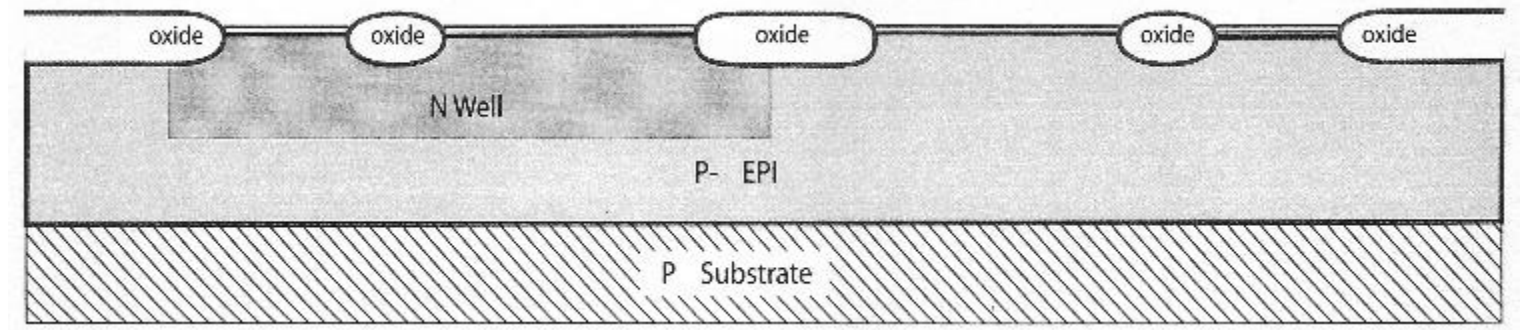
5. Strip resist



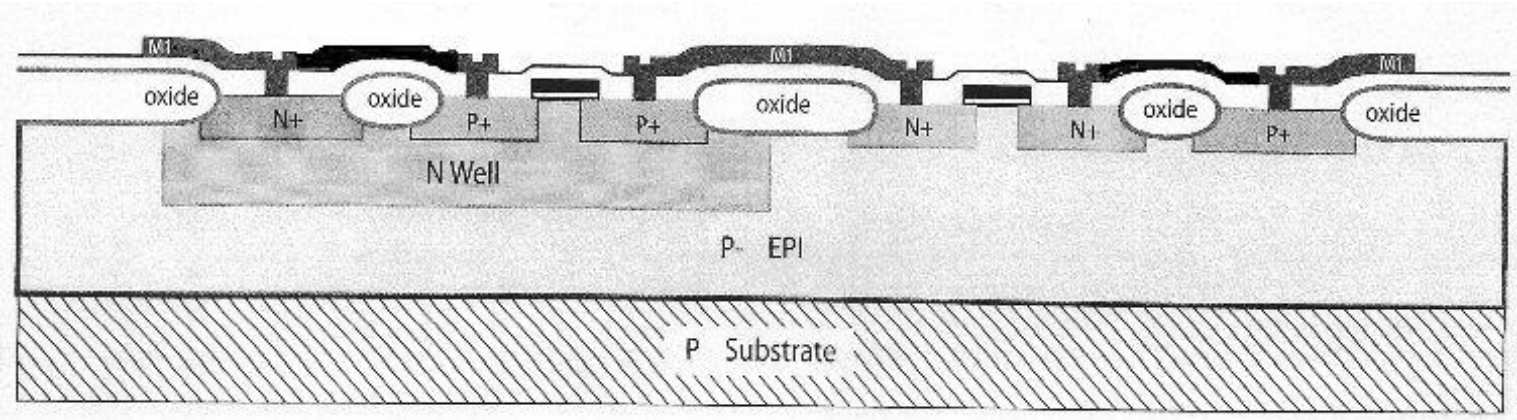


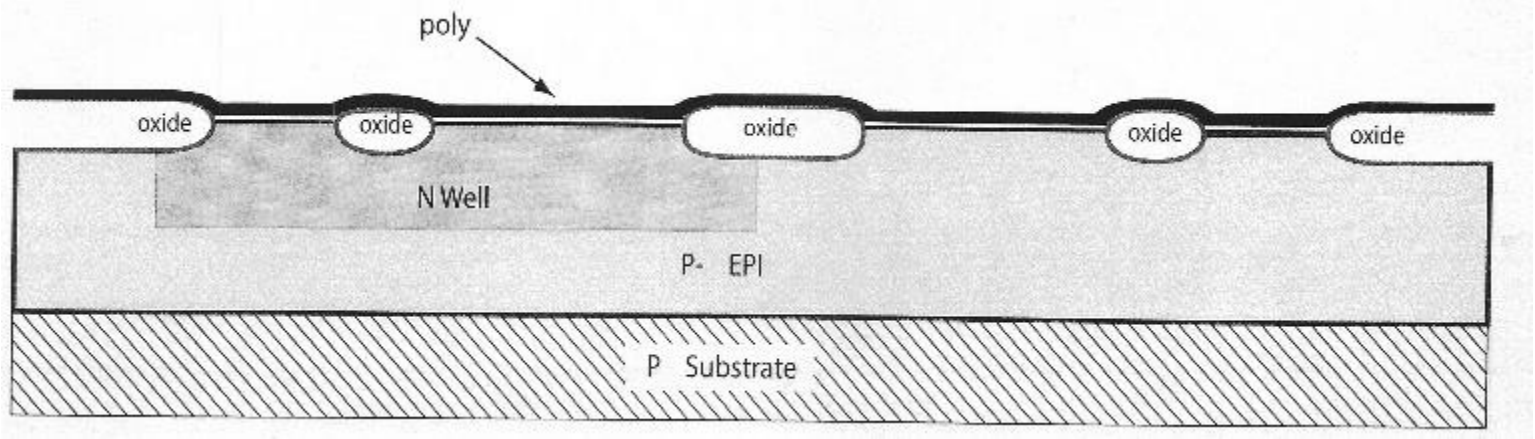
Grown thin oxide over silicon surfaces



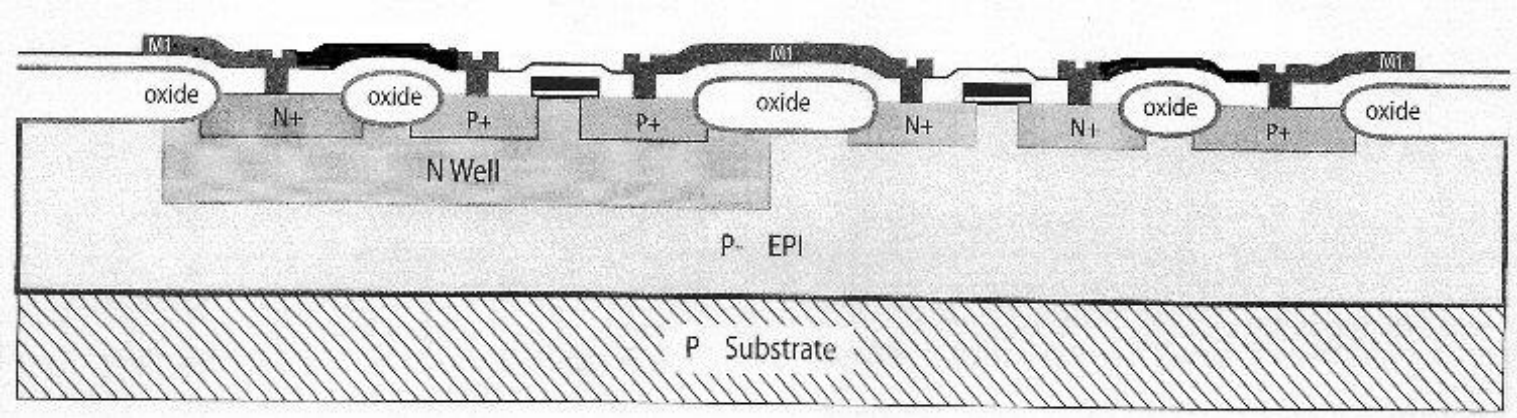


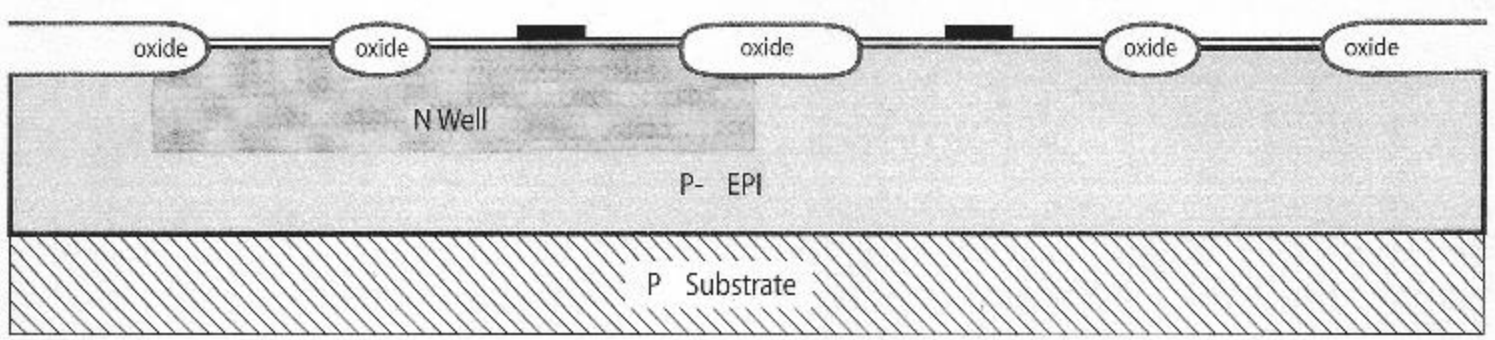
1. Deposit poly using Chemical Vapor Deposition (CVD)



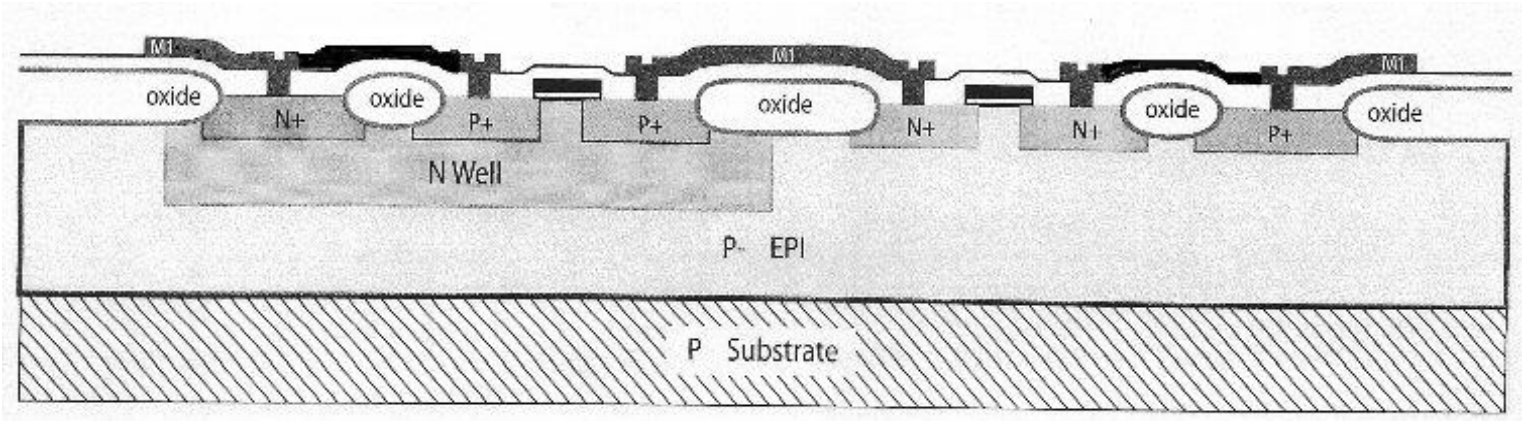


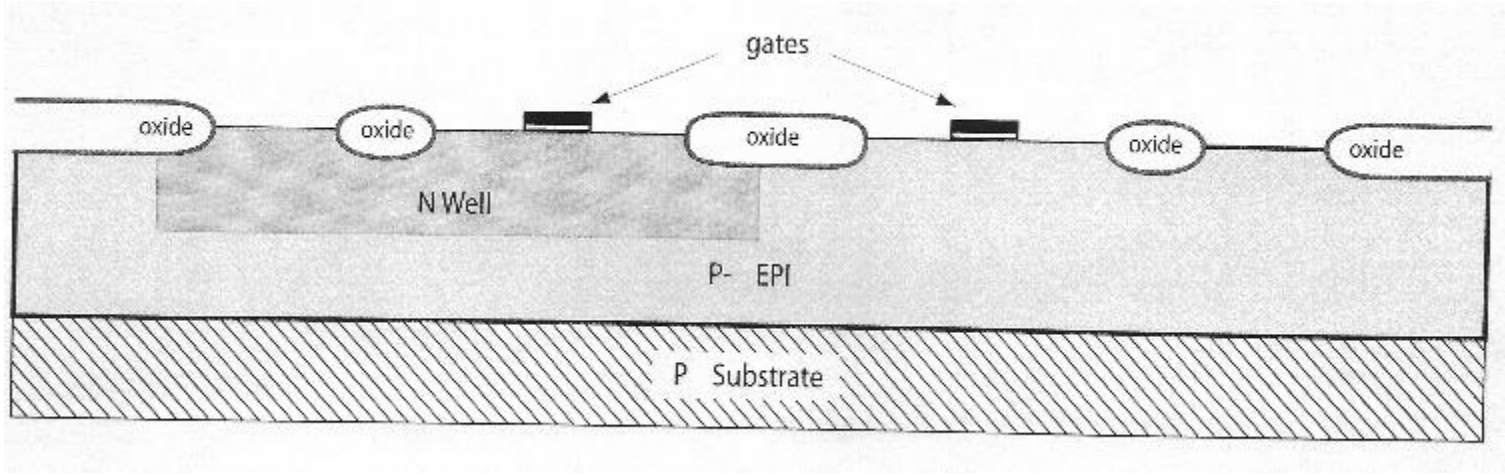
2. Spin resist 3. expose resist using the GATE mask 4. develop resist 5. etch poly



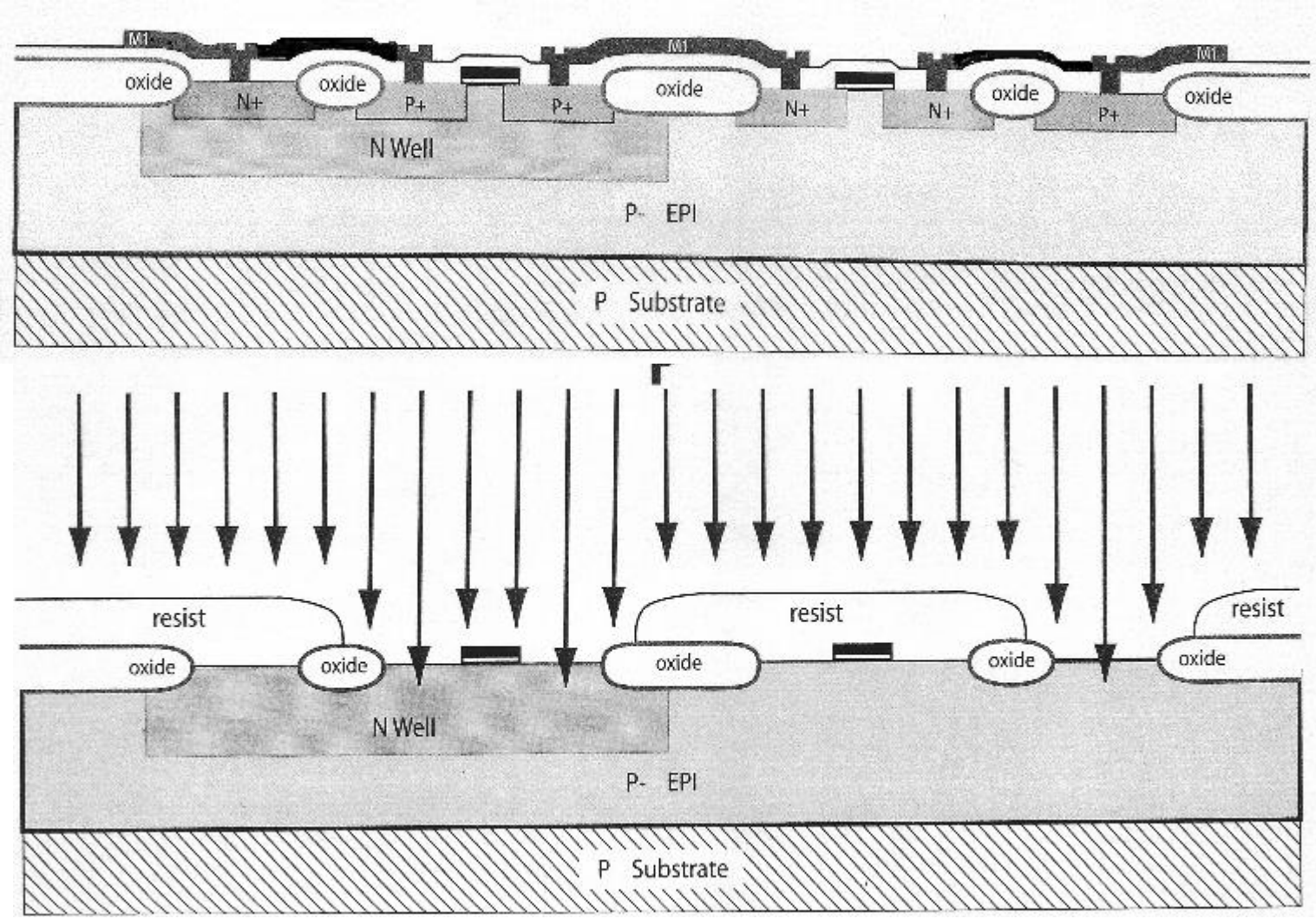


Remove thin oxide layer where exposed

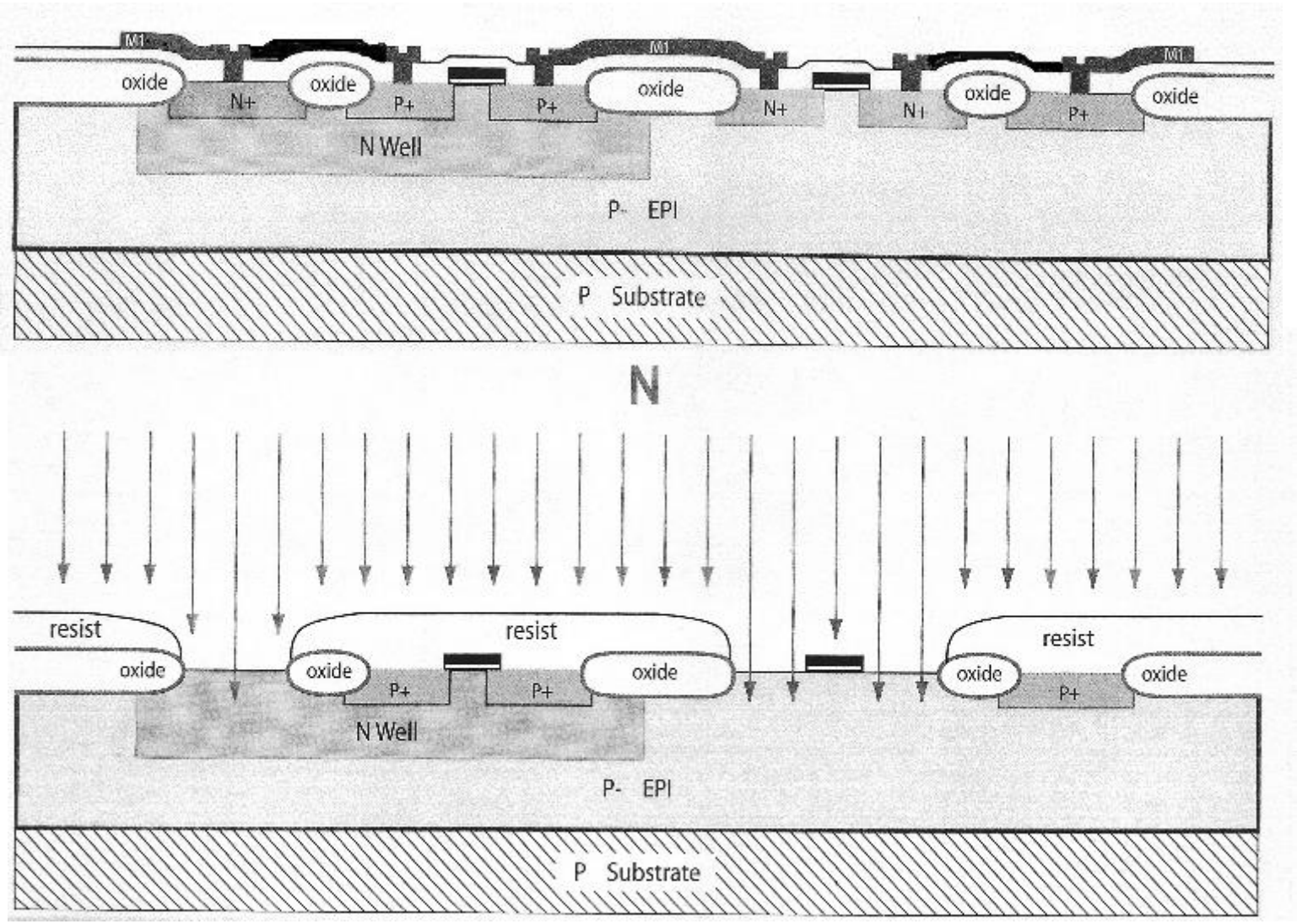




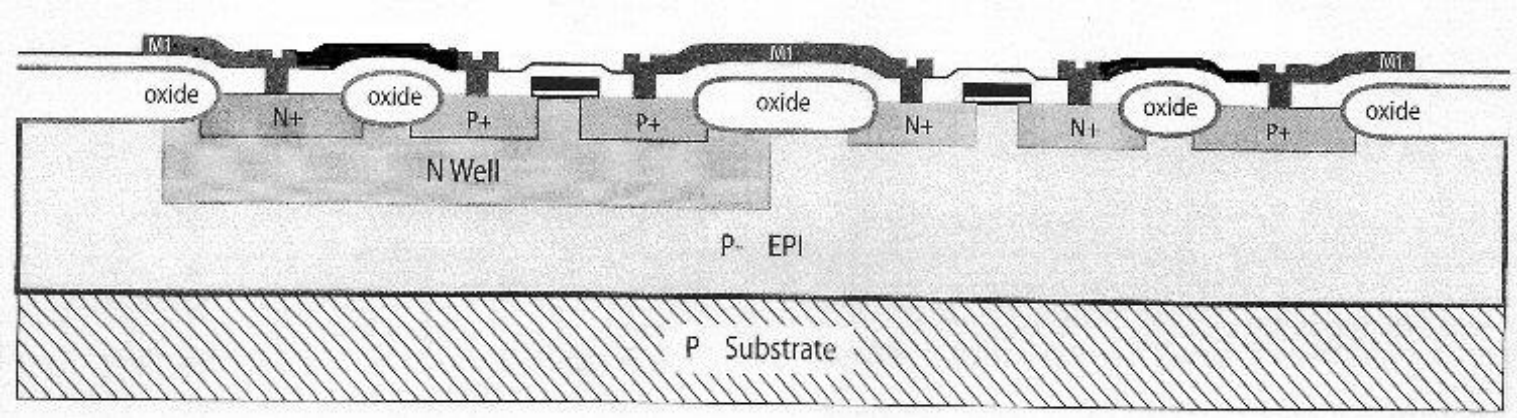
1. Spin resist 2. expose with P implant mask 3. develop resist 4. implant P 5. strip resist

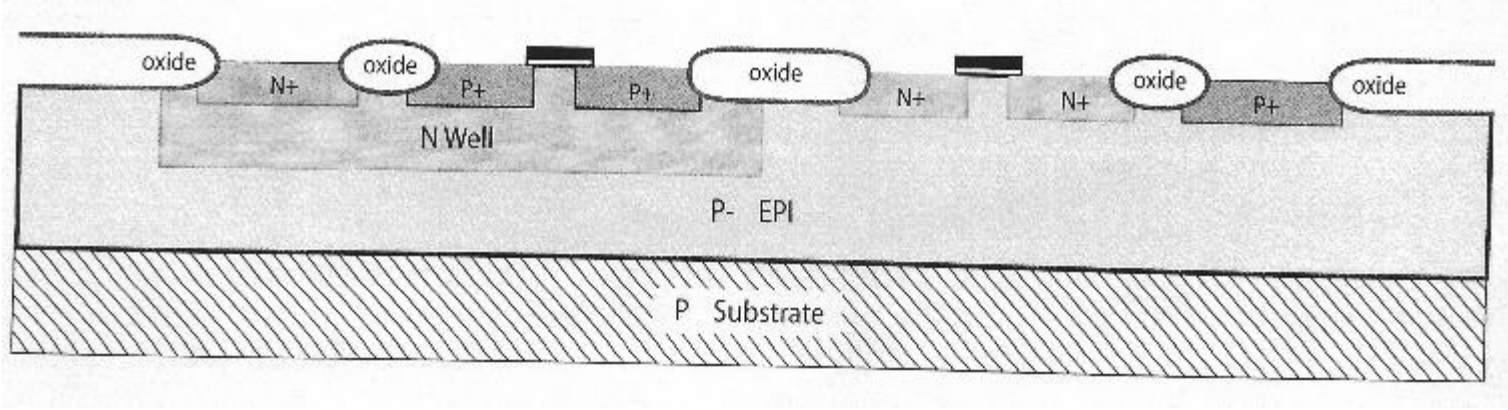


1. Spin resist 2. expose with N implant mask 3. develop resist 4. implant N 5. strip resist

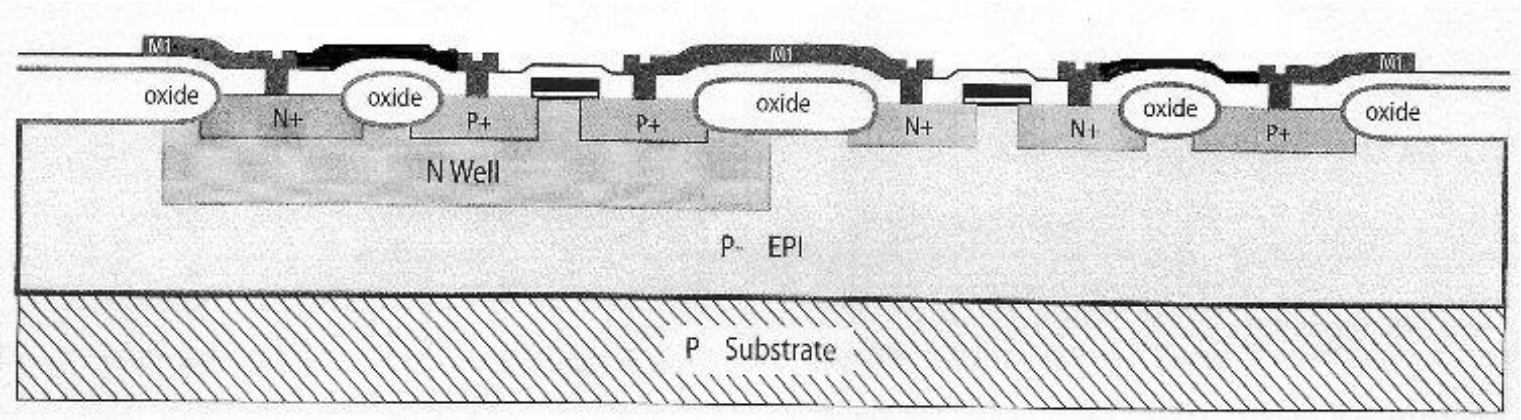


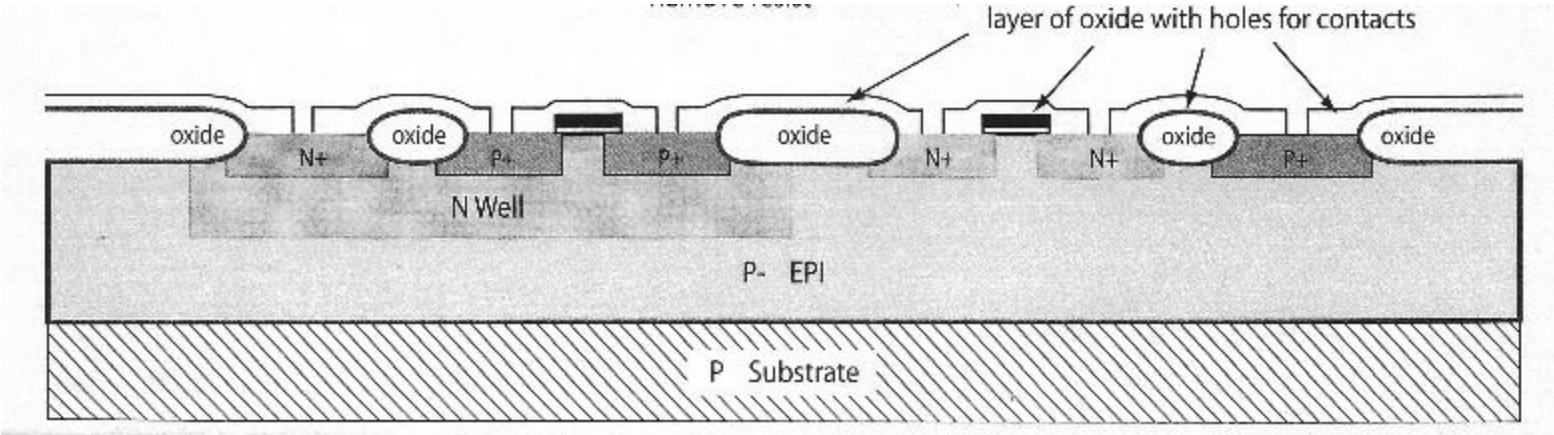
Remove resist – anneal wafer – oxide etch



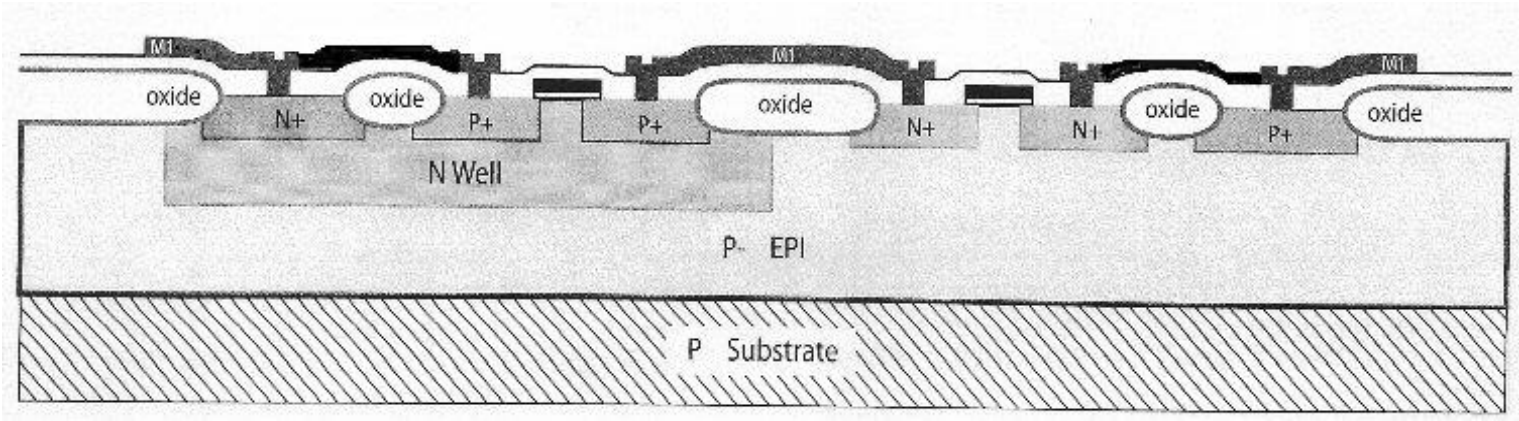


Grow oxide 1. spin resist 2. expose Contact mask 3. develop resist 4. etch contacts 5. strip resist

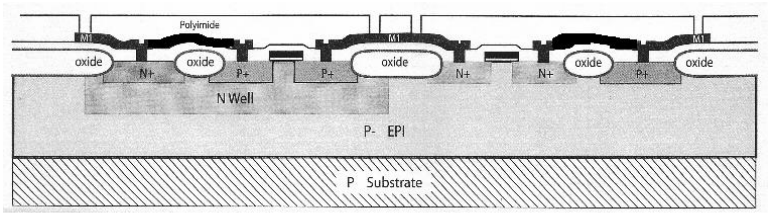


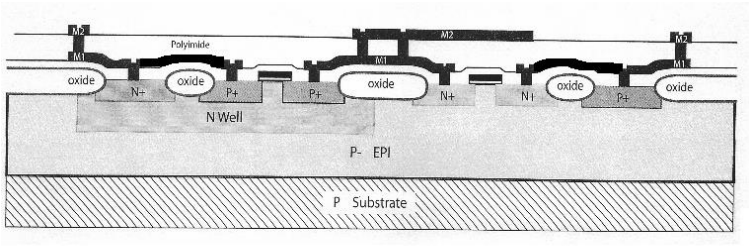


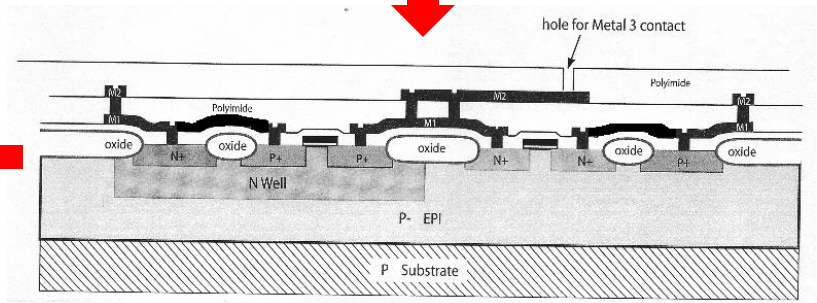
1. Deposit metal L1 2. spin resist 3. expose metal L1 mask 4. develop resist 5. etch metal 6. strip resist

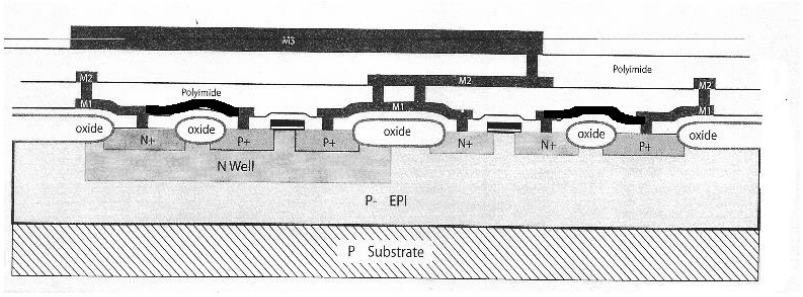


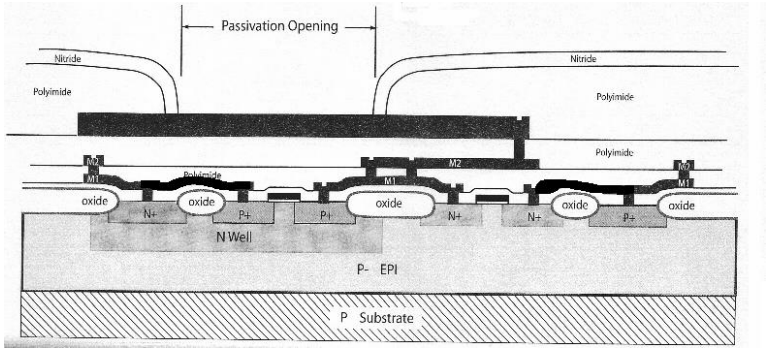
Rest of metal layers follow similarly



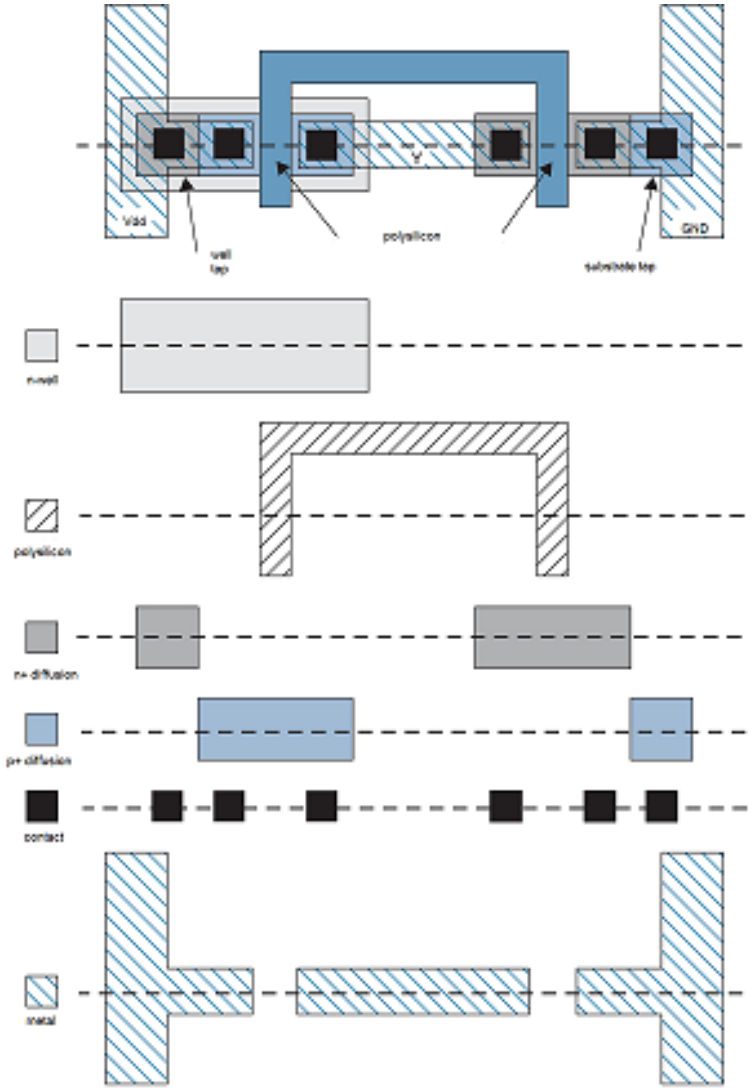




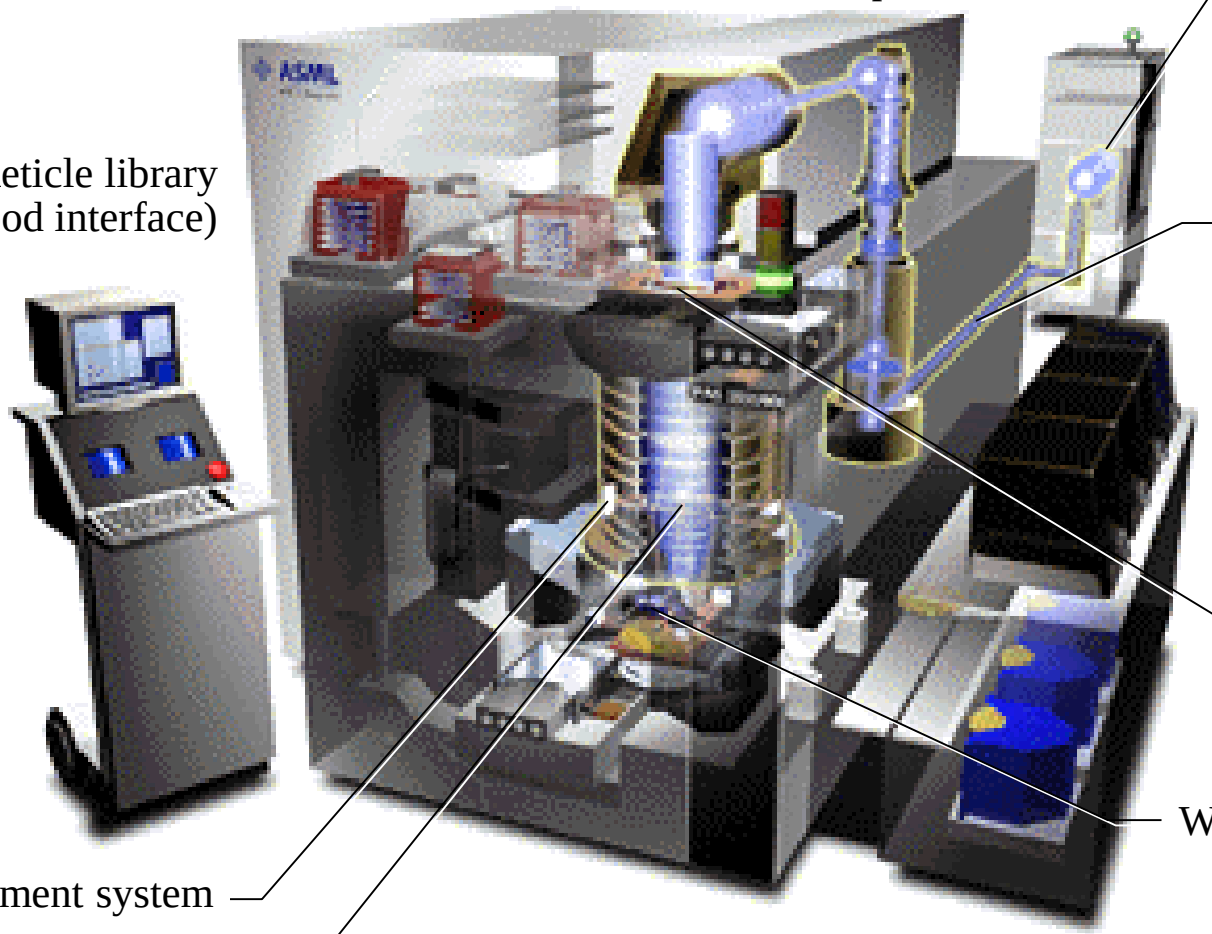




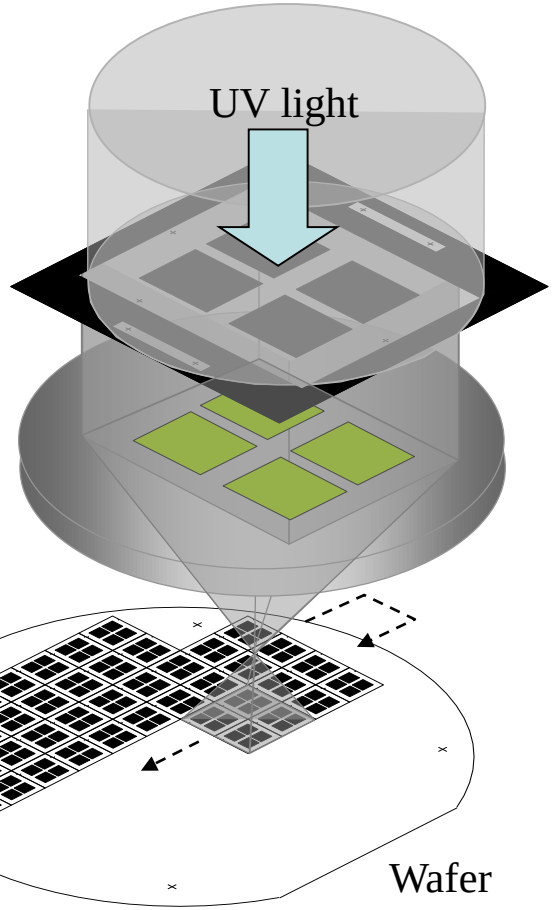
Printing masks



The printer

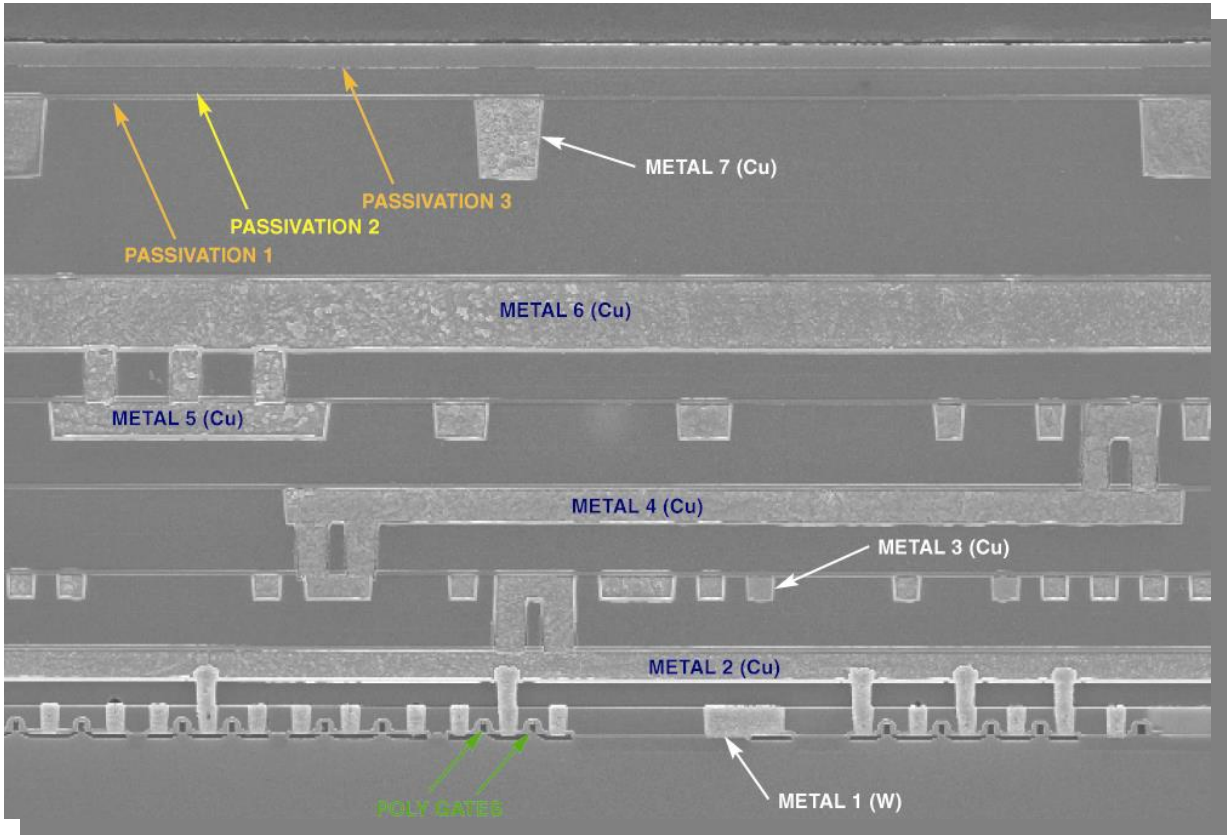

Illuminator optics
Excimer laser
(193 nm ArF)
Reticle library
(SMIF pod interface)
Beam line
Operator
console
Wafer transport
system
Reticle stage
Wafer stage
Auto-alignment system
4:1 Reduction lens
NA = 0.45 to □ 0.6

Photolithography is used to print desired patterns on the wafer



The feature size directly depends on the wavelength of your lithographic system

Cross section of a 7-metal layer IC



Next time:

How to print different gates?