Inyeon

Team members:

Hifzhi Dinullah <hifzhidinullah>
Ihsan Hidayat Rafi
Nabiel Aufi Danendra

Team background

- Academic Experience

  All team members just finished the 3rd year of Electrical Engineering, Institut Teknologi Bandung, Indonesia

- Work Experience

  None

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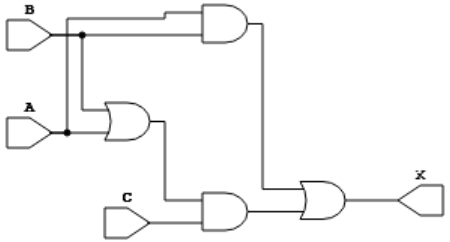
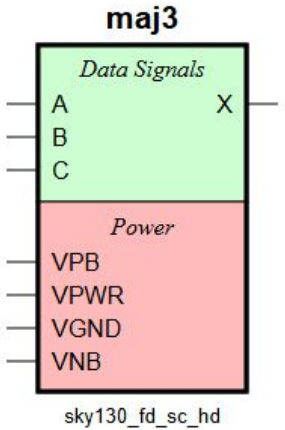
Project information

- Goal:
  - Create a layout of 3 input majority gate with 2x drive strength optimized for power and size efficiency
- Design:
  - Fulfill the logic function of X = AB + AC + BC
  - The circuit will be designed so that it have ideal dimension which be easily integrated into the GF180MCU ecosystem
- Application
  - Calculate the carry bit of a full adder
  - Error detection/correction circuit, used in TMR and fault tolerant designs
  - Can acts like a simple logic voting function





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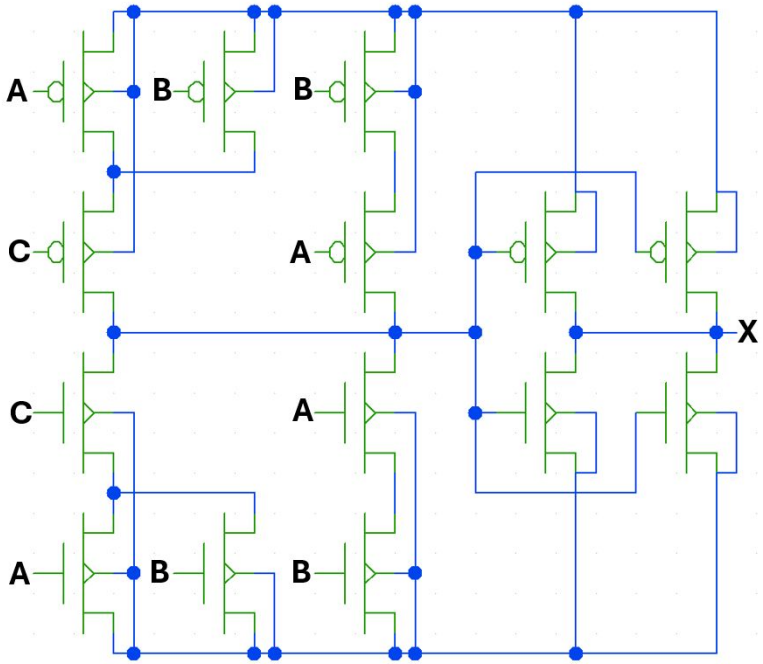

Parameter	Targeted Spec.
Drive Strength	2X
Track	9
VDD	3.3V
Area	≤ 75 μm²
Pin Capacitance	≤ 0.02 pf
Max Delay	≤ 0.5 ns
Leakage Power	≤ 0.5 nW

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Project Timeline

No	Task List	Week	Phase 2		Phase 3			Phase 4						
			July		August					September				
			29	30	31	32	33	34	35	36	37	38	39	40
1	Schematic Design and Simulation													
2	Layout Design, DRC + LVS, Post Layout Simulation													
3	Characterization													
4	Final Chip Review and Submission													

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Work Distribution

Name	Task
Hifzhi Dinullah	Schematic and layout design
Ihsan Hidayat Rafi	DRC + LVS, post-layout simulation
Nabiel Aufi Danendra	Optimization and characterization

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