Digital System Design with High-Level Synthesis in FPGA

HW/SW Setup: VivadoHLS+Vivado: Quiz Solution

www.highlevel-synthesis.com

- 1- These are the design tasks in the Xilinx Vivado-HLS software
 - Design capture
 - C-Simulation
 - HLS synthesis
 - Co-Simulation
 - and Package generation
- 2- These are the design tasks in the Xilinx Vivado software?
 - Design capture
 - RTL simulation
 - Logic synthesis
 - Implementation
 - and finally Bitstream generation