

# 1 Digital System Design with High-Level Synthesis in FPGA

If we have a look at the corresponding truth table of the two circuits, then it can be seen that they are opposite of each other.

L	R	U	D	Rule	EW	NS
0	0	0	0	5	1	0
0	0	0	1	4	0	1
0	0	1	0	4	0	1
0	0	1	1	3	0	1
0	1	0	0	2	1	0
0	1	0	1	2	1	0
0	1	1	0	2	1	0
0	1	1	1	3	0	1
1	0	0	0	2	1	0
1	0	0	1	2	1	0
1	0	1	0	2	1	0
1	0	1	1	3	0	1
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	0