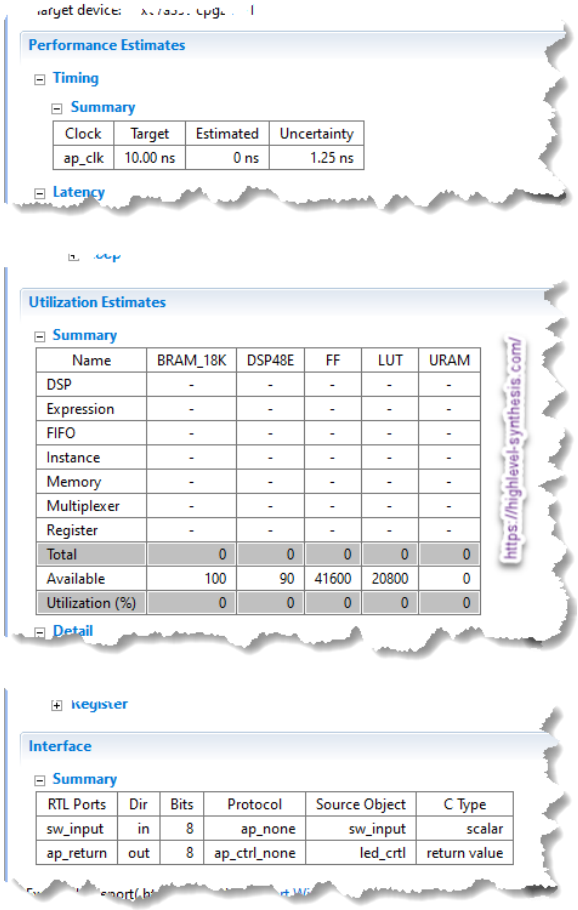
First, we should create a Vivado-HLS project and then create a source file and insert the design top-function.

Before synthesising the code, we should add port interfaces as follows:

```
unsigned char led_crtl(char sw_input) {
#pragma HLS INTERFACE ap_none port=sw_input
#pragma HLS INTERFACE ap_ctrl_none port=return
  return sw_input;
}
```

This figure shows parts of the synthesis report



Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	0 ns	1.25 ns

Latency

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	-	-	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	-	-
Register	-	-	-	-	-
Total	0	0	0	0	0
Available	100	90	41600	20800	0
Utilization (%)	0	0	0	0	0

Detail

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
sw_input	in	8	ap_none	sw_input	scalar
ap_return	out	8	ap_ctrl_none	led_crtl	return value