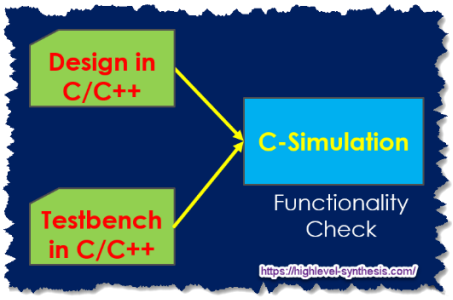
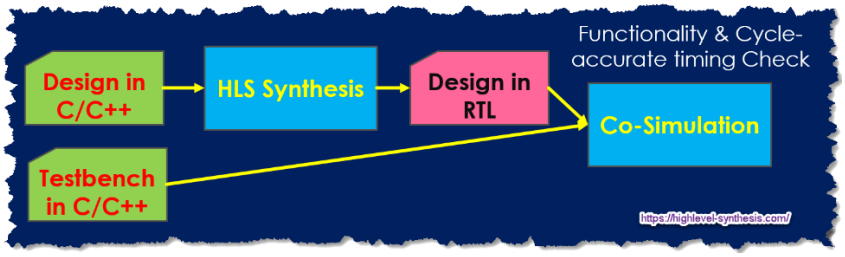
C-simulation: The C-simulation is used for checking the syntax, semantic and functional errors. It receives the C/C++ description of the design along with a testbench to apply some input data.



This simulation process ignores the HLS compiler directives, so it cannot check their correctness or efficiency.

Co-simulation: The co-simulation is used for checking the RTL design functional errors and cycle-accurate timing analysis. It receives the design in RTL along with a testbench in C/C++.



This simulation process can demonstrate the HLS compiler directive efficiency.