This file is a resource of the Udemy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF

We can use the codes in the previous lecture quiz solution and add proper pragmas as shown below

Case 1:

```
unsigned short int basic_output_16LED() {
#pragma HLS INTERFACE ap_ctrl_none port=return

	return 0b0000000011111111;

}
```

Case 2:

```
void basic_output_16LED(unsigned short int *led) {
#pragma HLS INTERFACE ap_ctrl_none port=return
#pragma HLS INTERFACE ap_none port=led

	*led = 0b0000000011111111;

}
```

Case 2:

```
void basic_output_16LED(unsigned short int &led) {
#pragma HLS INTERFACE ap_ctrl_none port=return
#pragma HLS INTERFACE ap_none port=led

	led = 0b0000000011111111;

}
```