

1 Digital System Design with High-Level Synthesis in FPGA

Integer Arithmetic-DSP Resource: Quiz-Solution

www.highlevel-synthesis.com

This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>

$$f = C + (A + D) * B$$

Figure 1 shows the dataflow graph of the above expression. To map this graph on the DSP shown in Figure 2, we should find the corresponding operators in the DSP and configure them to match with that of in the dataflow graph exactly.

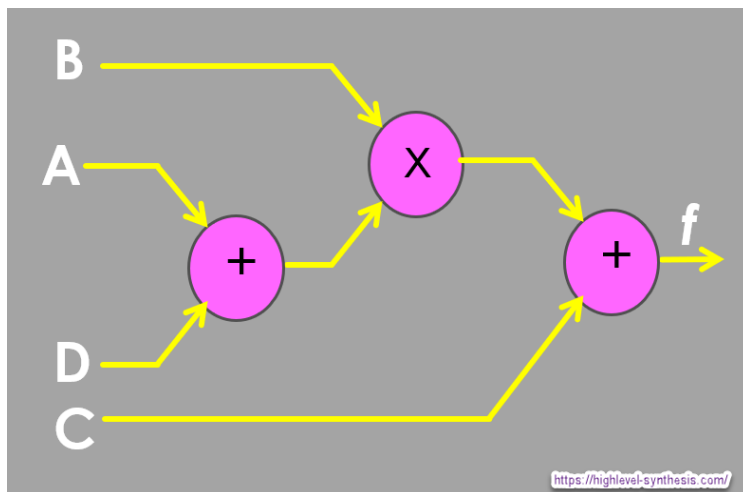


Figure 1

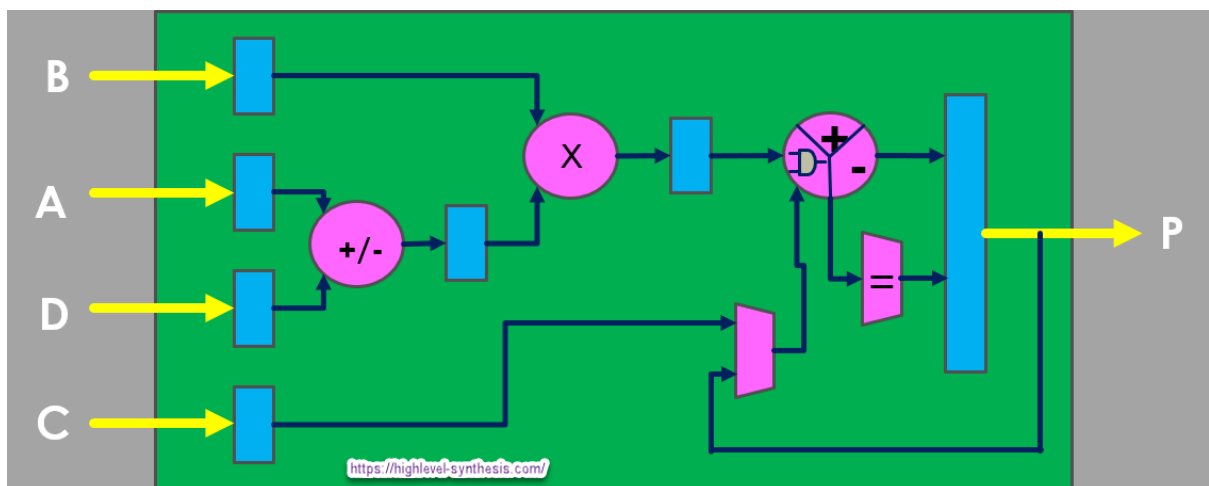


Figure 2

The solution is shown in Figure 3, in which the operators labelled with 1 & 2 should be configured to perform the addition operation.



Figure 3