

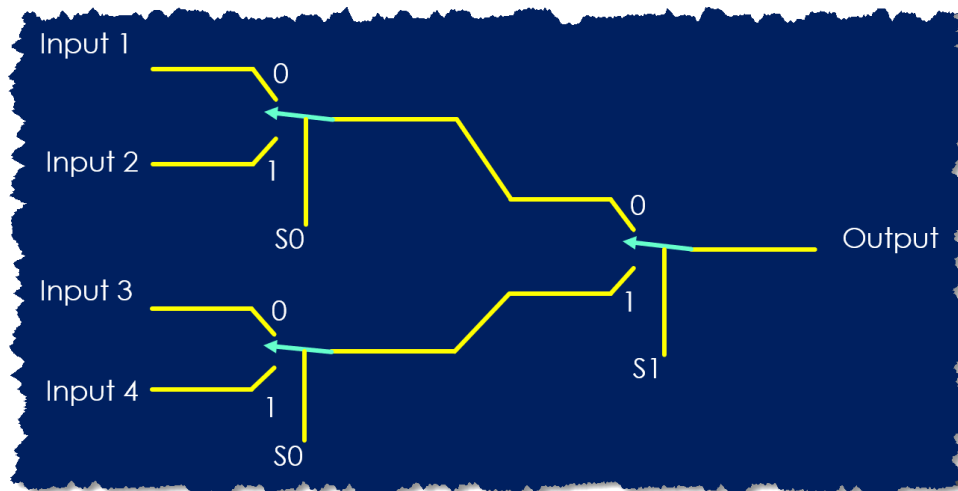
1 Digital System Design with High-Level Synthesis in FPGA

Conditional Statement-Definition: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>

As shown in the following figure, we can perform the selection among four options by using three switches and two selection bits.



This table shows the output corresponding to each value on the select bits.

S0	S1	Output
0	0	Input 1
0	1	Input 3
1	0	Input 2
1	1	Input 4