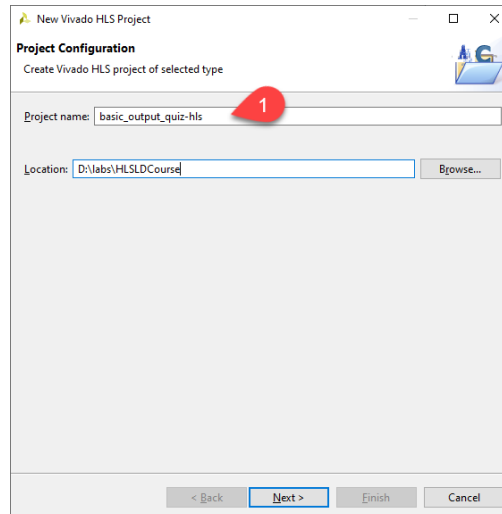
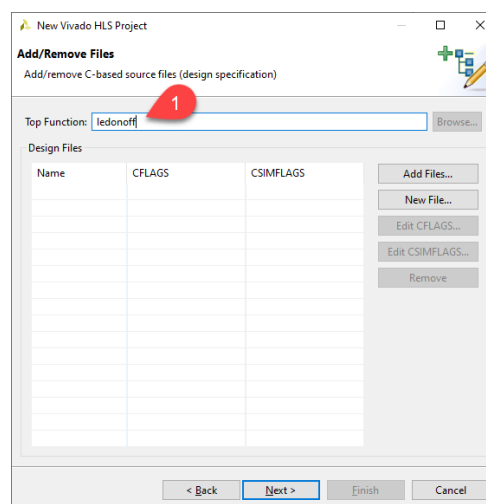


This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits  
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>

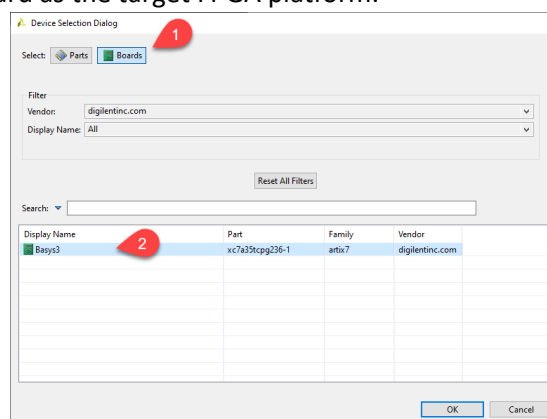
- 1- First, create a new project with the name shown in the figure



- 2- Choose "ledonoff" as the top-function name.

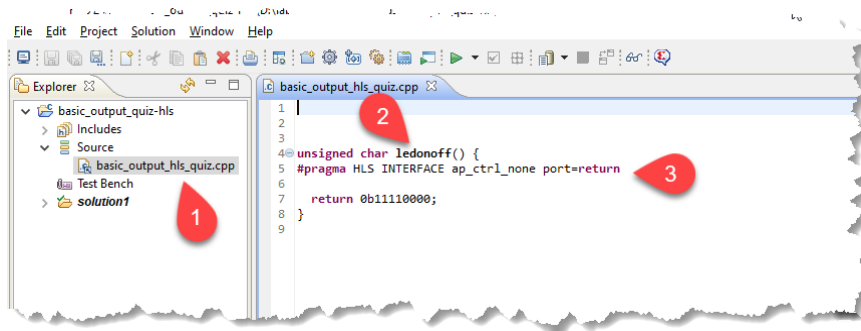


- 3- Choose the Basys3 board as the target FPGA platform.



## 2 Digital System Design with High-Level Synthesis in FPGA

- 4- Create a new file with the name of “basic\_output\_hls\_quiz.cpp” under the source folder in the Explorer view. Write the top function to the file and add the function block interface.



- 5- This figure shows part of the synthesis report.

