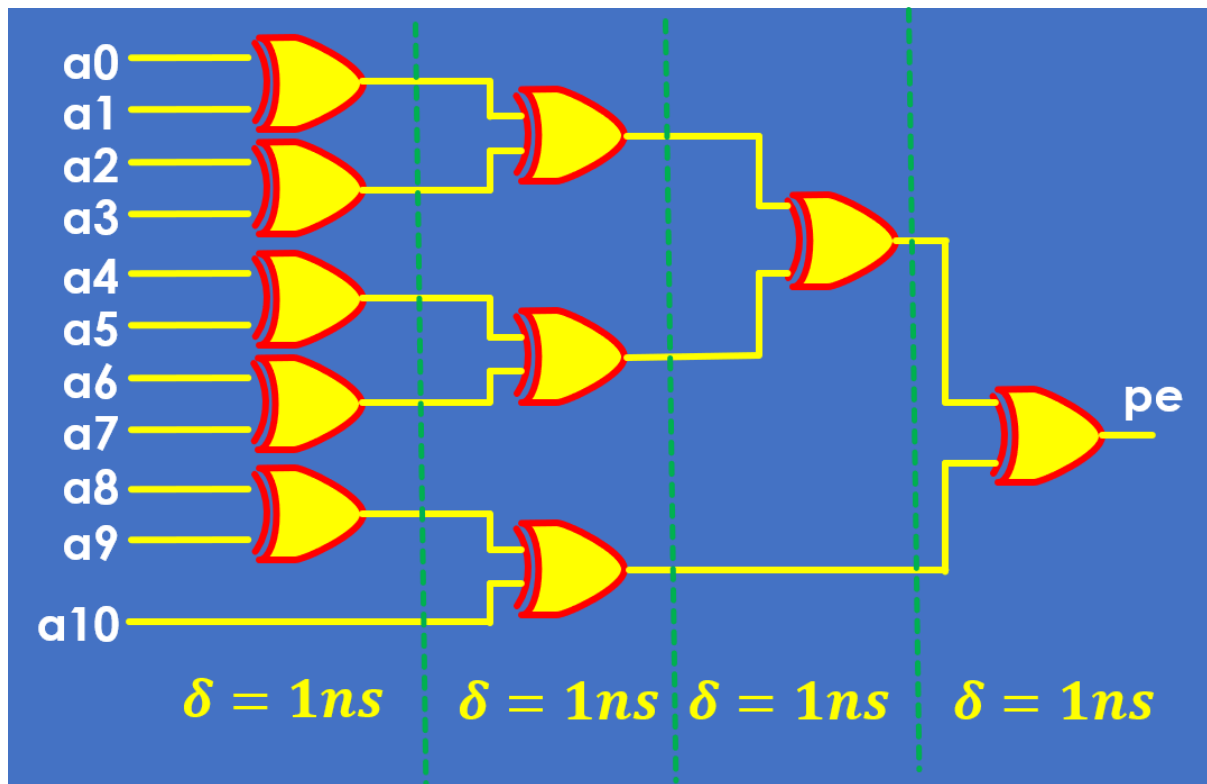


1 Digital System Design with High-Level Synthesis in FPGA

CombinationalLoop-ParityBit-Design: Quiz Answer

www.highlevel-synthesis.com



Design propagation delay = 4nsec