

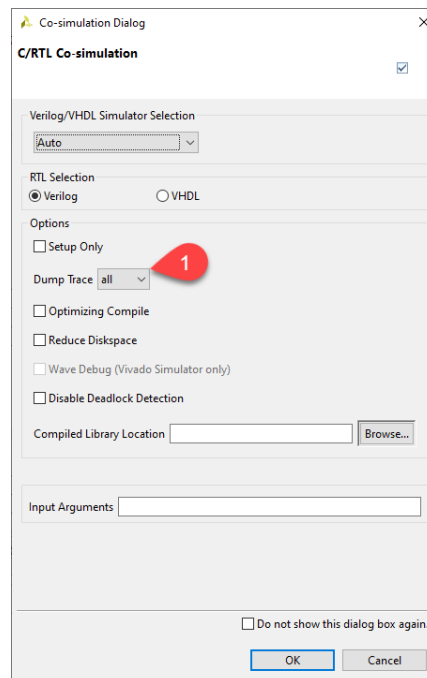
1 Digital System Design with High-Level Synthesis in FPGA

CC++ Testbench: Vivado-HLS Transcript

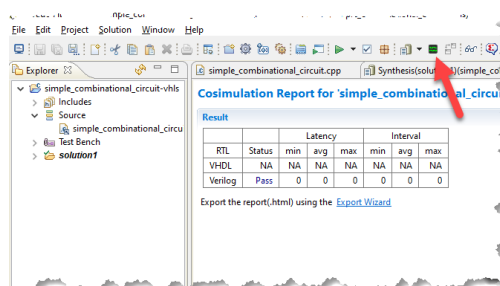
www.highlevel-synthesis.com

This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>

To see these extra signal, you should select the all option for the Dump Trace feature in “C/RTL Cosimulation” dialogbox, as shown in the following figure.

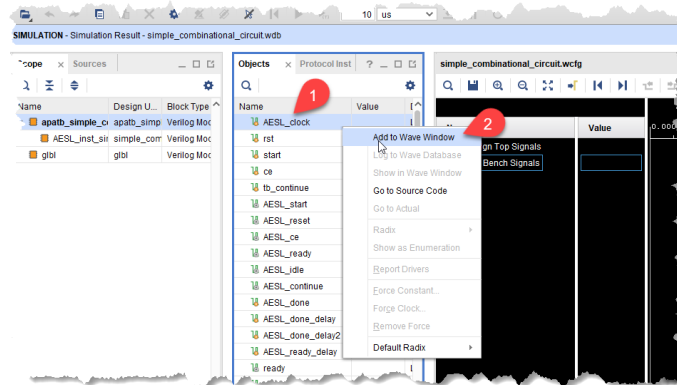


The open the waveform viewer

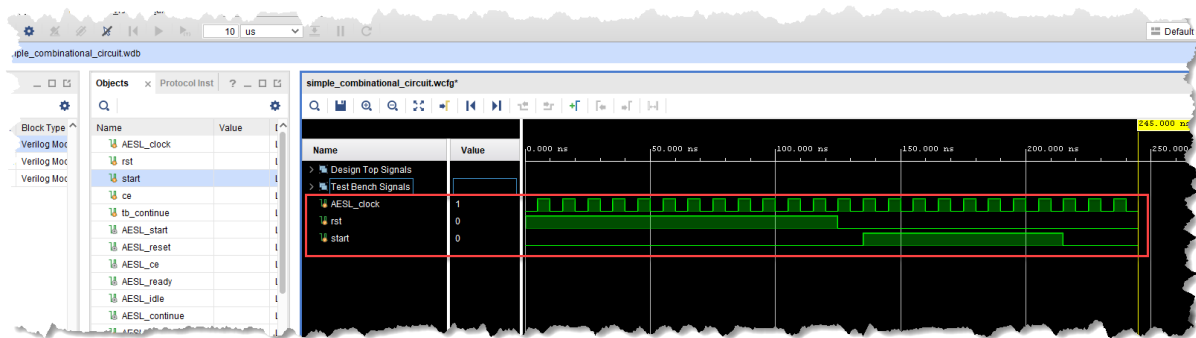


2 Digital System Design with High-Level Synthesis in FPGA

Then on the waveform viewer, right-click on the AESL_clock and select the “Add to Wave Window” option.



Do the same for rst, start signals.



Note that, these extra signals are not the design signals. These signals are part of the testbench environment that applies different test vectors to the design.