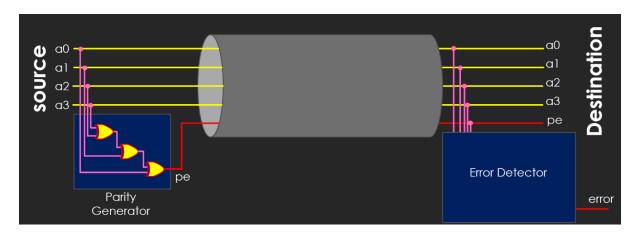
CombinationalLoop-ParityBit-Design: Quiz Solution

www.highlevel-synthesis.com

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The detector circuit should calculate the data prity again and compare that with the transmitted parity. An extra XOR gate can does this comparison. So the following figure shows the error detector.

