Data Type -Bit Precision Shift/Rotate: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the Udemy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits https://www.udemy.com/course/his-combinational-circuits/?referralCode=8D449A491B9F4582DDEF

```
ap_uint<13> r1, r2, r3;
ap_uint<7> v1 = 0x41;

r1 = v1 << 6;
r2 = ap_uint<13>(v1) << 6;
ap_int<7> v2 = -63;
r3 = v2 >> 4;

std::cout << " v1 = " << v1.to_string() << std::end1;
std::cout << " r1 = " << r1.to_string() << std::end1;
std::cout << " r2 = " << r2.to_string() << std::end1;
std::cout << " v2 = " << v2.to_string() << std::end1;
std::cout << " v2 = " << v2.to_string() << std::end1;
std::cout << " v2 = " << v2.to_string() << std::end1;
std::cout << " v3 = " << r3.to_string() << std::end1;</pre>
```

## The output of above code is

```
aunable to 🐪 afford a Warning. . . . of 🔊 le.
Vivado HLS Console
In file included from D:/Xilinx/Vivado/2020.1/include/hls_fpo.h:186:0
               from D:/Xilinx/Vivado/2020.1/include/hls_half.h:44
               from D:/Xilinx/Vivado/2020.1/include/etc/ap_privat
               from D:/Xilinx/Vivado/2020.1/include/ap common.h:641
               from D:/Xilinx/Vivado/2020.1/include/ap_int.h:54,
               from ../../bitprecision initialisation.h:4,
               from ../../bitprecision initialisation-tb.h:3,
               from ../../bitprecision initialisation-tb.cpp:1:
D:/Xillinx/Vivado/2020.1/include/floating point v7 0 bitacc_cmodel.h:1
#define GMP_LIBGMP_DLL 1
 v1 = 0b1000001
 r1 = 0b01000000
r2 = 0b1000001000000
v2 = 0b1000001
r3 = 0b1111111111100
INFO: [SIM 211-1] CSim done with 0 errors.
Finished C simulation.
```