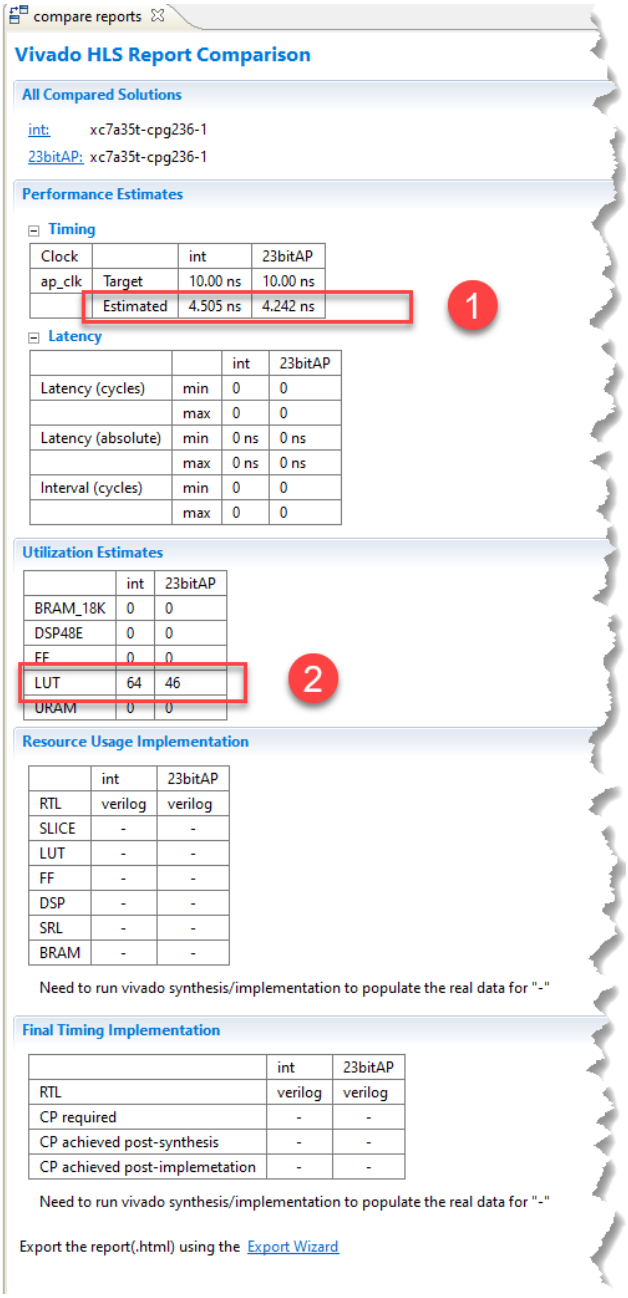
The main differences between the synthesis reports of two design are highlighted in the following figure.



compare reports

Vivado HLS Report Comparison

All Compared Solutions

int: xc7a35t-cpg236-1
23bitAP: xc7a35t-cpg236-1

Performance Estimates

Timing

Clock		int	23bitAP
ap_clk	Target	10.00 ns	10.00 ns
	Estimated	4.505 ns	4.242 ns

1

Latency

		int	23bitAP
Latency (cycles)	min	0	0
	max	0	0
Latency (absolute)	min	0 ns	0 ns
	max	0 ns	0 ns
Interval (cycles)	min	0	0
	max	0	0

Utilization Estimates

	int	23bitAP
BRAM_18K	0	0
DSP48E	0	0
FF	0	0
LUT	64	46
URAM	0	0

2

Resource Usage Implementation

	int	23bitAP
RTL	verilog	verilog
SLICE	-	-
LUT	-	-
FF	-	-
DSP	-	-
SRL	-	-
BRAM	-	-

Need to run vivado synthesis/implementation to populate the real data for "-"

Final Timing Implementation

	int	23bitAP
RTL	verilog	verilog
CP required	-	-
CP achieved post-synthesis	-	-
CP achieved post-implemetation	-	-

Need to run vivado synthesis/implementation to populate the real data for "-"

Export the report(.html) using the Export Wizard

1) The design with 23-bit arbitrary-precision data type is faster as its propagation delay is lower than the other implementation.
2) The design with 23-bit arbitrary-precision data type utilises less resources, here LUTs.