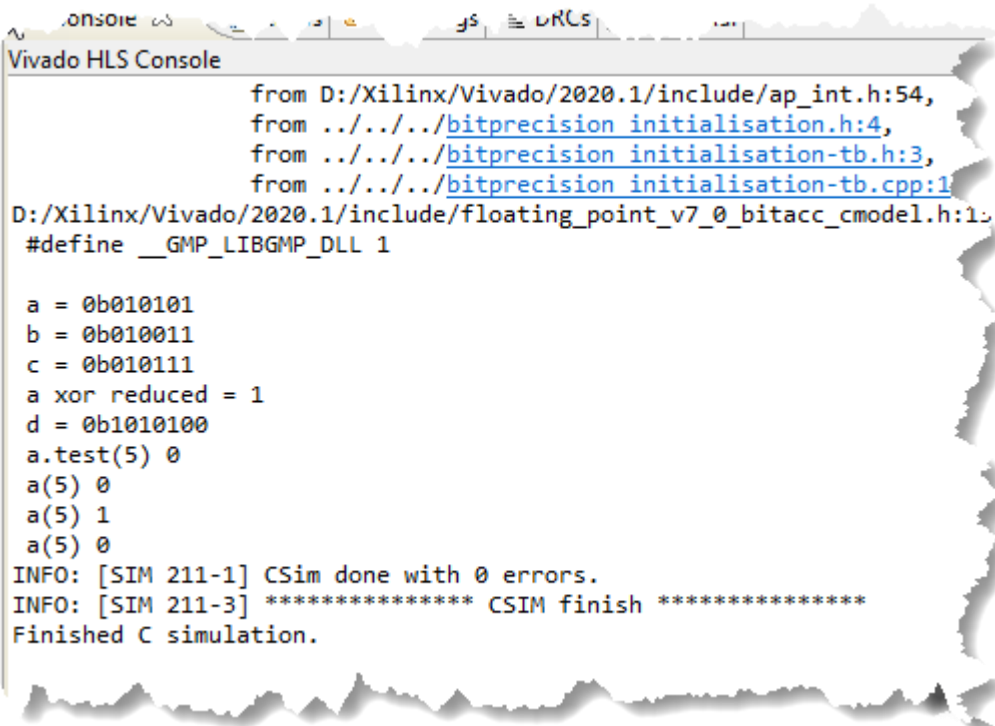


1 Digital System Design with High-Level Synthesis in FPGA

This is the output of the code

A screenshot of the Vivado HLS Console window. The window title is "Vivado HLS Console". The console displays the output of a C simulation. It shows several include paths at the top, followed by a preprocessor directive. Then, it shows the initialization of variables a, b, c, and d with binary values. It also shows the result of a XOR operation and the output of a test function. The simulation ends with an INFO message indicating it was completed successfully.

```
Vivado HLS Console
from D:/Xilinx/Vivado/2020.1/include/ap_int.h:54,
from ../../../../bitprecision_initialisation.h:4,
from ../../../../bitprecision_initialisation-tb.h:3,
from ../../../../bitprecision_initialisation-tb.cpp:1
D:/Xilinx/Vivado/2020.1/include/floating_point_v7_0_bitacc_cmodel.h:1:
#define __GMP_LIBGMP_DLL 1

a = 0b010101
b = 0b010011
c = 0b010111
a xor reduced = 1
d = 0b1010100
a.test(5) 0
a(5) 0
a(5) 1
a(5) 0
INFO: [SIM 211-1] CSim done with 0 errors.
INFO: [SIM 211-3] ***** CSIM finish *****
Finished C simulation.
```