

1 Digital System Design with High-Level Synthesis in FPGA

If we consider the default design clock period, as shown in Figure 1, and synthesis the code, then Figure 2 shows the synthesis report. In addition, Figure 3 depicts the design execution schedule taken from the analysis perspective.

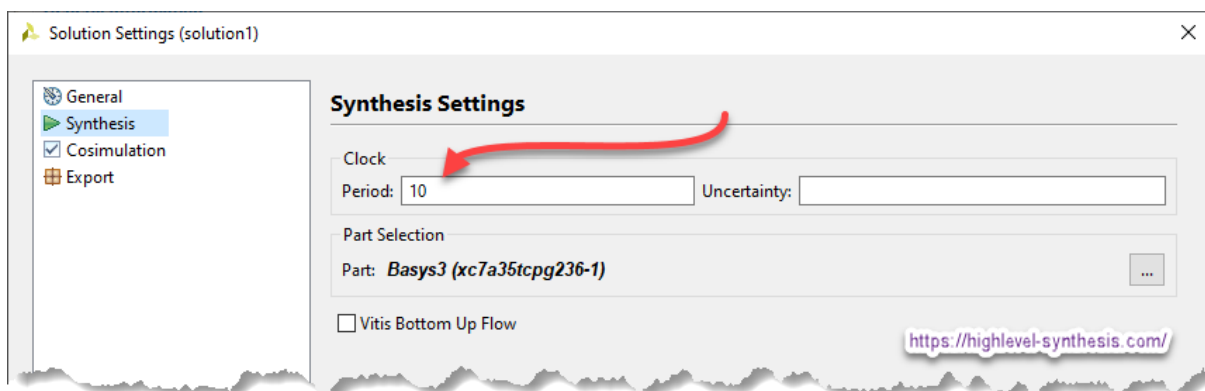


Figure 1

As can be seen, the design requires three steps to finish. Moreover, each step takes about 10ns. According to the label 2 in Figure 2, the design latency is 30ns. Therefore, if we change the design clock period from 10 to 30 (as shown in Figure 4), we should expect to have a fully combinational circuit.

The synthesis report in the last figure confirms that.

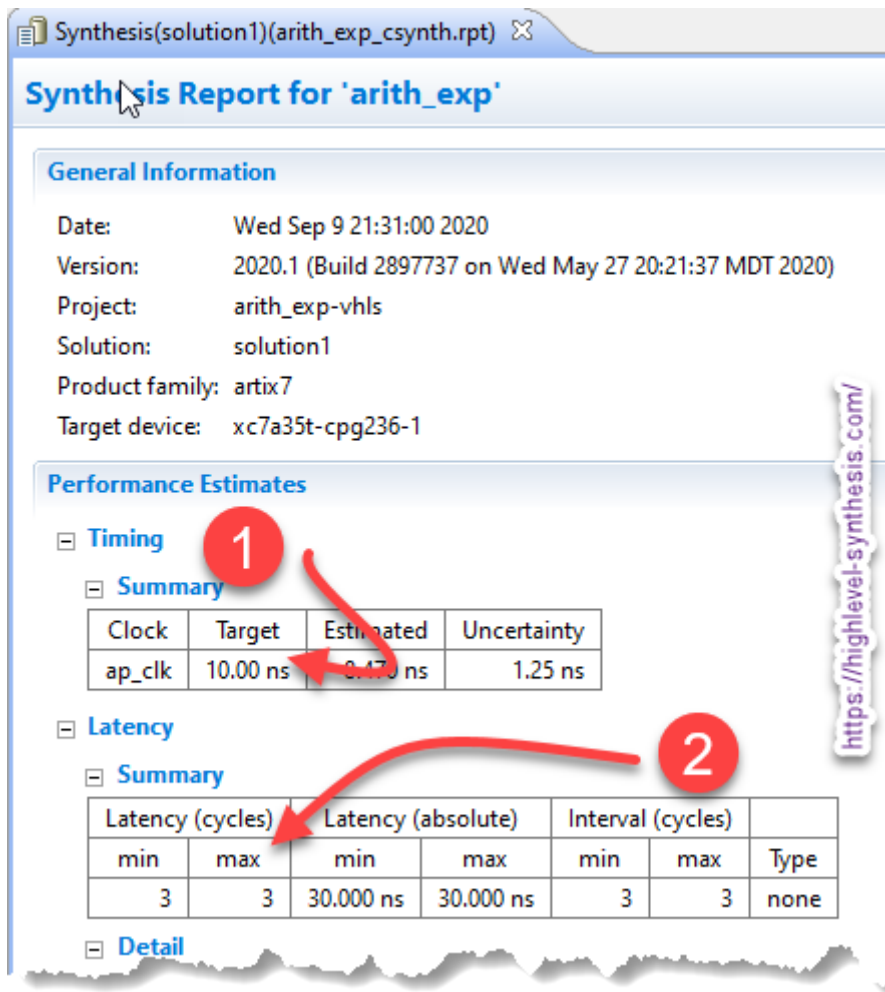


Figure 2 1) design clock period 10ns 2) design requires 3 cycles to finish

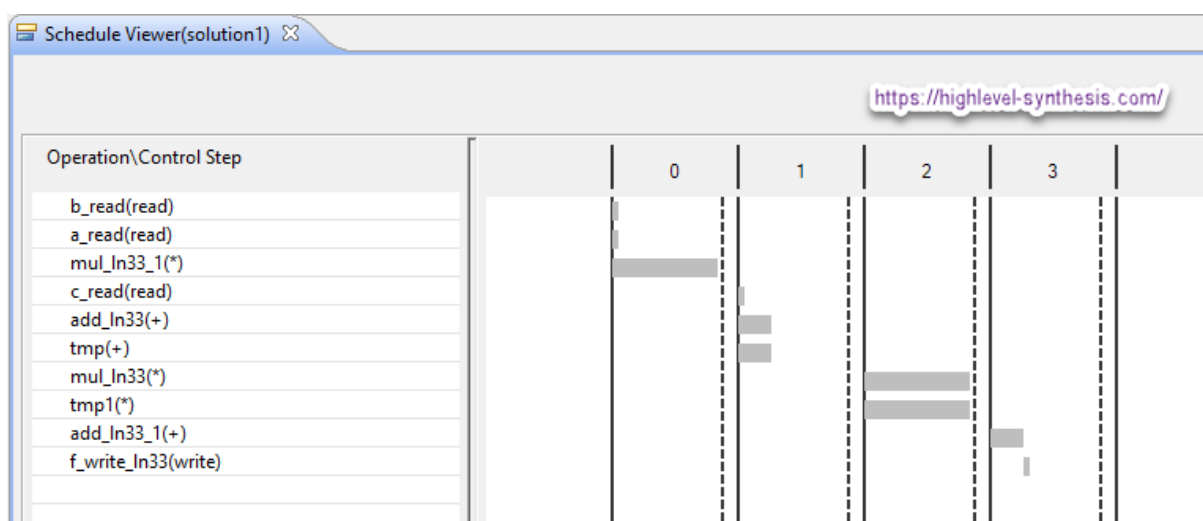


Figure 3

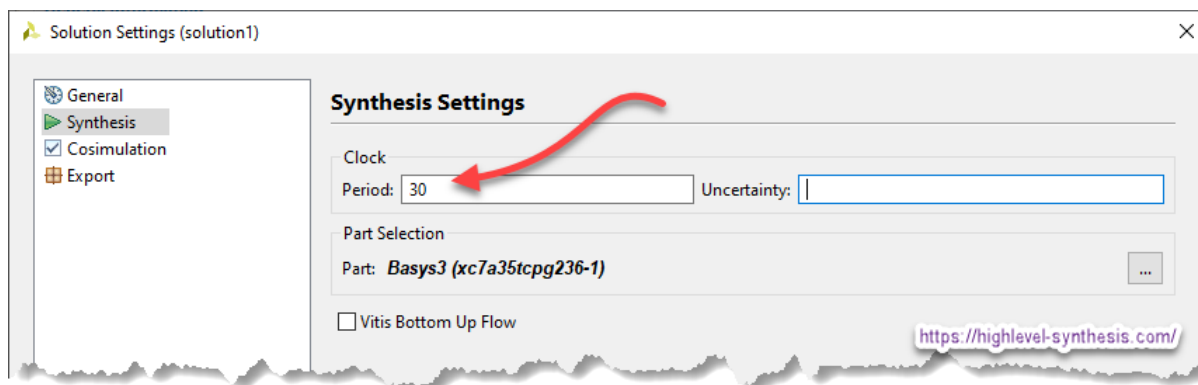


Figure 4

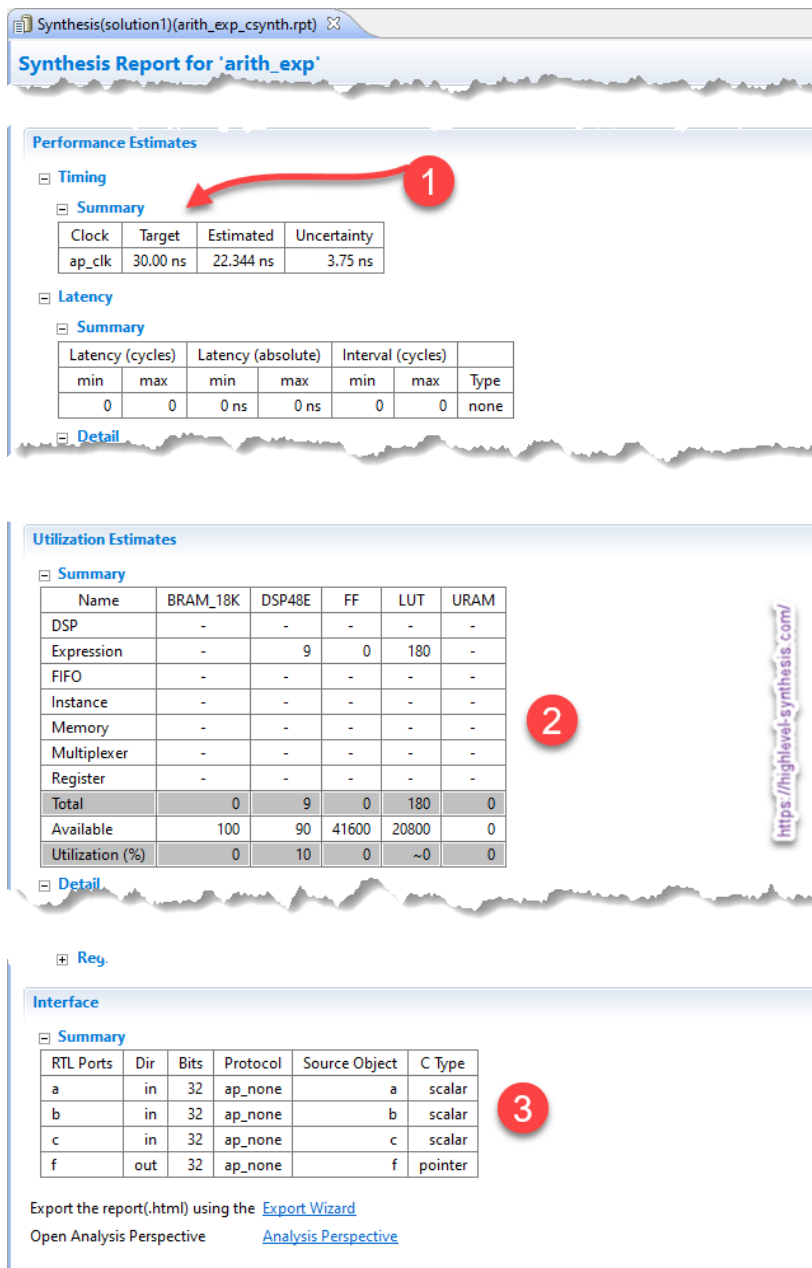


Figure 5 1) design clock period = 30ns, 2) no memory cell 3) only top-function arguments among the ports