## Digital System Design with High-Level Synthesis in FPGA

CombinationalLoop-ParityBit-Definition: Quiz Solution

www.highlevel-synthesis.com

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1-

data	(count of 1-bits)	Parity bit	
		pe	ро
0110101101001	7	1	0
0111101111101	10	0	1

## 2-

- 1- This data is erroneous as the number of ones in the data is 9, so then even parity should be 1, but it is 0.
- 2- This one also has an error as the number of ones is 7, so the odd-parity bit should be 0 but it is 1.