## Digital System Design with High-Level Synthesis in FPGA

HW/SW Setup: VivadoHLS+Vivado: Quiz Solution www.highlevel-synthesis.com

This file is a resource of the Udemy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF

- 1- These are the design tasks in the Xilinx Vivado-HLS software
  - Design capture
  - C-Simulation
  - HLS synthesis
  - Co-Simulation
  - and Package generation
- 2- These are the design tasks in the Xilinx Vivado software?
  - Design capture
  - RTL simulation
  - Logic synthesis
  - Implementation
  - and finally Bitstream generation