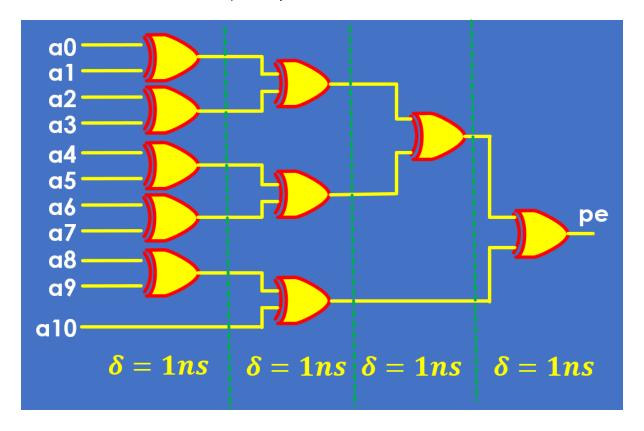
CombinationalLoop-ParityBit-Design: Quiz Answer

www.highlevel-synthesis.com

This file is a resource of the Udemy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF



Design propagation delay = 4nsec