

1 Digital System Design with High-Level Synthesis in FPGA

1-

int7 a7 = -3;



int10 a10 = a7;



uint7 b7 = 125;



uint10 b10 = a7;



2-

ap_uint<10> ua10, ub10;

ap_int<7> a7 = 0x71;



ap_uint<6> ua6 = 0x31;



ua10 = ua6;



ub10 = a7;



3-

uint10 ua10 = 5;



int7 a7 = -8;



uint13 ua13 = ua10+a7;



4-

uint10 ua10 = 5;



int7 a7 = -8;



uint13 ua13 = ua10+(uint7)a7;



5-

```

#include <ap_int.h>

void single_perceptron_nn (
    ap_int<8> x1,
    ap_int<8> x2,
    ap_int<8> x3,

    float w1,
    float w2,
    float w3,

    float b,

    bool &y) {
#pragma HLS INTERFACE ap_ctrl_none port=return

#pragma HLS INTERFACE ap_none port=x1
#pragma HLS INTERFACE ap_none port=x2
#pragma HLS INTERFACE ap_none port=x3

#pragma HLS INTERFACE ap_none port=w1
#pragma HLS INTERFACE ap_none port=w2
#pragma HLS INTERFACE ap_none port=w3

#pragma HLS INTERFACE ap_none port=b

#pragma HLS INTERFACE ap_none port=y

    float s = w1*x1 + w2*x2 + w3*x3 + b;

    if (b >= 0) {
        y = 1;
    } else {
        y = 0;
    }
}

```