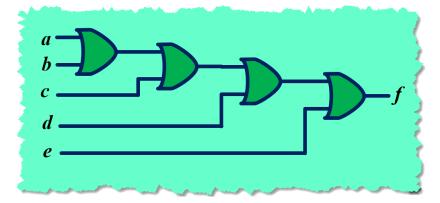
DataType-Synthesis: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the Udemy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits https://www.udemy.com/course/his-combinational-circuits/?referralCode=8D449A491B9F4582DDEF

The following graph represents the function before synthesis. It consists of four gates scheduled in four levels.



If we synthesis the code for performance (which is the default assumption in Vivado-HLS), then the following graph represents the function. It consists of four gates organised into three levels.

