Basic-Output Vivado-LAB: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the Udemy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits https://www.udemy.com/course/his-combinational-circuits/?referralCode=8D449A491B9F4582DDEF

## The original port name was o\_0[7:0]. So, the modified constraints are as follows

```
## LEDs
set_property PACKAGE_PIN U16 [get_ports {o_0[0]}]
        set property IOSTANDARD LVCMOS33 [get ports {o 0[0]}]
set_property PACKAGE_PIN E19 [get_ports {o_0[1]}]
        set property IOSTANDARD LVCMOS33 [get_ports {o 0[1]}]
set_property PACKAGE_PIN U19 [get_ports {o_0[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {o_0[2]}]
set property PACKAGE PIN V19 [get ports {o 0[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {o_0[3]}]
set_property PACKAGE_PIN W18 [get_ports {o_0[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {o_0[4]}]
set_property PACKAGE_PIN U15 [get_ports {o_0[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {o_0[5]}]
set property PACKAGE PIN U14 [get ports {o 0[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {o_0[6]}]
set_property PACKAGE_PIN V14 [get_ports {o_0[7]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {o_0[7]}]
```