

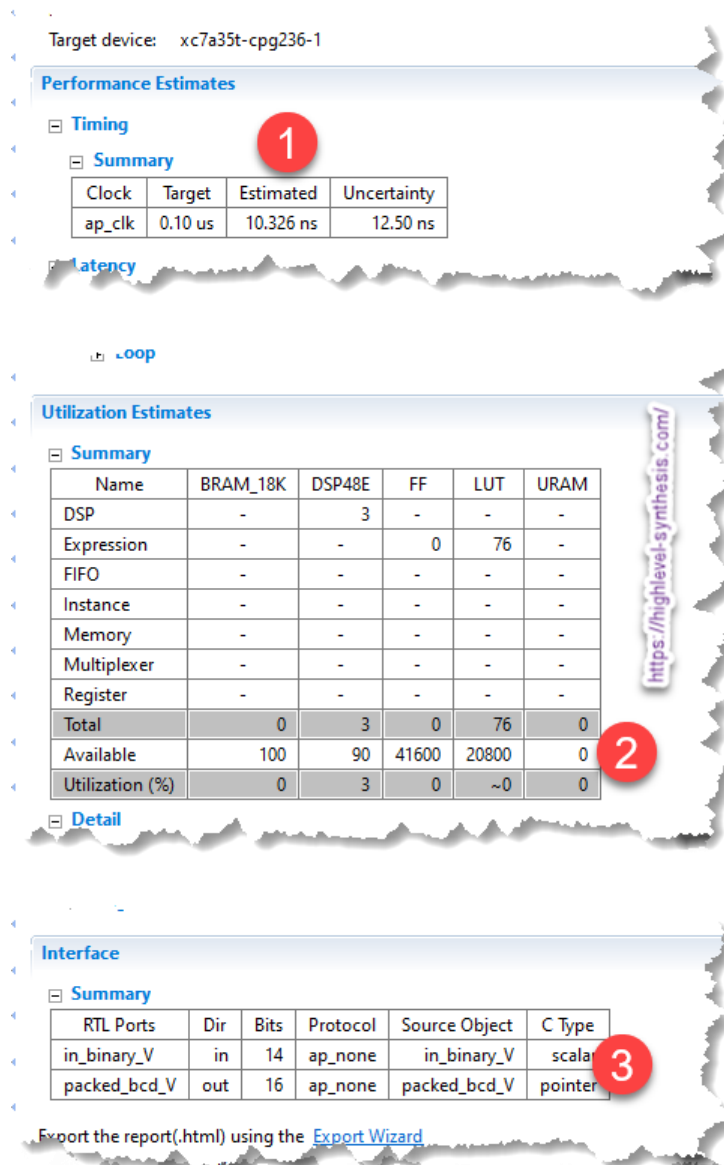
1 Digital System Design with High-Level Synthesis in FPGA

7Segment: BCD TO 7segment-Div/Mod: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>

The complete source code, including the test bench, can be found at the resources folder of this lecture. And the following figure shows the Vivado-HLS synthesis report



- 1) The design propagation delay is about 10.326 ns
- 2) The RTL hardware uses 3 DSP and 76 LUTs
- 3) The design has only two ports corresponding to the top-function arguments