

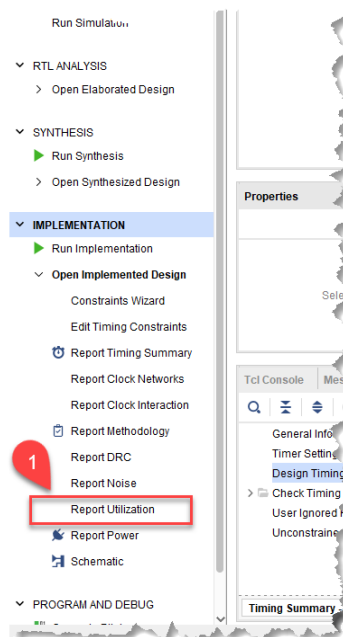
1 Digital System Design with High-Level Synthesis in FPGA

ComCircuit-Traffic Light: Quiz Solution

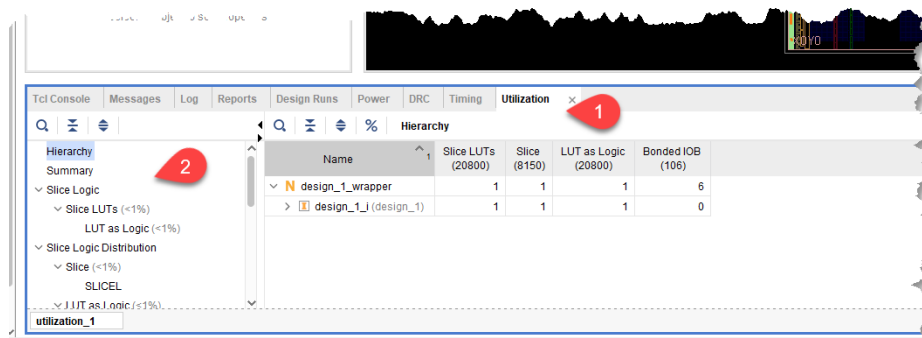
www.highlevel-synthesis.com

This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>

To find the resource utilisation of the final design in Vivado, click on the “Implementation→Open Implemented Design→Report Utilization” option in the Flow Navigator.



The Utilization tab will appear in the bottom area which contains resource utilisation details.



If you click on the Summary link, then the resource utilisation summary is shown in a table and by a graph.

