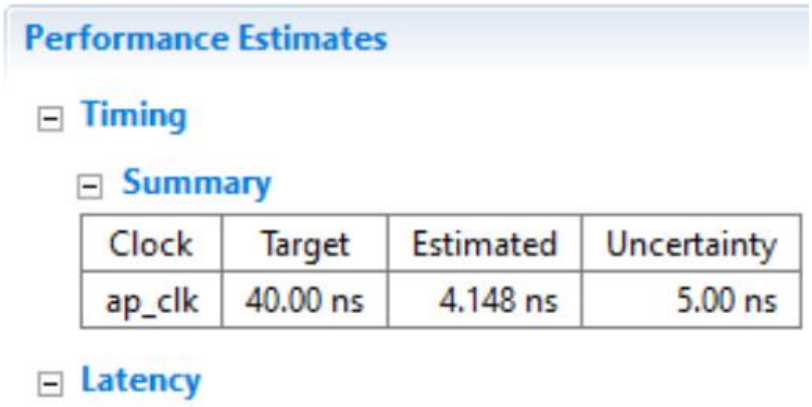
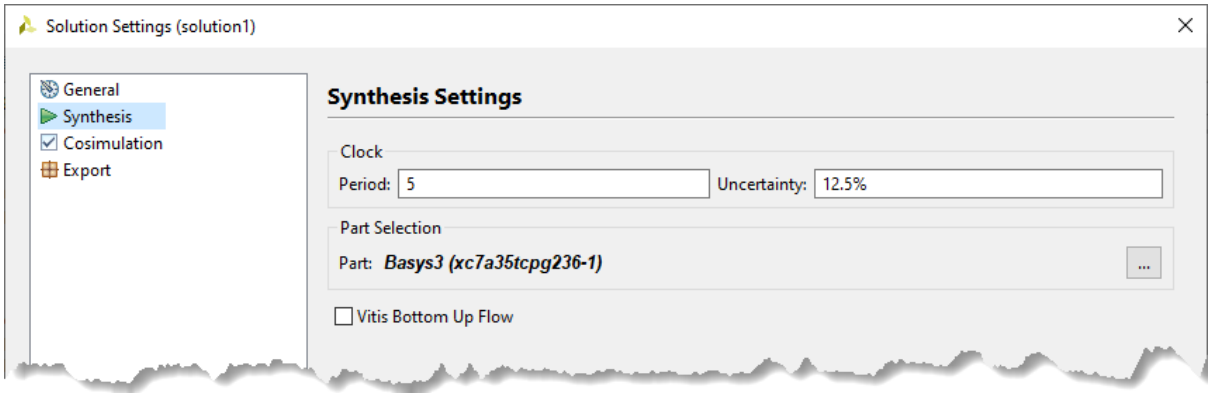
Our first implementation used the following expression

$$r = a\%n;$$

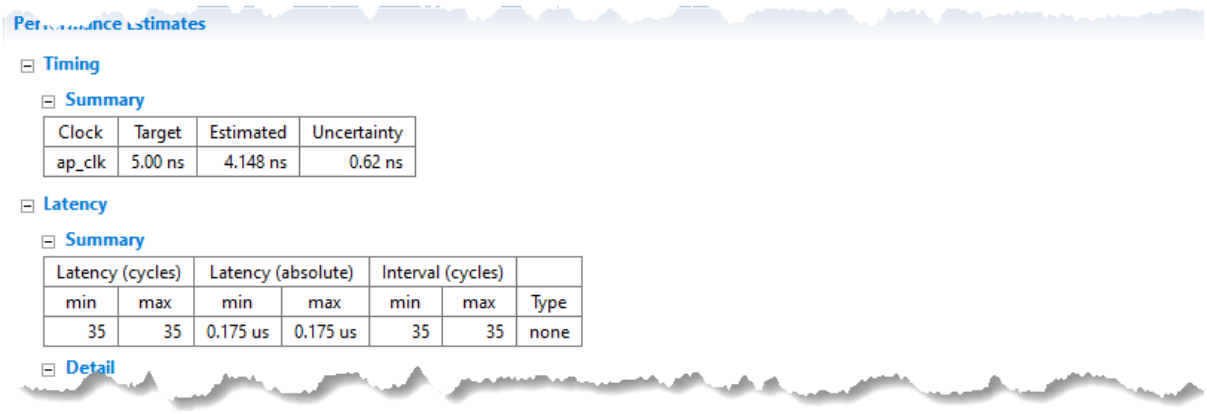
The resulted hardware was not fully combinational and required multiple stage to complete. According to the synthesis report shown in the lecture, the estimated clock period (or the timing of a single stage) is $4.148\ ns$.



Therefore, the design clock period constraint can be reduced to $5\ ns$.



The following figure shows the timing report after synthesising the code with this constraint.



Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00 ns	4.148 ns	0.62 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
35	35	0.175 us	0.175 us	35	35	none

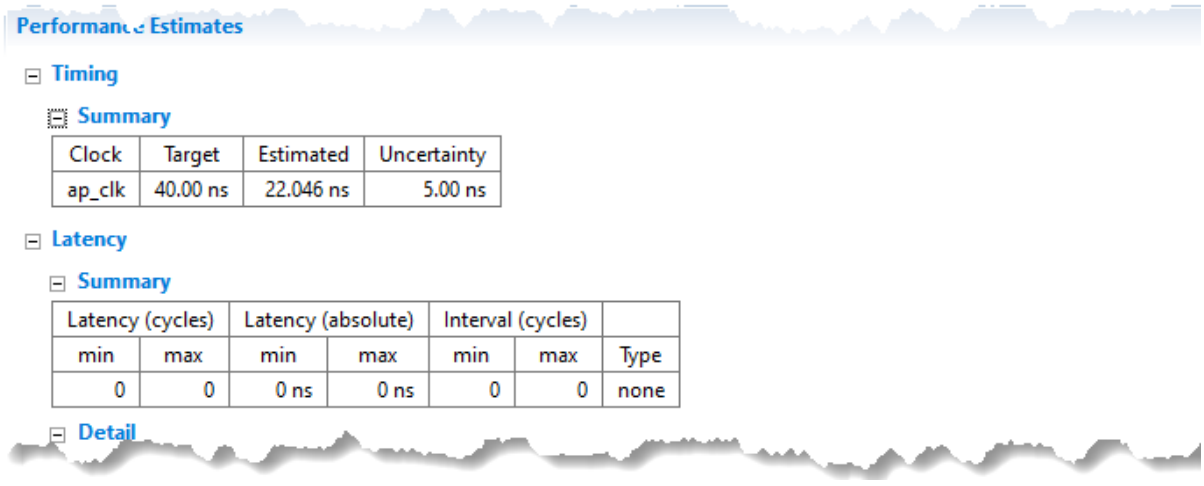
Detail

Therefore, the latency of the whole design (or propagation delay) is about $0.175\ \mu s$.

The second implementation was based on this expression

$$r = a - n * divbyconstant(a);$$

The following figure shows the timing report after synthesising the code.



Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	40.00 ns	22.046 ns	5.00 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
0	0	0 ns	0 ns	0	0	none

Detail

As the circuit is combinational, it needs only one stage to complete. Therefore, based on the above figure the propagation delay or the design latency is $22.046\ ns$.