Digital System Design with High-Level Synthesis in FPGA

Data Type – Bit Precision-Print: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the Udemy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF

The following figure shows the output of the code

```
💚 🖳 Errors | 🎂 Warnings | 📜 DRUS 🐶 Terminal
Vivado HLS Console
             from D:/Xilinx/Vivado/2020.1/include/etc/ap_private.h:90,
             from D:/Xilinx/Vivado/2020.1/include/ap_common.h:641,
             from D:/Xilinx/Vivado/2020.1/include/ap_int.h:54,
             from ../../bitprecision initialisation.h:4,
             from ../../bitprecision initialisation-tb.h:3,
             from ../../bitprecision initialisation-tb.cpp:1:
D:/Xilinx/Vivado/2020.1/include/floating_point_v7_0_bitacc_cmodel.h:135:0: note: this is the
 #define __GMP_LIBGMP_DLL 1
a in octal = 000416777773345651416625031020
a in decimal = 1279761234872144636424720
a in hexadecimal = 0x010EFFFEDCBA9876543210
a = 000416777773345651416625031020
a = 1279761234872144636424720
a = 0x010EFFFEDCBA9876543210
INFO: [SIM 211-1] CSim done with 0 errors.
Finished C simulation.
```