Digital System Design with High-Level Synthesis in FPGA

Combinational Circuit-Functions: Quiz Solution

www.highlevel-synthesis.com

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We only need to turn off the automatic inlining feature by using the related pragma.

```
bool or_gate(bool a, bool b) {
#pragma HLS INLINE off
   return (a | b);
}

bool not_gate(bool a) {
#pragma HLS INLINE off
   return !a;
}

void automatic_inlining(bool a, bool b, bool *c ) {
#pragma HLS INTERFACE ap_ctrl_none port=return
#pragma HLS INTERFACE ap_none port=a
#pragma HLS INTERFACE ap_none port=b
#pragma HLS INTERFACE ap_none port=c

*c = or_gate(not_gate(a), not_gate(b));
}
```