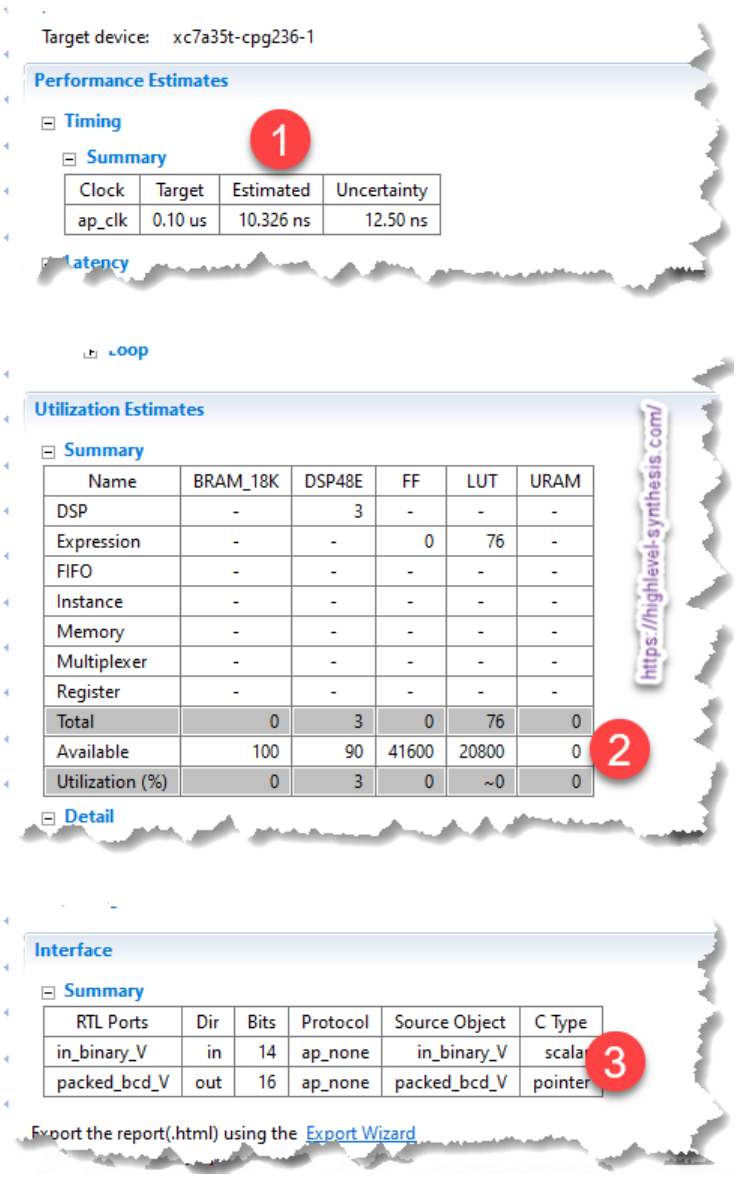
The complete source code, including the test bench, can be found at the resources folder of this lecture. And the following figure shows the Vivado-HLS synthesis report



1) The design propagation delay is about 10.326 ns
2) The RTL hardware uses 3 DSP and 76 LUTs
3) The design has only two ports corresponding to the top-function arguments