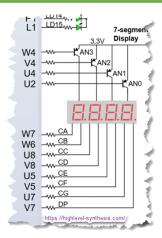
## Digital System Design with High-Level Synthesis in FPGA

7Segment-Basis3: Quiz Solution

www.highlevel-synthesis.com



To enable the left-hand side display, we should apply 0 on W4 pin

To disable the others, V4, U4 and U2 should receive the logic value 1.

And the code on the data pins is 0b10010010

