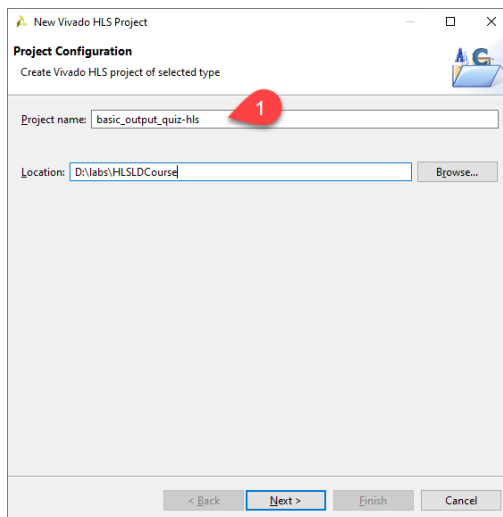
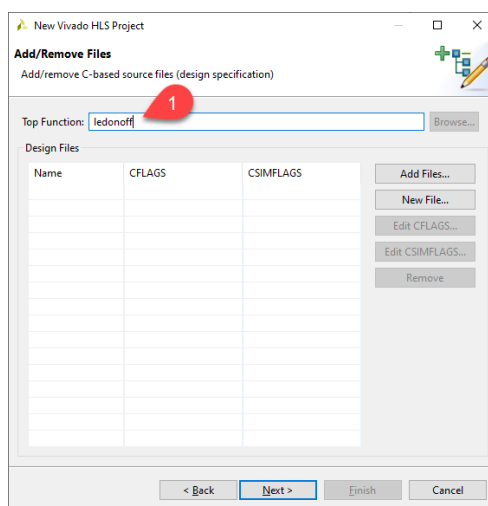


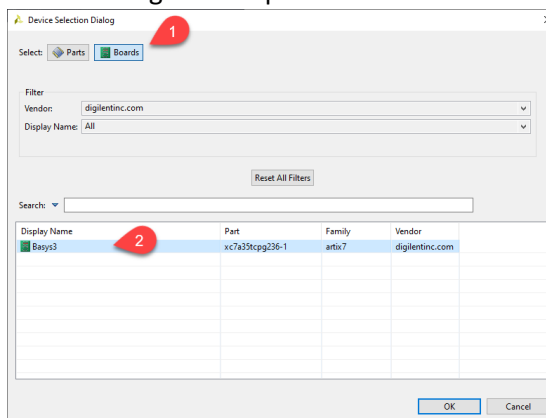
- 1- First, create a new project with the name shown in the figure



- 2- Choose "*ledonoff*" as the top-function name.

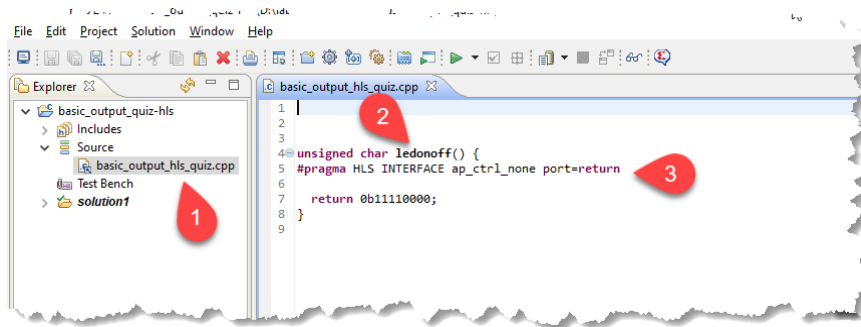


- 3- Choose the Basys3 board as the target FPGA platform.



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- 4- Create a new file with the name of “basic_output_hls_quiz.cpp” under the source folder in the Explorer view. Write the top function to the file and add the function block interface.



- 5- This figure shows part of the synthesis report.

