

1 Digital System Design with High-Level Synthesis in FPGA

Combinational Circuit: HLS: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>

This code shows how to add the HLS pragmas to the code.

```
bool simple_combinational_circuit(  
    bool a,  
    bool b,  
    bool c  
) {  
#pragma HLS INTERFACE ap_ctrl_none port=return  
#pragma HLS INTERFACE ap_none port=a  
#pragma HLS INTERFACE ap_none port=b  
#pragma HLS INTERFACE ap_none port=c  
  
    return (a && b) || !c;  
}
```