Digital System Design with High-Level Synthesis in FPGA
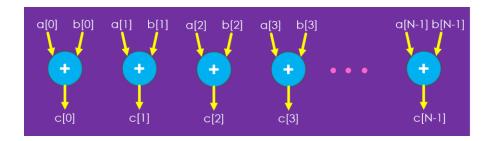
Combinational Loop Definition: Quiz Solution   www.highlevel-synthesis.com

A *for*-loop can represent this dataflow graph. However, to execute iterations in parallel, adding the unrolling compiler directive is required.

```
1       for (int i = 0; i < N; i++) {
2   #pragma HLS UNROLL
3           c[i] = a[i] + b[i];
4       }
```