Digital System Design with High-Level Synthesis in FPGA

Data Type – Bit Precision-Bitlevel: Quiz Solution

www.highlevel-synthesis.com

As b has 5 bits and p(3, 0) has 4 bits, then we expect that r has at least 5+4=9 bits.

```
ap_uint<9> p = 0xef;
ap_int<5> b = 0x3;
ap_int<9> r = (p(3,0), b);
```

The output would be

p = 0b011101111 b = 0b011

r = 0b111100011

