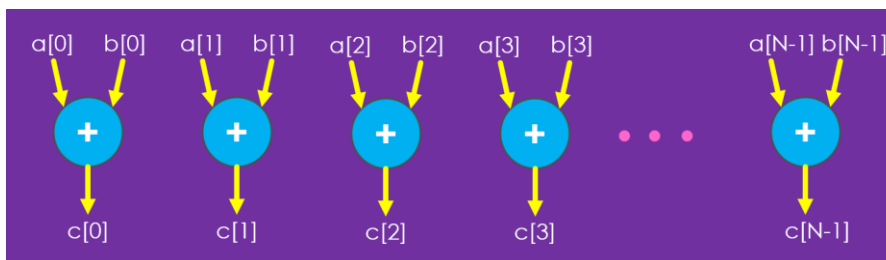


This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>



A *for*-loop can represent this dataflow graph. However, to execute iterations in parallel, adding the unrolling compiler directive is required.

```
1 |   for (int i = 0; i < N; i++) {  
2 |   #pragma HLS UNROLL  
3 |       c[i] = a[i] + b[i];  
4 |   }
```