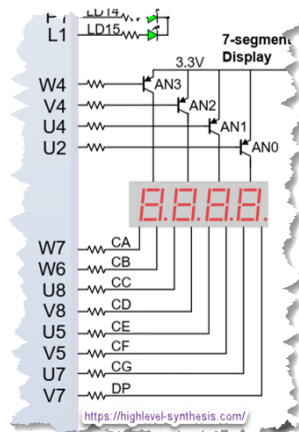


1 Digital System Design with High-Level Synthesis in FPGA

7Segment-Basis3: Quiz Solution

www.highlevel-synthesis.com

This file is a resource of the UdeMy course: Digital System Design with High-Level Synthesis for FPGA: Combinational Circuits
<https://www.udemy.com/course/hls-combinational-circuits/?referralCode=8D449A491B9F4582DDEF>



To enable the left-hand side display, we should apply 0 on W4 pin

To disable the others, V4, U4 and U2 should receive the logic value 1.

And the code on the data pins is 0b10010010

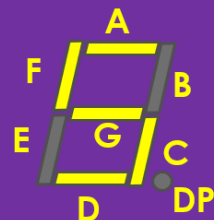
Control
Signals

U2	U4	V4	W4
1	1	1	0

0b1110

Data
Signals

DP	CG	CF	CE	CD	CC	CB	CA
V7	U7	V5	U5	V8	U8	W6	W7
1	0	0	1	0	0	1	0



<https://highlevel-synthesis.com/>